Ville Naumanen

MULTILEVEL CONVERTER MODULATION: IMPLEMENTATION AND ANALYSIS

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Abstract

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Multilevel converter modulation: implementation and analysis

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Multilevel converters provide an attractive solution to bring the benefits of speed-controlled rotational movement to high-power applications. Therefore, multilevel inverters have attracted wide interest in both the academic community and in the industry for the past two decades.

In this doctoral thesis, modulation methods suitable especially for series-connected H-bridge multilevel inverters are discussed. A concept of duty cycle modulation is presented and its modification is proposed. These methods are compared with other well-known modulation schemes, such as space-vector pulse width modulation and carrier-based modulation schemes. The advantage of the modified duty-cycle modulation is its algorithmic simplicity. A similar mathematical formulation for the original duty cycle modulation is proposed. The modified duty cycle modulation is shown to produce well-formed phase-to-neutral voltages that have lower total harmonic distortion than the space-vector pulse width modulation and the duty cycle modulation. The space-vector-based solution and the duty cycle modulation, on the other hand, result in a better-quality line-to-line voltage and current waveform.

The voltage of the DC links in the modules of the series-connected H-bridge inverter are shown to fluctuate while they are under load. The fluctuation causes inaccuracies in the voltage production, which may result in a failure of the flux estimator in the controller. An extension for upper-level modulation schemes, which changes the switching instants of the inverter so that the output voltage meets the reference voltage accurately regardless of the DC link voltages, is proposed. The method is shown to reduce the error to a very low level when a sufficient switching frequency is used.

An appropriate way to organize the switching instants of the multilevel inverter is to make only one-level steps at a time. This causes restrictions on the dynamical features of the modulation schemes. The produced voltage vector cannot be rotated several tens of degrees in a single switching period without violating the above-mentioned one-level-step rule. The dynamical capabilities of multilevel inverters are analyzed in this doctoral thesis, and it is

shown that the multilevel inverters are capable of operating even in dynamically demanding metal industry applications.

In addition to the discussion on modulation schemes, an overvoltage in multilevel converter drives caused by cable reflection is addressed. The voltage reflection phenomenon in drives with long feeder cables causes premature insulation deterioration and also affects the common-mode voltage, which is one of the main reasons for bearing currents. Bearing currents, on the other hand, cause fluting in the bearings, which results in premature bearing failure. The reflection phenomenon is traditionally prevented by filtering, but in this thesis, a modulation-based filterless method to mitigate the overvoltage in multilevel drives is proposed. Moreover, the mitigation method can be implemented as an extension for upper-level modulation schemes. The method exploits the oscillations caused by two consecutive voltage edges so that the sum of the oscillations results in a mitigated peak of the overvoltage. The applicability of the method is verified by simulations together with experiments with a full-scale prototype.

Keywords: Multilevel inverter, Modulation, Overvoltage, DC link, Voltage ripple, Common-mode voltage.
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Dr. Hanna Niemelä helped me to place all the *a*'s and *the*'s and words in the right order into the sentences of this thesis. Her effort made the text readable and helped me to bring my ideas and thoughts into, hopefully, an understandable format. I am still amazed how you managed to proofread my text several times in such a tight schedule.

Even though the doctoral thesis is considered to be an achievement of one individual, I have to disagree with this. This thesis would still remain unwritten, if I did not have such a large group of colleagues around me. Even though I cannot list here all the people with whom I had a pleasure to work, and to whom I should express my gratitude, I dare mention a few exceptional persons in addition to the guys around the coffee table. Especially, I have to thank highly skilled Dr. Julius Luukko for the help and professional guidance he gave me throughout my academic ventures. You are a man who I will always look up to. Excitement and enthusiasm of Mr. Juhamatti Korhonen acted as a source of inspiration for me during

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Financial support for this work by Jenny and Antti Wihuri Foundation and Walter Ahlström Foundation is highly appreciated.

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Lappeenranta, Village of Ylämaa, May 7th, 2010

Ville Naumanen

Contents

Symbols and abbreviations

Roman letters

C	Capacitance
d_{ph}	Duty cycle
$\mathrm{d}u/\mathrm{d}t$	Rate of rise of voltage
f_{car}	Carrier frequency
f_{IGBT}	Switching frequency of an IGBT
f_{sw}	Sampling frequency of the reference or apparent switching frequency
I	Current, RMS value
l_{c}	Length of a cable between the inverter and the motor
M	Number of modules in series in the SCHB inverter
N_{inv}	Neutral point of a three-phase Y-connected SCHB inverter
n_{level}	Number of voltage levels of a multilevel inverter
S	Apparent power
sign	Mathematical function that gives the sign of a number
$\mathbf{sw}_{ph}^{Q}$	Switching state matrix
$sw_{M}^{t_{\mathrm{on},1}}$	Switching state of M^{th} module at the first part of the switching period
t	Time
$t_{1\mathrm{st}}$	Time instant of the first switching in the switching period
$t_{2\mathrm{nd}}$	Time instant of the second switching in the switching period
t_{d}	Propagation delay
$t_{\mathrm{on},1}$	On-time of the first state during the switching period

$t_{\mathrm{on},2}$	On-time of the second state during the switching period
$t_{\mathrm{on},3}$	On-time of the third state during the switching period
$t_{\mathrm{on},4}$	On-time of the fourth state during the switching period
$t_{\mathrm{on},5}$	On-time of the fifth state during the switching period
T_{sw}	Sampling interval of the reference or duration of the switching period
U	Voltage, RMS value
u_0	Zero-component
u_{0+}	An additional constant for the zero component
$u_{t_{\mathrm{on},1}}$	Voltage level in the first state during the switching period
$u_{t_{\mathrm{on},2}}$	Voltage level in the second state during the switching period
$u_{t_{\mathrm{on},3}}$	Voltage level in the third state during the switching period
$u_{t_{\mathrm{on},4}}$	Voltage level in the fourth state during the switching period
$u_{t_{\mathrm{on},5}}$	Voltage level in the fifth state during the switching period
u^*_α	α-component of the reference vector
u^*_β	β-component of the reference vector
u_{car}	Carrier waveform of the carrier-based modulation methods
u_{cm}	Common-mode voltage
u_{dc}	DC link voltage
$u_{\mathrm{dc},1}$	DC link voltage of the first module
$u_{\mathrm{dc},2}$	DC link voltage of the second module
$u_{\mathrm{dc},M}$	DC link voltage of the M^{th} module
$\hat{u}_{\mathrm{dc}}$	Nominal DC link voltage
u_{frac}	Fractional part of the phase-voltage average
$u_{\mathrm{l-l}}$	Line-to-line voltage
u_{mod}	Output voltage of a module of the SCHBI
$\hat{u}_{\mathrm{osc}}$	Peak value for the oscillating overvoltage at the motor terminals
u_{osc}	Measured voltage oscillation at the motor terminals
u^*_{ph}	Phase voltage reference
u^*_{U}	Phase voltage average, phase U

u_{V}^{*}	Phase voltage average, phase V
u_{W}^{*}	Phase voltage average, phase W
v	Propagation speed
Z_{c}	Cable characteristic impedance
Z_{L}	Motor characteristic impedance
Z_{S}	Inverter impedance

Greek letters

α	Abscissa of the Cartesian coordinate system attached to the stator reference frame
β	Ordinate of the Cartesian coordinate system attached to the stator reference frame
Δt_{sw}	Interval between two consecutive edges
$\Delta t_{\mathrm{sw}}^{\mathrm{opt}}$	Interval between two consecutive edges resulting in optimal mitigation of the oscillating overvoltage
ε	Permittivity
Γ_{L}	Reflection coefficient at the motor terminals
Γ_{S}	Reflection coefficient at the inverter terminals
μ	Permeability

Subscripts

cm	Common-mode
N	Nominal value
ph	Any phase of the SCHBI
pri	Primary side of the transformer
sec	Secondary side of the transformer
U, V, W	Phases of a three-phase inverter

Superscripts

$*$	Reference
$^{\circ}$	Degree, unit of an angle
neg	Carrier for the negative voltage
pos	Carrier for the positive voltage

Acronyms

DC	Direct Current
DCM	Duty Cycle Modulation
FPGA	Field Programmable Gate Array
IGBT	Insulated Gate Bipolar Transistor
IG	Induction Generator
IM	Induction Motor
L	Inductor
LSPWM	Level Shifted Pulse Width Modulation (carriers shifted vertically)
M2C	Modular-Multilevel Converter
M2LC	Modular-Multilevel Converter
MDCM	Modified Duty Cycle Modulation
mod1	First module in series
mod2	Second module in series
mod3	Third module in series
NPC	Neutral Point Clamped inverter
PSPWM	Phase Shifted Pulse Width Modulation (carriers shifted horizontally)
PVC	Polyvinyl Chloride, an insulation material
PWM	Pulse Width Modulation
R	Resistor
SCHBI	Series-Connected H-Bridge Inverter, also known as cascaded H-bridge inverter
SVPWM	Space Vector Pulse Width Modulation
THD	Total harmonic distortion

List of publications

Publication **I**:

Naumanen, V.; Luukko, J.; Itkonen, T.; Pyrhönen, O. & Pyrhönen, J. (2009), "Modulation technique for series-connected H-bridge multilevel converters with equal load sharing", *IET Power Electronics*, vol. 2, pp. 275–286.

Publication **II**:

Naumanen, V.; Luukko, J.; Silventoinen, P.; Pyrhönen, J.; Sarén, H. & Rauma, K. (2009), "Compensation of Unequal Voltages in the DC links of a Multilevel Series-Connected H-Bridge Inverter", *In proceedings of the 35th Annual Conference of the IEEE Industrial Electronics Society, IECON 2009.*

Publication **III**:

Naumanen, V.; Luukko, J.; Silventoinen, P.; Pyrhönen, J.; Sarén, H. & Rauma, K. (2010), "Compensation of DC Link Voltage Variation of a Multilevel Series-Connected H-Bridge Inverter", *IET Power Electronics*, Accepted for publication.

Publication **IV**:

Naumanen, V.; Luukko, J.; Pyrhönen, J. & Silventoinen, P. (2009), "Analysis of dynamic performance of multilevel modulators with switching pattern restricted to single voltage level steps", *In proceedings of the 13th European Conference on Power Electronics and Applications*, EPE '09, pp. 1-9.

Publication **V**:

Naumanen, V.; Korhonen, J.; Silventoinen, P. & Pyrhönen, J. (2010), "Mitigation of high $\mathrm{d}u/\mathrm{d}t$-originated motor overvoltages in multilevel inverter drives", *IET Power Electronics*, Accepted for publication.

Publication **VI**:

Naumanen, V.; Korhonen, J.; Silventoinen, P. & Pyrhönen, J. (2010), "Multilevel Modulation Method for Mitigation of High du/dt-Originated Oscillating Overvoltages at Motor Terminals", *IET Power Electronics*, Accepted for publication.

Chapter 1

Introduction

Over the past two decades, multilevel inverters have attracted wide interest both in the scientific community and in the industry. The reason for the increased interest is that the multilevel inverters are a viable technology to implement controlled rotational movement in high-power applications.

This doctoral thesis focuses on multilevel converter modulation with a special emphasis on a series-connected H-bridge topology. The thesis consists of four main themes, which are

1. Comparison of the three selected modulation methods.
2. Equal load sharing between the modules of the inverter.
3. Compensation of the voltage error caused by fluctuating DC link voltages by means of modulation.
4. Motor terminal overvoltage mitigation by modulation.

This chapter begins with a literature review, which aims at providing the backgrounds of the research and the topic. After the literature review, the prototype that was used to verify the analysis is introduced. The thesis is based on six publications written by the author. The publications and scientific contributions together with the outline of the thesis are introduced in brief at the end of the chapter.

1.1 Multilevel inverters

The history of multilevel inverters begins in the mid-1970s, when the first patent describing a converter topology capable of producing multilevel voltage from various DC voltage sources

was published (Baker and Bannister, 1975). The topology was achieved by connecting single phase inverters in series. Figure 1.1(a) shows an example of a circuit related to the topology presented by Baker and Bannister. The topology depicted in the figure is a series-connected H-bridge inverter (SCHBI), also known as a cascaded H-bridge inverter.

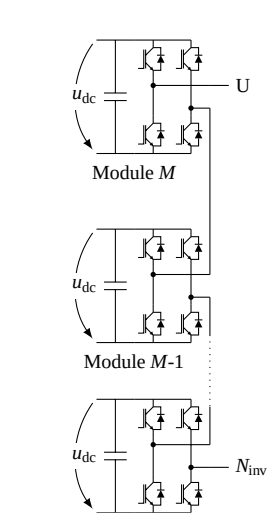
In Baker (1980), a modified multilevel topology was introduced. Two topology examples are shown in Figure 1.1(b) including three-level and five-level inverters. The five-level circuit described in the figure differs from the topology originally proposed by Baker (1980) considering the series-connected clamping diodes. The voltage can be shared over several diodes as described in Yuan and Barbi (2000) and depicted in Figure 1.1(b). In contrast to the series-connected single phase inverters, this converter can produce multilevel voltage from one DC source with extra diodes connected to the neutral point. This topology is referred to as a neutral point clamped inverter (NPC). A pulse width modulation (PWM) for the NPC was introduced by Nabae et al. (1980). In the same paper, an implementation of the NPC with test results was introduced.

The interest in the multilevel inverters (except three-level inverters) faded during the 1980s, but in the 1990s this technology began to draw some attention again. For example Marchesoni et al. (1990) proposed that an SHCBI could be used in nuclear fusion experiments. Moreover, Marchesoni and his research group made a significant contribution to the multilevel inverter research, especially in control and modulation, in the early 1990s; see for instance (Marchesoni, 1989; Marchesoni et al., 1990; Carrara et al., 1990; Fracchia et al., 1992). After the mid-1990s, several patents were published including (Lavieville et al., 1997; Hammond, 1997). In Meynard and Foch (1992) and later in Lavieville et al. (1997), a flying capacitor inverter was introduced. The topology of the flying capacitor inverter is depicted in Figure 1.1(c) for three-level and five-level applications. Hammond (1997), on the other hand, proposed a practical method to implement an SCHBI.

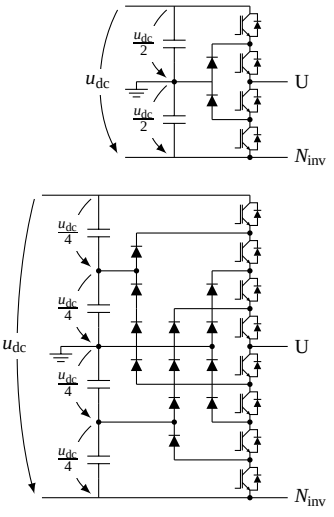
In the 1990s and 2000s, several other variations of multilevel inverter topologies have been proposed. Several alternative ways to implement a cascaded inverter were introduced in (Stemmler and Guggenbach, 1993; Kawabata et al., 1996; Corzine et al., 1999; Kang et al., 2000). One of the proposed cascaded inverter topologies includes a machine with open-end windings, and a two-level inverter, which is connected to one end of the windings and the H-bridges to the other side (Kang et al., 2000). Another interesting topology that has attracted increasing attention is the modular-multilevel converter (M2LC or M2C) (Lesnicar and Marquardt, 2003; Glinka and Marquardt, 2003, 2005; Hagiwara and Akagi, 2008; Rohner et al., 2009; Antonopoulos et al., 2009). These evolving topologies are left outside the scope of this thesis.

The three topologies, the SCHBI, the NPC, and the flying capacitor, have aroused the widest interest to date. The SCHBI has an advantage over the NPC and flying capacitor topologies owing to its modularity, as can be noted by comparing the topologies in Figure 1.1. The number of voltage levels can be increased without complicating the circuitry, because the number of levels is increased by adding H-bridge modules in series. The drawback of the SCHBI is the need for an isolated DC source for every module, while the other two converters require only one DC source. In this thesis, the topology of the SCHBI is chosen to be investigated

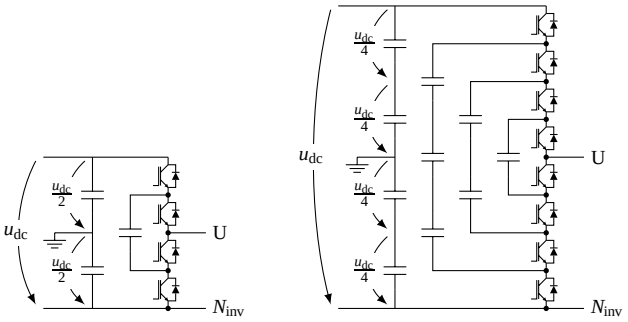
because of its attractive feature of modularity over the other two main topologies.



(a) $2M+1$ level SCHB inverter



(b) Three-level (top) and five-level (bottom) NPC inverter



(c) Three-level (left) and five-level (right) capacitor-clamped inverter

Figure 1.1. Multilevel converter topologies.

1.2 Modulation methods

One module of the SCHBI can form the voltage levels -u_{dc}, zero, and u_{dc}. A phase circuit of the SCHBI with M-modules in series can form voltage levels from -Mu_{dc} to Mu_{dc} including zero voltage. Therefore, an inverter with M-modules in series is usually referred to as an n_{level}-level inverter and the number of levels can be calculated as

$$n_{level} = 2M + 1. \tag{1.1}$$

In a three-phase multilevel inverter, the phase circuits illustrated in Figure 1.1 are either Y connected from N_{inv} points or Δ connected. The phase circuits are usually connected to symmetric windings of the motor, and to obtain rotational flux in the stator, a 120° shift between the voltage of phases has to be arranged. The phase shift is arranged by means of modulation.

A combination of the phase–voltage levels is denoted as a switching state. A switching state is an instantaneous voltage vector composed of three phase–voltage levels according to the well-known space vector theorem, and graphically, all the switching states together form a voltage hexagon lattice. Each node on the lattice represents a producible voltage vector, some of the nodes having multiple redundant switching states. A voltage hexagon lattice for a five-level inverter is depicted in Figure 1.2. Because the phase voltages can change in steps of u_{dc}, the distance between two adjacent nodes is also u_{dc}.

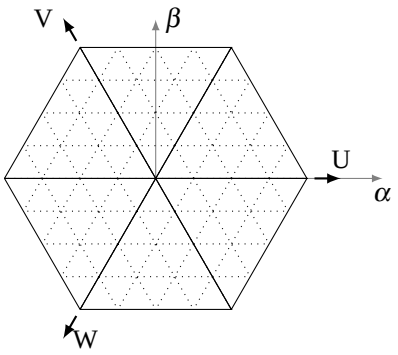


Figure 1.2. Voltage hexagon lattice of a five-level inverter with an $\alpha\beta$ reference frame and positive phase-voltage directions. Every crossing of lines is denoted as a node.

The nodes are used to produce the time-averaged voltage vector assigned by a controller. The voltage vector is usually attached to a stationary stator reference frame, that is, a Cartesian $\alpha\beta$ coordinate system. The task of the modulator is to select such switching states that meet the reference.

Several different modulation methods have been proposed in the literature; a popular categorization of these was presented in Rodriguez et al. (2002) and updated in Franquelo et al. (2008). The main parts of the categorization are reproduced in Figure 1.3.

This thesis focuses on the comparison of carrier-based modulation methods with the space vector pulse width modulation (SVPWM) and the duty cycle modulation (DCM) first introduced by Corzine and Baker (2001) and modified in Hyrkäs (2008); Pajari (2007), and in publication **I**. The low switching frequency controls, such as space vector control (Rodriguez et al., 2001) and harmonic elimination (Chiasson et al., 2004), are ruled out from this comparison, because they require stiff DC links. 'Stiff' means here that the voltage of the DC link does not vary considerably even under a high load. This can be achieved with large capacitors in every module of the SCHBI. Next, the basics of carrier-based modulation methods and the SVPWM are introduced. The DCM is introduced later in Section 2.1.

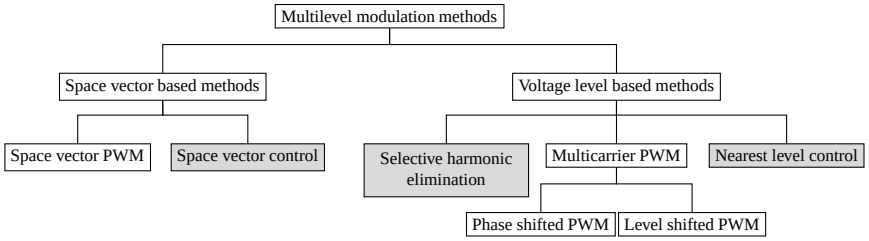


Figure 1.3. Modulation strategies for multilevel inverters. The shaded methods are low switching frequency methods, which are outside the scope of this thesis (Rodriguez et al., 2002; Franquelo et al., 2008).

1.2.1 Carrier-based modulation methods

In the carrier-based multilevel modulation, each level in a phase requires a carrier of its own. For the SCHBI, this means that every module has its own carrier, which is compared with the reference voltage.

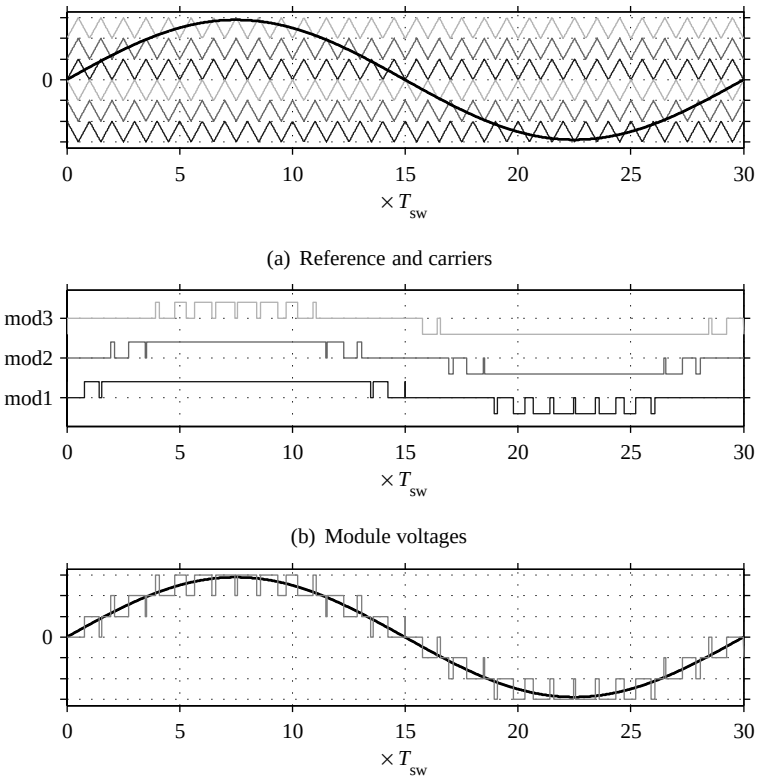
Carrier-based modulation schemes are mainly divided into two categories: level-shifted (LSPWM) and phase-shifted (PSPWM) methods. Both of these have several variations, which differ by the allocation of module carriers with respect to each other. Next, one LSPWM method and two PSPWM methods are introduced.

Level-shifted PWM

In all level-shifted PWM methods, the carriers of the modules have a frequency of $f_{\mathrm{car}} = 1/T_{\mathrm{sw}}$ and an amplitude of the module DC link voltage u_{dc}. The reference voltage, on the other hand, can have values between $-Mu_{\mathrm{dc}}$ and Mu_{dc}. To cover the whole voltage range, the carriers are shifted vertically so that the carrier of the first module covers the range from zero to u_{dc}, while the second covers the range from u_{dc} to $2u_{\mathrm{dc}}$. The last module covers the voltage from $(M-1)u_{\mathrm{dc}}$ to Mu_{dc}. At the negative side, the order of the carriers is shuffled for example in the opposite order. In the literature, this is called carrier disposition. The carriers of the LSPWM can also have a phase shift between each other.

Figure 1.4 illustrates the allocation of the carriers with respect to the reference voltage according to the level disposition method presented by Carrara et al. (1990). The produced module voltages and the output voltage of the inverter are also depicted in the figure. The output voltage is a sum of module voltages.

The switching instants are obtained by comparing the voltage reference with the module carrier. The module state is determined to be $+u_{\mathrm{dc}}$ if the reference is higher than the positive carrier. For the negative carrier, the comparison is made vice versa, and otherwise, the module



(a) Reference and carriers

(b) Module voltages

(c) Modulated phase voltage and reference

Figure 1.4. Carrier allocation, module voltages, and phase voltage of the level-shifted PWM. The darkest carrier is for module 1 and the lightest for module 3.

produces a zero voltage. Mathematically, this can be formulated as

$$u_{\text{mod}} = \begin{cases} u_{\text{dc}}, & \text{if } u^*_{ph} > u^{\text{pos}}_{\text{car}} \\ -u_{\text{dc}}, & \text{if } u^*_{ph} < u^{\text{neg}}_{\text{car}} \\ 0, & \text{otherwise} \end{cases} \tag{1.2}$$

The switching frequency that is visible in the output voltage of the inverter is denoted as an apparent switching frequency f_{sw}. With the LSPWM, f_{sw} is equal to the carrier frequency f_{car}, while the switching frequencies of the modules f_{mod} vary depending on the carrier allocation. f_{mod} is the switching frequency seen at the output voltage of a module.

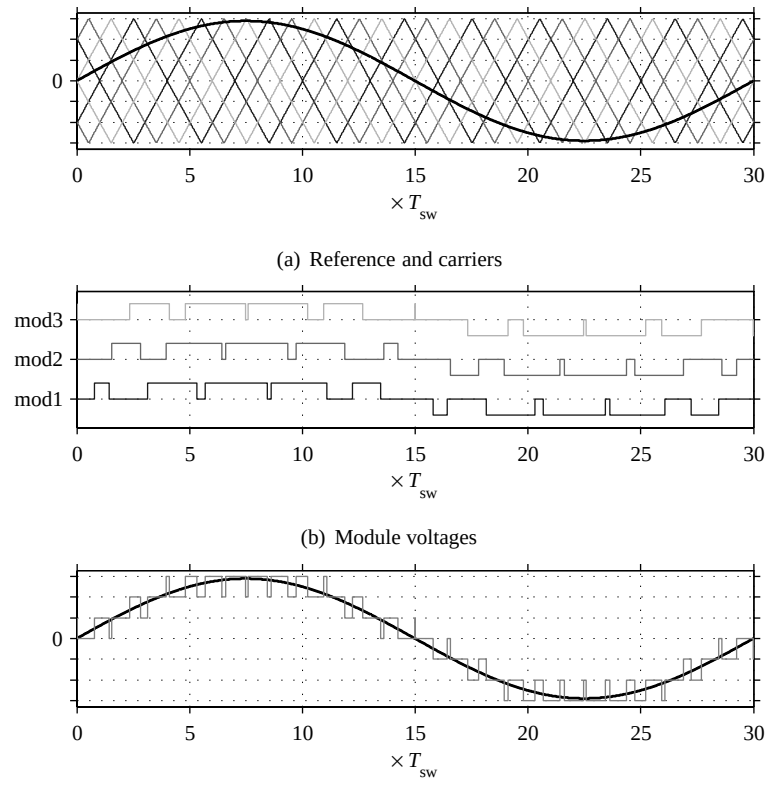
This method is not suitable for the SCHBI modulation, because the modules are not loaded equally (Franquelo et al., 2008). Comparing the load encountered by the modules, the Mth module has a low utilization rate, while the first module is utilized almost all the time. Therefore, the DC link capacitors of different modules are loaded differently, and the voltage bal-

ance is not maintained between them. When the energy is flowing back from the load, the first module takes most of the energy. This may result in a capacitor breakdown as the voltage over the DC link increases drastically.

Phase-shifted PWM

The phase-shifted PWM (PSPWM) aims at solving this equal loading problem. At least two different methods to allocate the carriers of the PSPWM have been proposed in the literature (McGrath and Holmes, 2002). In the first method, there are two carriers per module as in the LSPWM, but the carrier has an amplitude of Mu_{dc}. This method is here referred to as the PSPWM1. The carrier of the other method has a $2Mu_{\mathrm{dc}}$ amplitude ranging from $-Mu_{\mathrm{dc}}$ to Mu_{dc} and is referred to as the PSPWM2. Next, these two methods are discussed in brief.

The carriers in both PSPWM methods have a frequency of $f_{\mathrm{car}} = 1/(MT_{\mathrm{sw}})$, and are phase shifted by an angle determined by T_{sw} with respect to each other. The modulation principle

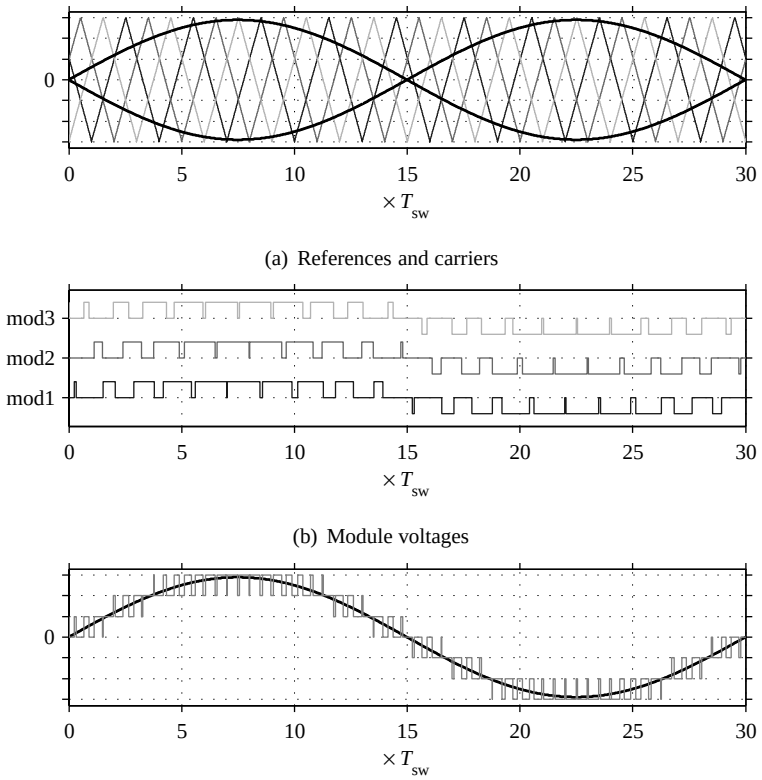


(a) Reference and carriers

(b) Module voltages

(c) Modulated phase voltage and reference

Figure 1.5. Carriers, module voltages, and output voltage of the PSPWM1.



(a) References and carriers

(b) Module voltages

(c) Modulated phase voltage and reference

Figure 1.6. Carriers, module voltages, and output voltage of the PSPWM2.

of the PSPWM1 is shown in Figure 1.5. With respect to the reference and switching instant comparison, it behaves like the LSPWM. In the PSPWM2, the reference is also multiplied by -1, as shown in Figure 1.6, where the switching instants are determined by comparing the carrier with both reference waveforms. For the PSPWM2, the output voltage of a module is determined as

$$u_{\text{mod}} = \begin{cases} u_{\text{dc}}, & \text{if } -u^*_{ph} < u_{\text{car}} < u^*_{ph} \\ -u_{\text{dc}}, & \text{if } u^*_{ph} < u_{\text{car}} < -u^*_{ph} \\ 0, & \text{otherwise} \end{cases} \tag{1.3}$$

Comparing the first and second PSPWM methods, there is a notable difference between the methods in both the module switching frequency f_{mod} and the apparent switching frequency f_{sw}. Even though the carrier frequencies are equal, the second LSPWM switches twice as often the first one. The higher switching frequency will better maintain the load balance between the modules, but its drawback is the increased switching losses.

1.2.2 Space vector pulse width modulation

From the late 1990s, several SVPWM schemes for multilevel inverters have been introduced (Mahdavi et al., 1999; Celanovic and Boroyevich, 2001; McGrath et al., 2001; Wei et al., 2003; Gupta and Khambadkone, 2007; Leon et al., 2009). The SVPWM schemes are developed to find the three nearest nodes on the voltage hexagon lattice with respect to the reference vector. The mathematical formulation of the early SVPWM methods was quite complex, because the voltage hexagon lattice was used in the Cartesian coordinate system. The coordinates of the nodes on the lattice are fractional numbers, which made the node selection difficult. This was until Wei et al. (2003) suggested a coordinate transformation to be applied to the reference vector. The idea was that the reference vector was transformed from the Cartesian coordinate system to the 60° coordinate system. The 60° coordinate system represents one sector on the lattice, and its benefit is that the coordinates for the nodes can be presented by integers. Therefore, determination of the nodes could be accomplished by simple rounding functions and integer calculation.

The use of the phase voltages was not very efficient in the method proposed by Wei et al. (2003). The three nearest nodes were used, but only in such a way that no switching state redundancies were exploited. This resulted in phase voltages where one phase did not change its state at all during one switching period. McGrath et al. (2003) proposed to use four switching states during the switching period to minimize the harmonic content of the voltage. The fourth switching state is redundant with the first state, and therefore only the three nearest nodes were used. An explicit description of an algorithm for the SVPWM scheme based on the above-mentioned methodology is given in Lauttamus and Tuusa (2007).

The advantage of determining the switching states according to the vector location on the voltage hexagon lattice is that the whole area covered by the lattice can be used without a need to consider modulation indices. With symmetric sinusoidal phase references, the carrier-based modulation schemes achieve 75% of the maximum vector length $2Mu_{\mathrm{dc}}$. To exceed this limit, a third harmonic has to be added to the references. With the SVPWM, the modulation is successful as long as the reference vector is located inside the voltage hexagon. The addition of third harmonic does not have to be considered separately.

1.3 Implementation of the modulation algorithms

The carrier-based PWM methods are traditionally used in analog implementation of modulators, where the advantage of the continuous reference can be exploited in full when switching instants are determined. With a certain carrier frequency, the average voltage will be as close to the reference as possible. Nowadays, the control systems are digitally implemented, and therefore the references are not continuous but sampled. The same reference remains in force for a sampling period, which is now determined as T_{sw}. The switching instants can be calculated in advance so that the resulting average voltage will meet the reference.

If the modulation methods are considered from the gate driver point of view, any PWM method can be considered to be carrier based. The processor provides a timer (perceived as the carrier waveform), which is compared with the predetermined switching instants (perceived as the reference waveform) to time the turn-on or turn-off instants for the switches.

1.4 Deficiencies of the modulation

1.4.1 DC link voltage feedback

As described above, the output voltage of a multilevel inverter consists of steps. The height of a step is the voltage at the DC source, which is exposed to the load by switching. Ideally, the DC sources remain constant regardless of the load current, but in reality, the DC source is buffered by a capacitor that has a finite capacitance, and therefore, the DC voltage will fluctuate when it is under load. If the fluctuation in the DC voltages is not taken into account in the modulation, the output voltage will be erroneous. The effects of the DC voltage ripple on the modulated voltage are discussed further in Section 2.4 of this thesis.

The fluctuation can be compensated by measuring the voltages and modifying the modulation algorithm so that the resulting voltage will meet the reference. With carrier-based modulation schemes, the fluctuation can be compensated by modifying the amplitude of the module carriers as proposed for example in Kouro et al. (2006, 2008). The authors of Kouro et al. (2005) introduce a method in which the output voltage is integrated during T_{sw} to determine the switching instants.

In this thesis, an extension for space-vector-based modulation algorithms is proposed and analyzed in Section 2.4. The suggested method is used to calculate the switching instants according to the measured DC link voltage.

1.4.2 Overvoltages induced by cable reflection phenomenon

It has been widely reported that an inverter-driven motor suffers from an extra voltage stress caused by the overvoltages at the motor terminal caused by the voltage reflection phenomenon (Persson, 1992; Saunders et al., 1996; Skibinski et al., 1997; Rahman et al., 1999; Endrejat and Pillay, 2009). This extra voltage stress may lead to premature insulation failure in the motor windings (Campbell and Stone, 2000).

The voltage stress in the winding insulation is caused by an uneven allocation of the voltage in the winding of the motor after a high $\mathrm{d}u/\mathrm{d}t$ voltage edge. When the voltage edge reaches the motor terminals, it begins to intrude into the winding while simultaneously charging the stray capacitances from the winding to the chassis and from turn to turn (Wright et al., 1983). The edge will therefore propagate also in the winding. This causes a voltage difference, reaching

up to 75 % of the edge amplitude, between the first few turns of the winding (Fenger et al., 2002). This accelerates the aging process of the insulation material even with a normal two-level inverter.

The reflection phenomenon causes an increase in the amplitude of the voltage at the motor terminals as will be shown later in this work. Therefore, the voltage stress over the insulation material also increases. Another symptom of the reflection phenomenon is that the motor terminal voltage oscillates after a high $\mathrm{d}u/\mathrm{d}t$ edge. The oscillating voltage intrudes into the winding and repetitively introduces high $\mathrm{d}u/\mathrm{d}t$ edges causing stress to the insulation.

Another problem relating to high $\mathrm{d}u/\mathrm{d}t$ voltage edges in inverter-fed motors is the bearing currents, which cause premature bearing failures resulting from material loss (fluting) caused by electrical discharges (Lawson, 1993; Chen et al., 1996; Link, 1998). One of the significant reasons for bearing currents is the common-mode voltage introduced to the motor by the modulated voltage (Hoppler and Errath, 2007; Särkimäki, 2009). The common-mode voltage u_{cm} is the average voltage seen at the motor terminals, and it is calculated from the phase voltage as

$$u_{\mathrm{cm}}(t) = \frac{u_{\mathrm{U}}(t) + u_{\mathrm{V}}(t) + u_{\mathrm{W}}(t)}{3} \tag{1.4}$$

where u_{U}, u_{V}, and u_{W} are phase-to-ground voltages seen at the motor terminals (Dzhankhotov, 2009; Särkimäki, 2009).

The common-mode voltage charges the stray capacitances of the motor so that a voltage difference is built up over the lubrication film of the bearings. When a high $\mathrm{d}u/\mathrm{d}t$ change in the common-mode voltage occurs, the capacitances are discharged and a high-frequency current flows through the bearings causing a spark, which damages the surface of the iron (Särkimäki, 2009). A bearing current that leads to fluting may also take place when a high $\mathrm{d}u/\mathrm{d}t$ change in the common-mode voltage occurs even without precharged capacitances.

As explained above, the phase voltages at the motor terminals may oscillate at frequencies from several kilohertz up to megahertz after a steep voltage edge. If one of the phases oscillates, the common-mode voltage will also oscillate.

The occurrence of the reflected overvoltage is a complex phenomenon, but the basic principle is well explained for example in Persson (1992); Saunders et al. (1996). Here, the phenomenon is described in brief.

The reflection occurs especially in drives with long cables. The cable may be considered to be long, if the propagation delay t_{d} of the cable is higher than the rise time of the voltage edge. The propagation delay of the cable is mostly dependent on the insulation material and the length l_{c} of the cable and is determined as

$$t_{\mathrm{d}} = \frac{l_{\mathrm{c}}}{v} \tag{1.5}$$

where v is the cable insulation material-dependent speed of the propagating pulse (Kerkman et al., 1997). The value of v depends on the permittivity and permeability of the material in

which the electromagnetic wave propagates as

$$v = \frac{1}{\sqrt{\mu\varepsilon}}, \tag{1.6}$$

where μ is the permeability and ε the permittivity of the material (Pozar, 2005). In the vacuum, where both the relative permittivity and the relative permeability are one, and the speed of the propagating electromagnetic wave is the speed of light. The relative permittivity of the PVC-insulated cable is approximately four, while the relative permeability is close to one, when the speed of the propagating electromagnetic wave in the cable is approximately half the speed of light (Skibinski et al., 1997). For example with a 20 m PVC-insulated cable, the propagation delay is about 133 ns.

The rise time of the voltage edge is determined by the properties of the switches in the inverter, and with modern-day IGBTs, the rise time is in the range of tens to hundreds of nanoseconds. Therefore, even a 20 m cable is long, when fast IGBTs are used to switch the voltage, which will result in an oscillating voltage in the cable.

The oscillation is caused by the impedance mismatch between the cable and the motor terminal and also between the inverter and the cable. The impedance mismatch can also be explained by the change in permeability and permittivity. The permeability of the cable insulation is very low compared with that of the motor iron surrounding the conductors inside the motor stator slots. The change in the permeability, encountered by the propagating edge, leads also to a change in the propagation speed at the interface of the cable and the motor. A reflection will occur.

The impedance mismatch is usually described by reflection coefficients at both ends of the cable. The load-side (or motor terminal) reflection coefficient is determined as

$$\Gamma_{\mathrm{L}} = \frac{Z_{\mathrm{L}} - Z_{\mathrm{c}}}{Z_{\mathrm{L}} + Z_{\mathrm{c}}} \tag{1.7}$$

Z_{L} is the motor characteristic impedance and Z_{c} is the cable characteristic impedance (Skibinski et al., 1997; Ström, 2009). Γ_{L} is a complex value determining the amplitude and the phase shift of the reflected voltage, but it is usually simplified to a real value that represents the amplitude of the reflected voltage. The impedance of the motor is higher than that of the cable, and therefore $\Gamma_{\mathrm{L}} > 0$. Depending on the size of the motor, the reflection coefficient can have values from 0.65 to 0.95 (Persson, 1992).

At the inverter end of the cable, the reflection coefficient is determined as

$$\Gamma_{\mathrm{S}} = \frac{Z_{\mathrm{S}} - Z_{\mathrm{c}}}{Z_{\mathrm{S}} + Z_{\mathrm{c}}} \tag{1.8}$$

where Z_{S} is the characteristic impedance of the inverter, which is very small, because the current either flows through small impedance switches or through switches and DC link capacitors, and therefore, the reflection coefficient at the inverter end of the cable is close to -1.

A simplified explanation of the oscillation phenomenon can be given as follows: The inverter switches a voltage pulse to the cable, which encounters the impedance mismatch Γ_{L} at the motor end of the cable after the propagation delay t_{d}. The voltage reflects at the impedance barrier and sums up to the original voltage level. This causes an overvoltage to the motor terminals. The reflected voltage travels back to the inverter end, where it reflects again, but now with an opposite polarity. The reflected wave heads again back to the motor end. The voltage continues to reflect at both ends of the cable, while attenuating in the cable. An example of the resulting oscillating motor terminal voltage together with the voltage at the inverter end is shown in Figure 1.7.

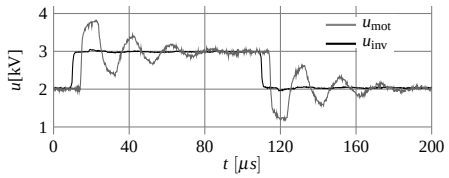


Figure 1.7. Measured voltage at the seven-level inverter terminals and at the open end of a 300 m cable.

With a cable, the permittivity and the permeability of which are equal to that of vacuum, and the conductivity of the line is infinite, the oscillating voltage would have exactly the same $\mathrm{d}u/\mathrm{d}t$ in every cycle as the original pulse, and only the amplitude of the pulse would be attenuated. As Figure 1.7 shows, the edge attenuates in its amplitude and high-frequency components more and more, cycle after cycle. The distortion is caused mainly by the filtering properties of the cable, because the cable acts as a high-bandwidth low-pass filter in the system.

Several methods to reduce the overvoltage by filtering in two-level drives have been proposed in the literature, and many of them are successfully applied in the industry. Finlayson (1998) gives an extensive survey on the passive filtering methods such as a line-reactor (further discussed in Steinke (1999)), a sinusoidal filter (Skibinski, 2002), a $\mathrm{d}u/\mathrm{d}t$ filter (Habetler et al., 2002), and a line-terminator (Skibinski, 1996). The filters are composed of passive components, and they aim at damping the high-frequency components of the output voltage of the inverter. Even though these filters provide a good solution to overvoltage reduction, the drawbacks are the size of the filters and the losses they cause.

Also some active filtering methods have been presented. For example in Ström et al. (2009); Korhonen et al. (2009), the size of the output filter is reduced by modulating the voltage edges, in which case the output of the filter will have a considerably lower $\mathrm{d}u/\mathrm{d}t$ compared with that of the inverter. To be viable, this active filtering method requires very fast switches with excellent switching characteristics, which are not yet reached in practice by the modern-day IGBTs without considerably degrading the current-carrying capability of the switches. The inverter cooling system has to be dimensioned to cover the losses caused by the extra switchings during the modulation cycle.

Another active filtering method was first introduced by Lee and Nam (2002), which is suitable to be used with multilevel inverters. The method is based on the exploitation of the

oscillating voltages caused by two consecutive voltage edges induced to a long cable. Lee and Nam suggested this method to be used in a two-level inverter drive with a modified inverter. The modified inverter circuit is actually a three-level inverter. In publications **V** and **VI** the method proposed in Lee and Nam (2002) is further developed and applied to multilevel inverters.

1.5 Prototype

A prototype of a three-phase seven-level SCHB inverter was built to verify the applicability of the proposed methods. The modules of the converter consist of a three-phase diode-rectifier, a DC link capacitor, and a single-phase IGBT H-bridge. Three modules per phase are connected in series, forming approximately a 6 kV peak-to-peak phase voltage.

The converter is connected to the grid through a single-primary–multi-secondary transformer. Each secondary feeds one module. A custom-wound medium voltage induction motor was used as a load for the converter.

The control of the converter is implemented with an FPGA-based control and a communication circuit in each module, and a central controller board. The communication is based on fibre-optic data transfer between the central board and the modules. Each phase forms a data transfer ring of its own, because the modules are connected in series with the fibre-optic links.

The main parameters of the prototype are shown in Table 1.1, and the configuration is depicted in Figure 1.8.

Table 1.1. Main parameters of the prototype

Inverter		
Nominal peak phase voltage	u_{N}	2925 V
Nominal current	I_{N}	34 A
Modules in a phase	M	3
Nominal module DC link voltage	$\hat{u}_{\mathrm{dc}}$	975 V
DC link capacitance	C_{dc}	550 µF
Transformer		
Primary power	S_{pri}	101 kVA
Secondary power	S_{sec}	9×11.5 kVA
Primary voltage	U_{pri}	400 V
Secondary voltage	U_{sec}	690 V

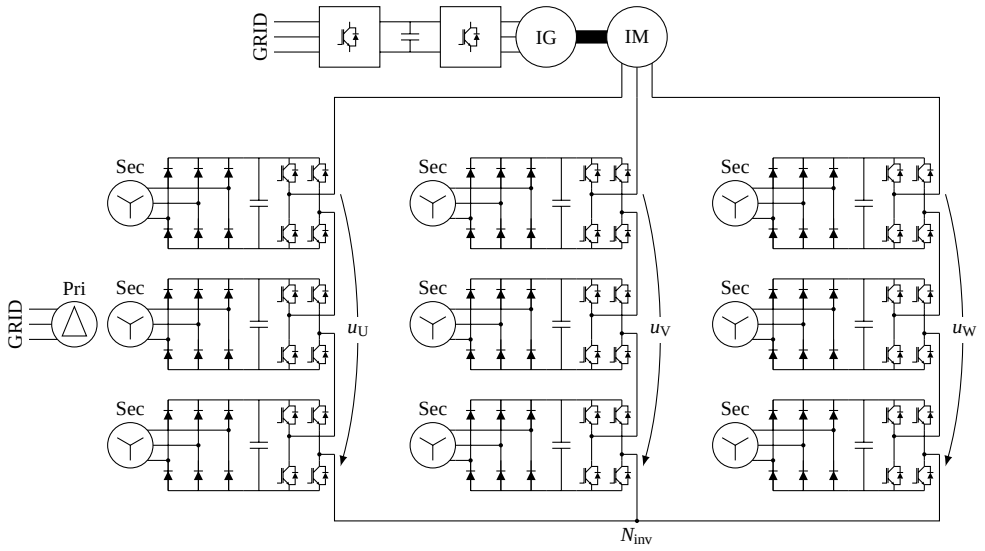


Figure 1.8. Arrangement of the prototype. A one-primary–nine-secondary transformer feeds the inverter modules. IM denotes an induction motor and IG is an induction generator connected to the same shaft with the IM.

1.6 Description of publications

Publication I describes a duty cycle modulation method for multilevel inverters. A similar method has been presented in Corzine and Baker (2001) and in Corzine and Baker (2002). Publication **I** formulates equations differently allowing lower common-mode voltage and simpler implementation of the method. Also a voltage formation method that aims at distributing the load evenly between the phase modules of the inverter is proposed. The scientific contributions of the publication are discussed in Section 2.

The author of this thesis participated in the development process of the method discussed in publication **I**. The analysis and the prototype testing were mainly carried out by the author. Also the manuscript of the publication was written by the author.

Publication II: Publication **I** showed that the modulation method maintains the balance between the DC links of the phase modules. On the other hand, publication **II** shows that the DC link voltages vary considerably. This variation affects the quality of the phase voltage. A simple compensation method to improve the voltage quality by duty cycle modulation is introduced in this publication.

The algorithm was developed and the results were produced by the author and the publication was mainly written by the author.

Publication III is a continuation of publication **II**. In this publication, the compensation method is developed further to be applicable with the SVPWM also. The analysis of the compensation is more thorough compared with **II**.

The author is responsible for the development of the algorithm and the analysis discussed in the publication. Also the manuscript of the publication was written by the author.

Publication IV presents the analysis of the modulation when the output voltage is restricted to one voltage level steps. This restriction causes some limitations to the operation of the modulation under dynamic operating conditions.

The methods, results, and analysis described in the publication are fully made by the author. The manuscript was written by the author.

Publications V and VI discuss the cable reflection phenomenon in multilevel inverters. Cable reflection phenomenon causes an oscillating voltage at the motor terminals after each switching. This causes extra stress to the windings of the motor. In these publications, a method to mitigate the oscillation is introduced and analyzed. In publication **V** the phenomenon and the mitigation principle is discussed, and in **VI** the principle is extended to a modulation method.

The method was developed and the publications were written in co-operation with Juhamatti Korhonen.

1.7 Scientific contributions

The main scientific contributions of this thesis are the following:

1. Development of a modified algorithm for duty cycle modulation.
2. Comparative analysis of space vector modulation and duty-cycle modulation for an SCHBI multilevel inverter.
3. Analysis of equal load sharing among the modules of the SCHBI by space vector modulation and duty-cycle modulation.
4. Comparative analysis of duty-cycle modulation and space vector modulation with respect to common-mode voltage production.
5. Development of an extension for modulation algorithms, which compensates the error in the modulated voltage caused by fluctuating DC link voltages.
6. Development and analysis of a modulation method to mitigate oscillating overvoltages without a filter in a multilevel inverter drive with a long cable.

1.8 Outline of thesis

This thesis reports the results of research work carried out by the author during the years 2006–2009. The research focused on multilevel inverter modulation, with a special reference to a series-connected H-bridge inverter. The outline of the thesis is as follows.

In Chapter 1, a brief glance at the history of multilevel inverters is given including different topologies and various modulation methods presented in the literature. A prototype used to verify the methods and simulations is introduced. The outline of the thesis is given and the author's contribution to the publications is reported at the end of the chapter.

In Chapter 2, modulation of a series-connected H-bridge inverter is discussed. This chapter is an introduction to the publications **I**-**IV** even though some previous, unpublished results and modulation methods are also discussed. Unpublished results include the analysis of the common-mode voltage production, the effects of switching frequency on voltage quality, and a comparative analysis of different modulation schemes.

Chapter 3 discusses a multilevel drive with long cables between the inverter and the motor. A modulation method that aims at mitigating oscillating overvoltages at the motor terminals is proposed. The main function of the chapter is to act as an introduction to the publications **V** and **VI** where oscillating overvoltages and the proposed method are discussed in detail.

In Chapter 4, a summary of the methods, results, and the analysis is given. Some suggestions for future work on multilevel inverter modulation are laid out.

Chapter 2

Modulation of a series-connected H-bridge inverter

This chapter provides an introduction to publications **I**, **II**, **III**, and **IV**. In **I**, duty cycle modulation is introduced with voltage formation aiming at equal loading of the modules in the inverter. Publications **II** and **III** address a method to use the measured DC link voltages in modulation, while **IV** discusses the allowable changes in the reference voltage when certain restrictions on voltage formation apply.

2.1 Duty cycle modulation

This section gives a short review on the duty cycle modulation discussed in publication **I**. The section also aims at clarifying the basic functionality of two versions of the duty cycle modulation. The first version is the one proposed in publication **I**, while the second is a reformulation of the duty cycle modulation proposed by Corzine and Baker (2001). The first is referred to as modified duty cycle modulation (MDCM) and the second as duty cycle modulation (DCM).

The idea of the duty cycle modulation was originally proposed by Corzine and Baker (2001); the modulation introduced in publication **I** differs from the original DCM by the mathematical formulation and by the voltage formation. First, the modulation suggested in publication **I** is discussed in brief followed by a brief description on the original DCM. In the discussion following this, the MDCM is reformulated so that it will correspond to the DCM proposed by Corzine and Baker (2001). The presentation of the DCM differs from the method by Corzine and Baker (2001) by the mathematical formulation. The format of the algorithm presented here allows straightforward implementation without a need for angle calculations.

2.1.1 Modified duty cycle modulation

The task of the modulator is to produce such switching commands that meet the reference. In a single-phase system, the reference is for example the value of the voltage during a switching period. In a three-phase system, the reference is usually a vector in an $\alpha\beta$-coordinate system. The reference is typically formed by a controller.

The duty cycle modulation described in **I** is based on the original idea by Corzine and Baker (2001) to extract the phase voltage references from the reference vector and modulate the phases independently. The method was further developed by Hyrkäs (2008) in his Master's thesis while the implementation of the modulation was demonstrated in Pajari (2007). The algorithm was also discussed in publication **I**, where the measurement results and the analysis of the algorithm were presented. Here, only the main parts of the algorithm are discussed to clarify the notations in this thesis.

The modulation method is based on finding the phase voltage averages $[u^*_{\mathrm{U}}, u^*_{\mathrm{V}}, u^*_{\mathrm{W}}]$, which correspond to the voltage vector reference. One of the possible methods is to use a coordinate transformation from a two-axis coordinate system to a three-axis coordinate system. Here, the two-axis coordinate system is the above-mentioned $\alpha\beta$-coordinate system, and the three-axis system is formed from the phase voltages. The transformation from the controller-given vector to phase voltage averages can be made with

$$\begin{bmatrix} u^*_{\mathrm{U}} \\ u^*_{\mathrm{V}} \\ u^*_{\mathrm{W}} \end{bmatrix} = \begin{bmatrix} 1 & 0 & \frac{3}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{3}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix} \begin{bmatrix} u^*_{\alpha} \\ u^*_{\beta} \\ u_0 \end{bmatrix} \tag{2.1}$$

where u_0 is a zero voltage, or the average of the phase voltages. In a totally symmetrical system, u_0 equals zero. For the simplicity of the mathematical formulation, all the voltages are normalized to the nominal voltage of one DC link $\hat{u}_{\mathrm{dc}}$.

From the phase voltage averages $[u^*_{\mathrm{U}}, u^*_{\mathrm{V}}, u^*_{\mathrm{W}}]$, the voltage levels used during a switching period (phase states) can be determined by a rounding function. The switching period is selected to begin with a low phase state, and the high phase state is used in the middle of the period. The low phase state can be determined by a rounding function, which rounds the phase voltage average to the nearest integer toward zero. The high phase state on the other hand can be determined by a rounding function, which rounds to the nearest integer away from zero. Thus, the high phase state is formed with a higher number of active modules compared with the low phase state. The concept of phase states is clarified in Figure 2.1.

The switching instants can be determined from the fractional part of the phase voltage reference by the following means. With the duty cycle modulation, the voltage is formed so that the high state is used for the duration $u_{\mathrm{frac}} T_{\mathrm{sw}}$, and the low state is used for the rest of the switching period. The switching period is started with a low phase state and a high phase state is used in the middle of the period. The period is ended with a low state. Therefore, two switchings occur during the switching period. The time instant for the first switching is

$$t_{1\mathrm{st}} = \frac{(1 - u_{\mathrm{frac}}) T_{\mathrm{sw}}}{2} \tag{2.2}$$

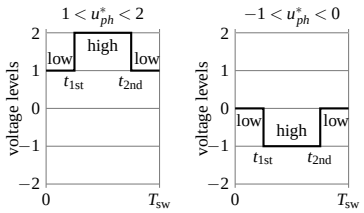


Figure 2.1. Concept of phase states with two example phase voltage references.

and the instant for the second switching

$$t_{2nd} = T_{sw} - t_{1st}. \tag{2.3}$$

This way, the modulated phase voltage will be symmetric with respect to $T_{sw}/2$ and also with respect to the voltage level 0.

As stated above, u_0 is zero in a symmetric three-phase system. With a multilevel inverter, the phase voltages are limited to achieve an amplitude between $[-M, M]$. If this restriction is taken into account together with the u_0=0, Equation (2.1) results in a varying maximum vector length from $3/2M$ to $\sqrt{3}M$. The maximum is achieved at the vector angle $\pm[30°, 90°, 150°]$ while the minimum is achieved at the angles $\pm[0°, 60°, 120°, 180°]$. Thus, the largest achievable circle will have a radius of $3/2M$. This is illustrated in Figure 2.2.

The largest circle that fits inside the voltage hexagon lattice is $\sqrt{3}M$ of radius, while the longest possible vector is $2M$. The longest vector can be achieved when two of the phases are at their maximum M and one phase is at its minimum $-M$, or vice versa.

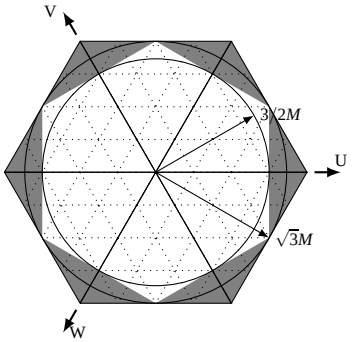


Figure 2.2. Largest possible circular loci of the voltage vector is $3/2M$ when symmetricity of phase voltages is maintained. The largest circle that fits inside the hexagon is $\sqrt{3}M$. In the shaded areas $u_0 \neq 0$. The voltage hexagon lattice in the figure is for the SCHBI with $M = 2$, and the values are normalized by using the nominal DC link voltage of a module as a reference.

To reach the largest circle inside the voltage hexagon lattice, Corzine and Baker (2001) suggested that a third harmonic is added to the phase voltage references. It is a viable method, but requires calculation of the angle of the reference vector and also calculation of sine at

an arbitrary angle. To reach the largest circle inside the voltage hexagon lattice with the MDCM, the zero component u_0 has to be set to other than zero, when no angle calculations are needed. In publication **I**, it is suggested that u_0 is selected to be the voltage exceeding the phase voltage maximum. Mathematically,

$$u_0 = -\text{sign}(u^*_{ph})(|u^*_{ph}| - M) \quad \text{where} \quad \{|u^*_{ph}| > M\}. \tag{2.4}$$

This results in a phase voltage waveform where no switchings occur during the switching period in which u_0 is used. The switchingless periods occur in both the positive and negative half cycle in a phase voltage and may extend from 60° to 120° and from 240° to 300°, respectively. The maximum length of a switchingless period is achieved when the largest circle fitting inside the lattice is used. This assumption neglects the overmodulation.

With the space vector pulse width modulation, the largest circle is not a problem, because the switching states are selected to be the three nearest vectors with respect to the reference vector. This will automatically take the zero component into account, but as a drawback, the zero component, which is the sum of phase voltages, is used throughout the voltage hexagon lattice, resulting in unsymmetrical phase voltages.

2.1.2 Original duty cycle modulation

In this section, an alternative method for the MDCM algorithm is suggested, which will ensure the use of the three nearest nodes and thereby improve the line-to-line voltage. The alternative method results in a similar modulation scheme as the one suggested in Corzine and Baker (2001), even though the mathematical formulation and the use of zero-component introduced here differ from the original DCM.

In contrast to the SVPWM schemes presented in the literature and the original DCM by Corzine and Baker (2001), the above-discussed MDCM scheme uses four nodes instead of three on the voltage hexagon lattice during the switching period as will be explained below. Figure 2.3 clarifies the difference between these modulation schemes. The use of four nodes affects the quality of the line-to-line voltage as will be shown in Section 2.3.

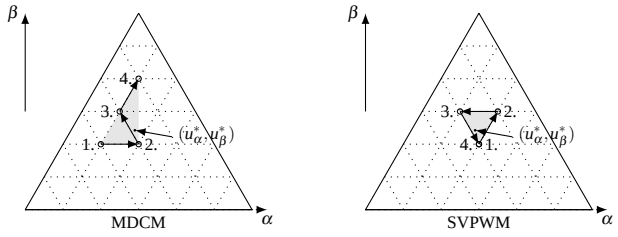


Figure 2.3. Nodes used by the MDCM and the SVPWM

The reason why the MDCM uses four nodes is explained by the following. All the phases start the switching period with a low phase state (see publication **I**). The phases switch to the high phase state consecutively so that the phase having the largest duty cycle switches to the high phase state first. The phase having the second largest duty cycle will switch next and the phase having the shortest duty cycle will be switched last. This will result in four nodes if all the phases have different duty cycles. It may also occur that some of the phases have equal duty cycles. In such a case, these two phases will switch at the same instant, when one of the nodes is not used. This unused node is always the third node, when the same area on the voltage hexagon lattice is still covered.

The MDCM can also be modified so that it will use only the three nearest nodes. This can be achieved with a simple modification to the MDCM algorithm discussed in **I** and in Section 2.1.1. After the phase voltage references are calculated by Equation (2.1) and the zero component is added, the number of modules is added to the phase voltage references. That is,

$$\begin{bmatrix} u^*_{\mathrm{U}} \\ u^*_{\mathrm{V}} \\ u^*_{\mathrm{W}} \end{bmatrix} = \begin{bmatrix} 1 & 0 & \frac{3}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{3}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix} \begin{bmatrix} u^*_{\alpha} \\ u^*_{\beta} \\ u_0 \end{bmatrix} + \begin{bmatrix} M \\ M \\ M \end{bmatrix} \tag{2.5}$$

Now, all the phase voltage references are positive. With these positive references, high and low phase states are selected by rounding the reference nearest to the lower and higher integer, respectively. The maximum voltage level gained is now $2M$ while the minimum voltage level is 0, which means that the phase states are also offset with M. The switching instants per phase can be calculated as in the MDCM from the fractional parts of the average phase voltages obtained by Equation (2.5).

After the phase states are obtained, the offset is removed. This will now result in phase voltages that are formed with low-high-low states with the positive phase references and high-low-high phase states with the negative.

Another drawback of the modified DCM algorithm is the use of u_0, which results in the prolonged use of switchingless voltage as explained in the previous section. The same is valid with the DCM. This use of a constant voltage level for a long time may result in a voltage drop in the DC links because all the DC links are directly connected to the load. This causes distortion in the phase current. The phase can be forced to switch during the use of the zero component if a result of Equation (2.4) is manipulated as

$$u_0 = -\operatorname{sign}(u^*_{ph}) \left(|u^*_{ph}| - M - u_{0+} \right) \quad \text{where} \quad \{|u^*_{ph}| > M\}, \tag{2.6}$$

where u_{0+} is a constant or some suitable function that maximizes the DC voltages in the modules. Other alternative to select u_{0+}, could be restriction on the maximum pulse width. If the maximum allowable pulse width is limited to, for example, 95 %, a switching at every switching period is ensured. The use of an additional zero component restricts the maximum achievable phase voltage average, and therefore, the value should be less than 0.5. The selection of u_{0+} is left for further studies.

2.2 Equal load sharing among the modules of a single phase

The energy used by the load is taken from the grid, and the DC link capacitors of the inverter are used as buffers. The inverter output voltage level is dependent on the electrical charge, or energy, stored in the DC link capacitor. With the SCHBI, the energy is divided between multiple DC links. One task of the modulation algorithm is to share the energy flow evenly between the capacitors, which will result in balanced DC link voltages between the modules.

Various carrier-based PWM schemes have been proposed in the literature, the target of these being to share the load between the modules as discussed in Section 1.2. Sharing the load with the SVPWM, DCM, or MDCM schemes can be executed with a voltage formation method including module circulation introduced in publication **I**. A short review of the voltage formation method and an alternative method are presented in this section also.

The analysis in this section is made by comparing the DC link voltages in a single-phase SCHB inverter, which is controlled by the carrier-based PWM or a voltage formation method described in publication **I** and later in this section.

2.2.1 Duty cycle modulation with module circulation

The DCM, MDCM, and SVPWM algorithms are based on sampling of a vector at a constant rate. The sampling rate is the apparent switching frequency. The sampled voltage is the average voltage that should be produced during the switching period T_{sw}. The voltage of the modules can be arranged in many different ways, still resulting in the same voltage average.

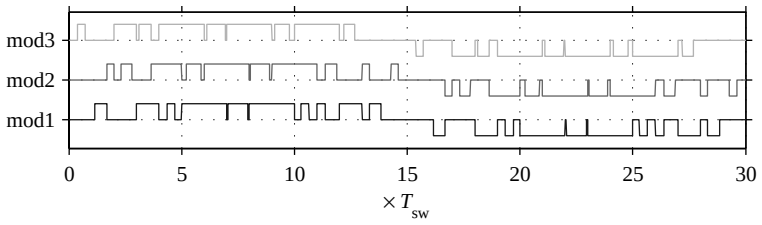
The equal loading of the modules requires that the modules have to alternate in voltage production. Every module has to take part in the voltage production at least in every M^{th} switching period to share the load evenly in the long run. The obvious choice to arrange the voltage formation is to make the pulse with one module while the other modules produce the necessary number of levels. In other words, one module carries out both the $t_{1\mathrm{st}}$ and the $t_{2\mathrm{nd}}$ switching while other modules do not switch at all during T_{sw}. The pulse-producing module is changed for the next switching period. The method is referred to as *module circulation 2*, while the *module circulation 1* denotes the voltage formation discussed in publication **I** and later in this section.

The module voltages of a seven-level inverter modulated with module circulation 2 are shown in Figure 2.4 together with the output voltage of the inverter. The apparent switching frequency is selected to be the same as the frequency of the carriers in the carrier-based PWM method analyzed in Section 1.2.1.

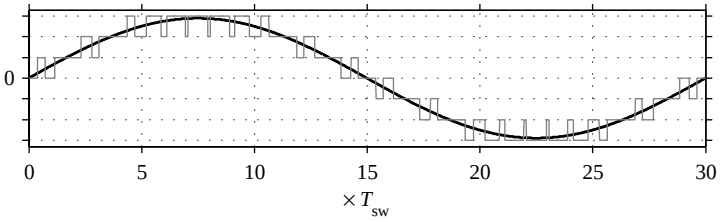
Another method to form the voltage, module circulation 1, is proposed in publication **I**. In this method, one module carries out the first switching at $t_{1\mathrm{st}}$ while one of the other modules will carry out the second switching at $t_{2\mathrm{nd}}$. The rest of the modules participate in the voltage production by producing the required number of levels. This is valid when the formation of

the voltage requires more than one module. When u^*_{ph} is below the first voltage level, the voltage is formed with one module, which carries out both switchings. The module voltages and the output voltage of this method are illustrated in Figure 2.5.

Comparing these two methods, the obvious difference is the number of switchings required to produce the voltage. Even though the module circulation 2 is more straightforward to

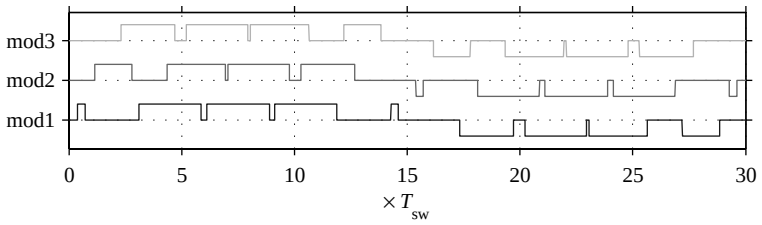


(a) Module voltages

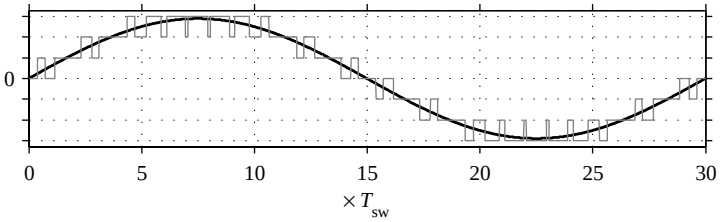


(b) Modulated phase voltage and reference

Figure 2.4. Module voltages and output voltage of the module circulation 2.



(a) Module voltages



(b) Modulated phase voltage and reference

Figure 2.5. Module voltages and output voltage of the module circulation 1.

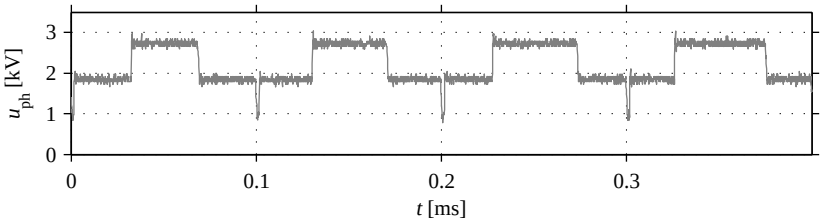


Figure 2.6. Voltage spikes at the measured phase voltage produced by the module circulation 2 when moving form one switching period to another. The switching period is 0.1 ms.

implement, the other method minimizes the number of switchings required to produce the same voltage waveform.

Nonidealities of the power switches require the use of a safe time between the switching commands of the upper and lower switches of an arm. The safe times on the other hand result in the use of minimum pulses, which restricts the modulator not to give commands in a shorter interval than the minimum pulse allows. With the module circulation 1, the use of the minimum pulse is necessary only close to the zero voltage and the maximum voltage, because otherwise one module does not switch consecutively in a short interval. In the module circulation 2, the minimum pulse is required throughout the voltage range, since the pulsed voltage is produced with one module.

The module circulation 2 introduces yet another problem, which is caused by the nonidealities of the power switches. The safe times between the upper and lower switches of the arm result in variation in the output voltage pulse timing when considering the load and no-load situation of an H-bridge. When the load current is flowing through the switch, the turn-off is faster than that of the no-load switch. Therefore, at the end of the switching period, the module that is producing the pulse and that holds the active state during the next switching period will turn active later than the module that produces the pulse in the next switching period will turn passive. This will show in a phase voltage as extra switchings or voltage dips. The measured phase voltage with module circulation 2 is shown in Figure 2.6, where the spikes at the switching period limits have been caused by this nonideality. The spikes are as wide as is the safe time set between the switches.

2.2.2 Simulation results

A thorough analysis of the voltage quality of the carrier-based PWM methods is given in McGrath and Holmes (2002); nevertheless, the issue of voltage balance is not discussed in the paper.

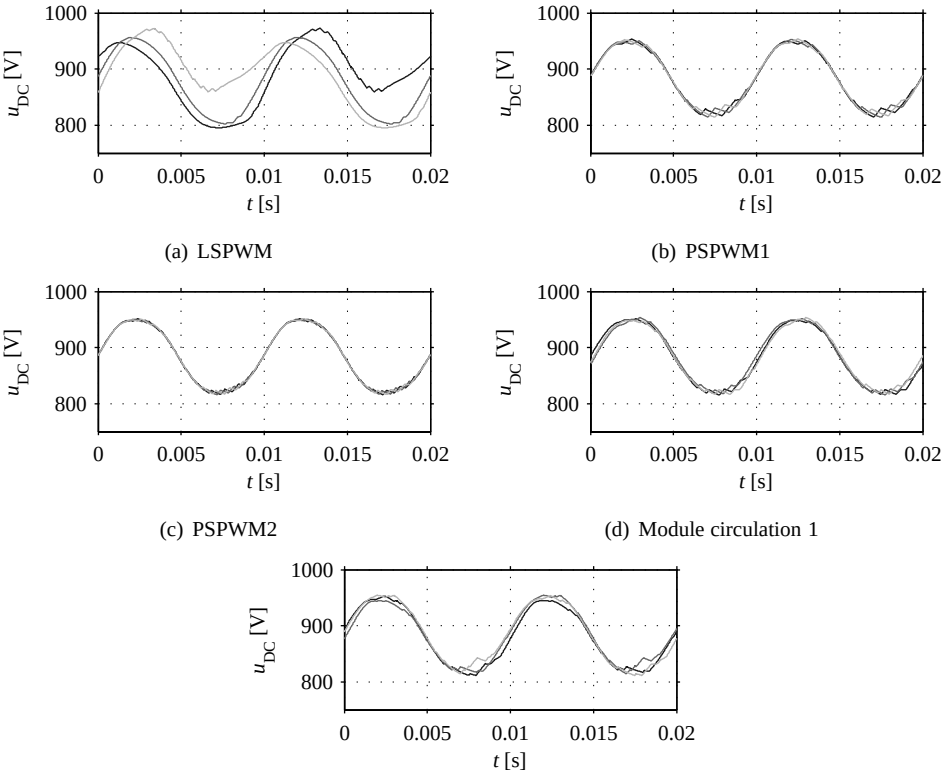
To compare the capabilities of the modulation algorithms to share the load among modules, a single-phase simulation model of an SCHBI was constructed. The parameters of the inverter model correspond to the prototype parameters, and as a load, a series RL circuit was used.

The load caused a 20° phase-shift between voltage and current. The apparent switching frequency was selected to be 2 kHz, which is also the frequency of the carriers in the PWM methods. The DC link voltages with all five modulation methods are shown in Figure 2.7.

The DC link voltages with the LSPWM show that the level-shifted carrier methods are not suitable for the modulation of the SCHBI. This has already been shown in several reports, such as McGrath and Holmes (2002), but the issue is investigated also here for comparison.

Both PSPWM methods keep the voltage balance well throughout the voltage range, even where the module circulation methods fail. The PSPWM2 performs best because of the higher apparent switching frequency. One module participates in the voltage formation approximately for half of the duration compared with other methods. This is an advantage, because the difference between the DC link voltages of an active module and a passive module will vary less compared with the longer switching period modulation.

Both the PSPWM1 and the module circulation 1 result in a very good voltage balance. The



(a) LSPWM

(b) PSPWM1

(c) PSPWM2

(d) Module circulation 1

(e) Module circulation 2

Figure 2.7. Simulated DC link voltages of one phase with different modulation and voltage formation schemes.

module circulation 2 on the other hand lets the module voltages diverge considerably at the highest loads, which can be seen in Figure 2.7(e) near the deepest voltage drop of the DC links. One module is in the passive state twice during the switching period while other modules are under a heavy load all the time. During these passive states, the module draws energy from the network, and its voltage rises rapidly, because the voltage difference between the capacitor and the grid voltage is high. This causes a voltage unbalance between the modules for a short time. After a few switching periods, the voltage balance has recovered.

2.3 Comparison of modulation methods

In this section, the DCM, the MDCM, and the SVPWM are compared. First, the phase voltages produced by the modulators are analyzed. Before the current spectra are drawn and analyzed, the line-to-line voltages are compared. Finally, the common-mode voltages of the different modulators are given.

Simulations in this section are made with a Simulink model including a three-phase seven-level inverter with constant DC link voltages. The voltage in the DC links is selected to be 900 V which is also selected to be $\hat{u}_{\mathrm{dc}}$. The apparent switching frequency is 2 kHz and the reference frequency is 50 Hz. A three-phase series RL circuit is used as a load. The load caused a 20° phase shift between the phase voltage and the current at this frequency. The amplitude of the voltage vector reference is used as a parameter, and the amplitudes used are shown in Figure 2.8. The amplitudes $4.5 \times \hat{u}_{\mathrm{dc}}$, $4.6 \times \hat{u}_{\mathrm{dc}}$, and $5.195 \times \hat{u}_{\mathrm{dc}}$ are selected to be compared. The amplitude $4.6 \times \hat{u}_{\mathrm{dc}}$ is selected, because it represents the case where the MDCM and the DCM has exceeded the limit of the zero component usage, which is $4.5 \times \hat{u}_{\mathrm{dc}}$. The reference vector locus with radius of $5.195 \times \hat{u}_{\mathrm{dc}}$ is selected, because it is very close to the largest possible circle inside the voltage hexagon lattice with $M = 3$. When the reference vector amplitude exceeds the largest possible circle, an overmodulation is required. The overmodulation is, however, ruled out from this thesis and is suggested for future work.

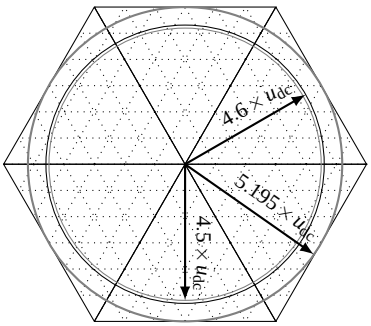
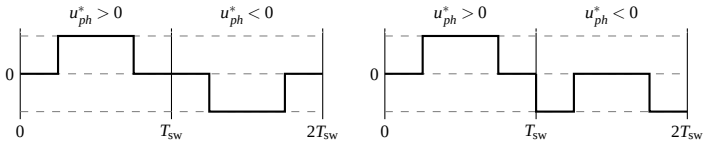


Figure 2.8. Simulated references.

2.3.1 Phase voltages

The DCM and the MDCM are developed from the phase voltage point of view, while the SVPWM is a vector-based solution. Therefore, the phase voltages produced by the SVPWM and the DCM or the MDCM differ from each other. DCM and MDCM modulate the output voltage so that the phase voltage references of all phases are met. The phase voltage references are formed according to the reference vector. The SVPWM, such as Lauttamus and Tuusa (2007) have presented, does not consider the phase voltage averages at all. The phase voltage is formed by selecting the first switching state and then moving from node to node by changing the voltage level in some phase. All the nodes used during one switching period enclose the reference vector. The switching instants are calculated to meet a geometric average, which should correspond to the reference vector.

The pulse pattern in the phase voltage of the MDCM is symmetric with respect to the zero voltage level. Both the negative and positive voltage is formed by starting and ending the switching period with a low state, and the high state is used in the middle. On the contrary, the phase voltage of the SVPWM or the DCM is not symmetric with respect to the zero voltage. The positive voltage is formed as with the MDCM, but when the reference is negative, the voltage is formed so that the switching period begins and ends with a high phase state and the low state is used in the middle. The difference in phase voltages is illustrated in Figure 2.9, where both the positive and negative voltages are formed during one switching period by a method used in the MDCM and in the SVPWM and the DCM.



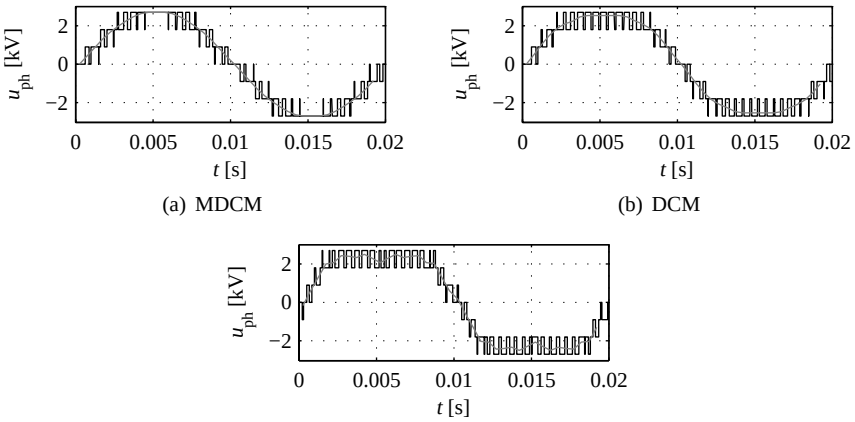
(a) MDCM (b) SVPWM or DCM

Figure 2.9. Difference between phase voltage formations used with the MDCM and the DCM, or the SVPWM.

The simulated phase voltages with the DCM, the MDCM, and the SVPWM are shown in Figures 2.10 and 2.11 for the amplitudes of $4.6 \times \hat{u}_{\mathrm{dc}}$ and $5.195 \times \hat{u}_{\mathrm{dc}}$, respectively. Both the modulated voltage and the resulting phase voltage average are depicted in the figures.

As explained in publication **I** and in Section 2.1, the MDCM adds a zero component u_0 to every phase reference when one of the phases exceeds its maximum achievable voltage. This occurs near the corners of the voltage hexagon lattice. With the circular reference vector loci, u_0 is added occasionally when the vector length exceeds 75% of the absolute maximum achievable voltage. For a seven-level inverter, this limit is $4.5 \times \hat{u}_{\mathrm{dc}}$. The addition of u_0 can also be seen in the phase voltages. The voltage remains at the same level as long as u_0 is used. In Figure 2.10, the phase voltage reference exceeds the maximum only for a short duration at the peak voltage while the largest circle requires an extensive use of u_0 (see Figure 2.11).

The DCM formulated in Section 2.1.2 is based on the MDCM. Hence, the zero component is

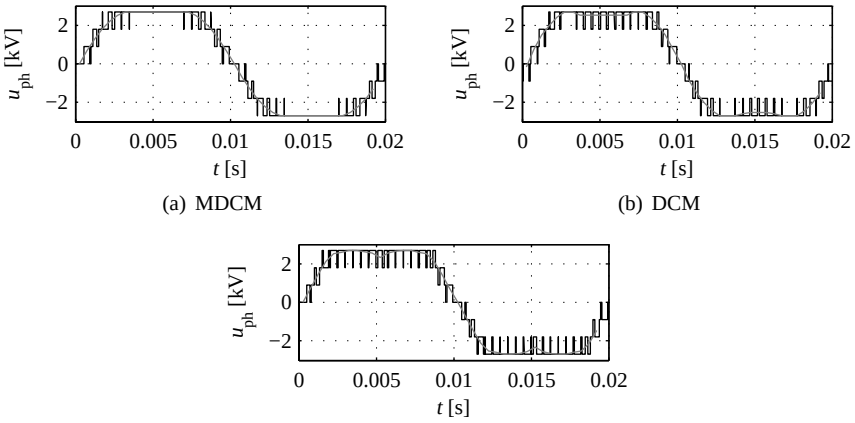


(a) MDCM (b) DCM

(c) SVPWM

Figure 2.10. Phase voltage waveform with the MDCM, the DCM, and the SVPWM when the amplitude of the reference vector is $4.6 \times \hat{u}_{dc}$. *The gray line indicates the low-pass filtered voltage. A moving average filter with a length of the switching period was used.*

also used in this modulation scheme. In Equation (2.6), an extra component u_{0+} is suggested to be added to the zero component calculated similarly as in the MDCM. Here, the component is selected to be constant $u_{0+} = 0.2$. This constant ensures that the voltage remains pulsed during the use of the zero component, and the resting DC link will have time to regain its charge. As a drawback, the produced average voltage in the phase becomes limited to the value $|M - u_{0+}|$. The use of u_{0+} limits the modulable area on the voltage hexagon lattice



(a) MDCM (b) DCM

(c) SVPWM

Figure 2.11. Phase voltage waveform with the MDCM, the DCM, and the SVPWM when the amplitude of the reference vector is $5.195 \times \hat{u}_{dc}$. *The gray line indicates the low-pass filtered voltage. A moving average filter with a length of the switching period was used.*

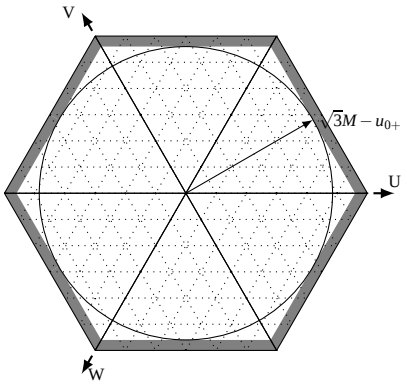


Figure 2.12. Limitation of the area on the voltage hexagon lattice caused by the use of u_{0+}.

so that the overmodulation region is reached with a smaller amplitude of the voltage vector. Normally, the overmodulation is required when the voltage vector exceeds the borders of the lattice. To reach the borders of the lattice, full voltage in two of the phases is required, and to reach the corners, full voltage in all of the phases is required. Therefore, restricting the phase voltage below the full voltage rules out an area near the borders of the lattice as is illustrated in Figure 2.12.

In contrast to the MDCM and the DCM, the SVPWM produces highly distorted voltage averages in the phases. A third harmonic is clearly visible in the low-pass-filtered waveform of the voltage, since the voltage dips at the instant at which the peak value should be. Actually, the third harmonic amplitude is about 20% of the fundamental wave with both of the simulated vector trajectories, as can be seen in Figures 2.13 and 2.14, where the harmonic contents of the voltage waveforms are given. With the lower amplitude of the reference vector, the 9^{th} and 15^{th} harmonics have a notable amplitude causing a significant ripple to the produced phase voltage averages.

The symmetricity with respect to the zero voltage level in the voltage pulse pattern can be regarded as an advantage, because a symmetric voltage performs clearly better when considering the spectra of the voltage. This can be noticed by comparing the phase voltage spectrum of the MDCM and the SVPWM or the MDCM and the DCM shown in Figures 2.13 and 2.14. The voltage spectrum of the MDCM has a considerably lower harmonic content compared with the unsymmetric voltage methods. Especially the third harmonic is almost negligible when the amplitude of the reference vector is $4.6 \times \hat{u}_{\mathrm{dc}}$. Actually, the third harmonic will be even lower, if the reference vector is shortened below $4.5 \times \hat{u}_{\mathrm{dc}}$. The third harmonic amplitude should be very near to the value of u_0 since the third harmonic in a three-phase system represents the average of the phase voltages. The third harmonic of the MDCM remains lower compared with the SVPWM even though the reference vector follows the largest possible circle. As was pointed out above, achieving the largest circle requires the MDCM to use u_0 extensively, but the value of u_0 will remain below $u_{\mathrm{dc}}/2$.

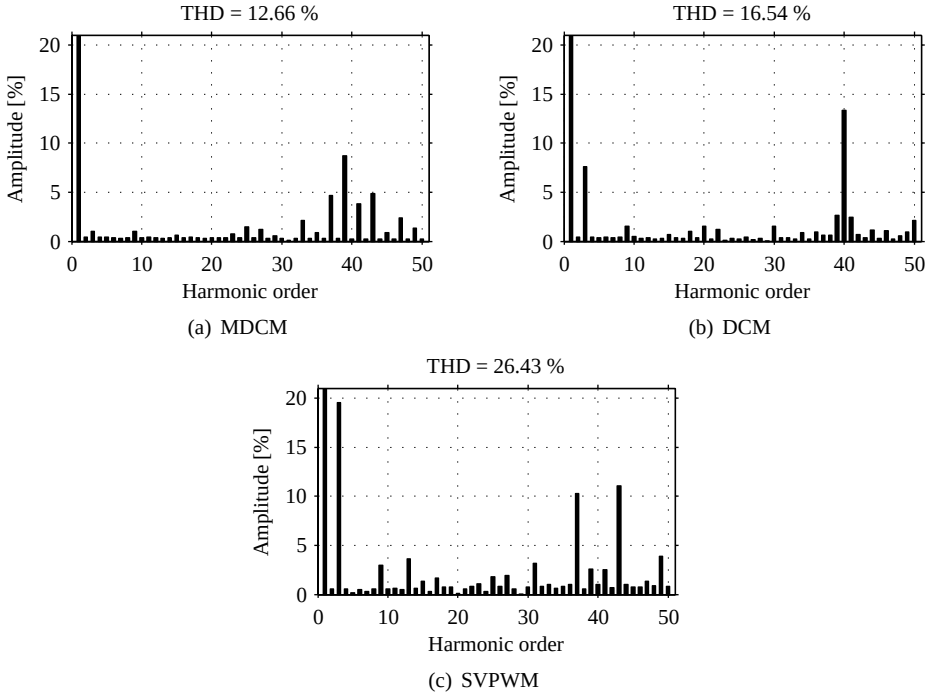


Figure 2.13. Spectra of the phase voltages with the MDCM, DCM, and the SVPWM. The amplitude of the reference vector is $4.6 \times \hat{u}_{\mathrm{dc}}$.

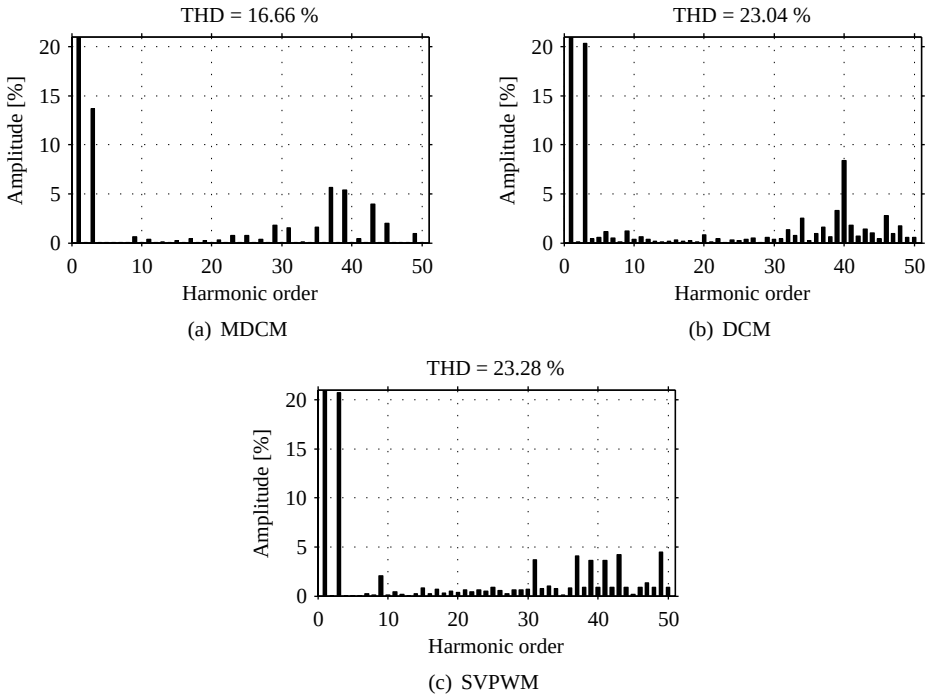


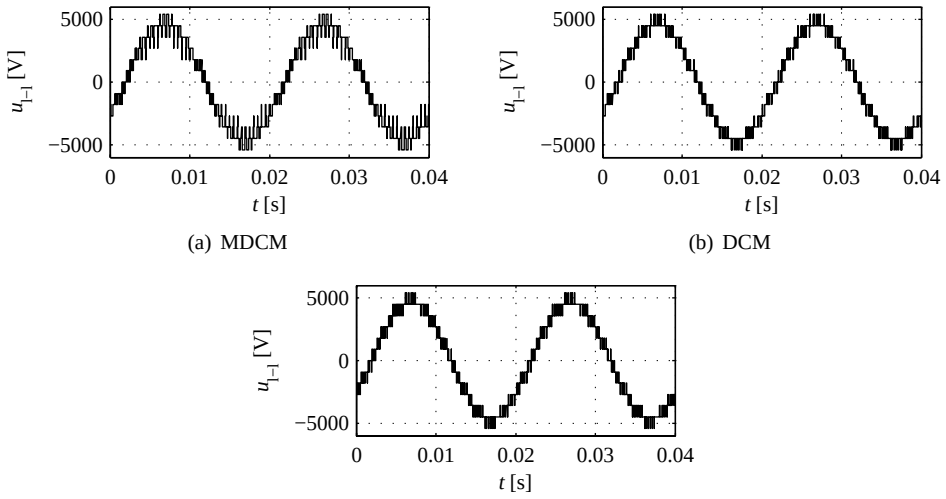
Figure 2.14. Spectra of the phase voltages with the MDCM, the DCM, and the SVPWM. The amplitude of the reference vector is $5.195 \times \hat{u}_{\mathrm{dc}}$.

The spectrum of DCM contains also the third harmonic, but its amplitude remains lower compared with the SVPWM. When the largest circle is followed, the DCM induces harmonics that other two modulations do not produce. These harmonics are for example the 5^{th},7^{th},9^{th},11^{th}, and 17^{th}, even though the amplitude of all of these harmonics remains below 1.5%.

2.3.2 Line-to-line voltage

The advantage of the use of the three nearest nodes is that the line-to-line voltage is smoother. No two-level steps occur in either the phase or line-to-line voltage. This can be seen in Figures 2.15 and 2.16, where the simulated line-to-line voltages of the MDCM, the DCM, and the SVPWM are shown with the reference vector amplitude of $4.5 \times \hat{u}_{\mathrm{dc}}$ and $5.195 \times \hat{u}_{\mathrm{dc}}$, respectively.

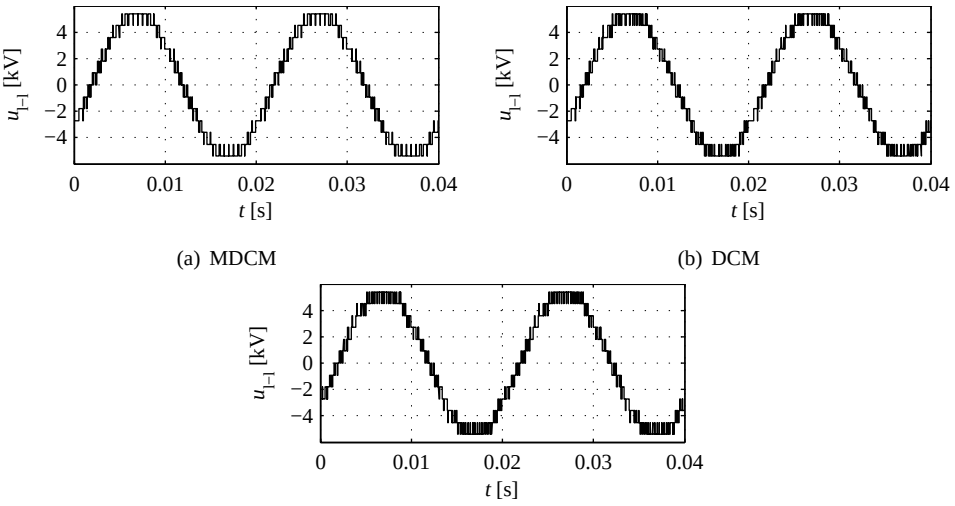
The two-level steps in the phase-to-phase voltages reflect to the voltage hexagon lattice as the use of four nodes during one switching period. These nodes of the MDCM spread to a wider area than that of the SVPWM or the DCM. This is shown in Figure 2.17, where the nodes are shown for all three modulation methods with the reference vector following the largest circle, and in contrast to the previous analysis, with a length of $4.49 \times \hat{u}_{\mathrm{dc}}$. The latter reference was selected to show the MDCM when no zero component is used. The usage of the zero component removes the need for a pulsed voltage in one of the phases, and therefore, one of the nodes to be used. When u_0 is used throughout the reference circle, the MDCM uses the three nearest nodes, just as the other two modulation methods do.



(a) MDCM (b) DCM

(c) SVPWM

Figure 2.15. Line-to-line voltages with the MDCM, the DCM, and the SVPWM when the amplitude of the reference vector is $4.5 \times \hat{u}_{\mathrm{dc}}$. *Two-level steps occur with the MDCM.*

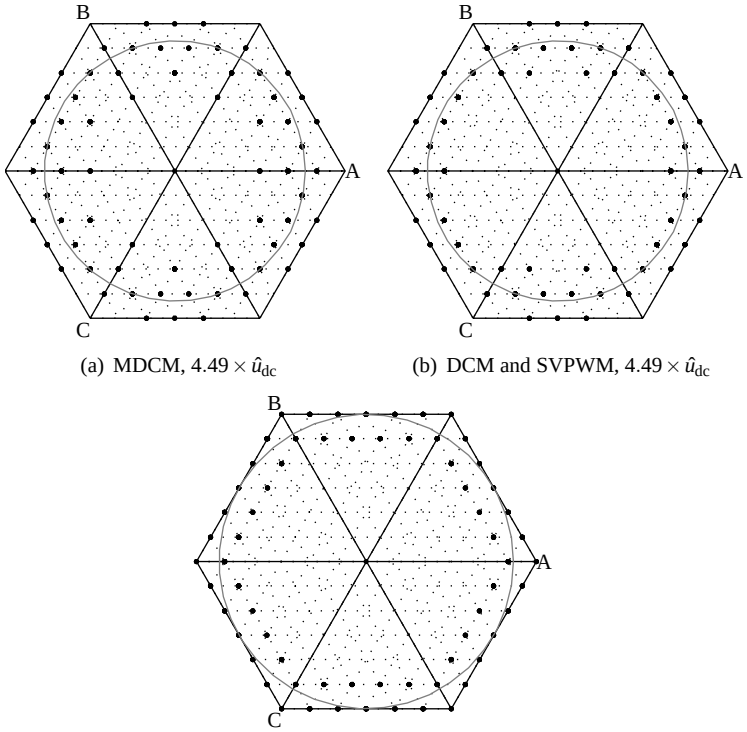


(a) MDCM

(b) DCM

(c) SVPWM

Figure 2.16. Line-to-line voltages with the MDCM, DCM, and the SVPWM when the amplitude of the reference vector is $5.195 \times \hat{u}_{\mathrm{dc}}$*. No two-level steps occur in the MDCM any more.*



(a) MDCM, $4.49 \times \hat{u}_{\mathrm{dc}}$

(b) DCM and SVPWM, $4.49 \times \hat{u}_{\mathrm{dc}}$

(c) MDCM, DCM, and SVPWM, $5.195 \times \hat{u}_{\mathrm{dc}}$

Figure 2.17. Nodes used with the MDCM, the SVPWM, and the DCM with $u_{0+} = 0$*.*

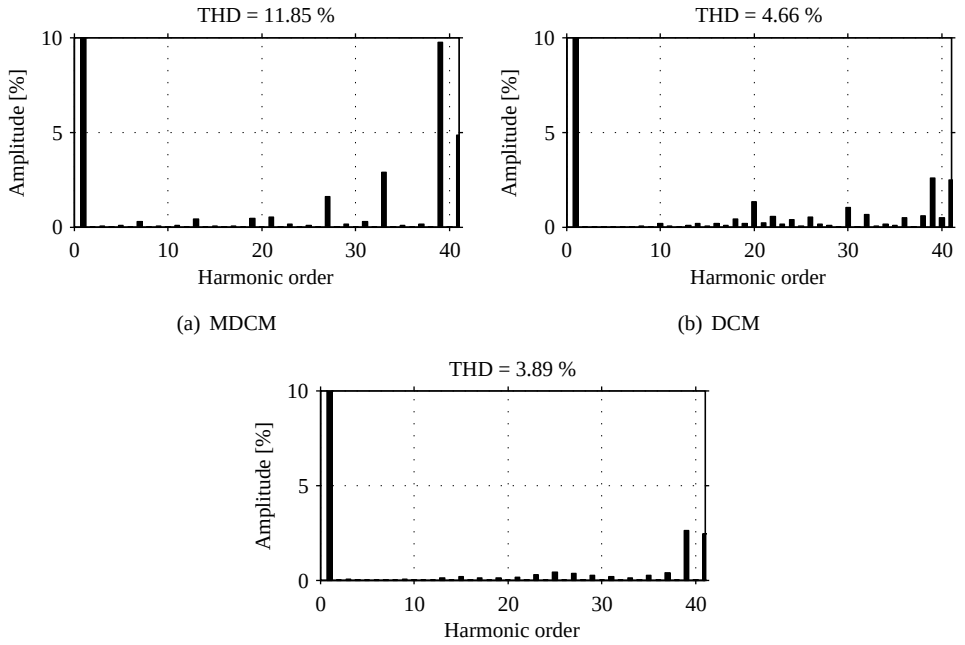
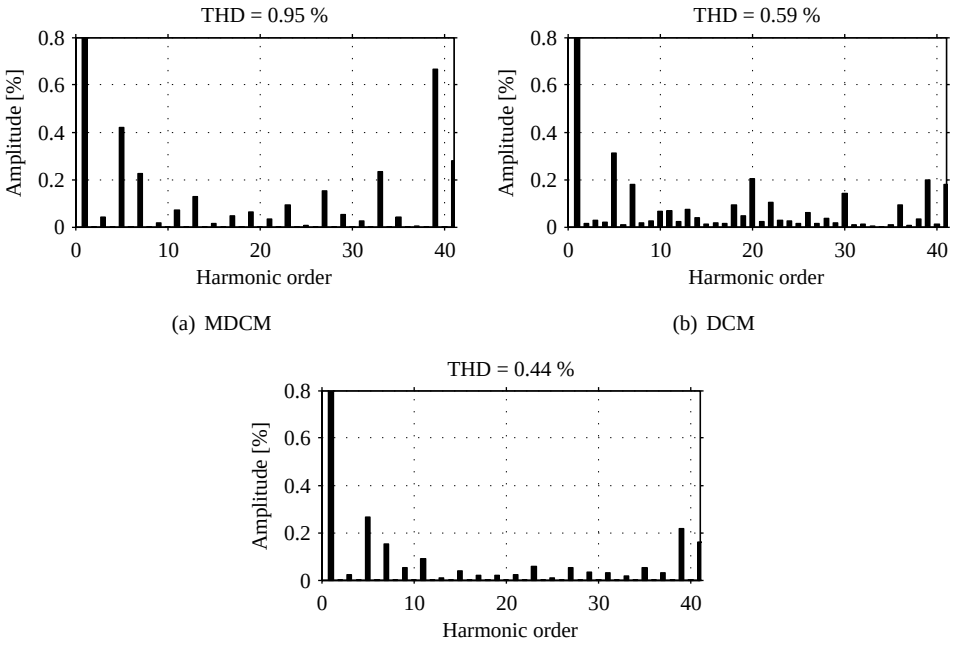


Figure 2.18. Spectra of line-to-line voltage with the MDCM, the DCM, and the SVPWM. The amplitude of the reference vector is $4.5 \times \hat{u}_{\mathrm{dc}}$

The spectra of line-to-line voltages for $4.5 \times \hat{u}_{\mathrm{dc}}$ are shown in Figure 2.18. The MDCM is the only modulation method under consideration, which shows the fifth and seventh harmonic in the line-to-line voltage. Its total harmonic distortion is also more than double of the THD of the other two modulation methods. The two-level steps in the line-to-line voltage cause the harmonics near the switching frequency to increase. The 39^{th} harmonic of the MDCM has an amplitude of 10 %.

2.3.3 Current spectrum

The previous sections showed that the MDCM, the DCM, and the SVPWM produced voltages of different quality. In this section, the modulation algorithms are compared from the current point of view. Current waveforms with all three modulation schemes are obtained by simulating the seven-level inverter with constant DC links and a series RL circuit as a load. The load was set to cause a 10° phase shift between voltage and current at the fundamental frequency. The apparent switching frequency was selected to be 2 kHz and the amplitude of the reference vector $4.6 \times \hat{u}_{\mathrm{dc}}$ at 50 Hz. The harmonic content of the current for all three modulation schemes is shown in Figure 2.19. Also the corresponding total harmonic distortion (THD) is shown in the figure for every modulation scheme. Fifty first harmonics are included



(a) MDCM

(b) DCM

(c) SVPWM

Figure 2.19. Current spectra with the MDCM, the DCM, and the SVPWM. The amplitude of the reference vector is $4.6 \times \hat{u}_{\mathrm{dc}}$

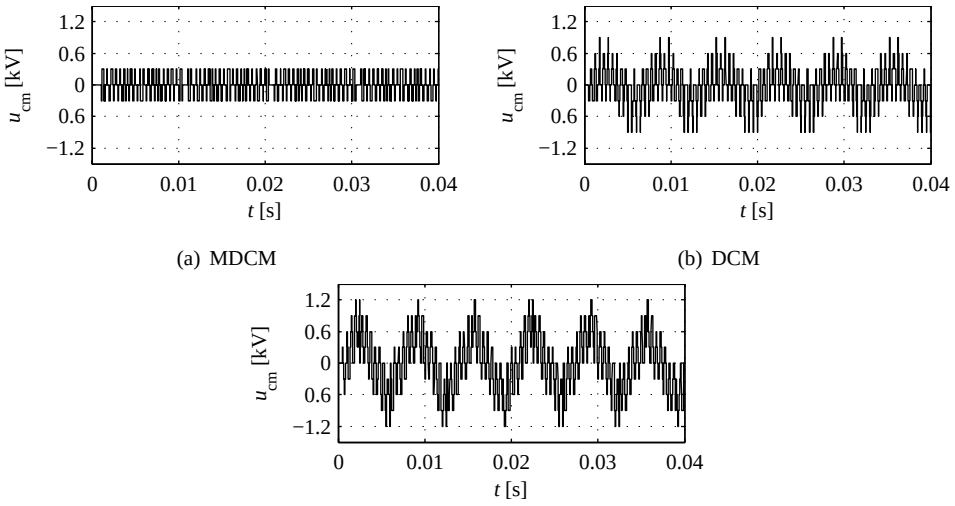
in the THD.

Comparing the current THDs of the modulators, the MDCM produces the most distorted current while the SVPWM produces the current with the lowest distortion. A notable difference between the MDCM and other two modulators is the amplitude of the fifth, seventh, and thirteenth harmonic. A similar behavior can seen in the spectrum of line-to-line voltage in Figure 2.18. Also the MDCM causes a ripple, the frequency of which is near the apparent switching frequency. This kind of a ripple with as high an amplitude is not seen with the other two currents under comparison. The DCM causes even-order harmonics in addition to odd harmonics, which are also caused by the MDCM and the SVPWM.

2.3.4 Common-mode voltage

A high-frequency common-mode voltage induced by the inverter is one of the main causes for bearing currents in inverter-fed drives. The bearing currents cause premature failures of the machine bearings (Chen et al., 1996; Särkimäki, 2009).

The common-mode voltages of the SVPWM and the MDCM differ dramatically from each



(a) MDCM

(b) DCM

(c) SVPWM

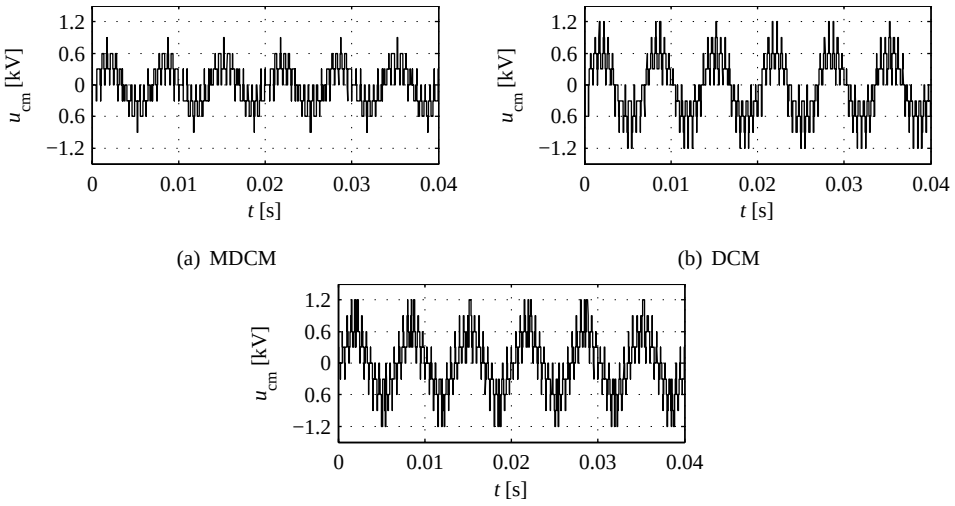
Figure 2.20. Common-mode voltage with the MDCM, the DCM, and the SVPWM. The amplitude of the reference vector is $4.6 \times \hat{u}_{\mathrm{dc}}$

other, which can be noticed by comparing the spectra of the phase voltages of the SVPWM and the MDCM in Figure 2.13. The third harmonic in the phase voltage of a three-phase system is actually the common-mode voltage. The SVPWM produces phase voltages with a high third-harmonic content, but the third harmonic of the MDCM remains moderate with the lower amplitude of the reference vector. One can come to the same conclusion by comparing the common-mode voltages shown in Figure 2.20. The common-mode voltages of the figure are calculated from simulated phase voltages by Equation (1.4).

Comparison of the common-mode voltage produced by the SVPWM at the reference vector amplitude of $4.6 \times \hat{u}_{\mathrm{dc}}$ and $5.195 \times \hat{u}_{\mathrm{dc}}$ shows that there is no difference in the amplitude of the common-mode voltage. The MDCM produces a significantly lower common-mode voltage at $4.6 \times \hat{u}_{\mathrm{dc}}$ than at the largest circle.

2.4 Voltage quality improvement

In Section 2.2, methods to share the load equally among the modules of one phase of an SCHBI were discussed. The results showed that the voltage levels in each module are fairly well balanced between each other. Regardless of the balance, the voltage in the DC links still fluctuates with a considerable amplitude. The fluctuation is a result of small-capacitance DC links and the fact that the returning magnetic energy in the motor cannot be shared between all the three phases of the inverter.



(a) MDCM

(b) DCM

(c) SVPWM

Figure 2.21. Common-mode voltage with the MDCM, the DCM, and the SVPWM. The amplitude of the reference vector is $5.195 f \hat{u}_{\mathrm{dc}}$

The fluctuation has to be taken into account and compensated in the modulation algorithm. For carrier-based PWM algorithms, multiple fluctuation reduction methods have been proposed. For example Kouro et al. (2006) gave a good analysis of both the LSPWM and the PSPWM. In publications **II** and **III** a compensation algorithm appropriate for the MDCM, DCM, and the SVPWM is suggested. Here, only the main ideas behind the compensation method are discussed to help the understanding of the results analyzed at the end of this section.

In a three-phase two-level inverter, a current path from one phase to the other phases is ensured. Thus, the reactive power traveling from one phase of the motor toward the inverter is transferred to other phases. This keeps fluctuation of the DC link voltage moderate in the traditional two-level inverter DC link capacitor dimensioning. When the same inverter is used as a single-phase H-bridge inverter, the capability to handle reactive power will change considerably. The returning reactive power will pass through the free-wheeling diodes to the DC link of a single-phase H-bridge inverter. This energy will accumulate with the energy already stored in the capacitor and result in a voltage increase over the DC link. The voltage will continue to increase as long as the voltage and the current have opposite signs. If the voltage is allowed to increase without limit, it will finally result in a breakdown in the DC link capacitor. This can be avoided either by a four-quadrant front-end in the inverter or by a break resistor.

When the current sign turns to the same sing as the voltage has, the energy stored in the DC link capacitor begins to travel from the inverter toward the motor. At the same instant, the voltage over the capacitor begins to decrease. The voltage decreases until either the energy flow changes its direction or the grid begins to feed the H-bridge via the diode-bridge.

The described energy flow ends up in oscillating, or fluctuating, voltage in the DC link of a module. The oscillation is at the frequency of twice the frequency of the output voltage (Perez et al., 2005). The amplitude of the fluctuation depends on the capacitance of the capacitor, the amplitude of the load current, and the phase shift between voltage and current. The phase shift and amplitude of the current are dependent on the load, but the capacitance is a design parameter. If the capacitance is increased, the amplitude of the fluctuation will decrease. The size of the capacitor is a matter of cost, and the capacitance is preferably kept as small as possible. The benefit of a modular structure and the ability to use commercial inverter modules in an SCHBI might also be lost if large-scale modifications to the modules need to be made before installation. Yet again, this is a matter of cost.

The DC link voltage in every module is time varying. The module circulation used with the MDCM or the SVPWM keeps the voltages inside a phase fairly well balanced. In a three-phase system, the phases have a 120° phase shift, which makes the DC links between the phases fluctuate with a 60° phase-shift. Therefore, the DC link voltages between the phases are not equal.

The main task of the modulator is to calculate the switching instants that produce the output voltage corresponding to the reference as accurately as possible. The fluctuation will cause the modulator to calculate erroneous switchings if the actual DC link voltage is not taken into account. This will lead to an erroneous output voltage of the inverter and may cause the controller to fail. It is essential for the controller, for example in flux estimating controls, that the produced voltage is as close to the reference as possible.

In a two-level inverter, the DC link voltage can be taken into account when forming the reference vector. The DC link voltage is used only to scale the voltage hexagon, because all the phases form their output voltages from the same DC link voltage. With the scaled voltage hexagon, the switching instants are easily calculated to accurately correspond to the reference (Sarén, 2005).

For single-phase multilevel inverter, for example Kouro et al. (2006) have developed a compensation method for the DC link voltage fluctuation based on the LSPWM and the PSPWM. The method is based on scaling the amplitude of the module carrier with the actual value of the DC link. A three-phase analysis is not discussed in the article because the method is not viable with the space-vector-based PWM methods.

As explained in Section 1.2, the voltage hexagon lattice of a multilevel inverter is formed from the switching states. Several redundant switching states may point to the same node. This is of course the case when all the modules have equal voltages in their DC links. When the DC link voltages differ from each other, the redundant switching states do not produce the same vector anymore. This will deform the voltage hexagon lattice, and the produced voltage vector will be dislocated if the modulator assumes ideal DC link voltages. An example of this dislocation is shown in Figure 2.22, where one node is highlighted with all its redundant switching states. The vectors that are produced with the unideal DC link voltages are also depicted in the figure for all the redundant switching states. As can be seen, the produced states are dislocated and scattered around the node. This dislocation occurs differently around

every node as a function of time. Therefore, the compensation algorithm is significantly more complicated compared with a two-level inverter.

Compensation of the fluctuation can be made phase-by-phase as is proposed in publications **II** and **III**. In this case, the reference vector is divided into its phase components, which are time-averaged voltages for each phase. The time averages can be obtained either by the MDCM, or the SVPWM. Obtaining the time averages by the MDCM is a straightforward task: u^*_{ph} includes the necessary information. The average voltages with the SVPWM on the other hand have to be calculated with the switching states and switching instants.

2.4.1 Compensation with different voltage formations

Publications **II** and **III** suggest the compensation algorithm assuming that voltage is formed during the switching period with two switchings allocated symmetrically with respect to the middle of the switching period. This kind of a voltage formation is illustrated in Figure 2.23(b), and it is widely used with the SVPWM methods and also with the MDCM. The equations for the switching instant calculation are derived in Appendix A.1. The first switching instant $t_{1\text{st}}$ can be calculated as

$$t_{1\text{st}} = \frac{(u^*_{ph} - u_{t_{\text{on},2}})T_{\text{sw}}}{u_{t_{\text{on},1}} - 2u_{t_{\text{on},2}} + u_{t_{\text{on},3}}}, \tag{2.7}$$

where $u_{t_{\text{on},1}}$, $u_{t_{\text{on},2}}$, and $u_{t_{\text{on},3}}$ are actual voltage levels, which are produced with the measured DC link voltages.

If the switching frequency of an IGBT f_{IGBT} has to be lowered, the voltage has to be formed differently. An obvious choice to reduce f_{IGBT} is to form the voltage during T_{sw} with only one switching. This results in asymmetric voltage formation as shown in Figure 2.23(b). In this case, the switching instant calculation in the compensation method differs from the one presented in the publications, and in Equation (2.7). Because only two voltage levels are used during the switching period, the equation for the switching instant simplifies to

$$t_{1\text{st}} = \frac{(u^*_{ph} - u_{t_{\text{on},2}})T_{\text{sw}}}{u_{t_{\text{on},1}} - u_{t_{\text{on},2}}}. \tag{2.8}$$

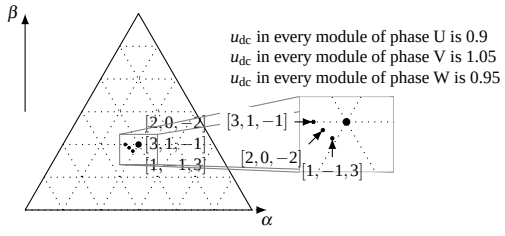
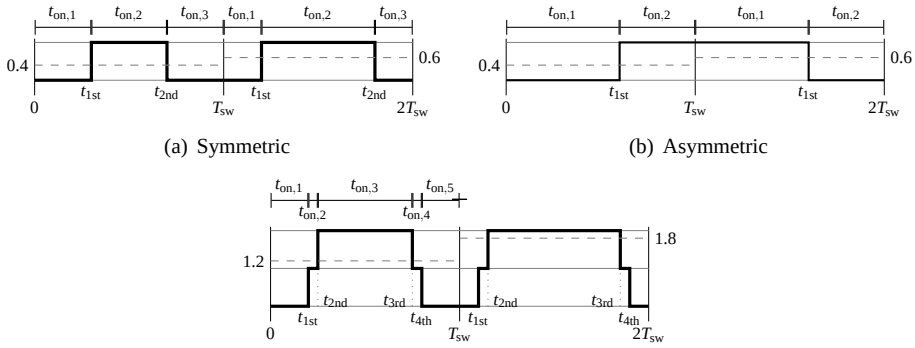


Figure 2.22. Example of dislocation of the node produced with redundant switching states when the DC link voltages are not ideal.



(a) Symmetric (b) Asymmetric

(c) Multiple switchings

Figure 2.23. Different voltage formation methods during the switching period.

The derivation for the equation is given in Appendix A.2.

Chapter 3 and publications **V** and **VI** propose a modulation scheme that mitigates the oscillating overvoltages after switchings. The modulation is based on voltage formation where two consecutive switchings are made in the same direction. The voltage formation is illustrated in Figure 2.23(c). This will also result in a switching instant calculation that differs from the one presented in publications **II** and **III**, because of four switchings per period occur. The first switching instant can be calculated with

$$t_{1\mathrm{st}} = \frac{(u^*_{ph} - u_{t_{\mathrm{on},3}})T_{\mathrm{sw}} - (u_{t_{\mathrm{on},2}} + u_{t_{\mathrm{on},4}} - 2u_{t_{\mathrm{on},3}})\Delta t_{\mathrm{sw}}}{u_{t_{\mathrm{on},1}} + u_{t_{\mathrm{on},5}} - 2u_{t_{\mathrm{on},3}}}, \tag{2.9}$$

the derivation of which is given in Appendix A.3. The other switching instants are symmetrically aligned in the switching period, and the equations for them are also given in the appendix.

2.4.2 Effect of apparent switching frequency

In publications **II** and **III**, the simulation and the results measured with the apparent switching frequency of 10 kHz are given. The error caused by the deviation of the DC link voltage during the switching period remains moderate or even negligible, because the duration of the switching period is short. Such a high switching frequency introduced to the high power motor is somewhat useless, since the motor time constants (either electronic or mechanical) are slow compared with the switching period. Therefore, a lower apparent switching frequency should be considered in high-power applications.

The selection of apparent switching frequency affects the successfulness of the compensation algorithm, since the DC links have a notable slope during the switching period. This causes an error to the produced voltage or the location of the produced voltage vector. Next, the

modulated voltage vector is investigated with $f_{\mathrm{sw}} = 2$ kHz and $f_{\mathrm{sw}} = 8$ kHz. Three modulation methods, the MDCM, the DCM, and the SVPWM were simulated and the results are plotted in Figures 2.24, 2.26 and 2.27, respectively. The simulation model consists of a three-phase seven-level SCHB inverter with parameters similar to the prototype (see Table 1.1). A series RL circuit dimensioned to match the nominal load of the inverter was used as a load. The load caused a 20° phase shift between the phase voltage and the current. The amplitude of the reference vector used in the simulations is $4.5 \times \hat{u}_{\mathrm{dc}}$ with a 50 Hz frequency.

The produced voltage vectors are attained by calculating the integral of the modulated phase voltages per switching period and calculating the voltage vector with inverse of the transformation presented in Equation (2.1).

The amplitude error is shown as a percentage value and for the base value, the amplitude of the reference vector, is used. The amplitude error is calculated by subtracting the amplitude of the produced vector from the amplitude of the reference vector and dividing the result by the amplitude of the reference vector. The error in the angle is obtained by subtracting the angle of the produced voltage vector from the angle of the reference vector.

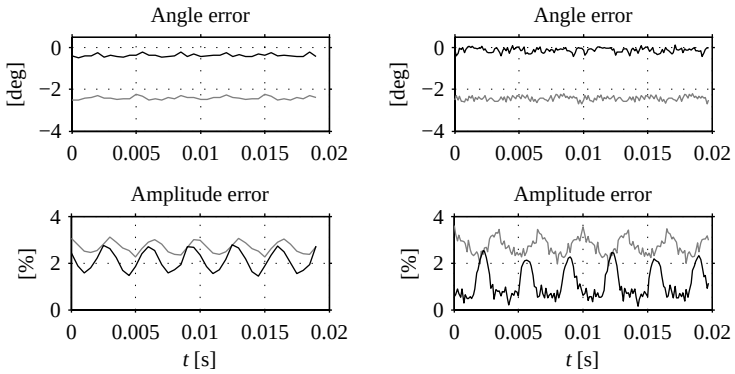


Figure 2.24. Error in the modulated voltage vector with the MDCM. The black line illustrates the compensated vector.

Figure 2.24 shows the error in the produced vector when the MDCM is used as the modulation method. The compensation algorithm will make the error of the angle of the produced vector nearly negligible regardless of the apparent switching frequency. The amplitude error on the other hand is highly dependent on f_{sw}. The average error in amplitude with $f_{\mathrm{sw}} = 2$ kHz is reduced only slightly by compensation. The compensated produced average voltage is erroneous, because the switching instants are calculated assuming that the DC link voltages do not vary during the switching period. As stated above, the DC link voltages with such small capacitance modules will have a considerable slope during the switching period. The slope of the DC link voltages cause inaccuracy to the produced average voltage. The inaccuracy becomes higher when the length of the switching period is increased. This is illustrated in Figure 2.25.

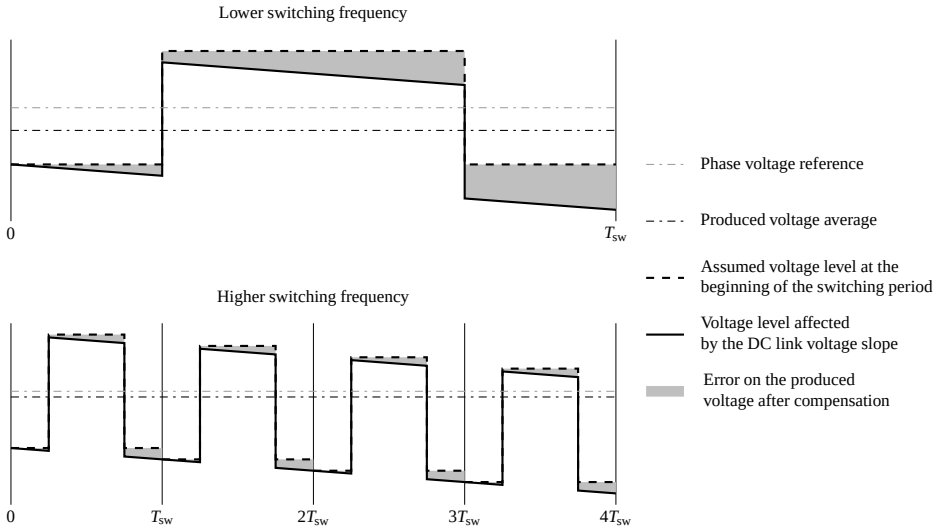
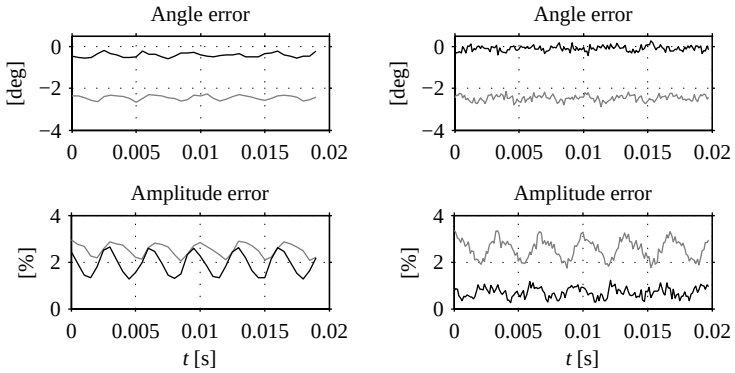


Figure 2.25. Principle of the error in the produced voltage caused by the DC link voltage fluctuation during the switching period. The error per switching period is smaller with a higher switching frequency.

Another alarming feature is the deviation in the amplitude. The deviation should be reduced with the compensation, but with both of the switching frequencies the MDCM will result in a higher amplitude deviation in the amplitude. This deviation will also cause deviation in the flux of the motor, and therefore, the flux estimator of the controller may fail. The deviation in the amplitude originates from the use of the zero component. With the MDCM, one of the phases does not switch at all for multiple consecutive switching periods, which shows as a hump in the amplitude error with $f_{\mathrm{sw}} = 8$ kHz. Even though the compensation algorithm itself uses the u_0 to fine-tune the location of the produced voltage vector.

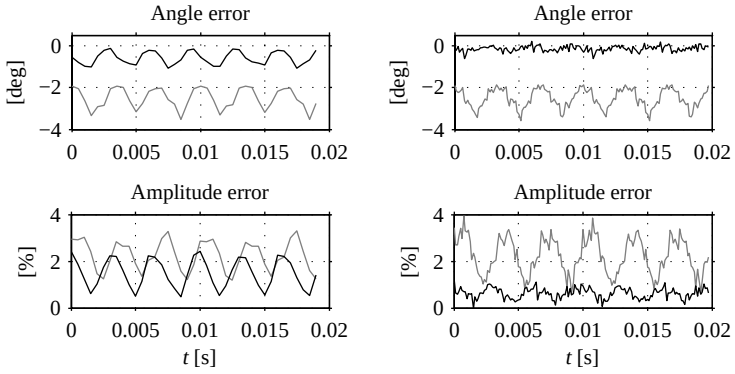
Figure 2.26 shows the error in the produced vector when the DCM is used as a modulation method. The compensation algorithm applied to the DCM behaves as with the MDCM when the lower investigated apparent switching frequency is used. The angle error is reduced close to zero with the compensation, but the amplitude of the produced vector deviates more than that of the uncompensated vector. Even so, the average error on the amplitude of the vector is reduced. The notable difference between these two modulation methods is in the amplitude error with $f_{\mathrm{sw}} = 8$ kHz. The amplitude error is well compensated with the DCM. The error, and most importantly the error deviation (as a function of time), in the amplitude and in the angle of the produced vector remains moderate. The compensation algorithm can be perceived to be successful with the DCM, if the apparent switching frequency is high enough.

When the fluctuation of the DC links is not taken into account with the SVPWM, the error in the produced vector is considerably higher than that of the MDCM or the DCM. This can be noticed by comparing the error waveforms of the uncompensated vectors in Figure 2.27 with Figures 2.24 and 2.26. The comparison shows that the DC link voltages will fluctuate more



(a) f_{sw}= 2000 Hz (b) f_{sw}= 8000 Hz

Figure 2.26. Error in the modulated voltage vector with the DCM. The black line illustrates the compensated vector.



(a) f_{sw}= 2000 Hz (b) f_{sw}= 8000 Hz

Figure 2.27. Error in the modulated voltage vector with the SVPWM. The black line illustrates the compensated vector.

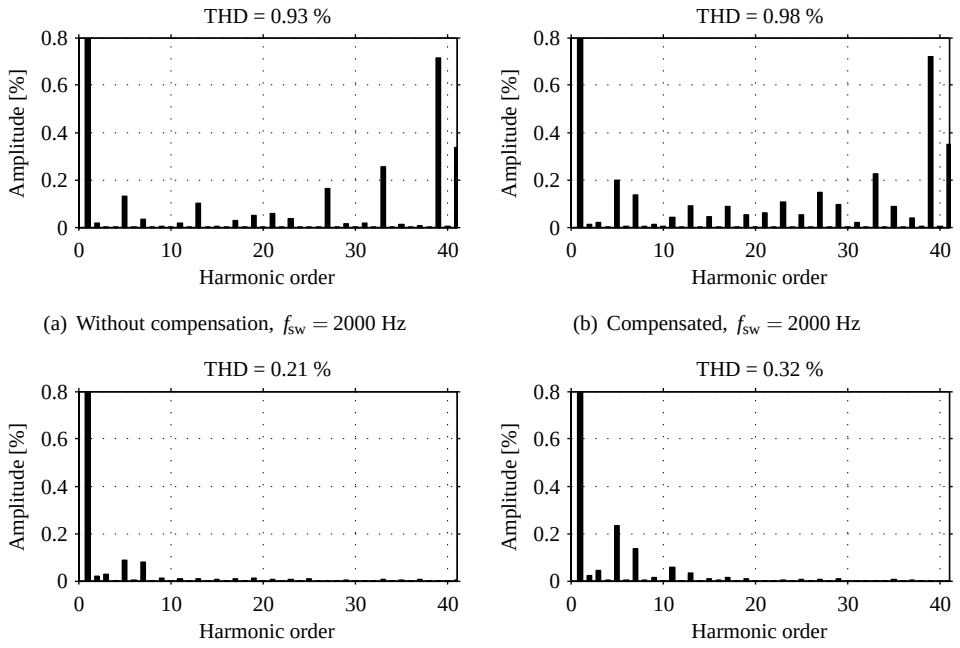
with SVPWM than with other two modulation methods. Therefore, the compensation of the fluctuating DC link voltages is of the essence for the SVPWM.

When the compensation algorithm is applied to the SVPWM and f_{sw} is high, the vector is produced as accurately as with the DCM. With a lower f_{sw}, the deviation in the amplitude of the compensated vector is more than 1.5 %, whereas the other two modulation methods remain below 1 %.

2.4.3 Current spectrum

The compensation method affects the quality of the current. The simulation model described in the previous section was used to obtain the current waveforms analyzed here. The analyzed phase current was approximately 23 A with the reference vector amplitude $4.5 \times \hat{u}_{\mathrm{dc}}$ at 50Hz. The same apparent switching frequencies used in the previous section were used here also. The harmonic analysis was conducted from data, the length of which equals one second. Total harmonic distortion (THD) was also calculated. For $f_{\mathrm{sw}} = 2$ kHz, fifty first harmonics are included in the THD, and 200 first harmonics for 8 kHz. This way, also the switching frequency is taken into account in the THD. The results are depicted in Figures 2.28, 2.29, and 2.30 for MDCM, DCM, and the SVPWM, respectively.

The current spectra with the MDCM are shown in Figure 2.28. Regardless of the fact that the uncompensated voltage vector produces a larger average error compared with the compensated one, the harmonic content of the current in the compensated case is worse. The deviation in the amplitude error with the MDCM is increased by the compensation algorithm, which results in an increase in the THD of the current. The fifth and seventh harmonics and several other higher-order odd harmonics are higher than those of the uncompensated case. The third harmonic with the MDCM is now increased by the compensation, because of the



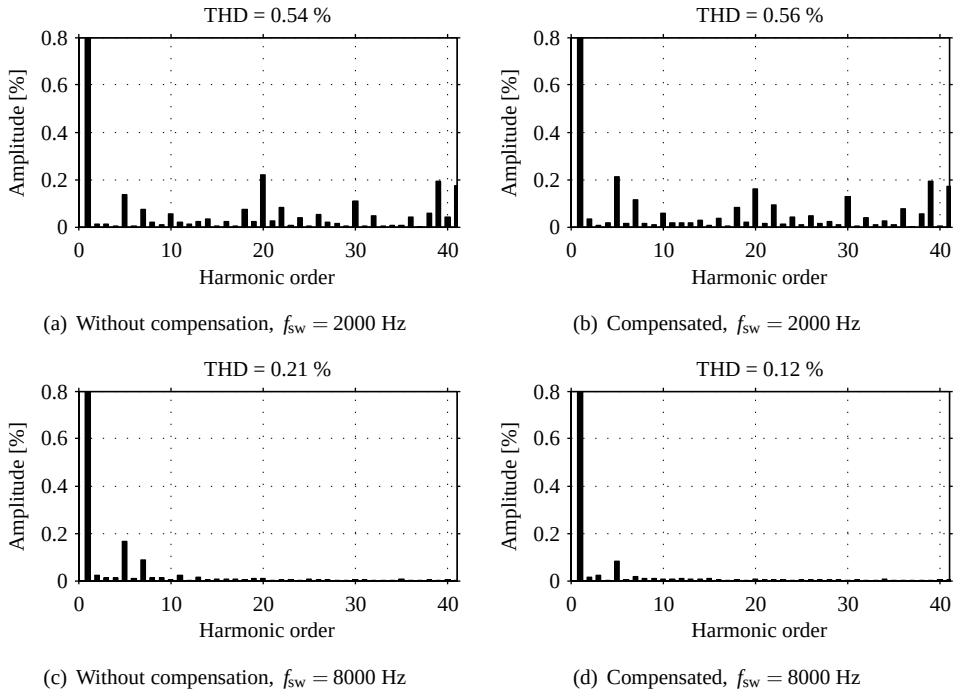
(a) Without compensation, $f_{\mathrm{sw}} = 2000$ Hz

(b) Compensated, $f_{\mathrm{sw}} = 2000$ Hz

(c) Without compensation, $f_{\mathrm{sw}} = 8000$ Hz

(d) Compensated, $f_{\mathrm{sw}} = 8000$ Hz

Figure 2.28. Spectra of the simulated phase current with the MDCM. The amplitude of the reference vector is $4.5 \times \hat{u}_{\mathrm{dc}}$.



(a) Without compensation, $f_{\mathrm{sw}} = 2000$ Hz

(b) Compensated, $f_{\mathrm{sw}} = 2000$ Hz

(c) Without compensation, $f_{\mathrm{sw}} = 8000$ Hz

(d) Compensated, $f_{\mathrm{sw}} = 8000$ Hz

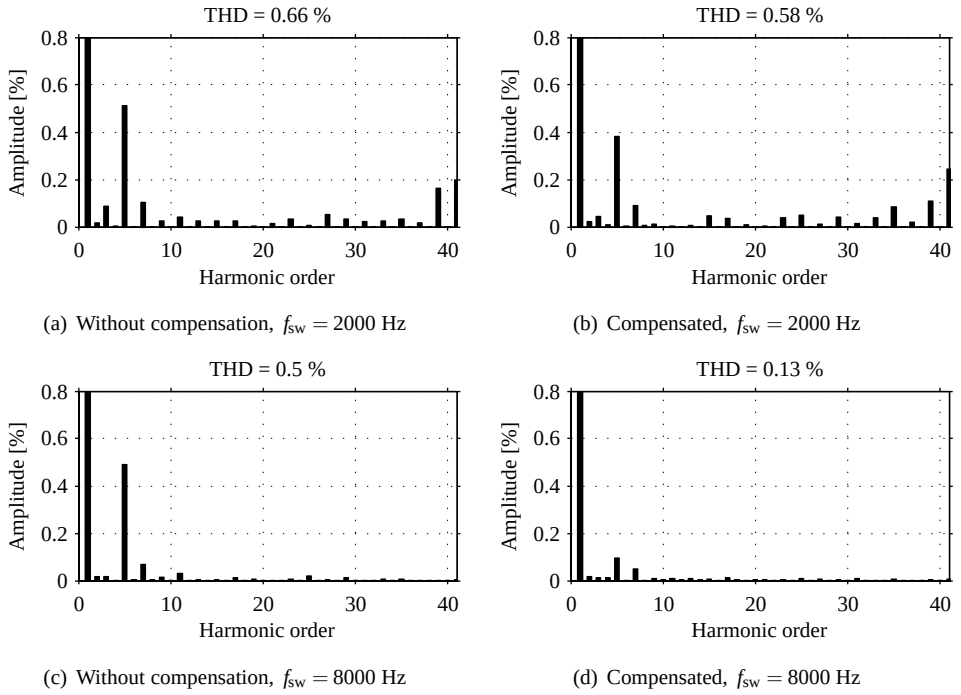
Figure 2.29. Spectra of the simulated phase current with the DCM. The amplitude of the reference vector is $4.5 \times \hat{u}_{\mathrm{dc}}$.

use of u_0. A zero component is added, because one of the phases does not have enough voltage reserve because of the fall of the DC link voltages.

In contrast to the MDCM, the compensation algorithm applied to the DCM improves the current quality at the higher f_{sw} as shown in Figure 2.29. The fifth harmonic is nearly halved, while the seventh harmonic becomes absent. Considering the lower apparent switching frequency, the fifth and seventh harmonics are increased slightly by the compensation, resulting in a slightly higher THD. Comparing the current THD of DCM with other two modulation methods, the DCM provides the lowest THD.

The benefit of the DC link compensation applied to space vector modulation is clear when comparing the current spectra in Figure 2.30. As the error in vector production showed, the SVPWM fails in accurate voltage production. This can be also noted in the current spectra. Regardless of the switching frequency, the amplitude of the fifth harmonic of the current is considerable without compensation. At the lower switching frequency, also the third and seventh harmonics are present. When the compensation is turned on, the current quality of the SVPWM is improved substantially even though it does not achieve the level of the DCM.

The fact that the DCM produces a lower THD current than the SVPWM is contradictory to the results in Section 2.3.3. This is explained by the fact that the space vector PWM causes



(a) Without compensation, $f_{sw} = 2000$ Hz

(b) Compensated, $f_{sw} = 2000$ Hz

(c) Without compensation, $f_{sw} = 8000$ Hz

(d) Compensated, $f_{sw} = 8000$ Hz

Figure 2.30. Spectra of the simulated phase current with the SVPWM. The amplitude of the reference vector is $4.5 \times \hat{u}_{dc}$.

more severe DC link voltage fluctuation than the DCM.

2.5 Operational restrictions on modulation

Publication **IV** discusses the dynamic performance of different voltage formation schemes when the modulation is restricted to take only one voltage level step at a time. The restriction is based on the oscillating overvoltages introduced to the motor terminals when a long feeder cable is used. A two-level step causes an oscillation that has a double amplitude compared with a one-level step. The higher the amplitude is, the higher is the risk for an insulation failure.

This kind of a restriction will limit the operation of the modulation during transients. A transient means a sudden change in the location of the voltage vector reference on the voltage hexagon lattice. If the reference vector moves outside the limited area described in the publication, a two-level step will definitely occur.

According to Kaukonen (1999), a dynamically demanding metal industry application requires that the drive can produce a torque change from zero to 70% of the nominal torque in 3.5 ms.

From a voltage vector point of view, this kind of a change in torque means that the vector has to turn tens of degrees in the corresponding time. If the flux of the motor is kept low during the no-load period, the amplitude of the voltage vector must also be increased to correlate with the load.

Whether the multilevel inverter can produce such a voltage change or not can be examined in the following. The boundary conditions are that only a one-level step change in a phase voltage is allowed at a time, and that the switching period begins and ends at the same voltage level. Let us next discuss a hypothetical example shown in Figure 2.5. The previous switching period of the seven-level inverter has ended in a switching state [3,-1,-1]. The voltage vector reference needs to be transferred for example by 78° as fast as possible. Because the phases can change only one voltage level at a time, several nodes have to be used during the transfer. The changes in the phase voltages and the nodes used are shown in the figure.

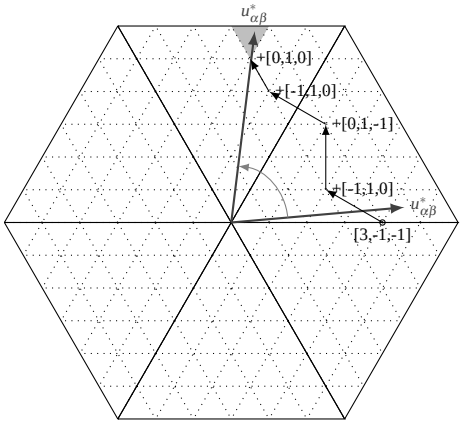


Figure 2.31. Example of how the nodes are used to change the location of the voltage vector when a rapid change in the reference takes place. The target triangle is shaded. The transfer begins from the switching state [3,-1,-1] and is followed by one voltage level steps simultaneously in two of the phases. After three switching periods, the target triangle is reached.

In the example, the first change is made at the beginning of the first switching period. The state is maintained for the period because of the second boundary condition set above. The next node is switched at the beginning of the second switching period. The nodes are selected so that two of the phases change their state simultaneously but in the opposite directions. Hence, the common-mode will not contain any high $\mathrm{d}u/\mathrm{d}t$ edges. This is continued until one of the nodes outlining the target triangle is reached. After the target triangle is reached, the modulation can continue its normal operation. This consideration is valid for a seven-level inverter. For inverters with a higher number of levels, more nodes have to be visited to make a similar change.

Based on the example, it can be deduced that the time spent on changing the location of the voltage vector depends on the sampling period T_{sw} and the number of nodes required to be visited. Assuming that the sampling period is 0.1 ms ($f_{\mathrm{sw}} = 10$ kHz), the three switching periods are then 0.3 ms. This is far less than the requirement for a dynamically demanding

metal industry application, and therefore more than adequate. For a seven-level inverter, it would be possible to lower the switching frequency down to 1 kHz, while still meeting the dynamic requirements.

2.6 Discussion

In this chapter, a modulation method called modified duty cycle modulation (MDCM) and its variations were discussed, analyzed, and compared with other well-known modulation methods. The MDCM produces the voltage vectors with an emphasis on the phase voltage waveforms. The phase voltage waveforms have a very low distortion below 75 per cent of the peak amplitude of the vector. Above the mentioned limit, a zero component is added, which results in a fact that the phase voltage may remain in the same state for a long period of time. Depending on the load current, this may cause a severe drop in the DC link voltages. In contrast to the MDCM, the SVPWM emphasizes the line-to-line voltages. The SVPWM performs the switchings throughout the voltage hexagon. With a voltage formation proposed in Section 2.2 of this thesis, the DC link capacitors will have time to "rest" during the switching period when the voltage is pulsed.

From the common-mode voltage production point-of-view, the MDCM performs better than the SVPWM. The common-mode voltage caused by the MDCM remains at the amplitude of one-third of u_{dc} when u_0 is not used. The common-mode voltage of the SVPWM has an amplitude of two-thirds of u_{dc} in the region where MDCM does not use u_0. This is caused by the use of redundant switching states with the SVPWM. The use of u_0 increases the amplitude of the common-mode voltage of the MDCM up to one u_{dc}, which is still exceeded by the SVPWM. The SVPWM will cause a $4/3u_{\mathrm{dc}}$ common-mode voltage maximum.

The voltages of the DC links fluctuate, which will affect the quality of the output voltage if not taken into account in the modulation. The erroneous voltage production may even result in a failure of the flux estimator in the controller. An extension that aims at compensating the mentioned error was proposed in Section 2.4. The suggested method compensates the error phase by phase by adjusting the switching instants. The method is shown to be applicable to the MDCM and SVPWM schemes.

As a conclusion, the DCM with the module circulation 1 and with compensation of DC link voltage fluctuation would be a good choice for a modulation method for an SCHBI. The voltage balance between modules is maintained and the fluctuation of the DC link voltages remains lower than of the space vector PWM. The vector production with the DCM is shown to be very accurate if the apparent switching frequency is selected to be high or the module capacitances large. The DCM also produces currents with the lowest distortion in comparison with the other two methods. Even though the space vector pulse width modulation produces the lowest THD line-to-line voltage, the difference to the DCM is small.

Chapter 3

Overvoltage mitigation with modulation

This chapter is an introduction to publications **V** and **VI**, in which oscillating overvoltages and their suppression in multilevel inverter drives are discussed. The basics of the oscillation phenomenon, including voltage reflection and the effects that overvoltages have on drives, are presented in Section 1.4.2.

In this chapter, the basic principles of the overvoltage mitigation methodology are first discussed in brief. Secondly, some previously unpresented analyses of the method are introduced including the effects of the mitigation on the line-to-line voltage and the common-mode voltage.

3.1 Mitigation methodology

The idea of the oscillation mitigation method was first proposed by Lee and Nam (2002) for two-level inverters, and further developed in publications **V** and **VI**. The mitigation is based on the use of the oscillations of two consecutive voltage edges (or in other words, switchings) to cancel each other. This is explained in detail in publication **V**, and also briefly discussed in the following and illustrated in Figure 3.1. The method is called *edge modulation* in publication **VI**.

First of all, the motor terminal voltage is a sum of the voltage levels introduced by the inverter and the oscillations caused by the reflection phenomenon. There can be multiple simultaneous oscillations in the cable of the drive, if the oscillations of the previous voltage edges have not attenuated before a new edge is launched to the cable. This existence of multiple simultaneous oscillations is exploited to achieve a lower peak value of the overvoltage. As shown

before, the mitigation is achieved with two consecutive voltage edges introduced to the cable. Neglecting the filtering properties of the cable, the second edge can be considered to be launched to the cable at the same instant when the first edge reflects back from the inverter terminals, resulting in a situation where both the two times reflected first edge and the second edge are traveling in the same direction, that is, from the inverter to the motor. The reflected voltage of the first edge has a negative polarity because of the reflection at the inverter terminals (Γ_S= -1). Both of these edges reflect from the impedance barrier at the motor terminals and accumulate into the total voltage. Because the reflected edges have opposite polarities, they will partly cancel each other resulting in a mitigated total voltage. The cancellation will not be complete, because the propagating first edge has attenuated more than the second edge owing to the reflections and the cable attenuation.

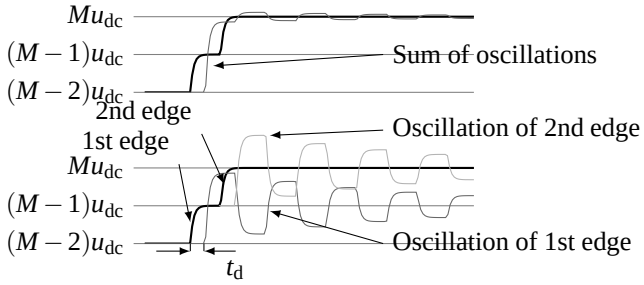


Figure 3.1. Principle of the mitigation method. Oscillations by the individual edges are summed, when a cancelling effect takes place.

The reduction in the peak amplitude of the overvoltage seen at the motor terminals is evident when comparing the voltage of the edge modulation and the normal modulation with an equal amplitude of the switched voltage. Consider that the modulation induces a voltage edge with an amplitude of $2u_{dc}$ to the cable. With the normal modulation, the edge results in a peak of the motor terminal voltage as high as almost $4u_{dc}$ because of the reflection. Extending the measured results in publication **V**, the motor terminal voltage will reach the peak of $3.6u_{dc}$ with the setup under investigation. With the edge modulation, the peak voltage will remain clearly below $2.5u_{dc}$ ($2.36u_{dc}$ with the setup in the publication). Thus, the overvoltage is reduced from nearly $2u_{dc}$ to less than $0.5u_{dc}$.

Comparing the edge modulation with the modulation that is restricted to switch only one voltage level at a time, the reduction will not be as clear as in the previous example, but the edge modulation still results in a better overvoltage behavior. The measured results in publication **V** show that the overvoltage is reduced from $0.8u_{dc}$ to $0.32u_{dc}$ by using the edge modulation.

In addition to the mitigation of the peak voltage, another advantage of the edge modulation is that the remaining oscillation will have a considerably lower amplitude compared with the normal modulation. As was stated in Section 1.4.2, the high $\mathrm{d}u/\mathrm{d}t$ voltage edges tend to cause extra stress on the first few turns in the windings. The oscillation after the inverter-induced voltage edge causes not only one, but multiple consecutive high $\mathrm{d}u/\mathrm{d}t$ voltage edges

to the motor terminals, even though the back and forth propagation of the voltage in the cable reduces the $\mathrm{d}u/\mathrm{d}t$ and amplitude in time. Each of these oscillation-originated voltage edges causes extra stress on the winding insulation and leads to a premature insulation failure.

3.2 Finding an optimal interval between the voltage edges

The interval between the consecutive edges launched from the inverter is the essence of the method. If the reflection phenomenon is considered from an ideal point of view as Lee and Nam (2002) did, the interval is $2t_\mathrm{d}$, which is the time taken for the first edge to travel from the inverter to the motor and back. The interval $2t_\mathrm{d}$ does not result in optimal mitigation in a real drive, but the residual overvoltage is suppressed only a little. This is shown in publication **V**. The time interval resulting in optimal mitigation (namely $\Delta t_\mathrm{sw}^\mathrm{opt}$) in a real drive, as shown in publication **V**, is greater than $2t_\mathrm{d}$. This is because the cable acts as a filter distorting the voltage as it keeps traveling back and forth in the cable. The $\mathrm{d}u/\mathrm{d}t$ of the second edge will be higher than that of the first edge at the instant when the second edge is launched to the cable.

A method to find an optimal time interval between the two voltage edges is proposed in publication **V**. The method requires a measurement of the motor terminal voltage of the drive when a voltage edge is launched to the cable. The measured oscillation u_osc is then used to find a value for $\Delta t_\mathrm{sw}^\mathrm{opt}$. A procedure to find the optimal time interval begins by calculating the peak value for the resulting voltage when the delayed u_osc is added to the non-delayed u_osc. The sum of these voltages is now denoted $\hat{u}_\mathrm{osc}$. Then, $\Delta t_\mathrm{sw}^\mathrm{opt}$ can be found by finding the time delay resulting in the minimum $\hat{u}_\mathrm{osc}$. The procedure in pseudocode is as follows:

```
1: Initialize u_max = 2 max(û_osc)
2: for Δt_sw = t_min to t_max do
3:    û_osc(t) = u_osc(t) + u_osc(t − Δt_sw)
4:    if max(û_osc(t)) < u_max then
5:       Δt_sw^opt = Δt_sw
6:       u_max = max(û_osc(t))
7:    end if
8: end for
9: return Δt_sw^opt
```

where t_min is an initial guess for the $\Delta t_\mathrm{sw}^\mathrm{opt}$ and is suggested to be $2t_\mathrm{d}$, while t_max is the maximum value for the time delay. The maximum value for the time delay is proposed to be less than the length of the measured oscillation. In publication **V** t_min is set to zero to show the behavior of the peak of the overvoltage as a function of Δt_sw.

3.3 Edge modulation algorithm

Publication **VI** proposes phase voltage formation methods exploiting edge modulation for multilevel inverters with a different number of voltage levels. The edge modulation is an extension of multilevel modulation schemes such as the SVPWM, the MDCM, or the DCM. It modifies the voltage levels and switching instants calculated by the modulation scheme so that the resulting phase voltages have mitigated oscillation after each switching, and the phase voltage reference is met.

The edge modulation uses voltage levels that are odd or even levels for odd and even number of modules in the inverter, respectively. These voltage levels are called active levels, since the average phase voltage is produced by them. For example if $M = 1$, the active voltage levels are -1 and 1, and therefore the modulated voltage resembles the modulated phase voltage of a two-level inverter. For $M = 2$, the active voltage levels are -2, 0, and 2, and therefore the output voltage resembles the voltage of a three-level inverter instead of a five-level inverter. The concept of active and passive levels is illustrated in Figure 3.2.

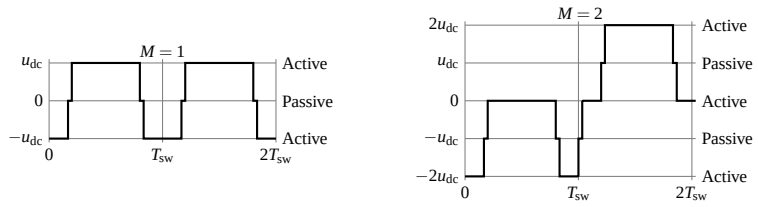


Figure 3.2. Concept of active and passive levels with a three-level inverter ($M = 1$) (left) and a five-level inverter ($M = 2$) (right).

Other than active voltage levels are used for the edge modulation during the transition from one active level to another. These levels are now called passive levels. For inverters with an odd number of modules, the passive levels are even levels, and for the inverters with even number of modules, the passive levels are odd levels. The time spent on the passive voltage level should be such that the transition from an active level to another active level minimizes the overvoltage seen at the motor terminal, that is, $\Delta t_{\mathrm{sw}}^{\mathrm{opt}}$. The concept of $\Delta t_{\mathrm{sw}}^{\mathrm{opt}}$ is discussed in brief in the Section 3.2 and further in publications **V** and **VI**.

The voltage levels calculated by the modulation algorithm (for example the SVPWM, the MDCM, or the DCM) are rounded to the active voltage levels. The rounding is made so that the average voltage remains between the active levels. After the active voltage levels are attained, the switching instants are redetermined to meet the reference. With an assumption of symmetric voltage formation, the correct switching instants can be easily obtained by modifying the duty cycle, or in other words, the on-time for the voltage level at the middle of the switching period. The duty cycle is modified by the following procedure:

Require: Symmetric voltage formation: *level1* = *level3*
1: **if** *level1* < *level2* **then**

```
  if u*_ph < passive level then
    d*_ph = d_ph/2
  else
    d*_ph = d_ph + (1 − d_ph)/2
  end if
else
  if u*_ph < passive level then
    d*_ph = d_ph + (1 − d_ph)/2
  else
    d*_ph = d_ph/2
  end if
end if
return d*_ph
```

The switching instants calculated from the duty cycle represent the instants when a two-level step would occur if the voltage was formed using only active levels without visiting a passive level. But with the edge modulation, the voltage is formed by the first switching from the active to passive level at $\Delta t_{\mathrm{sw}}^{\mathrm{opt}}/2$ earlier than the original switching instant. The second edge from the passive to another active level is switched $\Delta t_{\mathrm{sw}}^{\mathrm{opt}}/2$ after the original switching instant. By forming the voltage as described, the edge modulation does not affect the accuracy of modulation.

3.4 Zero common-mode voltage modulation with oscillation minimization

As shown in Section 1.4.2, the common-mode voltage is an average of the phase voltages. The common-mode voltage, and especially rapid changes in it, is one of the reasons for bearing currents in the drives, and is therefore harmful. A rapid change in the common-mode voltage is induced in the motor every time when only one of the phases changes its output voltage level. If the motor terminal voltage oscillates after the switching, the common-mode voltage will also oscillate. In this section, a modulation method, which keeps the oscillations in the common-mode voltage moderate, while the oscillations in line-to-line voltage are mitigated, is discussed.

With multilevel inverters, it is possible to arrange the phase voltages so that the common-mode voltage will be zero at all times (Zhang et al., 2000; Rodriguez et al., 2004). This is based on the fact that some nodes on the voltage hexagon lattice have such redundant switching states that the sum of the phase voltages is zero. Zhang et al. (2000) propose a carrier-based PWM for common-mode elimination, while Rodriguez et al. (2004) introduce an SVC method, where the zero common-mode node closest to the reference vector is used. These nodes are highlighted in Figure 3.3.

By observing the switching states of the nodes, one can notice that moving from any zero

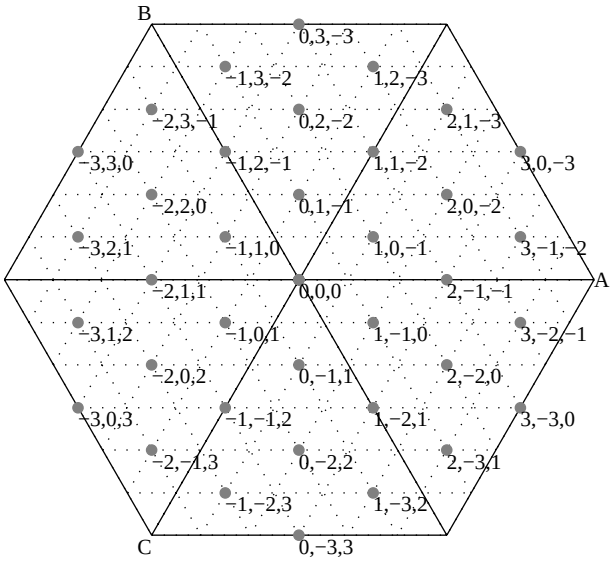


Figure 3.3. Nodes that can be produced with a zero common-mode voltage. The switching states which give a zero common-mode voltage are given beside the nodes.

common-mode node to another requires a one-level change in two of the phases. As an example, let us consider the node, the zero common-mode switching state of which is (2,0,-2). It is surrounded by six zero common-mode nodes, the states of which can be obtained by adding a combination of step changes in two of the phases. One phase has to change in the positive direction, while the other phase changes in the negative direction. All the possible combinations are:

$$\begin{aligned}\text{change in states} &\rightarrow \text{resulting state}\\ (1,-1,0) &\rightarrow (3,-1,-2)\\ (1,0,-1) &\rightarrow (3,0,-3)\\ (0,1,-1) &\rightarrow (2,1,-3)\\ (0,-1,1) &\rightarrow (2,-1,-1)\\ (-1,1,0) &\rightarrow (1,1,-2)\\ (-1,0,1) &\rightarrow (1,0,-1)\end{aligned}$$

A movement from a zero common-mode node to another will cause a two-level step in the line-to-line voltage between the phases, the voltages of which are changed. Other two line-to-line voltages will see only a one-level step. Continuing the example, the movement from the node (2,0,-2) to (3,-1,-2) is made by causing a change of (1,-1,0) to the states, which means that in the phase U the change is positive, while in the phase V the change is negative. The

phase W remains unchanged. The line-to-line voltages see the change as

$$u_{\mathrm{UV}} = u_{\mathrm{U}} - u_{\mathrm{V}} = 1 - (-1) = 2 \tag{3.1}$$

$$u_{\mathrm{VW}} = u_{\mathrm{V}} - u_{\mathrm{W}} = -1 - 0 = -1 \tag{3.2}$$

$$u_{\mathrm{WU}} = u_{\mathrm{W}} - u_{\mathrm{U}} = 0 - 1 = -1. \tag{3.3}$$

The oscillation in the phase voltages causes the line-to-line voltages to oscillate, and the oscillations accumulate similarly as in the phase voltage. If the line-to-line voltage sees a change of two levels, the peak value for the oscillation will also be doubled compared with the one-level step. This can be seen in Figure 3.4(a). As can be seen, two of the line-to-line voltages suffer from an oscillation caused by a one-level change, while one of them suffers from an oscillation of a two-level change. As stated earlier, the common-mode voltage remains zero.

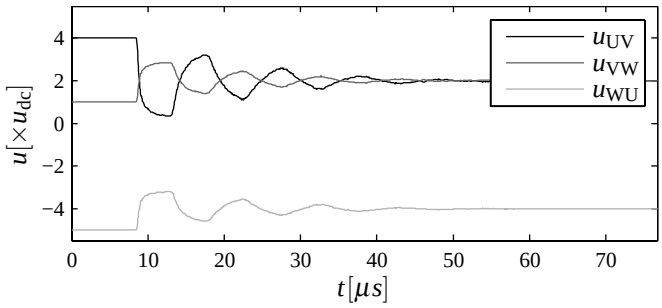
The principle of the edge modulation can be also applied to the line-to-line voltages to mitigate the two-level step oscillations. The mitigation requires that the line-to-line voltage resembles the edge-modulated voltage, that is, a two-level change is produced with two one-level changes with a time interval $\Delta t_{\mathrm{sw}}^{\mathrm{opt}}$ between them. This can be attained by delaying the change in one of the two changing phases by the time $\Delta t_{\mathrm{sw}}^{\mathrm{opt}}$. The resulting line-to-line voltages are shown in Figure 3.4(b). As a trade-off, the totally zero common-mode voltage is lost. The common-mode voltage will then reach the peak amplitude of one-third of the amplitude of oscillation of one edge.

3.5 Simulations and results

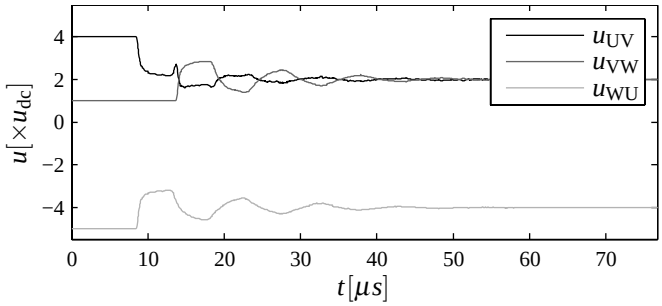
3.5.1 Simulation model with oscillations

To investigate the overvoltages induced in the motor terminals by different modulation schemes, a simulation model was constructed. The model imitates the motor terminal phase voltage by adding a measured oscillation after each voltage edge induced by the inverter. Such a measured terminal voltage is illustrated in Figure 1.7 in Section 1.4.2. The oscillation at the motor terminals is extracted from the measured data for both the rising and falling edges independently. The inverter itself is simplified to a programmable voltage source, which outputs a pulse pattern that represents the voltage pattern of an actual inverter. The DC link voltages were assumed to be nominal and constant throughout the simulation range. The concept of the simulation method described above is illustrated in Figure 3.5.

The modulation methods chosen for comparison were the DCM, the DCM with edge modulation, and the zero common-mode voltage modulation described in the previous section. To facilitate the comparison, the voltage vector was chosen to have an amplitude of $4.2\hat{u}_{\mathrm{dc}}$ and a frequency of 50 Hz. The sampling frequency for the reference was 2 kHz. The oscillation added to every step change in the inverter output voltage was measured with an approximately 300 m PVC-insulated cable with an open end. The sampling rate for the oscillation



(a) Phases changed simultaneously



(b) Phases changed with an interval of Δt_{sw}^{opt}

Figure 3.4. Line-to-line voltages at the motor terminals when the inverter changes its state from one zero common-mode node to another.

was 20 MHz. The measured propagation delay was 2.28 µs while the optimal time interval between the voltage edges was found with the method discussed in Section 3.2 to be $\Delta t_{sw}^{opt} = 2.28\, t_d$.

The phase voltages shown in Figure 3.6 were simulated in the above-described manner. The line-to-line and motor terminal common-mode voltages were calculated afterwards from the simulated data. The THD calculated with 50 harmonics is given in the caption of each figure.

The phase voltages express the voltage stress over the phase winding in the motor, if the stator is Y connected and there is a connection from the inverter common coupling point (N_{inv}) to the motor common coupling point (N_{mot}). Then, the phase voltage propagates in the insulation material between the phase lead and the neutral lead. The voltage after a step change will distribute unevenly in the windings, and the first few turns are subjected to most of the voltage stress.

The phase voltage of the DCM and the zero common-mode modulation includes the oscillation of one-level steps after each edge. The reflection attenuates in time, but it still causes multiple high du/dt voltage edges by the reflection to the winding. Each of these ringing edges causes a voltage difference over the first few turns of the winding with an amplitude of up to 75% of the amplitude of the edges (Fenger et al., 2002).

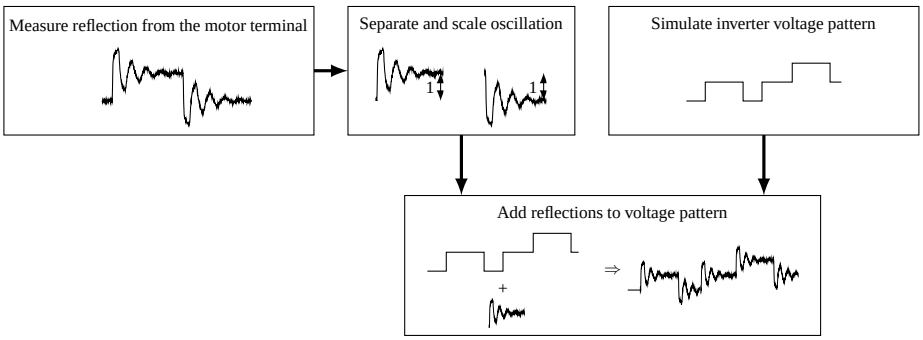


Figure 3.5. Formation of the simulation model. 1. The oscillation is measured and scaled. 2. The modulated voltage pattern is calculated. 3. The measured oscillation is added to every edge, in which case the result simulates the motor terminal phase voltages.

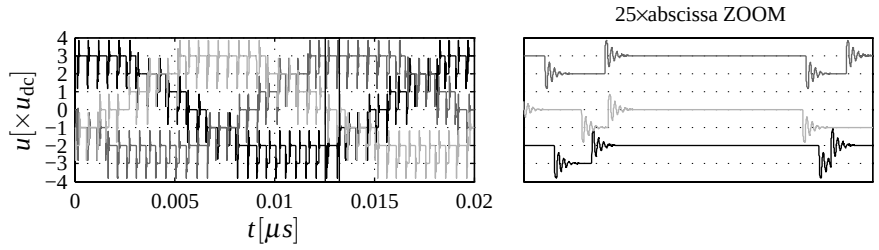
In the edge modulation, as a result of each change in the phase voltage, the motor winding sees a voltage edge, the $\mathrm{d}u/\mathrm{d}t$ of which is as high as it was in the earlier case. The difference lies in the oscillation: While the DCM and the zero common-mode modulation caused several consecutive voltage edges (although with an attenuating amplitude and $\mathrm{d}u/\mathrm{d}t$), the edge modulation causes an oscillation with a considerably attenuated amplitude. Therefore, the voltage stress over the first turns in the winding is not as severe as it is with the modulation methods using one voltage level steps.

The fact that the edge modulation uses only the active levels for voltage production results in a more distorted phase voltage than the methods that use all available voltage levels. This can be noticed by comparing the phase voltage THDs given in the labels of Figure 3.6. The THD of the phase voltage modulated with the DCM with edge modulation is approximately two times the THD of the DCM. The THD of the zero common-mode modulation is in the same range as is the THD of the DCM.

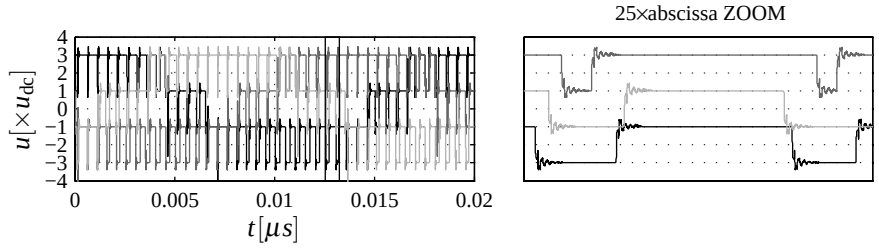
3.5.2 Line-to-line voltage

Motor terminal line-to-line voltages oscillate with the DCM (Figure 3.7(a)) similarly as the phase voltages did. The difference between the phase-to-neutral and line-to-line voltages is the accumulation of oscillations. The voltage edges in different phases can be switched at short intervals. The oscillation caused by the edge in one phase has not attenuated before the other phase launches a new edge, resulting in doubling the peak of the oscillation in the line-to-line voltage. This is clearly visible on the right-hand side of the enlarged part of Figure 3.7(a) in the waveform u_{WU}.

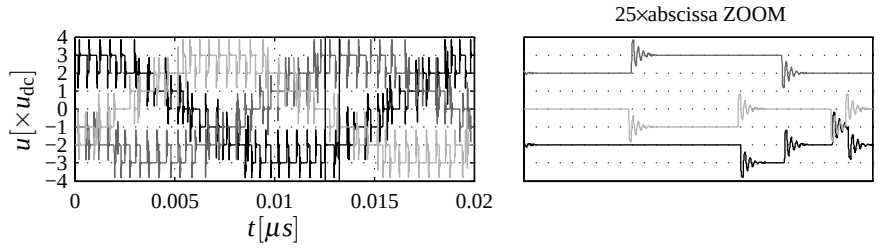
The DCM with the edge modulation, on the other hand, suppresses the amplitude of the oscillation after each voltage edge in the line-to-line voltage, even though a high amplitude oscillation is at present in u_{UV} and u_{VW} in the enlarged region of Figure 3.7(b). This kind of a failure is caused by the modulation algorithm at the instants when two of the phases



(a) DCM, THD= 17.56%



(b) DCM with edge modulation, THD= 37.04%

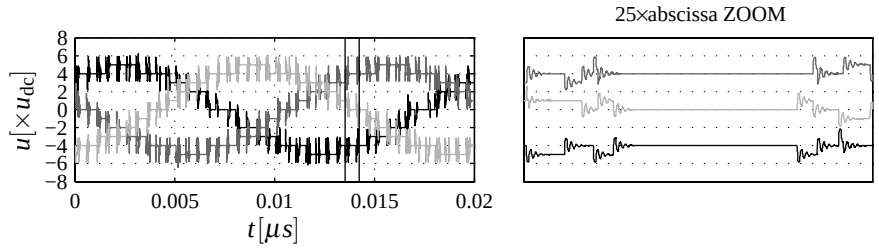


(c) Zero common-mode modulation with oscillation mitigation, THD= 14.83%

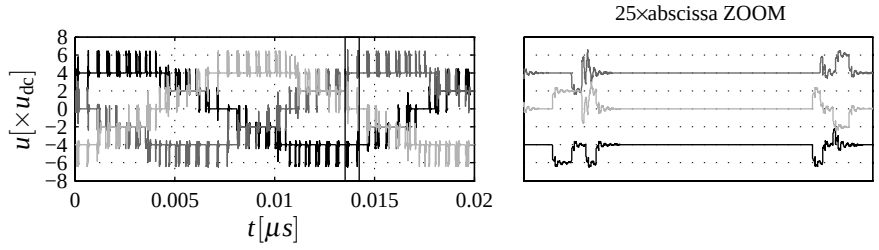
Figure 3.6. Simulated phase voltages at the motor terminals. The enlarged region is indicated by a rectangle on the left axis.

change their state simultaneously in the opposite direction. This can happen for example right at the beginning of the switching period. Kerkman et al. (1997) called this phenomenon *polarity reversal* for two-level inverters and claimed that this kind of a voltage substantially accelerates the deterioration of the insulation.

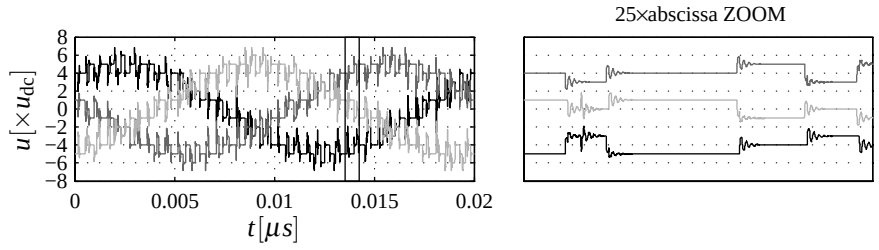
The total harmonic distortion of the line-to-line voltage for the DCM with and without edge modulation is clearly lower than the THD of the phase voltage. This is explained by the fact that the line-to-line voltage includes more voltage levels than the phase voltage, which reduces the effect of switching-originated harmonics on the THD. Even so, the total harmonic distortion of the edge-modulated voltage is almost twice the THD of the normally modulated voltage. With the zero common-mode voltage modulation, there is no significant difference between the THD of the line-to-line and phase voltage.



(a) DCM, THD= 8.36%



(b) DCM with edge modulation, THD= 13.52%



(c) Zero common-mode modulation with oscillation mitigation, THD= 14.93%

Figure 3.7. Simulated line-to-line voltages at the motor terminals. The enlarged region is indicated by a rectangle on the left axis.

3.5.3 Common-mode voltage

The common-mode voltage at the motor terminals is shown in Figure 3.8 for all the three modulation methods under investigation.

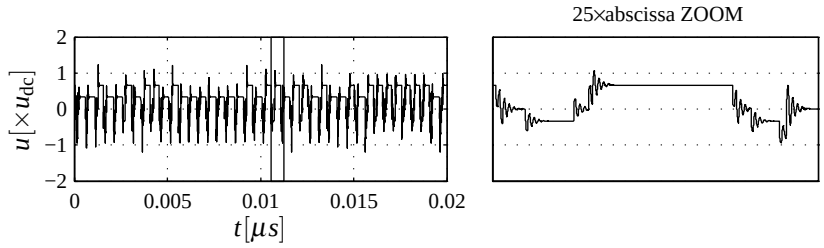
As stated above, the common-mode voltage is the average value of the phase voltages. When the changes in the phase voltages are distributed across the switching period so that no simultaneous switchings occur between the phases, the maximum change in the common-mode voltage should then be one-third of the change. If the changes are restricted to one-level steps, and their oscillation will reach 1.8 times the step, the maximum change in the common-mode voltage should be 0.6 times the step amplitude.

In the DCM-modulated common-mode voltage, the oscillations remain mainly at the level of

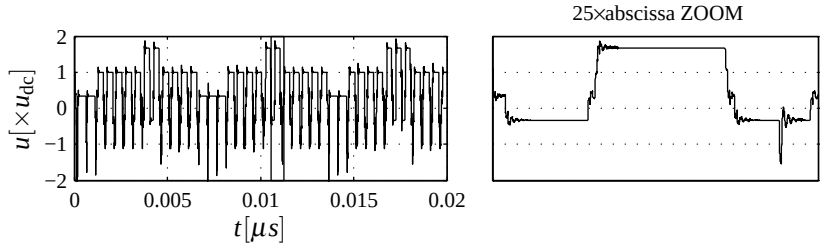
one step, but because the changes in the phases are occasionally too close to each other, the oscillations accumulate as explained in the line-to-line voltage analysis.

When the edge modulation is applied to the DCM, the oscillations in the common-mode voltage are suppressed as in the phase or line-to-line voltage, but the voltage level to which the stray capacitances are charged is occasionally double that of the DCM. The risk and amplitude of the bearing currents increase.

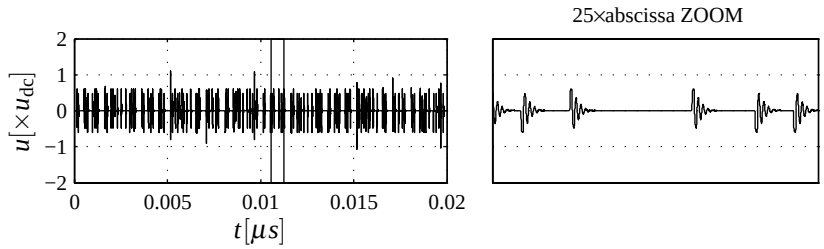
In contrast to the DCM, the zero common-mode modulation keeps the DC component of the common-mode voltage zero regardless of the switching state. Only the transitions from one node to another cause a change in the common-mode voltage, because the changes in the phases are made with intervals of Δt_{sw}. Even though the common-mode voltage oscillates after each change, the peak of the oscillation remains at the minimum level.



(a) DCM



(b) DCM with edge modulation



(c) Zero common-mode modulation with oscillation mitigation

Figure 3.8. Common-mode voltages calculated from the simulated motor terminal phase voltages. The enlarged region is indicated by a rectangle on the left axis.

3.6 Discussion

The effectiveness of the edge modulation is highly dependent on the selection of the right value for $\Delta t_{\mathrm{sw}}^{\mathrm{opt}}$. The method to find the optimal interval between the edges described in Section 3.2 is quite a straightforward task to complete with a personal computer, but implementing the algorithm in the embedded control system of the inverter could be challenging because of the large amount of data to be analyzed. Another drawback of the method is that it requires a high-frequency bandwidth measurement of the voltage at the motor terminals. The measurement may be difficult to arrange in an industrial environment where the inverter and the load are far apart.

Even though there are difficulties in the measurement of the motor terminal voltage, the measurement has to be executed only once for the drive if the cable is kept the same. Therefore, the waveform of the oscillation could be achieved for example at the initial start-up of the drive. The interval $\Delta t_{\mathrm{sw}}^{\mathrm{opt}}$ is obtained off-line and the parameter determining the interval in the drive is then adjusted to match the optimal mitigation.

Another way to find the optimal interval would be to use the current waveform at the inverter end of the cable. As shown in (Tarkiainen et al., 2002), instead of the voltage, the current oscillates at the inverter end of the cable. The current measurement is a default accessory in a modern-day inverter, and therefore, it would be natural to use it also for edge modulation purposes. One obvious problem would be the bandwidth requirement for the measurement, because the frequency of the oscillation is in the range from tens of kilohertz to a few megahertz depending on the cable.

The results presented in this chapter show that the modulation-based mitigation of oscillating overvoltages caused by the reflection phenomenon is always a trade-off between the mitigation and the common-mode voltage or the modulation accuracy.

The modulation accuracy is now lower because the number of active voltage levels is reduced, but this is not as adverse a trade-off as is the oscillation versus the common-mode voltage. If the oscillations in the phase or line-to-line voltages are mitigated, the common-mode voltage is increased, and vice versa. This holds even for the zero common-mode modulation, where the totally zero common-mode voltage can be reached, but the oscillations in the line-to-line voltage will then accumulate. If this high-amplitude oscillation in the line-to-line voltage is mitigated by delaying the change in one of the phases, the common-mode voltage will show an oscillation.

The switching frequency per switch will also increase with the edge modulation if the sampling frequency of the reference is kept constant when comparing the modulation with and without edge modulation. The edge modulation forms the voltage with four voltage edges, whereas the normal modulation uses only two edges per switching period per phase.

If the oscillation was considered only from the overvoltage point of view, it would be insignificant at least for higher-voltage-level drives. The overvoltage that the motor has to endure depends on the number of levels. For two-level inverters, the oscillation causes a relatively

high stress to the motor, since the peak voltage almost doubles. With multilevel inverters, the voltage steps are relatively small compared with the steps of two-level inverters. Therefore, the amplitude of the oscillations are also relatively small. For seven-level inverters, the oscillation of one-level step with an amplitude of u_{dc} will cause an overvoltage of less than one sixth of the peak-to-peak phase-voltage, which is considered as the nominal voltage that the insulation endures. Therefore, the use of edge modulation is recommended for three- to five-level inverters, where the benefits can be justified. For higher-level inverters instead, the use of edge modulation is questionable.

Chapter 4

Conclusions

Multilevel modulation methods suitable especially for a series-connected H-bridge inverter were discussed. Voltage waveforms, common-mode voltages, and dynamic capabilities were analyzed. The emphasis was on sampled reference modulation methods such as space vector modulation and duty cycle modulation. Carrier-based modulation methods were discussed in brief, and some simulation results were given for comparative reasons. Operation of the investigated modulation methods in the overmodulation region was left out from the analysis. The subject is important for the total utilization of the inverters, and therefore, it should be considered as a topic of future studies.

The duty cycle modulation (DCM) method and the modified duty cycle method (MDCM) were discussed in detail. The MDCM forms the vectors with an emphasis on the phase voltages, while the DCM with an emphasis on the vector location. The emphasis on the phase voltages results in the use of four nodes on the voltage hexagon lattice, whereas the other approach uses only three nodes. The space vector PWM methods also use the three nearest nodes. The use of three nodes is shown to have a positive effect on the line-to-line voltage and current waveforms. On the other hand, phase-to-neutral voltages produced by the MDCM had the lowest distortion compared with the DCM and the SVPWM.

A voltage formation method called module circulation for the phase circuit of the SCHBI was also introduced. The method aims at sharing the load evenly among the modules, when the voltage in the DC links remains in balance. It was shown that the method is effective, and most of all, implementable. Another benefit of the module circulation is that the switching frequency of the modules is lower than the apparent switching frequency if the number of modules is higher than one.

Regardless of the fact that the module DC link voltages remain well in balance with the use of module circulation, the DC link voltages vary considerably under load. It was discussed how the varying DC link voltages affect the vector and voltage production of the inverter. An algorithm that aims at compensating the varying DC link voltages was proposed. The

algorithm can be implemented as an extension to upper-level modulation schemes such as the MDCM, the DCM, or the SVPWM. The compensation scheme was shown to be effective considering voltage vector accuracy. With the DCM and the SVPWM, the compensation algorithm also improved the voltage and current quality with a sufficient switching frequency. For lower switching frequencies, the compensation improves the modulation accuracy only slightly.

An appropriate way to modulate with multilevel inverters is to allow only one voltage level steps in the phase voltages. This sets some limits on the voltage vector production, but it was found that regardless of the limitations on the modulation, the multilevel modulation schemes can operate even in dynamically challenging applications.

The above-mentioned restriction on the voltage pattern is justified by the oscillating overvoltages when a long feeder cable is used. The overvoltage at the motor terminals caused by the reflection phenomenon may deteriorate the winding insulation. Overvoltages of this kind can be reduced by extra filters in the output of the inverter. The filter lowers the $\mathrm{d}u/\mathrm{d}t$ of the voltage edges, and therefore mitigates the oscillation (Tarkiainen et al., 2002).

Another option for the oscillation mitigation was proposed in this thesis. The suggested method does not require extra filters, but the mitigation is achieved by exploiting two correctly timed consecutive voltage edges and their oscillations. The method can be implemented as an extension to an upper-level modulation scheme such as the SVPWM or the DCM. The drawbacks of the method include the reduction of the voltage levels and the increased amplitude of the common-mode voltage. Even though the proposed scheme successfully mitigates the oscillation, the $\mathrm{d}u/\mathrm{d}t$ of the edges that encounter the motor windings is not reduced.

The implementation of the oscillation mitigation method requires knowledge of the motor terminal voltage to determine the proper timing of the edges. Even though the measurement has to be made only once, it would be difficult to carry out. Therefore, it is proposed that an option to determine the proper time interval by some other means should be considered as a subject for future work. One opportunity would be that the current waveform at the inverter end of the cable is exploited somehow. Instead of the voltage, the current will oscillate at the inverter terminals.

The common-mode voltage caused by the multilevel inverters through modulation was analyzed. It was shown that the common-mode voltage may include several steps and even oscillate at the pace of the phase voltages. Even though the effects of a common-mode voltage on two-level electrical drives have been in the focus of research for several years now, multilevel-modulation-originated common-mode voltages have not received as much attention. It would be an interesting and useful research topic to analyze how the amplitude-varying common-mode voltage affects the bearing currents.

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Appendix A

Derivation of switching instant calculation for compensation of DC link voltage fluctuation

A.1 Switching instant calculation for symmetric voltage formation

In contrast to publications **II** and **III**, where the duty cycle d_{ph} was a result of the compensation algorithm, this appendix aims at calculating the switching instants $t_{1\text{st}}$ and $t_{2\text{nd}}$. This should ease the comparison of the algorithms for different voltage formation methods.

The voltage is formed during a switching period according to the pulse pattern decided by the modulation algorithm. The pulse pattern can be described with a switching matrix $\mathbf{sw}^{Q}_{ph}$, where the columns represent modules and the rows represent times. The first row of the matrix represents the module states during the time interval $[0, t_{1\text{st}}]$. The second row describes the states between $t_{1\text{st}}$ and $t_{2\text{nd}}$, and the third row from $t_{2\text{nd}}$ to T_{sw}. The module states can be either -1, 0, or 1. The formulation of the matrix is

$$\mathbf{sw}^{Q}_{ph} = \begin{bmatrix} sw_1^{t_{\text{on},1}} & sw_2^{t_{\text{on},1}} & \dots & sw_M^{t_{\text{on},1}} \\ sw_1^{t_{\text{on},2}} & sw_2^{t_{\text{on},2}} & \dots & sw_M^{t_{\text{on},2}} \\ sw_1^{t_{\text{on},3}} & sw_2^{t_{\text{on},3}} & \dots & sw_M^{t_{\text{on},3}} \end{bmatrix} \tag{A.1}$$

If the matrix is multiplied by a vector that includes all the DC link voltages, we get the actual voltage levels during T_{sw}. It is convenient to scale the DC link voltages with the nominal

value $\hat{u}_{\mathrm{dc}}$. The value of $\hat{u}_{\mathrm{dc}}$ can be arbitrarily selected, but it is recommended to select it low enough so that regardless of the load, overmodulation can be avoided at all times. The voltage-level matrix is calculated by

$$\mathbf{u}_{\mathrm{sw}} = \begin{bmatrix} u_{t_{\mathrm{on},1}} \\ u_{t_{\mathrm{on},2}} \\ u_{t_{\mathrm{on},3}} \end{bmatrix} = \begin{bmatrix} sw_1^{t_{\mathrm{on},1}} & sw_2^{t_{\mathrm{on},1}} & \dots & sw_M^{t_{\mathrm{on},1}} \\ sw_1^{t_{\mathrm{on},2}} & sw_2^{t_{\mathrm{on},2}} & \dots & sw_M^{t_{\mathrm{on},2}} \\ sw_1^{t_{\mathrm{on},3}} & sw_2^{t_{\mathrm{on},3}} & \dots & sw_M^{t_{\mathrm{on},3}} \end{bmatrix} \begin{bmatrix} u_{\mathrm{dc},1} \\ u_{\mathrm{dc},2} \\ \dots \\ u_{\mathrm{dc},M} \end{bmatrix} \tag{A.2}$$

The basis of the compensation is to carry out switchings so that the resulting time-averaged voltage will correspond to the time integral of the phase reference u^*_{ph}. That is,

$$\int_0^{T_{\mathrm{sw}}} u \mathrm{d}t = \int_0^{T_{\mathrm{sw}}} u^*_{ph} \mathrm{d}t. \tag{A.3}$$

where u is the output voltage of the inverter. Since the output voltage is now defined in (A.2) as discrete voltages assuming $\mathrm{d}u/\mathrm{d}t$ to be infinite, and u^*_{ph} is constant, Equation (A.3) can be written as

$$\begin{bmatrix} t_{\mathrm{on},1} & t_{\mathrm{on},2} & t_{\mathrm{on},3} \end{bmatrix} \begin{bmatrix} u_{t_{\mathrm{on},1}} \\ u_{t_{\mathrm{on},2}} \\ u_{t_{\mathrm{on},3}} \end{bmatrix} = u^*_{ph} T_{\mathrm{sw}} \tag{A.4}$$

where $t_{\mathrm{on},1}$, $t_{\mathrm{on},2}$, and $t_{\mathrm{on},3}$ are on-times for the voltage levels $u_{t_{\mathrm{on},1}}$, $u_{t_{\mathrm{on},2}}$, and $u_{t_{\mathrm{on},3}}$, respectively. In publications **II** and **III** the compensation is derived so that $t_{\mathrm{on},2}$ is solved from Equation (A.4). This can be considered the duty cycle or the time instant between the switchings $t_{1\mathrm{st}}$ and $t_{2\mathrm{nd}}$. Now the equation is rewritten so that the switching instants are solved.

First, the relation between on-times and switching instants has to be determined. The voltage is formed symmetrically at the center of the switching period. Therefore

$$t_{\mathrm{on},1} = t_{\mathrm{on},3} \tag{A.5}$$

is valid. On the other hand, $t_{\mathrm{on},1}$ describes the time interval between 0 and $t_{1\mathrm{st}}$. Thus, after $t_{\mathrm{on},1}$ the time $t_{1\mathrm{st}}$ is achieved, and we can say that $t_{\mathrm{on},1} = t_{1\mathrm{st}}$. Considering the switching period from the end to the beginning, we see that

$$t_{2\mathrm{nd}} = T_{\mathrm{sw}} - t_{\mathrm{on},3}. \tag{A.6}$$

From symmetry, it follows that $t_{\mathrm{on},3} = t_{1\mathrm{st}}$. $t_{\mathrm{on},2}$ is the time interval between $t_{1\mathrm{st}}$ and $t_{2\mathrm{nd}}$ and it can be calculated as $t_{\mathrm{on},2} = t_{2\mathrm{nd}} - t_{1\mathrm{st}}$. Now we can write Equation (A.4) in the form

$$\begin{bmatrix} t_{1\mathrm{st}} & T_{\mathrm{sw}} - 2t_{1\mathrm{st}} & t_{1\mathrm{st}} \end{bmatrix} \begin{bmatrix} u_{t_{\mathrm{on},1}} \\ u_{t_{\mathrm{on},2}} \\ u_{t_{\mathrm{on},3}} \end{bmatrix} = u^*_{ph} T_{\mathrm{sw}} \tag{A.7}$$

from which $t_{1\mathrm{st}}$ is solved to be

$$t_{1\mathrm{st}} = \frac{(u^*_{ph} - u_{t_{\mathrm{on},2}}) T_{\mathrm{sw}}}{u_{t_{\mathrm{on},1}} - 2u_{t_{\mathrm{on},2}} + u_{t_{\mathrm{on},3}}}. \tag{A.8}$$

The equation is valid if $u_{t_{\mathrm{on},1}} - 2u_{t_{\mathrm{on},2}} + u_{t_{\mathrm{on},3}} \neq 0$. Otherwise, no switching occurs during the switching period, and the voltage level is chosen to be the closest one to the reference.

A.2 Switching instant calculation for asymmetric voltage formation

As Figure 2.23(b) shows, the asymmetric voltage formation switches only once per switching period. Therefore, $\mathbf{sw}_{ph}^{Q}$ has to be reformulated, and it will have only two rows. The first row presents the module states from the beginning of the switching period to $t_{1\mathrm{st}}$ and the second row from $t_{1\mathrm{st}}$ to the end of the switching period. These time intervals are denoted $t_{\mathrm{on},1}$ and $t_{\mathrm{on},2}$, respectively. The matrix will now have the form

$$\mathbf{sw}_{ph}^{Q} = \begin{bmatrix} sw_1^{t_{\mathrm{on},1}} & sw_2^{t_{\mathrm{on},1}} & \dots & sw_M^{t_{\mathrm{on},1}} \\ sw_1^{t_{\mathrm{on},2}} & sw_2^{t_{\mathrm{on},2}} & \dots & sw_M^{t_{\mathrm{on},2}} \end{bmatrix} \tag{A.9}$$

Calculation of the actual voltage levels is similar to the symmetric voltage formation: $\mathbf{sw}_{ph}^{Q}$ is multiplied by u_{dc}. This results in a 2×1 matrix

$$\mathbf{u}_{\mathrm{sw}} = \begin{bmatrix} u_{t_{\mathrm{on},1}} \\ u_{t_{\mathrm{on},2}} \end{bmatrix}. \tag{A.10}$$

The switching instant $t_{1\mathrm{st}}$ must be selected so that the voltage average u_{ph}^{*} is met. u_{ph}^{*} is met with

$$\begin{bmatrix} t_{\mathrm{on},1} & t_{\mathrm{on},2} \end{bmatrix} \begin{bmatrix} u_{t_{\mathrm{on},1}} \\ u_{t_{\mathrm{on},2}} \end{bmatrix} = u_{ph}^{*} T_{\mathrm{sw}} \tag{A.11}$$

From the voltage pattern presented in Figure 2.23(b), we see that $t_{\mathrm{on},1}$ actually equals the $t_{1\mathrm{st}}$. The relation between $t_{\mathrm{on},2}$ and $t_{1\mathrm{st}}$ is

$$t_{\mathrm{on},2} = T_{\mathrm{sw}} - t_{\mathrm{on},1} = T_{\mathrm{sw}} - t_{1\mathrm{st}}. \tag{A.12}$$

Substituting $t_{\mathrm{on},1} = t_{1\mathrm{st}}$ and (A.12) to (A.11) we get

$$\begin{bmatrix} t_{1\mathrm{st}} & T_{\mathrm{sw}} - t_{1\mathrm{st}} \end{bmatrix} \begin{bmatrix} u_{t_{\mathrm{on},1}} \\ u_{t_{\mathrm{on},2}} \end{bmatrix} = u_{ph}^{*} T_{\mathrm{sw}} \tag{A.13}$$

or

$$t_{1\mathrm{st}}(u_{t_{\mathrm{on},1}} - u_{t_{\mathrm{on},2}}) + T_{\mathrm{sw}} u_{t_{\mathrm{on},2}} = u_{ph}^{*} T_{\mathrm{sw}} \tag{A.14}$$

from which $t_{1\mathrm{st}}$ can be solved:

$$t_{1\mathrm{st}} = \frac{(u_{ph}^{*} - u_{t_{\mathrm{on},2}}) T_{\mathrm{sw}}}{u_{t_{\mathrm{on},1}} - u_{t_{\mathrm{on},2}}} \tag{A.15}$$

which is valid when $u_{t_{\mathrm{on},1}} \neq u_{t_{\mathrm{on},2}}$; otherwise no switching occurs at all, but the inverter holds its state during the whole switching period. Equation (A.15) will result in a correct voltage average regardless of whether $u_{t_{\mathrm{on},1}} < u_{t_{\mathrm{on},2}}$ or $u_{t_{\mathrm{on},1}} > u_{t_{\mathrm{on},2}}$.

A.3 Switching instant calculation for multiple-edge voltage formation

The edge modulation explained in Chapter 3 uses four switchings during a switching period. This will complicate the DC link voltage fluctuation compensation even further. Now the switching state matrix will be of the size of $5 \times M$ including the module states for the time intervals $t_{\text{on},1} ... t_{\text{on},5}$.

The volt-second-average equation for the edge-modulation will become

$$\begin{bmatrix} t_{\text{on},1} & t_{\text{on},2} & t_{\text{on},3} & t_{\text{on},4} & t_{\text{on},5} \end{bmatrix} \begin{bmatrix} u_{t_{\text{on},1}} \\ u_{t_{\text{on},2}} \\ u_{t_{\text{on},3}} \\ u_{t_{\text{on},4}} \\ u_{t_{\text{on},5}} \end{bmatrix} = u_{ph}^{*} T_{\text{sw}}. \tag{A.16}$$

where the on-times for the switching states correlate with the switching instants according to the following two assumptions. The first assumption is that the switchings are aligned symmetrically inside the switching period. The second assumption is that the intervals $t_{\text{on},2}$ and $t_{\text{on},4}$ are known and equal. A notation Δt_{sw} is introduced to denote the interval. A method to select the time interval Δt_{sw} is suggested in Chapter 3. From these assumptions it follows that

$$t_{\text{on},1} = t_{\text{on},5} = t_{1\text{st}} \tag{A.17}$$

$$t_{\text{on},2} = t_{\text{on},4} = \Delta t_{\text{sw}} \tag{A.18}$$

$$t_{\text{on},3} = t_{3\text{rd}} - t_{2\text{nd}} \tag{A.19}$$

which leads to

$$t_{2\text{nd}} = t_{1\text{st}} + \Delta t_{\text{sw}}, \tag{A.20}$$

$$t_{3\text{rd}} = t_{4\text{th}} - \Delta t_{\text{sw}}, \tag{A.21}$$

$$t_{4\text{th}} = T_{\text{sw}} - t_{1\text{st}}. \tag{A.22}$$

Substitution of Equations (A.17)–(A.22) to (A.16) results in

$$\begin{bmatrix} t_{1\text{st}} \\ \Delta t_{\text{sw}} \\ T_{\text{sw}} - 2(t_{1\text{st}} + \Delta t_{\text{sw}}) \\ \Delta t_{\text{sw}} \\ t_{1\text{st}} \end{bmatrix}^{\text{T}} \begin{bmatrix} u_{t_{\text{on},1}} \\ u_{t_{\text{on},2}} \\ u_{t_{\text{on},3}} \\ u_{t_{\text{on},4}} \\ u_{t_{\text{on},5}} \end{bmatrix} = u_{ph}^{*} T_{\text{sw}}. \tag{A.23}$$

from which the first switching instant is solved to be

$$t_{1\text{st}} = \frac{(u_{ph}^{*} - u_{t_{\text{on},3}}) T_{\text{sw}} - (u_{t_{\text{on},2}} + u_{t_{\text{on},4}} - 2u_{t_{\text{on},3}}) \Delta t_{\text{sw}}}{u_{t_{\text{on},1}} + u_{t_{\text{on},5}} - 2u_{t_{\text{on},3}}} \tag{A.24}$$

and the rest of the switching instants can be obtained by Equations (A.20)–(A.22).