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Master's Degree Programme in Energy Technology

Comparison and evaluation of eddy current sensors

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ABSTRACT

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In the work eddy current sensors are described and evaluated. Theoretical part includes physical basics of the eddy currents, overview of available commercial products and technologies. Industrial sensors operation was assessed based on several working modes. Apart from this, the model was created in Matlab Simulink with Xilinx Blockset and then translated into a Xilinx ISE Design Suite compatible project. The performance of the resulting implementation was compared to the existing implementation in the Xilinx Spartan 3 FPGA board with the custom made sensor. Additionally, an introduction to FPGAs and VHDL is presented.

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Lappeenranta

List of abbreviations and symbols

AC – Alternating current;

AD/DA – Analog-Digital/Digital-Analog;

Ag – Argentum;

AMB – Active magnetic bearings;

Au – Aurum;

CLB – configurable logic block;

COW – Conventional copper wire;

DCM – Digital clock manager;

EMC – Electromagnetic compatibility;

Fe – Ferrum;

FFT – Fast Fourier Transform;

FIR – Finite impulse response;

FPGA – Field programmable gate array;

FTBGA – Fine-Pitch Thin Ball Grid Array;

HTCC – High temperature cofired ceramics;

IIR – Infinite impulse response;

IOB – input/output block;

JTAG – Joint Test Action Group;

LTCC – Low temperature cofired ceramics;

LTI – Linear time-invariant;

MPW – Magnetoplated wire;

Ni – Nickel;

PAL – Programmable Array Logic;

PLA – Programmable Logic Array;

PLD – Programmable logic device;

PROM – Programmable read-only memory;

RTL – Register transfer level;

Si – Silicium;

SRAM – Static random access memory;

TTL – Transistor-transistor logic;

VDC – Voltage direct current;

VHDL – Very high speed integrated circuit hardware description language;

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1 INTRODUCTION

1.1 Theoretical background

Eddy-current sensors proved their reliability, robustness, sensitivity and precision along with simplicity and low cost in different industrial applications. This type of sensors belongs to inductive sensors, whose working principle is based on the Faraday's Induction Law. Applications of the eddy-current sensors can be found in turbines, electrical machines, aircrafts, nuclear industry, automated assembly lines and bearings. The applications related to bearings include:

- radial motion;
- differential expansion;
- quantity and quality;
- rotation monitoring;
- speed/phase;
- position and proximity;
- vibration;
- alignment;

Eddy-current sensors have several advantages. The fact that they use magnetic fields for sensing gives the opportunity to conduct measurements with contaminated air gap without affecting sensor's output. It makes the eddy-current sensors the best choice for hostile environment. One of the leading manufacturers – "Lion Precision" – produces sensors, which can even be used when immersed in non-corrosive liquid [1].

Other feature is that they can be operated under high temperatures (even up to +600 °C [2]), in a large range and in vacuum (nevertheless, special cleaning procedures of a target should be provided in order to maintain vacuum environment) [1]. Solution for the high temperature measurements was found using low temperature co-fired ceramics (LTCC). LTCC are multiple layer tapes, which contain glass and ceramics composites, and have several advantages, such as temperature stability, low thermal coefficient of expansion, corrosion resistance. Another method for improving

thermal properties is insulation of a sensor from heat sources [2, 3]. Manufacturers also try to improve characteristics (peak-to-peak value of the output signal, for instance) of coils by adding layers from different compounds (e.g. NiFe) on their surface [4]. High temperature stability of eddy current sensors explains their wide use in electrical machines applications.

There are still several problems of industrial applicability of the eddy current sensors. The leading manufacturers include Micro-Epsilon, Lion Precision, SKF and others. Available solutions of the material dependence in measurements using eddy current sensors are described in the work. In addition, such problems as temperature stability and temperature compensation and increasing of the linear range are considered. Nowadays several efforts are taken in order to compensate material and temperature influences by developing improved signal processing, self-calibration and special sensor design [5].

Advanced technologies are also observed. One of the attractive methods in precise surface inspection is the use of arrayed eddy-current sensors. Zetec Company offers special ECT (Eddy-current testing) array inspection systems, which consists of several sensors assembled and grouped together. It gives the opportunity for faster, more reliable and simpler inspections of the complex surfaces.

One of the most important applications of the eddy current sensors is in active magnetic bearings (AMB). AMB applications require significantly precise and reliable measurements in high temperature conditions. Solutions that meet those needs are presented in the work.

1.2 Main objectives

The major scope of the work is in investigation of possibility to build alternative, time and resource efficient solution for configuration of the FPGA circuit for custom-made eddy current sensors.

The existing custom sensor system is studied and then rebuilt as a Matlab Simulink model with help of the Xilinx Blockset and the System Generator. Xilinx tools for

Matlab Simulink give the opportunity to make models, which can be then transferred to Xilinx software (Xilinx ISE Design Suite or Xilinx ISE Webpack) and used for configuration of Xilinx FPGA chips even without considerable VHDL programming skills. Simulink modeling approach has distinctive advantages such as its visualization feature or possibility for easy model improvements with built-in blocksets. For instance, complete model can be added with signal processing algorithms effortlessly and without significant time consumption.

The custom made sensor, which is used in the work, communicates with PC and its tools via Xilinx Spartan 3 FPGA board. FPGA technology has several significant advantages such as the possibility of reprogramming and the opportunity to implement different architectures for various purposes. At the same time Spartan 3 family boards have a reasonable price. Performance of the Spartan 3 FPGA board configuration generated from the Simulink model will be evaluated and compared to the existing Xilinx ISE project.

Apart from this, practical part of the work consists of measurements using available industrial sensors. The scope of these measurements is sensors evaluation, which includes the analysis of several system modifications (terminator attachment, different target samples and others). Noise measurements, dependences of an output signal from a distance for different cases and standard deviation values are presented.

2 POSITION MEASUREMENTS

2.1 Eddy current nature and principles

First who discovered eddy currents was the french scientist Arago. In 1824 he observed a rotating cooper disc attached to an axis with a magnet needle. Later this phenomenon was described by Faraday with his electromagnetic induction law. According to this law, a rotating magnetic field induces currents (eddy currents) in the copper disc, which interact with a magnet needle. Subsequently, eddy currents were named Foucalt currents in honor of Leon Faucalt, who researched and analyzed them in details.

Therefore, eddy currents are currents, which are induced in a conducting material, interacting with a primary altering magnetic field. Changing magnetic field creates an electromotive force (EMF) in a conductor due to the fact that magnetic flux changes. As a result, eddy currents start to flow in the conductor, generating a secondary magnetic field directed opposite to the main field [6]. The expression for the EMF is showed below:

$$E = -N \cdot \frac{\mathrm{d}\Phi}{\mathrm{d}t},$$

where

N – number of turns of coil winding;

Φ – magnetic flux, [Wb];

E – electromotive force, [V];

t – time, [s].

The principle of eddy current is shown in Fig. 1.

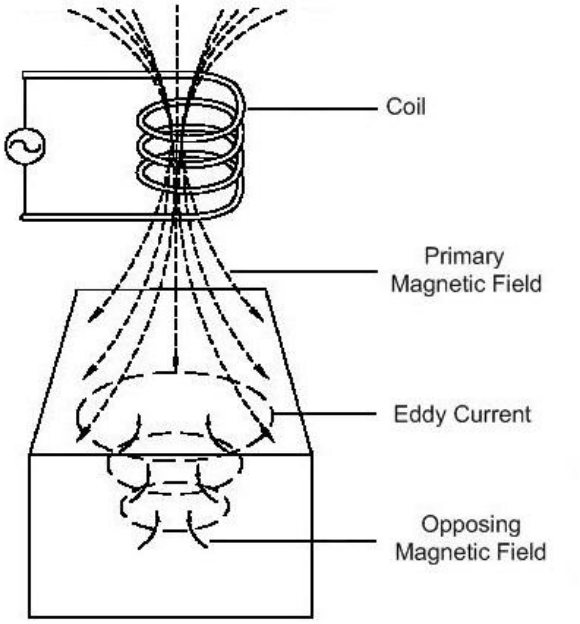

Fig.1. The eddy current principle [7].

In order to understand an effect of eddy currents and why they are named eddy, the analogy with water and an oar can be held: when an oar is moved along a boat, it causes eddies appearance in water.

Eddy currents can both affect a system performance in a negative way, and to be useful. As other currents, eddy currents cause heating when they flow. Due to thermal effect of eddy currents, they are used in inductive furnaces. Conducting material is placed in a coil supplied by the powerful high-frequency generator. Eddy currents are induced in the material rising its temperature until it starts to melt. Heating of metal parts of vacuum units is also provided by the eddy current's thermal effect.

An induction motor is another important example of the eddy current application, where an alternating magnetic field induces eddy currents in a rotor, causing its rotation [7]. When a conductor moves in a strong magnetic field, it brakes due to interaction between eddy currents and the field. This effect is used for damping of moving parts in such devices as galvanometers and others. One application which is described and used in the thesis is position sensing based on using eddy current sensors. Principles, methods and equipment will be described later.

Nevertheless, eddy currents have often a negative effect. They cause skin effect, when the density of the alternating current is bigger at the surface of a conductor decreasing to the depths. Heating of transformer core is another problem, which is avoided by using cores, assembled from thin plates, or utilizing ferrites as materials.

In conclusion, it can be said that the eddy currents are still not fully investigated and developed phenomenon, despite of a wide variety of applications based on their principles.

2.2 Industrial sensors and their manufacturers.

Position measurements have been conducted widely in different professional areas from automated assembly lines to nuclear industry. Consequently, in such various, often dangerous and harmful conditions equipment must meet all the requirements including accuracy, stability and safety. As reliable and proven tools, the eddy current sensors satisfy these expectations, and this fact is a good reason for their popularity. Along with position measurements, eddy current sensors are used for other purposes such as crack and air-gap detection, vibration monitoring, shaft orbit monitoring, angular speed and frequency measurements, and others [9]. It's important to mention that they also found their application in active magnetic bearings (AMB) systems.

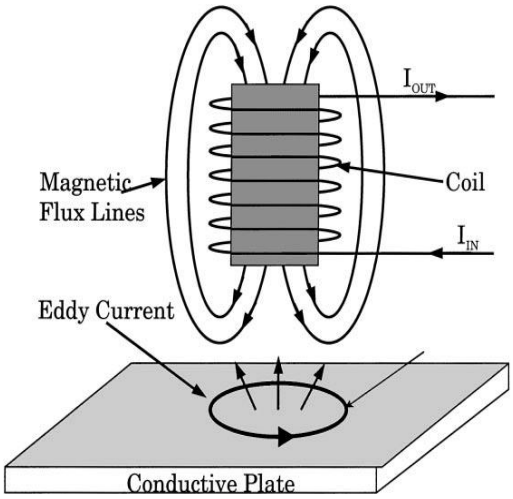

Fig.2. The eddy current effect on a conductive plate, placed inside a magnetic field of a coil [8].

As it was mentioned above, the considered sensor type belongs to inductive sensors, and the Faraday's Induction Law is the basis of their work. The main part of the sensor is a sensing coil. Alternating current flows through the coil generating an alternating magnetic field (Fig. 2.). When a conducting target is placed into the

magnetic field, the eddy current effect appears. A secondary magnetic field is produced as a result of the induced on the surface of the target eddy currents according to Len's law. The secondary magnetic field opposes to the primary magnetic field changing the impedance of the coil (increasing active resistance and decreasing inductive reactance) [2]. The change of impedance depends on a distance to the target, its permeability, conductivity, thickness.

The main eddy current sensors manufacturers are SKF, Micro-Epsilon, Lion Precision and others. Micro-Epsilon is a leading company with 40-years history from Germany. In the middle of 1980s they focused on industrial applications (for instance, nuclear industry) and exactly on displacement measurements [10]. In 1988 they developed the smallest eddy current sensor for that time U05. Then sensors with the significantly low noise ratio and expanded range were created. Nowadays the company has a lot of customers around the world and offers advanced solutions for measuring systems.

Lion Precision is another industry leader. Its history started in 1958 and to the present day the company continues generating innovative technologies in measurements. They developed the first fully digital eddy current sensor, which has temperature stability, improved linearity, and electromagnetic interference protection. Another solution provides direct reading of digital outputs to the LabVIEW system avoiding AD/DA conversions and, as the consequence, it has low noise levels [11].

SKF sensors are intensively used in rotating machinery, bearing systems and have excellent frequency response without lower frequency limit. They can be used in harsh conditions of chemical and oil industries because of the unique material of Eddy Probe tips – Ryton. Ryton is not affected by the devastating effects of acids, bases and solvents. The SKF CMSS 65 Eddy probe as a part of measuring system with dSpace control panel and Matlab software will be used in the work for its evaluation and analysis.

2.3 Known issues

Eddy current sensors have been developed and improved for many years due to their popularity. Nonetheless, several known issues still exist. They should be avoided or their influence must be minimized in order to increase performance of sensors. Among these problems are temperature stability, increasing of a linear range, material dependence and others. Consequently, world leading companies are working hard to develop advanced technologies or improved algorithms to make customers satisfied.

2.3.1 Temperature stability

One of the main problems with the operation of the eddy-current sensors is temperature compensation. All the measurements should be conducted in a stable environment, because any insignificant temperature change affects the output signal accuracy.

There are two traditional methods of temperature compensation. One of them is the differential method, when the output signal is evaluated between the measuring coil and the compensating coil. Significant level of matching between two coils is required for this approach. Moreover, the ratio value of the power stroke and the overall volume is rather small. The second method is to use special thermally sensitive components (non-destructive resistors, for example). The major drawback of the method is that those sensitive components should have the same characteristics as the coil, and it is relatively hard to satisfy. Nevertheless, there are also several improved solutions. One of those methods is the compensation circuit approach, which is based on advanced design of signal evaluating circuits [12]. Although it has impressive performance, the complexity level of the method is high. The explanation of the approach is in following facts. The change of operational temperature causes significant change of the coil resistance. At the same time, the inductance of a well-designed coil varies only slightly. This is the basis of the compensation method

proposed in [12]. The compensating coil (with the equal resistance as in the sensing coil for the same temperature variations), is placed around the sensing coil (Fig. 3).

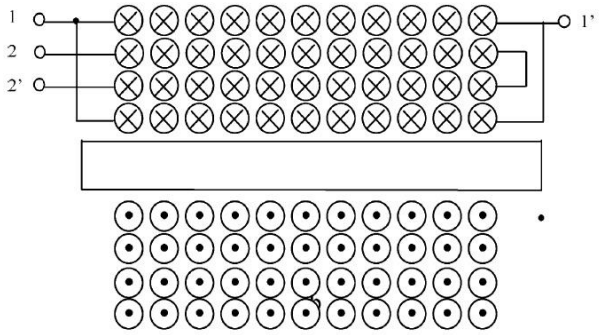

Fig.3. The placement of the coils:

the sensing coil (1) and the compensating coil (2) [12].

Furthermore, the compensating coil is not-inductive in order not to disturb working conditions of the sensing coil. The performance of the approach can be observed from the Fig. 4:

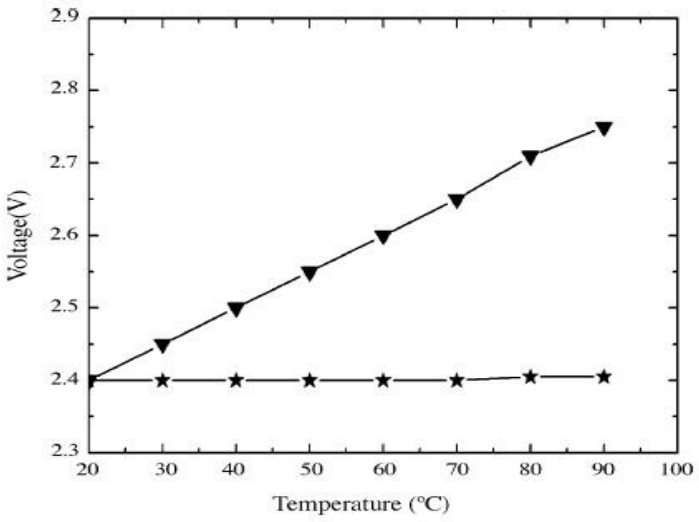

Fig.4. Comparison of the output signal for a system with temperature compensation (stars) and without it (triangles) [12].

Another possibility for increasing temperature stability is the insulation of a measuring system from the heat sources. In addition, Micro-Epsilon is one of the first manufacturers, which offer eddy-current sensors with active temperature compensation and possibility of the field calibration.

Eddy current sensors are widely used in bearings, and particularly, in active magnetic bearings due to high resolution, small size and temperature stability. Active magnetic bearings allow contactless operation of rotating shafts with low friction and material wear. AMB applications require high temperature operation and precision. SKF is one of the manufacturers, which specializes on sensors for bearing systems. They developed special magnetic bearing digital control system MBControl with sensors having the following operating parameters:

- **Sensitivity**: 50 μm/V;
- **Linearity**: 1%;
- **Range**: 1.5 mm;
- **Resolution**: 30 nm
- **Operating temperature**: 17 Kelvin to 250 °C.

Additionally, sensors have a small size and mounted as a ring. This configuration gives high precision and does not require further adjustments. Moreover, MBControl has a built-in noise rejection filtering, which is important for noisy environments.

2.3.2 Linear range

Increasing of the linear range is commonly solved by software linearization or analog signal processing. Exponential function can be used for approximation of the output signal at frequencies lower than the resonance frequency [5, 9]. Also the special method of using magnetoplated wire (MPW) for the windings to improve linearity range is proposed in [13]. The comparison of the MPW wire and the conventional copper wire (COW) is shown in Fig. 5:

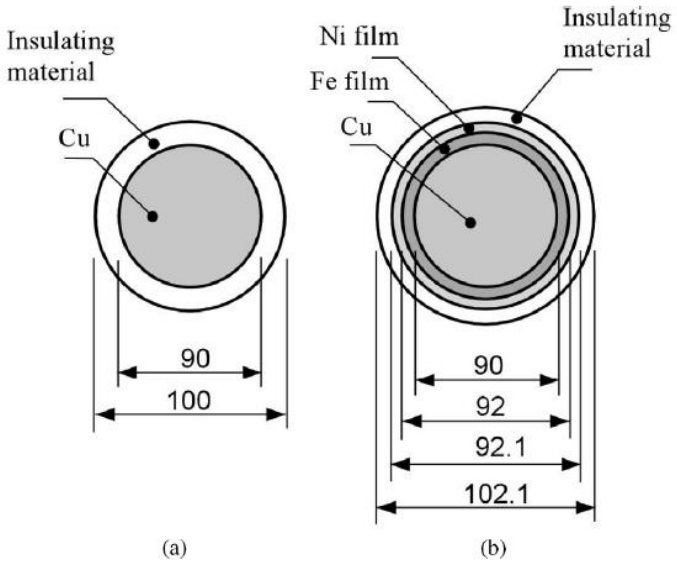

Fig.5. Comparison of the structures of the COW (a) and MPW (b) wires (units: μm) [13].

The magnetoplated wire, whose perimeter is surrounded by the thin magnetic films made from Ni and Fe, gives the opportunity to improve impedance characteristics (coil resistance, eddy currents losses decrease) and, therefore, detection sensitivity and linear range ratio, which can be described by the following expression [13]:

$$r = \frac{L_0}{D},$$

where r - linear range ratio; L_0 – linearity range, mm; D – diameter of the coil, mm;

For linearization of the output signal of the coil along with the exponential function such math functions as logarithmic, polynomial, tangent and others can be used. When the linearizer is applied to the system with the magnetoplated wire, the L_0/D ratio increased to more than twice [13].

2.3.3 Material dependence

The main drawback of the eddy current sensors is the material dependence and the associated problem of inhomogeneity (electrical run out). According to [14], the

impedance of the sensor coil is the function of several parameters, including resistivity ρ and permeability μ. As eddy current sensors can operate with both nonmagnetic (e.g. aluminum, titanium) and magnetic (iron or steel, for instance) materials, permeability and resistivity values for different target materials vary. This fact becomes the reason for the output noise and the resolution degradation because of disturbance in the eddy currents dissemination. Consequently, in each application the sensor should be calibrated exactly for the specific target with unique characteristics and properties in order to partially avoid the inhomogeneity issue. It is worth to notice that calibration is a sophisticated process, it consumes money and time.

Another source of inhomogeneity is the non-equalization between resistivity and permeability of the target. In this case, increase of the excitation frequency (in the amplitude modulated mode) and the oscillating frequency (in the frequency modulated mode) leads to inhomogeneity reduction [14]. The important fact, which should be mentioned, is that inhomogeneity in non-ferrous materials is lower than in ferrous because of lower resistivity ρ.

Pioneered digital multiple echo technique developed by Cygnus Instruments provides measurements with automatic recognition of probes and protective coating ignoring [15].

Material independent solution for eddy current sensor is described in [16]. The principle of this approach is in projection of the coil impedance vectors onto a projection plane. This projection gives the opportunity to eliminate the influence of electromagnetic properties of the material. As the result, resistance and inductance lines are linear for the same distance and various measurement targets [16, 17].

In addition, there is one fact, which should be taken into consideration. If the eddy current probes are located close to each other, their magnetic field can interact. It should be avoided by keeping probes in acceptable distance (approximately 3 diameters to the sides and 1.5 diameters back [1]) or by the special calibration procedure, which is performed in the Lion Precision ECL202, for instance.

2.3.4 Advanced solutions

One of the novel technologies, which can be used for performance improvement of the eddy current sensors in high temperature operational conditions, is the LTCC technology. The key point of the technology is production of the glass-ceramic multilayer system from single tapes, which are laminated and fired using low resistance materials such as Au or Ag with melting temperatures of 1100 °C and 960 °C, respectively. Low temperature co-fired ceramics (LTCC) consist of multiple layer tape made from glass-ceramic composites and include benefits from the previous technologies such as High Temperature Cofired Ceramics (HTCC) and Thick Film technologies:

- low processing temperature;
- metal with low resistance (Au, Ag);
- the use of printed resistor;
- number of layers is limitless;
- design is not difficult;
- price and weight are low;
- high durability;
- good thermal characteristics;
- independent to the gas properties [2].

Eddy current sensor coil with a ferrite core has a temperature range limited by the Curie temperature for the ferrites of 450 °C. Therefore, normal working temperature for such type of a core is below 300 °C. At the same time, when the core is made from ceramics, it increases the maximum operational temperature theoretically up to 1000 °C [2]. Consequently, those facts proved that the ceramics are the most preferred solution for eddy current sensors operated in high temperature environments both from the economic and technical points of view. The technology can be successfully implemented in avionics, computer, telecommunications and other areas.

Another advanced approach the use of arrayed eddy-current sensors (Fig. 6.). The system consists of the array of coils which are supplied from the same power source.

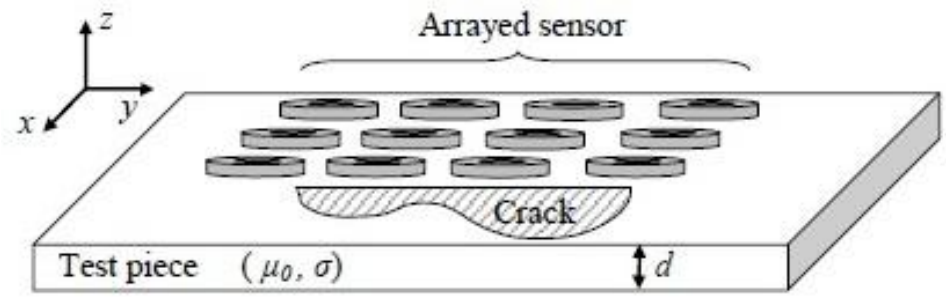

Fig.6. Arrayed eddy-current sensor [5].

Comparing to the separate feeding, which would have a positive effect of interference absence between the adjacent coils, such configuration have obvious advantages: no synchronization is needed for the supply and measurement, the system impedance is calculated using the voltage values, and more concretely voltage matrix (Fig. 7).

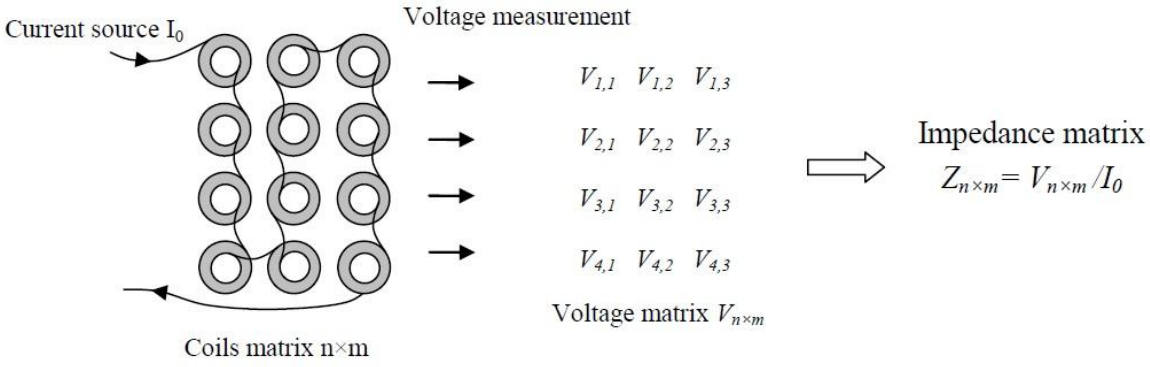

Fig.7. Impedance and voltage matrices [5].

Array inspection systems give the opportunity to make measurements and inspections more reliable, faster, and simpler.

Arrayed eddy current sensors found their implementation in AMB systems. One of perspective applications is described in [18]. Conventional technology of rotor deflection control is in using two eddy current sensors, one for each of two axes. Nevertheless, this approach has one obvious drawback of runout harmonics in sensor

signal. One of possible ways of overcoming this problem is increasing a number of sensors. In other words, the system is designed as a circular sensor array (Fig. 8).

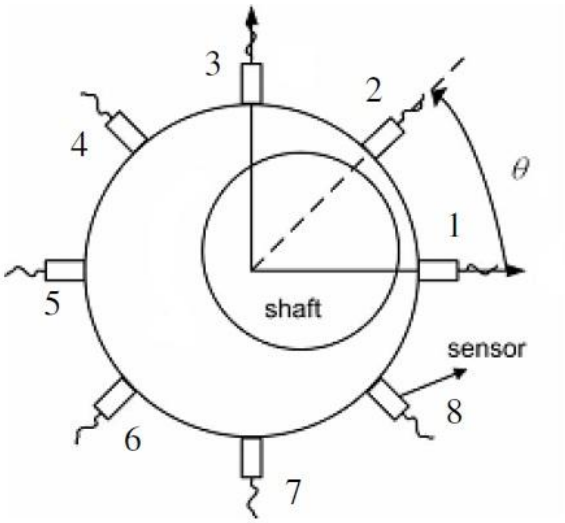

Fig.8. Configuration of the arrayed eddy current sensor [18].

The weighting sum of sensors outputs allows to remove certain runout harmonics.

2.4 Signal processing

Signal processing mechanisms have been used to handle digital and analog signals for many years in such wide range of areas as telecommunications, medicine, avionics, industry, robotics, control engineering and many others. For the sake of comparison between analog signal processing (ASP) and digital signal processing (DSP), DSP systems have now practically suppressed ASP because of the following advantages: better energy efficiency, low costs, resistance to temperature and aging. Development of the Discrete Fourier Transform (DFT) algorithms and the Digital Signal Processors only strengthened the superiority of digital signal processing based systems [19]. The typical signal scheme of DSP is shown in Fig. 9.

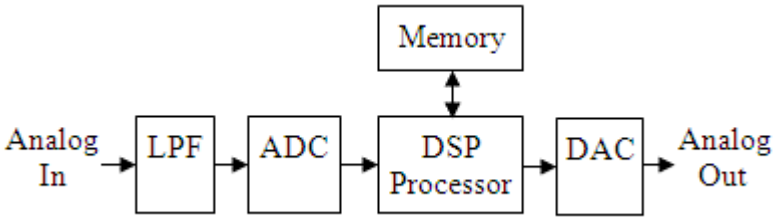

Fig.9. The typical signal scheme of DSP [19].

Before analog signals are converted to digital in Analog-to-Digital converter (ADC), they are going through the anti-aliasing filter, which is a low-pass filter (LPF). LPF filter limits the maximum sampling frequency to less than a half of the sampling rate of ADC. The DSP Processor manipulates the sampled signals and after that they pass Digital-to-Analog Converter (DAC) to the analog output.

2.4.1 Types of filters

One of the main purposes of filtering is to modify signals in the time and frequency domain [19]. As other analog components, analog filters based on RLC elements were replaced with their digital analogues. Laplace or *s* domain and Laplace Transform are used for modeling of analog filters. Linear time-invariant (LTI) filter is one of the most common types of digital filters. It is described by the following convolution process:

$$y[n] = x[n] \cdot f[n] = \sum_k x[k] \cdot f[n-k] = \sum_k f[k] \cdot x[n-k], \qquad (1)$$

where $y[n]$ – is the output signal; $x[n]$ – is the input signal; $f[n]$ – filter's impulse response [19].

LTI filters in their turn are divided into two groups: Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). The word *finite* stands for a finite number of samples, and, therefore, the sum in (1) is finite. At the same time, the IIR filters have an infinite number of samples and no sum limits in (1).

Another form of the LTI filter representation is the transfer function form in the *z*-domain:

$$Y[z] = X[z] \cdot F[z],$$

where $Y(z)$ – the system output, $X(z)$ – the system input, $F(z)$ – the transfer function of the system.

Transfer function for the L^{th} order FIR filter in the *z*-domain can be described by the following expression [19]:

$$F[z] = \sum_{k=0}^{L-1} f[k] \cdot z^{-k}. \qquad (2)$$

The transfer function of the FIR filter has only zeros, which can be found as roots of the polynomial (2). Therefore, FIR filters are also known as all zero filters [19]. In addition, it is important to mention that typical FIR filters (not special CIC FIR filters) are nonrecursive filters, they do not have a feedback.

The block diagram of the FIR filter is shown in Fig. 10.

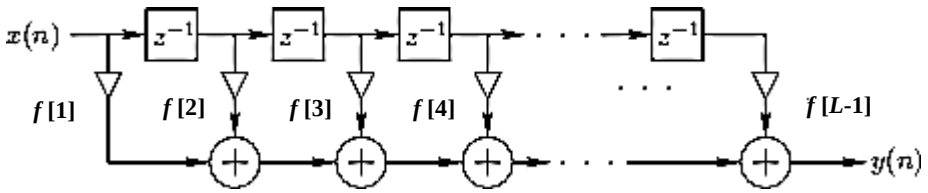

Fig.10. The FIR filter block diagram [19].

IIR filters can be designed as the transformation of analog filters to the digital domain. Unlike FIR filters, IIR filters are always recursive filters, they have a feedback and their impulse response is infinite.

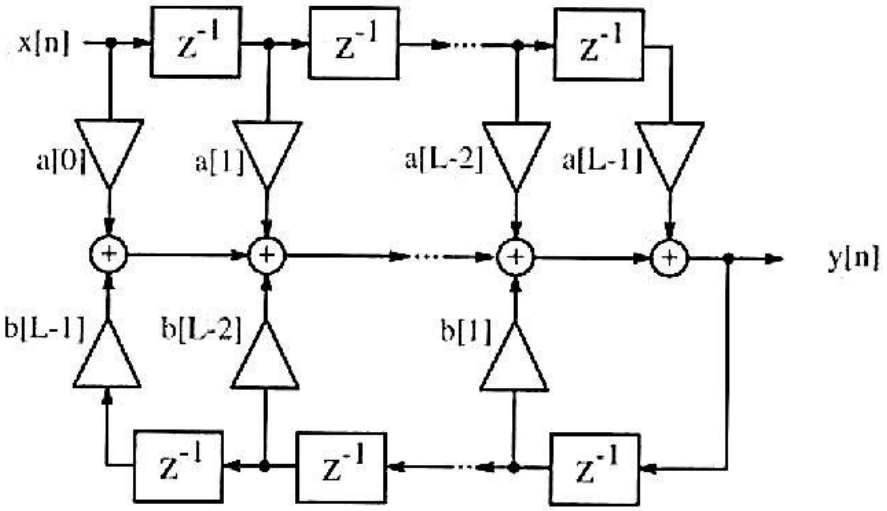

Fig.11. The block diagram of the typical IIR filter [19].

The block diagram (Fig. 11) shows *two parts* of the IIR filter – nonrecursive (upper) and recursive (bottom). The transfer function of the filter can be written as the following:

$$F[z] = \frac{\sum_{l=0}^{L-1} a[l] \cdot z^{-l}}{1 - \sum_{l=1}^{L-1} b[l] \cdot z^{-l}}. \qquad (3)$$

As it can be seen, the transfer function has a nonrecursive part in a nominator and a nonrecursive part in a denominator, while roots of the nominator are zeros and roots of the denominator are poles.

Comparison between FIR (typical) and IIR filters is presented in Table 1.

Table 1. FIR (typical) and IIR filters comparison [19, 20].

Factor	**FIR filters**	**IIR filters**
Linearity	Linear applications	Non-linear applications
Feedback	No feedback	Feedback is involved
Stability	Always stable	Can be unstable
Usability	Become long in feedback systems and make problems	Due to short delays, they are widely used and have good performance

Memory requirements	Require more memory	Require less memory
Roots	Zeros	Zeros and poles
Multiband design	Multiband filters are possible	Multiband design is difficult
Tapping order	High-order tapping	Low-order tapping
Multi-rate applications	Suitable for multi-rate applications (decimation and/or interpolation) due higher computational efficiency	Multi-rate applications are difficult to implement because of presence of a feedback.
Cycle limits	Unlimited cycles	Limit cycles can occur

As we can see, both filter types have their advantages and disadvantages and suit for specific applications.

2.5 Field Programmable Gate Array (FPGA)

Field Programmable Gate Array (FPGA) is an integrated circuit that can be programmed and configured repeatedly. FPGAs take their beginning as the successors of the Programmable Logic Devices (PLD) and Programmable read-only memory (PROM). The main advantage of such chips is the possibility to implement a wide range of user functions by software programming. Furthermore, nowadays FPGAs have significantly less cost and development time compared with the Application Specific Integrated Circuit (ASIC) technology; however, at early stages of FPGA history, they were slower and less energy efficient than their ASIC rivals. Nowadays, after many years of development FPGA chips proved their feasibility from technical and economical points of view.

2.5.1 History of FPGA

Xilinx is not the only company producing solutions based on the FPGA technology. For instance, Altera, Actel and Lattice Semiconductor are their rivals. Nonetheless, the FPGA chip, which was used in the work, is from Xilinx, therefore all the descriptions will concern mainly this company.

History of programmable logic started in the beginning of the 1970s with Programmable Logic Arrays (PLA). PLA chip consisted of AND and OR gates and could give the opportunity to implement simple design in disjunctive normal form. There was only one opportunity to program the chip. Typical PLA structure is shown in Fig. 12.

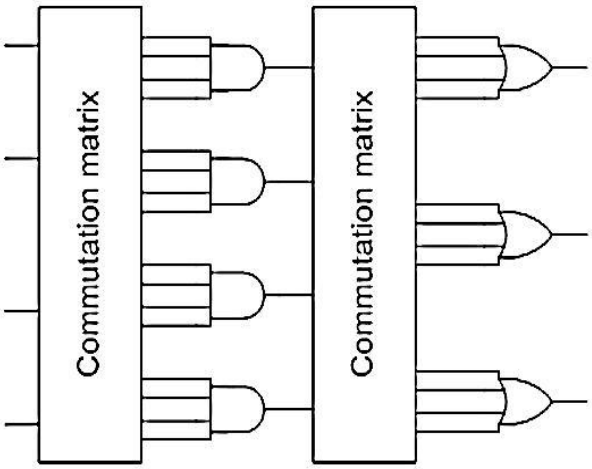

Fig.12. The structure of PLA [21].

The structure of PLA includes inputs, outputs (OR gates), AND gates and commutation matrices (fuses). It is important to mention that the logic gates are hardwired; only commutation matrices can be programmed, and it is done by burning the fuses [21]. In addition, configuration of the structure presented in Fig. 12 with only left programmable commutation matrix (right one is fixed) is called Programmable Array Logic (PAL). Later the PLA technology was improved and transformed into the Complex Programmable Logic Devices (CPLD) technology, now competing with the FPGA.

The FPGA technology introduced new features, which were not available before. Among them were special antifuse elements with initially high resistance, which were made from Si, for instance, and placed at the junctions of the communication paths. When a device was programmed, the resistance decreased to few Ohms [22]. The disadvantage is that the interconnections are not programmable.

The first commercially available application of the FPGA was developed in 1985 by Ross Freeman, co-founder of the Xilinx Company, which was in turn founded in 1984. The name of the product was the XC2064. It had 64 configurable logic blocks and two 3-input lookup tables [23].

The Virtex board family, the main revenue driver for Xilinx to the present day, was introduced in 1998 [23]. The architecture offered outstanding operating characteristics for the implementation of a wide range of designs, including sophisticated ones.

In 2003 Xilinx presents their one of the popular architectures – the Spartan 3 family. The main advantage of those chips is their low price. At the same time they have rather high performance comparing to more advanced and expensive Virtex chips. Nowadays Xilinx is the world leader in programmable logic devices market with 51% (Altera is the closest rival with 34 %), supplying reliable and effective solutions for different applications in various areas. In addition to mentioned facts, it is the Xilinx Spartan 3 xc3s1000-4ft256 chip, which is used in the work.

In 2010 Xilinx introduced their 7 Series, including such product families as high-end Virtex, medium range Kintex and low range Artix family. It means that history of Spartan series ended with the previous sixth generation. The new family lines are based on 28 nm process with low power consumption (up to 50% lower than in 40 nm solutions) and extremely high capacity of 2 million logic cells [24].

To go even further Xilinx introduced multi-chip packing technology. The key feature of the technology is in stacking several (three or four) 28 nm chips side-by-side on a silicon interposer [25]. This approach is developed for complex designs in order to increase performance, productivity and efficiency.

At the beginning of 2011, Xilinx acquired AutoESL Design Technologies company to make it possible to implement designs in their new family series using high level languages (for instance, C, C++ and System C), expanding the design community [26].

2.5.2 Architecture of FPGA

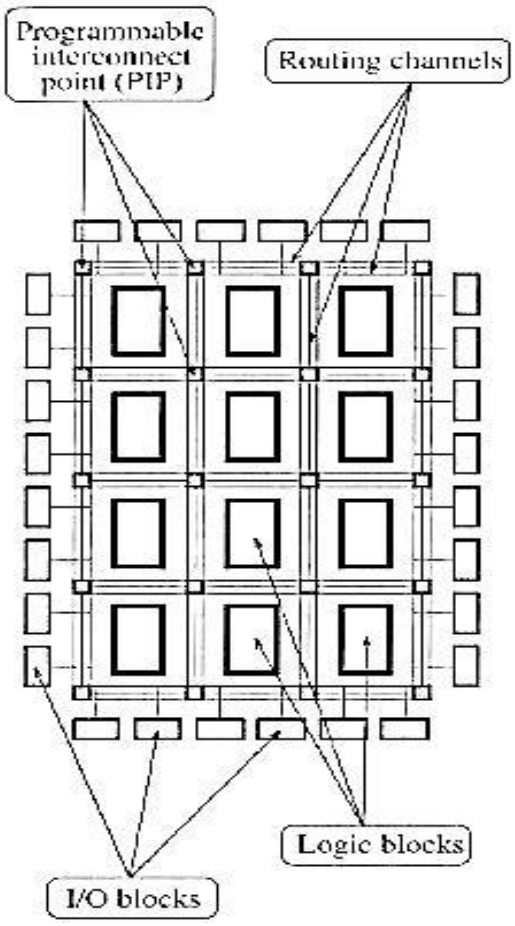

Fig.13. The architecture of a FPGA [19].

The architecture of the FPGA technology, which describes its key points, is shown in Fig.13.

The primary parts of the chip are the configurable logic blocks (CLB) for the implementation of different logical functions; the input/output blocks (IOB) for the interface between external pins and internal signals; and the routing channels for connection between blocks.

There are two types of IOBs. The first is used for the FPGA configuration; the second one defines the user configurable blocks – they can be programmed as inputs, outputs or to be bidirectional for internal and external interconnections [22]. The input block can route a signal straight to the channel or through an input register. At the same time, the output block sends a signal (which can be inverted) through a register to the output buffer.

As it was stated above, one of the main parts of the FPGA is a configurable logic block (CLB). Both synchronous and combinatorial circuits can be designed with CLBs [27]. The structure of the CLB comprises four slices and basically includes a

Look-Up Table (LUT), a Flip-Flop (latch) and multiplexers (Fig. 14 a)). Any 4-input boolean function (AND, OR, NOT, XOR) can be generated by a Look-Up table with four inputs and one output. So the main purpose of a Look-Up Table is a realization of logic functions. Storage elements are generally utilized to synchronize data to a clock signal, and wide-function multiplexers provide combination of LUTs to perform complicated logic operations. D Flip-Flops have a clock enable input that can be inverted for the negative or positive triggering edge. In addition, set/reset input allows asynchronous resetting of the Flip-Flop.

a) b)

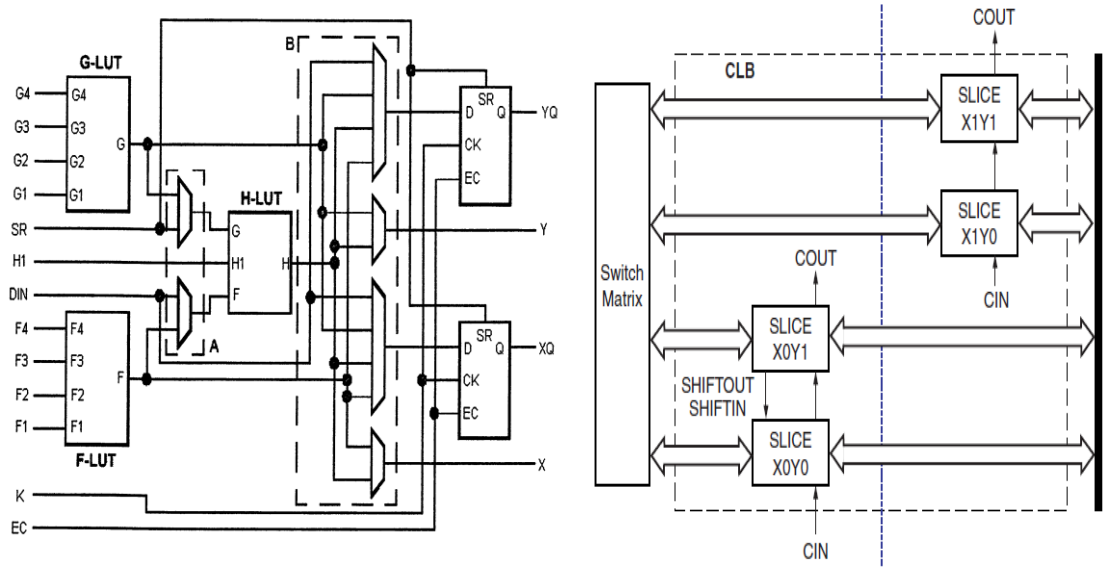

Fig.14. a) the structure of CLB (Spartan family) and b) slices arrangement [27].

All four slices of the configurable logical block can be virtually divided into two parts – the left pair and the right pair. In addition to the functions (arithmetic, logic, ROM), available for both left and right pairs of slices of the CLB (Fig. 14 b)), the left pair can implement shifting data and distributed RAM functions.

Routing channels are metallic conductors, and they are used to connect the FPGA components. There are three types of routing channels [22]:

- **Global routing channel**, which are used to transmit global signals;
- **CLB routing channel** goes through a configurable logical block;
- **IOB routing channel** connects IOBs with the CLB routing channels and creates a kind of ring around the CLB array.

Depending on the length of the line routing channels can also be classified as single length, double length and long lines. Single length lines go through the one CLB or provide short connections between CLBs. Double length lines are used to communicate between two CLB with low transfer delays. Long lines are spread along the whole length of a chip.

FPGA architecture is based on the SRAM memory technology and should have the volatile type of memory for storing a current configuration. At the same time, Complex Programmable Logic Device (CPLD), a competing technology, has energy-independent memory (Flash or EEPROM). As the FPGA technology requires downloading the programming configuration to a device it is less protected against unauthorized use than the CPLD technology, which has not such a requirement.

2.5.3 Very High Speed Integrated Circuit Hardware Description Language (VHDL)

There are two languages, which are used in FPGA design – VHDL (common for US east coast and Europe) and Verilog (spread in US west coast and Asia) [19]. Both languages have their own advantages, and after implementation of IEEE standards 1364-1999 in the Verilog language supporting signed math operations (that made it more readable), the choice of language became the matter of personal preferences.

Very High Speed Integrated Circuit Hardware Description Language (VHDL) is used for configuration of hardware in different applications. Nevertheless, firstly the VHDL language was developed for the US Department of Defense and only for simulation purposes [28]. Nowadays it is widely used and supported by all major hardware design tools manufacturers.

Description of any object in VHDL consists of two stages: definition of inputs/outputs (interface part) with `entity` keyword and `architecture` part, which includes all the rules how the block works. The example of OR gate description in VHDL is shown below:

Example 1. OR Gate VHDL implementation

```
entity ORGATE is

    Port ( X : in  STD_LOGIC;

           Y : in  STD_LOGIC;

           Z : out  STD_LOGIC);

end ORGATE;

architecture ORGATE_ARCH of ORGATE is

begin

    Z <= X or Y;

end ORGATE_ARCH;
```

List of instructions are written in `architecture` body after `signal` declaration within a `process`. Instructions can be executed sequentially or concurrently. The process declaration:

```
process (x,y)
```

contains sensitivity list in brackets. Sensitivity list includes signals, whose change affects execution of a process. Processes give the opportunity to separate combinatorial and sequential logics and make the code more readable and modular.

There are three types of objects in the VHDL language: signals, constants and variables.

Communication between processes and even between entities is conducted with signals, which are declared before `begin` keyword in the `architecture` body. For instance, the string

```
signal clk: std_logic := '0';
```

shows a declaration of the signal with name `clk` with length of a single bit (`std_logic`) and initial value of 0. In addition, multiple bit values (busses) are

written as `std_logic_vector(x downto y)`, where the number of bits or selection of concrete bits are defined with `x` and `y`.

Constants represent just names for values: `timer_limit := "100101";` or `clock_enable := '1'.` They help to keep the code more organized.

Variables are declared locally and remain visible only in a process. One of the main differences between signals and variables is that variable assignment is scheduled immediately, and it takes certain time delay for a signal (called delta time) [29].

2.5.4 FPGA software

Manufacturers of field programmable gate arrays (Xilinx, Altera) along with hardware development create their own software for their products. The ISE Design Suite is a powerful design environment from Xilinx.

Initial step of the design in ISE is adding *source* files to a created project. Those source files can include: HDL files such as VHDL, Verilog; schematics, test benches, Xilinx Core Generator modules, user constraints and others. The project should have a top-module and lower level source files.

Implementation of the design for a device in ISE Design Suite from a project with VHDL files or schematics to a programming file consists of several steps:

- Synthesize, where the design synthesis and generation of netlist files take place. User can also check syntax, view RTL (Register Transfer Level) schematic and generate post-synthesis simulation model at this step.
- Implement design – is the main part for a hardware implementation. It includes translation, mapping, place-and-route procedures. User constraints (timing and I/O planning) are also checked here.
- Generate Programming File. This step prepares design information and generate output file for specific device family.

Created design can be verified using behavior or timing simulations. It is important to notice, that timing simulations require full design implementation for the FPGA with place-and-route procedures done.

Key components of the ISE Design Suite: Logic Edition, which help to optimize a design and make it more effective, are presented in Table 2.

Table 2. Components of the ISE Design Suite: Logic Edition [30].

Components	**Description**
Xilinx Synthesis Technology (XST)	Makes a VHDL Synthesis
ISim	Provides a possibility to implement functional and time simulations of the design
PlanAhead software	Helps to arrange inputs/outputs, ports and pins
CORE Generator software	Provides user with a rich library of Xilinx elements from simple (comparators, counters, memory elements, registers) to complex (turbo decoders, video timing controllers)
SmartGuide technology and Design Preservation	Gives the opportunity to use results of previous implementations in a current design
iMPACT	Allows to configure Xilinx FPGAs with Xilinx programming cables
XPower Analyzer	Analyzes power consumption of a Xilinx device

DSP (Digital signal processing) Edition of the ISE Design Suite along with features of the Logic Edition provides capabilities of System Generator for Matlab Simulink. This tool gives the opportunity to implement your own design in Simulink and generate a programming file for a device without any experience with the VHDL coding. This feature of the Xilinx ISE Design Suite is used in the work.

3 MEASURING SYSTEM

3.1 Industrial sensors evaluation

The scope of this part of the work is to evaluate and compare industrial and custom made eddy-current sensors. Custom made eddy-current sensors are constructed in order to reduce costs and space. Design of the custom made sensor includes the use of the FPGA chip and AD-converters, which give the opportunity to process measured signals right from the sensor and avoid utilizing the huge analog driver boxes. Moreover, FPGA chip allows to improve signal to noise ratio by implementing additional signal processing algorithms.

3.1.1 System components description

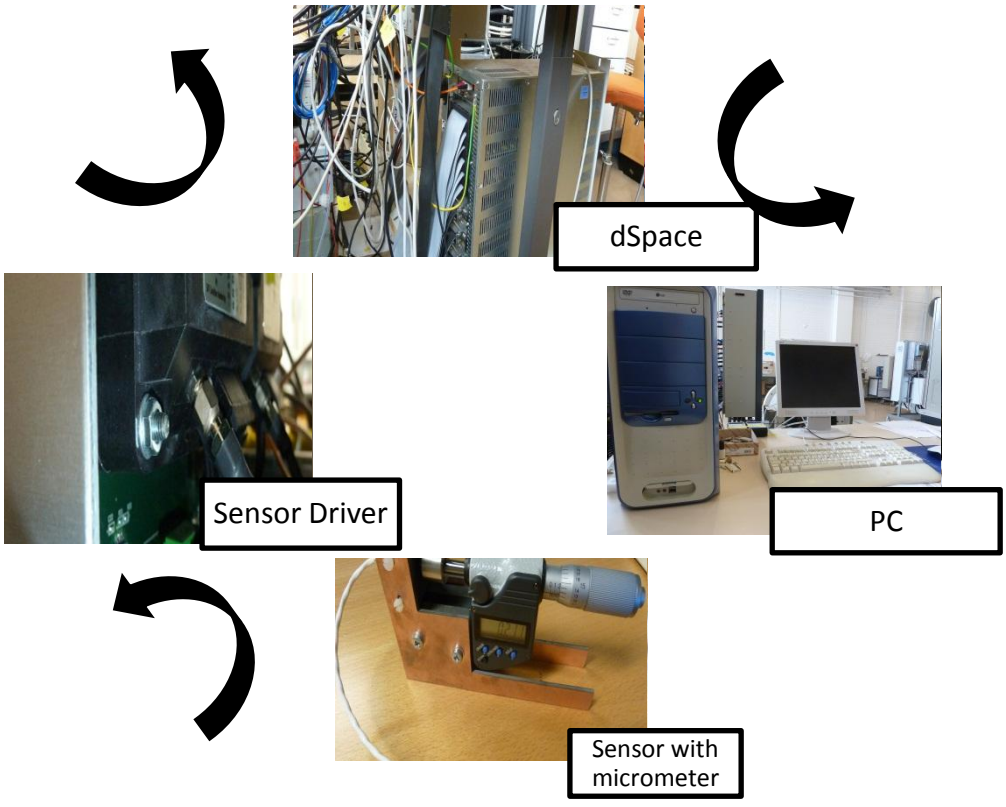

Fig. 15. Experimental installation.

The objective of the experiments is to track dependences of sensors work and evaluate necessary operating parameters. The experimental system (Fig. 15) comprises SKF Eddy Probe Systems, dSpace control panel, digital micrometer, connections between them and PC software (Matlab, Simulink).

The custom made sensor was compared to an industrial SKF CMSS 65 Eddy probe system. SKF offers a wide range of eddy probe systems for different applications. SKF sensors probe tips are made from Ryton - special material with such advantages as high stability, accuracy, resolution and linearity. Furthermore, Ryton allows operating in harsh environments (acids and other fluids, high temperature, pressure). Reliability of the system is also increased by using an internal sealing system, which protects components from moistening and corrosion [31]. Eddy Probe System consists of a probe, a driver and an extensional cable (optional).

Specifications of the SKF CMSS 65 Eddy probe system according to [31]:

Operating Range: 0.2 mm to 2.3 mm;

Operating Temperature Range: -34°C to +177°C;

Differential Pressure: to 4 Bar;

Sensitivity: 7.87 mV/ micron;

System Length: 5 meters;

Linearity: ± 25.4 microns of best straight line over 2 mm range;

Frequency Range: DC to 10 kHz;

Driver Signal Output: Impedance – minimum calibrated load resistance of 3 kΩ; Voltage - nominal sensitivity of 7.87 mV/micron corresponding to -18 VDC at 2.3 mm with -24 VDC supply.

Power Supply Requirements: 15 mA from -24 VDC to -30 VDC;

The dSPACE platform consists of the DS4003 Digital I/O board (96 TTL I/Os), DS1005-09 PowerPC board (PowerPC 750FX running at 800MHz, 512 KB level 2

cache, 128 MB SDRAM), DS2001 ADC boards and PC. Noise measurements and output signal values as the function of distance were collected with dSpace control panel and saved to .mat files. Noise measurements were conducted by setting the target to the middle of the operating range with a digital micrometer.

All measurements results were processed and visualized in Mathworks Matlab environment. Matlab is a powerful computational software tool, which is capable to resolve different problems in various areas, including economics, engineering, industry and others. Data files with .mat extensions obtained from dSpace control panel served as input data for plotting the graphs. The Fourier series expansion was held for spectrum analysis.

3.1.2 Dependence of the output signal from a distance

The experiment includes the output signal measurements as the function of a distance for three different samples (the aluminum sample, the Saimaa University sample and the NiFe sample). Theoretically, this dependence should be linear.

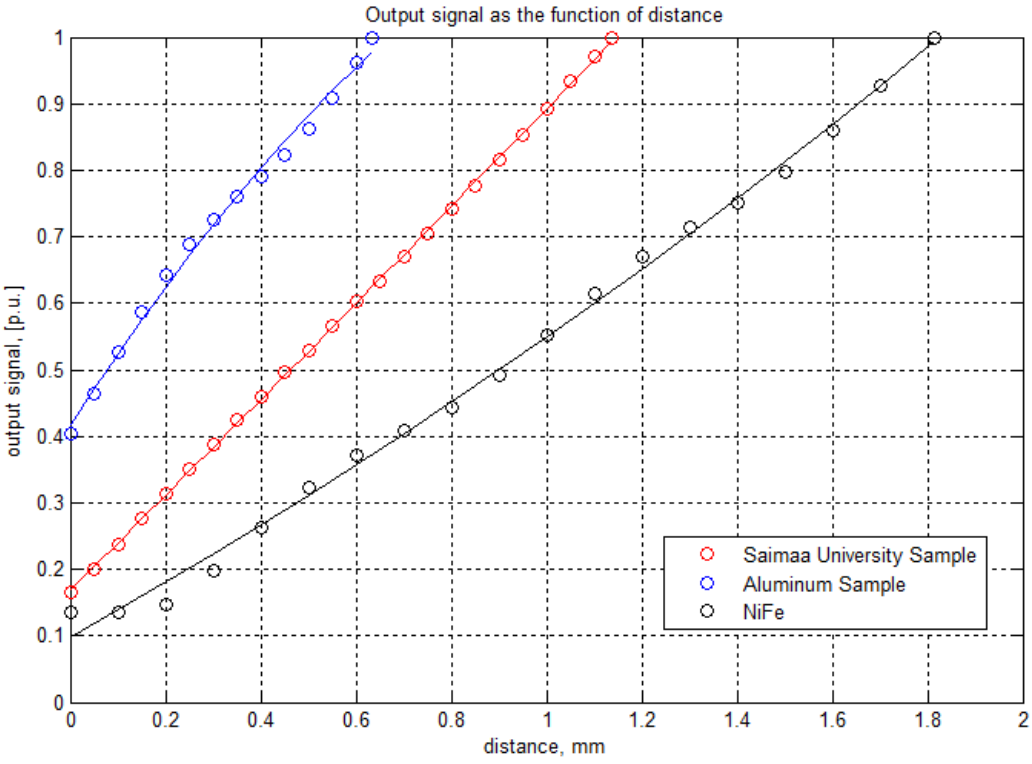

Fig. 16. Dependence of the output signal from a distance.

As it can be seen from the Fig. 16 all three plots are reasonably close to linear, but the Saimaa University sample is the closest one.

3.1.3 Assessment of the terminator impact

Adding a terminator at the operational amplifier or on the dSpace side leads to the resistance mismatch between them. Experiments were conducted in order to track the influence of the terminator.

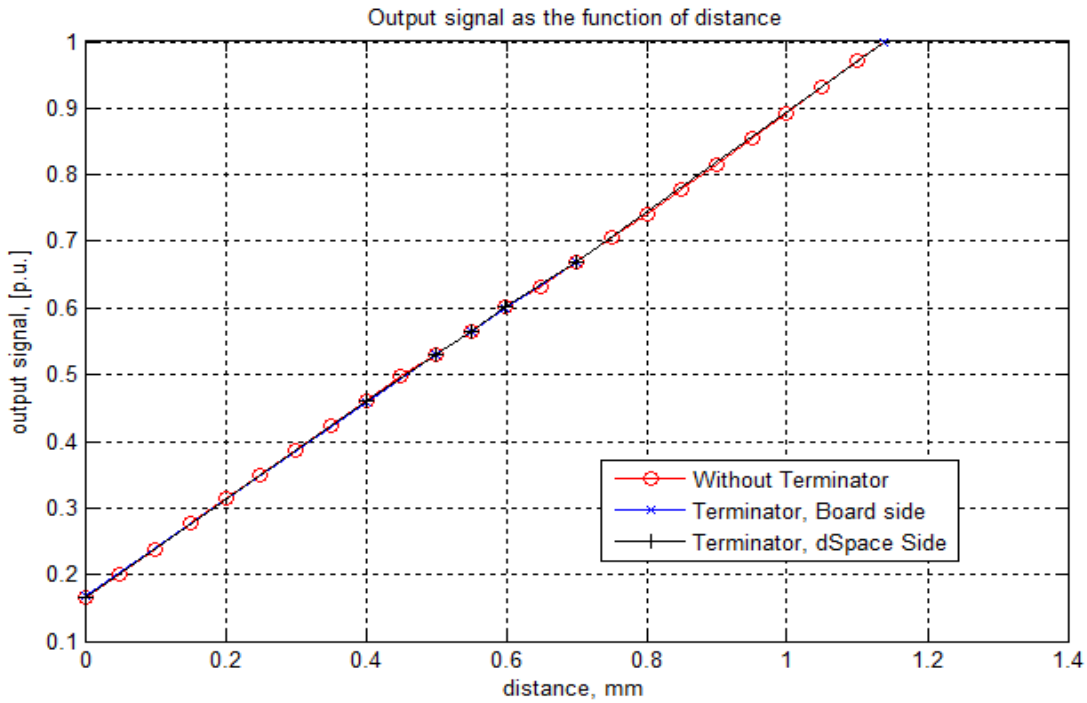

Fig. 17. Dependence of the output signal from a distance.

The dependences of the output signals from a distance for three different situations (without a terminator, with a terminator at the amplifier, with a terminator on the dSpace side) are shown on the Fig. 17.

It can be concluded, that the terminator impact is negligible. Nevertheless, let us track the impact on the noise and spectrum plots. The measured data were mean centered for noise analysis (Fig. 18) and decomposed into a Fourier series for a spectrum plot (Fig. 19).

Initial parameters for the Fourier transform:

- Sampling frequency: F_s = 40000 Hz;
- Sampling period: T = 25 µs;
- Length of signal: 5 s;
- Spectrum is plotted in a range from 0 to 5000 Hz.

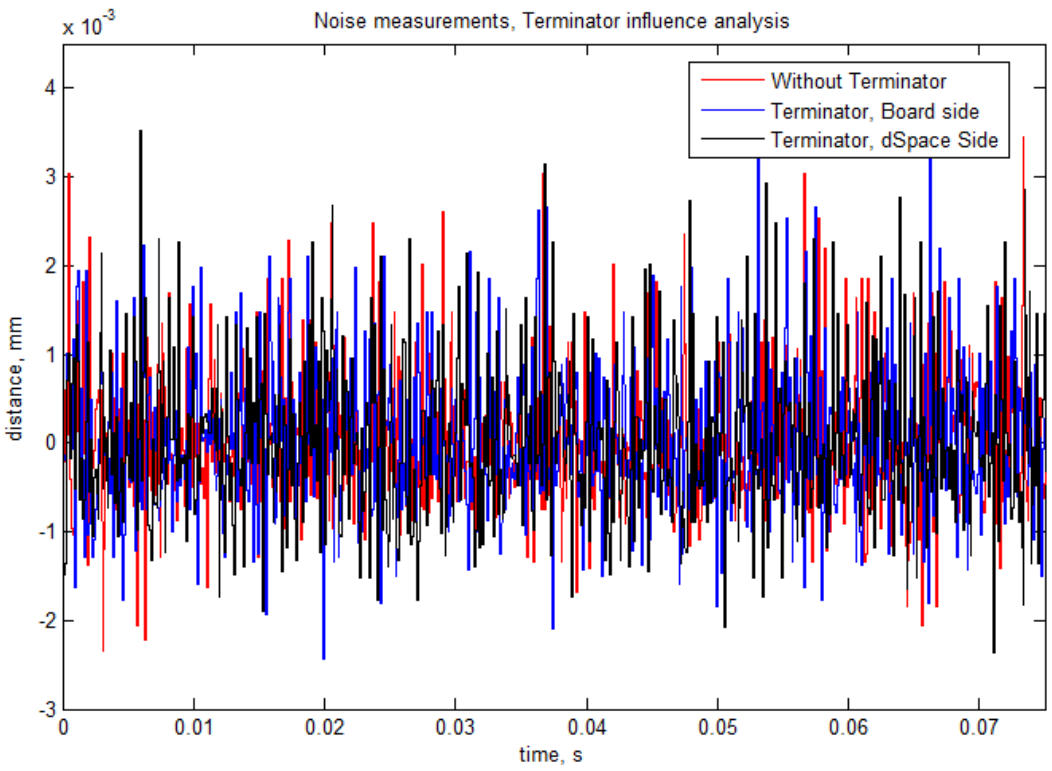

Fig. 18. Noise measurements (terminator impact analysis).

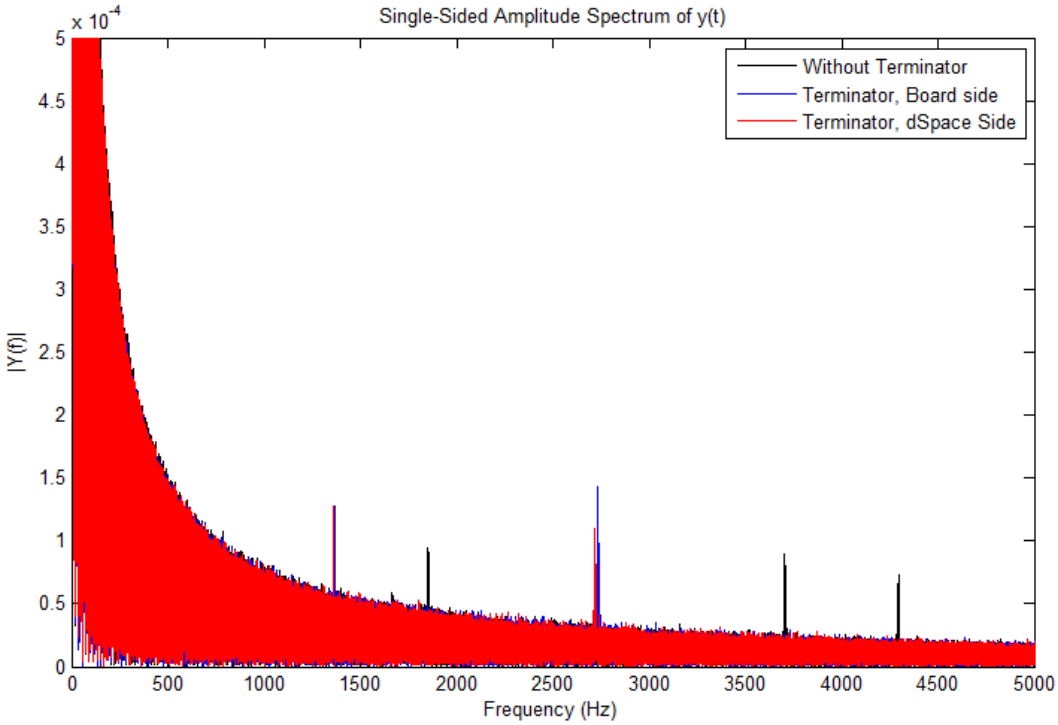

Fig. 19. Spectrum (terminator impact analysis).

The parameters of the measurements can be found in the Table 3.

Table. 3. Parameters of the experiments (terminator impact analysis).

Paramater	without a terminator	with a terminator at the amplifier	with a terminator on the dSpace side
Measurements time,s	5		
Sampling time, µs	25		
Deviation value, V	$6.0450 \cdot 10^{-4}$	$6.2932 \cdot 10^{-4}$	$6.5750 \cdot 10^{-4}$
Deviation value, mm	$0.8319 \cdot 10^{-3}$	$0.8775 \cdot 10^{-3}$	$0.9069 \cdot 10^{-3}$

It can be concluded from the noise and spectrum plots, that the data have a tendency to the white noise. Harmonics, which are presented in Fig. 19, can be caused by errors of calculation algorithms of the Fast Fourier Transform (FFT) in Matlab. In addition, the spectra for the three situations are practically identical.

3.1.4 Assessment of the sensor type impact

The measurements were conducted with three same SKF sensors (marked as Sensor 1, Sensor 2 and Sensor 3) to investigate potential differences. As in previous experiments the graph, presenting the output signal as a function of distance, was plotted. The results are shown in Fig. 20.

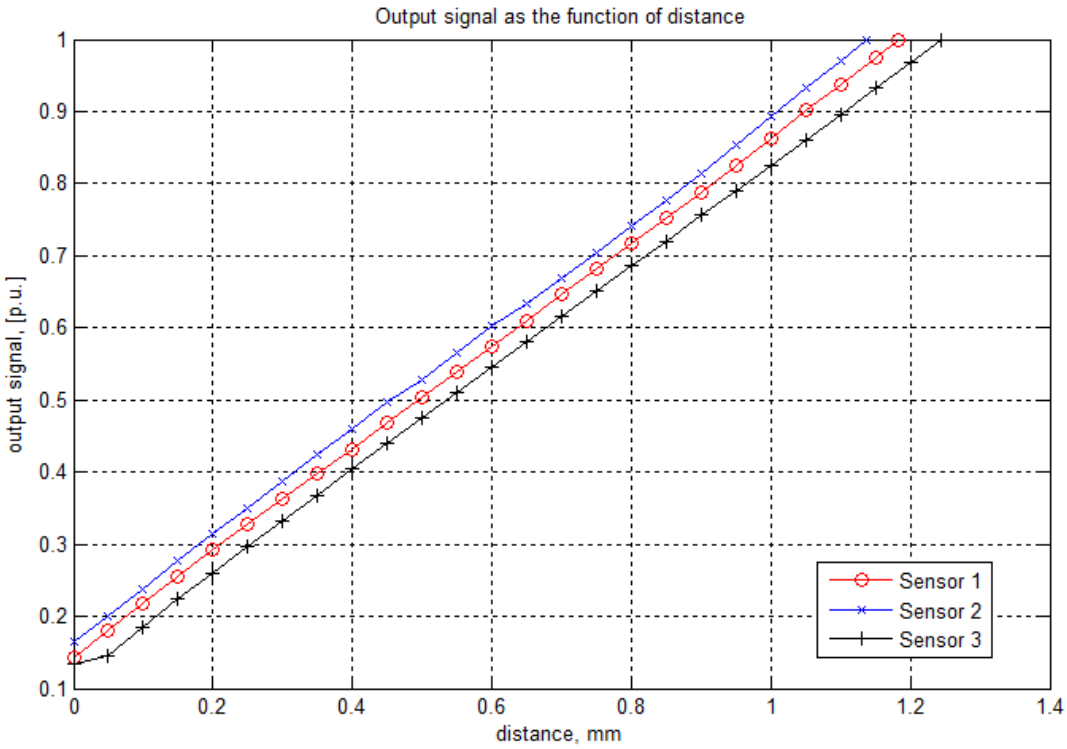

Fig. 20. Dependence of the output signal from a distance.

Three SKF sensors of the same type showed divergence between lines. For the sake of comparison, output signal values for the fixed target sample position of 700 µm are shown in the Table 4.

Table 4. Output signal values.

	Sensor 1	Sensor 3	Sensor 4
Output signal value, V	0.646	0.669	0.617

Thus, the divergences are:

- Between sensor 1 and sensor 3:

$$\delta_1 = \frac{0.669 - 0.646}{0.669} \cdot 100\% = 3.438\%;$$

- Between sensor 3 and sensor 4:

$$\delta_2 = \frac{0.669 - 0.617}{0.669} \cdot 100\% = 7.773\%;$$

- Between sensor 1 and sensor 4:

$$\delta_2 = \frac{0.669 - 0.617}{0.669} \cdot 100\% = 4.489\%.$$

The mean value for the divergence is:

$$\delta = \frac{3.438 + 7.773 + 4.489}{3} = 5.233\%.$$

Noise and spectrum plots are presented in Fig. 21 and Fig. 22 respectively. Initial parameters for the Fourier transform are the same as for the experiments from 3.1.3 section.

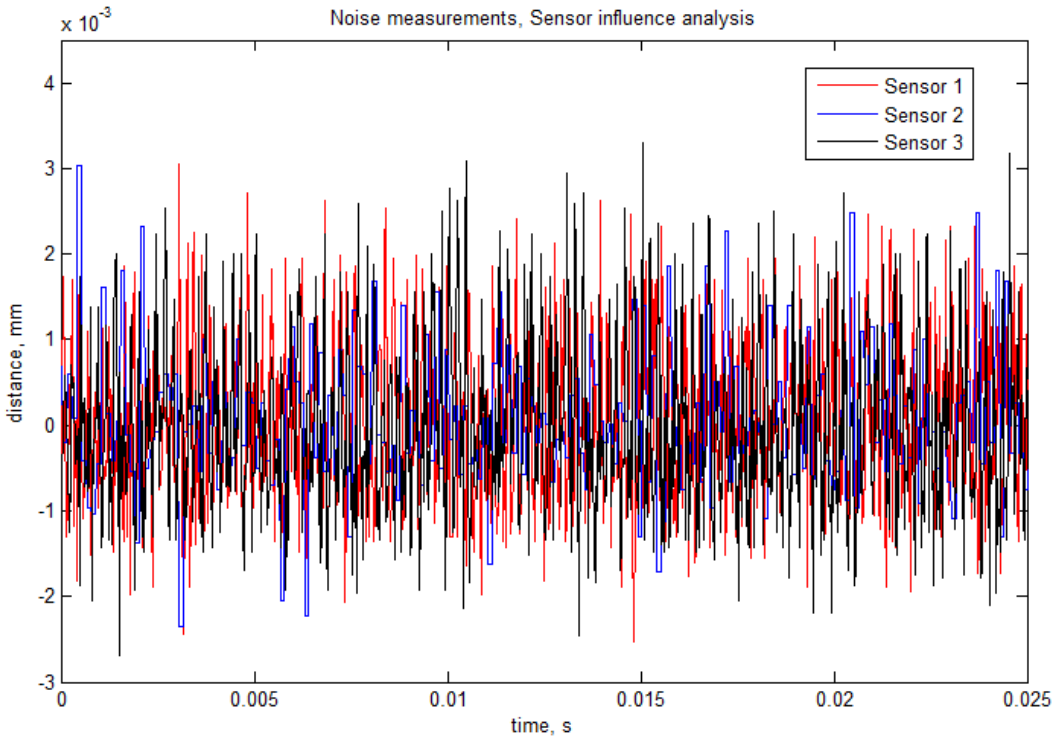

Fig. 21. Noise plot.

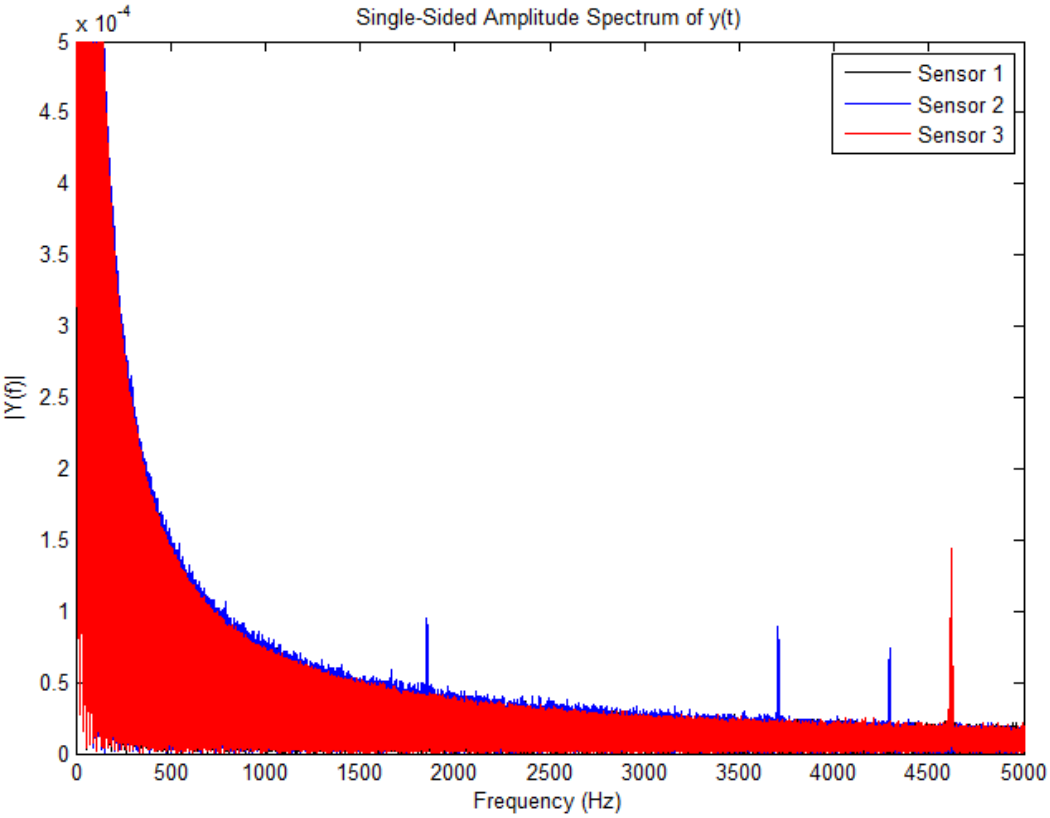

Fig. 22. Spectrum plot.

Spectrum and noise plots prove the fact of identity of the sensors.

3.2 Custom-made sensor

The system (Fig. 23) based on the custom-made eddy current sensor, Xilinx Spartan 3 FPGA board, Xilinx programming cable and USB cable for the interface between PC and board was developed in Electrical Engineering Department of Lappeenranta University of technology. The scope of the work is to rebuild existing project for the custom-made sensor, implemented with VHDL coding in Xilinx ISE Design Suite, with a new one, generated by Xilinx System Generator for Matlab Simulink.

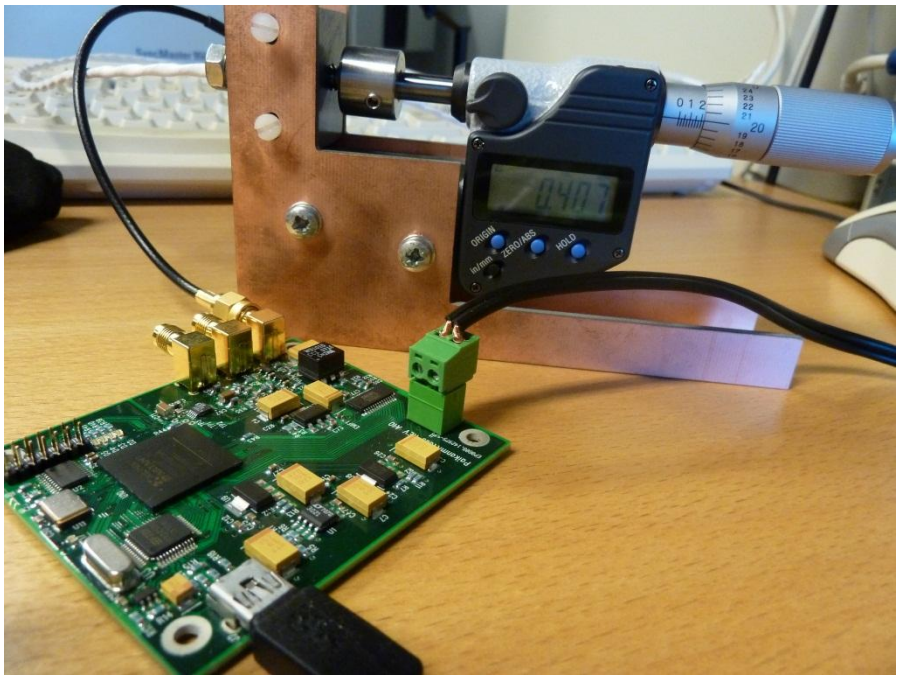

Fig. 23. Custom made sensor system.

3.2.1 FPGA board components description

The major part of the system is the FPGA board, which is used to handle signals from the sensor, process them and transfer to PC. The board is based on Xilinx Spartan 3 xc3s1000-4ft256 FPGA chip. Xilinx Spartan 3 family is a 90-nm solution

that offers high performance in wide range of applications at the reasonable price. Specifications of the chip are shown in Table 5.

Table 5. Attributes of Xilinx Spartan 3 xc3s1000-4ft256 [32].

Attribute	**Value**
System gates	50000
Logic cells	17280
Total amount of CLBs	1920
Distributed RAM	120000 bits
Block RAM	432000 bits
Dedicated multipliers	24
DCMs	4
Maximum user I/O	391
Speed grade	Standard Performance
Package type/ Number of pins	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)

Fine-Pitch Thin Ball Grid Array stands for one of the possible package types. FTBGA is a thinner version of Ball Gate Array (BGA), based on using metal spheres for external electrical interconnection [33]. The balls are attached at the bottom side of the chip. Main benefit of FTBGA is high possible density of pins on a package.

Among other advantages of Spartan 3 Family the following can be mentioned:

- DDR, DDR2 SDRAM support;
- Fast logic resources;
- Full support of Xilinx ISE and WebPack software design tools;

As it was mentioned in previous chapters, FPGAs have static memory for storing load configuration when the power is off. After powering on, the chip is programmed by writing the configuration from memory. One of the best choices of memory is a cheap Xilinx Platform Flash PROM, which gives the opportunity to make the programming process more efficient and flexible due to such features as small area

per megabit, on-board programming support, advanced compression technologies for improved memory capacity, easy field upgrades, Xilinx ISE environment support [34].

Xilinx USB Programming cable was used to load configuration from Xilinx ISE Design Suite to the FPGA board. With this cable indirect programming through JTAG port using flash memory is possible. Nonetheless, platform cable is recommended by the manufacturer for design development purposes, not production programming.

For AD/DA conversion purposes corresponding 14-bit ADC and DAC modules are included in the board.

3.3 Model synthesis

The model was developed in Simulink environment as the interpretation of the existing project for the custom-made eddy current sensor. The purpose of this approach is to investigate the possibility of time and resource efficient design, thanks to new features of enhanced integration between Xilinx software tools and Matlab Simulink.

3.3.1 Software description. Xilinx System Generator for Simulink

Xilinx System Generator for Matlab Simulink provides the possibility to implement design for Xilinx FPGA hardware without VHDL coding using just Simulink blocks from the Xilinx Blockset. This approach significantly decrease time consumption and enable user to build projects from simple to complex, improve them with signal processing mechanisms and make necessary simulations right in Simulink environment. Moreover, synthesis and place-and-route procedures for generation of the programming file can also be performed.

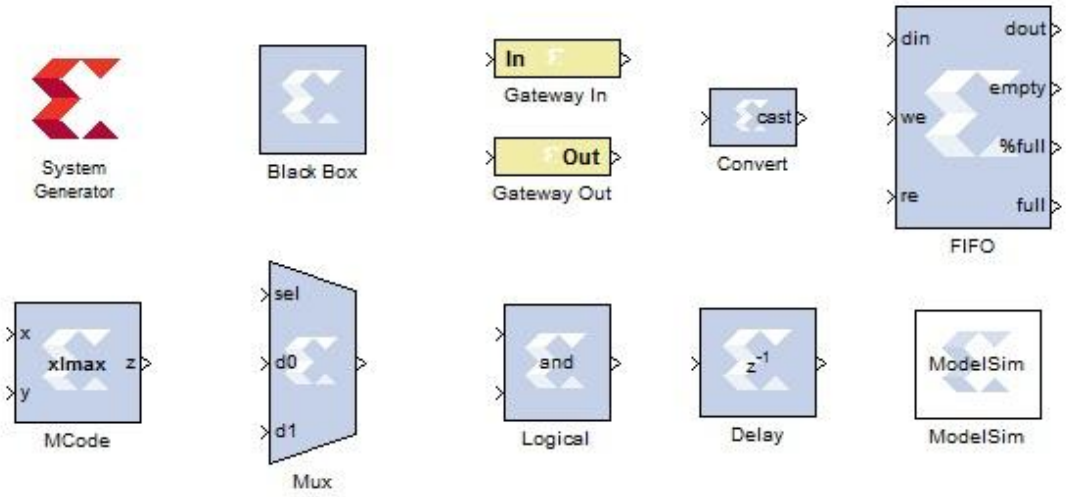

Fig. 24. Xilinx Blockset blocks.

System Generator provides over 100 blocks in Xilinx Blockset to build custom design as a Simulink model. The blockset includes basic, control logic, data types, math, memory, DSP and other blocks. Several main blocks are shown in Fig. 24.

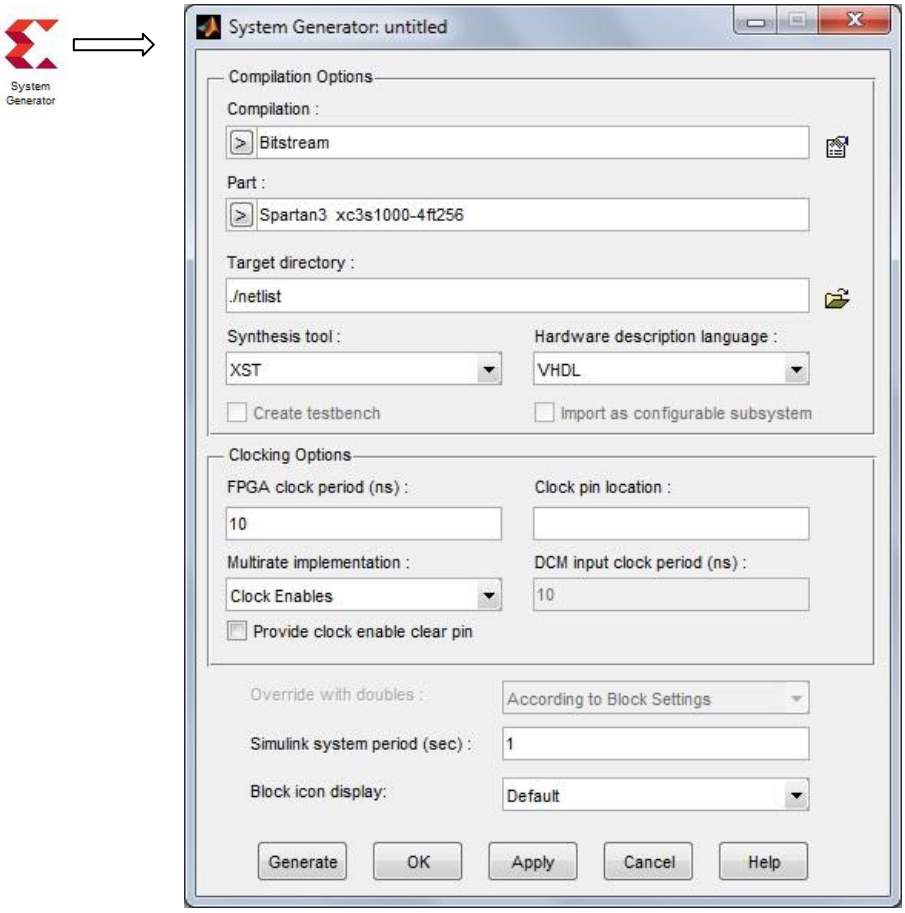

Fig. 25. System Generator token and configuration window.

One of the important blocks is a System Generator token. Configuration window of System Generator can be accessed by double-click on the System Generator token (Fig. 25).

Configuration window allows customizing settings and parameters of the System Generator. It includes the following main fields:

- *Compilation* – user can choose the type of compilation. It can be HDL Netlist (default), Bitstream (comprises HDL Netlist, synthesis and the XFLOW process of configuration and implementation);
- *Part* – specifies FPGA product family and its parameters. In the project it is Spartan 3 xc3s1000-4ft256;
- *Target directory* – defines a folder, where compilation files are stored;
- *Synthesis tool* can be chosen from several possibilities: Synplify, Synplify Pro, XST (default);
- *Hardware description language* – VHDL or Verilog;
- *FPGA clock period* – specifies the clock of the FPGA chip in ns;
- *Clock pin location* – sets the position of the clock pin on the FPGA;
- *Block icon display* provides the possibility to specify information that is displayed on the icon. It can be sample frequencies, normalized sample periods, HDL port names, input/output data types or pipeline stages;
- *Simulink system period* – defines internal period for Simulink. Default value of 1 means that the Simulink system period is equal to FPGA the clock period.

Gateway In and *Gateway Out* blocks are designed to separate Xilinx blocks from Simulink blocks in the model. It is important to notice that the Simulink project that is intended to be used in generation of the configuration files for the FPGA hardware utilizing the System Generator should not include native blocks from the Simulink library. Otherwise, the part of the model consisting of such blocks will be ignored.

The *MCode* block gives the opportunity to insert Matlab scripts into a model and use them in the FPGA design. Such instances as state machines can be implemented as the MCode blocks. Another interesting feature is the *Black Box.* With this block user

can import HDL code parts to the Simulink environment. In addition to this, major blocks of the thesis project are Black Boxes.

In the end of compilation process, the System Generator creates the ISE Design Suite compatible project, which includes configuration files such as HDL modules, constraints. This project can be used for simulation, design implementation in FPGAs or its evaluation using test benches.

3.3.2 Model description

The model built in Simulink using the Xilinx Blockset and the System Generator is an interpretation of the existing Xilinx ISE project for the custom-made eddy current sensor system. Main parts of the model are AD/DA transmit, USB connection and measurement control. Together these parts form a system that receives, processes signals from the sensor and transmits them to a computer.

The full model block diagram is shown in Fig. 26. As it was mentioned above, Black Box blocks were used as the basis for the model. The Black Boxes comprise HDL code parts from the existing ISE project. Nonetheless, some parts of this project were edited in order to improve modularity of the system. Descriptions of the signals and instances are presented in Table 6.

Table 6. Signals and instances descriptions [35, 36, 37].

Name	Description
Instances	
clk_management	Includes a clock input buffer (IBUFG), which is driven by the global clock pins.
measurement_control	Comprises a state machine with several stages of the measurement process: read FIFO, start measurement, AD conversion, USB data transmit. Changing of states affects several parameters.
clock_divider	Used to achieve 10 MHz clock signal from 50 MHz
reset_control	Generates reset signal for counters in the design

da_connection	Provides DA transmit mechanisms. In addition, includes Xilinx RAM core.
ad_connection	AD conversion part. External and internal AD converter signals are also generated.
usb_connection	Implements data transfer via USB. Designed as a state machine
Signals	
Input	
CLK_50M	Global clock signal of 50 MHz (sample period – 20 ns)
RXF_A ,RXF_B*	Do not read data from FIFO when high, data is available when low
TXE_A, TXE_B*	Do not write data from FIFO when high, data is available when low
ADC_SDO	Three-state serial data output. Each pair of output data words becomes two analog input channels when the previous conversion starts
Output	
RD_A, RD_B*	Enables the data byte from the current FIFO on D0…D7 pins. Gets the new value of byte from the receive FIFO when low goes to high
WR_A,WR_B*	Writes the data byte on D0…D7 pins in the transmit FIFO when WR changes from high to low
ADC_SCK	External clock input. Sequences output data on the rising edge
ADC_CONV	Starts conversion for two analog input signals on the rising edge
DAC_CLK	DA clock input
DAC_D (13 downto 0)	DA data bits
LED (3 downto 0)	A four bit value that changes according to the state of the state machine in the **measurement_control** instance
Bidirectional	
ADBUS, BDBUS (7 downto 0)*	Eight bit input/output ports for data interconnection.

* USB signals in 245 FIFO mode of the FT2232D USB to Serial chip (Channels A and B)

During the model development there were several design problems. One of them is the sample rates convergence issue. The problem was analyzed with *Block Icon Display* feature of the System Generator displaying sample rates on the Simulink diagram and solved by adding *Assert* block to the design. The block allows to instruct the system about sample rates values. Another issue was the following. The System Generator does not support combinational feedbacks. The solution which was used in the work is to add a delay block to feedback. Nevertheless, delay should be set as small as possible in order to provide same performance of the system. Internal Simulink blocks including Delay block from the Xilinx Blockset are supplied with separate clock signal. During the compilation process the System Generator handles this clock signal and afterwards it can be configured in Xilinx ISE project editing a user constraints file. Sample period was set to 2 ns.

Subsystems of the full model (AD/DA connections) are shown in APPENDICES 2 and 3.

3.3.3 Model evaluation

Xilinx ISE Design Suite project created with the System Generator from the Simulink model was evaluated using a test bench. For the purposes of simulations built-in simulator iSim was used. It is important to mention that iSim simulator can be used right in Simulink environment using iSim block from the Xilinx Blockset. The test bench was made for behavioral simulations in order to compare performances of the new and existing ISE projects. As it was noticed above, there is an internal clock signal for Simulink blocks. The sampling period was set to 2 ns. At the same time, the global sampling period is the 20 ns.

Performance comparison between two projects is presented in Fig. 27. It can be seen from signal shapes that models behave identically.

As it was mentioned above, Xilinx Spartan 3 family represents middle range chips, significantly complex designs can be implemented with high-end Virtex series. Nevertheless, Spartan 3 chip has enough performance to work with a wide range of applications. Resource overview of the Xilinx Spartan 3 xc3s1000-4ft256 chip is presented in Table 5. For the sake of comparison, resource consumption data for existing and rebuilt implementations are shown in Table 7.

Table 7. Resource consumption comparison.

Logic Utilization	**Available**	**Used, Existing implementation**	**Used, Rebuilt model with the System Generator**
Number of Slice Flip Flops	15360	130 (1 %)	146 (1 %)
Number of 4 input LUTs	15360	210 (1 %)	208 (1 %)
Number of occupied Slices	7680	151 (1 %)	193 (2 %)
Number of IOBs	173	47 (27 %)	49 (28 %)
Number of RAMB16s	24	14 (58 %)	14 (58 %)
Number of BUFGMUXs	8	6 (75 %)	6 (75 %)
Number of DCMs	4	2 (50 %)	2 (50 %)

As it can be seen, two implementations have comparatively same resource utilization values.

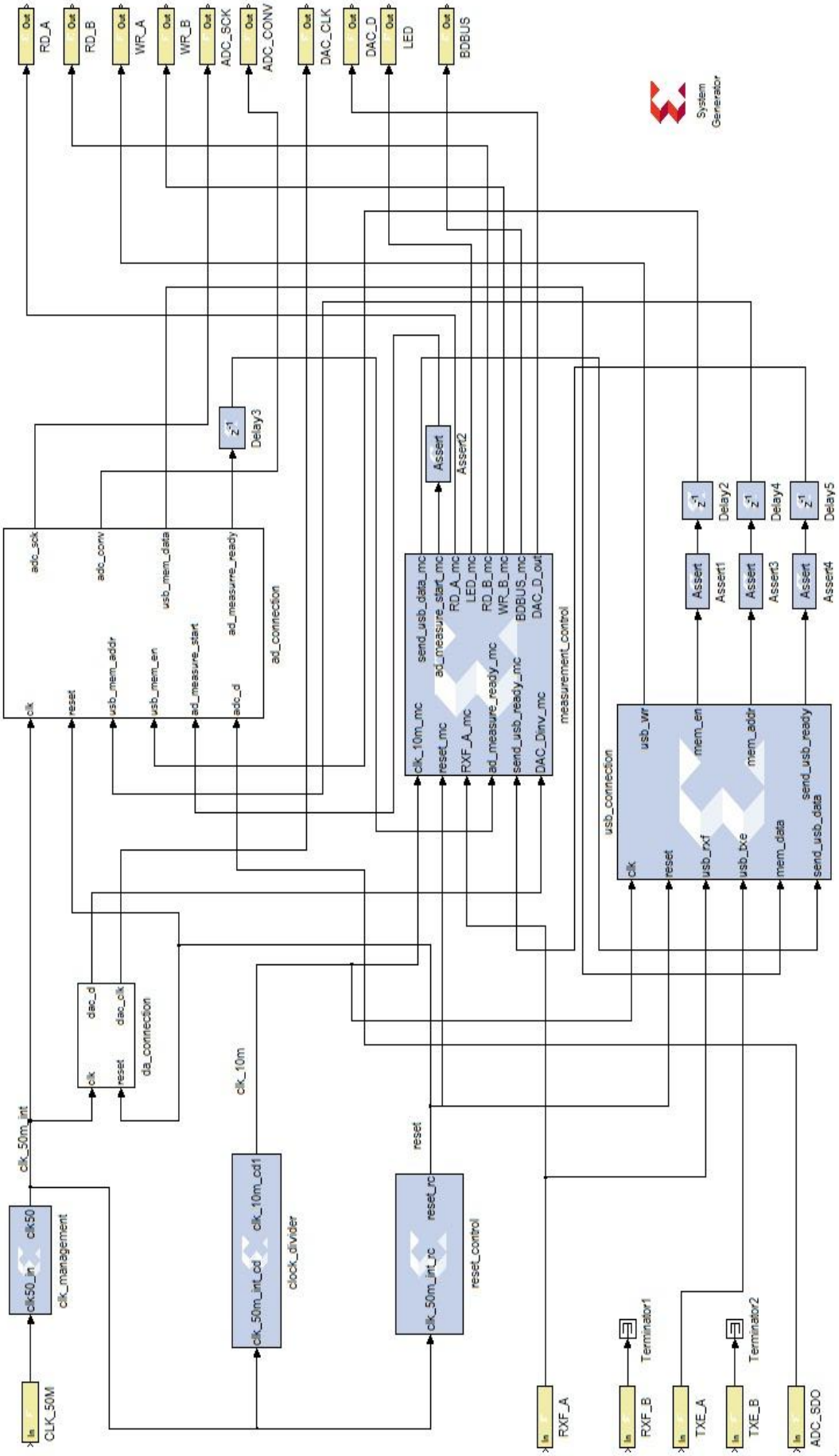

Fig. 26. Full Simulink block diagram of the model.

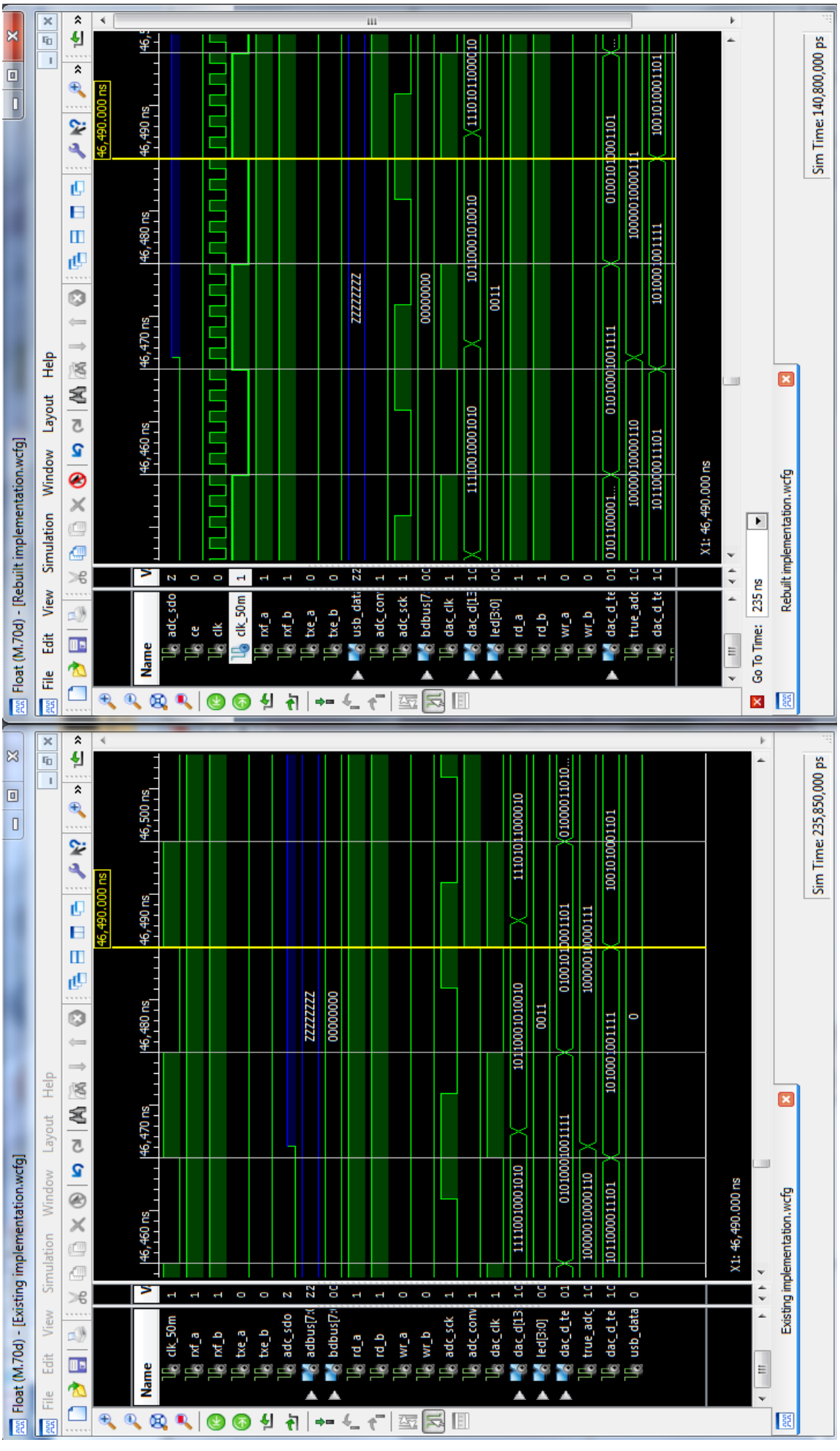

Fig. 27. iSim simulation comparison – existing model (left) and rebuilt model (right)

4 CONCLUSIONS

During the work the following results were achieved. Theoretical principles and basics of eddy currents, position measurements are considered. Special attention was paid to AMB systems, in which eddy current sensors are widely used. In addition, overview of existing and advanced technologies is included.

Industrial eddy current sensor system SKF CMSS 65 Eddy probe was evaluated under several operational modes. Firstly, it was revealed that adding a terminator to cables of measurement system does not affect performance substantially. Secondly, operation with different types of target materials was examined. Sample from the Saimaa University showed better results (improved linearity of the output signal as the function of distance) in comparison to aluminum and NiFe targets.

In the work the possibility to build a model for a FPGA device in Simulink environment using the Xilinx Blockset and System Generator was investigated. The new model showed the performance and resource consumption practically identical to the characteristics of the existing project. This fact opens new possibilities for easy system design and improvements, taking into consideration the fact that the System Generator gives the opportunity to implement configuration for a FPGA device decreasing resource and time consumption. Moreover, all necessary simulations can be done right in Simulink environment and it is not necessary for user to have deep skills of VHDL programming anymore.

Among the possible tasks of future studies can be the following:

- decomposition of the model to basic logic blocks, implementation of the design in the FPGA and testing it with a real system;
- implementation of the noise resistance and EMC mechanisms, operation in the vicinity of a drive;
- optimization of the custom sensor, its excitation frequency and implementation of faster ADCs and signal processing.

There are also such issues concerning the Simulink implementation as counters and state machines implementation, combinational feedbacks, clock signals handling, bidirectional ports and others.

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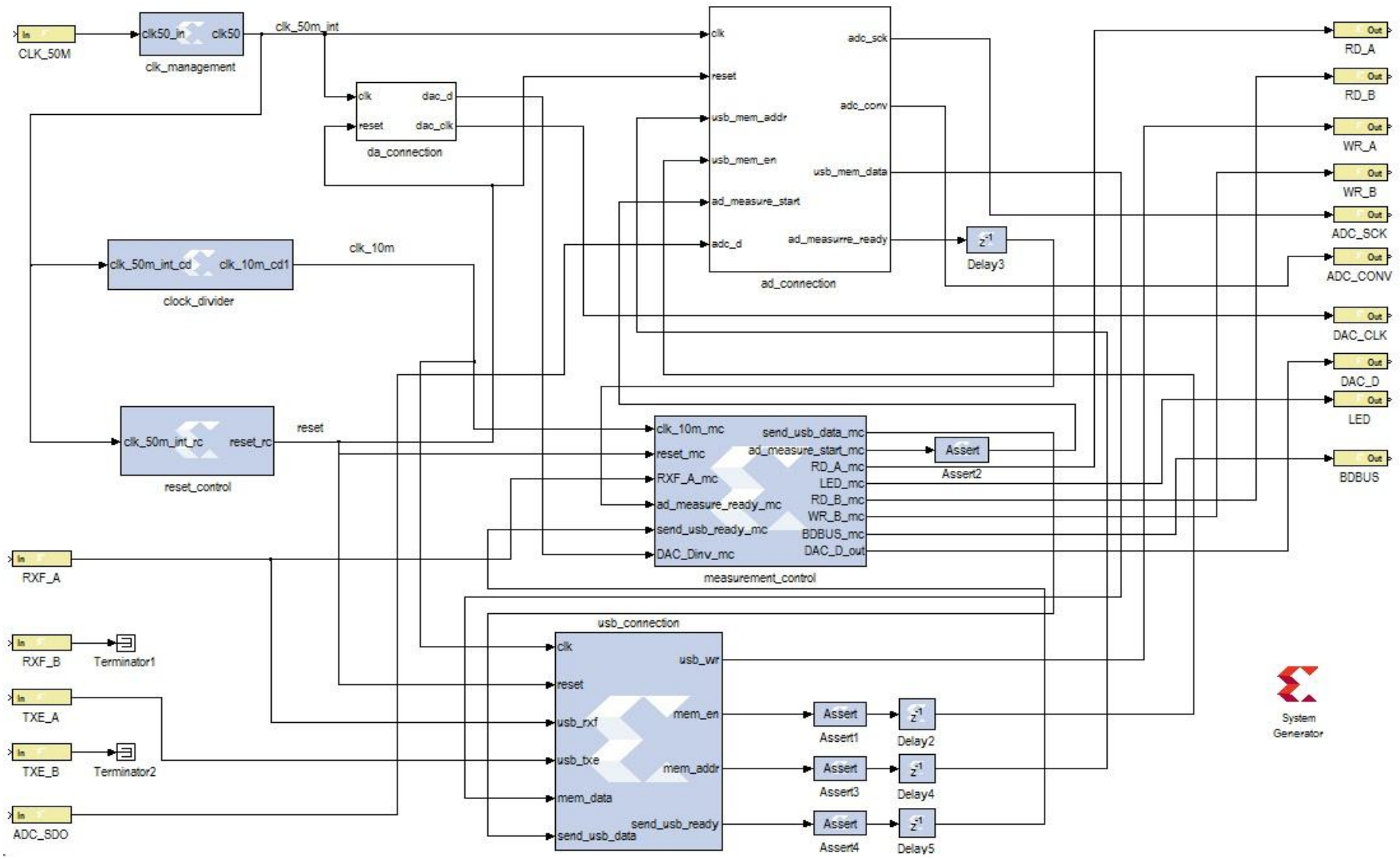
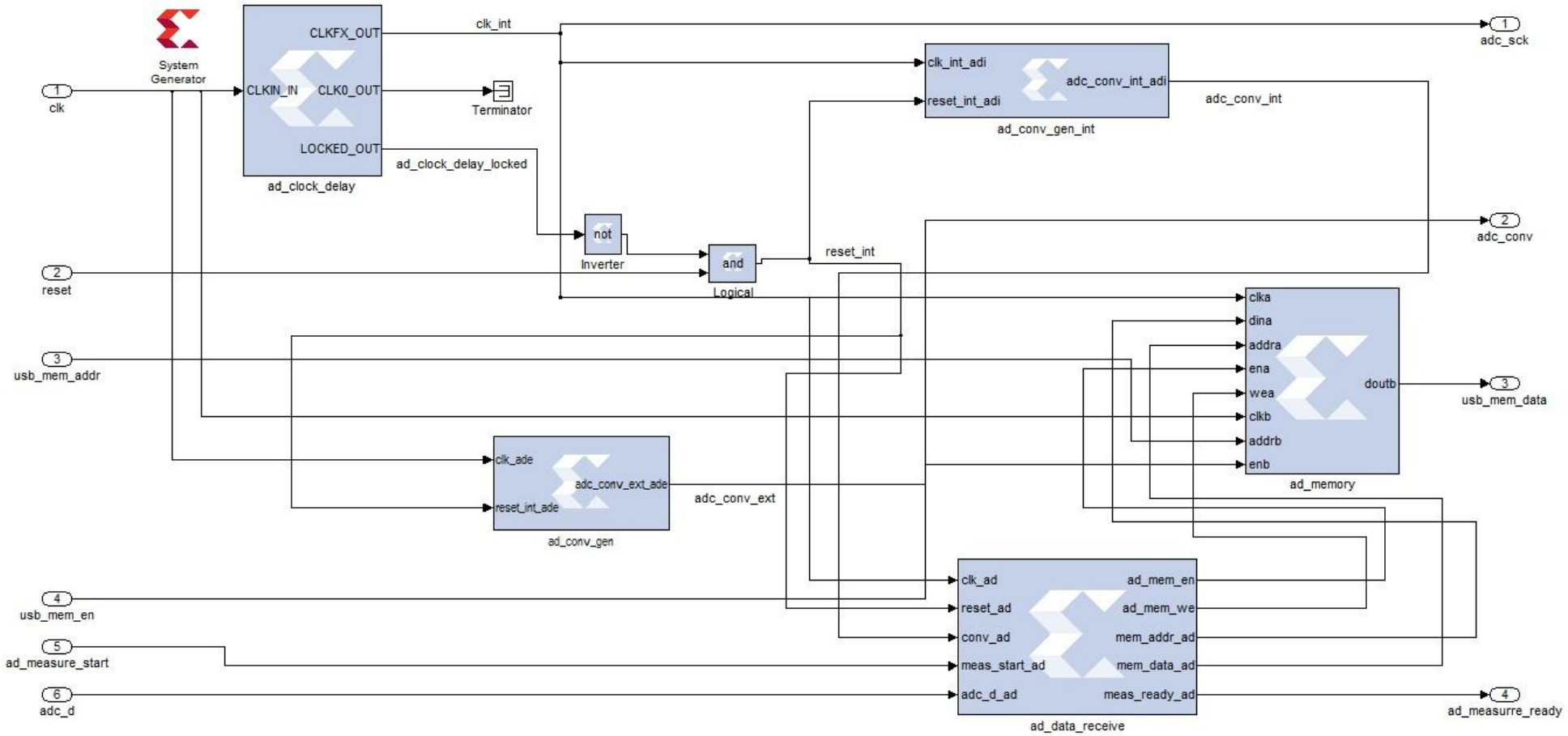
APPENDIX 1. Full Simulink block diagram of the model



APPENDIX 2. Simulink block diagram – ad-connection



APPENDIX 3. Simulink block diagram – da-connection