Lappeenranta
University of Technology

Mika Ikonen

POWER CYCLING LIFETIME ESTIMATION OF IGBT POWER MODULES BASED ON CHIP TEMPERATURE MODELING

Thesis for the degree of Doctor of Science (Technology) to be presented with due permission for public examination and criticism in the Auditorium 1382 at Lappeenranta University of Technology, Lappeenranta, Finland, on the 11th of December, 2012, at noon.

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Abstract

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In this doctoral thesis, methods to estimate the expected power cycling life of power semiconductor modules based on chip temperature modeling are developed. Frequency converters operate under dynamic loads in most electric drives. The varying loads cause thermal expansion and contraction, which stresses the internal boundaries between the material layers in the power module. Eventually, the stress wears out the semiconductor modules. The wear-out cannot be detected by traditional temperature or current measurements inside the frequency converter. Therefore, it is important to develop a method to predict the end of the converter lifetime.

The thesis concentrates on power-cycling-related failures of insulated gate bipolar transistors. Two types of power modules are discussed: a direct bonded copper (DBC) sandwich structure with and without a baseplate. Most common failure mechanisms are reviewed, and methods to improve the power cycling lifetime of the power modules are presented. Power cycling curves are determined for a module with a lead-free solder by accelerated power cycling tests. A lifetime model is selected and the parameters are updated based on the power cycling test results. According to the measurements, the factor of improvement in the power cycling lifetime of modern IGBT power modules is greater than 10 during the last decade. Also, it is noticed that a 10°C increase in the chip temperature cycle amplitude decreases the lifetime by 40%.

A thermal model for the chip temperature estimation is developed. The model is based on power loss estimation of the chip from the output current of the frequency converter. The model is verified with a purpose-built test equipment, which allows

simultaneous measurement and simulation of the chip temperature with an arbitrary load waveform. The measurement system is shown to be convenient for studying the thermal behavior of the chip. It is found that the thermal model has a 5°C accuracy in the temperature estimation.

The temperature cycles that the power semiconductor chip has experienced are counted by the rainflow algorithm. The counted cycles are compared with the experimentally verified power cycling curves to estimate the life consumption based on the mission profile of the drive. The methods are validated by the lifetime estimation of a power module in a direct-driven wind turbine. The estimated lifetime of the IGBT power module in a direct-driven wind turbine is 15 000 years, if the turbine is located in south-eastern Finland.

Keywords: Power cycling, lifetime, thermal model, IGBT, power module
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Lappeenranta, November 22, 2012
Mika Ikonen

Contents

Symbols and abbreviations

α	Curve fitting constant
β	Curve fitting constant
λ	Thermal conductivity
ρ	Density
τ	Thermal time constant
A	Curve fitting constant
A	Area
C	Capacitance
c	Specific heat capacitance
C_{th}	Thermal capacitance
$\cos\varphi$	Power factor
d	Thickness
ΔT_{j}	Chip temperature swing
$T_{\mathrm{j-c}}\,(t)$	Temperature difference chip-case
E_{a}	Activation energy
E_{sw}	Switching energy
f_{sw}	Switching frequency
I	Current
$i\,(t)$	Current
I_{c}	Collector current
k_{B}	Boltzmann constant
N_{f}	Power cycling lifetime
P	Power loss
P_{tot}	Total power losses
P_{cond}	Conduction losses
P_{sw}	Switching loss
Q	Activation energy
R	Resistance
$R\,(t)$	Reliability function
r_0	Collector-emitter resistance
R_{th}	Thermal resistance
$T_{\mathrm{c}}\,(t)$	Case temperature
$T_{\mathrm{j}}\,(t)$	Chip temperature
T_{m}	Medium chip temperature
U_{CE}	Collector-emitter voltage

u	Voltage
Z_{th}	Thermal impedance

ASIC	Application specific integrated circuit
AlN	Aluminum nitride
Al_2O_3	Aluminum oxide
AlSiC	Aluminum silicon carbide
CTE	Coefficient of thermal expansion
DBC	Direct bonded copper
DFIG	Double-fed induction generator
DUT	Device under test
GaAs	Gallium arsenide
GaN	Gallium nitride
IGBT	Insulated gate bipolar transistor
IMS	Insulated metal substrate
LC	Life consumption
MMC	Metal matrix composite
MOSFET	Metal oxide semiconductor field effect transistor
MTTF	Mean time to failure
NREL	National renewable energy laboratory
PCB	Printed circuit board
PLD	Programmable logic device
PMSG	Permanent magnet synchronous generator
SAM	Scanning acoustic microscope
SiC	Silicon carbide
TSP	Temperature-sensitive parameter
PWM	Pulse width modulation
PMSG	Permanent magnet synchronous generator

Chapter 1

Introduction

1.1 Background

The topic of this doctoral thesis is frequency converter reliability. A frequency converter is a power electronic application used to drive an electrical motor or feed electrical power to the grid. It transforms the qualities of alternative current; frequency, amplitude, and phase shift. Thus, it can be used to change the rotational speed and electrical torque of electrical motors. It also can be used to feed power from various sources to the grid.

The operation of a frequency converter is based on pulse width modulation (PWM). It allows to modify the shape of the output voltage by changing the width of the generated voltage pulses. The advantages of this are the controllability of the output voltage shape and reduced power losses in the hardware. A disadvantage is the increased complexity of the hardware and control methods. Nevertheless, since the PWM has been widely used in power electronic applications for a couple of decades, the basic control methods are easily available. The modulator algorithms and the output current control are an integral part of any PWM modulator. Only the application-specific control and communications to other devices and to the user are left for the designer.

Frequency converters are widely used in various areas, for instance in transport, energy generation and transfer, and industries. Frequency converters are used or could be used in almost any situation where an electrical motor is needed. They are typically used to replace more primitive speed control hardware such as adjustable transformers, chokes, and resistors. Common targets in everyday life are elevators, trains,

and subways. The elevator motor, for example, is driven by a frequency converter, which ensures that the elevator accelerates smoothly and stops on the right floor. Similarly, crane lifts in harbors are equipped with frequency converters. Among the most recent applications of frequency converters in transport are electrical scooters and trolling motors. The reduced losses in the control devices extend the driving range of these vehicles.

In electricity generation, the electricity for a light bulb may be produced for instance by a wind turbine, which applies converters to the generator control. Alternatively, the power may come from a neighboring country through a DC link, which, similarly, is driven by a converter. Again, in industrial applications, a conveyor belt speed can be accurately controlled by a frequency converter instead of an adjustable choke or a transformer. Equally, the fan speed of a high-power air conditioner or a water pump speed can be controlled by a frequency converter.

In addition to replacing control devices in existing applications, frequency converters allow the development of totally new applications. For example, the development of frequency converters has made it possible to use permanent magnet synchronous generators (PMSG) without gears in wind turbines. These are called direct-driven PM generators. Keeping the generator synchronized to the grid is difficult with traditional direct connections, since the wind speed and the produced mechanical torque vary rapidly, thereby changing the rotation speed. A frequency converter installed between the generator and the grid allows the generator to rotate freely, and still, the generated power is fed to the grid in synchronism.

Frequency converters provide several advancements over the previous control hardware in motor drives. Typically, the power losses in a choke or a resistor increase when the drive is operated below its nominal point. This is due to the fact that the more the power has to be reduced, the larger proportion of the voltage losses take place in the control device. In frequency converters, power losses in a certain operation point are typically lower compared with traditional control devices because of the characteristics of the PWM technology: the voltage loss over the device is small during conduction. Savings in energy can be significant.

A further advantage of frequency converters is the avoidance of friction in the control device. Moreover, unlike frequency converters, adjustable resistors and transformers include connections that have to be modified sometimes even during operation. The connection surfaces wear down and need regular maintenance. In frequency convert-

ers there are no contacts that have to be opened once the device has been installed, and thus, the need for maintenance is decreased. The above-mentioned properties of frequency converters provide flexibility to the speed and torque control of an electrical motor. The rotational speed can be changed smoothly, the response to load changes is quick, and the reliability and lifetime of the drive are increased. The reliability is increased even more in those applications where gears can be omitted. Gears are traditionally among the weakest points in any electrical drive.

There are four main elements in a frequency converter: a rectifier, a DC link, an inverter, and a control system as depicted in Figure 1.1.

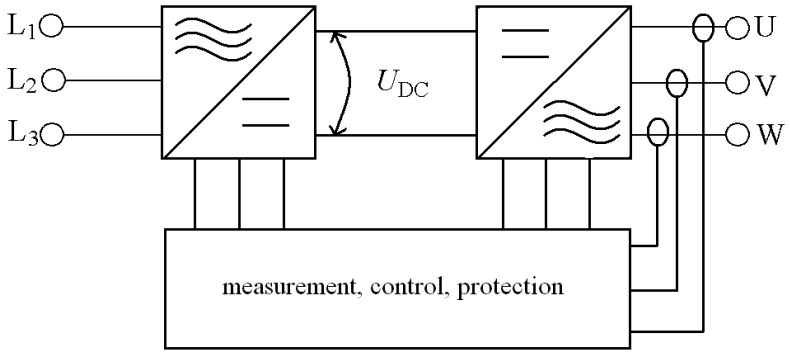

Figure 1.1: Elements of a frequency converter: a rectifier, a DC link, an inverter, and a control system.

It is common in small-power frequency converters that the rectifier and the inverter are integrated into one module, while in larger devices these are usually separated. In some cases, also the current and voltage sensors can be integrated into the power module. The structure of the rectifier is simpler with diodes, but on the other hand, the input waveform can only be controlled by controllable switches. This is the case in energy generation, where the voltage level or amplitude in the input can vary depending on the produced power. In addition, higher power can be drained from generators with an advanced control, which is not possible with diodes. The inverter part of the frequency converter is always made of controllable switches. In this doctoral thesis, it is always an insulated gate bipolar transistor (IGBT).

In addition to the semiconductor switches, which form the core of the converter, there is also a DC link, either a voltage or current one. A voltage DC link converter is used in this thesis, since it is widely used in the applications under study. The DC

link is made of large capacitors, which provide a path for the inductive currents in the rectifier and the inverter.

The fourth necessary element in a frequency converter is the control system. The control algorithms decide the next action based on the driving profile or external demand, output current measurement, and drive parameters given in the setup phase of the converter. The control gives a voltage reference to a modulator, which controls the voltage pulse widths formed by switching the IGBTs on and off. The external demand is acquired via a user interface, which can be as simple as a turnable knob or a complex system of local and remote computers in interaction with other devices on the grid. This means naturally that there are also communication buses on the converter.

The control system ensures that the output of the converter is in accordance with the demand. The control system can be based either on controlling the torque of the connected motor, or it can be just a control of the output frequency and current. It also keeps the converter hardware in safe operation both electrically and thermally. There are temperature measurements in the device, most often in the heat sink or in the power module. The temperature measurement of the actual semiconductor chips is seldom used, even though the chips are the most vulnerable part and generate the highest amount of heat.

The mechanical construction of the converter provides electrical, mechanical, and thermal connection to the larger system. It also provides, to some degree, protection against environmental factors such as moisture, dust, and electromagnetic interference. The mounting is separated from the bus bars for mechanical reliability and safety reasons. The large heat sink transfers the heat dissipated in semiconductor switches to air or liquid and away from the converter. The construction of the rest of the system should be open if the frequency converter is air cooled, because otherwise the ambient air heats up to an unacceptable level. On the other hand, liquid cooling is practical in sealed and high-power systems. Communication buses and connectors are also part of the mechanics of the converter.

1.2 Motivation for the work

The development of power electronic components and materials has led to the decreasing size per output power of the power modules. This has raised a problem

in the thermal management of the power modules, because extremely high power losses have to be dissipated through a very small area without increasing the chip temperature beyond the safe operation area. Usually, the power electronic chip temperatures are recommended to be kept below 125°C, 150°C, or 175°C. The problem can be tackled by a careful design of the device keeping in mind the nominal load and allowable overload operating points. However, the designer can only determine the margins for the absolute temperature. Now, the problem of aging remains because of the cyclic loading over time. The converter operates under dynamic loads in most electric drives. The varying loads cause thermal expansion and contraction, which stresses the internal boundaries between the material layers. Eventually, the stress wears out the semiconductor modules.

When a power module approaches the end of its lifetime, its electrical and thermal characteristics usually slowly deteriorate before a complete halt in operation. The voltage losses and therefore also the power losses increase, which further decreases the efficiency of the converter. Another consequence is that the thermal resistance increases over time thereby increasing the chip temperature. These gradual changes could be observed by specific measurement hardware and software, but in present converters changes are seldom observed, and consequently, the user only experiences an abrupt halt (Ciappa, 2002).

It is important to know when the service of the frequency converter is due. The optimum is to service the frequency converter just before the end of its life; too early maintenance means extra costs. On the other hand, if the service is delayed until the converter breaks down, extra costs may arise as a result of production losses or possible inconvenience or even danger to people. Frequency converters driving air conditioner motors in mines or road and subway tunnels are examples of critical applications where a breakdown of the frequency converter could even be life threatening in the worst case.

The wear-out can only be estimated by a model that takes into account the load profile or the mission profile. Wear-out cannot be detected by traditional temperature or current measurements inside the frequency converter. Therefore, it is important to develop a method to predict the end of the converter lifetime. The lifetime models are based on counting the cycles of the chip temperature during operation. The cycles are categorized according to their amplitude and mean temperature, which are depicted in Figure 1.2. The resolution by which the cycles are distributed depends on the user of the lifetime model. However, the accuracy of the temperature measurement, or

estimation if preferred, gives the lowest sensible resolution for the category.

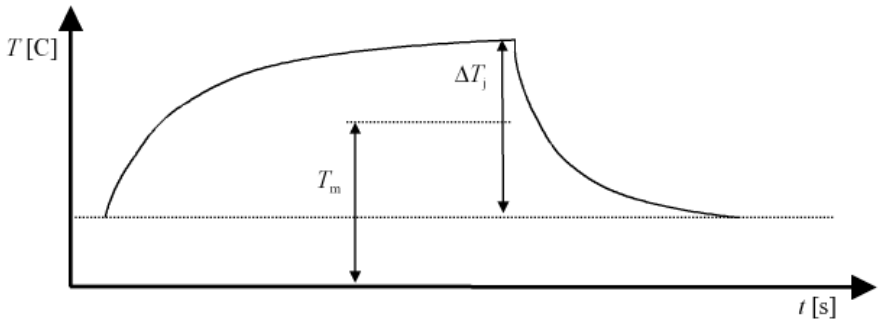

Figure 1.2: Temperature cycle. The temperature swing ΔT_j is the difference between the lowest and highest temperatures, while the mean temperature T_m is the midpoint value.

It depends on the application how many times each cycle type occurs. The frequency converter in a hybrid car experiences different mission profile from the frequency converter in a wind turbine.

There are thermal models desiged to work both in static and dynamic states, and there are models designed to estimate the end of life based on the output power profile, but usually, the models are intended for separate purposes, not to work as a single model. In the literature, the thermal modeling of frequency converters has been studied from the aspects of online temperature estimation and prediction of the converter lifetime (Blasko et al., 1999; Murdock et al., 2006; Musallam et al., 2004, 2008). However, the methods for lifetime prediction through thermal modeling have to be combined to work as a single package.

1.3 Scope of the work

The objective of the doctoral thesis is to develop methods to estimate the expected power cycling life of IGBT modules based on chip temperature modeling. The expected usage is estimated from the mission profile of the module by comparing it with the experimentally verified lifetime. The developed methods are validated by a power generation application, that is, a frequency converter of a direct-driven wind turbine.

The thesis concentrates on power-cycling-related failures of IGBTs. Two types of power modules are discussed: a direct bonded copper (DBC) sandwich structure with and without a baseplate. The DBC is a commonly used structure in power modules and has therefore been chosen for the study. The focus here is on the lifetime of the inverter side of a frequency converter.

To achieve the above targets, a thermal model of an IGBT chip is developed. The test equipment to verify the model is built. Next, the lifetime of a power module is determined by laboratory measurements, and the failure mechanisms are studied. A lifetime model and a method to count the cycles from the mission profile are selected. The selected methods with the thermal model are applied to define the lifetime of an IGBT power module in a direct-driven wind turbine to validate the methods.

1.4 Scientific contributions

The main contributions of this work are the following.

1. Development of a methodology for the thermal model verification in a frequency converter application.
2. Adaptation of the thermal model to be used in online power module lifetime estimation.
3. Demonstrating that the modeling methods for the power module lifetime are suitable also for the offline calculation of a wind turbine.
4. Updating the lifetime curves of power modules with a lead-free solder.

First, the methods and models available for lifetime estimation are studied in general. The most suitable model for the study is selected based on a wide use in industry. The power cycling lifetime of a power module is tested in laboratory, and the results are fitted to the selected lifetime model by tuning the model parameters. The laboratory tests showed that the selected model describes well the lifetime of the module.

Then, a thermal model for junction temperature calculation is constructed by estimating the power losses in the chips. This model is tested by simulations. The model is a ladder RC circuit, and its parameters are fine tuned for this specific application. It does not suffice to only consider the thermal parameters of the power module, but also the heat sink and the cooling system must be taken into account. It was shown that the model describes well the junction temperature in a static state, whereas

some improvements are required with the parameters with dynamic states.

A system for measuring the junction temperature is built and used to verify the thermal model in real time. The system makes it possible to both measure and simulate the junction temperature at the same time, and consequently, changes in the switching frequency and in loading of the module can be observed in real time. The system allows to measure only one IGBT of a frequency converter at a time, and therefore, the transverse thermal parameters are not taken into account in the study. Those include thermal resistance from chip to chip, from diode to IGBT, and from phase to phase.

It was also studied how the model could be implemented in a processor used in frequency converters. The processor handles all the numbers typically in a fixed point format instead of the floating point format used in digital signal processors. Therefore, a number of changes are required to the model in order for it to work accurately in programmable logic devices.

Last, the lifetime modeling methods were tested in off-line calculation of an IGBT power module in a wind turbine. An electrical and thermal models of a typical frequency converter of a direct-driven wind turbine were developed. The temperature cycles of an IGBT chip were calculated based on the turbine output power, and the cycles were compared against measured lifetime curves.

1.5 Outline of the thesis

The following chapters present the work carried out in this study.
In **Chapter 2**, the power module and temperature-related failure mechanisms are introduced.
In **Chapter 3**, a model for the chip temperature estimation is presented.
In **Chapter 4**, the module lifetime is estimated based on the thermal model.
Chapter 5 provides the conclusions of the work.

Chapter 2

Power modules

2.1 Introduction to Chapter 2

A power module consists of one or more semiconductor switches packaged together for easy connectivity. The module can be used to encapsulate thyristors, insulated gate bipolar transistors (IGBT), diodes, field effect transistors (FET), or similar semiconductor switches. Today, IGBTs are widely used because of their good switching performance combined with fairly low conduction losses Baliga et al. (1984). IGBT modules are studied in this doctoral thesis because IGBTs are usually used in frequency converters.

The module can comprise anything from a single switch to a full converter depending on both the required power rating and the package density. At low powers it is advantageous to pack the rectifier and the inverter into a single module with the brake chopper if needed. At higher currents, also the area of the chips increases so that in some point they have to be split up into individual modules. Then, the package may contain either a single chip or, as in some cases, a half bridge with antiparallel diodes.

Besides the easy connectivity, there are several other advantages in packaging up the semiconductor switches. Thermal management is handled with a low thermal resistance base plate construction together with an external heat sink. The chips can be placed close to each other, which is advantageous in balancing the chip behavior in parallel connection. The package also protects the chips from dust and moisture. These issues are addressed in detail in the next section.

In this chapter, the power module structure is examined. Then, the main failure

modes are presented. Last, latest development in the module structure addressing the failure modes is presented.

2.2 Power module structure

There are certain structural elements besides the semiconductor chips that form the power module. A rugged casing ensures appropriate mounting, electrical connection, insulation, and protection against environmental factors. A base made of a thin metal or ceramic composite produces a heat transfer path from the chip to the heat sink. The temperature of the module is monitored with a sensor installed inside. Last, the current-conducting circuitry is essential to transmit the gate signals and to conduct the currents.

The casing provides easy and reliable mechanical connectivity of the module. The enclosure is made of a plastic material, which provides electrical insulation for the chips. The cover with silica filling acts as a basic insulation against dust and water. Usually, however, the modules are not hermetically sealed. The package ensures a low-resistance electrical connection to the surrounding hardware.

There is a large variety of package types in the market. In conventional modules, the terminals for large currents are provided with busbars, while the control connections are made with pin contacts. Inside the module, the connections are soldered to the copper circuitry. Heat is conducted through a base plate, which also provides a rigid connection of the module to the heat sink with screws. In press pack modules, all the connections are replaced with spring pins. The module is mounted between the circuit board and the heat sink with a pressure plate, which tensions the pins ensuring good contact at both ends of the pins. One end contacts the internal circuit, while the other end contacts the external circuit board (Nicolai et al., 2000, pp. 90–91).

Semiconductor chips produce large amounts of heat as a result of conduction and switching losses. There is a need for a low thermal resistance path to keep the chip temperature within safe operating limits. Today, the maximum temperature of a power electronic chip is typically 150°C today, and the power losses are around a hundred watt per square centimeter. The power loss estimation is calculated based on Semitrans SKM100GB12T4 datasheet values with a 100 A load, power factor 1, modulation index 1, and the switching frequency of 3 kHz (Semikron, 2007). The heat is conducted to the heat sink through a base plate. In some module types, the

base plate is omitted, and the internal insulation layer is in direct contact with the heat sink.

The temperature of the module is monitored with a thermocouple placed inside the module. Usually, the base plate temperature is measured, since it reflects the chip temperatures depending on the load of the module. A direct measurement of the chip temperature is not practical, because a sensor attached on top of the IGBT chip ties the sensor to the emitter potential. The emitter potential changes quickly as a result of pulse width modulation. The high voltage of the emitter and the sensor causes a risk of a short circuit between the sensor wires and the rest of the internal circuitry and also between the sensor wires and the external hardware. The measurement electronics should be sophisticated enough to handle the rapidly changing potential of the sensor and to include galvanic isolation.

The circuitry inside the module is constructed either with a copper layer or a printed circuit board, depending on the structure. In the direct bonded copper (DBC) substrate, the circuitry is etched to one of the copper layers. The chips are soldered on the copper, while the other sides of the chips are connected with bond wires. In some sintered modules, the bond wires are replaced by a plastic circuit board. The current paths are optimized for low electrical resistance and inductance.

2.2.1 Direct bonded copper substrate

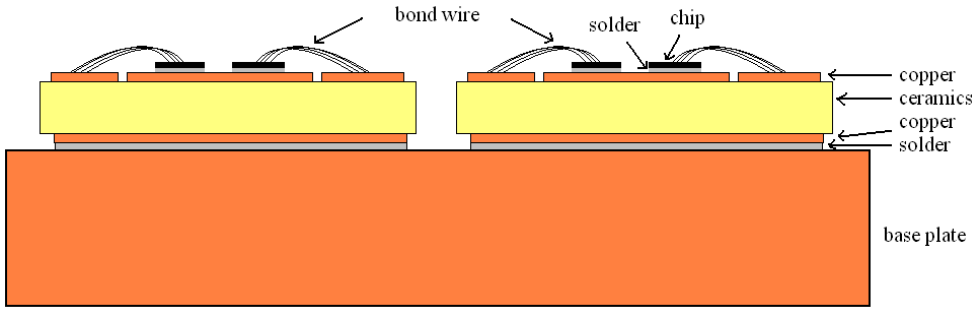

Figure 2.1: Two direct bonded copper sandwiches on a common base plate.

In the DBC sandwich structure, presented in Figure 2.1, a copper layer is bonded directly to a ceramic substrate. The ceramic substrate is typically made of aluminum oxide (Al_2O_3) or aluminum nitride (AlN). The upper copper layer is the current-conducting circuitry and has a pattern according to the module layout, while the

lower copper layer is plain. Both layers spread the heat laterally to decrease the thermal resistance of the module. Bonding the copper directly to the ceramics decreases the coefficient of thermal expansion (CTE) of the copper layer allowing better match of the copper and silicon dies. Otherwise, the large thermal expansion of the copper would cause the solder layer to degrade during temperature cycling. A wide copper area can also cause ruptures on the ceramic layer because of a high tension caused by differences in the CTE. This can be prevented by adding substances to the ceramic, which stop the rupture from progressing. The effective thickness of the copper can also be reduced by etching holes on the copper in the border regions (Schulz-Harder and Exel, 2003).

One or more DBCs are soldered to a common base plate depending on the area of the module. The larger the area of a single DBC is, the higher the thermal stress to the solder layer is. Paralleling DBCs on a common base plate improves the module reliability by decreasing the bending stresses of the DBC (Fusaro, 1996). Therefore, in higher-power modules, the DBC is divided into smaller DBCs, which are individually soldered to the base plate. The base plate, typically made of copper, provides mechanical support for the DBCs and spreads the heat flow in the horizontal direction.

Modules without a base plate are also available. The number of DBCs is limited to one in such modules, which limits the maximum power. The heat sink design is more critical as it now contributes to even larger part of the total thermal resistance. In liquid-cooled heat sinks, the liquid tunnels have to be placed accurately under the chip because the heat does not spread horizontally. Paralleling the chips decreases the thermal resistance thereby decreasing the thermal stress especially in modules without a base plate (Scheuermann and Lutz, 1999).

The chips are soldered to the copper layer so that the solder layer forms the collector connection of the IGBT and the cathode connection of the diode. On top of the chip there is an aluminum metalization layer on the emitter and gate contacts. Several parallel bond wires are bonded to these metalizations by an ultrasonic bonding process (Ramminger et al., 1998; Hager, 2000). The bond wires are usually made of at least 99.9 % pure aluminum (Ramminger et al., 1998), but lately, also copper bond wires have been studied (Guth et al., 2010). The other ends of the bond wires are bonded to the copper layer. The wires and busbars coming from the terminal connections are also soldered on the copper.

2.3 Degradation mechanisms

Materials expand with a rising temperature and contract with a decreasing temperature. The expansion is described by a temperature expansion coefficient CTE, which is a material-dependent parameter. Thermal parameters of the most common materials of power modules are shown in Figure 2.2. The expansion produces stress in the material interfaces inside the module. These interfaces are: 1) the bonding between the chip metalization and the bond wire, 2) the solder layer between the chip and the DBC, and 3) the solder layer between the DBC and the base plate. The stress is usually cyclic as a result of the load cycles, which causes the interface to weaken over time.

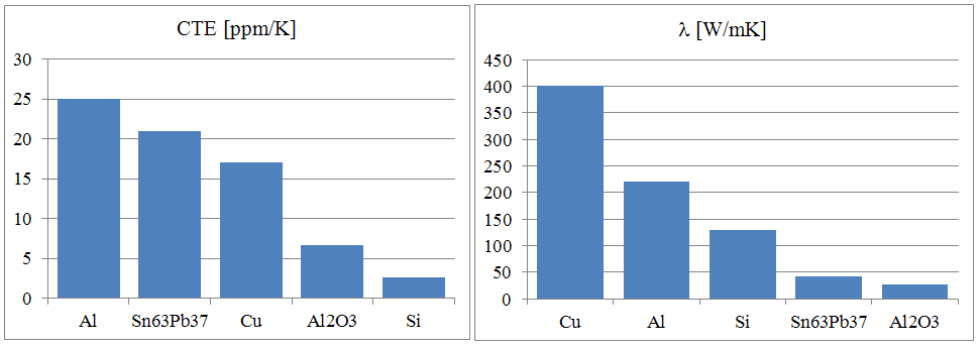

Figure 2.2: Coefficient of thermal expansion and thermal conductivity λ of the most commonly used materials in power modules (Mitic et al., 2000).

The coefficient of thermal expansion for aluminum is one order of magnitude higher than for silicon, 25 ppm/K and 2.6 ppm/K, respectively. The aluminum metalization on top of the chip and on the bonding wires expands ten times more than the silicon exerting a high stress on the bonding of the emitter wire. Also the CTE of silicon is lower than the overall CTE of the DBC leading to a high stress on the solder joint between the chip and the DBC.

One failure mechanism can speed up the other failure mechanism; for example, solder layer delamination increases the chip temperature thereby leading to a sooner bond wire lift-off. The bond wire lift-off is dominant at higher temperature swings, while solder fatigue is dominant at lower temperatures. The limit value where the dominant mechanism changes depends on the solder material and on the wire bond reliability, with a lead-tin eutectic solder being around 80°C to 100°C (Morozumi

et al., 2003).

2.3.1 Bond wire lift-off

The aluminum metalization layer on top of the chip reconstructs during power cycling, if the local temperature exceeds 110°C. The reconstruction is due to plastic stress relaxation of the aluminum. This roughens the aluminum layer and reduces the effective cross-section of the metalization, which leads to an increase in the collector-emitter voltage U_{CE} (Ciappa, 2002). An increased U_{CE} means increased power losses in the aluminum layer, which accelerates the bond wire lift-off by increasing the chip surface temperature.

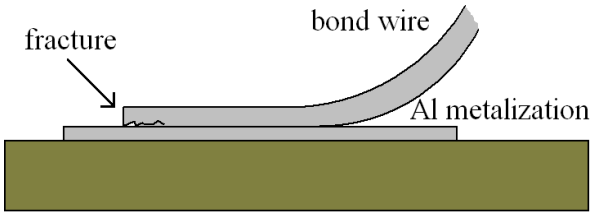

Figure 2.3: Bond wire lift-off starts along the boundary between the aluminum metalization and the bond wire.

The bond wire lift-off is initiated by a stress caused by the thermal expansion of the bond wire and the chip. The stress results in a rupture in the bonding, and the rupture starts to progress laterally, finally causing the bond wire to lift off. The bond wire lift-off is demonstrated in Figure 2.3 and the revealed footprint on the aluminum metalization layer is shown in Figure 2.4. The bond wire lift-off can be prevented by coating the bond with an organic coating material, but this leads to heel cracking (Ciappa, 2002). There is no room for the bonding to move, so the stress concentrates on the heel of the bonding.

If one emitter bond wire lifts off, the current distribution on the emitter is altered; more current is conducted by the remaining bond wires. The same applies to the gate bond wires, although the gate contact is made with a smaller number of bonds. However, the research usually focuses on the emitter bond wires. This accelerates the lift-off of the remaining bond wires in two ways: as a result of the uneven current distribution in the chip, more power loss is developed in the area of the remaining bond wires causing a higher thermal stress, and the overall U_{CE} is increased thereby

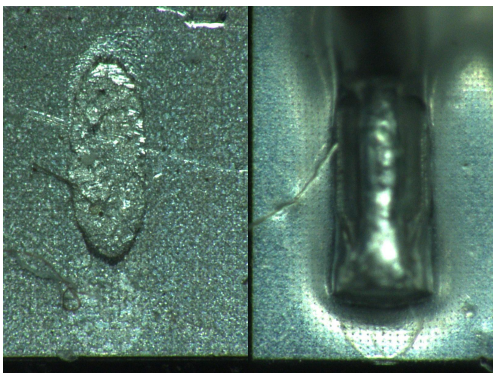

Figure 2.4: Bond wire has lifted off after the power cycling test, revealing the contact surface along which the aluminum has fractured. The aluminum metalization has also deformed. The power module was cycled with a temperature swing $\Delta T_\mathrm{j} = 100°\mathrm{C}$ for 40 700 cycles.

increasing the overall power losses. This leads to a higher stress on the remaining bondings.

2.3.2 Solder layer fatigue

Several intermetallic layers are formed when a chip is soldered on top of the DBC substrate. Closest to the DBC is a layer rich with copper. Layers rich with tin and lead are formed in the middle of the solder layer. The grain sizes of these layers become coarser during thermal cycling and thus become weaker. The layer rich with copper is the weakest. The solder layer experiences cyclic shear stress caused by temperature swings and differences in the thermal expansion rates between the joined materials. As demonstrated in Figure 2.5, horizontal cracks in the solder layer usually initiate in the corner region and progress towards the center in the layer rich with copper (Herr et al., 1997; Ciappa, 2002).

Crack initiation on the edges can be seen in a scanning acoustic microscope image in Figure 2.6. The module was cycled with $\Delta T_\mathrm{j} = 80°\mathrm{C}$ and the medium junction temperature $T_\mathrm{m} = 95°\mathrm{C}$. The fatigued solder layer can be identified by a pale area on the corners.

Solder degradation increases the thermal resistance of the module causing the chip temperature to rise. A higher chip temperature accelerates the aluminum recon-

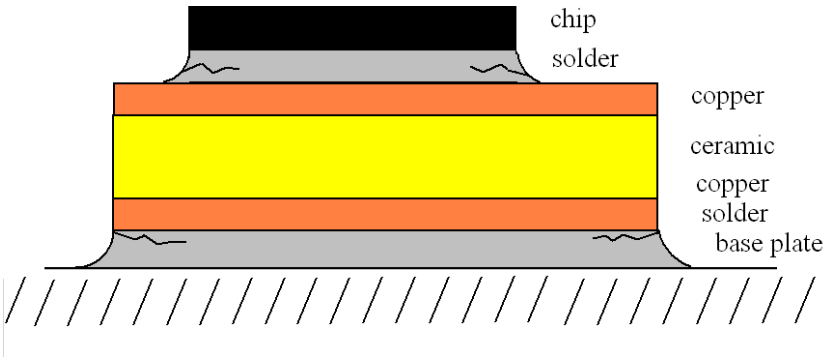

Figure 2.5: Cracks in the solder layer initiate on the edges and propagate towards the center of the solder.

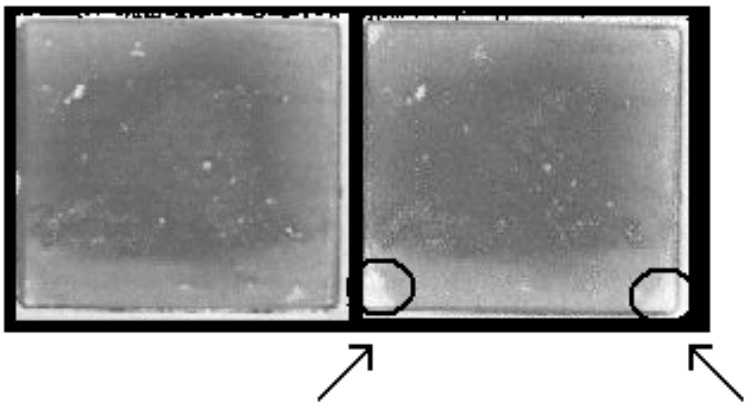

Figure 2.6: Scanning acoustic microscope image of a solder layer between the DBC and the base plate before (left) and after (right) a power cycling test. The solder layer has fatigued, and the degradation has started as can be seen from the white areas on the corners. The module was cycled 86 000 times with $\Delta T_\mathrm{j} = 80°\mathrm{C}$.

struction on top of the chip thereby accelerating the bond wire lift-off. The degraded solder layer between the chip and the substrate increases the collector-emitter voltage U_{CE} further increasing the power losses and the chip temperature.

The solder layer between the substrate and the base plate is the weakest in those modules where a base plate is used. This is due to the fact that the difference in the thermal expansion of the joined materials is at highest, along with the largest diameter of the joint (Ciappa, 2002).

2.3.3 Other mechanisms

There are also other mechanisms that are not directly related to the bonding or the solder layer. The ceramics may crack as a result of the residual stress originating from the assembly process, and especially because of the stress from the soldering of the ceramic to the base plate (Romero et al., 1995; Ciappa, 2001). Assembling the power module to the heat sink causes bending stress because the base plate is prebent (Ciappa, 2001). The bending stress can be reduced by using multiple ceramics on a common base plate (Fusaro, 1996).

The heat paste between the module and the heat sink is drifting away because of the cyclic bending of the base plate. This is also evident in the chip temperature in the power cycling test: initially, the chip temperature increases as a result of the increasing thermal resistance in the interface between the module and the heat sink. As soon as the thermal paste is spread evenly, the surplus paste is extruded, and the thermal resistance settles. This can be seen in Figure 2.7, where the chip temperatures and collector-emitter voltages of a half bridge module during power cycling are presented. In the test, a power module type SKM145GB123D was cycled with a temperature swing $\Delta T_{\mathrm{j}} = 100°\mathrm{C}$. If the vertical movement of the base plate is too large during cycling, which may be the case for example if the mounting screws are loosened, the paste may extrude too much. In that case, the thermal resistance from the module to the heat sink increases thereby accelerating the module wear.

2.4 Improvements in the module structure

Over the recent decade, the power module structure has been improved in several ways. The main focus has been on using materials that have coefficients of thermal expansion (CTE) close to each other in operation temperature to minimize the effect

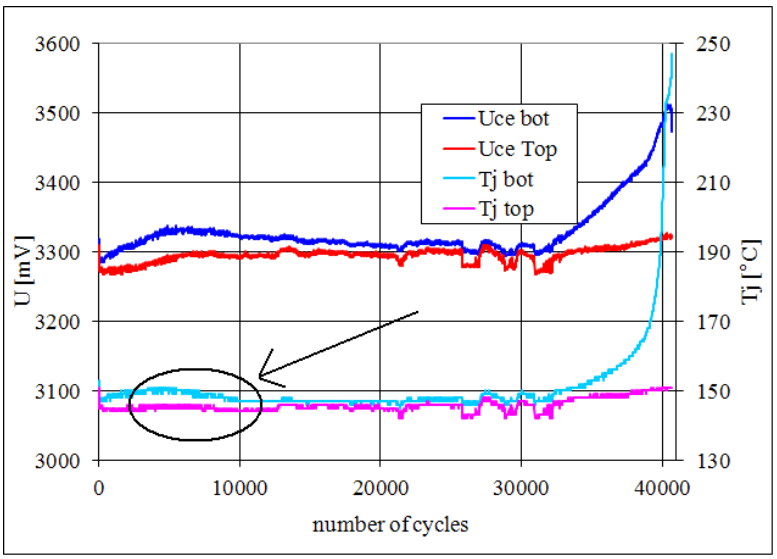

Figure 2.7: Thermal paste extrudes between the module and the heat sink during power cycling. This can be seen in the chip temperature also. After some cycles, the surplus paste is extruded and the chip temperature settles. The power module was cycled with a temperature swing $\Delta T_\mathrm{j} = 100°\mathrm{C}$ for 40 700 cycles.

of thermal stress. The base plate can be replaced with an aluminum silicon carbide (AlSiC) metal matrix composite (MMC), which has an expansion coefficient close to that of the Al_2O_3 substrate, 7 ppm/K and 6.7 ppm/K, respectively. In some cases, the aluminum oxide is replaced by aluminum nitride (AlN) as the substrate material, the coefficient of thermal expansion of which is 4.5 ppm/K (Mitic et al., 1999, 2000). By this technique, the lower copper layer and the solder layer connecting the DBC substrate to the base plate are omitted. Aluminum silicon carbide has a lower thermal conductivity (200 W/mK) than copper (400 W/mK), but on the other hand, it is also a more rigid material allowing to manufacture thinner base plates (Romero et al., 1995). The thermal parameters of the new materials are compared with the parameters of traditional materials in Figure 2.8. An aluminum silicon carbide base plate and an aluminum nitride substrate are used for example by Fuji in the traction modules (Yamamoto et al., 2012).

An insulated metal substrate (IMS) can be used instead of the DBC substrate. The ceramic layer is insulated from the base plate with an adhesive polymer layer instead of a solder layer (He et al., 1999). As a consequence, the lower copper layer and the solder layer are omitted resulting in a better reliability.

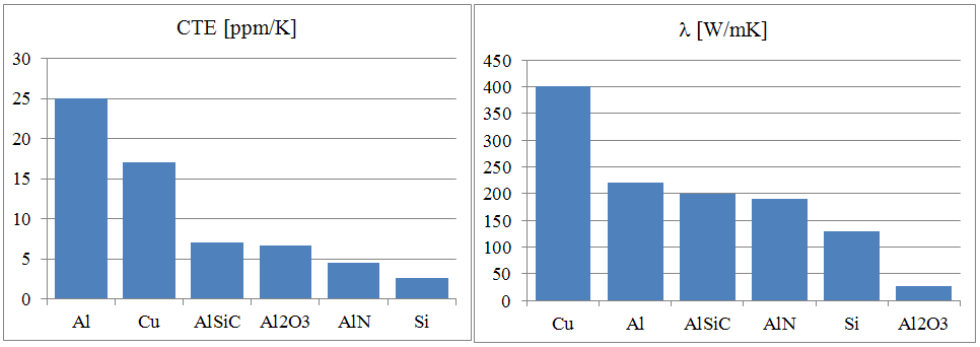

Figure 2.8: Coefficient of thermal expansion and thermal conductivity λ of new materials in power modules in comparison with traditional materials (Mitic et al., 2000).

Chip materials having less conduction losses and a higher operating temperature have been studied. These wide band gap materials are for example silicon carbide (SiC), gallium arsenide (GaAs), and gallium nitride (GaN), just to mention but a few (Elasser et al., 2003; Khan et al., 2005). A high chip temperature provides more margin for the thermal behavior of the power module and the heat sink. So far, the large-scale commercial use of these materials has been hindered by their higher price. Silicon carbide diodes are used in special applications, where the low losses and high speed weigh more than their higher price.

Other techniques have aimed at improving the bonding for example by coating of the bond foot or by bonding the wire to a molybdenum strain buffer (Hamidi et al., 1999, 2001). Bond foot coating glues the foot into its place even if the foot otherwise lifted off. The molybdenum buffer layer evens out the differences in the CTE of the chip and the aluminum and reduces the stress caused by thermal expansion. The aluminum wires can be replaced with copper wires (Siepe et al., 2010). The coefficient of thermal expansion of silicon is closer to the CTE of copper than the CTE of aluminum resulting in a reduced thermal stress. The aluminum metalization layer on top of the chip is replaced by a stack with copper on top.

2.4.1 Lead-free solder

The solder layer has been under development for many years. In some studies, glue has been used instead of solder, or it has been replaced with sintering (Rusanen and Lenkkeri, 1995; Eisele et al., 2007; Amro et al., 2006). The solder material has been

changed from a eutectic tin-lead alloy to a lead-free one because of initiatives around the world to reduce the use of lead.

In Europe, the "Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment 2002/95/EC", abbreviated RoHS, came into force at the beginning of July 2006 (EC, 2003). It bans the use of lead in new equipment which are have come to market in the EU after July 2006. Thus, new lead-free alloys have been developed to be used in new models of the power modules. The basic alloy is tin-silver with a small fraction of copper, from 0.5 to 0.7%. Adding copper to the alloy decreases the melting temperature compared with a pure tin-silver alloy (Ma et al., 2006). The melting point of the lead-free alloy is higher (around 220°C) compared with the conventional lead-based alloy (188°C), allowing higher values for the maximum chip temperatures (Huff et al., 2004). The melting points and thermal conductivities of the conventional tin-lead and the new tin-silver alloys are compared in Figure 2.9.

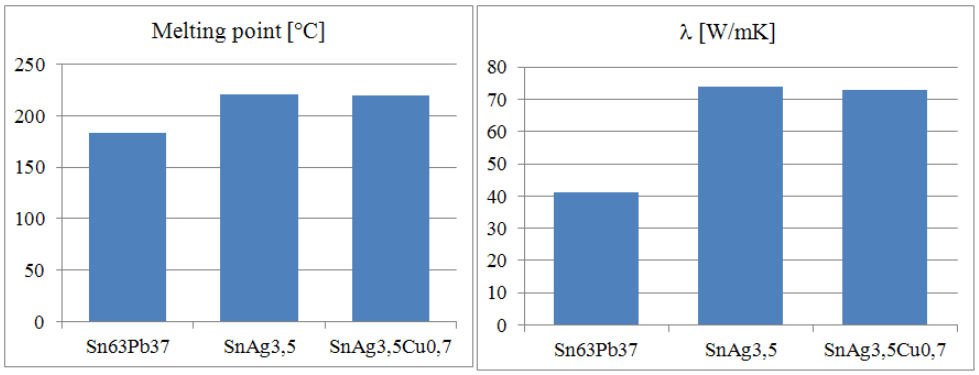

Figure 2.9: Melting temperatures and thermal conductivities of tin-lead and lead-free solder alloys (Kehoe and Crean, 1998; Stinson-Bagby et al., 2004).

Figure 2.9 shows also that the thermal conductivity is higher for lead-free alloys. The electrical conductivity of the solder depends on the reflow time, and thus, the values of different studies cannot be compared directly as such (Kang et al., 2002).

Morozumi et al. (2003) studied four lead-free alloys all containing 3.5% silver. Three of the alloys contained additional materials, which the authors do not disclose. According to their measurements, the yield strength of the lead-free solder is 38–57 MPa depending on the alloying element, which is 1.3 to 2.4 times as high as that of the tin-lead solder (22 MPa). They found that the failure behavior of the lead-free solder

differs from that of the tin-lead solder. With the tin-lead solder, the power cycling lifetime of a module depends on the solder at lower temperature swings, and on the wire bonding at higher temperature swings. With the lead-free solder, however, the situation is quite the opposite: the lifetime depends on the wire bonding at lower temperature swings. This is due to the higher lifetime of the solder.

Morozumi et al. (2003) also found that the failure mechanism of the lead-free solder joint is different to that of the tin-lead solder. The solder started to crack from the center of the solder whereas the tin-lead solder cracked from the edges. It was found that the crack starts at the grain boundaries of tin, accelerated by coarsening of the grain size under thermal stress. Morozumi et al. (2003) do not reveal the exact alloys they used, and hence, it is left to argue whether their results are valid in all cases with a lead-free solder, since the mechanical properties of the alloy depend heavily on the alloying elements.

Altogether, the power cycling lifetime of power modules with a lead-free solder is found to be 7 to 16 times as high as that of modules with a tin-lead solder (Morozumi et al., 2003).

2.4.2 Silver sintering

One of the major recent improvements from the power cycling reliability point of view is the replacement of the solder joints with sintered silver layers, also referred to as diffusion welding. The surfaces to be joined are first metalized with noble metal, usually silver or gold. Then, silver flakes are applied to the joint, and the module is kept under pressure of 40 MPa at a 240°C temperature from one to three minutes (Schwarzbauer and Kuhnert, 1991; Amro et al., 2005). Silver sintering is usually applied to the connection between the chip and the DBC, but it can also be applied to join a flexible foil on the chips instead the bonding wires (Steger, 2011).

The melting point of the silver layer is much higher (960°C) compared with the melting temperature of a lead-free solder (220°C). It enables the use of chips with high operating temperatures. The heat conductivity of the silver layer is also much higher, 250 W/mK compared with 70 W/mK of the lead-free solder (Amro et al., 2005; Göbl and Faltenbacher, 2010).

Amro et al. (2005) studied the lifetime of modules with sintered silver joints. They used both one-sided and two-sided sintering. In the one-sided sintering, the chip is

joined to the substrate with sintered silver, whereas in the two-sided joining also the bond wires are sintered. With a high temperature swing ΔT_j 130 K, Amro et al. (2005) discovered the module with the one-sided sintered joint to have 20 times as high lifetime as that of a module with soldered joints. With the two-sided sintering, the lifetime increased to 40 times. In their study, the bond wire lift-off was the failure mode. Amro et al. (2005) concluded that because only by changing the solder joint to the sintered joint, the lifetime increased even with high temperature swings, the bond wire lift-off is a consequence of the solder layer degradation. Goebl and Faltenbacher also achieved an increase in the module power cycling lifetime by sintering the chips to the substrate (Göbl and Faltenbacher, 2010). According to their tests, the module lifetime increased threefold. This is not as good improvement as Amro et al. (2005) found.

Because the wire bonding is the limiting factor of the power cycling lifetime in modules with sintered joints, the wire bonding has been developed further or replaced with other solutions. Siepe et al. (2010) used copper wires and chip metalization with a copper surface instead of aluminum. They reached 1 million cycles at a temperature swing ΔT_j of 130 K. This is more than ten times the results of Amro et al., obtained with 66 000 cycles at a similar temperature swing. Steger (2011) replaced the aluminum bond wire with a flexible circuit board, which is sintered directly on top of the chip to form the power connections. Based on the tests he made, the power cycling lifetime with the sintering technology was 500 000 cycles at a temperature swing of 110 K.

Sintering is not a new invention, but it was proposed as a joining technique for power semiconductor devices already in the early 1990s (Schwarzbauer and Kuhnert, 1991). High material costs caused by the use of silver, incompatibleness with the soldering process flow, and the demanding process parameters such as a high pressure hindered the use of sintering for long (Guth et al., 2010).

2.5 Modules studied in this work

Three different kinds of modules are used in this work. All of them are made by a DBC sandwich technology, because at the moment, most of the modules in the field are still based on that particular technology. Semikron modules were chosen because they are easily available, widely used, and they represent a technology that is applied by several manufacturers.

The first module type is a MiniSKiiP without a base plate, 32NAB12T1. A three-phase rectifier, an inverter, and a brake chopper are all integrated into one module. The terminal connections are equipped with spring contacts by attaching the module between the heat sink and the circuit board with a pressure plate. The nominal current of the module is 50 A, and the blocking voltage of the chips is 1200 V. There is a temperature sensitive resistor inside the module.

The second module type is a Semitrans with a base plate, SKM145GB123D. It is a half-bridge module consisting of two IGBTs and two free-wheeling diodes. The terminal connections are equipped with screws for the high current and pins for the gate signals. The module is mounted to the heat sink with screws. The nominal current of the module is 100 A, and the blocking voltage of the chips is 1200 V. The module lacks a temperature sensor. It is modified from a regular production version by replacing the solder between the DBC and the base plate with a lead-free alloy.

The SkiiP module used in wind turbine lifetime calculations is a 2403GB172-4DW integrated power system with a base plate and a liquid-cooled heat sink. It is a half-bridge module consisting of four parallel connected modules. The nominal current is 2400 A, and the blocking voltage is 1700 V.

2.6 Summary

A power module provides mounting and electrical connection for the power semiconductors. It can contain any number of chips from one switch to a full converter. The basic structure of the module is based on a sandwich, where copper is laminated on both sides of a ceramic layer. The sandwich is either soldered to a base plate or mounted directly to a heat sink. The chips are soldered to the sandwich, while the top connections of the chips are implemented with bond wires.

The solder layers and the bonding of the wires are the most vulnerable parts to degradation due to the stress from power – or thermal – cycling. The degradation rate depends on the cycle amplitude and the mean value. Thus, the power cycling lifetime can be increased either by reducing the cycles or by improving the solder layers and the bonding.

The module structure is being developed to improve the weak parts of the module.

The module materials are chosen to perform optimally together from the thermal expansion point of view. The solder layers are replaced with stronger silver sintering, while the bond wires are either omitted with sintered connections or the aluminum wires are replaced by copper wires.

Chapter 3

Modeling of the chip temperature

3.1 Introduction to Chapter 3

There are generally two reasons to observe the IGBT chip temperature online: one is the aspiration to reach smaller tolerances in the thermal design, the other is the effort to estimate the remaining power cycling lifetime of the module. The temperature can either be measured directly or estimated by a temperature model.

It is important to know the thermal behavior of the IGBT module in various load conditions to ensure safe operation at all times. There is a specified maximum temperature for an IGBT chip that cannot be exceeded without changes in the functionality of the device. The thermal dimensioning made in the design phase of a frequency converter should leave some safety margin in the heat transfer capacity because of variations in the thermal parameters of the power modules. The device must also be capable of temporary overloading in normal use. In practice, the safety margin is provided by oversizing the heat sink and cooling capacity, which increases the manufacturing costs of the device.

The thermal parameters of the power modules and of the whole system are required for accurate thermal dimensioning. In static loading, only the thermal resistances are taken into account, and the modeling is straightforward. In dynamical loading instead, also the thermal capacitances must be taken into account. This leads to temperature simulations with different load scenarios.

The safety margins can be reduced by observing the chip temperature online. The observation can be based on temperature measurement or online temperature estimation. Taking into account the objective to make the devices as cost-effective as possible, additional costs of the measurement sensor and the required peripheral electronics are not desirable. Temperature estimation, on the other hand, does not require any additional components, but is dependent on accurate thermal and loss models. If the chip temperature is estimated in real time, the thermal load of the chip can be temporarily reduced for example by reducing the switching frequency.

Another important application of the chip temperature estimation is associated with the power module reliability improvement. The power cycling lifetime depends on the amplitude of the chip temperature swing ΔT_j and the mean junction temperature T_m. If the chip temperature is observed online, the cycles can be counted and the remaining power cycling lifetime can be estimated. The lifetime estimation can be made by models that need the information about the chip temperature behavior.

When there are several chips in parallel forming one IGBT or diode, the average temperature is being measured. In practice, it is the hottest chip that is the most important one because a higher mean temperature T_m means a shorter lifetime. However, it suffices to measure the average temperature of the paralleled chips, since the lifetime model is calibrated with respect to that. A failure of one chip can be seen in the increased resistance and the temperature of the IGBT in any case, and thus, it is not necessary to observe the paralleled chips separately to find the highest junction temperature.

In Chapter 2, the structure and failure modes of a power module were examined. In this chapter, the chip temperature measurement and modeling are presented. Two alternative ways to measure the chip temperature, a thermocouple measurement and a temperature-sensitive parameter measurement, are examined. Then, a thermal model for a single chip is derived. A system for the model verification is constructed by applying the chip temperature measurement. Last, the system is used to verify a thermal model of an IGBT chip.

3.1.1 Literature survey

Hefner (1994) coupled an electrical model with a thermal model for an IGBT chip. The IGBT chip was packed into a TO247 package. The simulations were made on Saber. Blasko et al. (1999) derived the third-order thermal model parameters from

the data sheet. The model was also implemented in a microcontroller. The model is used to protect the devices from overtemperature by reducing the power losses by decreasing the switching frequency if necessary. As a last resort, also the load current can be decreased.

Krümmer et al. (1999) modeled a step-down converter and implemented the model in a microcontroller. They verified the model with an infrared camera using opened modules. The power losses were tabulated as a function of load current and chip temperature. The calculated temperature was within two degrees of the measured temperature in the dynamic state. The largest error was with the small thermal time constants, where the dynamics of the infrared camera is not sufficient. The thermal parameters were measured, but in the verification process the module was opened, thus changing the thermal behavior of the system, as is noticed by Kruemmer.

Musallam et al. (2004) implemented a real-time thermal model in a digital signal processor (DSP). The model was verified by a MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) device and by a chip temperature measurement using a temperature-sensitive parameter measurement. The parameters were based on material parameters. The forward voltage of the body diode was measured with a small measurement current. They achieved a good estimation of the static temperature, whereas the dynamic temperature estimation had some error.

Khatir et al. (2004) demonstrated that it is possible to estimate the junction temperatures of a multichip power module in real time in operating conditions. They used an AC converter with glycol water cooling, and junction and case temperature measurements in a test bench reproducing a real mission profile of a hybrid car. The profile was taken from the EU directive 98/69/EC (1998), which is used in the emission control of combustion engines. Optical thermocouples with a response time of 25 ms were used for the chip temperature measurements, while thermocouples were used for the baseplate temperature measurements.

Hirschmann et al. (2005) have also modeled the chip temperature in the case of a hybrid car with a mission profile FTP-72, which is a city driving profile defined by the US Environmental Protection Agency. They made a state-space simulation of a Cauer network. They found that the semiconductors experience large temperature cycles leading to a short lifetime.

Murdock et al. (2006) modeled the junction temperature of an IGBT to prevent

overtemperature. Temperature estimation was used in the feedback loop to control the switching frequency to regulate the losses in order to increase the power cycling reliability of the module.

Krah and Klarenbach (2010) implemented a thermal model in a field-programmable gate array (FPGA) circuit. They estimated the conduction power losses with a linear function without temperature dependency. The switching losses were also estimated without temperature dependency. The thermal model is based on a Foster ladder with parameter values from the module data sheet.

Profumo et al. (1999) modeled the chip temperatures in multichip power modules with a thermal impedance matrix. The coupling impedances between each chip were the elements of the matrix. The chip temperature was calculated with a convolution integral using a fast Fourier transform. They applied the method to a diode package where two diodes were connected in one module in series. The comparison between the measured and simulated temperature with a current surge proved the method suitable for chip temperature estimation. Khatir et al. (2004) also used a thermal impedance matrix in their chip temperature estimation in the case of a hybrid car. The thermal impedance matrix is especially useful in low-speed operation, where a single chip temperature estimation may give up to 30°C error (Wei et al., 2006).

James et al. (2008) applied the thermal impedance matrix to model the chip temperature in a system with varying thermal parameters of the heat sink resulting from fan speed changes. In their study, the heat sink was air cooled and the fan speed was changeable. The results show good agreement between the measured and estimated temperatures at a low power, but an increasing error at a high power. This is due to the fact that also the thermal parameters of the module change when the heat sink thermal impedance changes.

All the above mentioned studied show the efforts made in the chip temperature estimation in various applications. There are many similarities in the methods of thermal modeling; the model is based on power loss estimation and the temperature is calculated with a ladder circuit or with finite element modeling. The aim of the studies is to provide a tool to protect the semiconductor chips from overtemperature. However, these studies generally focus on only one thing at a time, either it is the power loss modeling, the temperature modeling, or the model verification. They seldom take into account the whole picture in one single study. Especially the accuracy requirement for the thermal model is frequently put aside. The accuracy requirement,

however, is an important factor in the accurate power cycling lifetime estimation.

3.2 Temperature measurement techniques

There are various ways to measure the temperature of an IGBT chip. These include thermocouple measurement, temperature-sensitive parameter (TSP) measurement, infrared imaging, and optical thermocouples (Khatir et al., 2004; Wernicke et al., 2007), just to mention a few. In this thesis, the two first ones are used. The thermocouple measurement is used in thermal model verification, while the TSP measurement is used in power cycling tests.

The term 'chip temperature' is vague, because there are temperature differences inside and on the chip (Shaukatullah and Claassen, 2003). In this doctoral thesis, the chip temperature refers to the average chip temperature, but in the case of a thermocouple measurement, it refers to the temperature in the measurement point at the surface of the chip. On the other hand, temperature-sensitive parameters measure the average temperature of the chip (Blackburn, 2004).

3.2.1 Thermocouple measurement

A thermocouple is made of two wires of different metals. Their Seebeck coefficients differ from each other resulting in a voltage, which is dependent on the temperature and on the materials. For example, a K-type thermocouple is made of nickel-chromium and nickel-aluminum wires, and the Seebeck voltage is in the range of 40 μV/K. The wires are joined together in the measurement point, which is called the measurement junction. The other ends of the wires are joined to the signal processing equipment, and these junctions together form the reference junction, assuming that the junctions are in the same temperature. There will be a potential difference between the junctions, when the junctions are at different temperatures. Hence, the thermocouple measures the temperature difference between the measurement junction and the reference junction. The temperature of the reference junction must be either at a constant temperature, or it must be measured constantly. The constant temperature can be achieved by placing the reference junction for example in 0°C water. 0°C water is easily available, only water and ice are needed. A thermocouple with a reference junction is presented in Figure 3.1.

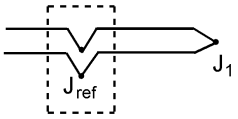

Figure 3.1: Thermocouple, where J_1 is the measurement junction and J_{ref} is the reference junction.

There are some problems involved in measuring the temperature with a thermocouple. The attachment method influences the thermal resistance from the device under test (DUT) to the thermocouple; for instance, gluing imposes a higher thermal resistance than soldering (Shaukatullah and Claassen, 2003). The thermocouple has also some thermal capacitance, which causes delay in the heat transfer from the object to the thermocouple (Wernicke et al., 2007). Thus, measuring a fast-changing temperature gives inaccurate results if the mass of the thermocouple is large.

The small output voltage level of the thermocouple and the poor galvanic contact to the DUT makes it vulnerable to electromagnetic-induced interference. This can be avoided if the thermocouple is properly tied to a predefined potential, for example to the emitter potential of the IGBT, but this, on the other hand, causes serious safety problems. A short circuit may occur if the thermocouple wires are damaged or if they are connected to the measurement equipment carelessly. The electrical insulation of the measurement equipment also has to be done with care. In an inverter, the potential of the emitter can be hundreds of volts compared with the ground level, and thus, the common-mode potential of the measurement equipment must be floating.

The wires of the thermocouple must run through the case of the module, which requires a hole to the casing. Although the modules are not hermetically sealed, drilling a hole to the module casing allows dust and moisture to get inside the module. Again, the sensor wires present a risk for a short circuit if they are cut for any reason.

The thermocouple always requires a reference junction with a known temperature, because it measures the temperature *difference* between two points. Ideally, this reference junction would be at 0°C to get accurate results. The temperature of the reference junction can vary arbitrarily, if only the temperature is also being measured.

Another temperature-related aspect in the thermocouple measurement is the temperature dependency of the Seebeck coefficient, which causes nonlinearity in the measurement. The nonlinearity can be compensated in the measurement software

using standard tables for the coefficient. Those charts are available for example from the ITS-90 thermocouple database provided by the National Institute of Standards and Technology (NIST).

There is a special kind of a thermocouple called an intrinsic thermocouple, which is formed by welding both wires separately to the DUT (Tszeng and Saraf, 2003). This requires both the junctions to be in the same temperature and the wires to be welded to the same material. The thermal resistance and the thermal capacitance are notably lower in this kind of a thermocouple, but the manufacturing is more difficult. Performing a temperature measurement of the IGBT chip temperature with an intrinsic thermocouple would mean welding the wires to the thin aluminum layer on top of the IGBT chip.

Generally speaking, with the current technology, the temperature measurement with a thermocouple is sensible only in laboratory conditions, since it requires mechanical contact with the object. The wires of the thermocouple are run through the module case, which is not desirable in most cases. Furthermore, the module must be customized to accommodate the thermocouple measurement.

3.2.2 Temperature-sensitive parameter measurement

Some electrical parameters of the IGBT change with temperature, including the gate-emitter threshold voltage, collector-emitter saturation voltage, and collector-emitter resistance. By keeping the other parameters, such as the collector current, constant, it is possible to determine the junction temperature by measuring any of the above-mentioned temperature-sensitive parameters (TSP).

Let us have a closer look at the chip temperature by the collector-emitter saturation voltage U_{CE} measurement. It is possible to derive the temperature from this voltage by keeping the collector current and the gate voltage constant with every measurement. The forward characteristics of an IGBT of SKiiP 32NAB12T1 (Semikron, 2001) is shown in Figure 3.2 with two temperatures, 25°C and 125°C.

First, the voltage must be calibrated with respect to the junction temperature to obtain the relation between the voltage and the temperature. This is usually done by heating the module externally and then measuring the temperature and the voltage with a calibration current, which is usually in the range of hundreds of milliamperes. The current must be low enough not to heat the device. The collector-emitter voltage

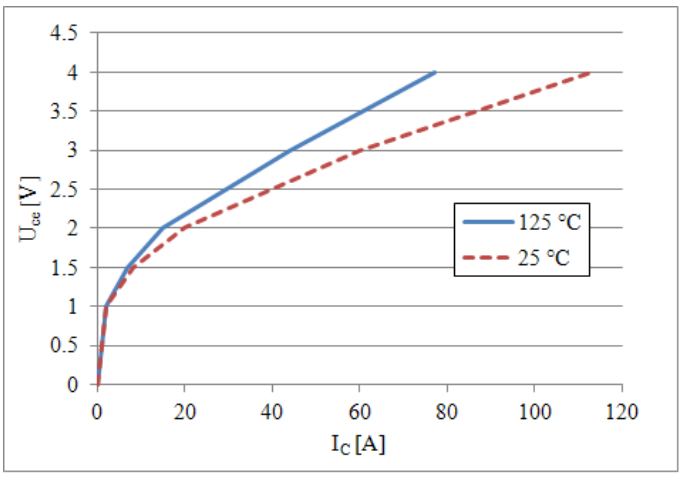

Figure 3.2: Temperature dependency of the forward characteristics of an IGBT according to the datasheet (Semikron, 2001).

dependency on temperature is characterized with coefficient k, unit [V/K] or [mV/K]. The voltage-temperature dependency is described as

$$U_{\mathrm{CE}} = U_{\mathrm{CE}(0)} + k \cdot \Delta T_{\mathrm{j}}, \tag{3.1}$$

where $U_{\mathrm{ce}(0)}$ is the collector-emitter voltage at 0°C and ΔT_{j} is in degrees Kelvin. The junction temperature is then

$$T_{\mathrm{j}} = \frac{U_{\mathrm{CE}} - U_{\mathrm{CE}(0)}}{k}. \tag{3.2}$$

There are some drawbacks in this system: the temperature of the whole module is assumed to be equal during the calibration so that the junction temperature is actually measured by measuring the temperature of the module case. Another drawback is that after the calibration, the temperature can be measured only with the calibration current (Wernicke et al., 2007).

Another option is to calibrate the collector-emitter voltage U_{CE} with respect to the junction temperature and the load current, and to keep only the gate voltage constant. In the calibration phase, the junction temperature is still measured with a thermocouple. The voltage must be measured with several temperature/current combinations. The change in the voltage is in the range of some millivolts per degree of Kelvin (Martin et al., 2000), while the overall collector-emitter saturation voltage

is in the range of a few volts. In an inverter application, the common-mode voltage of the top IGBT of each half bridge can be hundreds of volts when the IGBT is turned off. The measurement equipment must withstand a high voltage and be able to measure small signals. In practice, the measurement must be synchronized to ON-state of the IGBT.

3.3 Thermal model

Despite the increased use of multichip modules and the modeling methods to estimate the chip temperature in those modules, single-chip temperature estimation is still needed in high-power inverters, where each phase is implemented with a dedicated module with several paralleled chips. Thus, the effect of neighboring chips on the chip temperature is less significant even in low-speed operation, since each chip is driving the same current in synchronism.

A temperature estimation model was constructed, which calculates the temperature difference from the junction to the case $T_{\mathrm{j-c}}(t)$, demonstrated in Figure 3.3.

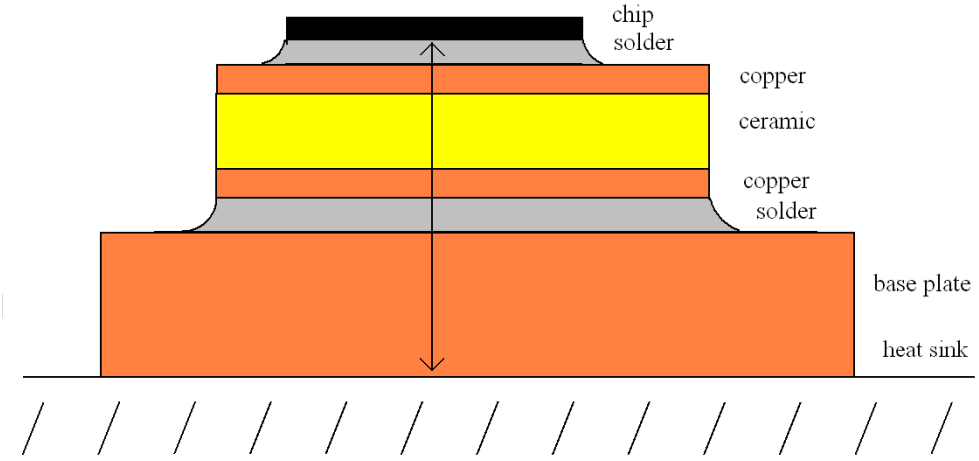

Figure 3.3: Temperature from the chip to the case $T_{\mathrm{j-c}}(t)$ is estimated with a thermal model.

The temperature model estimates the temperature difference based on the power losses of the chip in question. The power losses are estimated from the output current

and the data sheet parameters. The instantaneous junction temperature $T_\mathrm{j}(t)$ is

$$T_\mathrm{j}(t) = T_\mathrm{j-c}(t) + T_\mathrm{c}(t), \tag{3.3}$$

where $T_\mathrm{j-c}(t)$ is the estimated temperature difference and $T_\mathrm{c}(t)$ is the measured case temperature. The temperature difference $T_\mathrm{j-c}(t)$ between the chip and the reference point can be calculated by

$$T_\mathrm{j-c}(t) = P(t) \cdot Z_\mathrm{th}(t) \tag{3.4}$$

where $Z_\mathrm{th}(t)$ is the thermal impedance from the junction to the case [K/W] and $P(t)$ is the heat flux or power loss [W].

To take into account the effect of the junction temperature on the power losses, the junction temperature estimate is fed back to the power loss estimations. The top-level flow chart is presented in Figure 3.4.

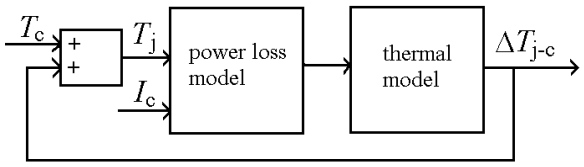

Figure 3.4: Temperature model consists of a power loss model and a temperature model. The case temperature $T_\mathrm{c}(t)$ and the collector current I_c are the measured inputs, and the junction-to-case temperature $T_\mathrm{j-c}(t)$ is the output of the model.

3.3.1 Power losses

The losses can be expressed as conduction P_cond, switching P_sw, and driving losses. The driving losses are mainly produced in the driver circuit and in the gate resistance, and therefore, their contribution to the chip temperature is minor; they are thus excluded from the temperature model. Thus, the total power loss is

$$P_\mathrm{tot} = P_\mathrm{cond} + P_\mathrm{sw}. \tag{3.5}$$

Conduction losses depend on the on-state resistance r of the chip and on the collector current i. Also the collector-emitter threshold voltage $U_\mathrm{CE,0}$ contributes to the losses

(Blaabjerg et al., 1996):

$$P_{\text{cond}} = \frac{1}{T} \int_0^T \left(\left(U_{\text{CE},0} + r \cdot i\,(t)^{\beta} \right) \cdot i\,(t) \right) dt, \tag{3.6}$$

where β is a curve fitting constant.
Conduction losses with temperature dependency are (Blaabjerg et al., 1996)

$$P_{\text{cond}} = \frac{1}{T} \int_0^T \left(C_1 \cdot T_{\text{j}} + U_0 + (C_2 \cdot T_{\text{j}} + r_0) \cdot i\,(t)^{\beta} \right) \cdot i\,(t)\, dt, \tag{3.7}$$

where C_1 and C_2 are the temperature coefficients and r_0 is the collector-emitter resistance at the starting temperature.

The momentary loss at the switching on or switching off can be high compared with the conduction losses. This is due to the high voltage over the switch while the current is flowing. However, the switching loss occurs only for a short period of time, and hence, the average switching loss P_{sw} is dependent on the switching frequency f_{sw}

$$P_{\text{sw}} = E_{\text{sw}} \cdot f_{\text{sw}}, \tag{3.8}$$

where E_{sw} is the switching energy, that is the energy wich is converter to heat during the switching.
The switching energy for one switching is the integral of the collector-emitter voltage times the collector current over the duration of the switching.

$$E_{\text{sw}} = \int_0^t \left(u_{\text{CE}}\,(t) \cdot i_{\text{C}}\,(t) \right) \cdot dt \tag{3.9}$$

The switching energy dependent on the DC link voltage and the junction temperature in hard switching can be estimated by Equation (Blaabjerg et al., 1996)

$$E_{\text{sw}} = A \cdot i\,(t)^{\beta} \cdot \left(\frac{U_{\text{DC}}}{U_{\text{base}}} \right)^{C} \cdot \left(\frac{T_{\text{j}}}{T_{\text{base}}} \right)^{D} \tag{3.10}$$

where A is dependent on the gate resistance and the chip characteristics, U_{base} is the base value for the DC link voltage, T_{base} is the base value for the junction temperature, and β, C and D are curve fitting constants. The curve fitting constants are determined with measurements after the base values are chosen.

In practice, modeling of the switching losses can be carried out based on the table from the data sheet values. This way, there is no need for parameter fitting. The

collector current I_{C} is the input, and the switching energy is the output

$$E_{\mathrm{sw}} = f\left(I_{\mathrm{C}}\right) \tag{3.11}$$

3.3.2 Dynamic temperature modeling

Junction temperature in a first-order circuit can be calculated with an equivalent electronic RC circuit with a current source. The electric current corresponds to the power loss, the voltage of the resistor corresponds to the temperature difference $T_{\mathrm{j-c}}\left(t\right)$, the electrical capacitance C to the thermal capacitance C_{th}, and the electrical resistance R to the thermal resistance R_{th}. The equivalent circuit is presented in Figure 3.5.

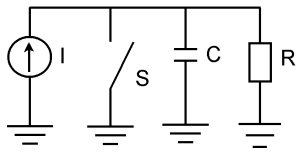

Figure 3.5: First-order RC circuit with a current source.

The step response of the circuit can be analyzed by current equations. The switch S is opened at the time $t = 0$, and the current starts flowing through the resistor and the capacitor. Since there is no inductance in the circuit, the current rises instantly to the value defined by the constant current source. The current divides between the capacitor and the resistor according to the voltage over the RC circuit.

$$C\frac{\mathrm{d}u}{\mathrm{d}t} + \frac{u}{R} = I. \tag{3.12}$$

This differential equation can be solved with respect to the voltage $u(t)$ according to Adams (1995)

$$u\left(t\right) = e^{-\mu(t)} \int_0^t e^{\mu(t)} q\left(t\right) dt, \tag{3.13}$$

where

$$q\left(t\right) = 0 \tag{3.14}$$

and

$$\mu\left(t\right) = \int_0^t \frac{1}{RC} dt. \tag{3.15}$$

Solving this, we get the voltage $u(t)$

$$u\left(t\right) = Ce^{-\frac{t}{RC}}. \tag{3.16}$$

This is the time-dependent component u_t of the voltage. The steady-state component of the voltage is $u_\mathrm{s} = RI$. At the time $t = 0$, the voltage u is zero:

$$u = u_\mathrm{s} + u_\mathrm{t} = RI + C = 0. \tag{3.17}$$

From this we can solve C

$$C = -RI \tag{3.18}$$

and we obtain for the voltage $u = u(t)$ for any given time t

$$u(t) = u_\mathrm{s} + u_\mathrm{t} \tag{3.19}$$

$$\Rightarrow u(t) = RI + (-RI)\, e^{-\frac{t}{RC}}$$

$$\Rightarrow u(t) = RI\left(1 - e^{-\frac{t}{RC}}\right). \tag{3.20}$$

Now, using the thermal notations and denoting the time constant τ

$$\tau = R_\mathrm{th} \cdot C_\mathrm{th} \tag{3.21}$$

we get the temperature difference $T_{\mathrm{j-c}}(t)$ for the power P

$$T_{\mathrm{j-c}}(t) = R_\mathrm{th} P\left(1 - e^{\frac{t}{\tau}}\right) \tag{3.22}$$

or the thermal impedance Z_th as a function of time

$$Z_\mathrm{th}(t) = R_\mathrm{th}\left(1 - e^{\frac{t}{\tau}}\right). \tag{3.23}$$

This is the step response of the system. The thermal capacitance C_th [J/K] is defined by

$$C_\mathrm{th} = cm, \tag{3.24}$$

where c is the specific heat capacitance [J/(K · kg)], and m is the mass in [kg]. Now we get for the thermal capacitance

$$C_\mathrm{th} = c\rho dA, \tag{3.25}$$

where ρ is the density [kg/m^3] of the material, d is the thickness of the heat transfer path [m], and A is the cross-sectional area [m^2] of the heat transfer path.

The step response $Y(s)$ of a system in the s-domain is

$$Y(s) = U(s) \cdot G(s), \tag{3.26}$$

where $G(s)$ is the transfer function and $U(s) = 1/s$ is the unity step input. By transforming the step function of the RC circuit in Eq. (3.23) to the Laplace domain and by dividing it by a unity step function $1/s$, we get the transfer function

$$Z_{\text{th}}(s) = G(s) \tag{3.27}$$

$$Z_{\text{th}}(s) = \frac{R_{\text{th}}}{1 + s\tau}. \tag{3.28}$$

This is easy to model in Simulink with a simulation model:

$$\frac{R_{\text{th}}}{1 + s\tau} = \frac{\frac{R_{\text{th}}}{\tau}}{s + \frac{1}{\tau}} = \frac{a}{s + b} = \frac{Y}{U} \tag{3.29}$$

$$\Rightarrow Y(s + b) = aU \tag{3.30}$$

$$\Rightarrow Y = \frac{1}{s}(aU - bY), \tag{3.31}$$

where

$$a = \frac{R_{\text{th}}}{\tau} \tag{3.32}$$

$$b = \frac{1}{\tau}. \tag{3.33}$$

The simulation diagram of one element is presented in Figure 3.6. In the model, the input and output are in the time domain, but the transfer function is in the s-domain. In reality, the Matlab simulation program transforms the transfer function back to a differential equation.

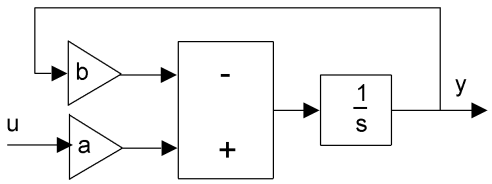

Figure 3.6: First-order RC circuit simulation model.

In practice, there are several thermal capacitances and resistances in the system as shown in Figure 3.7.
The thermal impedance $Z_{\text{th}}(t)$ for the ladder network with the Cauer topology is (Yun et al., 2001)

$$Z_{\text{th}}(t) = \sum_{i=1}^{n} \frac{T_i(t) - T_{i+1}(t)}{P}, \tag{3.34}$$

where T_i is the temperature of each physical layer. The thermal impedance for the

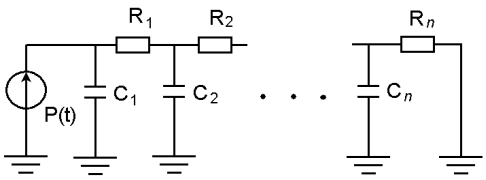

Figure 3.7: Ladder circuit with Cauer topology describing the physical thermal flow path. There can be an n number of thermal resistances and thermal capacitances.

ladder circuit in the s-domain is

$$Z_{\mathrm{th}}(s) = \cfrac{1}{sC_1 + \cfrac{1}{R_1 + \cfrac{1}{sC_2 + \cdots + \cfrac{1}{R_n}}}}. \tag{3.35}$$

This is inconvenient especially if there are many components in the system. However, this circuit can be represented by an equivalent circuit with the Foster topology of Figure 3.8.

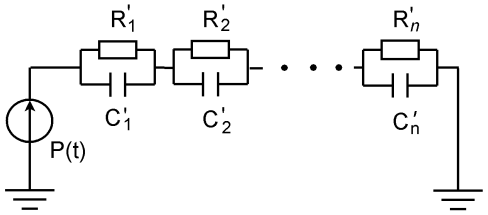

Figure 3.8: Equivalent circuit with the Foster topology describing the thermal flow path from the junction to the case.

The model with the Foster topology describes the junction temperature, but it is not capable of estimating the temperatures inside the system, since the nodes do not have physical counterparts in the system.

The thermal impedances of the Foster equivalent circuit can be summed as

$$Z_{\mathrm{th}}(t) = \sum_{i=1}^{n} R_{\mathrm{th},i}\left(1 - e^{\frac{t}{\tau_i}}\right) \tag{3.36}$$

which is in the s-domain

$$Z_{\mathrm{th}}(s) = \frac{R_{\mathrm{th},1}}{1+s\tau_1} + \frac{R_{\mathrm{th},2}}{1+s\tau_2} + \cdots + \frac{R_{\mathrm{th},n}}{1+s\tau_n}. \tag{3.37}$$

This can be simulated by paralleling the single elements of Figure 3.6.

The equivalent model only describes the total behavior of the system. Since the elements in the Foster circuit do not have real physical values, the temperature distribution inside the system cannot be described by this model. Furthermore, it cannot be extended simply by adding elements. If a heat sink needs to be added to the model, the values of all the elements have to be defined again (Pandya and McDaniel, 2002). Logically, it follows that the model cannot be extended with the interaction of the neighboring chips either without new measurements. However, a thermal model with several time constants is convenient to model in Simulink, if the Foster network is used, since it only requires the parallelling of the single elements in Figure 3.6.

3.3.3 Definition of thermal resistance

Thermal resistance R_{th} is defined according to material parameters, such as thermal conductivity and geometry

$$R_{\mathrm{th}} = \frac{d}{\lambda A}, \tag{3.38}$$

where d is the length of the heat transfer path, λ is the thermal conductivity [W/(m · K)], and A is the area of the cross section of the heat flow. The unit of thermal resistance is [K/W]. Thermal resistance between two points, for example the chip and the case, is usually defined by a temperature difference divided by the power losses

$$R_{\mathrm{th}} = \frac{\Delta T_{\mathrm{j-c}}}{P}, \tag{3.39}$$

where P is the power loss or heat flow between the two points of the temperature difference.

However, thermal resistance is an ambiguous parameter. Modifications outside the system also change the thermal resistance inside the system, as illustrated in Figure 3.9. This behavior was also shown in a study conducted by James et al. (2008). In their simulations, the change in the thermal parameters of the heat sink also influenced the thermal parameters of the module. This has to be borne in mind

when measuring the thermal resistance.

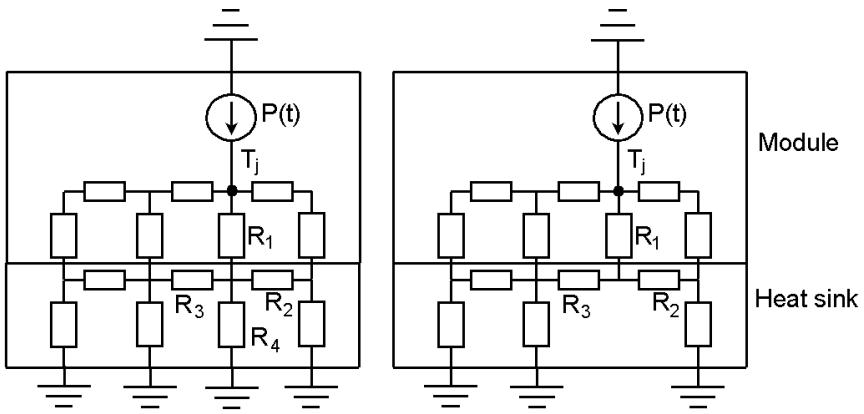

Figure 3.9: Module and heat sink. Drilling a hole inside the heat sink (right) changes the temperature difference over the thermal resistance R_1 inside the module. According to the definition of thermal resistance, this also changes the thermal resistance R_1 between these two points, even though the actual physical change is made to the outside of the module.

The heat flow is three dimensional, but the thermal resistance is defined only in two dimensions, from point to point. This is not realistic, and to accurately describe the heat transfer from the chip to the ambient, all the heat transfer paths have to be taken into account. Adding a heat sink with a smaller heat transfer coefficient changes the thermal resistance from the junction to the case. This is only a matter of definition, since actual material parameters cannot change that way.

Thermal resistance does not accurately describe the thermal behavior of the system, and therefore, a thermal characterization parameter Ψ (psi) is defined (Bar-Cohen et al., 1989; Dutta, 1988; Guenin, 2002)

$$\Psi_{\mathrm{j-c}} = \frac{\Delta T_{\mathrm{j-c}}}{P}, \tag{3.40}$$

where P is the power loss in the junction, or the total heat flow from the junction to ambient. This way, all the heat flow paths from the chip to the ambient are taken into account without defining them separately. The thermal characterization parameter Ψ includes all changes made to the system.

In this thesis, when R_{th} is used, the latter definition is actually meant in practice. Although it is not scientifically the most accurate method, it serves it's purpose in

this study better than the first definition. The thermal resistance of the materials is not of interest, but the total thermal *behaviour* of the module. These two have a different meaning, as explained in Figure 3.9.

3.4 Model verification

A test system was constructed to verify the thermal model (Ikonen et al., 2006). It allows to measure and simulate the temperature difference $T_{\mathrm{j-c}}(t)$ simultaneously. The load of the IGBT, that is, the switching frequency and the duty cycle can be varied freely during the measurement; they are also inputs in the simulation model at the same time.

3.4.1 Measurement setup

A commercially available voltage source frequency converter was used as the hardware and dSpace as the control system. dSpace is a DSP-based control system that allows to implement control methods directly form Simulink simulation models. The control system allows to change the switching frequency, the PWM duty cycle, and the base frequency independently.

The system consists of a frequency converter, a dSpace, an IGBT gate control circuit, measurement electronics, and an RL load. The measurement electronics provide measurements for the DC link voltage, the chip temperature and the reference temperature, and the load current. The temperature and the voltage measurement are connected with an optical cable to the control, whereas the current measurement is carried out with an analog circuit and analog-to-digital conversion in the dSpace input block. The author designed the top-level of the system and the measurement electronics for the temperature and the DC link voltage, whereas the LR circuit and the current measurement hardware were designed by Heikki Häsä, M.Sc. (Häsä, 2005).

A block diagram of the test system is presented in Figure 3.10 and a photo of the converter and the measurement electronics in Figure 3.11. The reason for conducting the measurements with a chopper instead of a fully functional frequency converter is the physical restraints in the temperature measurements. It is impossible to carry out the chip temperature measurement with normal hardware because the chip can-

not be accessed with the measurement equipment in question.

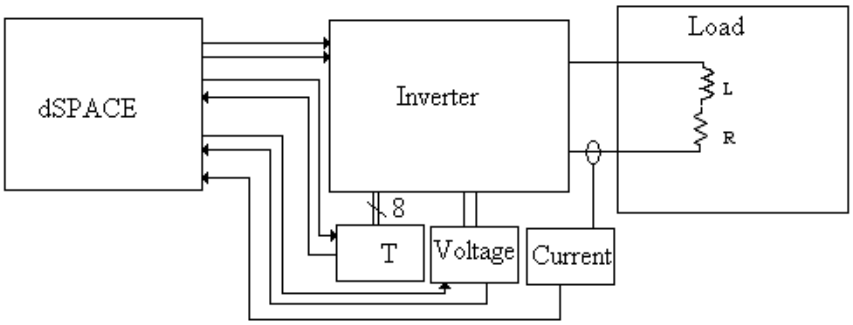

Figure 3.10: Block diagram of the system for the thermal model verification. It consists of a dSPACE, an inverter, a load, and measurements. There are eight thermocouples in the inverter, but only two of them are measured at a time. The DC link voltage and the output current are also measured.

The frequency converter is used as a one-phase chopper, driving a resistor with an inductor in series. The nominal current of the power module MiniSKiiP 32NAB12T1 is 32 A. The load resistor was selected aiming to keep the power as close to the nominal as possible. Thus, the selected resistance is 38 Ω and the nominal current is 14.7 A with a 560 V DC link voltage. The inductor with a 50 mH nominal inductance is used to smooth the load current ripple of the resistor. The load is connected to be driven either with the upper IGBT or the lower IGBT of the same branch, since these have thermocouples glued on top of them.

The temperature of the hottest chip in a three-phase full-bridge module is measured. The IGBT under test consists of two paralleled chips, but in the power loss and temperature estimation, the two chips are treated as one IGBT. It is estimated that in normal operation, the hottest IGBT is in the middle of the module. The heat sink temperature is measured underneath the chip center by drilling a hole from the backside of the heat sink until only 2 mm is left and then gluing the thermocouple as advised by Hecht and Scheuermann (2001).

The temperatures of the chips are measured with thermocouples. The power module MiniSKiiP 32NAB12T1 is customized by the manufacturer with thermocouples glued on the IGBT and diode chips in the middle phase. The thermocouples are on the emitter potential of each IGBT and on the anode potential of each diode.

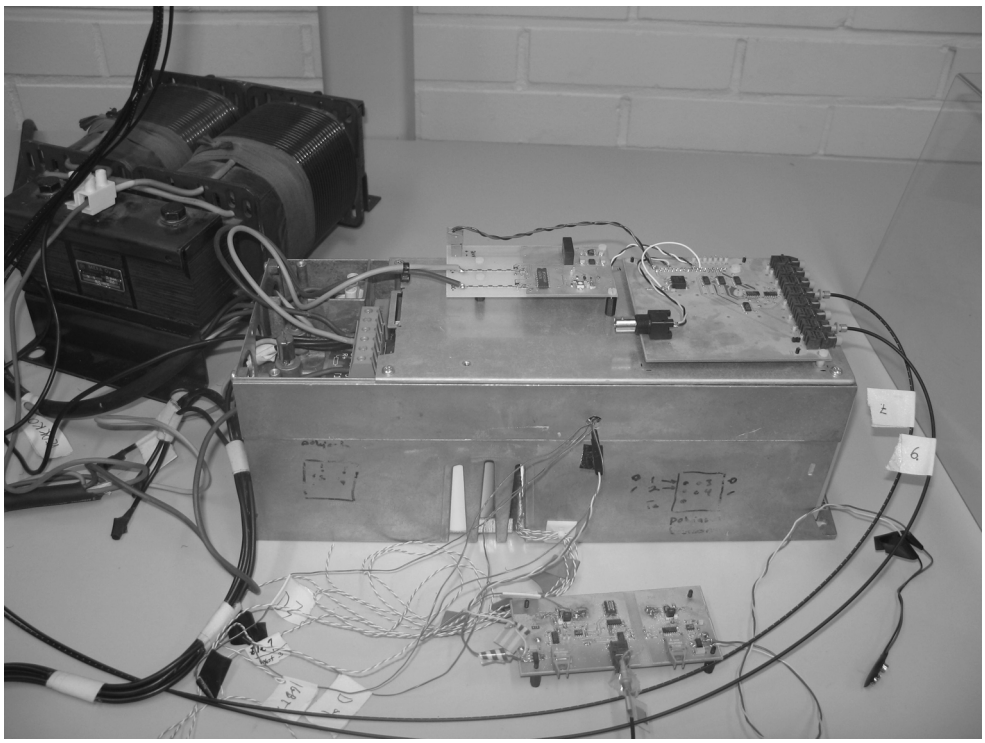

Figure 3.11: Test system for the thermal model verification. The IGBT gate control and the DC link measurement electronics are placed on top of the inverter, and the thermocouple measurement electronics is on the table. The thermocouple wires come through the sidewall of the converter.

The temperature measurement electronics is custom made because of the high requirements for the voltage range and the sampling frequency. The frequency converter is fed with a three-phase 400 V grid, and thus, the DC link voltage is 560 V. The thermocouple of each chip establishes a galvanic contact between the thermocouple wire and the IGBT emitter, and thus, the potential of the top IGBT thermocouple varies between DC+ and DC- according to the switching status. This potential is common for both of the two wires, and therefore, the measurement electronics has to provide a galvanic isolation between the thermocouple and the user and to withstand high-frequency common-mode voltage without affecting the measurement results. Because the model is only for the power module, the case temperature is measured as a reference temperature to acquire the temperature difference from the chip to the case $T_{\mathrm{j-c}}(t)$.

The signal from the thermocouple is first amplified with an analog circuit. Then an

analog-to-digital converter converts it to digital. The conversion is controlled via an optical fiber from the dSpace. Also the converted result is transmitted to the dSpace via an optical fiber.

The thermal time constants of the module are less than one second, and thus, the bandwidth of the temperature measurement has to be higher than one hertz. The bandwidth of the thermocouple is limited by its mass and thermal capacitance. A thermocouple was made from excess wire, and the time constant was measured. It was found that the thermal time constant is in the range of ten milliseconds, and thus, it was estimated that the the bandwidth is high enough for this application. The sampling rate was set to 50 kHz, because this sampling rate is readily available in the control equipment.

3.4.2 Thermal model

The verified thermal model is a Foster network with three time constants and thermal resistances. The simulation model of one IGBT chip is realized with parallel connection of elements which are presented in Figure 3.6. Only one IGBT is loaded to exclude the cross-effect of the other chips on the temperature. The load current is assumed to be in phase with the voltage. The power factor $\cos\varphi$ affects the power loss distribution between the IGBT and the free-wheeling diode; the lower the value, the more power losses are generated in the diode. In an ideal case with a purely resistive load, there would be power losses only in the IGBT.

The power losses are described as tables where the collector current is the input parameter. The tables are made of less than ten points, and if the input value is between the points, the output is interpolated linearly of the nearest values. Temperature dependence of the power losses on the IGBT chip temperature is taken into account by feeding back the estimated chip temperature to the power loss estimation.

3.4.3 Thermal parameter measurements

The hole in the heat sink changes the thermal resistance of both the heat sink and the module. This is the reason why thermal parameters are characterized using this very same frequency converter instead of using the data sheet values. Another reason is that the data sheet values are maximum values, and the real thermal resistance is within some tolerance of the data sheet value causing an error in the temperature

estimation.

The cooling curves of the IGBTs of the middle phase were recorded by first heating the IGBTs with a constant current source to a thermal equilibrium, and then letting it cool to the ambient temperature. After the thermal equilibrium was reached, the IGBT was turned off and the cooling curve was recorded with the dSpace. Then, the thermal parameters R_{th} and τ of Eq. (3.36) for the Foster type network were defined by a program called 'CurveExpert' version 1.3 with the least square method. Sets of two, three, and six thermal resistances and the corresponding time constants were determined (n = 2, 3, or 6) for each chip.

The bottom-leg IGBT was heated with a 49 A current, resulting in a 155 W power, to the temperature of $T_{\mathrm{j}} = 96°\mathrm{C}$ and $T_{\mathrm{j-c}} = 50°\mathrm{C}$. The top-leg IGBT was heated with a 50 A current, 157 W power, to $T_{\mathrm{j}} = 101°\mathrm{C}$ and $T_{\mathrm{j-c}} = 53°\mathrm{C}$. The cooling curves are similar in shape; the cooling curve of the bottom-leg IGBT is demonstrated in Figure 3.12.

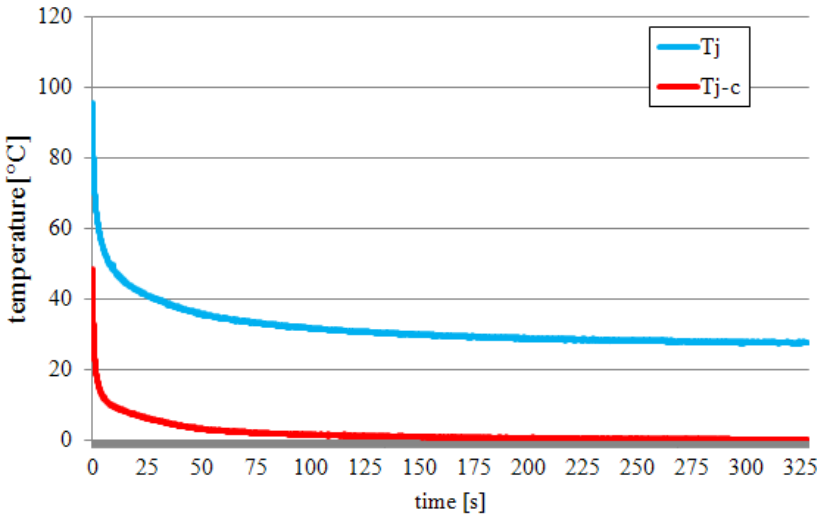

Figure 3.12: Cooling curve of the bottom-leg IGBT after the IGBT has been switched off. T_{j} is the chip temperature and $T_{\mathrm{j-c}}$ is the temperature difference between the chip and the case.

The resulting thermal parameters for the top-leg IGBT (n = 3) are listed in Table 3.1 and for the bottom-leg IGBT in Table 3.2.

The total thermal resistance of the top-leg IGBT is 0.336 K/W and of the bottom-leg

Table 3.1: Measured thermal parameters of the top-leg IGBT for n= 2, 3, and 6. The unit of thermal resistance is [K/W] and the unit of time constant [s]. Three thermal resistances and time constants suffice to define the thermal behavior of the IGBT. Using six parameter pairs gives no additional value over three parameter pairs.

index	n = 2	n = 3	n = 6
1	$R_{\text{th1}} = 0.284$	$R_{\text{th1}} = 0.213$	$R_{\text{th1}} = 0.17$
2	$R_{\text{th2}} = 0.05$	$R_{\text{th2}} = 0.036$	$R_{\text{th2}} = 0.029$
3		$R_{\text{th3}} = 0.087$	$R_{\text{th3}} = 0.034$
4			$R_{\text{th4}} = 0.034$
5			$R_{\text{th5}} = 0.034$
6			$R_{\text{th6}} = 0.034$
1	$\tau_1 = 0.996$	$\tau_1 = 0.98$	$\tau_1 = 0.98$
2	$\tau_2 = 58$	$\tau_2 = 48$	$\tau_2 = 48$
3		$\tau_3 = 5426$	$\tau_3 = 11134$
4			$\tau_4 = 11134$
5			$\tau_5 = 11134$
6			$\tau_6 = 11134$

Table 3.2: Measured thermal parameters of the bottom-leg IGBT for n= 2, 3, and 6. The unit of thermal resistance is [K/W] and the unit of time constant [s]. Three thermal resistances and time constants suffice to define the thermal behavior of the IGBT. Using six parameter pairs gives no additional value over three parameter pairs.

index	n = 2	n = 3	n = 6
1	$R_{\text{th1}} = 0.249$	$R_{\text{th1}} = 0.229$	$R_{\text{th1}} = 0.214$
2	$R_{\text{th2}} = 0.08$	$R_{\text{th2}} = 0.0698$	$R_{\text{th2}} = 0.066$
3		$R_{\text{th3}} = 0.027$	$R_{\text{th3}} = 0.0115$
4			$R_{\text{th4}} = 0.0115$
5			$R_{\text{th5}} = 0.0115$
6			$R_{\text{th6}} = 0{,}0115$
1	$\tau_1 = 1.11$	$\tau_1 = 1.045$	$\tau_1 = 1.044$
2	$\tau_2 = 35$	$\tau_2 = 27$	$\tau_2 = 27$
3		$\tau_3 = 586$	$\tau_3 = 1309$
4			$\tau_4 = 1309$
5			$\tau_5 = 1309$
6			$\tau_6 = 1309$

IGBT 0.326 K/W. The data sheet value for the maximum thermal resistance of the IGBT is 0.5 K/W (Semikron, 2001), which is much higher than the measured value.

The tables show that using more than three time constants in the curve fitting is unnecessary. The values of the thermal resistance and the time constant for the indices 3 to 6 are identical in the case of six time constants. This is due to the curve fitting, as it is difficult to find values for long time constants, especially if there are many of them.

The thermal resistance that corresponds to the smallest time constant is dominating in the case of $n = 2$ and $n = 3$. It makes 63% of the total thermal resistance of the top-leg IGBT and 70% of that of the bottom-leg IGBT. Based on the measurements, the smallest time constant is around 1 s. This is in line with the typical time constants of power modules, which are usually below 1 s. However, the other proportions of the thermal resistances, 30% and 37%, correspond to much longer time constants.

The cooling curves of both the chip temperature and the case temperature of the bottom-leg IGBT are shown in Figure 3.13. The plot shows that the case temperature changes during the measurement.

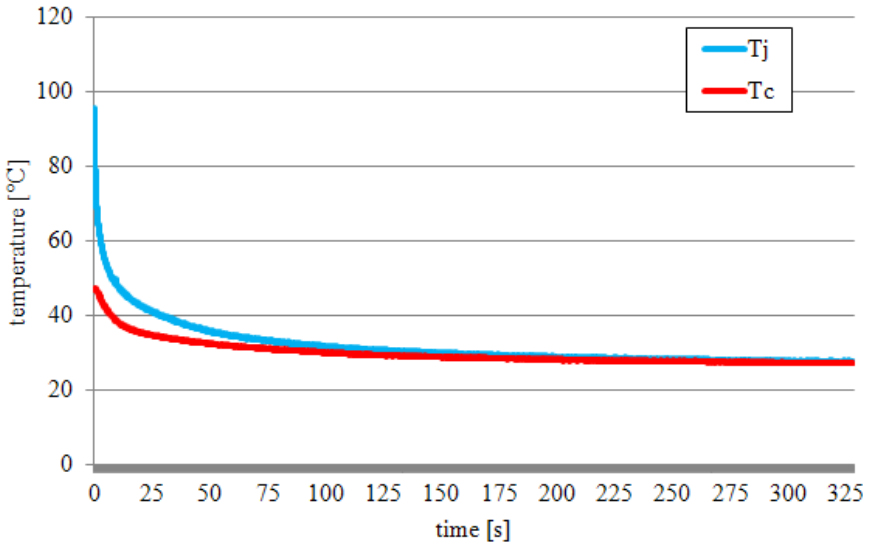

Figure 3.13: Cooling curves of the heat sink and the bottom-leg IGBT after the IGBT has been switched off. T_j is the chip temperature and T_c is the case temperature.

3.4.4 Model verification measurements

The model verification measurements were conducted with the bottom-leg IGBT with the set of three thermal parameters ($n = 3$) given in Table 3.3.

Table 3.3: Measured thermal parameters of the bottom-leg IGBT for n= 3. The unit of thermal resistance is [K/W] and the unit of time constant [s].

index i	$R_{\mathrm{th}i}$	τ_i
1	0.229	1.045
2	0.0698	27
3	0.027	586

First, the thermal model was tested with a step from no-load to full load. At the beginning of the measurement, the IGBT was constantly switched off. Then, it was modulated with a 16 kHz frequency and a constant duty cycle of 0.95 so that the constant output current was 14 A. The measured and simulated chip temperatures are presented in Figure 3.14. The figure is cropped from the graphical user interface of the dSpace. In the upper plot, there are the DC link voltage (red), the output current (green), and the total power loss (blue). In the lower plot, the measured temperature is in green and the simulated one in blue. The time on the x-axis is in seconds.

The thermal model was also tested with a sinusoidal load with a low frequency. The switching frequency was 16 kHz and the modulation index 0.9. The measured and simulated chip temperatures are presented in Figure 3.15 with the output current of the module and the duty cycle.

Figure 3.14 shows that there is some deviation between the measured and calculated chip temperatures. The time constant of the simulated temperature does not match that of the measured temperature. There is also some error in the final temperature. This may be due to the use of data sheet values of the voltage U_{CE} and the switching energy E_{sw}, which are only typical values.

Figure 3.15 shows that the simulated temperature follows the measured temperature with a 5°C accuracy.

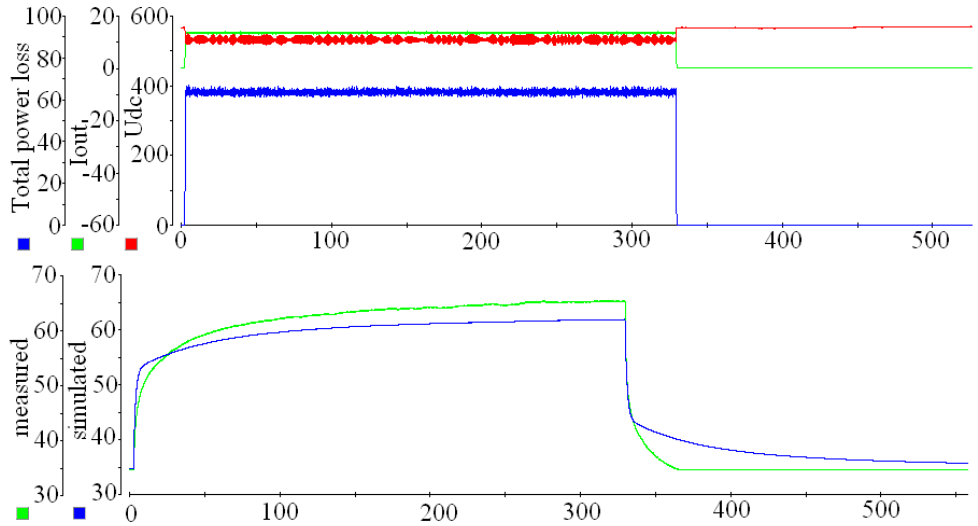

Figure 3.14: Simulated and measured IGBT temperatures with a load step. Upper plot: the DC link voltage (red), the output current (green), and the total power loss (blue). Lower plot: the measured (green) and simulated (blue) temperatures. The time is on the x-axis in seconds and the temperature on the y-axis in degrees of Celsius. The switching frequency is 16 kHz and the duty cycle 0.95.

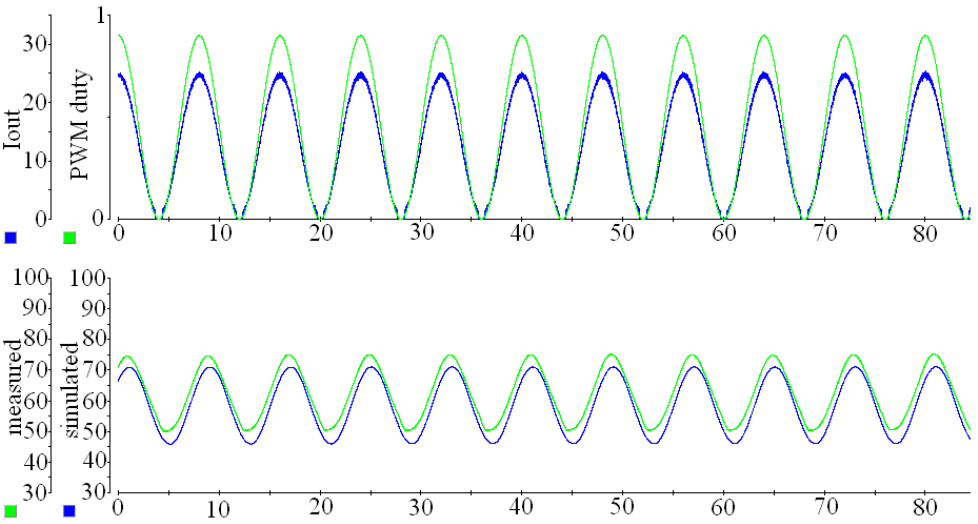

Figure 3.15: Simulated and measured IGBT temperatures with a sinusoidal load. Upper plot: the output current (blue) and the duty cycle (green). Lower plot: the measured (green) and simulated (blue) temperatures. The time is on the x-axis in seconds and the temperature on the y-axis in degrees of Celsius. The switching frequency is 16 kHz and the modulation index 0.9.

3.5 Hardware implementation

The thermal model was modified so that it can be programmed with a hardware description language (VHDL) to an FPGA. These modifications include signal conversion from the floating point format to the fixed point format and the use of per unit values and a fixed step time (Deziel, 2001, pp. 335–380). Additionally, the look-up tables in the model have to be changed so that the distances of the input values are always two's exponents and the integrators in the calculation are discrete. The signals have a limited bit width in the fixed point format, that is, they are quantized. Additionally, the sample time is fixed.

The input signals of the modified model are discretized, converted into per unit format, and quantized with A/D blocks. Such a block is presented in Figure 3.16.

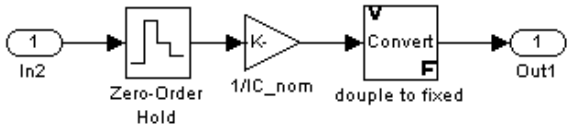

Figure 3.16: Example of an A/D-block, in which the input signals are discretized, converted into per unit format, and quantized.

In this study, the dependence of the conduction power losses on the chip temperature is excluded to simplify the simulations. In the original model, the conduction state voltage drop is given as a two-dimensional table. The temperature of the chip and the output current are the inputs of the original table, but in the modified table the only input is the output current. The tables are valid with a 25°C temperature.

The integrators are discretized with the forward Euler mapping. The integrator response in the z-domain is

$$\mathrm{H}(z) = \frac{Az^{-1}}{1 - Bz^{-1}}, \tag{3.41}$$

where the coefficients A and B are dependent on the step time h, the thermal resistance R_{th}, and the corresponding thermal time constant τ:

$$A = \frac{h \cdot R_{\mathrm{th}}}{\tau} \tag{3.42}$$

$$B = 1 - \frac{h}{\tau}. \tag{3.43}$$

The integrator is damped because the coefficient B is always less than one.

The coefficients of the integrators depend on the step time h according to Eq. (3.42) and Eq. (3.43); the shorter the step time, the more resolution is required. However, in the FPGA implementation, the effective bit width should be used. This leads to an optimization problem with the step time. The step time must be shorter than the shortest thermal time constant, but long enough to achieve a reasonable accuracy with a limited bit width. The step time and the bit width are given as parameters in the model, and thus, they can be easily changed for simulation purposes. The initial step time was decided to be 100 μs. The optimal global bit width in the model is 16 bits with this step time, except for the integrators, for which the bit width is 24 bits. The accuracy is worse with fewer bits, but on the other hand, extending the bit width from this value does not have a significant effect on the accuracy.

The aim in the model conversion is to retain a 5% accuracy compared with the original model. The converted model is made by using Fixed Point Blockset by Simulink, which ensures that all the signals are in the fixed point format. All input variables, parameters, and constants are given in a per unit (p.u.) format. Thus, all the signals have a certain nominal value, which is usually the maximum value plus some additional scale. The additional scale guarantees that the values are below one in every case, even if extraordinary operation occurs in a practical application. The conduction power losses have different nominal values from the switching power losses. The actual $T_{\mathrm{j-c}}(t)$ calculation also has a different nominal value. Because of this, there is a scaling factor between the power loss calculations and the $T_{\mathrm{j-c}}(t)$ calculations, and also between the switching loss calculation and the summing of the losses. The modified model is presented in Figure 3.17.

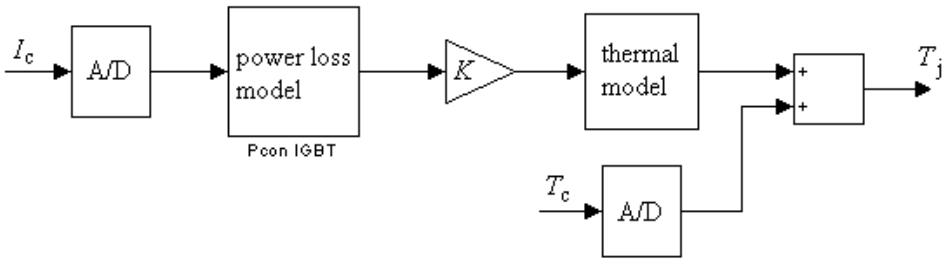

Figure 3.17: Block diagram of the modified model. In comparison with the original model there are A/D-blocks in the input signals and a scaling factor K for switching from one nominal value to another.

There are three look-up tables in the model: the IGBT conduction mode voltage drop versus the output current, and the IGBT switching energy versus the output current and versus the gate resistance. The tables must be modified so that the distance of two consecutive input value points is always a two's exponent. The look-up table for the switching energy E_{sw} versus the collector current I_c is presented in Table 3.4 as an example. The current is the input and the switching energy is the output of the table.

Table 3.4: The modified table of the IGBT switching energy E_{sw} versus collector current I_c.

I_c	I_c	interval	E_{sw}
[A]	[p.u.]	[p.u.]	[mW]
0	0		0
		$1/2^1$	
88	1/2		25

Both the original and modified tables are plotted as a function of current in Figure 3.18. As we can see from the figure, the modified look-up table is inaccurate. The table needs adjustments and more data points to give accurate results. However, it can be used in simulations to determine how much of the inaccuracy in the converted model comes from the look-up tables. An improved version of the modified table is presented in Table 3.5 with more data points. Both the original table and the improved version of the modified table are plotted in Figure 3.19.

Table 3.5: Improved version of the modified table of the IGBT switching energy E_{sw} versus the output current I_c.

I_c	I_c	interval	E_{sw}
[A]	[p.u.]	[p.u.]	[mW]
0	0		0
		$1/2^3$	
22	$1/2^3$		4.65
		$1/2^2$	
66	$3/2^3$		18

3.5.1 Simulations

Simulations of the modified model were made using both versions of the modified look-up tables in order to find out how much of the error in the power loss calculation results from the look-up table error. The results of this simulation were compared against the simulation results of the original model. In both models, the temperature dependency was neglected, and the only input parameter was the output current.

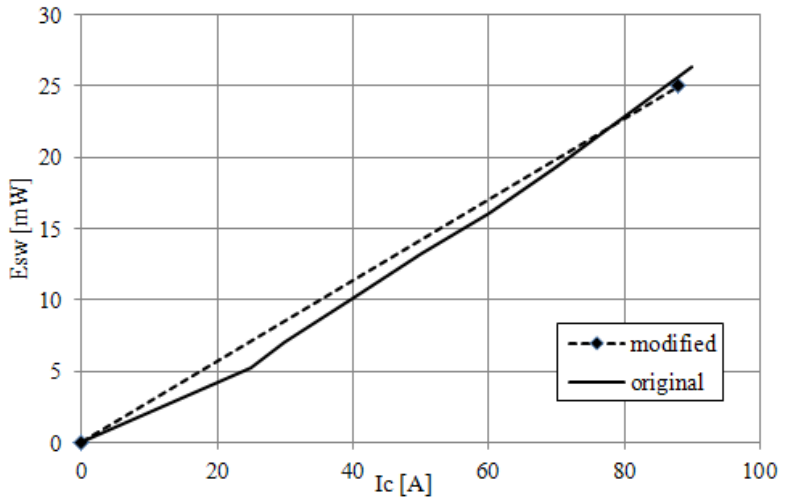

Figure 3.18: IGBT switching energy versus the output current of the inverter. The solid line presents the original look-up table and the dotted line presents the modified table.

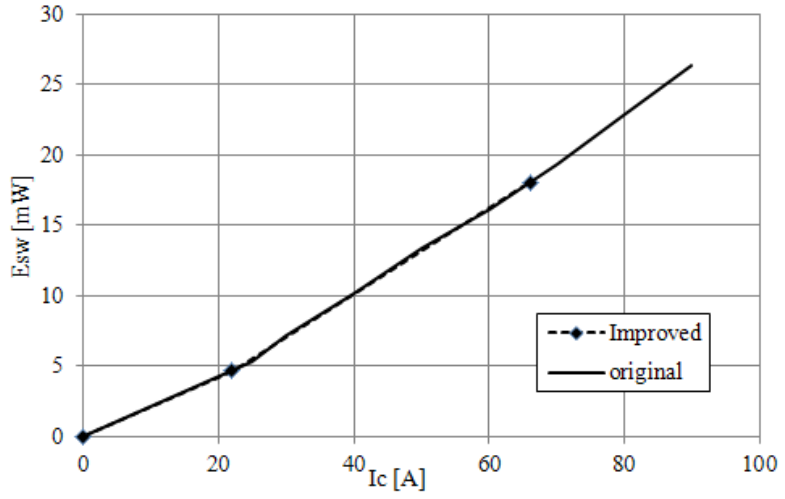

Figure 3.19: Plot of the improved table of the IGBT switching energy versus the output current of the inverter. The solid line presents the original look-up table and the dotted line presents the improved version of the modified table.

The current was sinusoidal with the amplitude proportional to the frequency of the current. The switching frequency was kept constant at 10 kHz. Table 3.6 presents the amplitude and frequency of the current and the simulation results for the IGBT power losses with both models. The first versions of the modified look-up tables were used in this simulation.

Table 3.6: Simulation results with the original and modified thermal models for the power losses of the IGBT as a function of frequency of the current. The first versions of the modified look-up tables are used.

		original	original	modified	modified
f	I	P_{sw}	P_{cond}	P_{sw}	P_{cond}
[Hz]	[A]	[mW]	[mW]	[mW]	[mW]
50	31	17.3	22.8	22.6	22.7
40	24.8	13.1	16.6	18	16.2
30	18.6	9.9	11.1	13.5	10.6
20	12.4	6.6	6.2	8.9	5.9
10	6.2	3.3	1.7	4.4	2.2
5	3.1	1.6	0.4	2.1	0.6

There is some difference in the simulated losses between the original model and the converted model. As an example, the switching losses are plotted as a function of frequency of the current in Figure 3.20.

As can be seen in Figure 3.20, the error between the models is as much as 37% with the first versions of the look-up tables. The simulation results with the improved versions of the tables are presented in Table 3.7.

Table 3.7: Simulation results with the original and improved modified thermal models for the power losses of the IGBT as a function of frequency of the current.

		original	original	improved	improved
f	I	P_{sw}	P_{cond}	P_{sw}	P_{cond}
[Hz]	[A]	[mW]	[mW]	[mW]	[mW]
50	31	17.3	22.8	17.9	22.5
40	24.8	13.1	16.6	13.6	16.4
30	18.6	9.9	11.1	10	10.9
20	12.4	6.6	6.2	6.6	6.1
10	6.2	3.3	1.7	3.2	1.7
5	3.1	1.6	0.4	1.5	0.4

In this case, the error is 7% at maximum. Again, the switching power losses are presented as a function of frequency of the current in Figure 3.21.

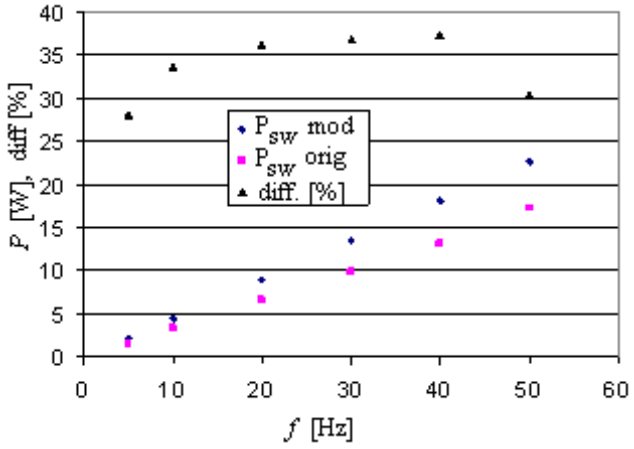

Figure 3.20: Simulation results for the switching losses of the IGBT as a function of frequency of the current. The black triangle indicates the difference between models. The first versions of the modified look-up tables are used.

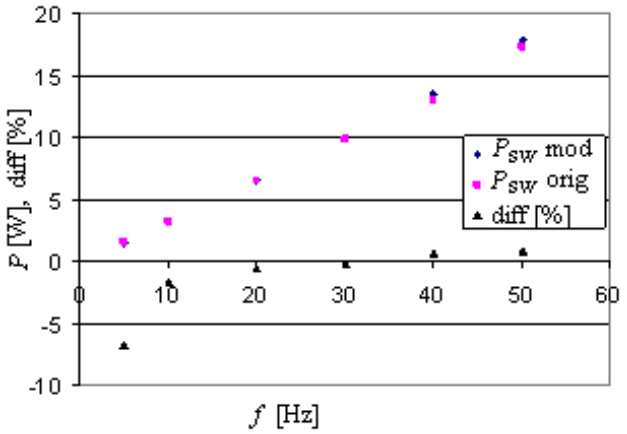

Figure 3.21: Simulation results for the switching losses of the IGBT as a function of frequency of the current. The black triangle indicates the difference between models. Improved versions of the look-up tables are used.

In addition, the temperature difference between the chip and the reference point was simulated. A sinusoidal current step was fed to the model at an instant of 0 s. The amplitude of the current was 31 A and the frequency 50 Hz. The simulations were carried out with the original and modified models. The improved versions of the modified look-up tables were used in the modified model. The results are presented in Figure 3.22. It can be seen that both models, the original and the fixed point, give accurately the same result for the temperature.

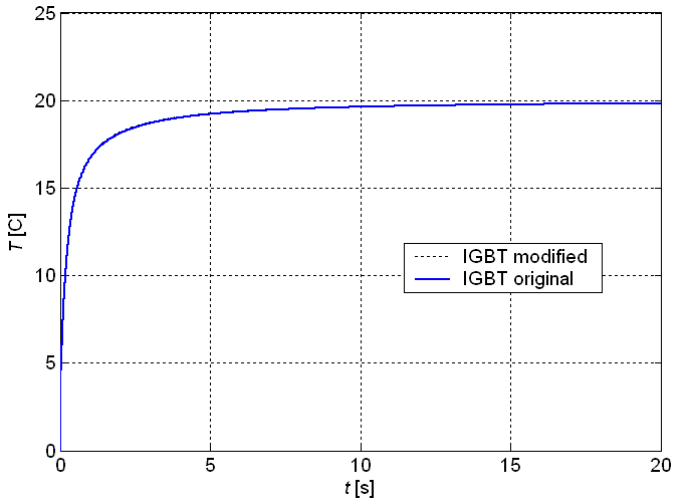

Figure 3.22: Simulated temperature of the IGBT when a current step is fed to the model. There is no visible difference between the original model (solid blue line) and the modified model (dotted black line).

3.6 Discussion

The constructed model does not take into account the influence of the power factor cosφ on the power losses of the IGBT. Now, the model assumes a power factor of 1. This situation is worse, however, than if the power factor were lower, and thus, we are on the safe side from the perspective of the power cycling lifetime estimation. The lifetime estimation does not give an overestimated value when this model is applied. Depending on the application, the power factor can be anything between 1 (resistive) and -1 (inductive or capacitive). In the future work, though, the power factor has to be taken into account when applying the model to the lifetime estimation of different applications. Moreover, it is essential in the temperature modeling of the diodes.

The constructed measurement setup allows to test the thermal behavior of the IGBT with variable loading. The loading parameters, that is, the duty cycle of the pulse width modulation and the switching frequency, can be set freely, which provides opportunities to test different kinds of loading scenarios. Additionally, it allows to run the simulation model simultaneously, making it possible to observe for example the effect of changes in the switching frequency on the simulation results and compare them with the actual measured chip temperature. It was found that there are certain issues in building this kind of a system that have to be taken care of.

One issue is the measurement of the chip temperature. The thermocouple is glued on top of the chip. The contact is not perfect, allowing glue to get between the chip and the thermocouple. This causes thermal resistance to the measurement itself and thereby changes the measurement dynamics. Moreover, when using pulse-width modulation, the output voltage interferes the output of the thermocouple. These interferences have to be filtered off. The third issue with the thermocouple measurement is again caused by gluing. If the contact between the thermocouple and the chip is not perfect, the common-mode potential of the thermocouple will float. This causes problems to the measurement electronics, which has a less-than-infinite common-mode rejection ratio in the input stage. In order to get accurate measurements, floating of the common-mode potential of the thermocouple has to be prevented.

The parameter variation is an issue the in power loss estimation. The on-state voltage drop of IGBTs can vary from module to module causing an error in the power loss estimation if the voltage drop is not verified first. This issue can be overcome if the actual collector-emitter voltage is being measured all the time. This type of measurement should be with high bandwidth and the sampling should be properly timed to match the on-state of each chip. It would mean additional costs because of additional measurement electonics placed in the frequency converter. On the other hand, if there is an accurate collector-emitter voltage measurement, the chip temperature can be calculated directly from it without the need for a sophisticated thermal model.

The simulated temperature of the IGBT deviated 5°C from the measured temperature. Furthermore, it was shown by simulations that the modified model for the hardware implementation corresponds with the original model with a 5% accuracy. This is a small difference but it adds up to the total error in the temperature estimation.

3.7 Summary

A thermal simulation model for a single IGBT was constructed. The model estimates the chip temperature based on the estimated power losses of the chip and the measured thermal parameters.

In addition, a test system was built to verify the simulation models. It was based on the simultaneous measurement and simulation of the chip temperature. Different alternatives to measure the chip temperature were considered, and the thermocouple measurement was examined in detail. The thermal parameters of the system were defined. Based on the research, this kind of a system proved to be convenient for studying the thermal behavior of the chip.

The thermal model was verified. It was found that the constructed thermal model has a 5°C accuracy in the temperature estimation.

The thermal model was prepared for hardware implementation. It was found that the hardware implementation increases the error in the temperature estimation by 5%.

Chapter 4

Lifetime estimation of power modules

4.1 Introduction to Chapter 4

Power modules are mostly used in dynamic-mode applications. The lifetime of a power module is strongly dependent on load conditions, because most of the breaking mechanisms are related to cyclic loading of the module. Thus, it is necessary to consider the mission profile of the application when estimating the power cycling lifetime of a power module. The mission profile can be the output power, output current, or the chip temperature. An example of the converter load is presented in Figure 4.1, where the mission profile of a full power converter in a direct-driven wind turbine is presented. The length of the data is 38 minutes, starting at 1:27 am and ending at 2:05 am. The data are from December 1$^{\text{st}}$, 2011. There are several power cycles with various heights visible in the data.

The power cycling lifetime N_{f} of a power module is typically given as a function of junction temperature swing amplitude ΔT_{j}. The module manufacturers define the lifetime with tests performed in the controlled environment, where each module is constantly loaded on and off to achieve the predefined chip temperature swing ΔT_{j}. The lifetime curves can be drawn after several pieces are tested with varying temperature swings. The chip medium temperature T_{m} is also varied in the tests.

The lifetime of a power module can be tens of years resulting in very long test times. To overcome this issue, the cycles are highly accelerated in the power cycling tests. In an accelerated test, the duration of the power cycle is reduced to a minimum and

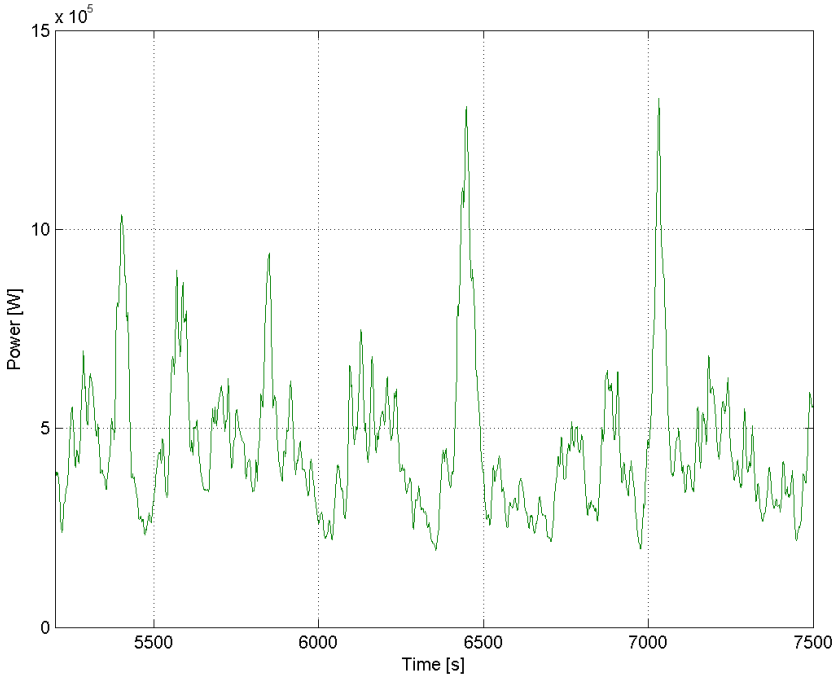

Figure 4.1: Example of a mission profile of an inverter in a wind turbine. The output power of a 1,5 MW direct-driven turbine is simulated based on wind measurements in south-east Finland.

the junction temperature amplitude is increased; however, the junction temperature is always kept within the safe operating area (Cova and Fantini, 1998).

There are five steps when estimating the consumed lifetime of a power module. The first step is the modeling of the IGBT chip temperature, which was presented in Chapter 3. Then, the number N of temperature cycles is counted from the temperature plot. The consumed life is calculated by comparing the cycle count with the nominal cycle count N_f of the module in question. The nominal cycle count is acquired by power cycling tests with a lifetime model. The lifetime estimation procedure is illustrated with a flow chart in Figure 4.2.

In this chapter, models to estimate the power cycling lifetime are presented. Then, power cycling lifetime tests of a module with a base plate and a lead-free solder layer are conducted. An estimation method is presented for the consumed life with cycle counting from the chip temperature profile.

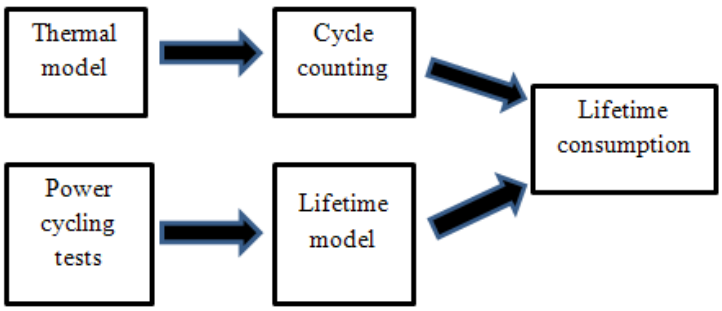

Figure 4.2: Flow chart of the lifetime consumption estimation.

Last, lifetime consumption of a full power converter of a direct-driven wind turbine is calculated based on wind measurements in a prospective wind park site using all the previously presented methods; thermal modeling of an IGBT chip based on the power loss estimation, cycle counting from the simulated temperature curve, and applying the measured lifetime curves to estimate the lifetime usage.

4.2 Lifetime modeling

It is possible to estimate the progress of the degradation by relating it to the amplitudes of the junction temperature cycles with a lifetime model. Typically, analytical models are used since they do not require a detailed analysis of the physical properties of the module. In addition, there is no distinction between the degradation mechanisms in the models. Only the test parameters such as ΔT_j or T_m are needed. All the analytical models presented in this chapter give the power cycling lifetime with a single value of ΔT_j.

However, the IGBT chips experience different temperature swings during the operation practically in every application. To overcome this issue in the lifetime estimation, the experienced temperature cycles are categorized based on the temperature swing ΔT_j and the medium temperature T_m into bins. Then, the life consumption in percentage of the total available life is calculated for each bin. These fractions are added up, and thus, the total life consumption (LC) is achieved.

4.2.1 Literature survey

The methods for the lifetime estimation have been studied by many research groups over the last years. Musallam et al. (2008) have studied the lifetime estimation methods using a thermal model and the rainflow counting method. They used an arbitrary mission profile to estimate the solder layer degradation as a case study. According to their study, the methods are usable in the crack growth estimation in the solder layer.

Hirschmann et al. (2006) estimated the lifetime of a hybrid car by using a thermal model and their own method to count the temperature cycles. They investigated the methods to estimate the remaining lifetime of power modules, with a hybrid car as an example case.

All the above studies apply a thermal model to the lifetime estimation. The output of the thermal model, that is, the chip temperature, is then used to estimate the used power cycling life with the rainflow counting or similar methods. The rainflow counting method is adopted from material science to power electronics. In the above studies, a case application is used to validate the methods; Musallam et al. (2008) used an arbitrary mission profile, which has no link to the real world, while Hirschmann et al. (2006) used a mission profile of a hybrid car. They obtained the power cycling curves from the module manufacturers.

Wei et al. (2008) studied the mean time to failure (MTTF) of an adjustable speed drive in various operation points. These include low-speed operation, overload operation, and low-switching-frequency operation. They found that the lifetime of the IGBTs in a variable speed drive decreases as the operation speed decreases. Their main finding was that the chip size is the most important parameter influencing the lifetime of the module. Further, at a low operation speed, the lifetime of the module can be increased by decreasing the switching frequency, thereby decreasing the losses of the IGBT and the diode chips.

In this study, the same methods are used as in the above-mentioned studies. This establishes a common ground to analyze the results of the study. However, the lifetime curves of the power module are measured by the author himself by power cycling tests. Based on the study, the load of the IGBT in a wind power application can be reduced and the operation point optimized according to the methods given by Wei et al. (2008).

4.2.2 Definition of the end of life

The solder layer delamination increases the collector-emitter voltage U_{CE} and the thermal resistance from the chip to the base plate of an IGBT towards the end of life. The increased thermal resistance and the collector-emitter voltage also increase the chip power losses and the chip temperature in the steady state.

Bond wire lift-off also increases the electrical resistance between the bond wire and the chip increasing the total R_{ce}. This can be seen as a rapid increase in the saturation value of the collector-emitter voltage in power cycling tests. The third factor influencing the voltage is the aluminum reconstruction during high temperature swings. It increases the contact resistance of the bond.

The total increase in the U_{CE} is in the range of hundreds of millivolts. For comparison, the saturation voltage is in the range of a few volts. It is relatively easy to see the end of life from the U_{CE} graph, as illustrated in Figure 4.3. In the figure, the collector-emitter voltage and the chip temperature of both IGBTs in a half-bridge module are presented. In the example, the module comes to end of life after 174 000 cycles.

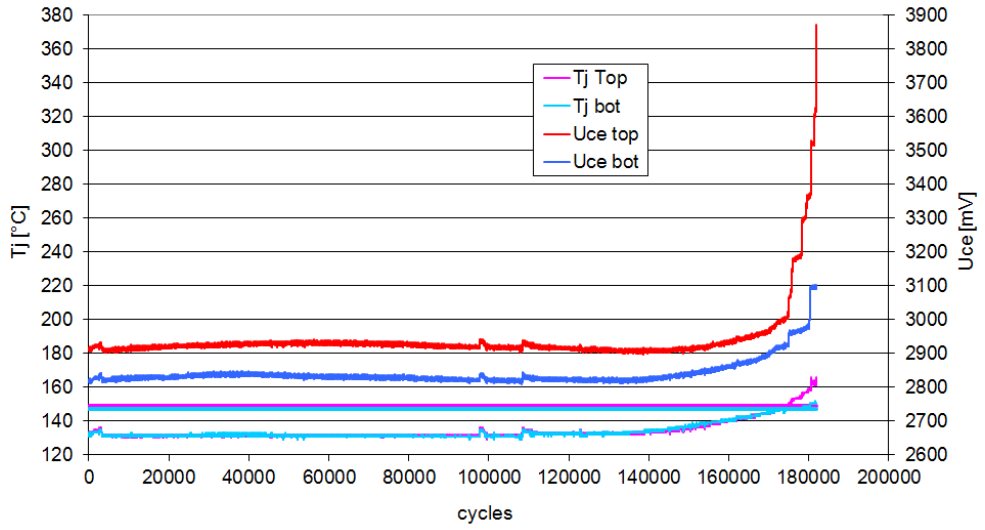

Figure 4.3: Collector-emitter voltage U_{CE} and junction temperature $T_{\mathrm{j}}(t)$ of two IGBTs in a half-bridge module as a function of power cycles. The bond wire lift-offs cause the steps; the slow increase in the voltage towards the end of the usable life is due to the solder layer degradation. In the test, ΔT_{j} was 80°C and T_{m} was 95°C.

The increase in both the collector-emitter voltage and the junction temperature can be used to define the end of life of a power module. In this work, a 20% increase in the chip temperature is chosen as the limit at which the module is considered to have reached its usable life.

4.2.3 Analytical lifetime models

The following analytical models do not take into account the order in which the temperature cycles occur. It is assumed that a small cycle has the same effect on the lifetime regardless of whether it occurred before or after a large cycle. However, there is no experimental data available about the issue of lifetime estimation accuracy in power electronics.

One of the commonly used analytical lifetime models in the power module lifetime estimation is based on Arrhenius model, known as the power-law (McPherson, 2010, p.41). The power-law states that the higher the temperature is, the higher the reaction rate is with an exponential factor

$$N_\mathrm{f} = e^{\left(\frac{Q}{R \cdot T}\right)}, \tag{4.1}$$

where $R = 8.31\mathrm{J/(K \cdot mol)}$ is the universal gas constant, T is the absolute temperature [K], and Q is the activation energy [J/mol]. The activation energy is the smallest energy that is required to start the reaction, and it is assumed to be independent of the temperature. In physics, the Boltzmann constant $k_\mathrm{B} = 1.38 \cdot 10^{-23}$ J/K is often used instead of the universal gas constant. In power cycling lifetime modeling, the temperature T is replaced with the mean temperature T_m. In addition, the activation energy has to be formulated as

$$E_\mathrm{a} = \frac{Q}{N_\mathrm{a}}, \tag{4.2}$$

where $N_\mathrm{a} = 6.022 \cdot 10^{23}$ 1/mol is the Avogadro number. The unit of the activation energy is now Joule [J].

The power-law model is modified by adding a term describing the effect of the temperature swing ΔT_j with an exponent α

$$N_\mathrm{f} = A \cdot (\Delta T_\mathrm{j})^{\alpha}\,. \tag{4.3}$$

In this case, the exponent α is negative, since the higher the temperature, the lower the lifetime is. Now, the two parts are combined to get a thermo-mechanical stress

model (Held et al., 1997)

$$N_\mathrm{f} = A \cdot (\Delta T_\mathrm{j})^{\alpha} \cdot e^{\left(\frac{E_\mathrm{a}}{k_\mathrm{B} \cdot T_\mathrm{m}}\right)}, \tag{4.4}$$

where A is a curve fitting constant. The coefficients A and α are acquired with curve fitting for the points of the experimental lifetime tests.

This model is useful in the lifetime estimation because it is relative simple, yet shows a good correlation with the measurement results by curve fitting. Nevertheless, it is not the most exact model as it does not take into account the cycle length. The relaxation time constant of the solder is in the range of a minute, whereas the time constant of the bond wire lift-off and the aluminum reconstruction is in the range of seconds (Ciappa, 2001). Cycles of certain length have an effect on the bond wire lift-off but not on the solder degradation. On the other hand, longer cycles have an effect on the solder degradation also. The cycle duration, or to be precise, the on-time, should be taken into account to correctly assess the individual failure mechanisms.

The Norris-Landzberg model takes into account the cycle frequency, which means in practice the cycle time (Norris and Landzberg, 1969):

$$N_\mathrm{f} = A \cdot f^{\beta} \cdot (\Delta T_\mathrm{j})^{\alpha} \cdot e^{\left(\frac{E_\mathrm{a}}{k_\mathrm{B} \cdot T_\mathrm{m}}\right)}, \tag{4.5}$$

where f is the cycle frequency and β a curve fitting constant. This is a good model to take into account the heating time t_{on}, which could have an effect on the lifetime. Ideally, it is close to an actual situation where the motor control dictates the current conduction time while the junction temperature is just a footnote per se. Nevertheless, it is inconvenient to add the heating time as a parameter in the lifetime tests, because it would require to control the heating time and the junction temperature swing at the same time.

Bayerer et al. (2008) have suggested a model that also takes into account the heating time t_on and the heating current I

$$N_\mathrm{f} = K \cdot (\Delta T_\mathrm{j})^{\beta_1} \cdot e^{\left(\frac{\beta_2}{T_\mathrm{max}}\right)} \cdot t_\mathrm{on}^{\beta_3} \cdot I^{\beta_4}, \tag{4.6}$$

where T_max is the maximum junction temperature in Kelvin degrees and K, β_1, β_2, β_3, and β_4 are curve fitting constants. The blocking voltage U and the bond wire diameter D can be taken into account by additional curve fitting constants β_5 and β_6. Also with this model there is the same inconvenience of too many parameters,

which cannot all be kept constant at the same time in the power cycling tests.

In this thesis, the modified Arrhenius model with Eq. (4.4) is used, because the wide use of the model establishes a common ground to compare the results of the research with other research results. Now, the lifetime can be plotted as a function of ΔT_j. Using the mean temperature T_m as a parameter, several curves can be plotted to achieve all the combinations of temperature swing and mean temperature.

An example of these curves is presented in Figure 4.4. The lifetime of the power modules of the 1990s was acquired from a study made in a project called LESIT (Held et al., 1997). The dots represent the measured values and the solid lines indicate the curves fitted to the measurements. Based on the results, A is 640, α is -5, and E_a is $1.3 \cdot 10^{-19}$ J.

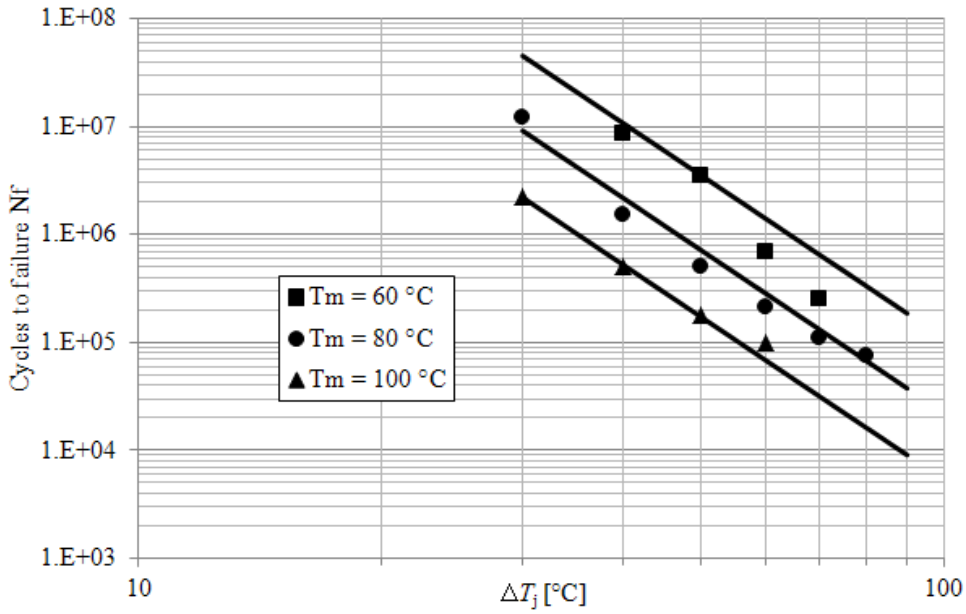

Figure 4.4: Power cycling lifetime of the base plate modules as a function of junction temperature swing ΔT_j and mean junction temperature T_m according to the results of the LESIT project (Held et al., 1997).

4.3 Lifetime test

Using real power cycles to test the lifetime of IGBT modules requires impractically long test times as the modules can withstand up to millions of cycles. The test can be accelerated by increasing the chip temperature swing, but there is a limit to the chip temperature. In addition, the failure mode activation depends on the temperature swing. Held et al. (1997) modified the power cycling test to investigate the bond wire lift-off by shortening the test cycles. Short cycles allow reasonable test times even with a high number of cycles. Held et al. (1997) installed the power module onto a liquid-cooled heat sink. The emitter voltage of the IGBT was permanently high to allow saturation, while the load current was controlled with an external circuitry. The junction temperature was measured periodically by applying a small measurement current and measuring the resulting collector emitter voltage U_{CE}. The measurement procedures described by Held et al. are used in this work where applicable.

The power cycling lifetime of a power module type Semitrans 2 SKM145GB123D was obtained by laboratory tests. The module is a half-bridge single-chip module with a copper base plate. The nominal current of the module is 100 A, and the blocking voltage of the chips is 1200 V (Semikron, 2007). The module under test was modified from a regular production version by replacing the solder between the DBC and the base plate with a lead-free alloy.

The tests were carried out with a mixture of the medium junction temperature T_{m} and the junction temperature swing ΔT_{j}. Each module was loaded with a single set of parameters as listed in Table 4.1.

Table 4.1: Lifetimes of tested modules. The modules were tested with varied settings for the junction temperature swing ΔT_{j} and the medium junction temperature T_{m}. The lifetime is expressed as a number of cycles N_{f} and as days and hours assuming a 30 s cycle time.

Module no	T_{m} [K] (°C)	ΔT_{j} [K]	N_{f}	duration
1	368 (95)	110	39 k	13 d 13 h
2	368 (95)	80	173 k	60 d 2 h
3	383 (110)	80	86 k	29 d 21 h
4	383 (110)	135	11.7 k	4 d 2 h

Opposed to the thermal model verification measurements, where the chip temperature was measured with a thermocouple, in this test, the chip temperature was measured by the TSP method. The collector-emitter voltage U_{CE} was the temperature sensitive parameter.

4.3.1 Parameter characterization

To set the control parameters of the power cycling test, the thermal parameters of the module under test must be identified first. The dependency of U_{CE} on the temperature and the thermal resistance R_{th} were measured by the following procedure.

The dependency of U_{CE} on the temperature with the coefficient k according to Eq. (3.1) was defined first. The module was attached to a liquid-cooled heat sink, and the temperature of the cooling liquid was controlled with an external heater/cooler. In the first phase, the heat sink was heated by the cooling liquid to thermal equilibrium, and the temperature of the heat sink was recorded. The heat sink and the whole module were assumed to be in a uniform temperature so that measuring the heat sink temperature also gave the chip temperature. Meanwhile, the collector-emitter voltage U_{CE} was measured by a 100 mA current, which is small enough not to cause self heating. The measurement was repeated at several temperatures to acquire the coefficient k. The collector-emitter voltage U_{CE0} at 0°C was acquired by extrapolation. The calibration plot of the coefficient k for the top-leg IGBT in one of the tested modules is presented in Figure 4.5. In this example, $k = -2.24\mathrm{mV/°C}$ and $U_{\mathrm{CE0}} = 580$ mV.

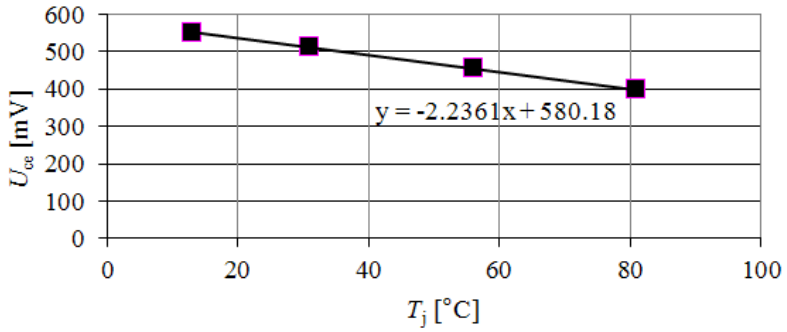

Figure 4.5: Measured U_{CE} (dots) versus the chip temperature T_j and a curve fitted to the measurements to determine the temperature dependency coefficient k at a 100 mA measurement current. The value of the coefficient is now -2.24 mV/°C, and the value for U_{CE} at a zero temperature is 580 mV.

After this calibration measurement, the junction temperature could be acquired at any stage according to Eq. (3.2) by measuring the U_{CE} by a 100 mA excitation

current.

Next, the thermal resistance was defined by heating the chip with a constant current and measuring the junction and base plate temperatures and the power loss of the chip. This time, the heat sink was cooled, and it was assumed that the heat sink is completely in a uniform temperature. The base plate temperature was measured underneath the chip by placing a thermocouple into a hole drilled through the heat sink. The current through the chip was constantly switched between the high load current and the small excitation current at a high enough frequency so that the chip did not cool during the measurement period, as illustrated in Figure 4.6.

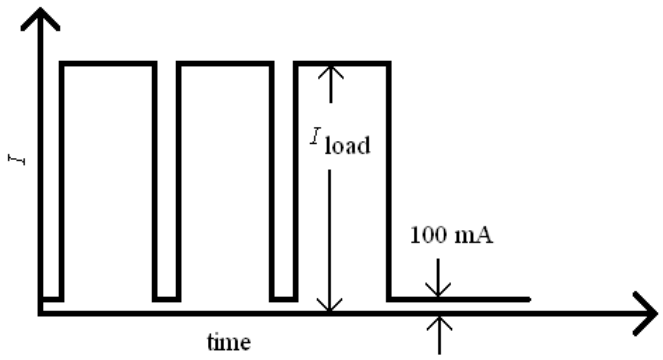

Figure 4.6: Load current and excitation current were cycled during the measurement of the thermal resistance. The power losses were calculated from the measured saturation voltage by the load current, and the chip temperature was measured from the collector-emitter voltage by the 100 mA excitation current.

The saturation value during the load current and the excited value during the measurement current of the U_{CE} were measured. The saturation voltage was used in the power loss calculations, while the voltage with the measurement current was used in the T_{j} calculations. The thermal resistance was calculated by Eq. (3.39).

4.3.2 Power cycling test

In the power cycling tests, the junction temperature swing ΔT_{j}, the mean junction temperature T_{m}, and the heating and cooling times were controlled. The chips were loaded internally by a controlled current source.

During the power cycling tests, the two IGBTs of the half bridge were connected in series. They were switched on permanently and the constant DC load current was switched on and off by an external switch. The diodes were not loaded at all. The collector-emitter voltage of the top-leg and bottom-leg IGBTs were measured using a four-cable configuration to eliminate the parasitic voltage drop of the cables. The power losses were determined during the heating phase by measuring the collector-emitter saturation voltage. The junction temperatures of the IGBTs were measured at the beginning of the cooling phase with a 100 mA excitation current.

The target junction temperature is adjusted based on the measured value of the thermal resistance of the chip. This is carried out as follows: The conduction power loss P_{cond} of the TOP IGBT chip was measured at $T_{\mathrm{j}}(t)$ of 150°C with a nominal collector current. The resulting case temperature $T_{\mathrm{c}}(t)$ was calculated by using the datasheet value for the thermal resistance R_{th}:

$$T_{\mathrm{c}} = T_{\mathrm{j}} - P_{\mathrm{loss}} \cdot R_{\mathrm{th(datasheet)}} \tag{4.7}$$

Next, the target junction temperature was calculated based on the measured power losses and the measured value of the thermal resistance

$$T_{\mathrm{j(target)}} = T_{\mathrm{c}} + P_{\mathrm{loss}} \cdot R_{\mathrm{th(meas)}} \tag{4.8}$$

This procedure establishes identical test conditions for an industrial series product. The thermal resistance for individual modules varies within an interval because of material tolerances. If the thermal resistance of an individual module is close to the maximum thermal resistance given in the datasheet, the target junction temperature is equal to the maximum junction temperature defined by the swing ΔT_{j}. However, if the thermal resistance of the individual module is smaller, the target junction temperature will also be smaller. This philosophy is consistent with the situation in an actual application, where the modules are not selected according to their thermal resistance but they are used according to the datasheet specification (Scheuermann and Hecht, 2002).

The heating and cooling phases were controlled with a thermocouple soldered on the side of the base plate, close to the top-leg IGBT. The limits for the maximum and minimum values for the case temperature were set such that the junction temperature will reach the maximum and minimum target value in the heating and cooling phases, respectively. After the maximum base plate temperature is reached, the load current is turned off and the coolant flow is turned on. The load current is turned

on and the coolant flow is turned off again after the reference point temperature has reached the minimum. The initial cycle time was 30 s.

In this work, the end of lifetime of a power module is defined as a 20% increase in the junction temperature swing. This was not a predefined trigger to stop the tests, but instead, the tests were stopped only after the module failed completely and could not conduct any current. The specification limit of a 20% increase in the junction temperature swing is taken into account when the test data is postprocessed.

The results of the module number 1 are presented as an example of the analysis of the end-of-life phenomena. The test ended after 40 700 cycles, which took 14 days and 3 hours, and the lifetime with the definition of a 20% increase in the junction temperature swing was 39 000 cycles. The maximum junction temperature and the collector-emitter saturation voltage of the BOT IGBT started to slowly increase already before this point. This indicates that the solder layer of the bottom switch has started to deteriorate. This increases the thermal resistance of the chip, which again, increases the junction temperature, which accelerates the solder layer weakening further. There are no sharp steps in the saturation voltage, and thus, there is no evidence of the bond wire lift-off. The junction temperature and the collector-emitter saturation voltage of both the top and bottom IGBTs for the module number 1 are shown in Figure 4.7.

A scanning acoustic microscope (SAM) image was taken of the module before and after the power cycling test. An image of the solder layer between the chip and the DBC substrate is presented in Figure 4.8.

The solder layer fatigue can be identified by the pale area in the image taken after the power cycling test. The reflected acoustic signal indicates microscopic cracks and delamination in the solder layer. The integrity of the bondings was also tested by a bond shear test and by visual inspection. The shear stress values for the TOP IGBT were between 160 and 460 g. Most of the bond wires on the BOT IGBT were lifted off, and for the rest (six bonds were tested), the values were between 186 and 560 g.

The analysis shows that the module failed because of solder fatigue, which caused a higher junction temperature and finally led to the bond wire lift-off.

Now, it is possible to plot the lifetime curves as a function of junction temperature swing. The curves are fitted to the measurements by the least mean square method.

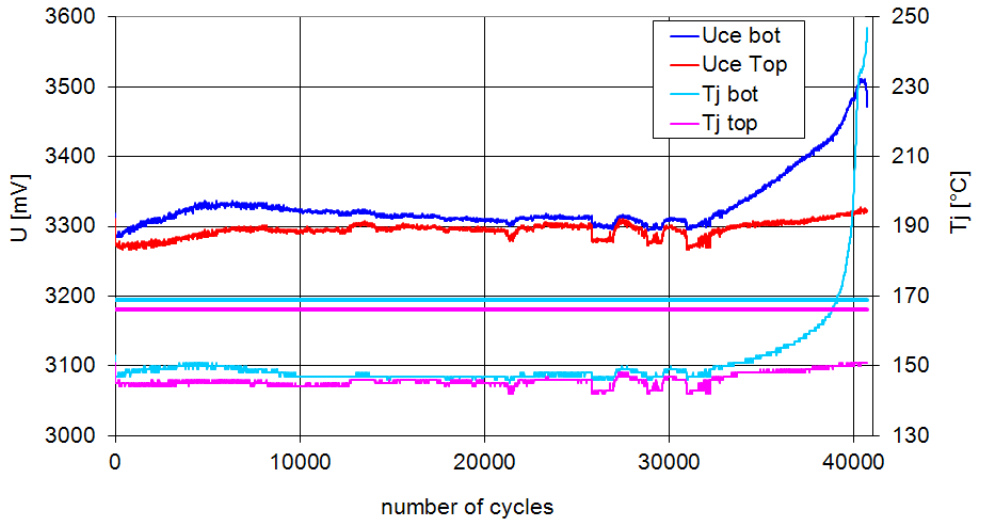

Figure 4.7: Collector-emitter voltage U_{CE} and junction temperature $T_{\mathrm{j}}(t)$ of two IGBTs in a half-bridge module as a function of power cycles. The two straight lines indicate a 20 % increase in the junction temperatures. In the test, ΔT_{j} was 110°C and T_{m} was 95°C.

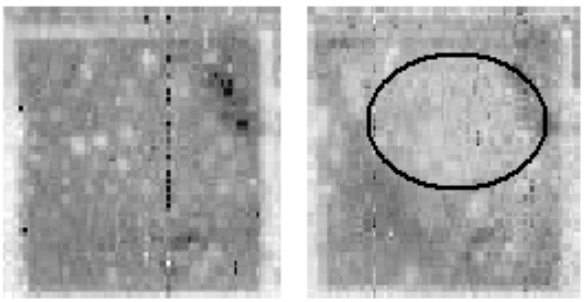

Figure 4.8: Scanning acoustic microscope image of the solder layer between the IGBT chip and the DCB substrate before (left) and after (right) the power cycling test. The pale area highlighted in the image after the power cycling test shows the fatigued solder.

Based on the test results, A is 7180, α is -5, and E_{a} is $1.3 \cdot 10^{-19}$ J. The scaling factor A is now 7180, which is more than ten times as high as according to the study by (Held et al., 1997), 640. The lifetime curves are presented in Figure 4.9 with the medium junction temperature as a parameter (Ikonen et al., 2007).

The lifetime curves could be extrapolated to even higher temperature swings, but there is no measurement data to confirm the plots. The test condition of $\Delta T_{\mathrm{j}} = 135$°C

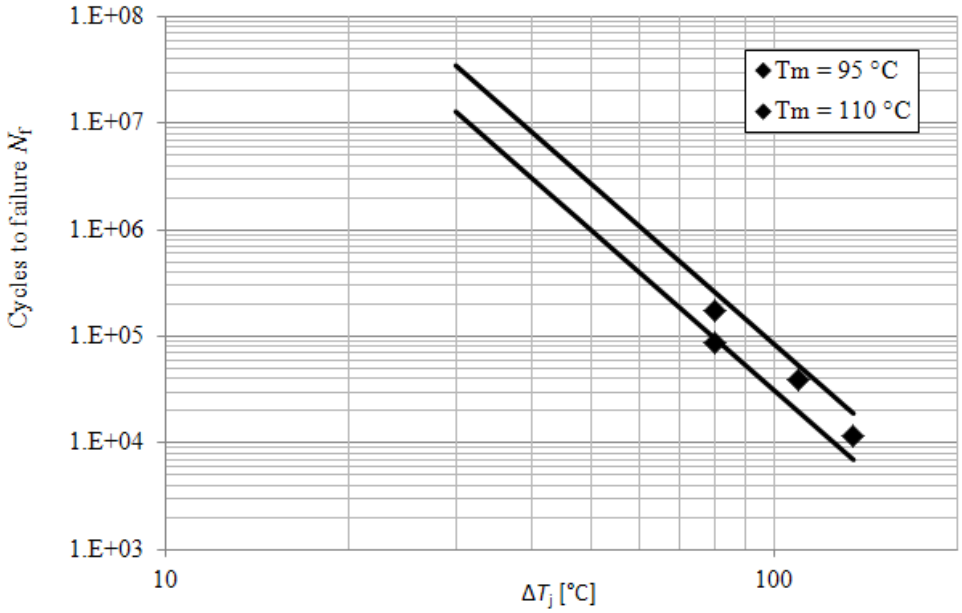

Figure 4.9: Module lifetime as a function of junction temperature swing ΔT_j and medium temperature of the junction T_m. The points represent measurements while the solid lines represent curve fitting of the lifetime model. The measurements are made by accelerated power cycling tests.

refers to the increased maximum junction temperature of 175°C, which is a general trend for IGBT power modules. As the results show, this increase has a considerable impact on the module lifetime since the higher the temperature swing goes, the lower the lifetime is.

4.4 Failure prediction

The progress of degradation can be calculated after the nominal lifetime of the module is measured with accelerated tests. The number and type of cycles that the device has endured are calculated from the mission profile of the device. The mission profile is either measured or estimated. It can be output power, current, power loss, heat sink temperature, or chip temperature. Usually, the output current or output power is available from the device controller, and thus, these are convenient to be used. However, to calculate the life consumption of the device, the chip temperature has to be used, since it is the dominant parameter after all. It can be calculated from

the output power or current by a thermal model presented previously.

4.4.1 Cycle counting from the mission profile

The chip temperature is typically arbitrary in inverter applications. For instance in wind turbines, the wind speed is often varying over time without any clear repeating pattern. If the wind speed is below the nominal speed of the turbine, the output power of the turbine is dependent on the wind speed. Output power variation causes similar variations in the junction temperature. Each temperature cycle is unique in terms of amplitude and duration. This calls for a method to find the cycles from the junction temperature curve, and to find the correlation between each cycle and the module degradation.

In this work, the temperature cycles are counted with a rainflow counting algorithm. Rainflow algorithm is one of the methods to count the cycles from a mission profile (ASTM, 2011). It is based on an idea that the mission profile is like a pagoda with rainwater flowing down the roof. A deeper analysis of the rainflow method is not in the scope of this work, but the principle is only explained in brief. In the rainflow method, half-cycles are searched from the data according to the specific rules of the method. A rainflow toolbox is used in this work (Nieslony, 2009).

The cycles are searched with water dropping off the peaks of the mission profile in both sides. In Figure 4.10, six half-cycles are detected by the rainflow method. The first cycle A starts from the bottom. It travels until a valley lower than the start value is found. Cycle B starts from the peak on the other side, and it travels until a value higher than the start value is found. Cycle C starts from a valley and ends when it intersects with another cycle falling off from a higher peak. Cycle D starts at the highest value, and it ends when a higher peak occurs. Similarly, cycle E starts from a peak and ends on a higher peak. Cycle F starts from a valley and ends after intersecting with another cycle. This continues until all the turning points in the mission profile are found. Then, the half-cycles are categorized to bins to an m x n matrix according to the selected resolution.

A simulated mission profile of the wind turbine is used once again to demonstrate the cycle counting. An IGBT chip temperature is presented in Figure 4.11, and the cycles according to the rainflow counting method are shown in Figure 4.12. The cycles are divided into bins according to the temperature swing and the mean temperature in a 20 x 20 matrix.

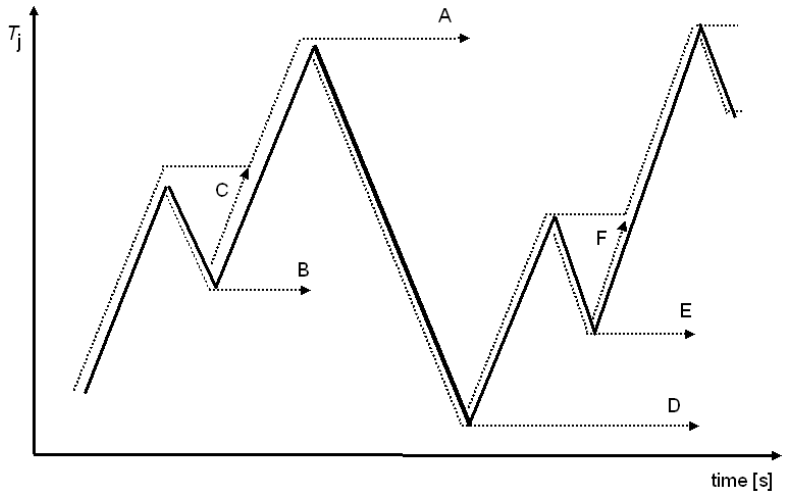

Figure 4.10: Half-cycles A to F in a mission profile detected by the rainflow method.

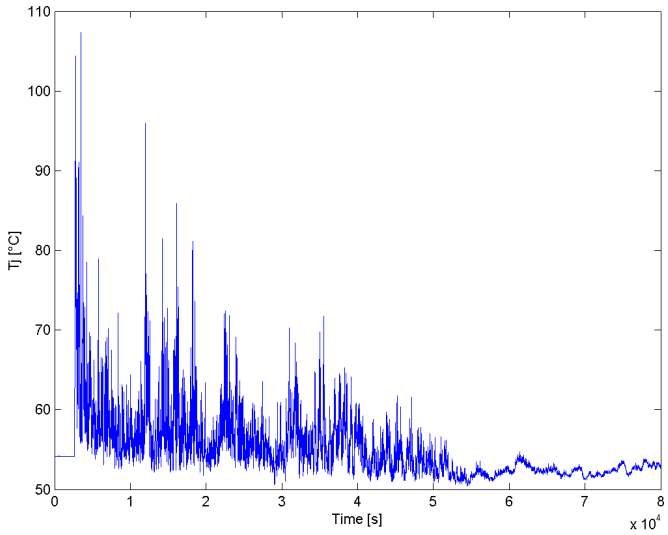

Figure 4.11: Simulated IGBT chip temperature in the wind turbine over 24 hours.

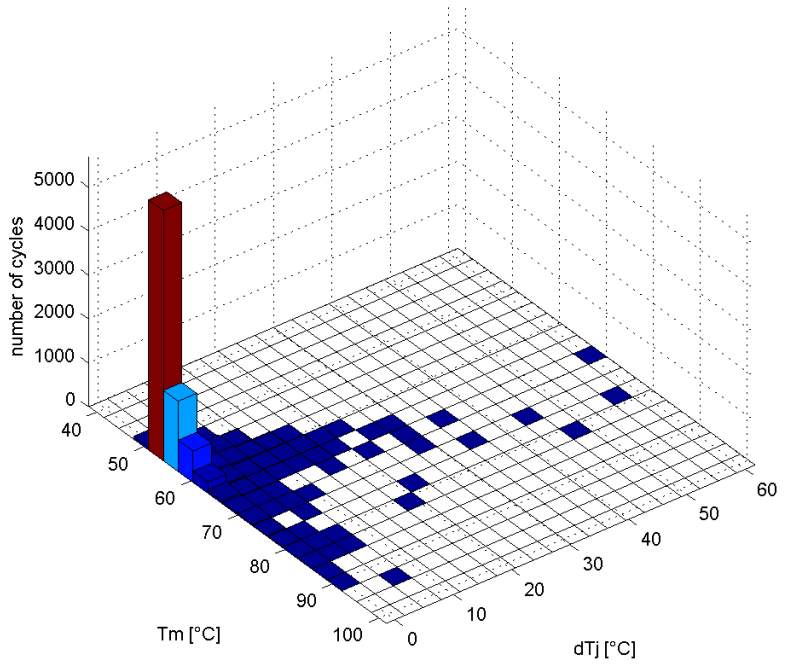

Figure 4.12: Cycles found in the IGBT chip temperature in the wind turbine within a 24 hour period.

4.4.2 Lifetime consumption

It is assumed that the damage is linearly accumulated so that the order in which the cycles occur does not have an effect on the life consumption of the cycles. The cycle lifetime can be divided into partial lifetimes for each cycle amplitude and mean value. The consumptions are summed up to achieve the total life consumption (LC). Miner's rule can be used to predict the failure (Musallam et al., 2008)

$$\mathrm{LC} = \sum_{i,j=1}^{n} \frac{N_{(i,j)}}{N_{\mathrm{f}(i,j)}}, \tag{4.9}$$

where $N_{i,j}$ is the number of cycles in each bin, i and j are the indices of the bin, and $N_{\mathrm{f}(i,j)}$ is the measured lifetime. The failure occurs when LC = 1.

Continuing the example in the previous subsection, the number of cycles in the mission profile with parameters $T_{\mathrm{m}} = 52$ and $\Delta T_{\mathrm{j}} = 1$ is $N_{52,1} = 5695$. Similarly, with $T_{\mathrm{m}} = 82$ and $\Delta T_{\mathrm{j}} = 48$, the number of cycles $N_{82,48}$ is 1.

On the other hand, the measured lifetime N_f for every bin is calculated using Eq. (4.4). Remembering that A is 7180, α is -5, and E_a is $1,3 \cdot 10^{-19}$ J, we get the lifetime $N_{\mathrm{f}(55,1)} = 2.47 \cdot 10^{16}$ and $N_{\mathrm{f}(82,48)} = 8.44 \cdot 10^{6}$. It follows that

$$LC_{(55,1)} = \frac{N_{(55,1)}}{N_{\mathrm{f}(55,1)}} = 2.3 \cdot 10^{-13} \tag{4.10}$$

and

$$LC_{(82,48)} = \frac{N_{(82,48)}}{N_{\mathrm{f}(82,48)}} = 1.2 \cdot 10^{-7}. \tag{4.11}$$

The same procedure is repeated for each bin of the temperature cycle matrix in Figure 4.12 to get a lifetime consumption matrix, which is presented Figure 4.13. After the life consumption of each bin has been calculated, the results are added up to acquire the total life consumption. In this example, the LC is $4.8 \cdot 10^{-5}\%$ of the available life.

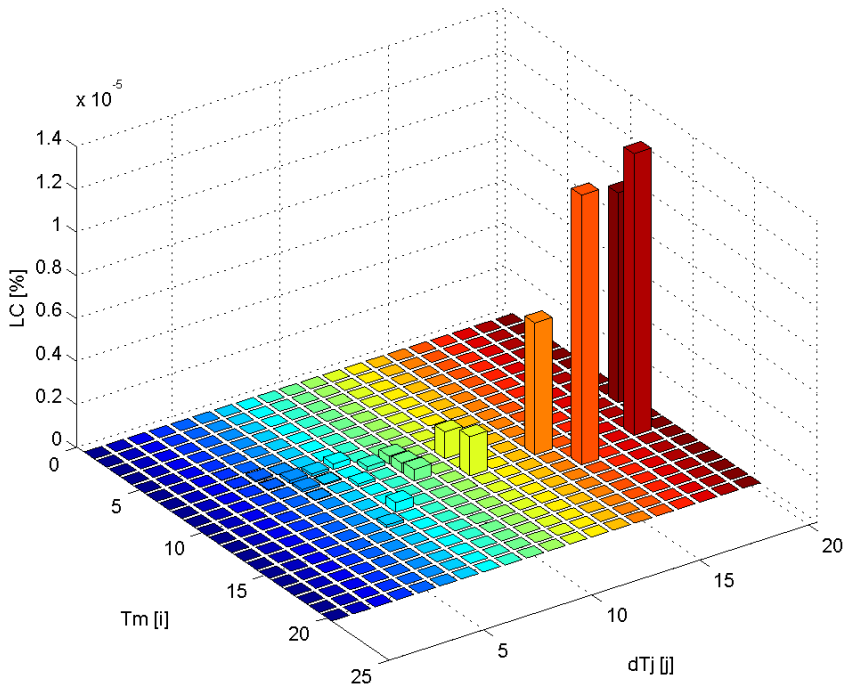

Figure 4.13: Consumption of available life in percents for each bin.

The figure shows that even a small number of power cycles at a high ΔT_j or a high T_m have a higher effect on the lifetime than a high number of cycles at lower temperatures. The lifetime curve is counterexponential so that the higher the chip

temperature swing is, the lower the lifetime is. The same applies to the medium chip temperature.

4.5 Lifetime estimation of an IGBT module in a wind turbine

The lifetime of an IGBT chip in the grid-side converter of a direct-driven wind turbine was taken as a case study. The direct-driven type of a wind turbine was selected because it is among the most popular types of turbines at the moment (Polinder, 2011). On the other hand, the full power converter technology has been in use in a large scale only for a few years. There is only small amount of empirical data on the failure rates of the direct-driven turbines of a multimegawatt scale. Most of the failure data are of low-power turbines. Furthermore, even though sintered modules are the most reliable power modules today, a significant number of the installed PMSG wind turbines are equipped with power modules with the DBC technology, solder layers, and bond wires. This gives motivation for a study of the power cycling lifetime of the IGBT modules with the DBC technology in multimegawatt direct-driven wind turbines.

Spinato et al. (2009) reviewed the failures of wind turbines in Denmark and Germany. They found that the power converters have a higher failure rate in wind power applications than in other industries. However, the reason is not given. Moreover, according to their study, the converter has the third highest failure rate of the subassemblies in a turbine, after the electrical system and the rotor.

Pittini et al. (2011) studied the thermal load of the IGBT module in a direct-driven offshore wind turbine by simulations. They used a 3.6 MW turbine and a 5 MVA converter in the circuit simulator software. The thermal load of the power module was simulated at various output power levels. However, they did not make any statement about the lifetime of the IGBT module based on the simulations.

Bohlländer et al. (2011) analyzed the cycles found in an offshore turbine output power during a measurement period of two weeks. The cycles were analyzed from two locations onshore in Norway. They used the presented rainflow counting method to extract the cycles. A commercially available converter was chosen for the chip temperature simulations. The cycle numbers of the two turbines were plotted and

compared with each other. It was found that the cycle count at higher ΔT_j differs significantly according to the location of the measurement place. Bohlländer et al. (2011) conclude that thus, the location has an effect on the failure mechanisms. However, there were only a small number cycles above $50°C$ and no cycles above $80°C$. The duration of the cycles was mostly over 10 s. The study does not give the actual lifetime of the IGBT module either.

In this study, the power cycling lifetime of an IGBT module in a direct-driven wind turbine is estimated based on wind measurements in Finland. The lifetime assessment procedure is illustrated in Figure 4.14. First, the turbine output power is simulated based on measured wind data. The wind measurement data is provided by the Finnish Meteorological Institute. The turbine output power is simulated by a turbine model from the National Renewable Energy Laboratory (NREL), USA. From the output power, the IGBT chip power losses and the temperature in the grid-side converter are simulated by a thermal model. Then, the temperature cycles are counted from the measured temperature by a rainflow counting algorithm. Last, the cycle count is compared with the lifetime measured in laboratory tests.

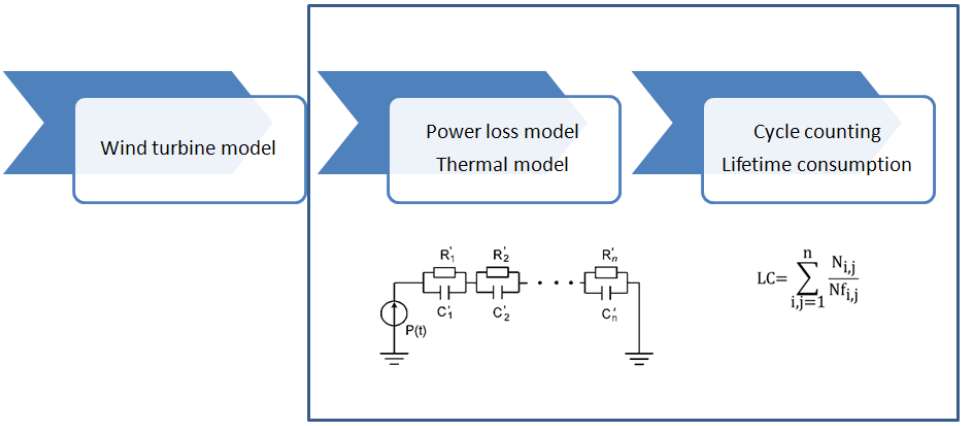

Figure 4.14: Wind turbine lifetime estimation starts with the turbine output power estimation based on the measured wind speed.

4.5.1 Studied wind turbine

In a direct-driven turbine, the permanent magnet synchronous generator (PMSG) is connected to the grid via a frequency converter. The nominal power of the frequency converter is the same as the nominal power of the turbine, and thus, it is called a

full power converter. This is opposite to the double-fed induction generator turbine type (DFIG), where only the magnetization current of the generator is fed through the frequency converter. Typically, in a DFIG turbine, the nominal power of the converter is one-third of the nominal power of the turbine. The advantages of the direct-driven turbine are the wider range of turbine speed independent of the grid frequency or the phase angle, and the capability to support the grid voltage during a fault with reactive current. The drawbacks of this type of a turbine are the unknown mean-time-to-failure because of the immature technology and the availability problems of the rear earth magnet materials used in the generators (Polinder, 2011).

The full power converter has a rectifier, called the generator-side converter, and an inverter, called the grid-side converter, presented in Figure 4.15. The input frequency of the generator-side converter is in the range of 10 to 100 Hz, depending on the drive train construction. The output frequency of the grid side is either 50 Hz or 60 Hz.

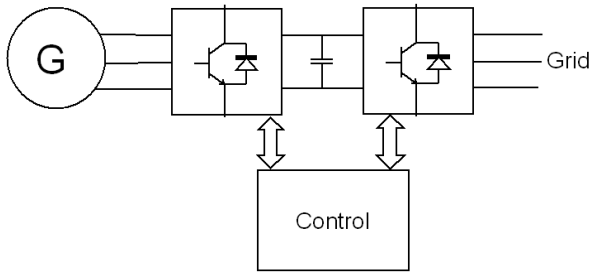

Figure 4.15: Schematic of the direct-driven wind turbine. Both the rectifier and the inverter are implemented with IGBTs.

In this doctoral thesis, the power cycling lifetime of the grid side converter is studied. The mission profile has a strong effect on the grid side converter, and hence it is a good object to validate the lifetime estimation methods. The lifetime of the generator side converter, on the other hand, is influenced strongly by the rotation speed of the generator. The thermal cycles in the IGBT due to the generator rotation speed are short, which gives requirements of high eccuracy of the thermal parameters of the thermal model. Those parameters are strongly dependent on the cooling system, and they are inaccessible in this case, and therefore, the generator side converter is not applicable for this study. However, the same lifetime estimation methods can be applied to the generator side converter, if there is a possibility to define the thermal parameters accurately.

The turbine simulation is not in the scope of this thesis; however, the turbine is discussed here in brief. The turbine output power simulations are done by Elvira Baygildina, M.Sc. The wind turbine model is based on a 1.5 MW direct-driven permanent magnet generator with a full power converter. The wind turbine is designed to the medium wind speed of 8.5 m/s, which makes it an IEC class II wind turbine (IEC, 2005). The aerodynamic efficiency of the turbine is highest at this speed.

The turbine height is 84 m and the rotor diameter is 70 m. The blades are pitched according to wind speed to acquire the highest possible amount of energy when the wind speed is above nominal. The cut-in wind speed is 3 m/s and nominal power is generated at a 12 m/s wind speed. The cut-off wind speed is 27.6 m/s (Poore and Lettenmaier, 2003). The generator torque as a function of rotation speed is presented in Figure 4.16.

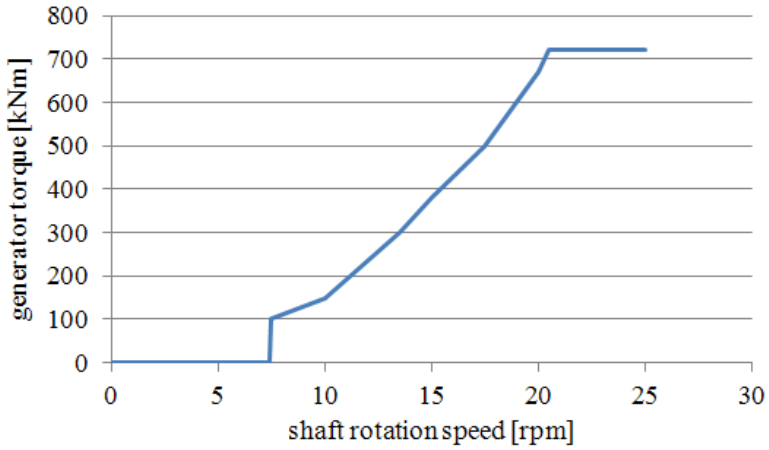

Figure 4.16: Wind turbine speed-torque curve. The cut-in wind speed is 3 m/s, which is 7 rpm of the shaft. The nominal power is produced at a 11.5 m/s wind speed, which is 21 rpm of the shaft (Poore and Lettenmaier, 2003).

For this study, an exemplary converter was designed based on the output power level of the turbine. This is due to the fact that the exact features of commercial turbine converters are trade secrets, and thus, not applicable for academic study. However, the main features of the converter can be designed with publicly available information from the IGBT module manufacturers.

A liquid-cooled SKiiP 2403GB172-4DW from Semikron was selected as the grid-side

converter module. It is a 2-pack module consisting of both the IGBTs and diodes of a single phase. The module is made of four submodules connected in parallel. The nominal current at a 25°C heat sink temperature is 2400 A and the nominal blocking voltage is 1700 V. For a 70°C heat sink temperature, the nominal current is 1600 A.

4.5.2 Thermal modeling of the grid-side converter

A model was constructed in Simulink to simulate the thermal behavior of an IGBT in the grid-side converter of a wind turbine. Switching losses depend on the peak value of the output current $\hat{i}$

$$P_{\mathrm{sw}} = \frac{1}{\pi} \cdot f_{sw} \cdot \left(E_{\mathrm{on}} \left(\hat{i} \right) + E_{\mathrm{off}} \left(\hat{i} \right) \right), \tag{4.12}$$

where f_{sw} is the switching frequency of the IGBT. The switching losses are described with a look-up table in the model with the current as an input, whereas the switching frequency is given as a constant. The values in the table were acquired from the module datasheet (Semikron, 2009). The switching frequency was set to 3 kHz.

On-state losses also depend on the modulation index m and the power factor $\cos\phi$ of the converter (Mestha and Evans, 1989)

$$P_{\mathrm{on}} = \frac{1}{2} \cdot \left(\frac{U_{\mathrm{ce0}}}{\pi} \cdot \hat{i} + \frac{r_{\mathrm{ce}}}{4} \cdot \hat{i}^2 \right) + m \cdot \cos\phi \cdot \left(\frac{U_{\mathrm{ce0}}}{8} \cdot \hat{i} + \frac{r_{ce}}{3\pi} \cdot \hat{i}^2 \right), \tag{4.13}$$

where U_{ce0} is the threshold voltage and r_{ce} is the on-state resistance. Both are temperature dependent, and therefore, they are described with a look-up table with the chip temperature fed back to the Simulink model. In this case, the power factor was assumed to be 1.

The phase current was calculated from the output power assuming the nominal grid voltage to be stable 690 V

$$i = \frac{P}{690\sqrt{3}}. \tag{4.14}$$

Both the effective and peak values were calculated. The modulation index was calculated by normalizing the effective phase current value to the nominal output current of the converter

$$m = \frac{i}{i_{\mathrm{nom}}}, \tag{4.15}$$

where i_{nom} is now 1255 A.

After summing these power losses together, the ΔT_j of the chip is calculated based on the thermal resistances of the module. Thermal capacitances were neglected to simplify the simulation model and to speed up the simulation. Most of the thermal time constants of the module are under 1 s, while the simulated output power of the turbine changes with time constants longer than 10 s. According to the datasheet, the total thermal resistance of this module is 0.0195 K/W. The heat sink temperature is added to the calculated ΔT_j to estimate the chip temperature. The ambient temperature is estimated to be 40°C and the liquid temperature difference to the ambient 10°C leading to a 50°C heat sink temperature. The Simulink model is shown in Figure 4.17.

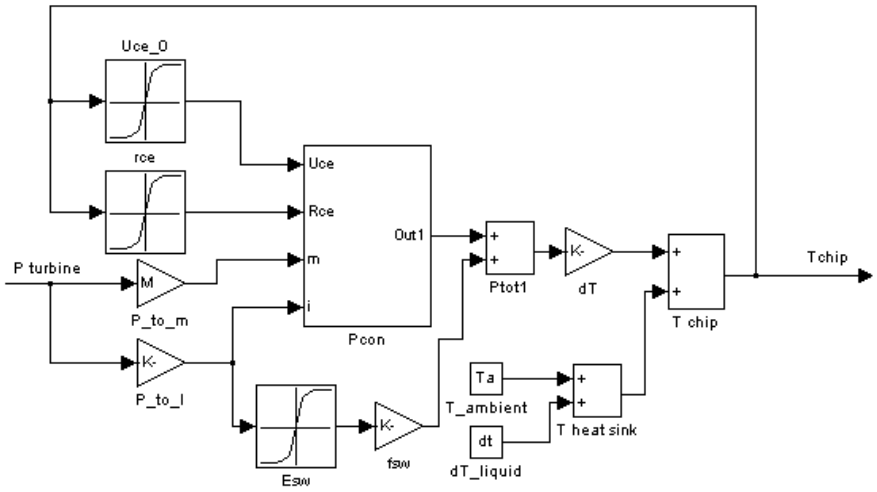

Figure 4.17: Thermal model of the grid-side converter in Simulink. Thermal modeling is based on the instantaneous output power of the turbine.

4.5.3 Wind measurement

To make a reliable estimation of the power cycling lifetime, the time resolution of the mission profile data must be 10 s or better to find the cycles. The average wind speed is not enough. This significantly limits the available data, since in many cases only the average wind speed, such as a 10 minute average, is logged. With the 10 min average wind speed, the short cycles would be smoothed out from the output power data. In this study, the data logged with a 1 s resolution was used to simulate the output power to find all the cycles present in the output power. The required time resolution was determined not only by the wind speed but also by the inertia

of the blades and the generator and by the control parameters of the turbine.

The wind data were provided by Tuulisaimaa Oy, and the wind measurements were carried out by the Finnish Meteorological Institute. The measurements were carried out on an onshore site in eastern Finland near Lake Saimaa. Lake Saimaa with the nearby Lake Ladoga in Russia influences the climate in the region by cooling the temperature in spring and warming in autumn. Lake Saimaa is 50 km measured from north to south and 80 km from east to west. The yearly average of the wind speed on the measurement site is around 7 m/s (Tuuliatlas, 2011).

Wind data were measured with LIDAR at altitudes of 80–140 m with a 20 m interval. LIDAR is a measurement instrument based on sending laser pulses to the air and measuring the reflected light intensity and/or frequency shift caused by the Doppler phenomenon. It can, in theory, measure wind speed up to a 300 m height. In this study, however, the altitudes of 80–140 m are relevant for the wind turbine, and therefore, this range was selected. Wind speed with each height was recorded at a 1 s interval and as a 10 min average.

4.5.4 IGBT chip lifetime

The IGBT chip temperature was simulated as 24 hour fragments. One fragment of each month was selected to represent the wind condition of that month. The simulated output power of the turbine in December 2011 over the period of 24 hours is presented in Figure 4.18 and the simulated IGBT chip temperature during the same period in Figure 4.19.

The output power plot shows that the output power seldom reaches the nominal power of 1.5 MW. There are a lot of small cycles in the output power. Similarly, there are numerous small cycles in the chip temperature. The chip temperature is under 110°C all the time, which leaves a wide margin for the allowed chip temperature. According to the datasheet, the maximum chip temperature is 150°C.

The cycles were counted from each 24 hour data sample by the rainflow algorithm. The cycles were categorized into bins with a 3°C resolution. For ΔT_j, the range was from 1°C to 60°C, and for T_m, the range was from 40°C to 100°C. The lifetime consumption for each bin was calculated by comparing the cycle count to the measured lifetime. The lifetime consumption follows the same procedure as presented Section 4.4.

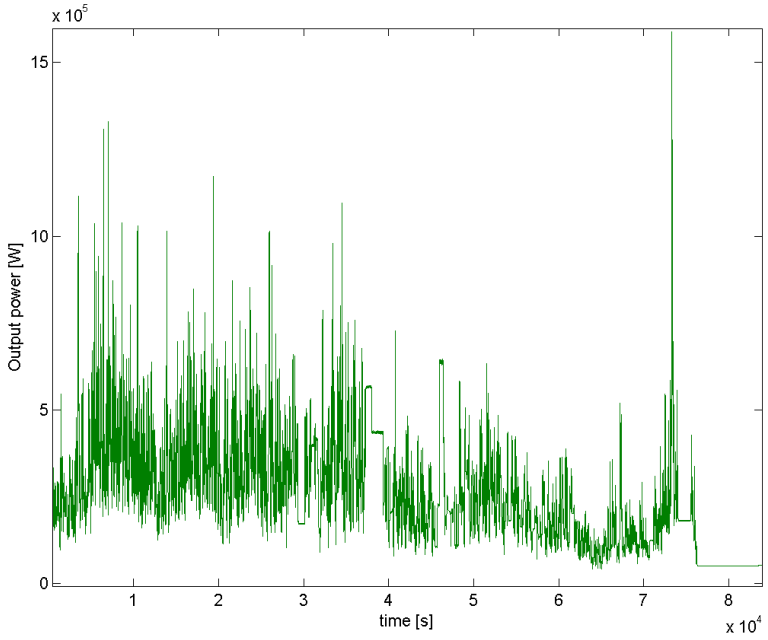

Figure 4.18: Simulated output power of the turbine in December 2011 over a period of 24 hours.

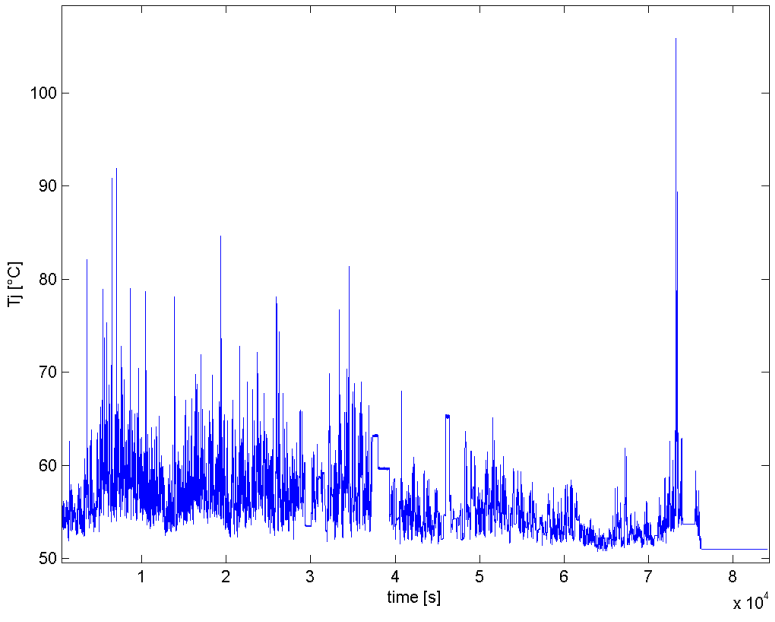

Figure 4.19: Simulated IGBT chip temperature in the wind turbine in December 2011 over a period of 24 hours.

The cycle matrix for one day in December is presented in Figure 4.20. There are a lot of small cycles at low and medium temperatures, but only a few cycles at higher temperatures. The lifetime consumption matrix is presented in Figure 4.21. The high number of cycles at low temperatures have no effect on the lifetime, whereas the small number of cycles at the higher temperatures have a noticeable effect. The sum of the bins in the matrix is $3.27 \cdot 10^{-5}\%$ for the 24 hour period, which gives LC $= 1.01 \cdot 10^{-03}\%$ for the whole month.

The same procedure was repeated for each month, and the yearly lifetime consumption was calculated by summing the lifetime consumption of each month. The lifetime consumption of each month is presented in Table 4.2.

Table 4.2: Estimated lifetime consumption in each month of an IGBT in a 1.5 MW turbine. The estimation is based on wind measurements in south-eastern Finland.

month	LC [%]
January	$4.25 \cdot 10^{-07}$
February	$4.12 \cdot 10^{-07}$
March	$1.48 \cdot 10^{-03}$
April	$2.21 \cdot 10^{-06}$
May	$8.80 \cdot 10^{-05}$
June	$6.06 \cdot 10^{-06}$
July	$6.82 \cdot 10^{-08}$
August	$2.80 \cdot 10^{-03}$
September	$2.17 \cdot 10^{-05}$
October	$5.43 \cdot 10^{-04}$
November	$5.25 \cdot 10^{-04}$
December	$1.01 \cdot 10^{-03}$
Total	$6.48 \cdot 10^{-03}$

The total lifetime consumption in one year is $6.48 \cdot 10^{-03}\%$ of the available life. This means a 15 000-year life for the IGBT in this application on this site.

4.6 Discussion

It was found that even a small number of power cycles at high ΔT_j or high T_m have a more significant effect on the lifetime than a high number of cycles at lower temperatures. It is therefore important to minimize the power cycles at high temperatures. It could be done online by a smart control of the IGBT chip temperature, for example by reducing the switching frequency. This, however, would require another study on

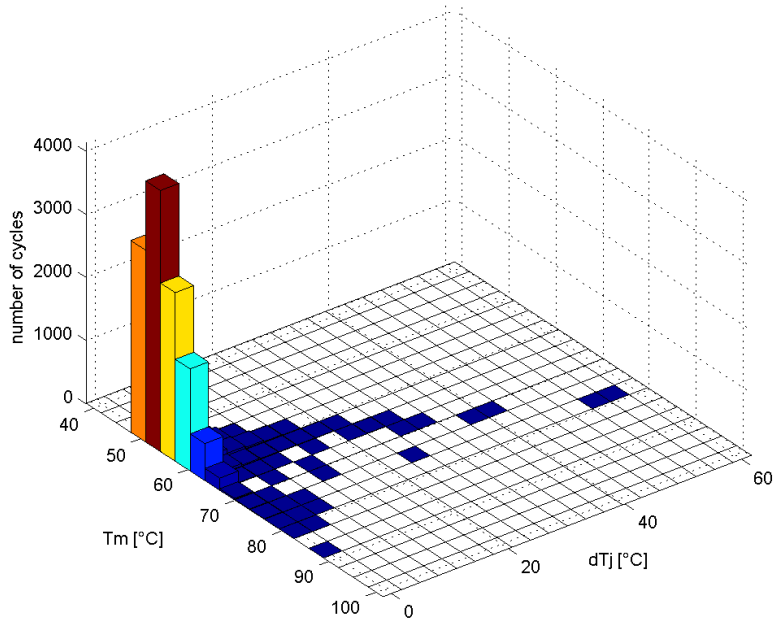

Figure 4.20: Cycles found in the IGBT chip temperature in the wind turbine in December 2011 within a period of 24 hours.

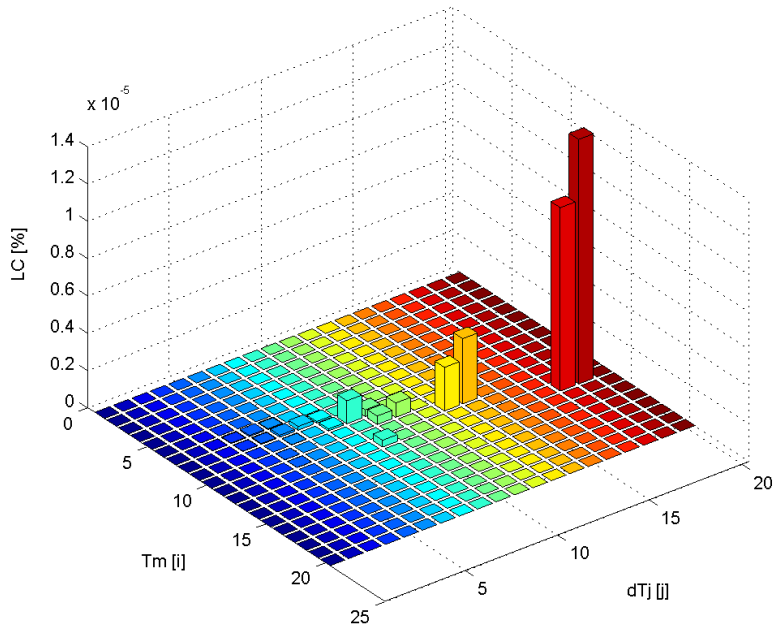

Figure 4.21: Consumption of available life in per cents for each bin over a period of 24 hours in December.

how to control the chip temperatures in order to increase the lifetime by thermal modeling and life consumption calculation.

Furthermore, because the lifetime is inverse-exponentially dependent on the temperature cycle amplitude, there is a great demand for the accuracy of the power loss estimation and for the thermal parameter characterization in the thermal modeling. A 10% error in the power loss estimation would cause an equal error in the temperature estimation. Increasing the ΔT_j, and thus also the T_m by 5%, would mean the lifetime to halve. For example, at $\Delta T_\mathrm{j} = 100°\mathrm{C}$ and $T_\mathrm{m} = 100°\mathrm{C}$, the lifetime is 60 000 cycles. If the temperature is increased by 10% to $\Delta T_\mathrm{j} = 110°\mathrm{C}$ and $T_\mathrm{m} = 105°\mathrm{C}$, the lifetime is 24 400 cycles.

4.6.1 Power cycling test

The slope of the lifetime curves does not correlate perfectly with the measurement results. This could be due to the fact that the activation energy of the breaking mechanism changes with the solder material. A further subject of study could also be to fit the activation energy to the measurement results to get a better agreement with the lifetime curves. However, the presented results do not constitute a sufficient database for this interpretation. Finding the correct value for the activation energy is not in the scope of this work.

The test was performed by only using one single value for the junction temperature swing ΔT_j and the medium junction temperature T_m for each module. A further relevant subject of study could be to investigate how changing the settings during the power cycling test influences the lifetime of the modules; also testing with a lower ΔT_j is worth considering. However, because of the long lifetime, the test would take years to complete even with an accelerated test.

Power cycling lifetime tests of this kind are used as an indicator of the power module lifetime. There are certain differences between the accelerated tests and the real-life chip temperature behavior. In the real life, the duration of the temperature cycle is not always constant nor is the case temperature controlled. In these tests, power is cut off after the threshold level of the case temperature is reached. In an actual application, the power is not cut off based on the module temperature but based on the control of the whole drive.

Accelerated tests together with the analytical model of Eq. (4.4) can be used to make

comparisons between the modules and to observe the effect of different $\Delta T_\mathrm{j}/T_\mathrm{m}$ combinations on the lifetime. The results can also be used to compare the available module lifetime in varied load conditions.

Based on the results of the power cycling tests made by the author, the selected model describes well the power cycling lifetime with different values of ΔT_j. The results are valid for the module technology with silicon chips, aluminum oxide ceramics, copper base plates, and lead-free solder.

To compare the lifetime of the modern modules with the lifetime of the modules ten years ago, it suffices to compare the scaling factor A of Eq. (4.4). Held et al. (1997) studied the lifetime of state-of-art power modules of that time in a project called LESIT. According to their study, the scaling factor A was 640. Now, repeating the power cycling test by modules with lead-free solder, the scaling factor A is 7180. Thus it can be said, that the factor of improvement in the power cycling lifetime of modern IGBT power modules is greater than 10 compared with the modules ten years ago Held et al. (1997); Ikonen et al. (2007).

4.6.2 Lifetime estimation of an IGBT module in a wind turbine

The estimated lifetime of the IGBT in the wind turbine, if located in south-eastern Finland, would be 15 000 years. This is extremely high compared with the traditional lifetime specification for wind turbines, which is 20 years. There are a couple of reasons for such a high lifetime. The average wind (7 m/s) on the measurement site is low compared with the wind speed of the turbine nominal power (12 m/s). This means that the turbine seldom produces full power, and temperature cycles of high ΔT_j are of rare occurrence.

On the other hand, assuming that if the IGBT chip generated more power losses than estimated and that the chip temperature cycled from 50°C at zero power to 150°C at full power once an hour, the lifetime would still be 6.8 years. This temperature cycle amplitude is a reasonable estimation for the maximum amplitude. The cooling system must be designed to work at the maximum ambient temperature, which would be 40°C. This leads to a 50°C cooling liquid temperature, and thus, the minimum heat sink temperature is the very same 50°C. On the other hand, the maximum chip temperature according to the data sheet is 150°C, which leads to $\Delta T_\mathrm{j} = 100$°C.

During the cold season, the heat sink temperature would be lower, but the heat sink temperature has no effect on the temperature cycle amplitude, only on the medium temperature. Thus, the temperature cycle from 50°C at zero power to 150°C is the worst case for this converter.
Furthermore, with the current converter design and temperature cycles once an hour from 50°C at zero power to 110°C at full power, the lifetime is 366 years.

We may be conclude that the power cycling lifetime of modern power modules is high enough not to limit the lifetime of wind turbines.

4.7 Summary

A method for the power cycling lifetime estimation of an IGBT power module was presented. Analytical lifetime models were reviewed and the most suitable model for the life consumption estimation was selected.

The available power cycling life of a power module with a lead-free solder was defined by laboratory measurements. Based on the results, the lifetime of modern power modules is ten times as high as the lifetime of power modules in the late 1990s.

The power cycling test results were used in the life consumption calculation of a power module in a wind turbine application. It was found that the power cycling lifetime of power modules does not limit the lifetime of wind turbines. The estimated lifetime is 15 000 years, if located in south-eastern Finland.

Chapter 5

Summary and conclusions

In this doctoral thesis, the IGBT chip temperature modeling was analyzed from the lifetime estimation point of view. The target was to find a suitable method to estimate the remaining lifetime of the module in an actual application. The objective was to find whether it is possible to represent the overall lifetime by a mathematical model, and whether it is possible to estimate the junction temperature of the IGBTs accurately enough to be used as an input to the lifetime model. This way, the remaining lifetime would be estimated only by using the existing measurements, such as the module temperature and the IGBT collector current.

The benefits of such a prediction lie in the maintenance of frequency converters and drives; an unexpected halt of operation of the converter can be avoided, and thus, the converter can be used most efficiently and maintained on time. On the other hand, there would be no need to maintain the converter in advance.

5.1 Key results of the work

1. Thermal modeling.
   A thermal simulation model for a single IGBT was constructed. The model estimates the chip temperature based on the estimated power losses of the chip and the measured thermal parameters.

   In addition, a test system was built to verify the thermal model. It was based on the simultaneous measurement and simulation of the chip temperature. Different alternatives to measure the chip temperature were considered, and the

thermocouple measurement was examined in detail. The thermal parameters of the system were defined for accurate temperature estimation. Based on the research, the measurement system proved to be convenient for studying the thermal behavior of the chip. It was found that the constructed thermal model has a 5°C accuracy in the temperature estimation.

The thermal model was prepared for hardware implementation. It was found that the hardware implementation increases the error in the temperature estimation by 5%.

2. Lifetime modeling.
   A power cycling lifetime model was selected and verified by tests. The available power cycling lifetime of the IGBT power modules with lead-free solder was determined by laboratory tests. According to the measurements, the factor of improvement in the power cycling lifetime of modern IGBT power modules is greater than 10 during the last decade.

   The selected lifetime model was fitted to the power cycling test results. It was found that the lifetime is highly dependent on the junction temperature swing amplitude ΔT_j and mean value T_m. It was noticed that a 10°C increase in the junction temperature swing decreases the lifetime by 40%. While the accuracy of the thermal model with datasheet values is not much better than 10°C, we may conclude that the thermal model parameters must indeed be fine-tuned according to the application and the individual converter.

3. IGBT lifetime estimation in a direct-driven wind turbine.
   The lifetime of an IGBT power module in a wind turbine application was estimated. The chip temperature was simulated with the thermal model based on wind measurements on an onshore site in south-eastern Finland. The temperature cycle count was compared with the measured lifetime of the power module. According to the estimation, the lifetime of the IGBT power module in a direct-driven wind turbine is 15 000 years. We may conclude that the power cycling lifetime of power modules does not limit the lifetime of wind turbines.

5.2 Suggestions for future work

There are many subjects to be studied in the thermal and lifetime modeling in order to accurately estimate the remaining power cycling lifetime of a power module. At the moment, the models work best when comparing the lifetime in various conditions, and when studying the effect of the load on the lifetime. There are many open issues that must be solved before the definite lifetime of a power module can be estimated.

One of the major issues is to determine how the cycles of different chip temperature swings ΔT_j accumulate. Now, linear accumulation is assumed in the life consumption estimation. However, there is evidence that the accumulation may not be linear (Scheuermann and Hecht, 2002). The temperature cycle excites different degradation mechanisms, depending on the cycle amplitude. This means that the LC should be counted separately for both failure mechanisms. This requires more work on the research of the cross-effect of the degradation mechanisms.

The correlation of accelerated power cycling tests to real life is another open issue. The lifetime requirement of IGBT power modules can be as high as 30 years (Berg and Wolfgang, 1998), whereas IGBTs have barely existed for that long.

The third issue is the order in which the temperature cycles occur. At the moment, the presented lifetime models do not take into account the order of the cycles. According to the lifetime models, a cycle with a small amplitude has the same effect on the lifetime regardless of whether it occurred before or after a cycle with a large amplitude. It would be important to find if the solder degradation speed is linearly dependent on the temperature cycle amplitude or not. This issue should be addressed in the lifetime modeling in the future.

The thermal model could be constructed more accurately in several ways. The heating effect of the neighboring chips could be taken into account by a heat transfer matrix, and the power division between the paralleled chips could be taken into account. However, if the paralleled chips are on a common DBC and/or base plate, the temperature tends to even out because of the heat transfer between the chips. It would be of interest to take into account the thermal resistance dependence on temperature in the model, especially in high-temperature modules that apply silicon carbide or other high-temperature devices. In addition, the effect of the power factor on the power division between the IGBT and the free-wheeling diode could be taken into account.

Measuring the temperature in the reference point is not possible in industry standard modules the same way it is carried out in this work. There is a temperature sensor in some modules, but it is far in the lateral direction away from the chips, and the thermal characterization from the chip to that point is challenging. On the other hand, drilling a hole to the heat sink as it is done in this study is not applicable in commercial manufacturing. As an alternative for measuring the reference point, also the heat sink and the cooling system could be modeled so that the thermal model would describe the behavior from the chip to the ambient.

The parameter variation is an issue in power loss estimation. The on-state voltage drop of IGBTs can vary from module to module causing an error in the power loss estimation if the voltage drop is not determined first. This issue can be overcome if the actual collector-emitter voltage is being measured all the time. This type of a measurement should be carried out with a high bandwidth, and the sampling should be properly timed to match the on-state of each chip. It would mean additional costs because of additional measurement electronics placed in the frequency converter. On the other hand, if there is an accurate collector-emitter voltage measurement, the chip temperature can be calculated directly from it without a need for a sophisticated thermal model. Moreover, if there is an accurate collector-emitter voltage measurement on the converter, the end of life can be detected directly from the rising saturation voltage level.

5.3 Conclusions

A thermal simulation model for a single IGBT was constructed. The model estimates the chip temperature based on the estimated power losses of the chip and the measured thermal parameters. A test system was built to verify the simulation models. It was based on the simultaneous measurement and simulation of the chip temperature. The thermal parameters of the system were defined. Furthermore, the thermal model was prepared for hardware implementation.

A method for the power cycling lifetime estimation of an IGBT power module was presented. Analytical lifetime models were reviewed, and the most suitable model for the life consumption estimation was selected. The available power cycling life of a power module with a lead-free solder was determined by laboratory measurements. The power cycling test results were used in the life consumption calculation of a

power module in a wind turbine application.

We may conclude that the lifetime of an IGBT power module can be estimated by modeling the chip temperature, with the following condition. The accuracy of the thermal model determines the accuracy of the lifetime estimation. A 10% error in the temperature estimation gives a 40% error in the lifetime estimation. For this reason, the thermal parameters of the power module in the final application must be measured, for each device, to obtain an accurate lifetime estimation.

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