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Mikko Purhonen

# MINIMIZING CIRCULATING CURRENT IN PARALLEL-CONNECTED PHOTOVOLTAIC INVERTERS

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# Abstract

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Parallel-connected photovoltaic inverters are required in large solar plants where it is not economically or technically reasonable to use a single inverter. Currently, parallel inverters require individual isolating transformers to cut the path for the circulating current.

In this doctoral dissertation, the problem is approached by attempting to minimize the generated circulating current. The circulating current is a function of the generated common-mode voltages of the parallel inverters and can be minimized by synchronizing the inverters. The synchronization has previously been achieved by a communication link. However, in photovoltaic systems the inverters may be located far apart from each other. Thus, a control free of communication is desired.

It is shown in this doctoral dissertation that the circulating current can also be obtained by a common-mode voltage measurement. A control method based on a short-time switching frequency transition is developed and tested with an actual photovoltaic environment of two parallel inverters connected to two 5 kW solar arrays. Controls based on the measurement of the circulating current and the common-mode voltage are generated and tested.

A communication-free method of controlling the circulating current between parallel-connected inverters is developed and verified.

Keywords: PV inverters, circulating current, parallel-connected inverters, wireless control
UDC: 621.383.51:621.314:621.3.014:621.313.3

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First, I express my gratitude to my supervisor, Professor Pertti Silventoinen, who made this process possible and provided the required time, tools, and funding to complete this journey. Additionally, I would like to thank Professor Olli Pyrhönen for his comments and Dr. Markku Niemelä for his guidance with both the experimental setup and the manuscript of this work. I also thank all the people involved in the previous projects of my research career during the years 2007 – 2012. The knowhow regarding solar inverters has been largely derived from the SofcPower project, the Vacon solar inverter project, and all the people involved in them. My most "grammatical thanks" goes to Dr. Hanna Niemelä for improving the language of this work.

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My special thanks goes to all of my great colleagues that I was blessed with during this journey, especially to Mr. Raimo Juntunen and Mr. Teemu Sillanpää for the help they provided during the building and commissioning of my experimental setup. Cheers to Dr. Juhamatti Korhonen, Dr. Juha Ström, Dr. Juho Tyster, Mr. Janne Hannonen, and Mr. Arto Sankala, who provided an inspiring work atmosphere and bitter moments outside the office as well.

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Helsinki, November 11th, 2014

Mikko Purhonen

# Contents

# Nomenclature

**Latin alphabet**

| | | |
|---|---|---|
| $A$ | area | $m^2$ |
| $c$ | scaling constant | |
| $C$ | capacitance | F |
| $d$ | distance | m |
| $i$ | current | A |
| $I$ | RMS value of current | A |
| $L$ | inductance | H |
| $m$ | sector | |
| $M$ | modulation index | |
| $\mathbf{N}$ | natural numbers | |
| $P$ | power | W |
| $t$ | time | s |
| $T$ | switching period length | s |
| $u$ | voltage | V |
| $U$ | RMS value of voltage | V |
| $x$ | phase variable of a three-phase system | |

**Greek alphabet**

| | | |
|---|---|---|
| $\alpha$ | uncertainty factor | |
| $\varepsilon$ | permittivity | F/m |
| $\theta$ | phase angle | rad |
| $\tau$ | time as an integration variable | s |
| $\phi$ | phase shift angle | rad |
| $\zeta$ | damping factor | |
| $\omega$ | angular frequency | rad |

**Superscripts**

| | |
|---|---|
| * | dimensionless |
| s | stationary frame |

**Other notations**

| | |
|---|---|
| $\hat{x}$ | peak value of $x$ |
| $\underline{x}$ | space vector |

**Subscripts**

| | |
|---|---|
| 0 | vacuum, zero-vector |
| 1 | inverter side, index number 1 |
| 2 | grid side, index number 2 |
| 3 | index number 3 |
| α | stationary coordinates, alpha component |
| A | phase A |
| β | stationary coordinates, beta component |
| B | phase B |
| C | phase C, capacitor |
| circ | circular |
| CM | common mode |
| d | synchronous coordinates, d component |
| DC | DC link |
| dry | dry conditions |
| inv1 | inverter 1 |
| inv2 | inverter 2 |
| inv*n* | inverter *n* |
| L1 | inverter side inductor of an LCL filter |
| L2 | grid side inductor of an LCL filter |
| LCL | LCL filter |
| *m* | index number |
| *n* | index number |
| MPP | maximum power point |
| OC | open circuit |
| q | synchronous coordinates, q component |
| r | relative, resonance |
| SC | short circuit |
| tot | total |
| wet | wet conditions |

**Abbreviations**

| | |
|---|---|
| AC | alternating current |
| ADC | analog to digital converter |
| DC | direct current |
| EU | European Union |
| FFT | Fast Fourier Transform |
| FPGA | field-programmable gate array |
| GHG | greenhouse gas |
| IC | incremental conductance |
| MPP | maximum power point |
| MPPT | maximum power point tracker |

| | |
|---|---|
| NP | neutral point |
| NPC | neutral point clamped |
| P&O | perturb and observe |
| PV | photovoltaic |
| PWM | pulse width modulation |
| RMS | root mean square |
| STC | standard test conditions |
| SVPWM | space vector pulse width modulation |
| TCO | transparent conductive oxide |
| TF | thin film |
| VSI | voltage source inverter |

# Chapter 1

# Introduction

In 2007, the European Union (EU) set the targets for a greener Europe and a greener Earth. In 2009, the European Parliament approved a directive on the use of energy from renewable sources (European Union, 2009). The targets for 2020 are a 20% reduction in the greenhouse gas emissions from the 1990 levels, increasing the share of energy consumption produced from renewable energy sources to 20%, and a 20% improvement in the energy efficiency. The two former of these objectives can be achieved by increasing the amount of clean renewable energy production such as hydropower, wind power, or solar power.

As a source of electricity, hydropower has the longest history of these three power sources. Hydroelectricity dates back to the time when the electrical machine was invented in the 19$^{th}$ century. In the early 20$^{th}$ century, the hydroelectricity gained popularity and reached over 25% of the electricity production in the United States. Ever since the early 20$^{th}$ century, hydropower has played a significant role in global energy production.

In the late 1990s, the wind power started to gain popularity when the discussion about greenhouse gases (GHGs), global warming, and renewable energy sources started to heat up. The amount of wind power in Europe has been rapidly increasing ever since, from the cumulative installed peak power of 12.9 GW in the year 2000 to 121.5 GW of installed peak power in the end of 2013 (EWEA, 2014).

The solar panel technology was not as advanced and cost-effective as the wind power in the late 1990s, and thus, it did not reach the same growth during that time. In 2006, the cumulative peak power of the installed photovoltaic (PV) systems in Europe was 3.1 GW (EurObserv'ER, 2008) compared with 48.1 GW of wind power (EWEA, 2014). The massive investments by Germany, mostly in the form of feed-in tariffs after the Renewable Energy Act of 2000, rapidly decreased the costs of photovoltaic systems. At the end of 2012, the amount of installed PV systems in Europe was 78.8 GW (EurObserv'ER, 2014). From 2006 to 2013, the amount of installed wind power in Europe has increased by 153%, compared with the increase of 2442% in PV power.

## 1.1 Background

The current PV systems vary in power from a few milliwatts up to hundreds of megawatts. The smallest solar panels are used, for example, in small calculators and watches, where the power requirements are measured in milliwatts. The solar panels designed especially for grid-connected power production are usually a few hundred watts in power. A relatively low power level of a single solar panel allows solar arrays to be modularly built and easily customized. The grid-connected rooftop PV systems vary in power from about one kilowatt in a household rooftop to hundreds of kilowatts in a rooftop of a commercial building or a factory. The ground installations range all the way up to hundreds of megawatts.

The solar panels produce direct current (DC) that needs to be transformed into alternating current (AC) for the grid. The DC to AC transformation is achieved with an inverter. The PV inverters are matched with the solar array during the planning and installation of the system. A single large PV inverter is called a centralized inverter. The benefits of a centralized inverter are high efficiency and a good price-power ratio. The main disadvantage of a centralized inverter is the operation in partly shaded conditions. This disadvantage is related to the number of maximum power point trackers (MPPTs) in the system. Compared with the centralized inverter, a string inverter is smaller in size. The benefit of including multiple string inverters instead of one centralized inverter is the modularity of the solar plant and the increased number of MPPTs in the whole system. However, the efficiency of the string inverters is not as high as the efficiency of centralized inverters (Pavan et al., 2007).

A single PV inverter has a maximum power rating limit that comes from the special characteristics of the PV system. The voltage of a single PV inverter is limited by the highest possible system voltage defined by the solar panels. The maximum system voltage used to be 600 volts, especially in the United States. For a while now, the maximum system voltage has been 1000 volts for solar panels manufactured in Europe and China. Currently, the solar panel manufacturers are trying to reach the 1500 volt limit of the low-voltage standard (European Union, 2006). The motivation in increasing the system voltage is the higher efficiencies of the power electronics and the cables with the higher voltage levels. The maximum system voltage also prevents the series connection of inverters beyond the rated maximum voltage (BELETRIC, 2012).

The current rating of the PV inverter is limited by the current rating of the individual semiconductor devices. In drives applications, the semiconductor devices are connected in parallel to increase the power rating of a single inverter (Azar et al., 2008). However, paralleling of semiconductor devices in PV inverters increases the power level of a single inverter, but simultaneously reduces the efficiency of the MPPT algorithm especially in shaded conditions (Mäki and Valkealahti, 2012). In order to achieve the maximum energy harvesting from the solar plant, the combined efficiency of the inverter and the MPPT has to be maximized under the prevailing conditions. Currently, the highest power ratings of single commercial PV inverters are around 4 MW (First Solar, 2014).

A common solution to increase the power level of the solar plant is, instead of connecting components in parallel inside of an inverter, to connect whole PV inverters in parallel. Thus, the number of MPPTs is also increased and the MPPT efficiency is not affected. The largest solar plants may have hundreds of PV inverters connected in parallel. The DC sides of the inverters are connected to their individual solar panels, and the AC sides are connected together either on the low-voltage side of a step-up transformer or on the medium-voltage side. An illustration of the parallel-connected PV inverters with solar panels and a medium-voltage transformer towards the grid can be seen in Fig. 1.1.

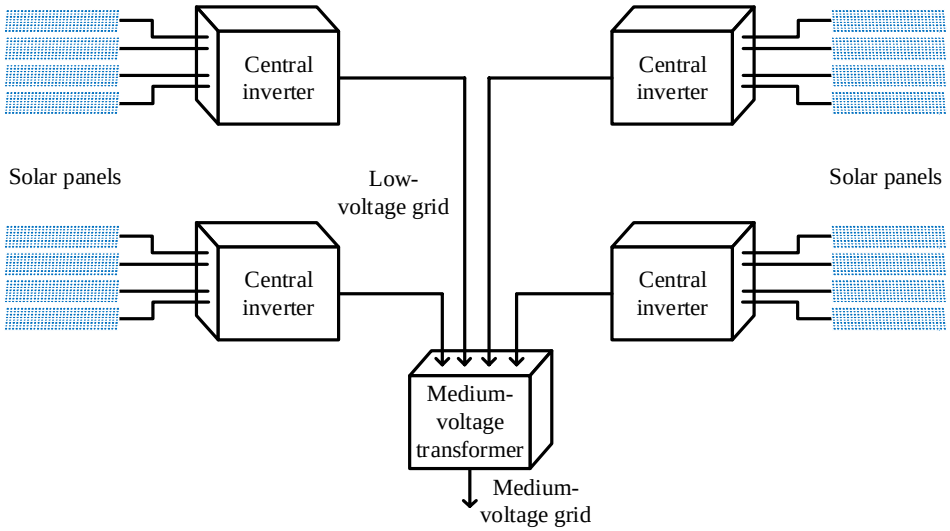


Fig. 1.1. Large solar plant with four parallel-connected PV inverters and a medium-voltage transformer towards the medium-voltage grid.

The main problem with the parallel-connected PV inverters is the circulating current at the switching frequency, which is well known from drives applications (Itkonen et al., 2009), (Itkonen et al., 2006). Usually, the circulating current is removed with isolating transformers. Most solutions to minimize the circulating current without a transformer include synchronization of parallel-connected inverters with a communication link.

## 1.2 Motivation of the work

Currently, large solar plants have individual low-voltage to medium-voltage Δ-Y step-up transformers at each PV inverter, or a custom-made multi-primary Δ-Y step-up transformer where each PV inverter feeds a single primary, as illustrated in Fig. 1.1, or individual isolating low-voltage Δ-Δ transformers and a single Δ-Y step-up transformer (Bae and

Kim, 2014; Oliva and Balda, 2003). These different transformer setups have to meet the following objectives:

- Increase the voltage level from the low-voltage network to the medium-voltage grid.
- Isolate the PV inverters separately to cut the path for the circulating current.

The first objective requires at least one standard Δ-Y step-up transformer. The second objective is met either by including individual isolating low-voltage transformers in the setup or by using a medium-voltage transformer with multiple primaries. The individual isolating low-voltage Δ-Δ transformers cause extra losses and costs in the system. The multi-primary step-up transformers, on the other hand, are more difficult to manufacture than the basic single-primary single-secondary step-up transformers.

The motivation for this doctoral dissertation is to meet the second objective without bulky extra transformers, by simply applying control algorithms. The circulating currents of the parallel-connected PV inverters have previously been studied in (Bae and Kim, 2014). The circulating current is minimized by synchronizing the parallel inverters. However, the control method introduced in the previous study implements communication links between the parallel inverters. The PV inverters may be located far apart, therefore, the motivation of this dissertation is further defined as achieving the task without extra communication links.

From here on, the term ‘circulating current minimizing control’ and all other minimizing controls refer to the minimization of the circulating current by means of synchronizing the modulators of the parallel inverters. Here, external factors to minimize the circulating current such as inserting circulating current filters or affecting the parameters of the solar panels are not included in the term.

## 1.3 Objective of the work

The objective of this doctoral dissertation is to perform measurements and control algorithms in order to

- synchronize the modulators of the parallel-connected inverters,
- minimize the circulating current between parallel PV inverters,
- remove the need for individual isolating transformers, and
- remove the need for a communication between synchronized modulators.

The control has to take into account the special characteristics of the photovoltaic systems. First of all, the control has to be able to operate over a distance of hundreds of meters, since the PV inverters may be spread across a wide area in the solar parks. When using a

communication link for the synchronization of the modulators, the long distance causes difficulties, adds costs and reduces reliability. This is why a wireless controller is strived for.

The second special character of the PV systems is the individual power generation of the inverters. The inverters have their own maximum power point (MPP) tracking algorithms that maximize the energy harvesting of the solar plant. The controller to minimize circulating current should not decrease the energy harvesting of the solar plant, and thus not interfere with the basic controllers of the inverter.

The goals are pursued by introducing a switching frequency transition in order to change the synchronization between the parallel-connected inverters and measuring the synchronization with the circulating current or with common-mode voltages (CMVs).

## 1.4 Outline of the work

This doctoral dissertation studies the circulating current and the common-mode voltages generated in parallel-connected PV inverters. The present methods to minimize circulating current are examined and analyzed. A new method for measuring the synchronization and the circulating current is introduced. A method of changing the synchronization by a temporary switching frequency transition is proposed. Control algorithms applying the measurements and the synchronization method are examined with an experimental setup.

The rest of the dissertation is divided into the following chapters:

**Chapter 2** introduces the background to the circulating current and the common-mode voltage of the PV inverters.

**Chapter 3** analyzes the theory behind the synchronization measurement and the temporary switching frequency transition. Further, the chapter introduces methods and limitations on the measurements and the control.

**Chapter 4** presents an experimental setup to confirm the theory and to test the measurements and the control methods.

**Chapter 5** concludes the doctoral dissertation. The main results are discussed and summarized, and suggestions for future work are made.

## 1.5 Scientific contributions

The scientific contributions of this doctoral dissertations are:

- Experimental verification of the synchronization method of the short-term switching frequency modification.
- Experimental verification of the control to minimize circulating current based on circulating current measurement.
- Generation and verification of the theory for the control to minimize the circulating current based on common-mode voltage measurement.
- Verification of multiple different control methods valid for the circulating current control.
- Generation and verification of the theory for the circulating current control for different ground impedance setups.

The author has published research results related to the subjects covered in this doctoral dissertation in the following publications:

1. Purhonen, M., Musikka, T., Korhonen, J., Silventoinen, P., and Viitanen, T. (2013), ”Wireless Circulating Current Control for Parallel Connected Photovoltaic Inverters,” in *AFRICON 2013, IEEE*.

2. Purhonen, M., Korhonen, J., Juntunen, R., Sillanpää, T., Silventoinen, P., and Viitanen T., ”Circulating Current Control Without Current Measurement for Parallel-Connected Photovoltaic Inverters With Independent Control Units,” *Transactions on Power Electronics, IEEE* (submitted for publication).

M. Purhonen has been the primary author in Publications 1–2. The background studies and the simulations as well as the building of the prototype and the implementation were entirely carried out by the author.

The author is also listed as a coinventor in the following patent application related to the subject presented in this doctoral dissertation:

**Finnish patent application 20136117** “Method and Apparatus for Minimising a Circulating Current or a Common-Mode Voltage of an Inverter,” application filed November 14, 2013.

# Chapter 2

# Parallel-connected photovoltaic inverters

*This chapter provides background for the parallel-connected photovoltaic inverters starting with the solar panels and covering more precisely the parallel connection of inverters. First, the solar panels, PV inverters, and inverter topologies are addressed. Next, the requirements for the parallel connecting of inverters and the synchronization of the inverters are discussed. Finally, the common-mode voltage and the circulating current of PV inverters are considered.*

## 2.1 Solar panels

From the perspective of power electronics, the solar panels have properties similar to a constant current source with voltages lower than the MPP voltage, and properties similar to a constant voltage source with voltages higher than the MPP voltage. This specific behavior between the current and voltage of the solar panel is illustrated in Fig. 2.1, along with the power of the solar panel (Nousiainen et al., 2013).

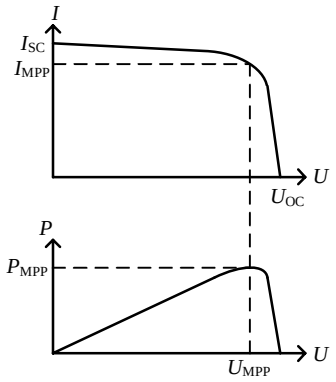


Fig. 2.1. IU and PU curves of a regular solar panel in standard test conditions (STC).

The depicted quantities in Fig. 2.1 are the open-circuit voltage $U_{\mathrm{OC}}$, the short-circuit current $I_{\mathrm{SC}}$, the MPP voltage $U_{\mathrm{MPP}}$, the MPP current $I_{\mathrm{MPP}}$, and the MPP power $P_{\mathrm{MPP}}$.

The curves in Fig. 2.1 are dependent on multiple factors. The two most dominant external factors are the temperature and the irradiation level on the semiconductor surface of the solar panel (Villalva et al., 2009). The absolute voltage and current levels of the solar panel depend on the solar panel technology. The nominal voltage and current values of a current crystalline silicon solar panel given by the five largest solar panel manufacturers are; $U_{\mathrm{OC}} = 30\,\mathrm{V} - 50\,\mathrm{V}$, $U_{\mathrm{MPP}} = (76\% - 83\%) * U_{\mathrm{OC}}$, $I_{\mathrm{SC}} = 6\,\mathrm{A} - 9\,\mathrm{A}$, $I_{\mathrm{MPP}} = (87\% - 95\%) * I_{\mathrm{SC}}$. The ratio between the voltage and the current of the panel is considerably lower with crystalline silicon panels than it is with thin film (TF) panels, the nominal values of which range between $U_{\mathrm{OC}} = 30\,\mathrm{V} - 150\,\mathrm{V}$, $U_{\mathrm{MPP}} = (72\% - 80\%) * U_{\mathrm{OC}}$, $I_{\mathrm{SC}} = 1\,\mathrm{A} - 4\,\mathrm{A}$, $I_{\mathrm{MPP}} = (85\% - 92\%) * I_{\mathrm{SC}}$ (Photon International, 2014).

### 2.1.1 Ground impedance of a solar panel

Compared with other power sources, the special characteristics of solar panels are the *IU* curve shown in Fig. 2.1 and the ground impedances of the solar panels. The *IU* curve requires the MPPT to get the maximum power out of the solar panels. A solar panel has parasitic capacitances between the positive and negative electrodes, and between the grounded mounting frame and the electrodes. The parasitic capacitances are illustrated in Fig. 2.2. The mounting frames are grounded because the solar panels are exposed-conductive-parts, which have to be grounded, according to the IEC standard 60364 (IEC, 2005).

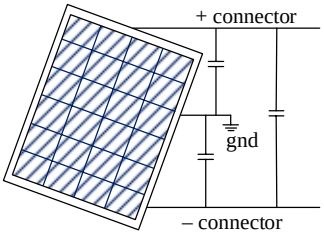


Fig. 2.2. Parasitic capacitances between the positive and negative buses of a solar panel and between the grounded rack and the positive and negative buses.

The parasitic capacitances are present in every PV installation. The capacitance $C$ between the grounded mounting frames and the electrodes of the solar panels can be calculated with the capacitance equation

$$C = \frac{\varepsilon_0 \varepsilon_{\mathrm{r}} A}{d}, \tag{2.1}$$

where $\varepsilon_0$ is the vacuum permittivity ($\varepsilon_0 \approx 8.854 \times 10^{-12}$ Fm$^{-1}$), $\varepsilon_r$ is the relative permittivity, $A$ is the effective surface area of the capacitor, and $d$ is the distance between the capacitor plates. The relative permittivity of air is $\varepsilon_r \approx 1$, as the relative permittivity of glass is $\varepsilon_r = 4 - 10 \approx 6$. The distance between the capacitor plates $d$ depends on the structure of the solar panel. The area of the capacitor $A$ is more difficult to determine. The area depends significantly on the structure of the solar panel and the weather conditions. An illustrations about the ground capacitances can be seen in Fig. 2.3.

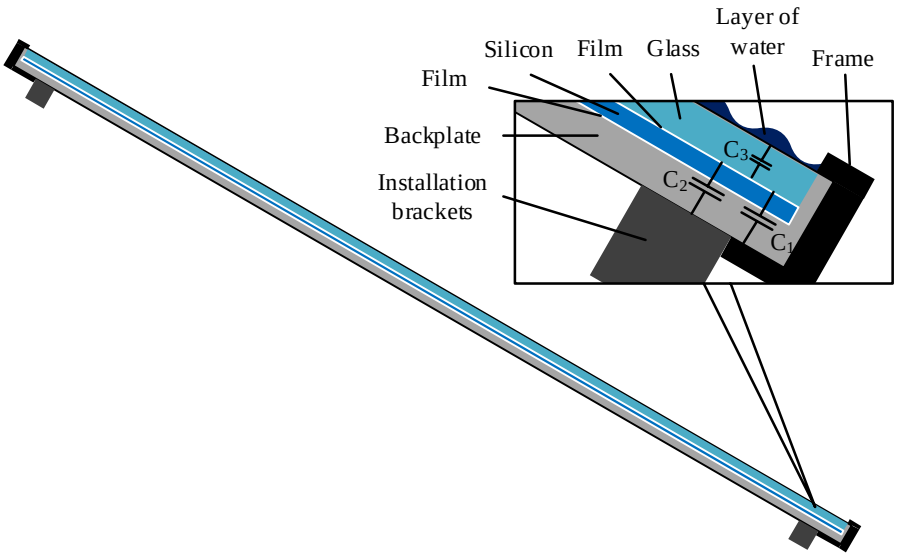


Fig. 2.3. Parasitic capacitances inside of a solar panel. Capacitances $C_1$and $C_2$ are between the semiconductor layer and the grounded frameworks and installation brackets. The capacitance $C_3$ is between the semiconductor layer and a layer of water on top of the solar panel in wet conditions (SMA, 2014).

In Fig. 2.3, the parasitic capacitances are against the aluminum frame ($C_1$), against the installation brackets ($C_2$), and against a film of water on top of the glass ($C_3$). Assuming that the panel is a common crystalline silicon solar panel and the electrical layer is in the mid-point of the solar panel, the distance $d$ to the top and bottom sides of the panel is about 4 mm. The effective area of both $C_1$ and $C_2$ combined can be estimated to be about 10%. Currently, a single 1.5 m$^2$ solar panel has a power rating of about 250 W. Thus, one kilowatt of solar panels requires 6 m$^2$ of panel area. With these values and Eq. (2.1), the ground capacitance in dry conditions can be calculated as a parallel connection of $C_1$ and $C_2$, thus $C_{\text{dry}} \approx 8\,\text{nF/kW}$ (SMA, 2014).

In wet conditions, a layer of water is situated on top of the solar panel and a capacitance $C_3$ between the water and the semiconductor layer. The area of the capacitance $C_3$ is equal

to the total area of the solar panel. With a different area of the effective capacitance, the ground capacitance in wet conditions can be calculated by Eq. (2.1) as $C_{\mathrm{wet}} \approx 88\ \mathrm{nF/kW}$.

The symmetric ground connection of the solar panels and a symmetrical ground connection in a PV inverter exposes the solar panels to a positive and negative voltage depending on the positions of the solar panel in the string of the series-connected solar panels. The system voltages in a setup of seven series-connected solar panels with a total open-circuit voltage of 300 volts is depicted in Fig. 2.4.

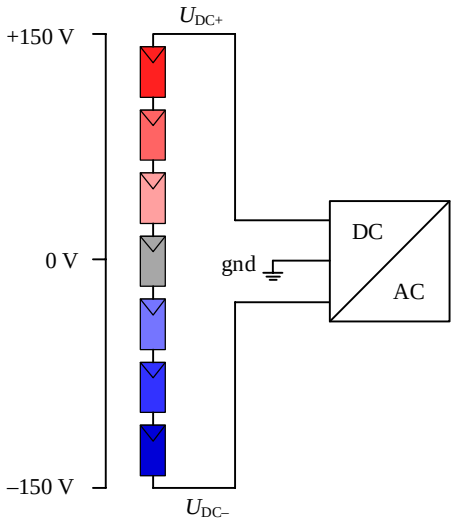


Fig. 2.4. Division of the DC voltage in a string of series-connected solar panels connected to an inverter with a symmetric grounding.

The symmetrical mid-point grounding as seen in Fig. 2.4 is common with crystalline silicon solar panels. The negative or positive bus of the solar panels may have to be grounded for functional reasons directly or through a resistance. These functional reasons take place for example in thin-film solar panels where the cover glass is directly in connect with the transparent conductive oxide (TCO) layer that is on top of the semiconductor material. This type of a setup along with a negative potential at the semiconductor surface inflicts irreversible corrosion damage on the TCO layer, which degrades the power rating of the solar panel. The TCO corrosion can be avoided by inserting a functional grounding to the negative bus, as depicted in Fig. 2.5. The functional grounding can be a direct grounding or more often a grounding through a resistance. The grounding prevents the presence of negative voltages from the semiconductor surfaces, and thereby inhibits corrosion (Wen and Ricou, 2012).

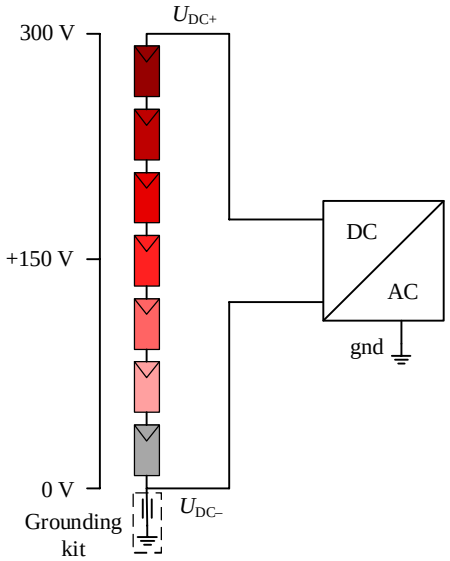


Fig. 2.5. Division of the DC voltage in a string of series-connected solar panels with a grounding kit on the negative bus to introduce functional grounding.

## 2.2 Photovoltaic inverters

The basic function of the PV inverter is similar to all the other inverters, that is, to convert direct current (DC) into alternating current (AC). The DC source of the PV inverter is composed of solar panels, from a single solar panel up to thousands of solar panels connected in series and in parallel. These solar panels pose special demands for the PV inverters. The main special character of the solar panels is the nonlinear output power curve shown in Fig. 2.1. To operate the solar panels in the optimal operating point, the PV inverter has to use a MPPT.

The solar panels can be connected in series to increase the MPP voltage of the PV system and in parallel to increase the MPP current of the system. If the MPP voltage of the solar panels is not high enough for the PV inverter, a DC–DC converter can be used to boost the voltage to a proper level. If the DC–DC converter is needed, the MPPT can be used at the DC–DC stage. When a DC–DC converter is not needed, the MPPT has to be used at the DC voltage reference control of the inverter to get the maximum power out of the solar panels.

There are dozens of different MPPT algorithms, some of which work well only in unshaded conditions and some that are better for panels that are often shaded. The simplest MPPT

algorithms are hill-climbing algorithms such as the perturb and observe (P&O) control and the incremental conductance (IC) control (de Brito et al., 2013).

The P&O controller measures the power of the system and performs a perturbation to the operating point by changing the current or voltage of the solar array. After the perturbation, the control performs another observation and measures whether the perturbation was in the right direction thereby increasing the power, or towards the wrong direction thereby decreasing the power. Based on this observation, another perturbation is made in the correct direction. This control algorithm seeks out the first maximum power point and oscillates around it.

The AC side of the PV inverters may be connected to the electricity grid or to an off-grid microgrid. The inverter has to meet the requirements defined by the AC side, whether it is an electricity grid or a microgrid. The requirements of the local electricity distribution company are written in grid codes. The grid codes vary depending on the country and the distribution company. Typical requirements by the distribution company include limitation of the harmonic content, an anti-islanding detection, and a fault ride-through capability.

### 2.2.1 PV inverter topologies

The topologies of the PV inverters can be divided into two categories, the first category being the single-phase inverters and the second category the three-phase inverters. The single-phase inverters are used at power levels below 10 kW. For example in Germany, the limit for the power generation phase unbalance and, thus, for the single phase inverter is 4.6 kVA (VDE, 2011).

The most common single-phase topologies can be divided into two categories; the H-bridge-derived topologies and the three-level topologies. The basic H-bridge topology and the neutral-point-clamped (NPC) topology are illustrated in Fig. 2.6. This dissertation focuses on the three-phase topologies, since the three-phase inverters are used in large-scale PV systems. The single-phase topologies are scrutinized in (Teodorescu et al., 2011).

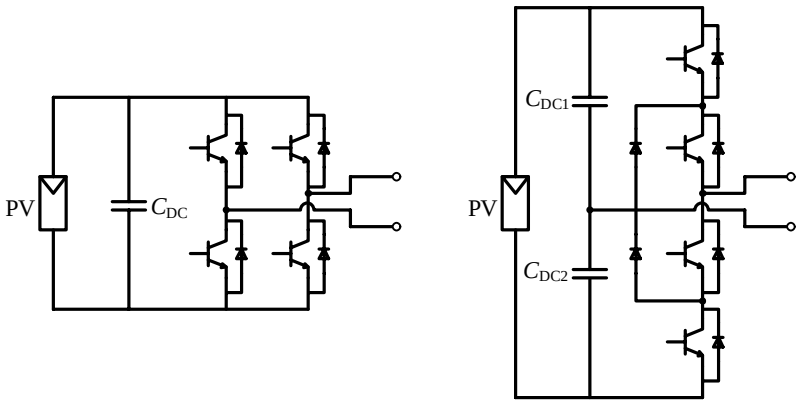


Fig. 2.6. Two single-phase PV inverter topologies. H-bridge topology on the left and an NPC topology on the right.

The most basic three-phase topology is the three-phase two-level voltage source inverter (VSI) that consists of three single-phase bridges as shown in Fig. 2.7. The output voltages of the phase legs have two possible voltage levels; the voltage of the positive DC bus and the voltage of the negative DC bus. In a typical symmetric PV inverter, the mid-point of the DC link is connected to the ground potential. Hence, the voltages of the DC buses and the output phase voltages may be either $U_{\mathrm{DC}}/2$ or $-U_{\mathrm{DC}}/2$. If the PV inverter uses a grounded negative DC bus, the possible output phase voltages are $U_{\mathrm{DC}}$ and 0. If the PV inverter uses a grounded positive DC bus, the possible output phase voltages are 0 and $-U_{\mathrm{DC}}$.

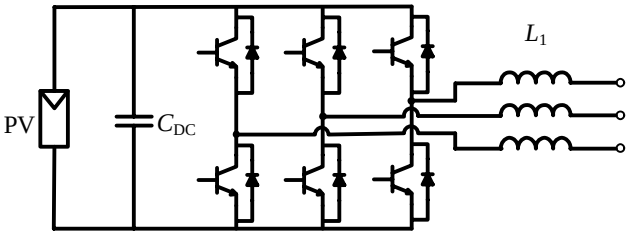


Fig. 2.7. Two-level three-phase voltage source inverter topology with a DC capacitor and a grid filter connected to a PV source.

Especially in a large-power PV application, inverter topologies with more than two levels have become more frequent. Two different three-phase three-level topologies can be seen in Fig. 2.8. On the left there is a normal NPC three-level inverter and on the right a NPC T-topology inverter. In these topologies, the output phase voltages have three possible voltage levels, the voltage of the positive DC bus, the voltage of the negative DC bus, and the voltage of the neutral point (NP) (Hao et al., 2012).

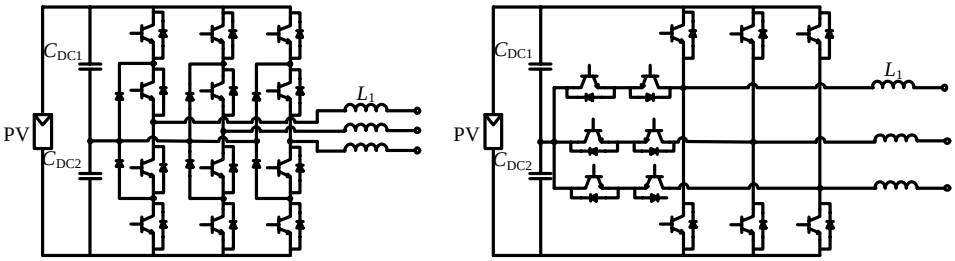


Fig. 2.8. Neutral-point-clamped three-level inverter topology on the left and a neutral-point-clamped three-level T-topology on the right.

A majority of the PV inverters are voltage-fed inverters. The voltage-fed PV inverter as a unit consists of at least the semiconductor bridge illustrated in Fig. 2.7, a DC link capacitor on the DC side of the inverter as a temporary energy storage for grid disturbances, and a grid filter on the AC side of the inverter to reduce the harmonic content of the output current of the inverter and to transform the voltage of the inverter into a current to the grid. In Fig. 2.7, the grid filter is an inductor. A more common grid filter especially in the PV applications is the LCL filter. An equivalent circuit of the LCL filter is depicted in Fig. 2.9.

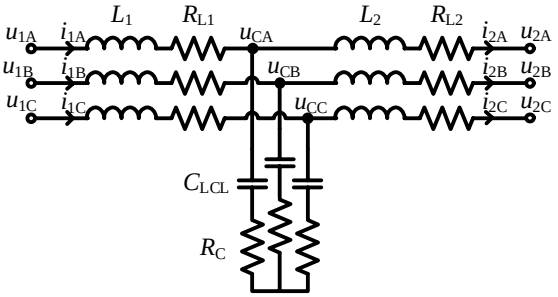


Fig. 2.9. Schematic of an LCL filter, where $L_1$ is towards the inverter and the positive direction of the current towards the grid.

The voltage on the grid side of the grid filter is defined by the grid. Thus, the power delivered towards the grid is determined by the current of the filter inductor in the L–filter, and the current of the inductor closer to the grid, $L_2$ in the LCL filter. The derivative of the current of the inductor, $L_1$ in the L–filter can be calculated by Eq. (2.2). The derivatives of the currents of the LCL filter inductors and the derivative of the voltage of the LCL filter capacitors can be calculated by Eqs. (2.3)–(2.5).

$$L_1 \frac{d}{dt}\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} u_{1A} \\ u_{1B} \\ u_{1C} \end{bmatrix} - \begin{bmatrix} u_{2A} \\ u_{2B} \\ u_{2C} \end{bmatrix} - R_L \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \tag{2.2}$$

$$L_1 \frac{d}{dt}\begin{bmatrix} i_{1A} \\ i_{1B} \\ i_{1C} \end{bmatrix} = \begin{bmatrix} u_{1A} \\ u_{1B} \\ u_{1C} \end{bmatrix} - \begin{bmatrix} u_{CA} \\ u_{CB} \\ u_{CC} \end{bmatrix} - (R_C + R_{L1}) \begin{bmatrix} i_{1A} \\ i_{1B} \\ i_{1C} \end{bmatrix} + R_C \begin{bmatrix} i_{2A} \\ i_{2B} \\ i_{2C} \end{bmatrix} \quad (2.3)$$

$$L_2 \frac{d}{dt}\begin{bmatrix} i_{2A} \\ i_{2B} \\ i_{2C} \end{bmatrix} = \begin{bmatrix} u_{CA} \\ u_{CB} \\ u_{CC} \end{bmatrix} - \begin{bmatrix} u_{2A} \\ u_{2B} \\ u_{2C} \end{bmatrix} - (R_C + R_{L2}) \begin{bmatrix} i_{2A} \\ i_{2B} \\ i_{2C} \end{bmatrix} + R_C \begin{bmatrix} i_{1A} \\ i_{1B} \\ i_{1C} \end{bmatrix} \quad (2.4)$$

$$C_{LCL} \frac{d}{dt}\begin{bmatrix} u_{CA} \\ u_{CB} \\ u_{CC} \end{bmatrix} = \begin{bmatrix} i_{1A} \\ i_{1B} \\ i_{1C} \end{bmatrix} - \begin{bmatrix} i_{2A} \\ i_{2B} \\ i_{2C} \end{bmatrix} \quad (2.5)$$

The inductance, capacitance, and resistance values in Eqs. (2.2)–(2.5) are specified by the installed grid filter. The current values and the capacitor voltage values can be integrated from the previous values while the grid voltages, $u_{2A}$, $u_{2B}$, and $u_{2C}$ are specified by the grid. Thus, a conclusion can be drawn that the current towards the grid and the output power of the inverter can be influenced by changing the voltages on the inverter side of the grid filter $u_{1A}$, $u_{1B}$, and $u_{1C}$.

The most common switching devices used in PV inverters are the insulated gate bipolar transistors (IGBTs). The output voltages of the inverter can be changed between the positive and negative DC buses, in the two-level semiconductor bridge shown in Fig. 2.7, as often as the switching components can withstand. The switching frequency limit of modern IGBTs used in PV applications is between 1 kHz and 20 kHz depending on the power level of the device.

The behavior of the switching components, and thus, the output voltage of the inverter bridge is discrete. Inserting discrete voltage to Eqs. (2.2)–(2.5) will result in a ramp-like behavior of the filter current. However, by averaging the output voltage of the inverter bridge and the current of the grid filter over a specified period of time, the desired grid frequency component of the current can be generated. The shortest period of time for the averaging is half of the switching period length of the switching devices.

### 2.2.2 Space vector theory

The space vector theory was first introduced in (Park, 1929) with an intention of introducing a two-dimensional vector, generated of the three-phase components. The mathematical representation for the space vector equations was introduced in (Kovacs and Racz, 1959). The original theory was intended for synchronous machines; however, the theory can be applied to all three-phase systems to determine the three-phase voltage, current, or flux of the system.

The phase quantities for a three-phase system, which rotates at an angular frequency of $\omega$, are expressed as

$$x_{\mathrm{A}}(t) = \hat{x}_{\mathrm{A}}(t)\cos\big(\theta(t) + \phi_{\mathrm{A}}(t)\big), \tag{2.6}$$

$$x_{\mathrm{B}}(t) = \hat{x}_{\mathrm{B}}(t)\cos\big(\theta(t) + \phi_{\mathrm{B}}(t)\big), \tag{2.7}$$

$$x_{\mathrm{C}}(t) = \hat{x}_{\mathrm{C}}(t)\cos\big(\theta(t) + \phi_{\mathrm{C}}(t)\big), \tag{2.8}$$

where $\hat{x}$ is the peak value of the phase quantity, $\phi$ is the phase shift angle, and the phase angle

$$\theta(t) = \int_0^t \omega(\tau)d\tau. \tag{2.9}$$

The three-phase system can be expressed as a complex space vector and a real zero-sequence component

$$\underline{x}^{\mathrm{s}}(t) = c\big(a^0 x_{\mathrm{A}}(t) + a^1 x_{\mathrm{B}}(t) + a^2 x_{\mathrm{C}}(t)\big), \tag{2.10}$$

$$x_0(t) = c_0\big(x_{\mathrm{A}}(t) + x_{\mathrm{B}}(t) + x_{\mathrm{C}}(t)\big), \tag{2.11}$$

where the superscript $s$ indicates that the space vector is in a stationary reference frame and

$$a = e^{j\frac{2\pi}{3}}. \tag{2.12}$$

The coefficients $c$ and $c_0$ can be chosen freely, but $c = 2/3$ and $c_0 = 1/3$ give a peak value scaling, which is mostly used. The coefficients $c = \sqrt{2/3}$ and $c_0 = 1/\sqrt{3}$ yield a power invariant form of the space vector. In this dissertation, the peak value scaling coefficients are used.

The space vector (2.10) can be presented in a Cartesian coordinate system by using the Clarke transformation (Clarke, 1943). The space vector $\underline{x}^{\mathrm{s}}(t)$ can be expressed as

$$\underline{x}^{\mathrm{s}}(t) = x_\alpha(t) + \mathrm{j}x_\beta(t), \tag{2.13}$$

where the following matrix relation is used

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} x_{\mathrm{A}} \\ x_{\mathrm{B}} \\ x_{\mathrm{C}} \end{bmatrix}. \tag{2.14}$$

The zero-sequence component is similar to Eq. (2.11) in the alpha-beta coordinate system. To best describe the three-phase system, the peak phase vectors and a single space vector

are illustrated in the alpha-beta coordinate system in Fig. 2.10. The direction of phase A is equal to the direction of the alpha component. The space vector is calculated with symmetrical phase peak values and phase shift angles of $\phi_A = 0$, $\phi_B = -2\pi/3$, and $\phi_C = -4\pi/3$, at $t = t_1$ when $\theta = \pi/4$.

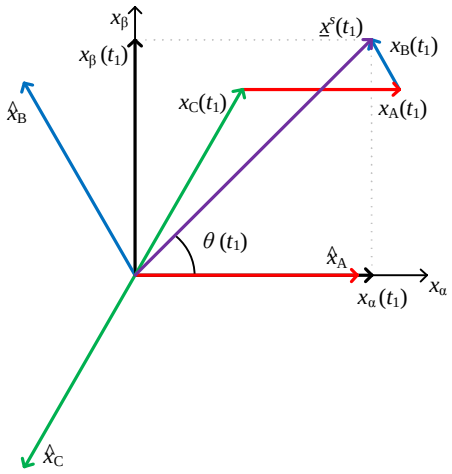


Fig. 2.10. Three-phase system $(x_A, x_B, x_C)$ in alpha-beta coordinates $(x_\alpha, x_\beta)$ and a single space vector $\underline{x}^s$ divided into abc components and αβ components at $t = t_1$ when $\theta = \pi/4$.

Using the space vector theory for the three-phase voltage of the inverter semiconductor bridge shown in Fig. 2.7, a hexagon will be generated to the alpha-beta coordinate system. The hexagon is shown in Fig. 2.11, with the eight discrete output voltage vectors $V_m$, where $m = \{0,1 \dots ,7\}$. The output voltage vectors form the six sectors of the hexagon, $m = \{1,2 \dots ,6\}$. The hexagon is used in the space vector pulse width modulator (SVPWM). The sectors are formed so that the sectors $m = \{1,2 \dots ,5\}$ are limited by the voltage vectors $V_m$ and $V_{m+1}$, and the sector $m = 6$ is limited by the voltage vectors $V_6$ and $V_1$.

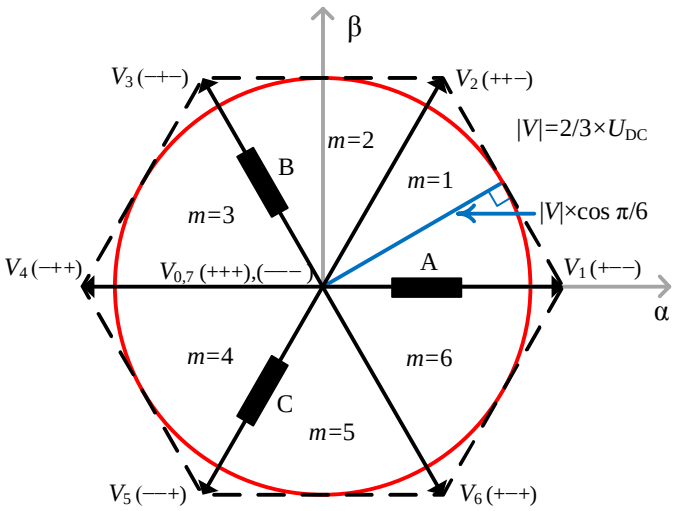


Fig. 2.11. Space vector modulator hexagon with the sectors and the voltage vectors.

The output voltage space vectors differing from the discrete voltage vectors can be applied by averaging the use of the discrete voltage vectors. The space vector can be divided into components of the active voltage vectors $V_m$ and $V_{m+1}$ in the sector $m$ during the switching period $T_s$ as

$$\underline{u}^s(t) = \frac{t_m}{T_s} V_m + \frac{t_{m+1}}{T_s} V_{m+1}, \tag{2.15}$$

where $t_m$ and $t_{m+1}$ are the active times of the corresponding vectors and are limited as

$$T_s \geq t_m + t_{m+1}. \tag{2.16}$$

The voltage vectors are defined as

$$V_m = \frac{2}{3} U_{\mathrm{DC}} \, \mathrm{e}^{j\frac{\pi}{3}(m-1)}, \tag{2.17}$$

$$V_{m+1} = \frac{2}{3} U_{\mathrm{DC}} \, \mathrm{e}^{j\frac{\pi}{3}(m)}. \tag{2.18}$$

As can be seen in Eqs. (2.17) and (2.18), the length of the voltage vector is directly proportional to the DC link voltage. Thus, the radius of the maximum circle inside of the hexagon is also proportional to the DC link voltage

$$\max\left|\underline{u}^{s}_{\mathrm{circ}}\right| = \frac{2}{3} U_{\mathrm{DC}} \cos\frac{\pi}{6} = \frac{U_{\mathrm{DC}}}{\sqrt{3}} \tag{2.19}$$

In order to produce the desired output voltage vector by average, the zero vectors $V_0$ or $V_7$ have to be used for the rest of the time. The component division of a single output reference space vector can be seen in Fig. 2.12.

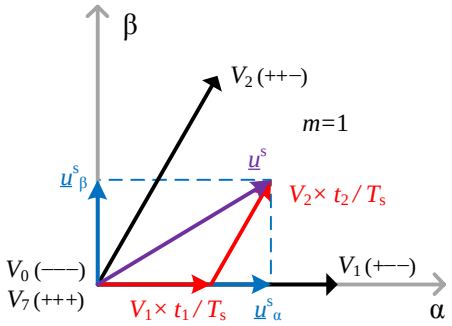


Fig. 2.12. A single output voltage vector and the component division of the vector in the alpha-beta coordinates and the active voltage vectors.

## 2.2.3 Common-mode voltage of an inverter

The generated common-mode voltage of an inverter is defined as the average of the phase leg output voltages,

$$u_{\mathrm{CM}} = \frac{u_{\mathrm{A}} + u_{\mathrm{B}} + u_{\mathrm{C}}}{3}. \tag{2.20}$$

In a two-level three-phase voltage source inverter, where the possible output phase leg voltages could be either $U_{\mathrm{DC}} / 2$ or $-U_{\mathrm{DC}} / 2$, the common-mode voltage can only be zero if the DC link voltage is zero. The possible common-mode voltages are listed in Table 2.1, where the two different output voltages are indicated by + for $U_{\mathrm{DC}} / 2$ and − for $-U_{\mathrm{DC}} / 2$.

Table 2.1
Two-level inverter output voltage vectors and the corresponding common-mode voltages.

| Output vector ($u_{\mathrm{A}}$, $u_{\mathrm{B}}$, $u_{\mathrm{C}}$) | Common-mode voltage, $u_{\mathrm{CM}}$ |
|---|---|
| (+ + +) | $U_{\mathrm{DC}} / 2$ |
| (+ + −), (+ − +), (− + +) | $U_{\mathrm{DC}} / 6$ |
| (+ − −), (− + −), (− − +) | $-U_{\mathrm{DC}} / 6$ |
| (− − −) | $-U_{\mathrm{DC}} / 2$ |

The common-mode voltages can be better illustrated with a figure of a single switching period of a PV inverter. The output phase voltage of the inverter bridge and the common-mode voltage during a single switching period of a synchronous space-vector-modulated PV inverter can be seen in Fig. 2.13.

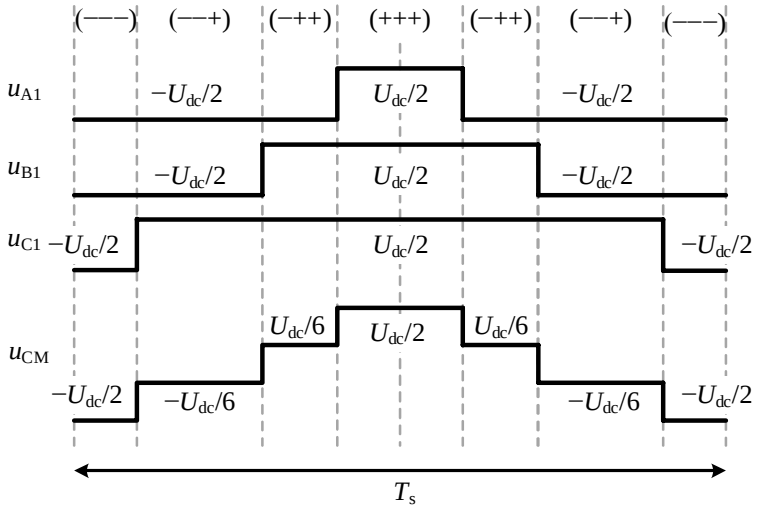


Fig. 2.13. Output voltages and common-mode voltages of a single random switching period of a PV inverter with the voltage vectors shown on the top.

The relation between the different output voltage vectors varies depending on the location of the voltage space vector. During a fundamental grid period, the output voltage space vector rotates a single circle in the hexagon. The modulation index during the operation depends on the ratio between the desired output voltage vector and the DC link voltage that limits the hexagon

$$M = \frac{|\underline{u}^s|}{\max|\underline{u}^s_{\text{circ}}|} = \frac{\sqrt{3}|\underline{u}^s|}{U_{\text{DC}}}. \tag{2.21}$$

Modulation indices larger than 1.0 are considered overmodulated vectors. More information about the overmodulation can be found in (Holtz, 1993). The overall common-mode voltage content during a fundamental period depends on the modulation index of the output voltage vectors. A Fast Fourier Transform (FFT) of the common-mode output voltage of a two-level inverter is illustrated in Fig. 2.14 with a constant modulation index of 1.0, a DC link voltage of 1 p.u., a sample period length of 1 µs, and a switching frequency of 10 kHz. The inherent property of the SVPWM is the addition of the third harmonic component of the fundamental frequency. This 150 Hz component is larger with larger modulation indices.

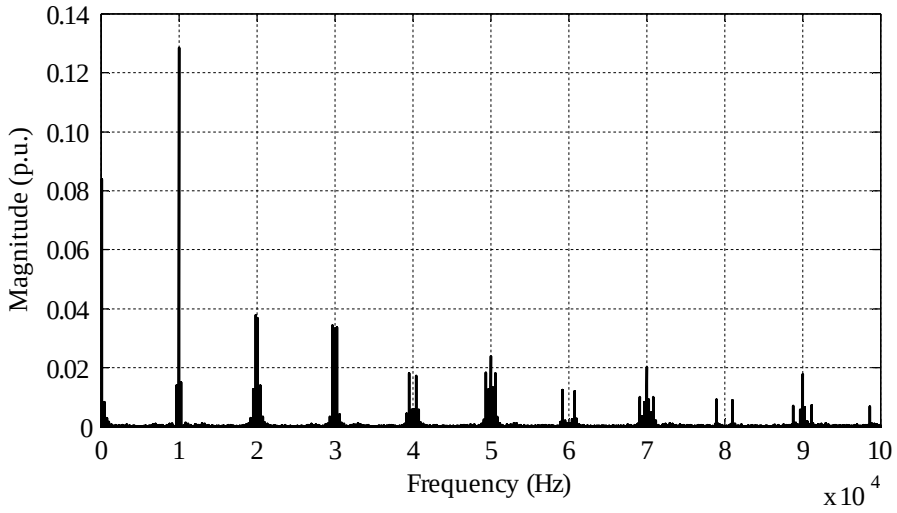


Fig. 2.14. FFT analysis of the output common-mode voltage over a single grid fundamental period of a SVPWM inverter with a 10 kHz switching frequency, 1 p.u. DC link voltage, and a 1.0 modulation index. The RMS value of the switching frequent component is 0.128 p.u.

With a higher modulation index, the injected third harmonic is larger and the switching frequency component is smaller since the zero-vectors that generate more common-mode voltage are used to a smaller extent. The main frequency components of the common-mode output voltage of the inverter are gathered in Table 2.2 with different modulation indices. The modulation indices are between 0.8 and 1.0, which is the usual scale in PV inverters that do not use overmodulation. The sidebands in Fig. 2.14 are calculated to the corresponding high-frequency component root mean square (RMS) value in Table 2.2.

Table 2.2
RMS values of the primary frequency components of a common-mode voltage generated by a two-level inverter with different modulation indices.

| Modulation index, *M* | 150 Hz component | 10 kHz component | 20 kHz component | 30 kHz component | 50 kHz component | 70 kHz component |
|---|---|---|---|---|---|---|
| 1.0 | 0.085 p.u. | 0.128 p.u. | 0.056 p.u | 0.060 p.u | 0.039 p.u | 0.028 p.u |
| 0.95 | 0.080 p.u. | 0.154 p.u. | 0.057 p.u | 0.072 p.u | 0.047 p.u | 0.035 p.u |
| 0.9 | 0.076 p.u. | 0.180 p.u | 0.058 p.u | 0.084 p.u | 0.055 p.u | 0.040 p.u |
| 0.85 | 0.072 p.u. | 0.205 p.u | 0.059 p.u | 0.095 p.u | 0.058 p.u | 0.038 p.u |
| 0.8 | 0.068 p.u. | 0.230 p.u | 0.059 p.u | 0.101 p.u | 0.055 p.u | 0.029 p.u |

As illustrated in Table 2.2, the 150 Hz component is directly proportional to the modulation index, contrary to the switching frequency component and its multiple components.

The three-level inverters in Fig. 2.8 have three possible output phase leg voltages, the voltage of the positive and negative DC buses and the voltage of the neutral point. In a symmetric PV inverter, where the neutral point is connected to the ground potential, the possible output voltages are $U_{DC}/2$, $-U_{DC}/2$, and 0. The corresponding output voltages are denoted by $+$, $-$, and 0 in Table 2.3, where the different common-mode voltages with different output voltage vectors are indicated.

Table 2.3
Three-level inverter output voltages and common-mode voltages.

| Output vector ($u_A$, $u_B$, $u_C$) | Common-mode voltage $u_{CM}$ |
|---|---|
| (+ + +) | $U_{DC}$ / 2 |
| (+ + 0), ( + 0 +), (0 + +) | $U_{DC}$ / 3 |
| (+ + −), (+ − +), (− + +), (+ 0 0), (0 + 0), (0 0 +) | $U_{DC}$ / 6 |
| (+ − 0), (+0 −), (− + 0), (0 + −), (− + 0), (0 − +), (0 0 0) | 0 |
| (+ − −), (− + −), (− − +), (− 0 0), ( 0 − 0), (0 0 −) | $-U_{DC}$ / 6 |
| (− − 0), (− 0 −), (0 − −) | $-U_{DC}$ / 3 |
| (− − −) | $-U_{DC}$ / 2 |

## 2.2.4 Common-mode current of a PV inverter

The common-mode voltage generated by the PV inverter will produce a common-mode current if there is a valid path in the system. In residential power systems, the neutral point of the low-voltage grid is always connected to the ground. In transformerless PV inverters, the path for the common-mode current is completed through the ground capacitances of the solar panels on the DC side presented in Section 2.1.1 and the grounded grid neutral point on the AC side. An isolating transformer shuts off the path of the common-mode current, and therefore, only transformerless inverters are discussed here. The common-mode circuit of a single PV inverter, connected to a grounded low-voltage grid is shown in Fig. 2.15.

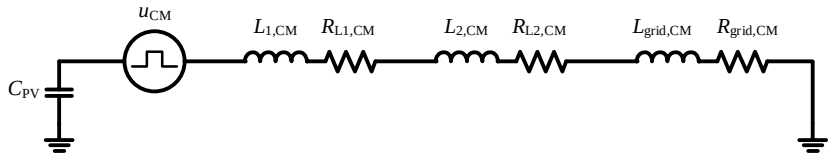


Fig. 2.15. Main components of a common-mode circuit of a grid-connected transformerless PV inverter and solar panels.

The common-mode current generated by the inverter is called a leakage current. The maximum leakage current is limited in a safety standard perspective by the current limit of the residual-current device. The residual-current device is designed to detect residual

currents and prevent an electrocution in locations where a direct contact with a person is possible. The device measures the common-mode current and disconnects the installation if the common-mode current exceeds the limit of 30 mA (IEC, 2011). In a situation when a person is in contact with a live voltage and a ground potential, the DC current will start to flow. Thus, the residual-current devices are only required to be low-frequency devices, and a larger leakage current at the switching frequency may not be detected by the residual-current device. However, the leakage current should be limited so that false disconnections do not appear in the residual-current device and also because the leakage current generates extra losses. The fault current is referred to as residual current in Fig. 2.16 that illustrates the common-mode currents of PV inverters (VDE, 2013).

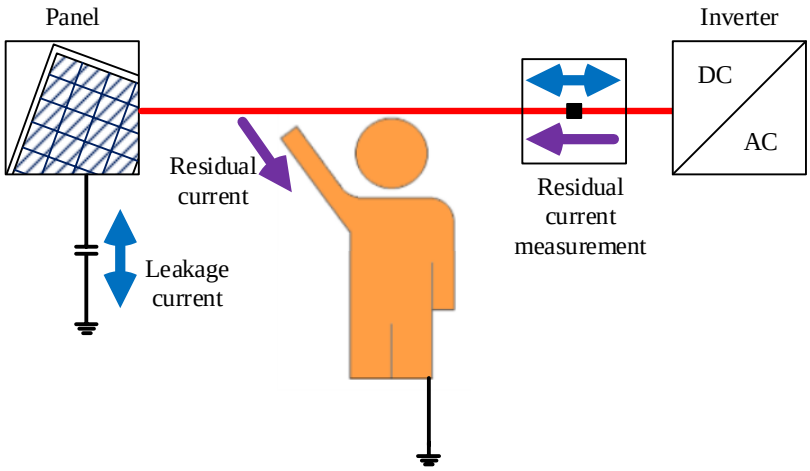


Fig. 2.16. Two types of common-mode currents of a PV system, the leakage current and the residual current. The residual current has to be detected for safety reasons.

In locations where the direct contact with a person is prevented with adequate preparations, the fault current limit is 300 mA (IEC, 2011). This limit is given to prevent fire hazards. By building fences around the solar plant, the panels can be isolated from persons, and thus, a larger fault current limit can be used.

## 2.3 Parallel-connected inverters

The power rating of the system can be increased beyond the power rating of a single semiconductor device by connecting the semiconductor devices in parallel or in series. The semiconductor devices can be connected in series in the phase legs of a single inverter thereby increasing the voltage rating of the inverter (Sasagawa et al., 2004) or in parallel in the phase legs of a single inverter thus increasing the current carrying capacity of the inverter (Azar et al., 2008). A more modular solution is to connect the power converter

blocks in parallel to increase the current of the system (Turner et al., 2010) or in series to increase the voltage of the system (Naumanen et al., 2009).

In the PV systems, the series connection of the semiconductor devices or the inverters is not recommended, since the maximum DC voltage level of the system is limited to 1000 V or 1500 V by the solar panels. With these voltage levels, the series connection is not necessary, since single semiconductors can withstand the required voltage levels. The parallel connection of the semiconductor devices is possible, but it will increase the amount of power generation connected to a single MPPT and hence decrease the efficiency of the MPPT especially in shaded conditions (Mäki and Valkealahti, 2012). Thus, connecting whole inverters in parallel is the preferred solution in order to increase the power level of the system beyond the power rating of a single semiconductor device in the PV applications (Borrega et al., 2013).

Parallel-connected inverters have been used in the drives applications for decades (Chandorkar et al., 1993). In a drive application, the inverters may be connected to the same DC link on the DC side. This denotes the demand for simultaneous switchings in the parallel inverters. Different switching states at the matching phase legs of the inverters generate a circulating current that is limited only by the inductances and resistances of the filters. The parallel connection can be implemented even without the individual intermodule filters when the synchronization is accurate enough (Itkonen et al., 2006). The parallel-connected inverters with a common DC link are depicted in Fig. 2.17.

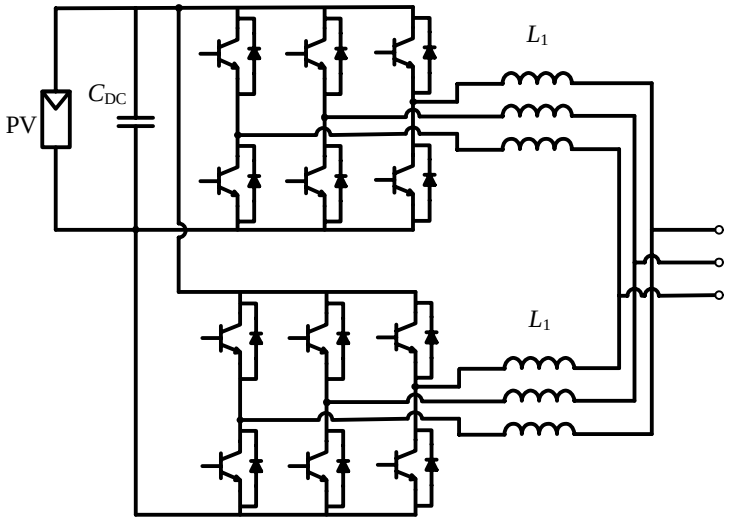


Fig. 2.17. Main circuit diagram of parallel-connected inverters with a shared DC link.

Large solar plants that require more than a single inverter spread across a wide area. In order to keep the solar plant modular and to reduce the need for an extra cabling, the PV

inverters may be situated hundreds of meters apart. The wide-spread PV inverters are individual units that have DC links and grid filters of their own. Even though the PV inverters are individual units that do not share the DC link, the mountings of the solar panels generate a capacitive connection to the ground potential and connect the DC sides of the PV inverters together.

### 2.3.1 Common-mode voltage of the parallel-connected inverters

The common-mode voltages of the individual inverters behave similarly as the common-mode voltages of the single PV inverters. However, the common-mode circuit becomes different in parallel-connected PV inverters that are isolated from the grounded grid. The parallel connection of two inverters has two independent common-mode voltage sources that are connected to the ground only from the DC sides of the inverters and are connected together on the AC side. This simplified common-mode setup is illustrated in Fig. 2.18.

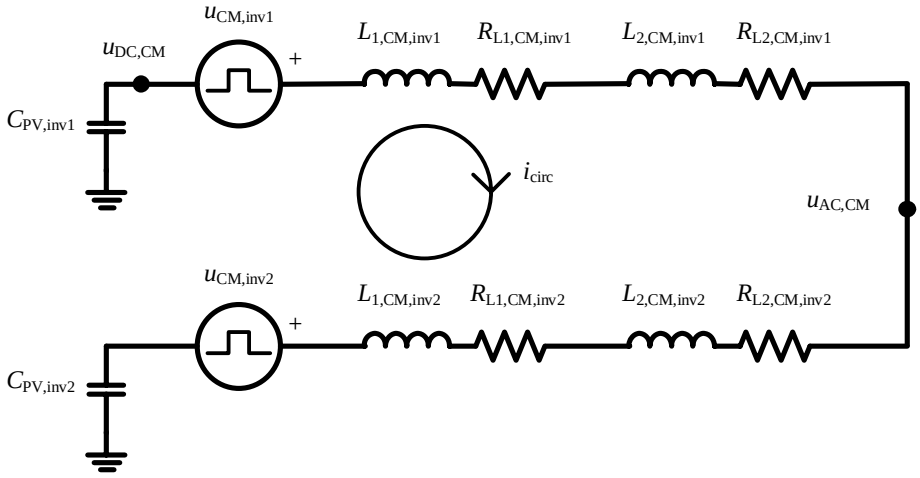


Fig. 2.18. Common-mode circuit of two parallel-connected PV inverters with solar panels.

The common-mode voltage towards the ground potential on the DC side of the inverter $u_{\mathrm{DC,CM}}$ is determined by the voltage of the solar panel parasitic capacitance. The voltage over the capacitance is calculated as

$$u_{\mathrm{DC,CM}}(t) = \frac{1}{C_{\mathrm{PV,inv1}}} \int_0^t i_{\mathrm{circ}}(\tau) d\tau. \tag{2.22}$$

Equation (2.22) shows that the common-mode voltage on the DC side of the inverter is determined by the common-mode current of the inverter in question. The high-frequency

common-mode voltage ripple amplitude is derived by the common-mode current ripple amplitude.

To calculate the common-mode voltage on the AC side of the grid filter $u_{\mathrm{AC,CM}}$, the circuit is analyzed in the Laplace domain. First, Kirchhoff's voltage law is applied to the circuit illustrated in Fig. 2.18. Since the inductances and resistances of the LCL filters are series connected, they can be simply summed together as

$$R_{\mathrm{LCL}} = R_{\mathrm{L1,CM}} + R_{\mathrm{L2,CM}}, \tag{2.23}$$

$$L_{\mathrm{LCL}} = L_{1,\mathrm{CM}} + L_{2,\mathrm{CM}}. \tag{2.24}$$

With Eqs. (2.23) and (2.24), Kirchhoff's voltage law for two parallel-connected inverters can be written as

$$U_{\mathrm{CM,inv1}} - U_{\mathrm{CM,inv2}} = \frac{1}{\mathrm{s}C_{\mathrm{PV,inv1}}} I_{\mathrm{circ}} + I_{\mathrm{circ}}\left(R_{\mathrm{LCL,inv1}} + \mathrm{s}L_{\mathrm{LCL,inv1}}\right) + \tag{2.25}$$

$$\frac{1}{\mathrm{s}C_{\mathrm{PV,inv2}}} I_{\mathrm{circ}} + I_{\mathrm{circ}}\left(R_{\mathrm{LCL,inv2}} + \mathrm{s}L_{\mathrm{LCL,inv2}}\right).$$

The circulating current can be solved as

$$I_{\mathrm{circ}} = \frac{U_{\mathrm{CM,inv1}} - U_{\mathrm{CM,inv2}}}{Z_{\mathrm{inv1}} + Z_{\mathrm{inv2}}}, \tag{2.26}$$

where

$$Z_{\mathrm{inv1}} = R_{\mathrm{LCL,inv1}} + \mathrm{s}L_{\mathrm{LCL,inv1}} + \frac{1}{\mathrm{s}C_{\mathrm{PV,inv1}}}, \tag{2.27}$$

$$Z_{\mathrm{inv2}} = R_{\mathrm{LCL,inv2}} + \mathrm{s}L_{\mathrm{LCL,inv2}} + \frac{1}{\mathrm{s}C_{\mathrm{PV,inv2}}}, \tag{2.28}$$

Using the upper inverter (inv1) and Kirchhoff's voltage law, the AC common-mode voltage can be calculated as

$$U_{\mathrm{AC,CM}} = U_{\mathrm{CM,inv1}} - Z_{\mathrm{inv1}} I_{\mathrm{circ}}. \tag{2.29}$$

By combining Eqs. (2.26) and (2.29), the circulating current can be eliminated from the AC side common-mode voltage equation as

$$U_{\mathrm{AC,CM}} = U_{\mathrm{CM,inv1}} + \frac{\left(U_{\mathrm{CM,inv2}} - U_{\mathrm{CM,inv1}}\right)Z_{\mathrm{inv1}}}{Z_{\mathrm{inv1}} + Z_{\mathrm{inv2}}} = \frac{U_{\mathrm{CM,inv1}}Z_{\mathrm{inv2}} + U_{\mathrm{CM,inv2}}Z_{\mathrm{inv1}}}{Z_{\mathrm{inv1}} + Z_{\mathrm{inv2}}} \quad (2.30)$$

Equation (2.30) can be simplified in the special case of identical LCL filters and identical solar panel capacitances as $Z_{\mathrm{inv1}} = Z_{\mathrm{inv2}} = Z_{\mathrm{inv}}$.

$$U_{\mathrm{AC,CM}} = \frac{U_{\mathrm{CM,inv1}}Z_{\mathrm{inv}} + U_{\mathrm{CM,inv2}}Z_{\mathrm{inv}}}{2Z_{\mathrm{inv}}} = \frac{U_{\mathrm{CM,inv1}} + U_{\mathrm{CM,inv2}}}{2} \quad (2.31)$$

With identical passive components, the AC side common-mode voltage is the arithmetic mean of the generated common-mode voltages of the two parallel inverters. With different passive component values, the AC side common-mode voltage is not directly the arithmetic mean of the generated common-mode voltages, but the result of the voltage division between the passive components. The same can be generalized for multiple parallel PV inverters, by calculating the circulating current with a mesh analysis given in Appendix A. The following equation is derived for $n$ parallel inverters with identical passive component values from Eqs. (2.29) and (A.24).

$$U_{\mathrm{AC,CM}} = \frac{U_{\mathrm{CM,inv1}} + U_{\mathrm{CM,inv2}} + U_{\mathrm{CM,inv3}} + \cdots + U_{\mathrm{CM,inv}n}}{n} \quad (2.32)$$

With unequal passive components, the AC common-mode voltage will be the result of a voltage division between the impedances according to Eqs. (2.29) and (A.11) as

$$U_{\mathrm{AC,CM}} = U_{\mathrm{CM,inv1}} - Z_{\mathrm{inv1}}\frac{\det(\boldsymbol{Z_1})}{\det(\boldsymbol{Z})}, \quad (2.33)$$

where $\boldsymbol{Z}$ is an impedance matrix and $\boldsymbol{Z_1}$ is a matrix containing impedances and voltages. The matrixes are indicated in Appendix A.

### 2.3.2 Circulating current between parallel-connected inverters

The circulating current in parallel-connected inverters is similar to the common-mode current of a single PV inverter, except that the current path is closed by the ground capacitances of the other inverters instead of the grid neutral point. With two parallel inverters, there are two common-mode voltage sources as illustrated in Fig. 2.18.

Every component in Fig. 2.18 is series connected, and thus, the location of the components can be changed to build a more simplified equivalent circuit for the circulating current with a setup of two parallel-connected inverters. The capacitances are moved to the right-hand side of the voltage sources, and all the passive components are connected in series as shown in Eqs. (2.35)–(2.37). The simplified equivalent circuit is illustrated in Fig. 2.19. The two

common-mode voltage sources are combined to get the common-mode voltage component that generates the circulating current as

$$u_{\mathrm{CM,tot}} = u_{\mathrm{CM,inv1}} - u_{\mathrm{CM,inv2}}. \tag{2.34}$$

$$R_{\mathrm{tot}} = R_{\mathrm{LCL,inv1}} + R_{\mathrm{LCL,inv2}} \tag{2.35}$$

$$L_{\mathrm{tot}} = L_{\mathrm{LCL,inv1}} + L_{\mathrm{LCL,inv2}} \tag{2.36}$$

$$C_{\mathrm{tot}} = \frac{C_{\mathrm{PV,inv1}} * C_{\mathrm{PV,inv2}}}{C_{\mathrm{PV,inv1}} + C_{\mathrm{PV,inv2}}} \tag{2.37}$$

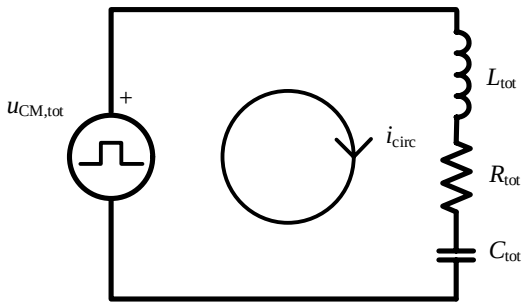


Fig. 2.19. Simplified equivalent common-mode circuit of two parallel-connected PV inverters with the solar panels.

As indicated in Eq. (2.34) and in Fig. 2.19, the circulating current is produced by the common-mode voltage difference between the two inverters and the series resonant RLC circuit containing all of the components in the circulating current path. The identifying parameters of the series RLC circuit are the damping factor $\zeta$ and the angular resonant frequency $\omega_{\mathrm{r}}$, which can be calculated as

$$\zeta = \frac{R_{\mathrm{tot}}}{2}\sqrt{\frac{C_{\mathrm{tot}}}{L_{\mathrm{tot}}}}, \tag{2.38}$$

$$\omega_{\mathrm{r}} = \frac{1}{\sqrt{L_{\mathrm{tot}}C_{\mathrm{tot}}}}. \tag{2.39}$$

In the Laplace domain, the circulating current component can be solved as

$$I_{\mathrm{circ}} = \frac{\mathrm{s}}{L_{\mathrm{tot}}\left(\mathrm{s}^2 + \frac{R_{\mathrm{tot}}}{L_{\mathrm{tot}}}\mathrm{s} + \frac{1}{L_{\mathrm{tot}}C_{tot}}\right)} U_{\mathrm{CM,tot}}. \tag{2.40}$$

Combining Eqs. (2.38), (2.39), and (2.40), the circulating current can be expressed as

$$I_{\mathrm{circ}} = \frac{\mathrm{s}}{L_{\mathrm{tot}}(\mathrm{s}^2 + 2\zeta\omega_{\mathrm{r}}\mathrm{s} + \omega_{\mathrm{r}}^2)} U_{\mathrm{CM,tot}}. \tag{2.41}$$

When the system contains multiple parallel-connected PV inverters as illustrated in Fig. 2.20, the circulating current has to be calculated with a mesh analysis presented in Appendix A. The circulating current with unequal inverter impedances is given in Appendix A. The combined circulating current of the first inverter $I_{\mathrm{CM,inv1}}$ can be calculated with $n$ parallel inverters and an identical impedance $Z_{\mathrm{inv}}$ as

$$I_{\mathrm{CM,inv1}} = \frac{(n-1)U_{\mathrm{CM,inv1}} - U_{\mathrm{CM,inv2}} - U_{\mathrm{CM,inv3}} - \cdots - U_{\mathrm{CM,inv}n}}{nZ_{\mathrm{inv}}}. \tag{2.42}$$

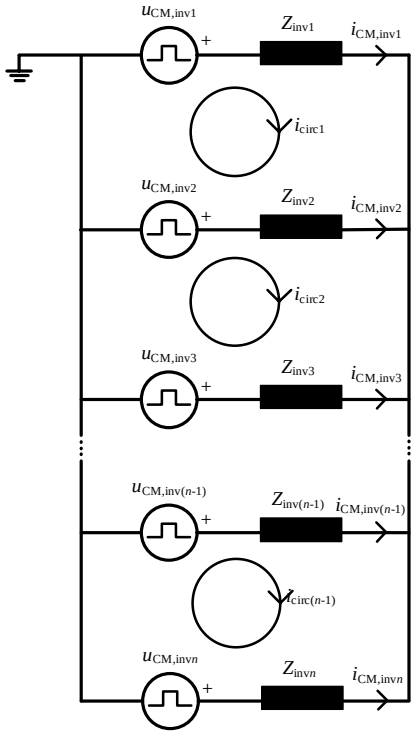


Fig. 2.20. Simplified common-mode circuit diagram of a parallel connection of $n$ inverters.

## 2.4 Inverter synchronization

In order to minimize the circulating current between two parallel-connected inverters, the common-mode voltage difference between the two inverters should be minimized, as indicated in Eq. (2.40). With multiple parallel-connected inverters, generating identical common-mode voltage in all of the inverters will neglect the circulating current as shown in Eq. (A.12).

As stated in Section 1.1, the parallel-connected PV inverters should have independent controls to maximize the energy harvesting. Without interfering with the energy harvesting, the common-mode voltage difference between the inverters can be minimized by synchronizing the parallel inverters. Synchronization refers to a situation when the switching periods of parallel inverters begin at the same time, in other words, the phase difference between the modulators is 0°. The hysteresis modulators are excluded from this and the following sections of the dissertation. The synchronization is limited to modulators that operate at a constant switching frequency, such as the carrier-based pulse width modulator and the space-vector pulse width modulator (SVPWM).

In the drives applications, the parallel-connected inverters are usually synchronized with a communication link. The communication can be a simple synchronization signal between a master and a slave inverter or a single master controller that controls all of the inverters. In order to guarantee a synchronized operation, the communication link is required to be bidirectional so that the communication delay can be determined (Laakkonen et al., 2009).

To elucidate the synchronization, an illustration of single-phase switching commands $sw_{\mathrm{inv1}}$ and $sw_{\mathrm{inv2}}$ of two modulators with a common switching period length $T_{\mathrm{s}}$, a common modulation reference $m$, and two different phase differences of 90° and 0° (synchronized) is given in Fig. 2.21. A carrier-based modulator triangle wave illustration is chosen to represent the modulators. The switching commands $sw_{\mathrm{inv1}}$ and $sw_{\mathrm{inv2}}$ can be derived from the inverter output voltage in a single-phase system

$$sw = \frac{u_1}{u_{\mathrm{DC}}}. \tag{2.43}$$

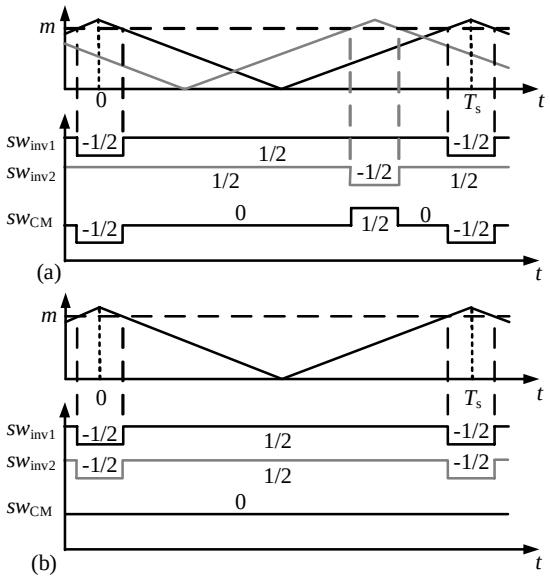


Fig. 2.21. Two modulators with (a) a 90° phase shift between the modulators and (b) a synchronized operation of the modulators. The corresponding switching states and the combined common-mode voltage difference with identical modulation references are in the bottom figures for both cases.

The same can be applied to the three-phase system for each phase. The common-mode voltage is defined as the average of the output phase voltages of the inverter in Eq. (2.20). The average of the output phase voltages of a single-phase system is the voltage of the single phase. Thus, the common-mode voltage of a single-phase system is equal to the output phase voltage. The common-mode voltage difference between the two single-phase inverters is the output voltage difference of the inverters

$$u_{\mathrm{CM,tot}} = u_{1,\mathrm{inv1}} - u_{1,\mathrm{inv2}}. \tag{2.44}$$

By combining Eqs. (2.43) and (2.44), a common-mode difference switching function can be obtained for the single-phase system

$$sw_{\mathrm{CM}} = sw_{\mathrm{inv1}} - sw_{\mathrm{inv2}} = \frac{u_{1,\mathrm{inv1}}}{u_{\mathrm{DC,inv1}}} - \frac{u_{1,\mathrm{inv2}}}{u_{\mathrm{DC,inv2}}}. \tag{2.45}$$

The three-phase common-mode difference switching function can be calculated by Eqs. (2.20) and (2.45):

$$sw_{\mathrm{CM,tot}} = \frac{u_{1,\mathrm{A,inv1}} + u_{1,\mathrm{B,inv1}} + u_{1,\mathrm{C,inv1}}}{3u_{\mathrm{DC,inv1}}} - \frac{u_{1,\mathrm{A,inv2}} + u_{1,\mathrm{B,inv2}} + u_{1,\mathrm{C,inv2}}}{3u_{\mathrm{DC,inv2}}}. \quad (2.46)$$

### 2.4.1 Common-mode voltage difference of parallel inverters with a phase difference

The common-mode voltage difference is zero during a single switching period only if the common-mode voltage waveforms are identical and perfectly synchronized during the switching period. Even when the parallel inverters are identical with identical common-mode voltage waveforms, a phase difference between the common-mode voltages generates a circulating current.

As indicated in Fig. 2.14 and in Table 2.2, the generated common-mode voltage of a single inverter contains multiple different frequency components. The phase difference between the two modulators is calculated of the switching period length, and it describes the behavior of the switching frequency component. A 180° phase difference equals the worst case, when the common-mode voltage difference (2.34) can be calculated for identical common-mode voltages as

$$u_{\mathrm{CM,tot}} = u_{\mathrm{CM,inv1}} - \left(\mathrm{e}^{-\mathrm{j}180^{\circ}} u_{1,\mathrm{inv1}}\right) = 2u_{\mathrm{CM,inv1}}. \quad (2.47)$$

However, the 180° phase difference at the switching frequency represents a 360° phase difference, and a perfect synchronization, for the second harmonic of the switching frequency component. The RMS values of the different frequency components of the common-mode voltage difference $u_{\mathrm{CM,tot}}$ are plotted as a function of phase difference in Fig. 2.22. The figure is produced using identical common-mode voltages, a sample period length of 1µs, a switching frequency of 10 kHz, and DC link voltages of 1 p.u. in the parallel inverters. A modulation index $M$ of 0.95 is used in Fig. 2.22, and 0.80 in Fig. 2.23.

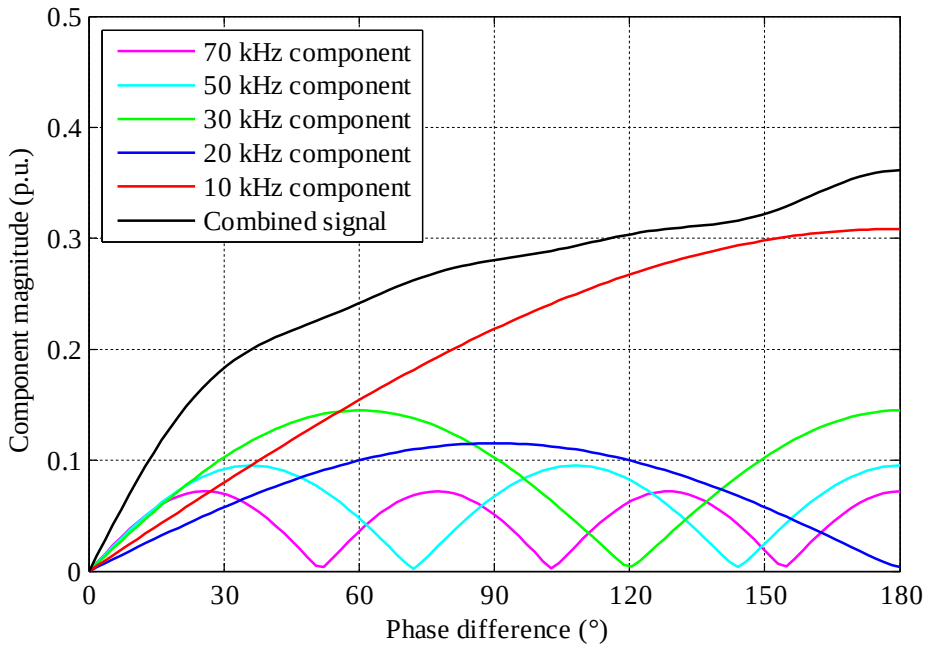


Fig. 2.22. Five main frequency components and the combined signal of the common-mode voltage difference of two inverters with distinct phase differences, identical switching patterns, and DC link voltages of 1.0 p.u. The RMS voltages of individual phase difference points are calculated over 100 ms. The modulation index is 0.95. The phase difference in the x-axis is the phase difference of the switching frequency component.

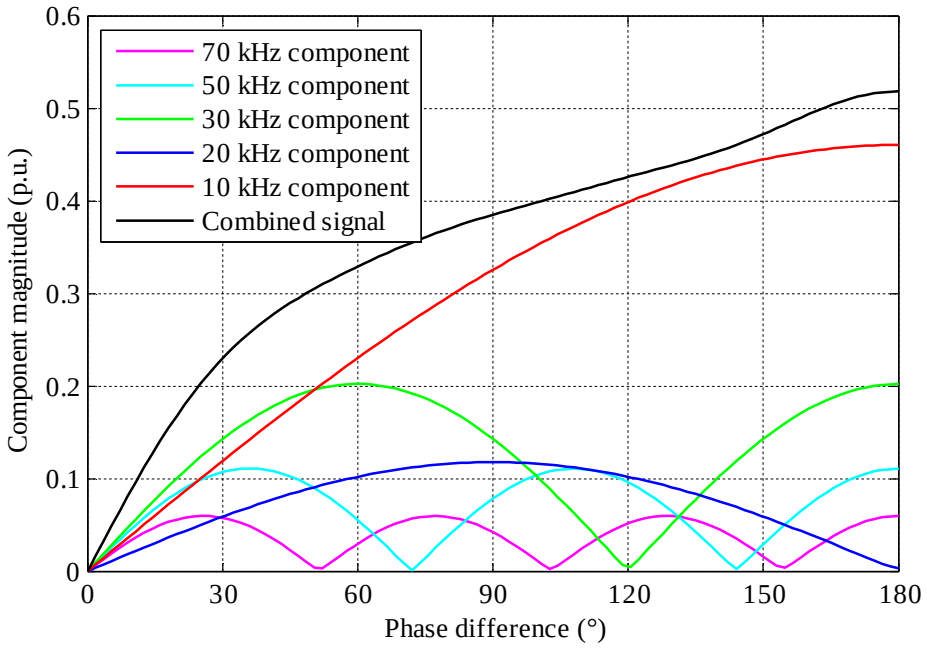


Fig. 2.23. Five main frequency components and the combined signal of the common-mode voltage difference of two inverters with distinct phase differences, identical switching patterns, and DC link voltages of 1.0 p.u. The RMS voltages of individual phase difference points are calculated over 100 ms. The modulation index is 0.80. The phase difference in the x-axis is the phase difference of the switching frequency component.

The stimulus for the circulating current, the common-mode voltage difference between the modulators of the two parallel inverters, varies both in amplitude and frequency spectrum according to the phase difference between the modulators. The previous common-mode voltage differences were calculated with identical DC link voltages and switching patterns in the parallel inverters. The zero common-mode voltage difference with the synchronization is only possible if the common-mode voltage difference is zero throughout the fundamental period. The common-mode voltage difference cannot be zero if the inverters have unequal DC link voltages or different switching commands because of individual inverter controllers. The uneven common-mode voltages in the parallel inverters are inevitable in real-life situations, when the inverters are not communicating.

The behavior of the common-mode voltage difference with distinct common-mode voltage sources is illustrated in Fig. 2.24, where the DC link voltages of the inverters are 1.0 p.u. and 1.05 p.u. Since the inverters are connected together on the AC side, the output voltage vectors of the inverters should be similar. Thus, the modulation index is proportionally smaller with the larger DC link voltage. The modulation indices are chosen to be 0.90 for the 1.0 p.u. inverter and 0.857 for the 1.05 p.u. inverter. The sample period is 1 µs.

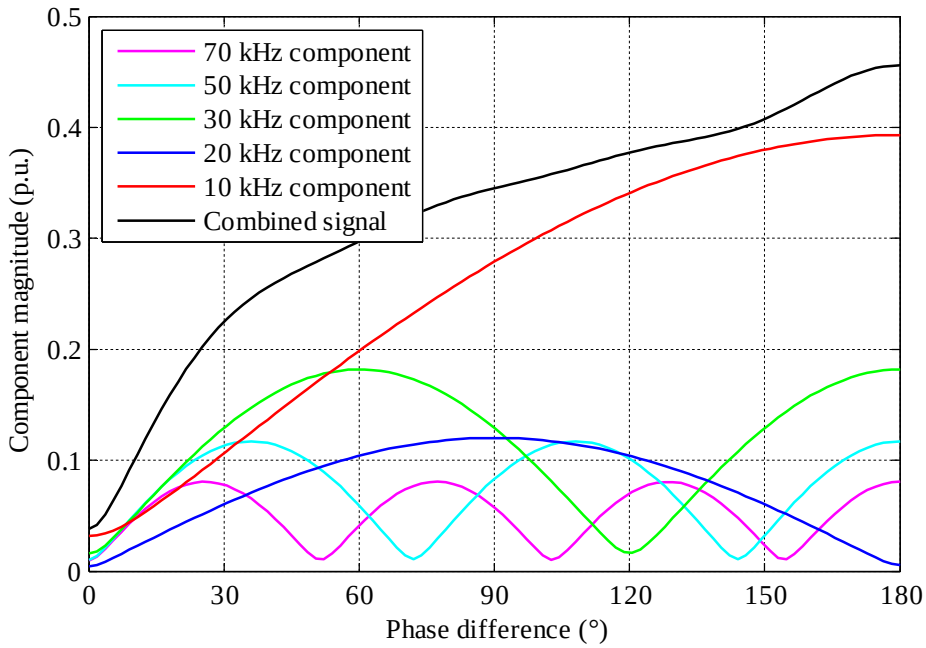


Fig. 2.24. Five main frequency components and the combined signal of the common-mode voltage difference of two inverters with distinct phase differences, the DC link voltages of 1.0 p.u. and 1.05 p.u., and the corresponding modulation indices of 0.90 and 0.857. The RMS voltages of individual phase difference points are calculated over 100 ms. The phase difference in the x-axis is the phase difference of the switching frequency component.

As illustrated in Fig. 2.24, the common-mode voltage difference is nonzero at the phase difference of 0° when the DC link voltages differ in the parallel inverters. The DC link voltage and the modulation index have a 5% difference in Fig. 2.24. A 10% larger DC link voltage is illustrated in Fig. 2.25 with a modulation index of 0.818.

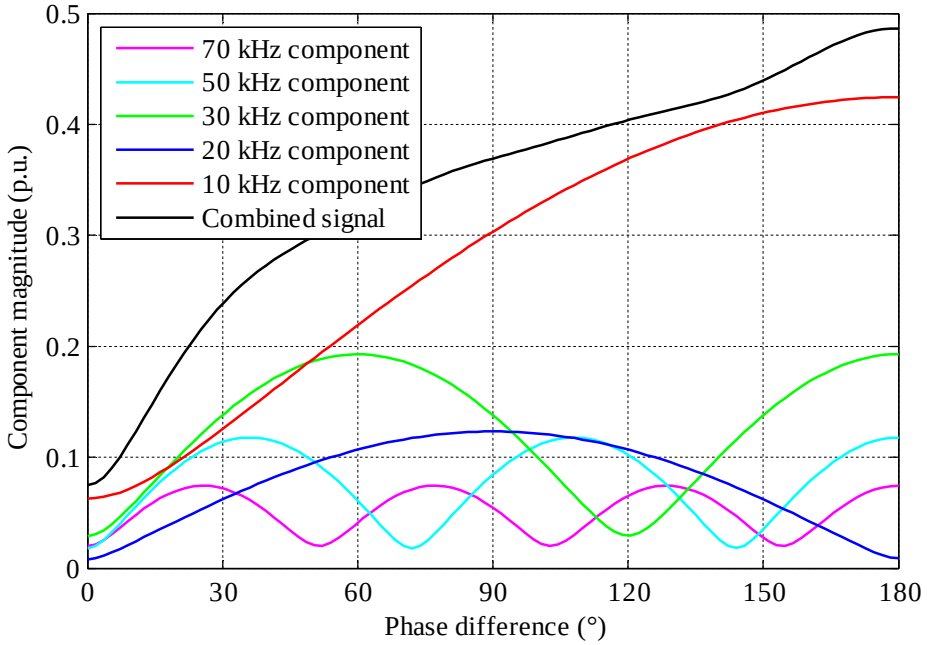


Fig. 2.25. Five main frequency components and the combined signal of the common-mode voltage difference of two inverters with distinct phase differences, the DC link voltages of 1.0 p.u. and 1.1 p.u., and the corresponding modulation indices of 0.90 and 0.818. The RMS voltages of individual phase difference points are calculated over 100 ms. The phase difference in the x-axis is the phase difference of the switching frequency component.

As illustrated in Fig. 2.25, none of the frequency components is zero at any given moment. However, the waveform of the combined signal as a function of phase difference is almost identical with distinct DC link voltages.

### 2.4.2 Circulating current of parallel inverters with a phase difference

The circulating current is generated by the common-mode voltage difference between the parallel inverters and the RLC circuit dynamics of the inverter as explained in Eq. (2.41). The frequency components of the common-mode voltage difference shown in the previous section will behave differently in the RLC circuit. The behavior of the frequency components depends on the frequency response of the RLC circuit. The setup of two parallel inverters seen in Fig. 2.19 is observed here. The RLC circuit of the setup is the series connection of the RLC circuits of the individual inverters. The RLC circuit behavior with different frequencies is illustrated in Fig. 2.26 as a form of a Bode diagram. The resonant frequency of the RLC circuit is determined by the inductance and capacitance values, where the resistance value determines the sharpness and magnitude of the resonance peak.

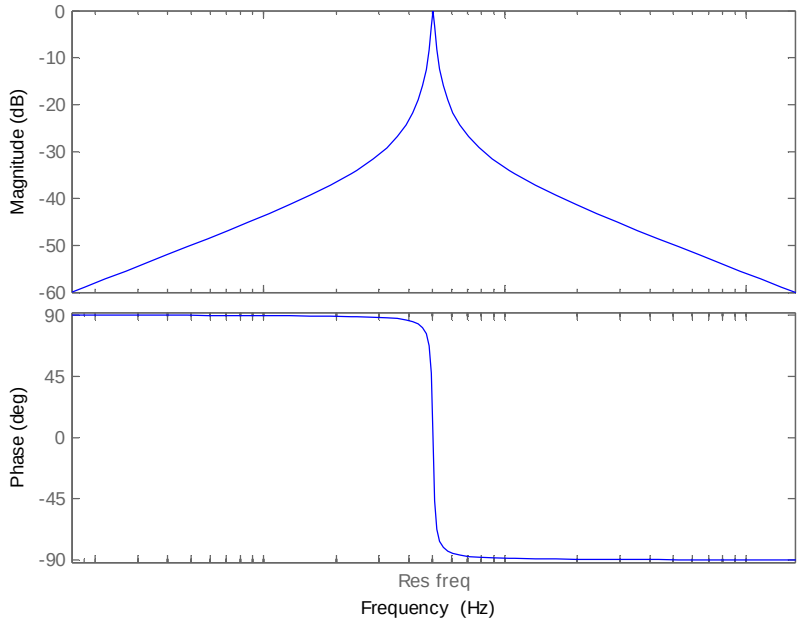


Fig. 2.26. Bode diagram of an RLC circuit.

The circulating current frequency spectrum is determined by the RLC components of the common-mode circuit. The position of the resonance frequency is determined by the common-mode inductances and the PV array ground capacitances. The resonance frequencies of few different setups are calculated by Eq. (2.39) in Table 2.4.

Table 2.4
Common-mode components of a PV setup and their RLC circuit resonance frequencies.

| Setup type | $L_{\mathrm{CM,inv}}$ | $C_{\mathrm{PV,inv}}$ | $f_{\mathrm{res}}$ |
|---|---|---|---|
| 1) 5 kW inverters in dry conditions | 450 µH | 40 nF | 37.5 kHz |
| 2) 5 kW inverters in wet conditions | 450 µH | 440 nF | 11.3 kHz |
| 3) 500 kW inverters in dry conditions | 18 µH | 4 µF | 18.8 kHz |
| 4) 500 kW inverters in wet conditions | 18 µH | 44 µF | 5.6 kHz |

As can be seen in Table 2.4, the RLC circuit resonance frequency is close to the second or third harmonic of the switching frequency during normal operation in dry conditions. The circulating current frequency spectrum with the setups described in Table 2.4 are calculated and similar figures are produced of the circulating current that are shown in Fig. 2.22–Fig. 2.25 for the common-mode voltage difference. The modulation index is 0.95, and the RLC

circuit resistance is 300 mΩ in the following figures. The setup 1 with 5 kW inverters in dry conditions is illustrated in Fig. 2.27. The characteristic impedance of the 5 kW system is chosen to be 50 Ω, which indicates that 1 p.u. current will generate a 1 p.u. voltage loss at a 50 Ω impedance. The impedance of the 500 kW system is chosen to be 2 Ω. The other setups are illustrated in Fig. 2.28, Fig. 2.29, and Fig. 2.30 in a numerical order.

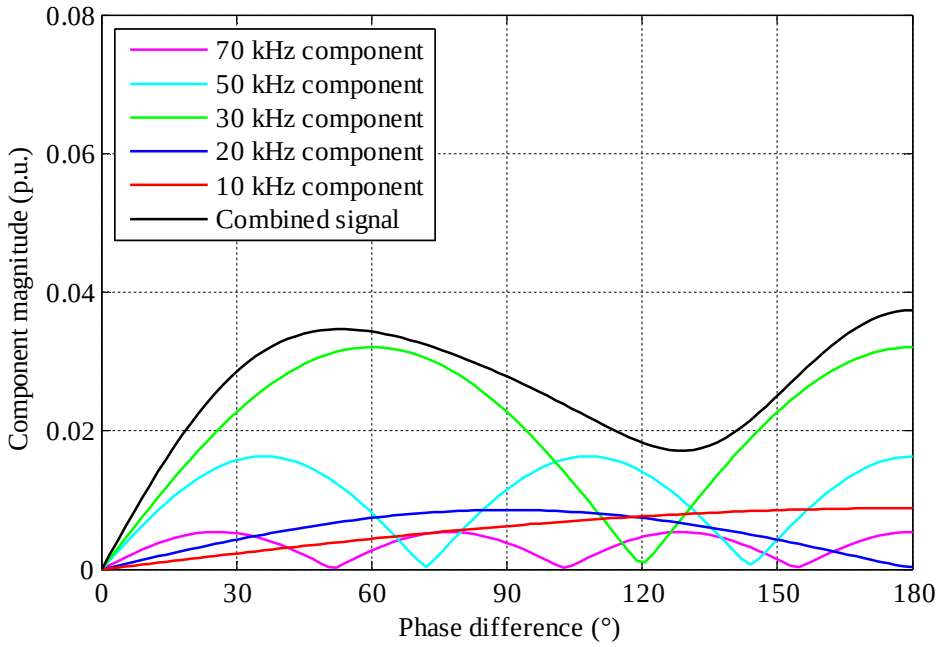


Fig. 2.27. Setup 1 with 5 kW inverters in dry conditions. Five main frequency components and the combined signal of the circulating current between two inverters with distinct phase differences, identical switching patterns, and DC link voltages of 1.0 p.u. The RMS currents of individual phase difference points are calculated over 100 ms. The modulation index is 0.95 and the resistance of the RLC circuit is 300 mΩ. The phase difference in the x-axis is the phase difference of the switching frequency component.

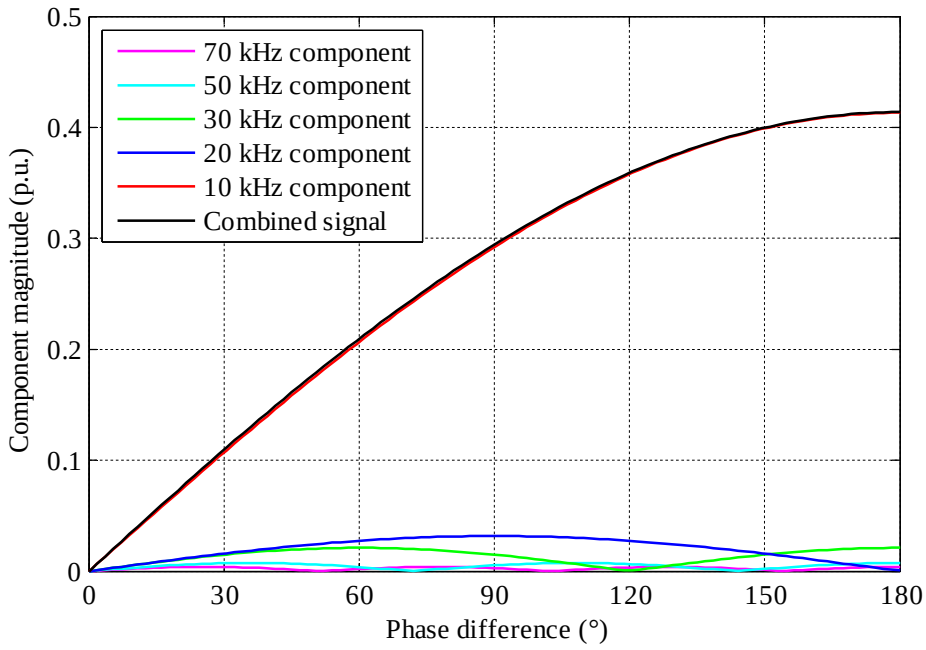


Fig. 2.28. Setup 2 with 5 kW inverters in wet conditions. Five main frequency components and the combined signal of the circulating current between two inverters with distinct phase differences, identical switching patterns, and DC link voltages of 1.0 p.u. The RMS currents of individual phase difference points are calculated over 100 ms. The modulation index is 0.95 and the resistance of the RLC circuit is 300 mΩ. The phase difference in the x-axis is the phase difference of the switching frequency component.

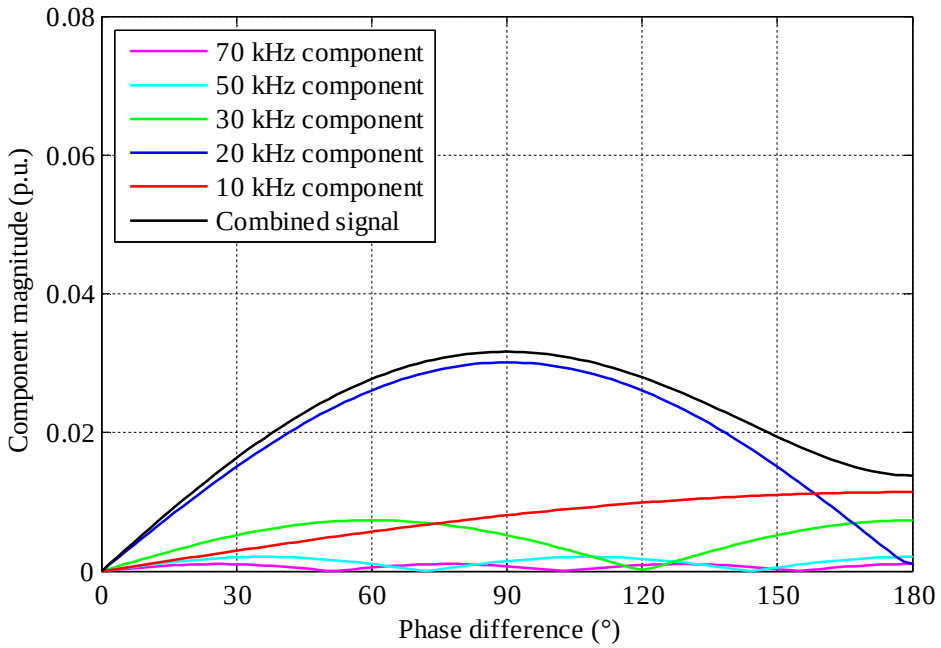


Fig. 2.29. Setup 3 with 500 kW inverters in dry conditions. Five main frequency components and the combined signal of the circulating current between two inverters with distinct phase differences, identical switching patterns, and DC link voltages of 1.0 p.u. The RMS currents of individual phase difference points are calculated over 100 ms. The modulation index is 0.95 and the resistance of the RLC circuit is 300 mΩ. The phase difference in the x-axis is the phase difference of the switching frequency component.

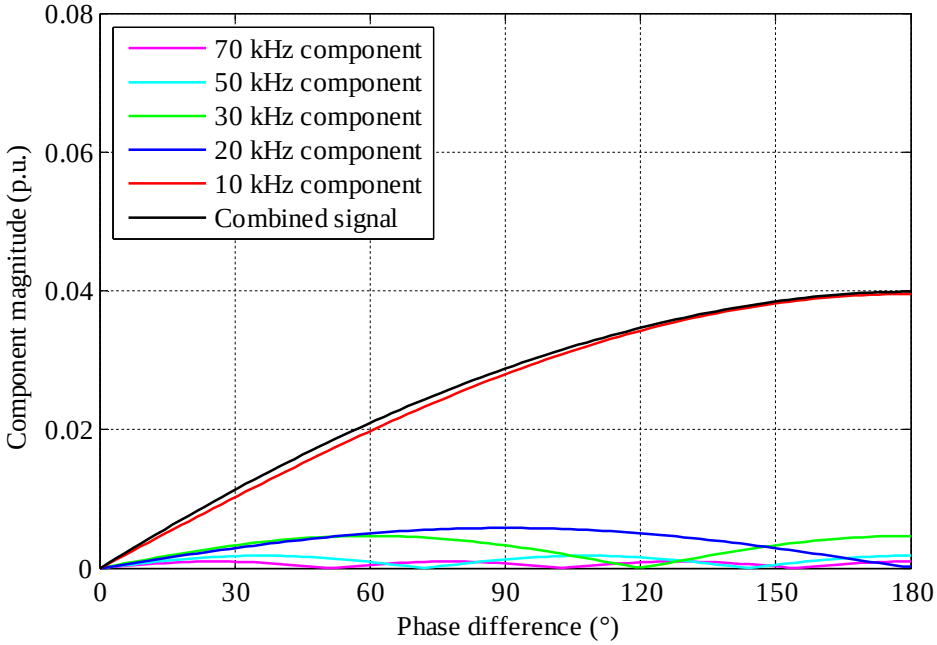


Fig. 2.30. Setup 4 with 500 kW inverters in wet conditions. Five main frequency components and the combined signal of the circulating current between two inverters with distinct phase differences, identical switching patterns, and DC link voltages of 1.0 p.u. The RMS currents of individual phase difference points are calculated over 100 ms. The modulation index is 0.95 and the resistance of the RLC circuit is 300 mΩ. The phase difference in the x-axis is the phase difference of the switching frequency component.

As can be seen in Fig. 2.27–Fig. 2.30, the RLC circuit changes the frequency spectrum of the common-mode voltage by reducing certain harmonics more than others. The resonance frequency of the RLC circuit determines which component is the largest in the circulating current. When one of the odd harmonic components of the switching frequency is the dominant one in the circulating current, the maximum circulating current value is observed when the inverters are in the opposite phases. When even harmonics are the dominant ones, such as in Fig. 2.29, the maximum circulating current may be observed at other phase differences. However, the global minimum is always during synchronized operation.

# Chapter 3

# Circulating current minimizing control

*This chapter introduces a synchronization method to minimize the circulating current of parallel-connected inverters. Two different measurement methods are analyzed; a circulating current measurement and a common-mode voltage measurement.*

## 3.1 Measuring the synchronization

The synchronization can be measured either as a circulating current of the inverter or as a common-mode voltage on the DC side of the inverter or on the AC side of the inverter and the grid filter as stated in the previous chapter.

The minimum control period to control the synchronization is half of a switching period. Instantaneous measurements cannot be used in controlling the synchronization since the instantaneous switching states may be different even with synchronized modulators. As indicated in Section 2.2.3, the common-mode voltage generated by an inverter has a switching frequency component and its multiple components along with the 150 Hz component generated by the SVPWM. In order to deal with multiple different frequency components, the root mean square (RMS) value of the measured signal has to be calculated. The RMS calculation cycle should be a multiple of 6.67 ms to operate without the disturbance of the harmonic components produced by the inverter.

### 3.1.1 Circulating current measurements

The circulating current can be measured from three different locations, from the AC side of the inverter, from the DC side of the inverter, or from the ground cable at the solar panels of the inverter in question as indicated in Fig. 3.1. The first two measurement locations are closer to the PV inverter and thus preferred. From the AC side of the inverter, the circulating current has to be measured as a sum current of the three phase currents. This can be achieved by measuring the three individual phase currents simultaneously and summing the currents together, or by measuring the sum current with a separate sum current measuring device. In an inverter where the phase current measurement uses only a

single sampling capacitor, the circulating current cannot be measured by summing the phase currents together since the three phase currents are taken at different times. Thus, the sum of the currents would not represent the circulating current. Standard inverters may have two or three phase current measurements. Inverters with two phase current measurements and inverters with measuring devices incapable of simultaneous current sampling require extra measuring devices to be added to measure the circulating current.

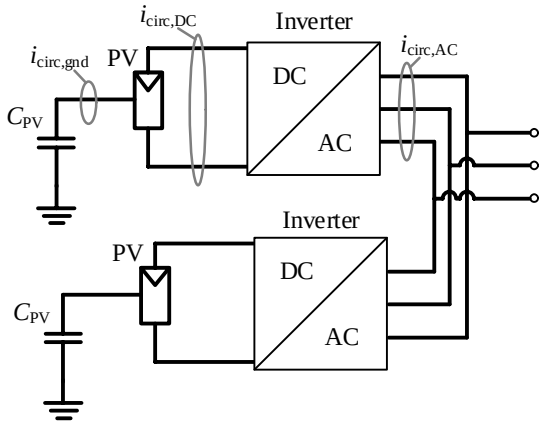


Fig. 3.1. Setup of two parallel PV inverters and three different circulating current measurement points.

The circulating current measurement from the DC side is similar to the AC side measurement. The difference is that the DC side has only two conductors for the current measurement; the negative DC bus and the positive DC bus. The sum of the currents in these conductors is the circulating current. Standard inverters may not have any current measurement on the DC side or one current measurement at most. Extra measuring devices are required for circulating current measurement from the DC side.

As explained in Section 2.3.1, the main frequency components that appear in the common-mode voltage of the parallel-connected inverters are the switching frequency component and the harmonics of the switching frequency component. To detect the circulating current correctly, the sampling frequency of the current measurement has to meet the Nyquist criterion, and be at least twice as large as the frequency of the measured components (Nyquist, 1928). The sampling frequency of the circulating current measurement should be larger than two times the largest desired harmonic component of the switching frequency to measure the current without aliasing.

The largest influential harmonic component of the circulating current is defined by the harmonic components of the common-mode voltage difference and the frequency response of the passive components in the setup.

### 3.1.2 Common-mode voltage measurements

The common-mode voltage of the inverter in question can be measured from the AC side of the switching devices, between the inverter unit and the grid filter. However, this common-mode voltage can also be calculated from the DC link voltage and the switching commands of the inverter, and it gives no information about the circulating current. The combined common-mode voltages of the parallel inverters that can be used as indicators of the circulating current can be measured in two different locations illustrated in Fig. 3.2. As shown in Eq. (2.29), the common-mode voltage on the grid side of the grid filter is determined by the generated common-mode voltage of the inverter in question and the voltage over the passive components of the inverter that is generated by the circulating current. The sign of the circulating current in Eq. (2.29) is negative. The negative sign indicates that the smaller the circulating current is, the larger the AC common-mode voltage is. To minimize the circulating current, the AC common-mode voltage has to be maximized.

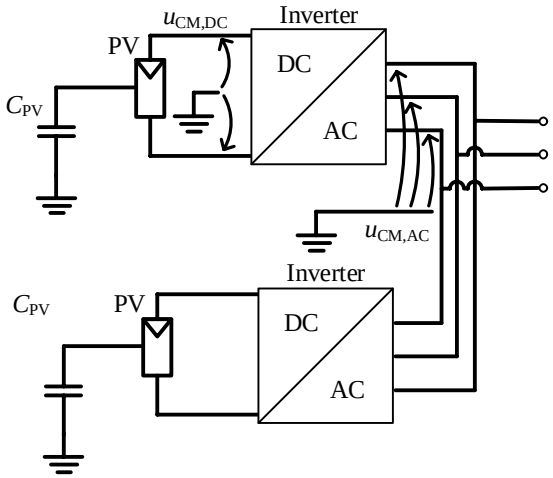


Fig. 3.2. Setup of two parallel PV inverters and two different common-mode voltage measurement points.

The common-mode voltage on the AC side has to be measured as three individual phase-to-ground voltage measurements and by calculating the mean of the three measurements. The standard control of the inverter may require the voltage measurements for grid disturbance monitoring and for a phase-locked loop (PLL) operation. However, if the inverter does not feature the three voltage measurements that can sample simultaneously, they need to be implemented to the system.

The DC side common-mode voltage is determined directly by the integral of the circulating current and the PV array capacitance as indicated in Eq. (2.22). Thus, the DC side common-mode voltage can be used as a direct indicator of the circulating current amplitude. The

larger the circulating current, the larger the DC common-mode voltage. The DC common-mode voltage can be obtained by measuring the voltage from the positive and negative DC buses against the ground and calculating the mean of the two measurements.

Similar measurement bandwidth issues are present with common-mode voltage measurements as with the circulating current measurements.

## 3.2 Modifying the synchronization

The phase shift between parallel inverters drifts slowly when the inverters are not communicating. This drifting is a result of control board clock frequency tolerances. Divergent clock frequencies implement a constant sweep to the modulators of the parallel inverters. This sweep needs to be controlled.

One method of controlling the synchronization is to insert a delay into the controlled inverter. Since the modulators have a constant sweep of the synchronization, a delay has to be increased all the time in the controlling inverter. A simple delay in the modulator causes a reduced phase margin of the controller of the inverter. A simple delay in the whole inverter operation leads to undesired switching states during transitions. In order to implement the delay into the modulator without undesired consequences, the voltage vectors have to be calculated with the combined length of the switching period and the delay. A longer/shorter switching period than normal equals the scenario of a modified switching frequency for a duration of a single switching period.

A benefit of the modified switching frequency is that the correct lengths for the switching vectors can be calculated. Hence, no extra switchings occur and the normal current control of the inverter is not affected. Implementing a simple delay to the end of the switching period modifies the calculated switching states and produces undesired current at the grid filter.

An illustration is given in Fig. 3.3 to describe the switching frequency transition. The two modulators are at a 90° phase shift at the beginning. At $t_1$, the lower inverter changes its switching period length to half of the nominal switching period length for a duration of half the new switching period length. At $t_2$, the inverters are synchronized and the inverter changes its switching period length back to nominal. A new switching period starts at $t_3$, when the modulators are perfectly synchronized.

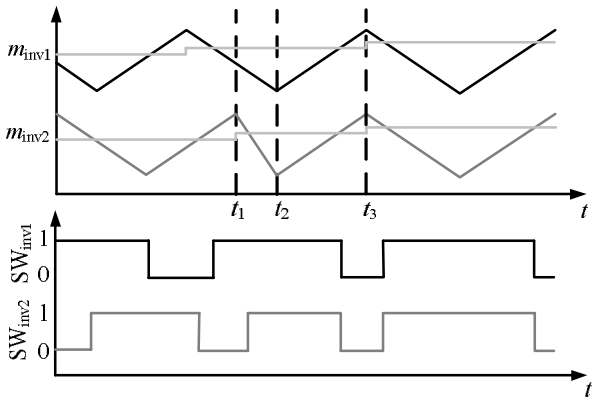


Fig. 3.3. Switching frequency transition at inverter 2 starts at $t_1$, when the switching frequency is doubled for a duration of half of the new switching period. At $t_2$, the inverters are synchronized and the inverter changes its switching frequency back to nominal. At $t_3$, both of the inverters start a new switching period in a perfect synchronization.

The switching frequency transition can be as short as half of the new switching period, or as long as desired. By modifying the switching frequency by only a small deviation, the frequency components of the system can be kept close to the nominal switching frequency.

## 3.3 Controlling the synchronization

The previous sections have demonstrated how to measure and modify the synchronization. In order to operate the parallel inverters synchronously, the synchronization have to be controlled.

As can be seen in Fig. 2.27 and Fig. 2.29, the circulating current may not always behave linearly since the harmonic components of the switching frequency may be the dominant components of the circulating current. Thus, it is suggested to use only the switching frequency component in the control. The switching frequency component behaves linearly with every phase difference. The switching frequency component is largest when the modulators are in an opposite phase and smallest when the modulators are synchronized, regardless of other parameters.

### 3.3.1 Circulating current control

The circulating current has its global minimum when the parallel-connected inverters are synchronized. A calculation of the frequency components of the circulating current with phase differences from 0° to 180° is made with the setup 1 illustrated in Table 2.4 and

unequal DC link voltages of 1.0 p.u and 1.1 p.u. The corresponding modulation indices are 0.9 and 0.818. The circulating current can be seen in Fig. 3.4.

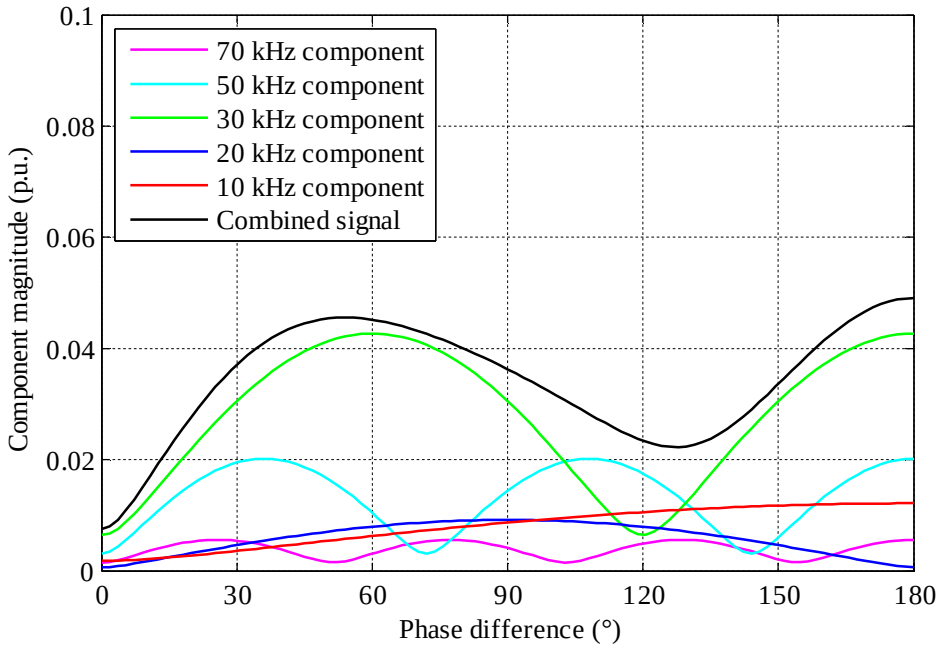


Fig. 3.4. Five main frequency components and the combined signal of the circulating current between two 5 kW inverters with distinct phase differences, the DC link voltages of 1.0 p.u. and 1.1 p.u., and the corresponding modulation indices of 0.90 and 0.818. The RMS currents of individual phase difference points are calculated over 100 ms. The inverters are in dry condition, setup 1 parameters are used. The phase difference in the x-axis is the phase difference of the switching frequency component.

The 150 Hz component is constant with every phase difference since it is synchronized to the grid frequency and not to the modulator frequency. The 150 Hz component is so small that it is neglected from Fig. 3.4. To minimize the circulating current, the instantaneous current cannot be controlled. A long enough RMS component has to be calculated to remove the variation produced by the 150 Hz component. Using RMS calculation that is not a multiple of 6.67 ms will result in aliasing of the 150 Hz component.

Controlling the circulating current from the calculated RMS current value (Fig. 3.4) is a challenging task. It has several similarities with the MPPT control task, which are:

- The phenomena of maximum power point tracking are slow compared with the basic controls of the inverter, similarly as in the RMS circulating current control.

- The controlled signals (power and circulating current) can have nonlinear behavior and multiple maxima and minima.
- The controls work indirectly. The power is controlled by changing the voltage or current of the system, and the circulating current is controlled by changing the phase difference between the modulators of the parallel inverters.
- Finally, the absolute value of the controlled signal is not of interest. The signal is desired to be controlled either to the maximum or minimum value.

Thus, it is recommended to use a control algorithm from the MPPT applications. The control task is not optimal for a regular PI controller because the circulating current reference is unknown and varying. A reference of zero circulating current is unreachable in real applications, and the error between the minimum circulating current and zero will accumulate in the integrator part of the controller.

Valid MPPT algorithms are, for example, hill-climbing algorithms such as P&O and IC (de Brito et al., 2013), fuzzy logic control and neural networks, or the sweep method (Esram and Chapman, 2007). The sweep method is the only method of finding the global maximum power point. All other algorithms detect the closest maximum power point of the initial operating point. The ability to find the global maximum power point is considerable in shaded conditions when multiple maximum power points may be present. The same holds for the circulating current control, when there are multiple circulating current minima present in the setup as in the total circulating current in Fig. 3.4.

By using the full frequency spectrum of the circulating current as a controlled variable, the sweep control method is the only possible algorithm to find the synchronization. All other control methods will find the local minimum around the 120° phase difference illustrated in Fig. 3.4. The sweep method in the circulating current control generates a sweep over the whole phase difference range and stores the minimum circulating current value. After the initial sweep, the method finds the minimum circulating current value again and stops there. A drawbacks of this method is that also the maximum circulating current is briefly obtained. In MPPT applications the brief minimum energy output from the solar panels is not significant by any means, and thus, the sweep method is a valid control method in MPPT applications.

When the switching frequency component of the circulating current can be filtered and isolated from the higher-frequency components, the rest of the MPPT algorithms are also valid control methods. The linear behavior of the switching frequency component makes it possible to place the initial operating point anywhere on the phase difference scale, and a correcting circulating current minimizing control step can be made from the second control step onwards. The first control step of a hill-climbing control algorithm may be in the wrong direction, because a perturbation step towards a random direction has to be done. A flow chart of a P&O control algorithm for the circulating current controller is given in Fig. 3.5.

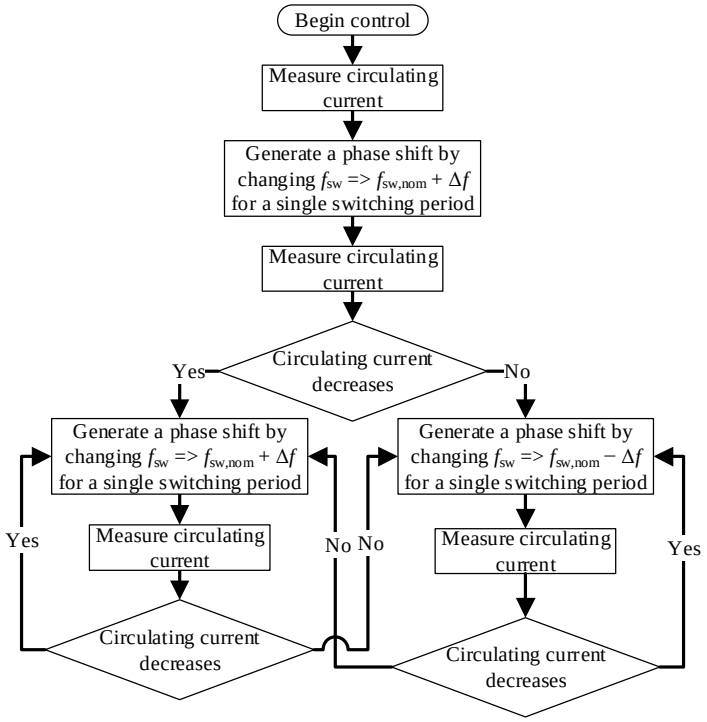


Fig. 3.5. Flow chart of the P&O control algorithm for the circulating current control.

A hybrid controller including an initial sweep method and further, a hill-climbing algorithm is also a possible solution if the full frequency domain of the circulating current has to be used. In that case, the maximum circulating current is achieved only once per operation, and only small perturbations are required in the later operation.

The three introduced circulating current control methods based on circulating current measurements are given in a state flow chart form in Fig. 3.6, Fig. 3.7, and Fig. 3.8. The first one is the simple sweep control method, based on the full frequency domain of the circulating current. The second is the hill-climbing P&O control method, based on filtered circulating current measurement. Finally, the third one is the hybrid control based on the full frequency domain of the circulating current.

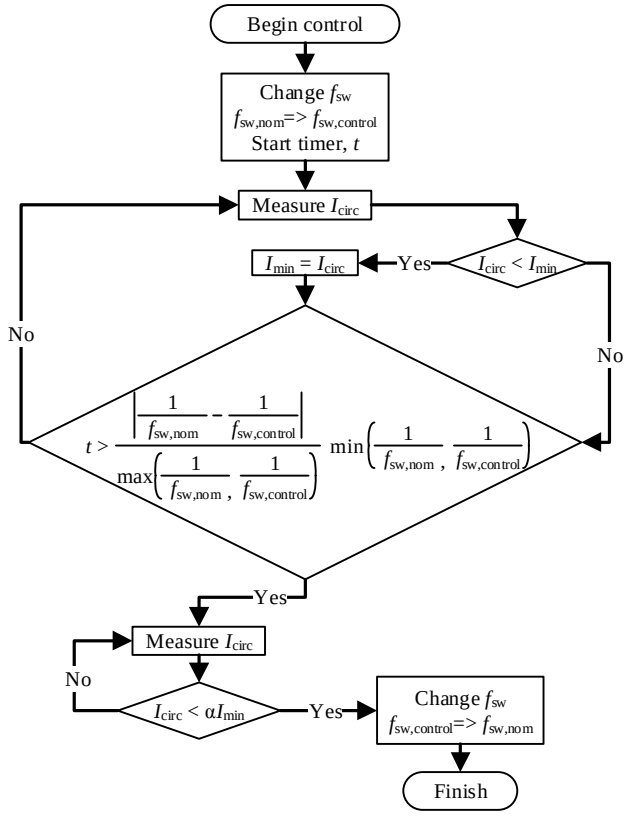


Fig. 3.6. Flow chart of the sweep control algorithm, which is based on the full frequency domain of the circulating current measurement.

The time comparison in the middle of Fig. 3.6 calculates the time required for the sweep to run through all the possible phase differences. The modified switching frequency should be as close to the original switching frequency as possible to achieve a better resolution for the control.

The α-factor in the bottom of the figure is an uncertainty factor. The conditions are changing and the minimum circulating current may not be exactly the same at the next sweep, thus an uncertainty factor is multiplied with the minimum circulating current value.

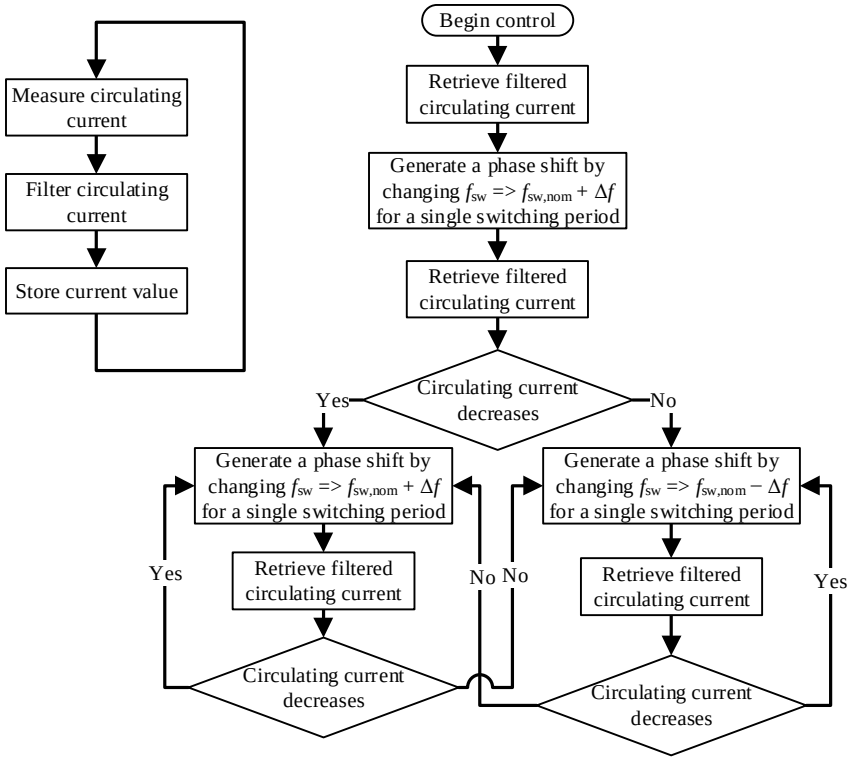


Fig. 3.7. Flow chart of the P&O control algorithm, which is based on the filtered circulating current measurement.

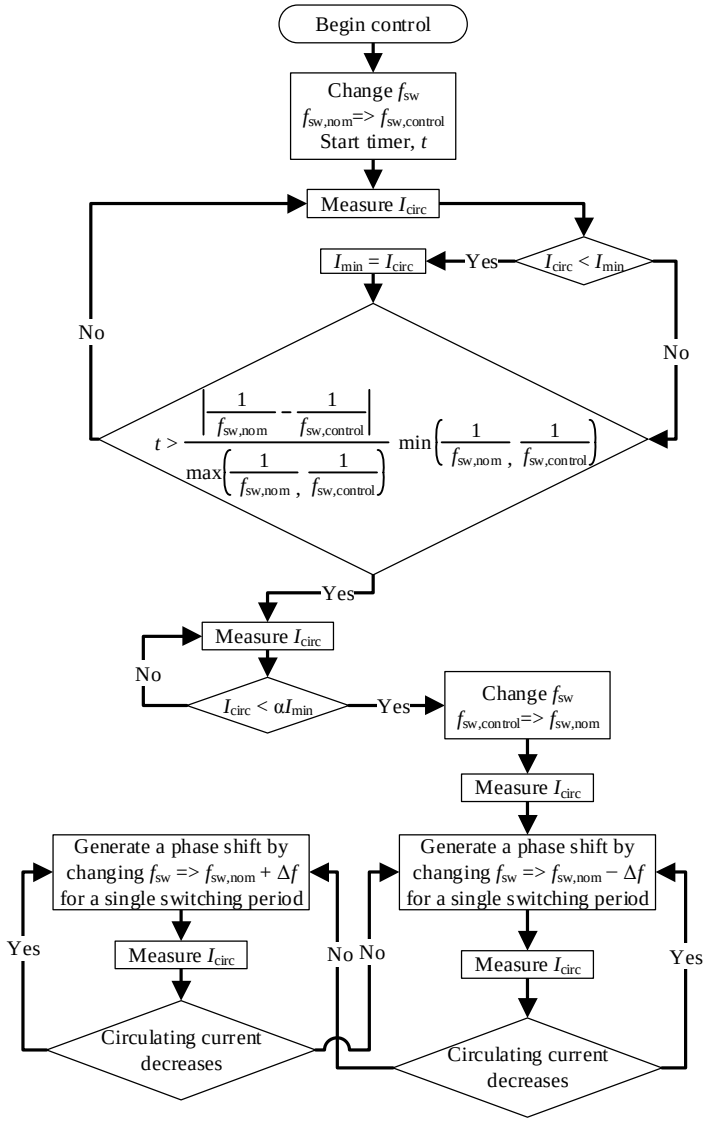


Fig. 3.8. Flow chart of the hybrid control algorithm, which is based on the full frequency domain of the circulating current measurement.

### 3.3.2 Common-mode voltage control

As mentioned above, the common-mode voltages on the DC side of the inverter and on the AC side of the grid filter are dependent on the circulating current. Thus, the behavior of the common-mode voltages is similar to the circulating current, and the same control methods are desired.

The same control methods shown in Fig. 3.6, Fig. 3.7, and Fig. 3.8 are feasible for the control based on common-mode voltage measurement. Two flow charts for the common-mode voltage measurements are given in Fig. 3.9 and Fig. 3.10. The P&O control method in Fig. 3.7 is used with the DC common-mode voltage measurement in Fig. 3.9 and with the AC common-mode voltage measurement in Fig. 3.10.

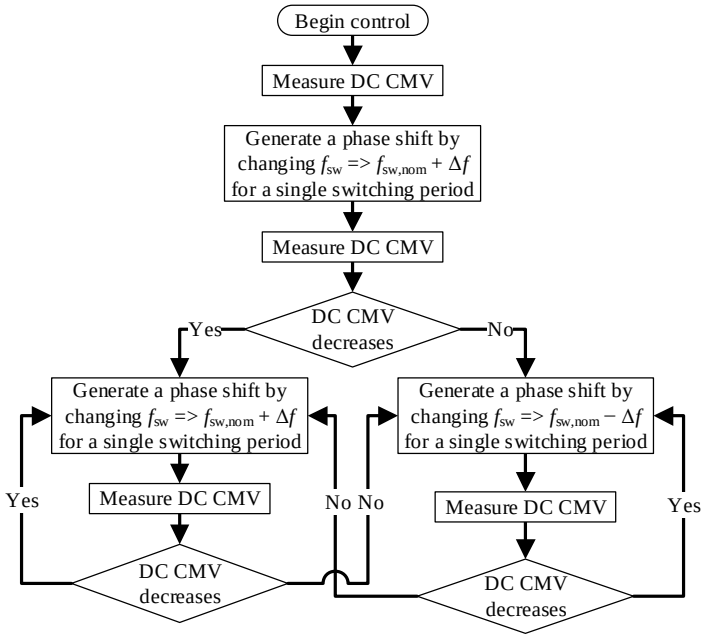


Fig. 3.9. Flow chart of the P&O control algorithm, which is based on the full frequency domain of the DC common-mode voltage measurement.

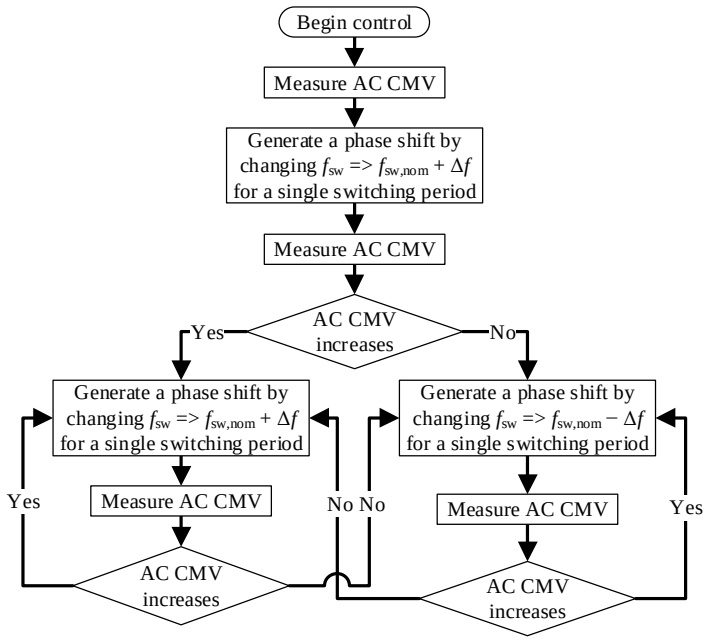


Fig. 3.10. Flow chart of the P&O control algorithm, which is based on the full frequency domain of the AC common-mode voltage measurement.

## 3.4 Control of *n* parallel-connected inverters

The theory presented in Chapter 2 is valid for *n* parallel-connected inverters. The controllers of the inverters are independent units that do not require communication. However, a problem may arise if the control operations of the inverters occur at the same time. Problems with the different control methods and solutions to the problems are presented next.

### 3.4.1 Problems with the sweep-based control

If a sweep control is initialized when a sweep control is active in another inverter, the sweeping inverters have a constant phase difference. However, when other inverters are present in the system, a minimum value is visible in the measurements. The result of the simultaneous sweeps is an unpredictable phase difference between the inverters. This is an unwanted situation, and thus, the sweep control method is unreliable in a setup of more than two inverters.

### 3.4.2 Problems with the P&O-based controls

The P&O-based controls operate as desired, regardless of the number of parallel-connected inverters, when the perturbations are not simultaneous in the inverters. Even if a single control period did occur simultaneously in the parallel inverters and the steps were in the wrong direction, the error could be corrected in the next step.

The time between the measurements of the P&O sequence can be randomized to get the controls of the parallel inverters working at separate times. The time demand for the P&O controller is derived from the clock frequency tolerances of the control boards. An example of the P&O control randomization is as follows: the P&O sequence is started once in every 0.5 s and the RMS measurements are calculated over 20 ms. By randomizing the P&O control period start between 0.35 s and 0.65 s, the control periods of two independent inverters are totally separate for 93% of the time. At least some part of the control periods are overlapping rest of the time. However, this may not even result in a misdirected perturbation.

# Chapter 4

# Experimental results

*In this chapter, the previously specified measurement and control methods to minimize the circulating current are tested in an experimental setup. First, the experimental setup is defined in detail, and the circulating current minimizing control based on the current measurements is described before the control based on the voltage measurements.*

## 4.1 Experimental setup

The experimental setup is constructed to be as similar to a large-scale setup as possible. However, the power of the setup has to be small enough so that the circulating currents do not generate a hazardous environment when the individual isolating transformers are absent. Two parallel inverters are chosen for the simplicity of the system and the control task. The solar panels used in the setup are Tianwei TW230P60-FA2 type solar panels. The setup consists of 22 solar panels connected in series per single inverter. Thus, the rated DC peak power of a single inverter is 5.06 kWp. The inverter hardware is ABB ACSM1-204AR-016A-4 back-to-back converters. The hardware is modified so that the inverter modules and the DC link capacitors of the main circuit are used. The diode rectifiers are bypassed and the solar panels are connected directly to the DC link. The AC sides of the inverters are connected to ABB WFU-02 LCL filters, which are connected to a 10 kVA Δ-Y transformer. The system is shown in Fig. 4.1.

The control of the inverters is completely modified. An SVPWM is used along with the PI-controlled DC voltage and PI-controlled currents. The reference value for the DC link voltage controller is 650 V.

### 4.1.1 Measurements and control

The measurements needed for the basic control of the inverter are:

- Output current measurements,
- DC link voltage measurements, and

- Grid synchronization measurements (e.g. grid voltages).

The output currents and the DC link voltage are measured with the measuring sensors of the inverters and analog-to-digital converters (ADCs). The measuring circuit has only a single sampling capacitor. Thus, the three-phase currents cannot be measured simultaneously, and the circulating current cannot be calculated from the phase current measurements.

Grid voltages are measured to synchronize the inverter to the grid voltage. In a symmetric three-phase system, without a neutral potential, two voltage measurements are required to synchronize the inverter to the grid. However, three voltage measurements are used in this experimental setup, since the same measurements can be used in the AC common-mode measurement.

The measurements needed by the different circulating current minimizing controls are:

- Three-phase AC voltage measurements,
- The DC link positive towards the ground potential and the DC link negative, towards the ground potential voltage measurements, and
- Circulating current measurement.

The first measurement is accomplished with the requirements by the basic inverter operation. The DC side voltage measurement of the inverter is only from the positive DC bus towards the negative DC bus. Thus, new voltage measurements from the positive DC bus to the ground potential and from the negative DC bus to the ground potential are needed to test the circulating current minimizing control. Since the current measurements of the inverter cannot be used in the circulating current measurement, an extra current measurement can be inserted either into the DC side of the inverter or into the AC side of the inverter. The current measurement is inserted into the AC side of the grid filter. The circulating current measurement probe is a LEM LA-125-P, and the extra voltage measurement probes are LEM DVL-1000.

The measured analog signals are fed to a Texas Instrument ADS8556 analog-to-digital converter. The digital measurement signals are then fed into a Xilinx Kintex-7 field-programmable gate array (FPGA) KC705 board, where the control of both inverters is executed. A single control board is chosen as the phase difference of the inverters can be precisely determined when the inverters have a common clock signal. The measurements and the control boards are illustrated in Fig. 4.1.

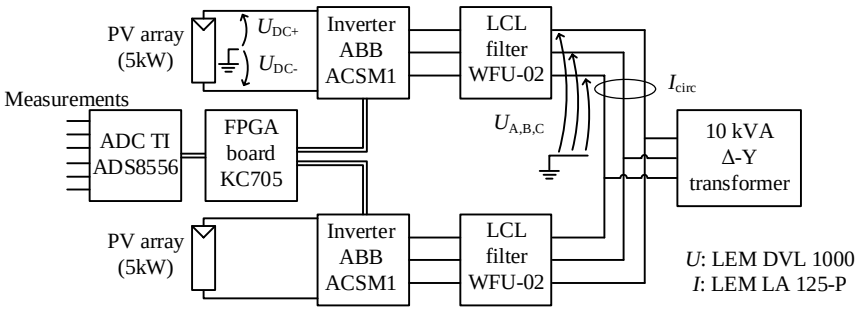


Fig. 4.1. Experimental setup with all the main circuit components and the measurement locations.

The ADC is sampled as often as possible. The hardware-defined maximum sample time for the conversion is 2 µs. This sample time enables measurement of frequency components smaller than 250 kHz. The response time of the current measurement probe is less than 1 µs. However, the frequency components between 250 kHz and 1 MHz are filtered in the measurement board. Thus, the digital circulating current measurement in the FPGA board has a sample time of 2 µs and all the frequency components under 250 kHz.

The frequency bandwidth of the voltage measurement probes has a -3 dB limit at 14 kHz. Thus, the voltage measurements are not feasible for measuring the higher-frequency components. The higher-frequency components cause problems for the control algorithms, and thus, the inherent filtering in the voltage measurements is a desired quality. The filtering of the harmonic components of the switching frequency enables the use of the P&O control algorithm.

The two parallel inverters have controls of their own, which run in parallel operation in the FPGA board. The system clock of the FPGA board is the only common factor between the inverters. The measurements required for the basic operation of the inverters are sampled at the mid-point of the switching period. These include the phase currents and the phase voltages towards the ground. The control sequence is then applied and the relative voltage vector lengths are calculated for the next switching period. The switching period length for the next switching period is obtained from the circulating current minimizing control block.

The effect of the modified switching frequency is first tested by driving the two inverters with slightly different switching frequencies. The nominal switching period is 100 µs and the modified period is 99.98 µs. The difference in the switching period length is the smallest possible difference defined by the modulator resolution. The RMS circulating current, the DC and the AC RMS common-mode voltages, and the phase difference between the modulators are illustrated in Fig. 4.2.

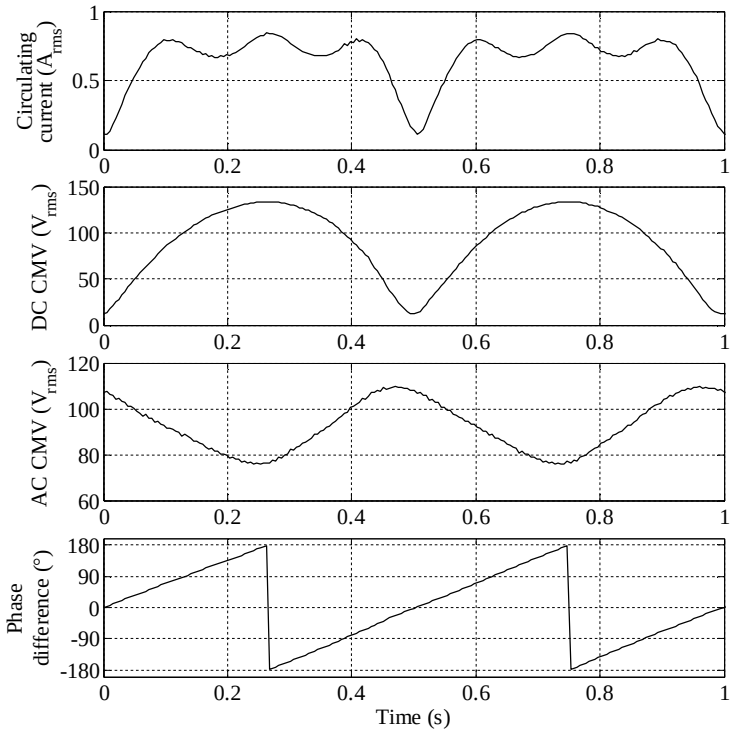


Fig. 4.2. RMS circulating current, the DC and the AC RMS common-mode voltages, and the phase difference between the modulators when the two inverters have different switching periods. $T_{sw,inv1}$ = 100 $\mu s$, $T_{sw,inv2}$ = 99.98 $\mu s$.

Fig. 4.2 shows that the circulating current measurement has the harmonic components of the switching frequency; especially, the third harmonic, which can be seen as the local maximum value around the 60° phase difference. However, the measurement probes of the voltages filter the harmonic components, and the pure switching frequency component is depicted in the figure.

## 4.2 Circulating current minimizing control with the current measurements

The circulating current minimizing control with the current measurements uses the 500 kHz sampled circulating current measurement. The measurement can be directly applied to the sweep control method and the hybrid control method. The 150 Hz component has to be neglected from the control in order not to track the 150 Hz component. Thus, an RMS value has to be calculated from the circulating current measurements. A 20 ms RMS

calculation is used because 20 ms is a multiple of both the 150 Hz component and the 10 kHz nominal switching frequency.

### 4.2.1 Sweep control method

The first tested control is made with the nonfiltered circulating current measurements and the sweep method. The control is activated at $t = 0$ s when the phase difference is largest. One of the inverters operate at the nominal switching frequency and the other changes its switching period from 100 µs to 99.98 µs and performs the control sequence illustrated as a flow chart in Fig. 3.6. The circulating current value is calculated over the last 20 ms, but updated once in a millisecond. Thus, the minimum RMS circulating current value should be calculated about 10 ms after the actual synchronization. The sweep control method is demonstrated in Fig. 4.3, where the control lasts until 0.5 s and finds the minimum circulating current value at $t = 0.75$ s. When the control stops, the phase difference between the two modulators is 3° and not the 0° of a perfect synchronization.

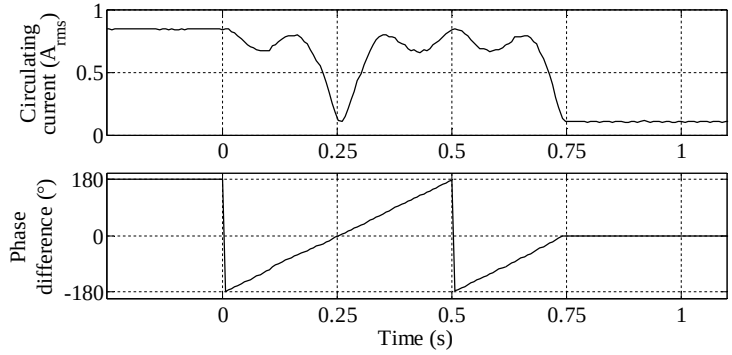


Fig. 4.3. RMS circulating current and the phase difference between the modulators when the sweep control method is activated at $t = 0$ s. The control seeks the minimum circulating current value until a full sweep is made at 0.5 s, and after 0.5 s searches for the stored minimum circulating current value. The minimum value is found again at $t = 0.75$ s.

### 4.2.2 P&O control method

The P&O control method requires the initial filtering for the harmonic components of the switching frequency. Therefore, a low-pass filter is used for the circulating current measurements. The cut-off frequency of the filter is 12 kHz, and the filter is designed using a second-order Type I Chebychev filter, with an allowed pass band ripple of 1 dB. The P&O controller is designed as shown in the flow chart in Fig. 3.7. The perturbation step is a 1.8° phase shift, and the perturbations are done every 0.5 s. The RMS circulating current,

the filtered RMS circulating current, and the phase difference between the modulators during the P&O control case are illustrated in Fig. 4.4.

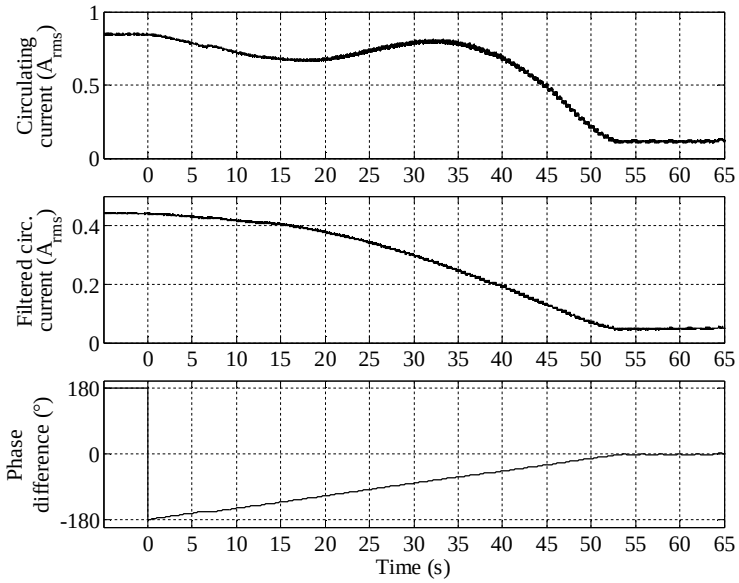


Fig. 4.4. RMS circulating current, the RMS filtered circulating current, and the phase difference between the modulators when the P&O control method based on the filtered current is activated at $t = 0$ s. The perturbations are 1.8° and made every 0.5 s.

As can be seen in Fig. 4.4, the filtered circulating current can be controlled with a P&O controller. The RMS value of the circulating current is cut down to half during the start of the control sequence, and the behavior compared with the phase difference becomes linear. The third harmonic of the switching frequency generated a major problem for the control; by filtering the third harmonic, the control can be simplified. The operation of the P&O control during the final oscillation is illustrated in Fig. 4.5.

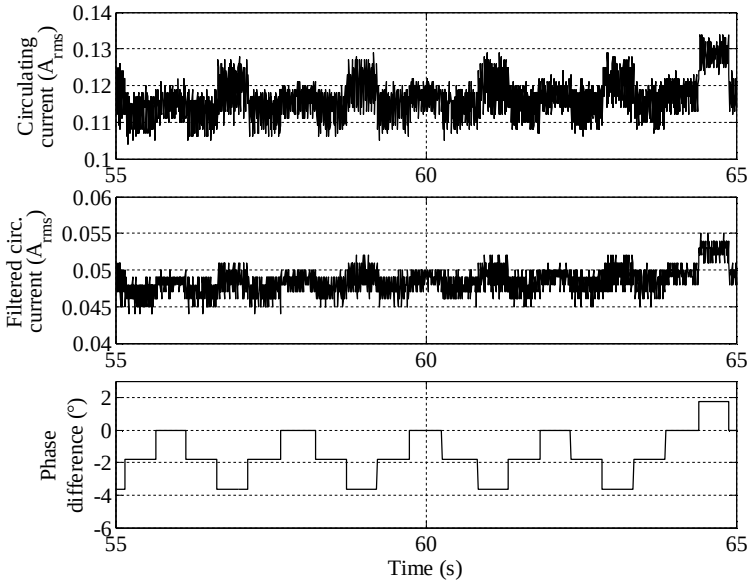


Fig. 4.5. RMS circulating current, the RMS filtered circulating current, and the phase difference between the modulators when the P&O control method based on the filtered current has reached the final oscillating state. The perturbations are 1.8° and made every 0.5 s.

### 4.2.3 Hybrid control method

The hybrid control method may be applied with the nonfiltered circulating current measurement. The initial sweep indicates the universal minimum circulating current value, and the behavior of the circulating current is linear around ± 40° phase difference as illustrated in Fig. 4.3. Thus, the P&O control method can find the actual minimum value, and no further sweeps are required. The same P&O control algorithm and sweep algorithm are used as in the two previous control methods. The flow chart of the hybrid control method is presented in Fig. 3.8. The circulating current and the phase difference between the inverters in the hybrid control case are illustrated in Fig. 4.6.

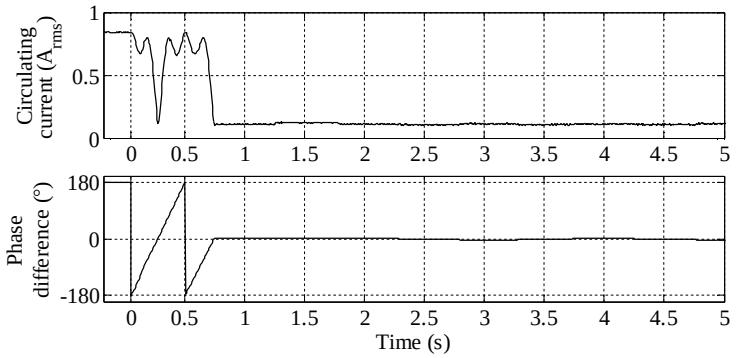


Fig. 4.6. RMS circulating current and the phase difference between the modulators when the hybrid control method is activated at $t = 0$ s. The initial sweep lasts 0.5 s and the control tracks the minimum value at 0.75 s. After the sweep, the perturbation steps are 1.8° and made every 0.5 s.

The P&O operation is not clearly visible in Fig. 4.6, and thus, an enlarged figure is provided to better illustrate the operation after the initial sweep. The P&O operation is illustrated 1 second after the initial sweep begins.

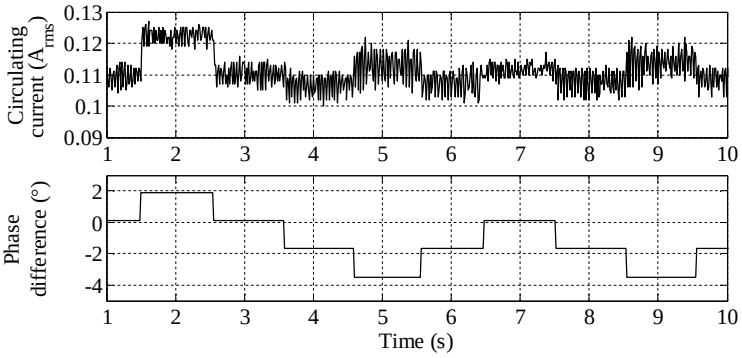


Fig. 4.7. RMS circulating current and the phase difference between the modulators during the P&O operation of the hybrid control method. The perturbation steps are 1.8° and made every 0.5 s.

Fig. 4.7 illustrates the operation of the P&O controller in the hybrid control mode. It can be seen that the minimum RMS circulating current value is achieved around the 0° and –2° phase differences. The circulating current is clearly higher with a phase difference of 2° and with a phase difference of –4°.

## 4.3 Circulating current minimizing control with the voltage measurements

As mentioned above, the common-mode voltage measurements include filtering of the harmonic components of the switching frequency. Thus, the only recommendable control method out of the three mentioned above is the P&O control method. The same 20 ms RMS value is calculated of the common-mode voltage measurements as is calculated of the circulating current.

### 4.3.1 P&O control method of the DC common-mode voltage

The P&O algorithm design for the control based on the DC common-mode voltage measurement is shown as a flow chart in Fig. 3.9. The P&O controller is chosen to be similar to the P&O controller used with the control based on the circulating current measurement. The perturbation step is 1.8° and the control sample time is 0.5 s. The measured circulating current and the DC common-mode voltage are presented with the phase difference in Fig. 4.8.

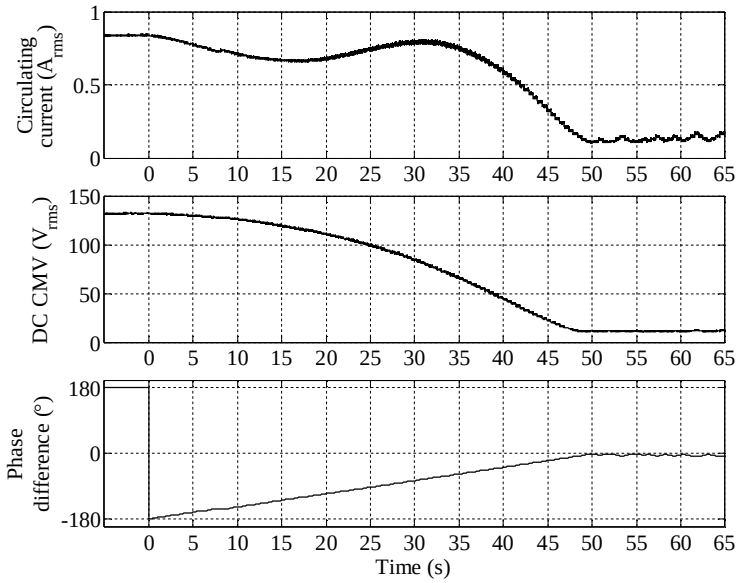


Fig. 4.8. RMS circulating current, the DC RMS common-mode voltage, and the phase difference between the modulators when the P&O control method based on the DC common-mode voltage measurement is activated at $t = 0$ s. The perturbations are 1.8° and made every 0.5 s.

The initial sweep from the opposite phases to the synchronization is achieved with only a few steps in the wrong direction. The incorrect steps are produced near the 180° phase difference, when the perturbation step does not produce a significant change in the DC RMS common-mode voltage. The final operation of the P&O controller near the synchronization is not clearly visible in Fig. 4.8, and thus, an enlarged illustration is provided from $t = 50$ s onwards in Fig. 4.9.

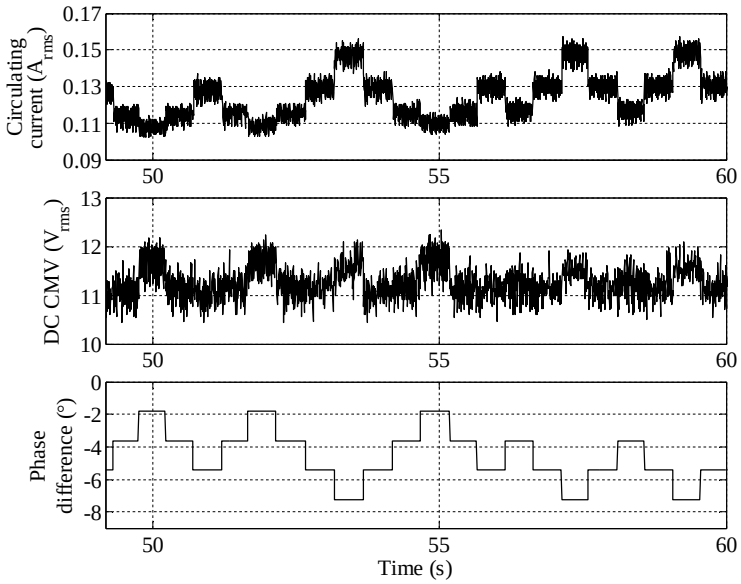


Fig. 4.9. RMS circulating current, the DC RMS common-mode voltage, and the phase difference between the modulators during the final state of the P&O control method based on the DC common-mode voltage measurement.

As can be seen in Fig. 4.9, the actual synchronization is not achieved with the DC common-mode voltage-based control. The minimum DC RMS common-mode voltage is found close to a 5° phase difference. However, the RMS circulating current value is reduced significantly.

### 4.3.2 P&O control method of the AC common-mode voltage

The P&O control is also tested with the AC RMS common-mode voltage. The flow chart of the control is illustrated in Fig. 3.10. The same control variables are used as with the previous controllers. The RMS circulating current and the AC RMS common-mode voltage are illustrated with the phase difference in Fig. 4.10.

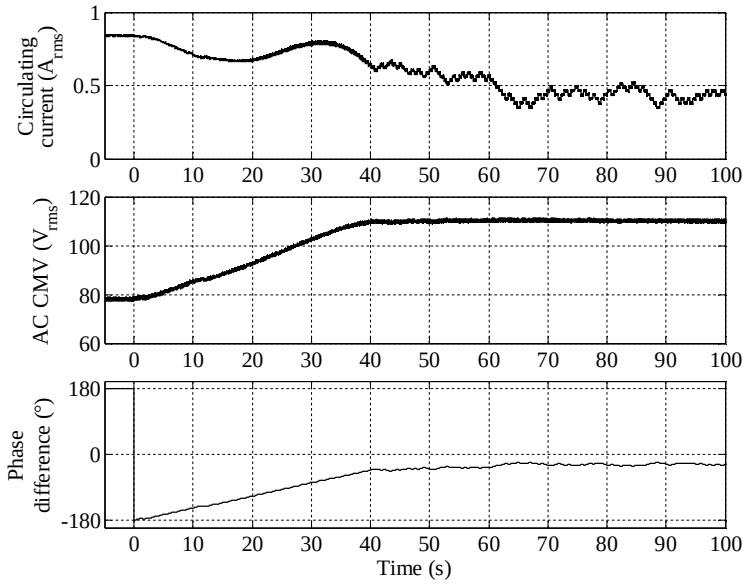


Fig. 4.10. RMS circulating current, the AC RMS common-mode voltage, and the phase difference between the modulators when the P&O control method based on the AC common-mode voltage measurement is activated at $t = 0$ s. The perturbations are 1.8° and made every 0.5 s.

An enlarged illustration of the control sequence after 50 s is given in Fig. 4.11.

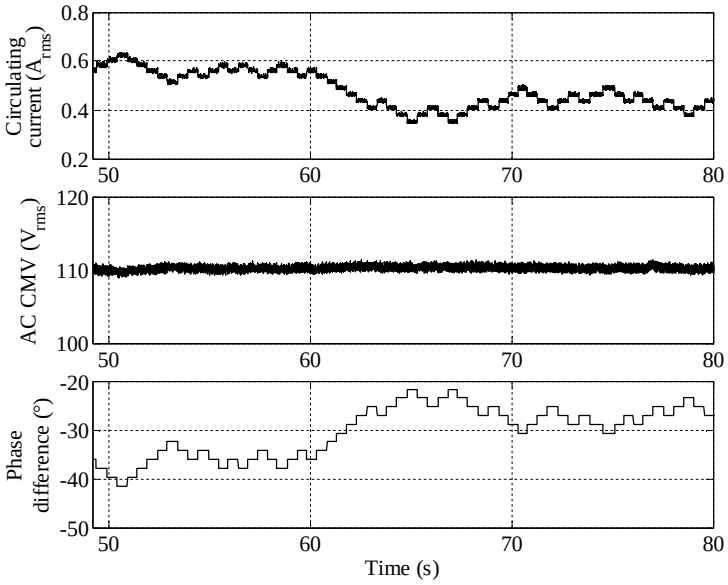


Fig. 4.11. RMS circulating current, the AC RMS common-mode voltage, and the phase difference between the modulators during the final state of the P&O control method based on the AC common-mode voltage measurement.

As can be seen from Fig. 4.10 and Fig. 4.11, the control based on the AC RMS common-mode voltage measurement is the least accurate one. The difference in the CMV is relatively small and the maximum is found around the 30° phase difference. The nonzero phase difference can be explained by the large constant area of the AC CMV. However, this does not fully explain why the maximum value is slightly phase shifted from the perfect synchronization.

## 4.4 Controls with different grounding setups

### 4.4.1 Grounded LCL filters

LCL filters may have grounding capacitors in the star point of the capacitors. This is not common with the PV inverters. Such filters generate an additional path for the circulating current. The simplified common-mode circuit is illustrated in Fig. 4.12.

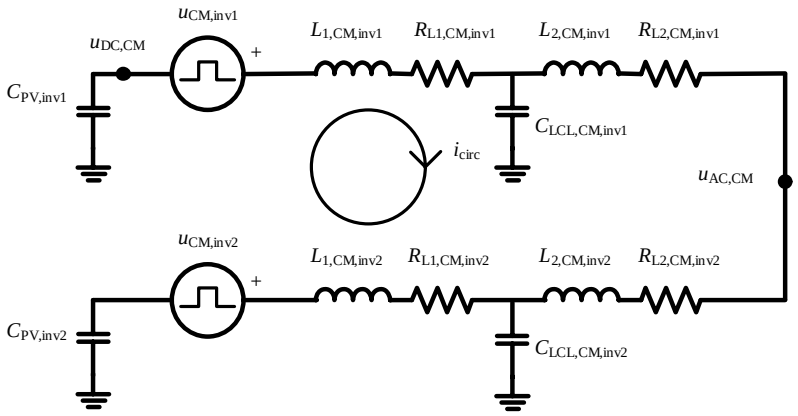


Fig. 4.12. Simplified common-mode circuit when the star point of the LCL filter has a grounding capacitance.

The circulating current is measured from two different locations in this setup. The first is the same location used with the previous setup, which is on the grid side of the LCL filter. In Fig. 4.12, the location is the same as the AC common-mode voltage measurement point. This location is referred to as LCL current measurement location. The other location is between the LCL filter and the inverter. This location is referred to as inverter current. Both of the currents and the RMS common-mode voltages during a sweep in one of the inverters are illustrated in Fig. 4.13.

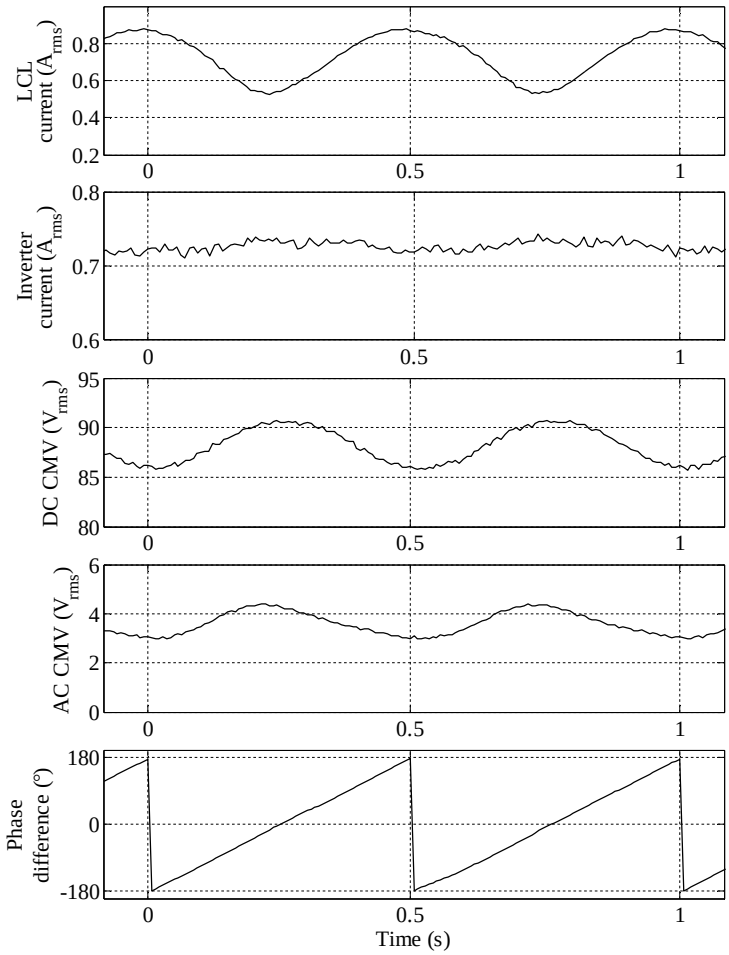


Fig. 4.13. RMS circulating current on the grid side of the LCL filter, the current on the inverter side of the LCL filter, the DC and AC RMS common-mode voltages, and the phase difference between the modulators when the two inverters have different switching periods. $T_{\mathrm{sw,inv1}} = 100\ \mu s$, $T_{\mathrm{sw,inv2}} = 99.98\ \mu s$. The star point of the LCL filter capacitances is connected to the ground with a capacitor.

As can be seen in Fig. 4.13, the RMS circulating current and the common-mode voltages are only slightly affected by the synchronization. The inverter current shown in the second plot and the DC CMV shown in the third plot are measured at the same inverter.

### 4.4.2 Earthing kit

The earthing kit, introduced in Section 2.1.1, is tested with the current setup. A 71 ohm resistance is used between the DC minus bus and the ground potential. The hypothesis about the earthing kit is that the circulating current increases when a fixed grounding is present. The circulating current and the common-mode voltages are illustrated in Fig. 4.14.

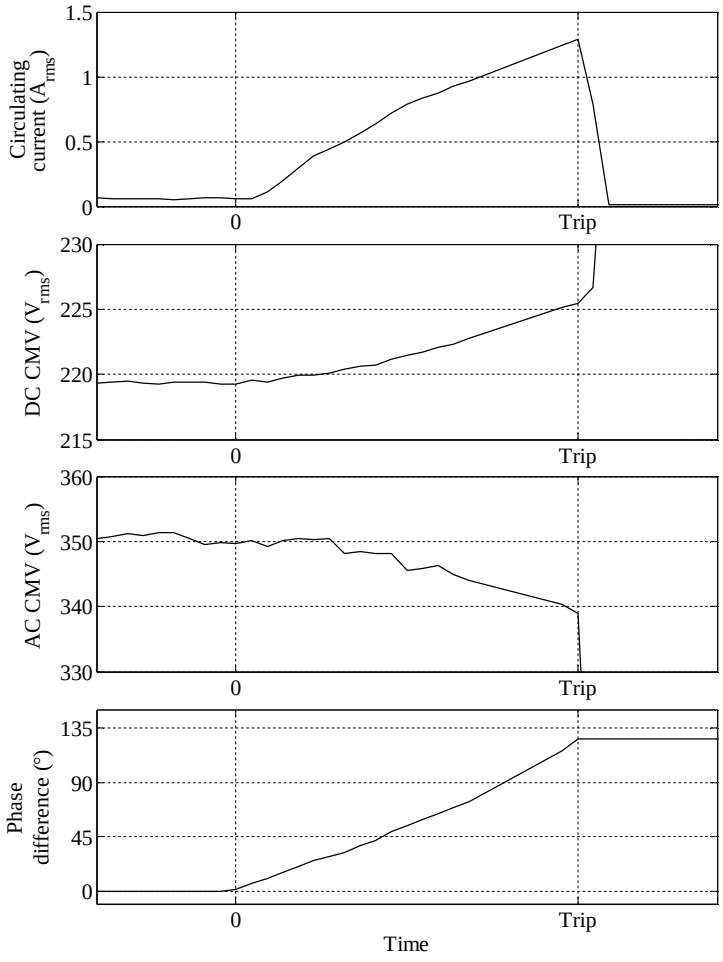


Fig. 4.14. RMS circulating current, the DC and AC RMS common-mode voltages, and the phase difference between the modulators when the two inverters have different switching periods. $T_{sw,inv1}$ = 100 $\mu s$, $T_{sw,inv2}$ = 99.98 $\mu s$. The negative DC buses are connected to the ground with 71 ohm resistors. The inverters start operating with different switching frequencies at time 0. The operation is stopped by a trip.

As the hypothesis predicted, the circulating current is much higher with a fixed grounding. Because of the higher circulating current, the inverters could not operate with a phase difference larger than 130°. With a phase difference of 130°, the RMS value of the circulating current exceeded 1.2 A.

It can be seen in Fig. 4.14 that the circulating current is highly proportional to the phase difference. However, the voltages of the system are tied to the ground potential, and thus, the change in the common-mode voltages is much smaller than when the solar panels are floating from the ground potential.

## 4.5 Discussion

As can be seen in this chapter, the common-mode voltage and the circulating current measurements can be used to synchronize the parallel-connected inverters and to minimize the circulating current between the parallel-connected inverters. The different control strategies are comparable by the circulating current RMS value in the constant state of the control. The RMS values are calculated over 10 s to get the average circulating current over the whole P&O oscillation. The RMS circulating current values can be seen in Table 4.1.

Table 4.1
RMS circulating current values after different control methods.

| Control | $I_{circ}$ |
|---|---|
| Original 180° phase shift | 0.85 A |
| Current based sweep control | 0.11 A |
| Filtered current based P&O control | 0.12 A |
| Current-based Hybrid control | 0.11 A |
| DC CMV-based P&O control | 0.13 A |
| AC CMV-based P&O control | 0.49 A |

As indicated in Section 2.2.4, the circulating current limits given in the standards are 0.03 A for solar panels with a possibility of a direct contact with a person and 0.3 A for solar panels with the prevented possibility of a direct contact with a person. The AC CMV-measurement-based control reduces the circulating current to 0.49 A from the original 0.85 A. The AC CMV control is not able to find the perfect synchronization, but oscillates near a 30° phase difference, where the circulating current is not even below the fire hazard level. Thus, the AC CMV-measurement-based control is not reliable for minimizing the circulating current.

All the other controls decrease the circulating current to 13%–15% of the maximum. The sweep-based control requires routine sweeps where the maximum circulating current is reached momentarily. Thus, the sweep control is not the optimal control method for the circulating current either. The DC CMV-based control, the filtered current-based control, and the hybrid current-based control are thus the preferred controls of the tested ones. All

of these controls reduce the circulating current below the fire hazard limit. However, the protection against direct contact cannot be achieved by the synchronization in this setup. Circulating current filtering is required in order to achieve the direct contact level.

# Chapter 5

# Conclusions

*In this chapter, the results are discussed in more detail, conclusions are summarized, and suggestions for future study are presented.*

## 5.1 Summary

The problem of circulating current in parallel PV inverters was the research subject of this doctoral dissertation. The previous studies have indicated that the circulating current can be limited by synchronizing the modulators of the parallel inverters.

In Chapter 2, the theory for the circulating current between parallel-connected inverters is presented. It is shown that the circulating current is derived from the common-mode voltage difference between the two inverters. It is further shown that by synchronizing the parallel inverters, the common-mode voltage difference between the inverters is reduced. Thus, the circulating current is mitigated by synchronizing the modulators of the inverters.

Alternative measurement methods are studied for the direct circulating current measurement. Equations in Chapter 2 indicate that the circulating current between the parallel inverters can also be obtained by voltage measurements. The common-mode voltage on the DC side of the inverter or on the AC side of the grid filter indicates the circulating current. On the DC side of the inverter, the common-mode voltage is an integral of the circulating current, while on the AC side the RMS common-mode voltage is inversely proportional to the RMS circulating current.

In Chapter 3, a method for synchronizing the parallel inverters without a communication link is introduced. The method makes it possible to control the circulating current independently in each inverter. Feasible control algorithms are presented for minimizing the circulating current. Both circulating-current-based controls and common-mode voltage-based controls are generated.

The generated controls and measurements are tested with an experimental setup composed of two parallel PV inverters and two solar arrays. The perturb and observe type controllers

for controlling the synchronization are implemented to the circulating current measurements and to the common-mode voltage measurements. It is indicated that if a simple P&O controller is desired, preliminary filtering is required. The harmonic components of the switching frequency can disturb the P&O controller. Local minimum and maximum values may appear in the circulating current. These minima and maxima are the result of the harmonic components of the switching frequency, generated by the modulators of the inverters, which are then amplified by the common-mode circuit frequency response. It is indicated that especially the second and third harmonic components of the switching frequency are problematic. When the pure switching frequency component can be acquired, the control task can be executed with a simple hill-climbing P&O controller.

The AC common-mode voltage-based controller did not reach the full synchronization. The control found the minimum around the 30° phase difference. The circulating-current-based controllers and the DC common-mode voltage-based controller reached a nearly perfect synchronization. Only a small oscillation is visible around the synchronization. The oscillation is a characteristic behavior of the P&O controller. The controller managed to reduce the RMS circulating current from the worst case of 0.85 A to 0.11 A–0.13 A. Thus, it is shown that the controllers work properly and significantly decrease the circulating current.

## 5.2 Suggestions for future work

In the course of the study, certain topics of further interest have arisen.

One of the main research objectives was to remove the need for individual isolating transformers or special multiprimary transformers. This doctoral dissertation demonstrates how to minimize the circulating current in order to be able to remove the need for transformers. However, the actual criteria for the demand for transformers is not clear, and further studies should be carried out to verify if the actions in this dissertation are comprehensive enough to remove the need for extra isolating transformers in the PV inverters.

The experimental setup used in this study did not include any common-mode current filters, and thus, the circulating current can be further reduced by implementing actual filters. The direct-contact circulating current limit of 30 mA was not achieved by the synchronization, and it could be further studied if the addition of common-mode current filters can reduce the circulating current below the limit of 30 mA.

Even though two special situation setups were examined, viz. the grounded LCL filter and the grounded negative DC bus, different setups should be further studied with both theoretical and experimental tools. Also the unexpected behavior of the AC common-mode voltage based control should be further evaluated.

The robustness of the control algorithms was only tested with two parallel inverters, where the circulating current is controlled by one inverter. A further topic of interest arose considering the setup of multiple parallel-connected inverters. In theory, the measurements and control are suitable for *n* parallel-connected inverters. The experimental verification calls for further study.

The measurements and the control are theoretically valid also for multilevel inverters. The study in this dissertation was carried out only with two-level inverters. Experimental verifications of the control are required for multilevel inverters. Again, further theoretical questions may arise with the multilevel systems.

A further application may include the circulating current or common-mode voltage measurements. The option of using the measurements for condition monitoring of the solar plant should be studied. The changes in the RMS values of the common-mode parameters could indicate a change in the parasitic capacitances of the solar array.

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# Appendix A
# Mesh analysis of parallel-connected inverters

A mesh analysis is provided for $n$ parallel-connected inverters as illustrated in Fig. A.1.

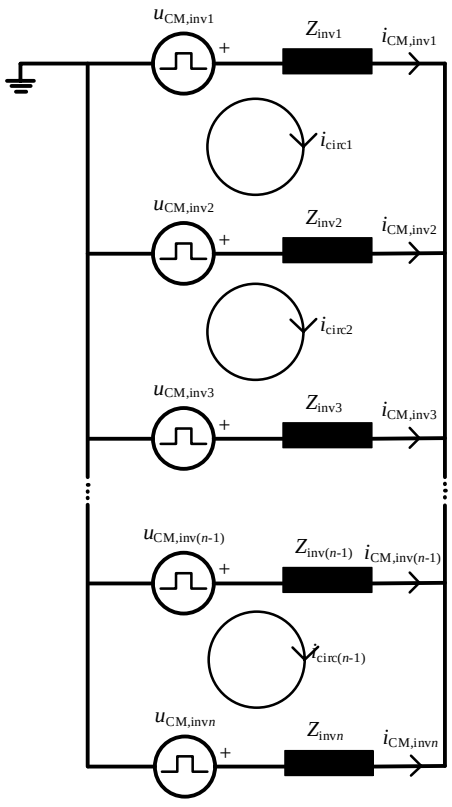


Fig. A.1. Circuit diagram of the mesh analysis with $n$ parallel-connected inverters.

The mesh analysis is started by generating equations for the parallel-connected setup. The voltages in the loops can be calculated by Kirchhoff's voltage law as

$$U_{\mathrm{CM,inv1}} - U_{\mathrm{CM,inv2}} = (Z_{\mathrm{inv1}} + \mathrm{Z}_{\mathrm{inv2}})I_{\mathrm{circ1}} - \mathrm{Z}_{\mathrm{inv2}}I_{\mathrm{circ2}}, \tag{A.1}$$

$$U_{\mathrm{CM,inv2}} - U_{\mathrm{CM,inv3}} = (Z_{\mathrm{inv2}} + \mathrm{Z}_{\mathrm{inv3}})I_{\mathrm{circ2}} - \mathrm{Z}_{\mathrm{inv2}}I_{\mathrm{circ1}} - \mathrm{Z}_{\mathrm{inv3}}I_{\mathrm{circ3}}, \tag{A.2}$$

$$\begin{aligned} U_{\mathrm{CM,invi}} - U_{\mathrm{CM,inv(i+1)}} = {} & \left(Z_{\mathrm{invi}} + \mathrm{Z}_{\mathrm{inv(i+1)}}\right)I_{\mathrm{circi}} - \mathrm{Z}_{\mathrm{invi}}I_{\mathrm{circ(i-1)}} \\ & -\mathrm{Z}_{\mathrm{inv(i+1)}}I_{\mathrm{circ(i+1)}}, \end{aligned} \tag{A.3}$$

$$U_{\mathrm{CM,inv}(n-1)} - U_{\mathrm{CM,inv}n} = \left(Z_{\mathrm{inv}(n-1)} + \mathrm{Z}_{\mathrm{inv}n}\right)I_{\mathrm{circ}(n-1)} - \mathrm{Z}_{\mathrm{inv}(n-1)}I_{\mathrm{circ}(n-2)}. \tag{A.4}$$

By regrouping the previous equations, a matrix representation can be formed of the mesh analysis as

$$\boldsymbol{U} = \boldsymbol{Z}\boldsymbol{I}, \tag{A.5}$$

where

$$\boldsymbol{U} = \begin{bmatrix} U_{\mathrm{CM,inv1}} - U_{\mathrm{CM,inv2}} \\ U_{\mathrm{CM,inv2}} - U_{\mathrm{CM,inv3}} \\ U_{\mathrm{CM,inv3}} - U_{\mathrm{CM,inv4}} \\ U_{\mathrm{CM,inv4}} - U_{\mathrm{CM,inv5}} \\ \vdots \\ U_{\mathrm{CM,inv}(n-2)} - U_{\mathrm{CM,inv}(n-1)} \\ U_{\mathrm{CM,inv}(n-1)} - U_{\mathrm{CM,inv}n} \end{bmatrix}, \tag{A.6}$$

$$\boldsymbol{Z} = \begin{bmatrix} Z_{\mathrm{inv1}} + Z_{\mathrm{inv2}} & -Z_{\mathrm{inv2}} & 0 & 0 & \cdots & 0 & 0 \\ -Z_{\mathrm{inv2}} & Z_{\mathrm{inv2}} + Z_{\mathrm{inv3}} & -Z_{\mathrm{inv3}} & 0 & \cdots & 0 & 0 \\ 0 & -Z_{\mathrm{inv3}} & Z_{\mathrm{inv3}} + Z_{\mathrm{inv4}} & -Z_{\mathrm{inv4}} & \cdots & 0 & 0 \\ 0 & 0 & -Z_{\mathrm{inv4}} & Z_{\mathrm{inv4}} + Z_{\mathrm{inv5}} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & Z_{\mathrm{inv}(n-2)} + Z_{\mathrm{inv}(n-1)} & -Z_{\mathrm{inv}(n-1)} \\ 0 & 0 & 0 & 0 & \cdots & -Z_{\mathrm{inv}(n-1)} & Z_{\mathrm{inv}(n-1)} + Z_{\mathrm{inv}n} \end{bmatrix}, \tag{A.7}$$

$$\boldsymbol{I} = \begin{bmatrix} I_{\mathrm{circ1}} \\ I_{\mathrm{circ2}} \\ I_{\mathrm{circ3}} \\ I_{\mathrm{circ4}} \\ \vdots \\ I_{\mathrm{circ(n-2)}} \\ I_{\mathrm{circ(n-1)}} \end{bmatrix}. \tag{A.8}$$

As shown in Fig. A.1, the combined common-mode current of the first inverter is the same as $I_{\mathrm{circ1}}$. $I_{\mathrm{circ1}}$ can be calculated from (A.5)–(A.8) by using Cramer's rule (Cramer, 1750). Cramer's rule indicates that a single value of vector $\boldsymbol{x} = [x_1\ x_2\ x_3\ \ldots\ x_n]^{\mathrm{T}}$ in the equation

$$\boldsymbol{Ax} = \boldsymbol{b}, \tag{A.9}$$

has a solution given by

$$x_i = \frac{\det(\boldsymbol{A}_i)}{\det(\boldsymbol{A})}, \tag{A.10}$$

where $i = 1, 2, \ldots, n$ and $\boldsymbol{A}_i$ is a matrix formed by replacing the *i*th column of $\boldsymbol{A}$ by $\boldsymbol{b}$. This denotes that

$$I_{circ1} = \frac{\det(\boldsymbol{Z_1})}{\det(\boldsymbol{Z})}, \tag{A.11}$$

where $\boldsymbol{Z}$ is indicated in Eq. (A.7) and $\boldsymbol{Z_1}$

$$= \begin{bmatrix} U_{\mathrm{CM,inv1}} - U_{\mathrm{CM,inv2}} & -Z_{\mathrm{inv2}} & 0 & 0 & \cdots & 0 & 0 \\ U_{\mathrm{CM,inv2}} - U_{\mathrm{CM,inv3}} & Z_{\mathrm{inv2}} + Z_{\mathrm{inv3}} & -Z_{\mathrm{inv3}} & 0 & \cdots & 0 & 0 \\ U_{\mathrm{CM,inv3}} - U_{\mathrm{CM,inv4}} & -Z_{\mathrm{inv3}} & Z_{\mathrm{inv3}} + Z_{\mathrm{inv4}} & -Z_{\mathrm{inv4}} & \cdots & 0 & 0 \\ U_{\mathrm{CM,inv4}} - U_{\mathrm{CM,inv5}} & 0 & -Z_{\mathrm{inv4}} & Z_{\mathrm{inv4}} + Z_{\mathrm{inv5}} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ U_{\mathrm{CM,inv(n-2)}} - U_{\mathrm{CM,inv(n-1)}} & 0 & 0 & 0 & \cdots & Z_{\mathrm{inv(n-2)}} + Z_{\mathrm{inv(n-1)}} & -Z_{\mathrm{inv(n-1)}} \\ U_{\mathrm{CM,inv(n-1)}} - U_{\mathrm{CM,invn}} & 0 & 0 & 0 & \cdots & -Z_{\mathrm{inv(n-1)}} & Z_{\mathrm{inv(n-1)}} + Z_{\mathrm{invn}} \end{bmatrix}.$$

Equation (A.11) is the common solution for a circulating current of an inverter in a setup with $n$ parallel inverters. Next, to simplify the equations, two special cases are illustrated. The first special situation is when the common-mode voltages of the different inverters are equal. Hence, $\det(\boldsymbol{Z_1})$ can be written as

$$\det(\boldsymbol{Z_1}) = \begin{vmatrix} 0 & -Z_{\text{inv2}} & 0 & 0 & \cdots & 0 & 0 \\ 0 & Z_{\text{inv2}} + Z_{\text{inv3}} & -Z_{\text{inv3}} & 0 & \cdots & 0 & 0 \\ 0 & -Z_{\text{inv3}} & Z_{\text{inv3}} + Z_{\text{inv4}} & -Z_{\text{inv4}} & \cdots & 0 & 0 \\ 0 & 0 & -Z_{\text{inv4}} & Z_{\text{inv4}} + Z_{\text{inv5}} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & Z_{\text{inv}(n-2)} + Z_{\text{inv}(n-1)} & -Z_{\text{inv}(n-1)} \\ 0 & 0 & 0 & 0 & \cdots & -Z_{\text{inv}(n-1)} & Z_{\text{inv}(n-1)} + Z_{\text{inv}n} \end{vmatrix}, \quad \text{(A.12)}$$

which equals zero. With a zero in the numerator of Eq. (A.11), the circulating current will equal zero. The smaller the differences between the common-mode voltages are, the smaller the numerator of the circulating current (A.11) is. Thus, by minimizing the common-mode voltage difference between the parallel-connected inverters, the circulating current can be minimized.

The second special case is the situation when the impedances of the parallel-connected inverters are equal. The effect of the common-mode voltages can be better evaluated when the impedances are equal. First, the denominator of Eq. (A.11) is formed

$$\det(\boldsymbol{Z}) = \begin{vmatrix} 2Z_{\text{inv}} & -Z_{\text{inv}} & 0 & 0 & \cdots & 0 & 0 \\ -Z_{\text{inv}} & 2Z_{\text{inv}} & -Z_{\text{inv}} & 0 & \cdots & 0 & 0 \\ 0 & -Z_{\text{inv}} & 2Z_{\text{inv}} & -Z_{\text{inv}} & \cdots & 0 & 0 \\ 0 & 0 & -Z_{\text{inv}} & 2Z_{\text{inv}} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & 2Z_{\text{inv}} & -Z_{\text{inv}} \\ 0 & 0 & 0 & 0 & \cdots & -Z_{\text{inv}} & 2Z_{\text{inv}} \end{vmatrix}. \quad \text{(A.13)}$$

The matrix in Eq. (A.13) is in the form of a tridiagonal Toeplitz matrix (Muir, 1960). The determinant of a tridiagonal matrix can be calculated with a recursive function as

$$\begin{aligned} D(-1) &= 0; \\ D(0) &= 1; \\ D(i) &= 2Z_{\text{inv}}\, D(i-1) - Z_{\text{inv}}^2\, D(i-2), \end{aligned} \quad \text{(A.14)}$$

where $D(i)$ is the $i$th determinant of the matrix shown in Eq. (A.13). With the coefficients in question, the recursive function for $(n-1)$ circulating current loops and $n$ parallel inverters can be proved with a mathematical induction to be

$$\det(\boldsymbol{Z}) = D(n-1) = n\,Z_{\text{inv}}^{n-1}. \tag{A.15}$$

In the first step of the induction, the previous equation is shown to work with the first natural number of circulating current loops, which is one. Equation (A.14) has to be equal to Eq. (A.15) with $n = 2$ as

$$D(1) = 2Z_{\text{inv}}\,D(0) - Z_{\text{inv}}^2\,D(-1) = 2Z_{\text{inv}}. \tag{A.16}$$

The equations indicated the same results with one circulating current path. The determinant of $k$ circulating current paths, $D(k)$ is used in the next step of the induction to indicate that if the induction is true with $k$ circulating current paths, the induction is also valid with $k + 1$ circulating current paths. We start with Eq. (A.15) as

$$D(k+1) = (k+2)Z_{\text{inv}}^{k+1}, \tag{A.17}$$

the same result has to be reached by using Eq. (A.14) and the hypothesis that Eq. (A.15) is true with $D(k)$ and $D(k-1)$ as

$$\begin{aligned} D(k+1) &= 2Z_{\text{inv}}\,D(k) - Z_{\text{inv}}^2\,D(k-1) \\ &= 2Z_{\text{inv}}\,(k+1)Z_{\text{inv}}^{k} - Z_{\text{inv}}^2\,kZ_{\text{inv}}^{k-1} \\ &= (2k+2)\,Z_{\text{inv}}^{k+1} - kZ_{\text{inv}}^{k+1} \\ &= (k+2)Z_{\text{inv}}^{k+1}. \end{aligned} \tag{A.18}$$

Thus, (A.15) is shown to be correct with all natural numbers, $\mathbf{N} = \{1,2,3,\ldots\}$

The $\det(\boldsymbol{Z_1})$ can be further calculated when the impedances of the parallel inverters are equal as illustrated in

$$\det(\boldsymbol{Z_1}) = \left(U_{\text{CM,inv1}} - U_{\text{CM,inv2}}\right)\begin{vmatrix} 2Z_{\text{inv}} & -Z_{\text{inv}} & 0 & \cdots & 0 & 0 \\ -Z_{\text{inv}} & 2Z_{\text{inv}} & -Z_{\text{inv}} & \cdots & 0 & 0 \\ 0 & -Z_{\text{inv}} & 2Z_{\text{inv}} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & 2Z_{\text{inv}} & -Z_{\text{inv}} \\ 0 & 0 & 0 & \cdots & -Z_{\text{inv}} & 2Z_{\text{inv}} \end{vmatrix} -$$

$$\left(U_{\text{CM,inv2}} - U_{\text{CM,inv3}}\right)\begin{vmatrix} -Z_{\text{inv}} & 0 & 0 & \cdots & 0 & 0 \\ -Z_{\text{inv}} & 2Z_{\text{inv}} & -Z_{\text{inv}} & \cdots & 0 & 0 \\ 0 & -Z_{\text{inv}} & 2Z_{\text{inv}} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & 2Z_{\text{inv}} & -Z_{\text{inv}} \\ 0 & 0 & 0 & \cdots & -Z_{\text{inv}} & 2Z_{\text{inv}} \end{vmatrix} +$$

$$(U_{\mathrm{CM,inv3}} - U_{\mathrm{CM,inv4}}) \begin{vmatrix} -Z_{\mathrm{inv}} & 0 & 0 & \cdots & 0 & 0 \\ 2Z_{\mathrm{inv}} & -Z_{\mathrm{inv}} & 0 & \cdots & 0 & 0 \\ 0 & -Z_{\mathrm{inv}} & 2Z_{\mathrm{inv}} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & 2Z_{\mathrm{inv}} & -Z_{\mathrm{inv}} \\ 0 & 0 & 0 & \cdots & -Z_{\mathrm{inv}} & 2Z_{\mathrm{inv}} \end{vmatrix} - \cdots, \quad \text{(A.19)}$$

where the new determinants are $(n-2) * (n-2)$ in size. By using Eq. (A.15), the determinants can be simplified into

$$\det(\boldsymbol{Z_1}) = \left(U_{\mathrm{CM,inv1}} - U_{\mathrm{CM,inv2}}\right)(n-1)\, Z_{\mathrm{inv}}^{n-2} +$$

$$Z_{\mathrm{inv}}(U_{\mathrm{CM,inv2}} - U_{\mathrm{CM,inv3}}) \begin{vmatrix} 2Z_{\mathrm{inv}} & -Z_{\mathrm{inv}} & \cdots & 0 & 0 \\ -Z_{\mathrm{inv}} & 2Z_{\mathrm{inv}} & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & 2Z_{\mathrm{inv}} & -Z_{\mathrm{inv}} \\ 0 & 0 & \cdots & -Z_{\mathrm{inv}} & 2Z_{\mathrm{inv}} \end{vmatrix} -$$

$$Z_{\mathrm{inv}}\left(U_{\mathrm{CM,inv3}} - U_{\mathrm{CM,inv4}}\right) \begin{vmatrix} -Z_{\mathrm{inv}} & 0 & \cdots & 0 & 0 \\ -Z_{\mathrm{inv}} & 2Z_{\mathrm{inv}} & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & 2Z_{\mathrm{inv}} & -Z_{\mathrm{inv}} \\ 0 & 0 & \cdots & -Z_{\mathrm{inv}} & 2Z_{\mathrm{inv}} \end{vmatrix} + \cdots. \quad \text{(A.20)}$$

Equation (A.20) shows that the determinants have lost a single row and a single column and acquired $Z_{\mathrm{inv}}$ as a gain, but otherwise remained the same as in Eq. (A.19). This recursive simplification can be calculated until $(n-1)$ loops, when the result can be expressed as

$$\begin{aligned} \det(\boldsymbol{Z_1}) &= \left(U_{\mathrm{CM,inv1}} - U_{\mathrm{CM,inv2}}\right)(n-1) Z_{\mathrm{inv}}^{n-2} \\ &+ Z_{\mathrm{inv}}(U_{\mathrm{CM,inv2}} - U_{\mathrm{CM,inv3}})(n-2)\, Z_{\mathrm{inv}}^{n-3} \\ &+ Z_{\mathrm{inv}}^{2}(U_{\mathrm{CM,inv3}} - U_{\mathrm{CM,inv4}})(n-3)\, Z_{\mathrm{inv}}^{n-4} + \cdots \\ &+ Z_{\mathrm{inv}}^{n-3}(U_{\mathrm{CM,inv}(n-1)} - U_{\mathrm{CM,inv}n})(n-(n-1))\, Z_{\mathrm{inv}}^{n-(n-1)}. \end{aligned} \quad \text{(A.21)}$$

The equation can be simplified further by taking the impedance as a common factor and opening the common-mode voltage difference brackets as

$$\det(\boldsymbol{Z_1}) = Z_{\text{inv}}^{n-2}\big(U_{\text{CM,inv1}}(n-1) - U_{\text{CM,inv2}}(n-1) + U_{\text{CM,inv2}}(n-2)$$

$$- U_{\text{CM,inv3}}(n-2) + U_{\text{CM,inv3}}(n-3) - U_{\text{CM,inv4}}(n-3)$$

$$+ U_{\text{CM,inv4}}(n-4) - U_{\text{CM,inv5}}(n-4) + \cdots + U_{\text{CM,inv}(n-1)}(1) - U_{\text{CM,inv}n}(1)\big), \quad \text{(A.22)}$$

when the equation can be expressed as

$$\det(\boldsymbol{Z_1}) = Z_{\text{inv}}^{n-2}\big(U_{\text{CM,inv1}}(n-1) - U_{\text{CM,inv2}} - U_{\text{CM,inv3}} - U_{\text{CM,inv4}} - \cdots$$

$$- U_{\text{CM,inv}(n-1)} - U_{\text{CM,inv}n}\big). \quad \text{(A.23)}$$

With Eqs. (A.15) and (A.23), the circulating current of the first inverter (A.11) in a parallel connection of $n$ inverters with identical impedances can be expressed as

$$I_{circ1} = \frac{U_{\text{CM,inv1}}(n-1) - U_{\text{CM,inv2}} - U_{\text{CM,inv3}} - U_{\text{CM,inv4}} - \cdots - U_{\text{CM,inv}n}}{nZ_{\text{inv}}}. \quad \text{(A.24)}$$

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