Lappeenranta University of Technology

School of Energy Systems

Degree Program in Electrical Engineering

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PRACTICAL APPROACH TO MAIN CIRCUIT AND EMI FILTER DESIGN OF A 15 KW DUAL ACTIVE BRIDGE CONVERTER

Examiners :   Professor Pertti Silventoinen

              Master of Science Jani Hiltunen

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ABSTRACT

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Master's Thesis

2017

54 pages, 14 figures, 8 tables

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Keywords: dual active bridge, power electronics, electromagnetic interference, DC/DC converter, practical, single phase shift, LC-filter

Fast paced product development does not leave much room for theoretical optimization of power electronic systems. There seems to be a lack of publications, which could be directly used as a reference for practical design of the bidirectional DC/DC converter called Dual Active Bridge. This thesis tries to fill a part of this void by presenting basic theory and easy and straightforward tools to calculate electrical parameters of the converter, which can be used for initial component selection for the main circuit and filters against electromagnetic interference. These estimates are based on ideal model of the converter and therefore generous margins must be used to make sure that the prototype will fulfil the set requirements. The room for optimization is created by selecting components wisely, which allows changing electrical parameters of the circuit in some extent at the prototyping phase without need to make changes to the printed circuit board. Design of a 15 kW converter is presented as an and components are also selected when possible.

TIIVISTELMÄ

Lappeenrannan teknillinen yliopisto

School of Energy Systems

Sähkötekniikan koulutusohjelma

Esa Malinen

DAB-konvertterin pääpiirin ja häiriösuotimien käytännönläheinen suunnittelu

Diplomityö

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Hakusanat: tehoelektroniikka, sähkömagneettinen häiriö, DC/DC-muunnin, käytännönläheinen, LC-suodin

Keywords: dual active bridge, power electronics, electromagnetic interference, DC/DC converter, practical, single phase shift, LC-filter

Nopeatempoisessa tehoelektroniikkajärjestelmien tuotekehityksessä ei ole usein varaa tehdä teoreettista optimointia. Kaksisuuntaisten DAB-konverttterien (Dual Active Bridge) käytännönläheiseen suunnitteluun liittyviä julkaisuja, joita pystyisi suoraan käyttämään apuna, ei juurikaan ole. Tämän työn tarkoitus on korjata tilannetta esittämällä tarvittava teoria ja tarjota helppoja sekä suoraviivaisia työkaluja konvertterin sähköisien arvojen laskemiseksi, joiden avulla voidaan tehdä ensimmäiset pääpiirin ja häiriösuotimien komponenttivalinnat. Nämä arviot perustuvat konvertterin ideaaliseen malliin, joten suunnittelussa on käytettävä reiluja turvamarginaaleja, jotta varmistutaan siitä, että konvertteri täyttää sille asetetut vaatimukset. Mahdollisuus optimoinnille luodaan valitsemalla komponentit siten järkevästi, että jonkin verran muutoksia prototyypin sähköisiin arvoihin pystytään tekemään muuttamatta piirilevyä. Esimerkkinä tässä työssä suunnitellaan 15 kW konvertteri ja osat valitaan niiltä osin kuin se on mahdollista.

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LIST OF SYMBOLS AND ABBREVIATIONS

C	Capacitance
D	Phase shift ratio
d	Voltage ratio
f	Frequency
i	AC current
I	DC current
L	Inductance, Laplace function
n	Turns ratio
P	Power
q	Charge
R	Resistance
r	Ripple factor
s	Laplace variable
t	Time
T	Time Period, Transistor, Temperature
u	AC voltage
U	DC voltage
ω	Angular frequency

AC	Alternating Current
BESS	Battery Energy Storage System
CISPR	Comité International Spécial des Perturbations Radioélectriques
DAB	Dual Active Bridge
DC	Direct Current
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
EU	European Union
IET	International Electrotechnical Comission

IGBT	Insulated Gate Bipolar Transistor
LISN	Line Impedance Stabilization Network
MLCC	Multilayer Ceramic Capacitor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracker
PCB	Printed Circuit Board
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Mean Square
Si	Silicon
SiC	Silicon-Carbide
SPS	Single Phase Shift
VFM	Variable Frequency Modulation
ZVS	Zero Voltage Switching

Subscripts

BESS	BESS side of the converter
c	Case
d	Damping
D	Drain, Diode
dead	Dead time
ds	Drain-Source
in	Input
j	Junction
lk	Leakage
max	Maximum
min	Minimum
N	Nominal
on	On-state
oss	Output
out	Output

pri   Primary

pulse Pulse

PV   PV side of the converter

r   Ripple

s   Switching

sec   Secondary

ZVS   Zero Voltage Swithing

φ Phase shift

1 INTRODUCTION

1.1 Background

Capacity of installed photovoltaic (PV) systems has been increasing exponentially all over the world, which is positive trend for health of the Earth, but it also brings in some problems. For instance, Germany introduced their new Energy Concept for increasing share of renewable energy production in the country at year 2010 (Federal Ministry for the Environment, Nature Conservation and Nuclear Safety 2010). The plan worked so well that, for example, at 8th of May 2016 renewable power provided around 90 % of the total consumption as shown in Agora Energiewende's data in figure 1.1. Conventional power plants could not reduce their production fast enough to balance the increased power generated mainly by the PV systems. Consumers had to be forced using excess power by driving electricity price highly negative.
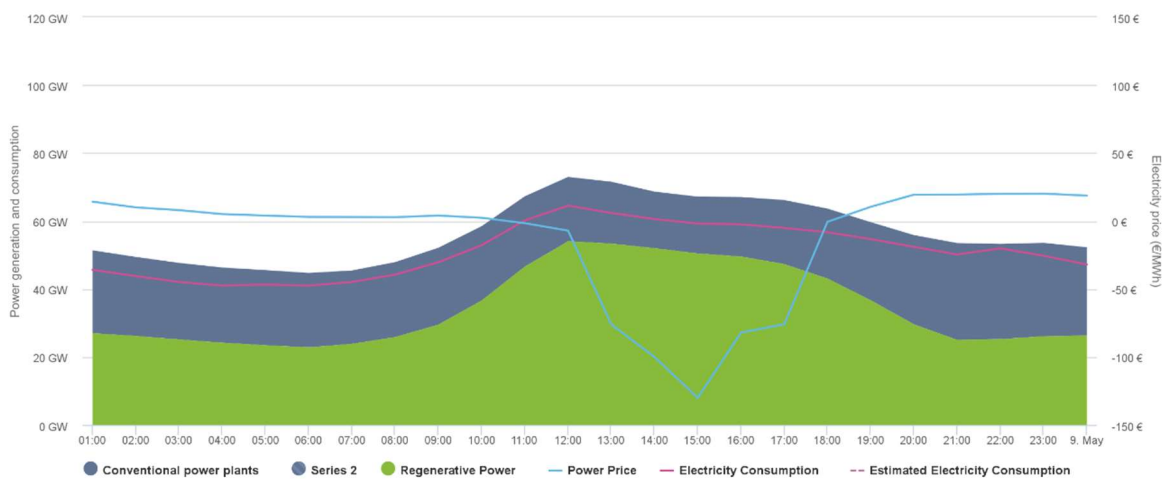

Figure 1.1. Electricity price, consumption and power produced by renewable and conventional plants in Germany 8th of May 2016. (Agora Energiawende)

Total production with near zero emissions can't be achieved with this kind of variability and unpredictability, because there must be a way to provide energy also when the sun is not shining. One good option to overcome this problem is storing excess energy produced at daytime and using it when there is more consumption than production. This would make the need of energy from the grid much more predictable and stable so the amount of conventional power plants could be reduced.

Residential PV systems seems to be the first group to implement energy storage systems in large scale. For example, Sweden offers subsidies for residential energy storage systems which will cover up to 60% of the system cost (Renewable Energy World 2016) and Germany supports these systems with 30 million euros until year 2018 (PV Magazine 2016). Residential houses will have much bigger benefit from the energy storage system than commercial buildings, because the house is often empty and own consumption is small at peak production hours. Batteries are still expensive so payback time of the installation is long, but rapidly increasing popularity of electric vehicles will most probably bring down prices and introduce completely new market of used batteries, which will make storage systems profitable even without subsidies.

Home owners who have an electric vehicle will have also additional benefit from owning an energy storage system; batteries can be used to charge the car rapidly while not affecting the maximum current draw from the grid. At least in Finland, where monthly fees are categorized based on the selected main fusing, this can save a significant amount of money.

This thesis is related to a proof of concept project, where the goal is to create easily retrofittable and affordable Battery Energy Storage System (BESS). Traditional way to add BESS in to existing PV system is AC coupling, in which the battery bank is connected directly to the AC grid using an inverter. In this project, a concept of DC coupling, where the battery bank is connected between the PV panels and the PV inverter (figure 1.2), is implemented and tested. Instead of DC-AC inverter required in the AC-coupled system, this concept is based on a DC-DC converter. Topology selected for the converter is Dual Active Bridge (DAB), which can achieve high efficiency operation in wide voltage and power range.

Based on a market analysis, DC-DC converters with rated power of 5 kW and 15 kW are selected for battery storage integration to most of the common PV system sizes and MPPT configurations. This thesis will focus on the main circuit design of the 15 kW converter.
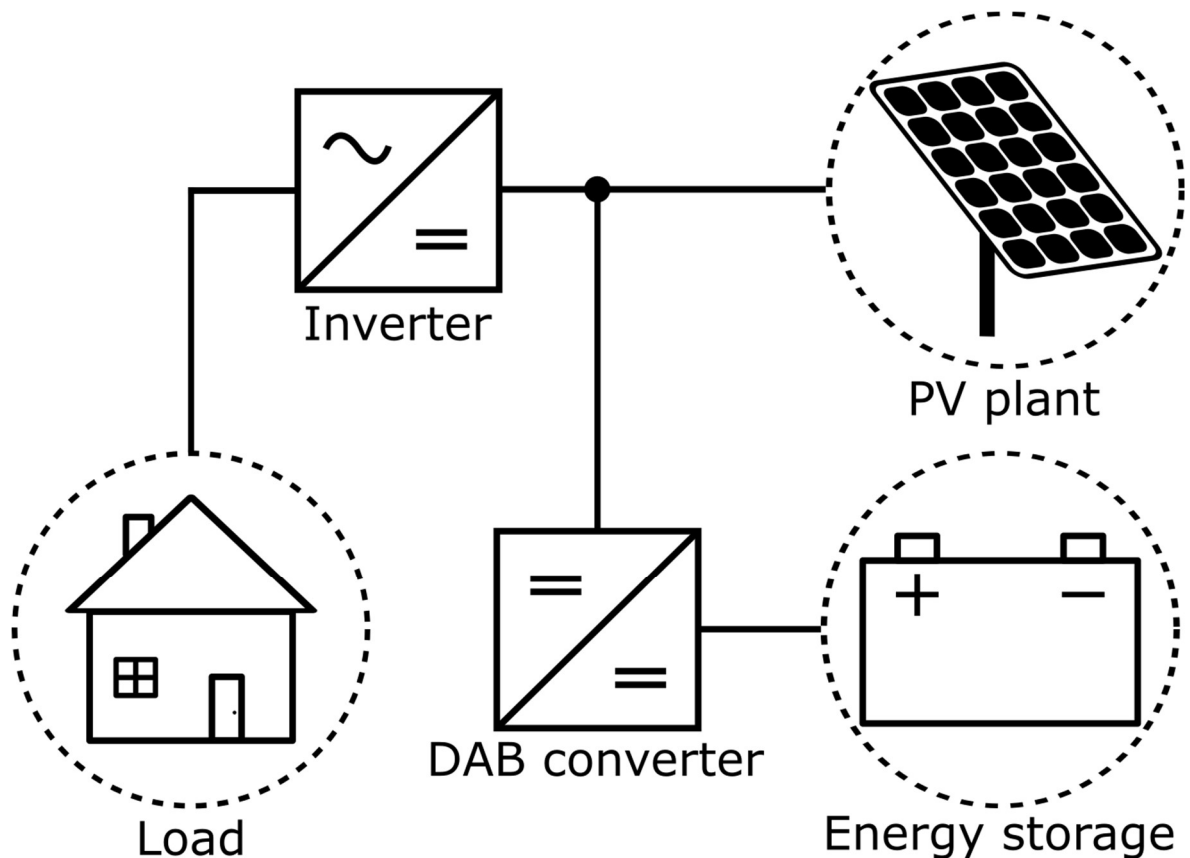
Figure 1.2. Block diagram of the DC coupled energy storage system.

1.2 Goals and delimitations

Design of a power electronic circuit is a difficult balancing act of many different parameters and there are endless amount of publications presenting yet another way to find the optimum values. In practice, rapid product development does not leave much room for optimization. It is often more important to just get a prototype with the basic functionality working in a short time to proof that the new idea is even working and worth investing time and money.

Goal of this thesis is to present tools for calculating initial values for the main circuit components including filtering circuits against electromagnetic interference (EMI). The initial selection of the components for the prototype can be done based on these values and the room for optimization is left for the prototyping phase. The key for optimizing in the prototyping phase is to find components with different electrical values and the same footprint. This gives flexibility to change values in the circuit in some extent without making changes to the printed circuit board (PCB). Some components for the designed converter

must be custom made due to the high power ratings, but selection of suitable transistors and capacitors are presented in this thesis as an example.

The proof of concept project was not progressed in to the prototyping phase of the 15 kW converter when this thesis was written, and for this reason, the results of using the proposed methods could not be presented. This thesis is therefore mainly done as a literature review of the theory of the DAB converter and EMI filters and some design choices like safety margins are based on educated guesses of the author and other product developers involved in the project. This is often necessary in practical development, because optimization of every variable is virtually impossible for such a complex power electronic system like DAB converter.

2 REQUIREMENTS FOR THE CONVERTER

The design of the converter begins from defining the electrical parameters and features, which must be accomplished with the main circuit. Topology to be used is then selected based on these requirements.

First requirement is that the nominal output power P_N should be 15 kW as stated in the previous chapter. The power is defined based on a market analysis of the existing PV systems and estimating the future trends. This analysis was done as a separate study and the details will not be presented here due to non-disclosure restrictions. The converter will be used for charging and discharging the batteries, so the power flow must be bidirectional.

The converter should not change the PV side voltage when solar inverter's maximum power point tracker (MPPT) is active, because it would change the operating point of the solar panel and reduce the efficiency of the solar power plant. In other words, the power control of the PV side is based on current control. As figure 2.1 illustrates, the MPPT tends to keep voltage stable at the nominal PV string voltage even when the production is minimal. To be able to optimize the PV side voltage range of the converter, the most common nominal voltage levels used in 15 kW sized systems must be determined.
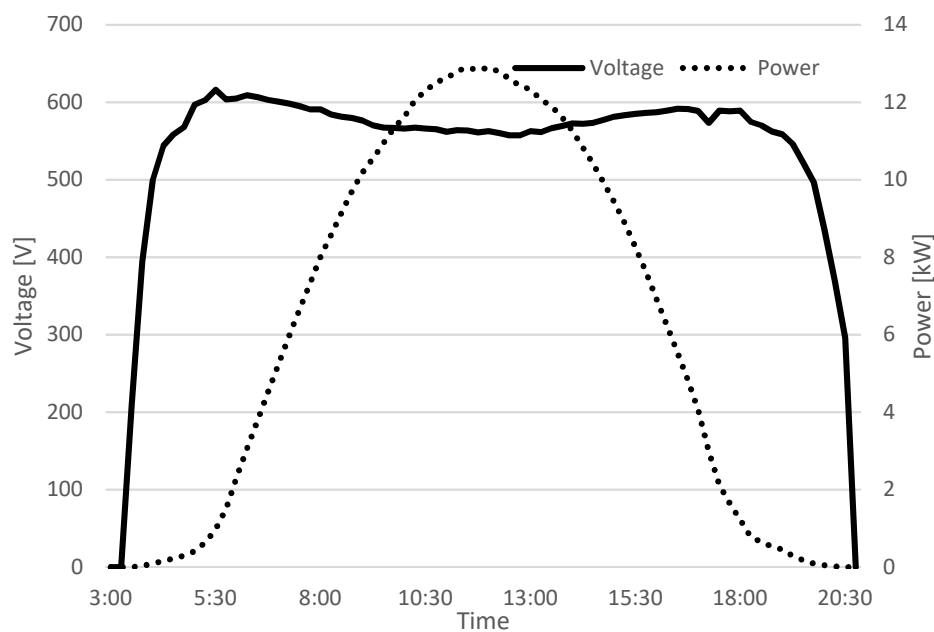
Figure 2.1. Behavior of the PV voltage relative to DC power during a day. Inverter used in this installation is ABB Trio 27.6.

The number of products on the market in the 15 kW range are limited and PV strings are usually sized to be compatible with these devices. Nominal voltages of available inverters can be used to estimate the most common voltage level. As shown in table 2.1, nominal voltages seem to be around 600 V.

Table 2.1. Nominal voltages and MPPT voltage ranges of common PV inverters used in Europe with similar power rating as the converter to be designed. (ABB 2016a, ABB 2016b, Fronius 2017, SMA 2016, Kostal 2016)

Inverter	Nominal voltage [V]	Voltage range [V]
ABB Trio 20.0	620	480 – 800
ABB PVI 12.5	580	445 – 750
Fronius Symo 15	600	320 – 800
Fronius Symo 20	600	420 – 800
SMA Tripower 15000TL	600	360 – 800
Kostal Piko 15	680	390 – 800

To support the previous statement, energy produced at different string voltages was calculated using data obtained from four existing PV plants in nominal power range of 20 kW to 50 kW. This data for one month period is presented in figure 2.2.

Based on this knowledge, nominal voltage $U_{PV,N}$ of the converters PV side is selected to be 600 V, minimum operating voltage $U_{PV,min}$ is 450 V and maximum operating voltage $U_{PV,max}$ is chosen to be 750 V.

Definition of BESS side voltage range was done also as a separate study and will not be presented here for the same reasons than the analysis of the power rating. Nominal voltage $U_{BESS,N}$ is 400 V, minimum voltage $U_{BESS,min}$ is 300 V and maximum voltage $U_{BESS,max}$ is 500 V.
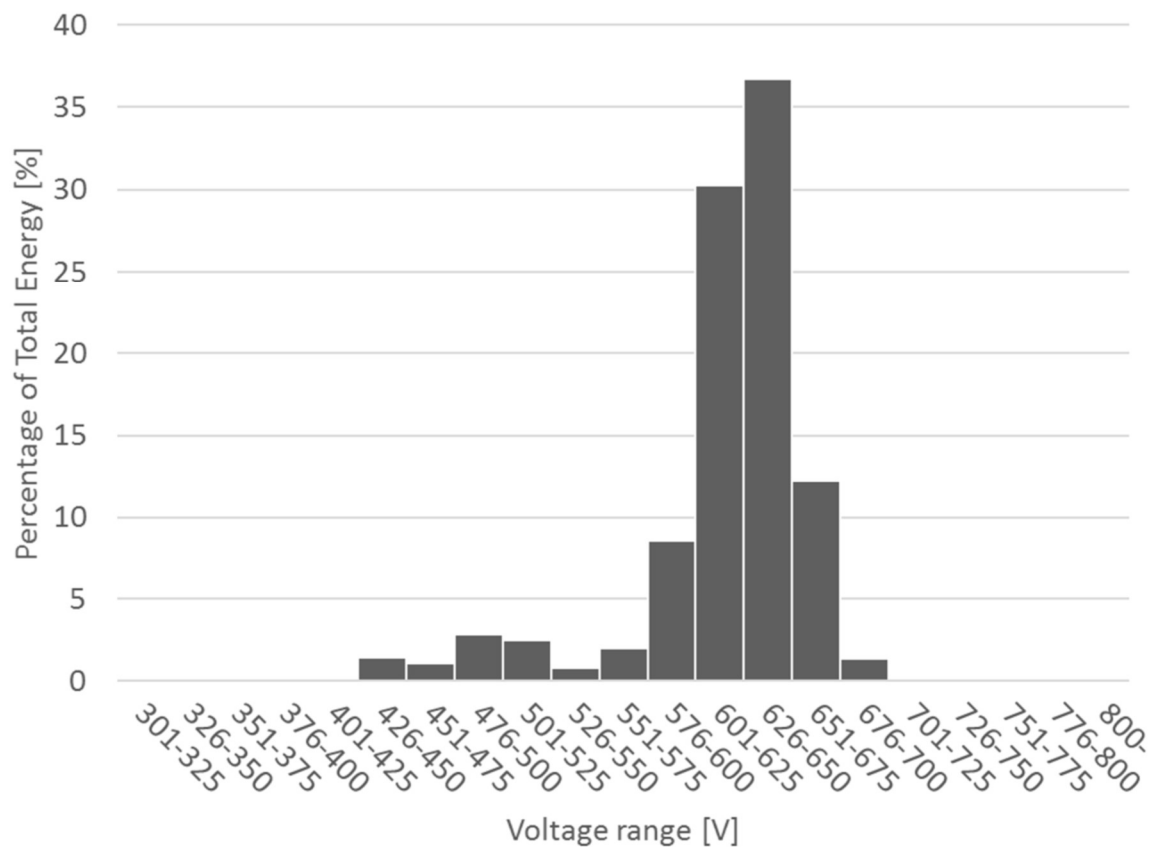
Figure 2.2. Energy produced at different DC string voltage ranges presented as a percentage of the total energy in four PV plants during 8th of April 2017 to 8th of May 2017. Nominal powers of the plants are in the range of 20 kW to 50kW.

Voltage ripple at each side should not be more than 1% to give stable conditions for the control loop of the converter and the PV inverter. Limits for allowed conducted emissions are presented in the EMI filter design chapter 5.

Efficiency should be optimized for conditions where U_{PV} is at the nominal point $U_{PV,N}$ and U_{BESS} is in the range of $U_{BESS,min} - U_{BESS,max}$, because most of the energy is transferred at these operation points. Percentage goals for efficiency will not be set, because calculating the theoretical efficiency is very time-consuming task and therefore it does not support the goal of this thesis. The methods presented later will optimize the efficiency in some level, but the final optimization for each application should be done by measuring the prototype and making necessary changes to raise the efficiency to required level based on these measurements.

The converter will be most probably installed on the wall and it would be preferable if the installation could be done by a single person. For this reason, the power density of the converter should be maximized to keep the weight down.

Isolation is preferred to keep the possible conducted emissions from the PV inverter out of the battery and the topology with a transformer is often more flexible if voltage ranges needs to be changed than non-isolated topologies.

Requirements for the voltages and power are summarized in the following table.

Table 2.2. Requirements for the voltages and output power.

Voltage	Minimum	Nominal	Maximum
PV voltage U_{PV}	450 V	600 V	750 V
BESS voltage U_{BESS}	300 V	400 V	500 V
Power	**Minimum**	**Nominal**	**Maximum**
Output power $P_{PV} = P_{BESS}$	0 W	15 000 W	-

3 DUAL ACTIVE BRIDGE TOPOLOGY

There are two common topologies often used in applications which require isolated highly efficient bidirectional power transfer – Dual Active Bridge and LLC. Both topologies have half-bridge, full-bridge and three phase variations, where each of them have their own pros and cons. Comprehensive comparison between these topologies are done by Krismer (2010) and Khaligh et al. (2017). Full-bridge DAB topology is chosen for this application because it is likely to achieve all the requirements, it is less complex to implement in its simplest form than LLC and it is highly flexible in terms of design and optimization.

3.1 Introduction

De Doncker et al. introduced first time the Dual Active Bridge topology in 1988 (De Doncker et al. 1988) and it has since been popular for example in many energy storage applications (Krismer 2010; Xue et al. 2013; Mi et al. 2008) where bidirectional power flow is necessary to be able to charge and discharge the batteries. One reason for its popularity is that the transistors of the converter can be operated in ZVS (Zero Voltage Switching) conditions also known as soft switching, which dramatically lowers switching losses and decreases electromagnetic interference (Chang et al. 1998).

Another good feature of the DAB is that bidirectional power flow can be controlled with a single parameter if the traditional Single-Phase-Shift (SPS) modulation is used. However, voltage operation area where soft switching is achieved is quite limited with this modulation method, especially at low power levels. This problem has been addressed by deriving many advanced modulation methods by adding degrees of freedom to the control. The SPS modulation method is explained in chapter 3.2.1 and some of the most common advanced methods are briefly introduced in chapter 3.2.2.

As shown in figure 3.1, full-bridge DAB consists of a high frequency transformer and two H-bridges at primary and secondary sides, respectively. Transformer provides isolation, but also makes it possible to set the voltage levels at primary and secondary sides freely by selecting suitable turns ratio n. Turns ratio is defined as a ratio of primary voltage and secondary voltage $n = U_{pri}/U_{sec}$.
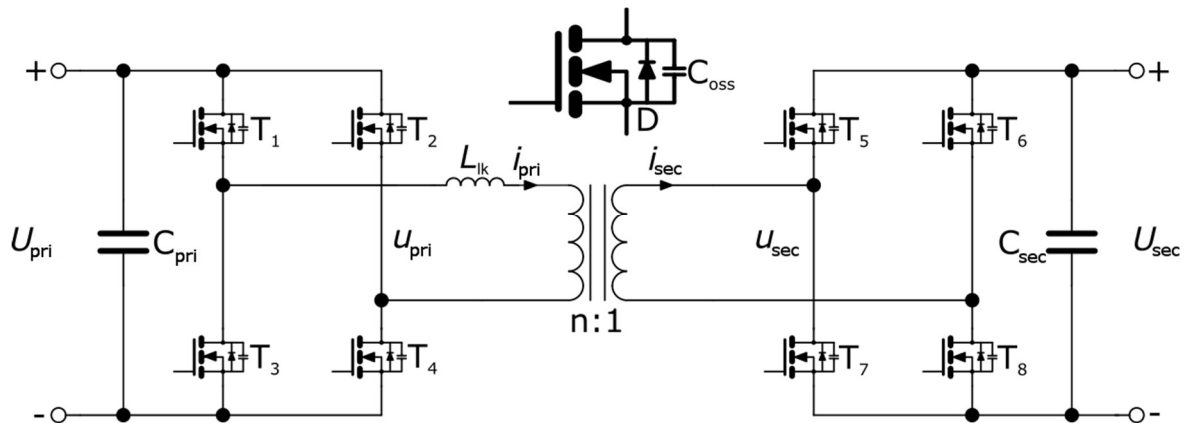
Figure 3.1. Main circuit of the Dual Active Bridge converter.

Leakage inductance L_{lk} is the main energy transfer medium and it is one of the most important parameters of the converter in the design phase. Internal leakage inductance of the transformer is sufficient in some cases, but auxiliary series inductor must be often added. Auxiliary inductor can be used to refine the inductance value in prototyping phase and therefore it is advisable to include if slight reduction of power density is not a problem.

Anti-parallel diode D is necessary to provide return path for the currents and the snubber capacitance C_{oss} is usually present, because IGBT transistors need it to lower the turn-off losses caused by the typical long current tail and it is intrinsic in the MOSFET transistors. More in-depth discussion about IGBT snubber capacitors can be found for example from the (Naayagi et al. 2011). The DAB converters are usually switched at high frequency (>100 kHz) to increase the power density due to smaller magnetic components, which is why fast switching MOSFET transistors are preferred. In addition, MOSFETs have an internal anti-parallel diode and the auxiliary snubber capacitor used with IGBTs can be left out, which simplifies the design.

When parameters of the converter are calculated, amount of capacitance in C_{pri} and C_{sec} are thought to be infinite. This means that there is no voltage ripple and constant voltages U_{pri} and U_{sec} can be used in the calculations. In practice, these capacitances must be designed to achieve some finite voltage ripple value and additional current filtering is also added. EMI filter circuits are designed in chapter 5.

3.2 Modulation methods

One of the main attractions of the DAB is that with the simplest method of control, the power flow can be controlled with a single parameter. But of course, the eternal pursuit of achieving better efficiency and higher power density has coined many more advanced and complex methods, which aim to increase the soft switching region and minimize circulating currents. Only one method, the traditional SPS modulation, is presented in detail in this thesis, because the focus is on presenting a straight forward way to design a working main circuit for the first prototype. If efficiency of the prototype is not high enough for the given application, it can be then increased without major hardware changes by just using one of these more complex modulation methods or even a combination.

3.2.1 Single-phase-shift modulation

Simplest and most common control method for DAB is the single-phase-shift (SPS) modulation (Kheraluwala et al. 1992), also known as just phase-shift modulation (Krismer 2010). In this control method, both H-bridges are modulating symmetric bipolar square wave voltage to the common energy transfer element, leakage inductance L_{lk}, and the phase shift between these voltages defines the DC power flow. Ideal circuit can be presented as a circuit in figure 3.2, where two PWM generators are supplying voltage to a common inductor.
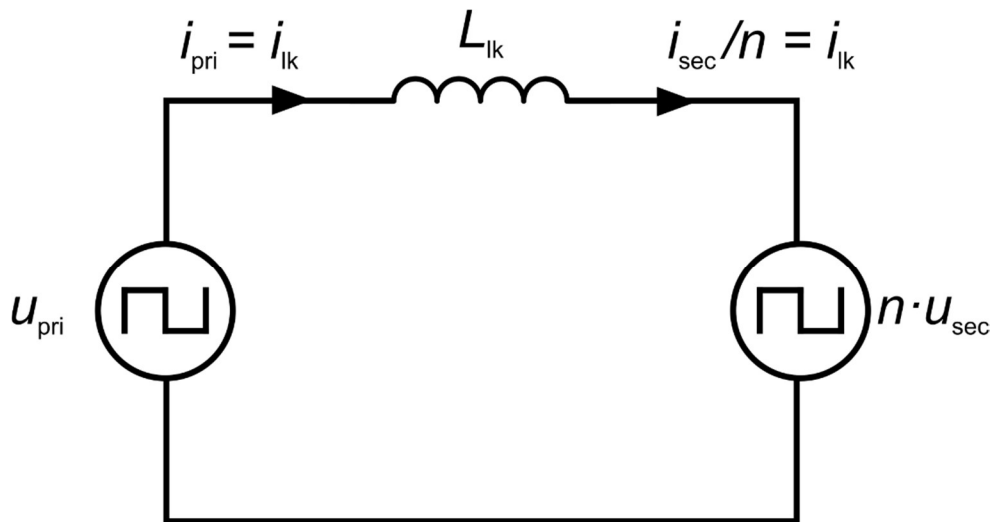

Figure 3.2. Simplified DAB circuit, where H-bridges are replaced with square wave generators producing voltages u_{pri} and u_{sec} and transformer is presented as its leakage inductance L_{lk}. Transformer turns ratio n is taken account by referring secondary side values to primary side.

The primary side AC voltage u_{pri} has an amplitude of the primary side DC voltage U_{pri} and correspondingly secondary side AC voltage u_{sec} has the amplitude of U_{sec}. Voltage difference between u_{pri} and u_{sec} over the transformer determines the induced leakage inductor current i_{lk}. According to Krismer (2010), the leakage current i_{lk} for first half of the switching period T_{s} can be calculated using equations

$$i_{\text{lk}}(t) = i_{\text{lk},0} + \frac{(U_{\text{pri}} + nU_{\text{sec}})\,t}{L_{\text{lk}}} \quad \forall\ 0 < t < T_{\varphi}, \tag{3.1}$$

$$i_{\text{lk}}(t) = i_{\text{lk}}(T_{\varphi}) + \frac{(U_{\text{pri}} - nU_{\text{sec}})(t - T_{\varphi})}{L_{\text{lk}}} \quad \forall\ T_{\varphi} < t < T_{\text{s}}/2. \tag{3.2}$$

And due to the half cycle symmetry, current i_{lk} is defined for the second half of the period as

$$i_{\text{lk}}(t + T_{\text{s}}/2) = -i_{\text{lk}}(t). \tag{3.3}$$

Initial current $i_{\text{lk},0}$ is defined as

$$i_{\text{lk},0} = i_{\text{lk}}(0) = \frac{nU_{\text{sec}}(1 - 4f_{\text{s}}T_{\varphi}) - U_{\text{pri}}}{4f_{\text{s}}L_{\text{lk}}} \tag{3.4}$$

and T_{φ} is the length of the phase shift period between the two AC voltages. It can be controlled with a single variable D which is defined as a ratio of switching period

$$T_{\varphi} = DT_{\text{s}}. \tag{3.5}$$

Phase shift ratio D is the only parameter needed to control the power flow of the DAB. Power equation for the ideal converter was first derived by Kheraluwala et al. (1992). The equation with modified definition of phase shift ratio D is defined as

$$P = \frac{U_{\text{pri}}nU_{\text{sec}}}{f_{\text{s}}L_{\text{lk}}} D(1 - 2|D|) \quad \forall\ -0.25 < D < 0.25, \tag{3.6}$$

where P is the DC power in primary and secondary side and f_s is the switching frequency defined as inverse of switching period T_s.

As shown in figure 3.3, maximum power P_{max} is achieved with a phase shift ratio $D = \pm 0.25$.
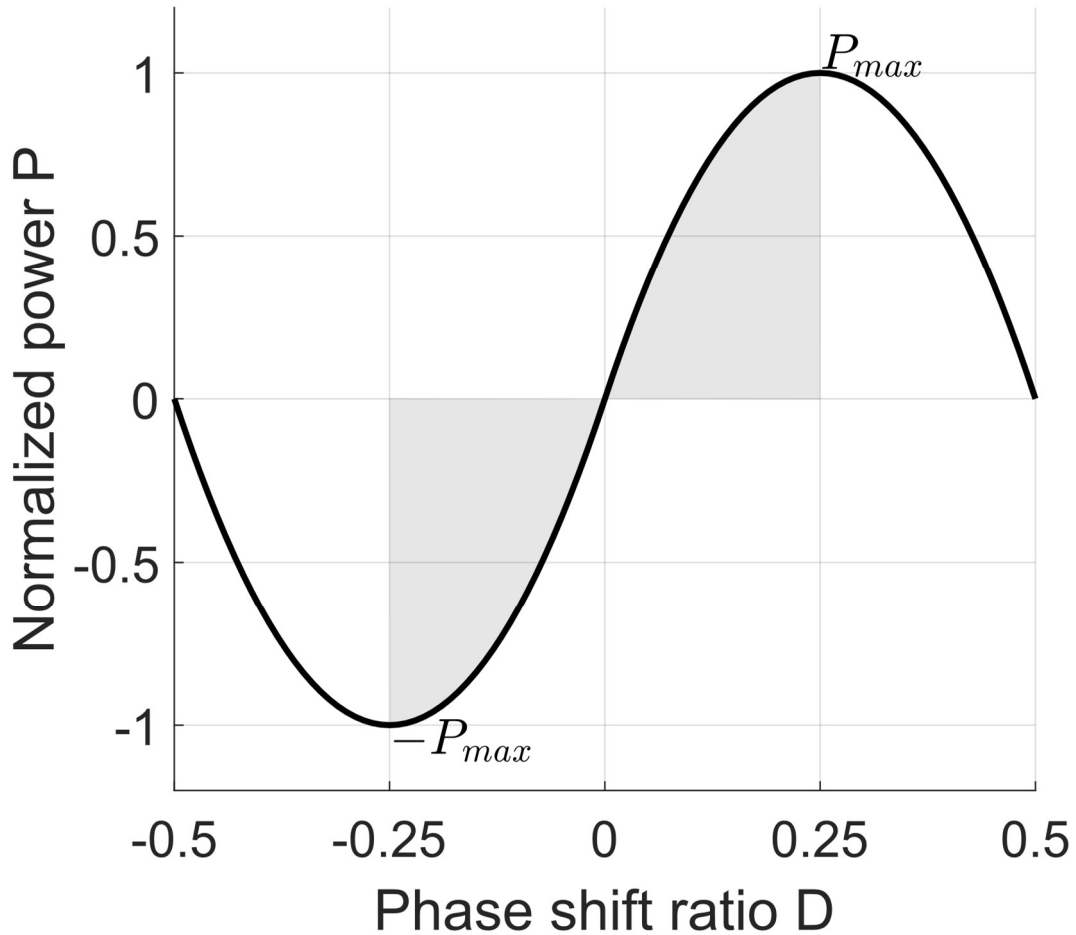

Figure 3.3. Normalized power P as function of phase shift ratio D. Maximum power P$_{max}$ is achieved when phase shift is 0.25 or -0.25. Operating area is highlighted with grey color.

By inserting phase shift ratio D = 0.25 to equation (3.6), maximum power can be calculated. Equation for P_{max} is then

$$P_{max} = \frac{U_{pri} n U_{sec}}{8 f_s L_{lk}}. \qquad (3.7)$$

SPS control is attractive, because of its simplicity, but it has one major problem. According to Kheraluwala (1992), soft switching can be achieved for the whole power range only when $U_{\text{pri}} = n \cdot U_{\text{sec}}$ in the ideal circuit and the situation is even worse when parasitic output capacitance C_{oss} of the transistors are taken in to account. Considering also the magnetising inductance of the transformer widens the soft switching region (Kheraluwala et al. 1992), but this inductance is so big compared to the leakage inductance in typical transformer design that it is usually neglected.

As described by Everts et al. (2013), low-loss zero voltage turn-off for example with T1 and T4 can be achieved if drain-to-source current flow $i_{\text{ds,T1/T4}}$ can be stopped before $C_{\text{oss,T1/T4}}$ is charged to a significant voltage level. Zero voltage turn-on is achieved if energy stored in the leakage inductance L_{lk} is big enough at the moment when T1 and T4 turns off that it is able to fully discharge capacitance $C_{\text{oss,T2}}$ and $C_{\text{oss,T3}}$ before T2 and T3 turns on. In order to avoid so called back commutation, this discharging should be done during the required dead time T_{dead}, which is preventing destructive current shoot-through in the switching leg. (Everts et al. 2013)

Parasitic C_{oss} capacitances change with voltage highly nonlinearly and average charge must be calculated from datasheet information of the device if accurate soft switching boundaries are needed (Kasper et al. 2016). However, rough estimation of the soft switching region can be calculated by ignoring these capacitances. Calculation of initial parameters and component selection are done using this simplification in the design chapter 4.

Simplified soft switching boundaries for primary and secondary side can be calculated by finding the voltage operation points for every power level where inductor current changes direction at primary and secondary side switching moments. Due to half-cycle symmetry of current i_{lk}, only two points of time needs to be analysed – initial current at time $t = 0$ and current after phase-shift period $t = T_{\varphi}$. Primary side boundary can be solved by first inserting equation (3.5) to (3.4) and rearranging phase-shift D from $i_{\text{lk}}(t{=}0) = 0$, which leads to equation

$$D_{pri} = \frac{U_{\text{pri}} - nU_{\text{sec}}}{4U_{\text{pri}}}. \tag{3.8}$$

and inserting this to the power equation (3.6). Secondary side boundary can be calculated in a same manner by solving D from $i_{\text{lk}}(t=T_\varphi) = 0$. Phase-shift equation for secondary side is

$$D_{sec} = \frac{nU_{\text{sec}} - U_{\text{pri}}}{4nU_{\text{sec}}}, \tag{3.9}$$

Soft switching region for the designed converter is plotted in the chapter 4.3.

3.2.2 Advanced modulation methods

The soft switching region is quite narrow, especially at low power levels, when SPS control is used. Fortunately, there are at least three parameters commonly used in addition to the phase shift D, which can be used to grow this region with a cost of increased complexity. These parameters are the primary and secondary side PWM duty cycles and the switching frequency f_{s}.

Ignoring the dead time between both transistors in a switching leg, primary and secondary side bridges are modulating square wave with 50 % duty cycle in the SPS control. This duty cycle can be decreased by adding phase shift between switching legs inside the bridge, which will effectively step down the RMS value of the voltage $u_{\text{pri/sec}}$. A big difference in the ratio of primary and secondary side voltages drives transistors of the DAB to hard switching and causes significant amount of circulating currents to flow inside the converter. Stepping down the voltage reduces this difference and therefore increases soft switching region and lowers losses caused by the circulating currents. Examples of this kind of control methods are presented for instance by Vangen et al. (1991), Oggier et al. (2006) and Bai et al. (2008).

Other option, which is especially useful in a half-bridge variant of the DAB where PWM modulation control can't be done, is controlling the switching frequency f_s (Hiltunen et al. 2015), which is called variable frequency modulation (VFM). It is virtually the same as changing inductance L_{lk} dynamically, which can be seen from the power equation (3.6). Increasing the switching frequency will reduce the maximum achievable power of the

converter, but it also extends the soft switching region and this behaviour can be used to achieve soft switching at low power levels. Higher switching frequency means higher switching losses and conduction losses due to the proximity and skin effects and therefore it must be studied for each case if the benefits are still greater than driving converter to hard switching. The variable frequency modulation is used for instance by Guidi et al. (2010), He et al. (2014) and Hiltunen et al. (2015).

4 MAIN CIRCUIT DESIGN

There are endless ways to theoretically optimize each parameter of the converter to achieve the highest possible efficiency and lowest component stresses, but in the fast-paced product development it is often too slow and unnecessary. The main goal of the following design procedure is to keep the design simple and practical by minimizing variables to be optimized and selecting initial components in such way that they can be easily changed if necessary.

The most important design parameter of the DAB is the leakage inductance L_{lk}. Estimate of the needed inductance can be calculated using the ideal circuit model presented in the previous chapter, after turns ratio n and switching frequency f_s are defined. Amount of leakage inductance defines the maximum achievable power and size of the soft switching region. Selecting the L_{lk} is a balancing act between these two – high inductance value allows maximum power at every voltage, but it leads to a narrow soft switching region and vice versa. The switching frequency has a same effect, but it can't be often changed freely due to component restrictions and EMI emission test limits.

When the leakage inductance is known, maximum transistor peak and RMS currents can be estimated based on ideal inductor current waveforms. This information is then used to find suitable commercial transistors, which have sufficient voltage, peak current, and RMS current ratings.

After the parameters of the DAB are known, the EMI filters can be designed. Simplified filter design is presented in the chapter 5.

4.1 Turns ratio

The ratio between number of turns in the primary side winding and the secondary side winding of the transformer is called turns ratio. It defines the voltage conversion ratio of the transformer and it can have very significant effect on Dual Active Bridge's efficiency if selected incorrectly. Widest soft switching region in terms of output power is achieved when primary side voltage and secondary side voltage referred to primary side are the same (Kheraluwala et al. 1992). Turns ratio should usually be selected in such way that the

converter is operating at this point when input and output voltages are at their nominal values, because most of the energy is most probably transferred at these voltage levels.

Turns ratio can be calculated based on the requirements defined in chapter 2. If nominal BESS side voltage $U_{BESS,N}$ is at the primary side of the transformer and nominal PV side voltage $U_{PV,N}$ is at the secondary side, turns ratio n is

$$n = \frac{U_{pri,N}}{U_{sec,N}} = \frac{U_{PV,N}}{U_{BESS,N}} = \frac{600\ V}{400\ V} = 1.5. \tag{4.1}$$

Existence of a transformer in the DAB converter makes it very flexible topology in terms of voltages, because transformer with a different turns ratio can be swapped in place of existing one without major changes in the rest of the design. This could be the case if nominal voltage in practice is not what it was estimated to be and converter is working in non-ideal operating point most of the time.

4.2 Switching frequency

In SPS control, transistors of the both H-bridges are switched with a symmetric 50% duty cycle at the switching frequency f_s. This frequency has as big effect on achievable power as the leakage inductance, which can be seen by analysing power equation (3.6). Using low frequency leads to physically large magnetic components, such as transformer and EMI filters. Using higher frequency leads to, for example, increased AC resistance due to skin and proximity effects. Switching losses are minimal, because of the soft switching.

Single installer should be able to install the converter, which means that weight must be minimized and therefore high frequency is preferable. The measurement range of the conducted electromagnetic interference defined by the European standard EN 55022 (CENELEC 2010) begins from the 150 kHz, which must be considered carefully especially if the high-magnitude second harmonic of the switching frequency is in this range. The reason why second harmonic is the most significant component in the current ripple can be seen later in the chapter 4.6 in figure 4.4.

The emission limits are highest at the 150 kHz and the limits go down until 500 kHz is reached. The switching frequency of $f_s = 145$ kHz is chosen for this design, because this way the second harmonic (290 kHz) stays relatively far from the 500 kHz limits and possible ripple current at the switching frequency is out of the measurement range. Details of the EMI standard are discussed more in depth in the chapter 5.

4.3 Leakage Inductance

Now there is only single parameter – leakage inductance L_{lk} – to be determined before ideal circuit can be solved. One way to find a suitable level of inductance is to find a value where converter can achieve the certain power level at every voltage operation point. This minimum power should be higher than nominal output power P_N to take account unidealities like phase drift phenomenon introduced by Xie et al. (2010) and power loss from input to output in general. Using 1/3 margin, minimum maximum power P_{max} is defined as

$$P_{max} = \frac{4}{3}P_N. \tag{4.2}$$

Solving inductance L_{lk} from maximum power equation (3.7) using lowest voltage for primary ($U_{PV,min}$) and secondary side ($U_{BESS,min}$) and power P_{max} gives a value of $L_{lk} \approx 8.73$ µH. Current waveforms can be now plotted using equations (3.1), (3.2) and (3.3). Waveform at nominal voltages and power of P_{max} is presented in figure 4.1.
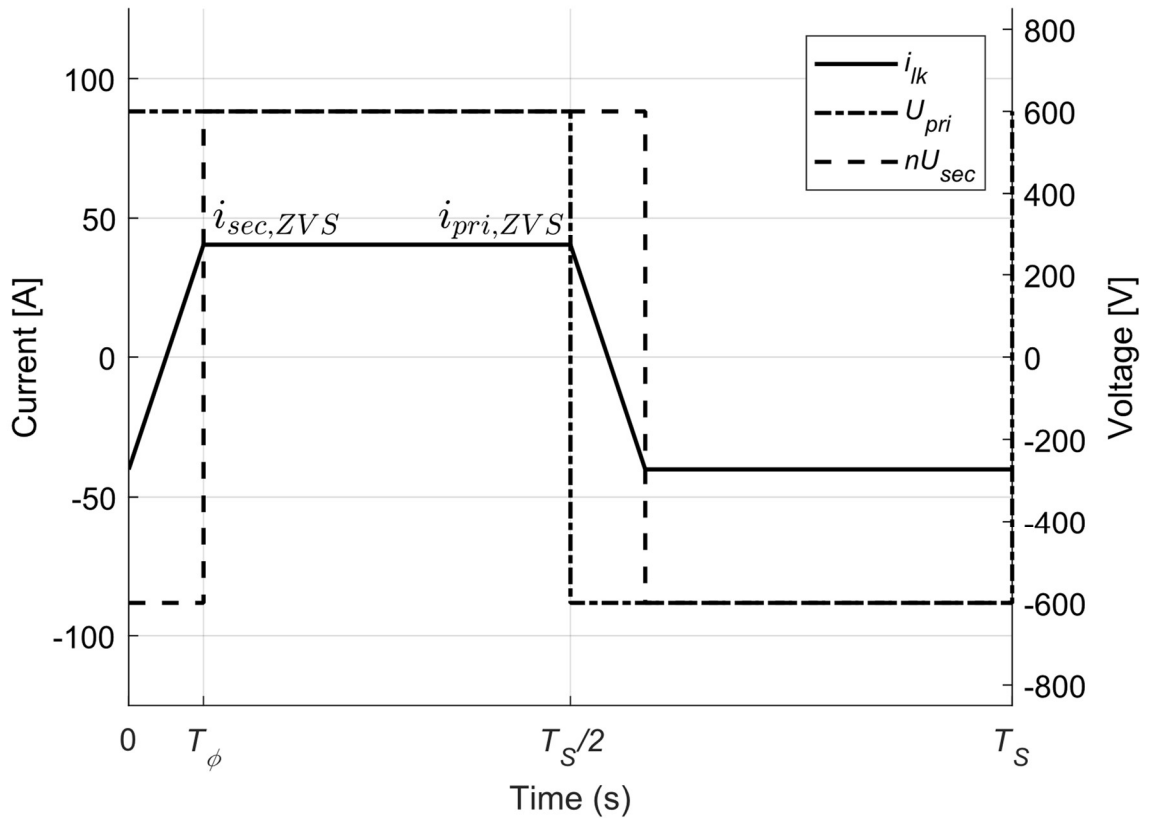
Figure 4.1. Current through leakage inductance when primary and secondary side voltages are at their nominal values and power is 20 kW. Current $i_{pri,ZVS}$ is the current when primary side transistors switches and $i_{sec,ZVS}$ is the current when secondary side transistors switches.

The current waveform with a maximum voltage difference between primary and secondary side is presented in figure 4.2. When the secondary side transistors are switched on, the current $i_{sec,ZVS}$ at the switching instant has not changed direction like in the nominal case in the figure 4.1, which means that the operation point is out of the soft switching region. As was discussed in the chapter 3.2.1, the soft turn-on requires current flow through a transistor to be at least zero in the ideal case and more than zero to the opposite direction when output capacitors of the unideal transistors must be discharged. This change of current flow direction clamps the drain-source voltage to near zero and therefore zero-voltage switching can be achieved.
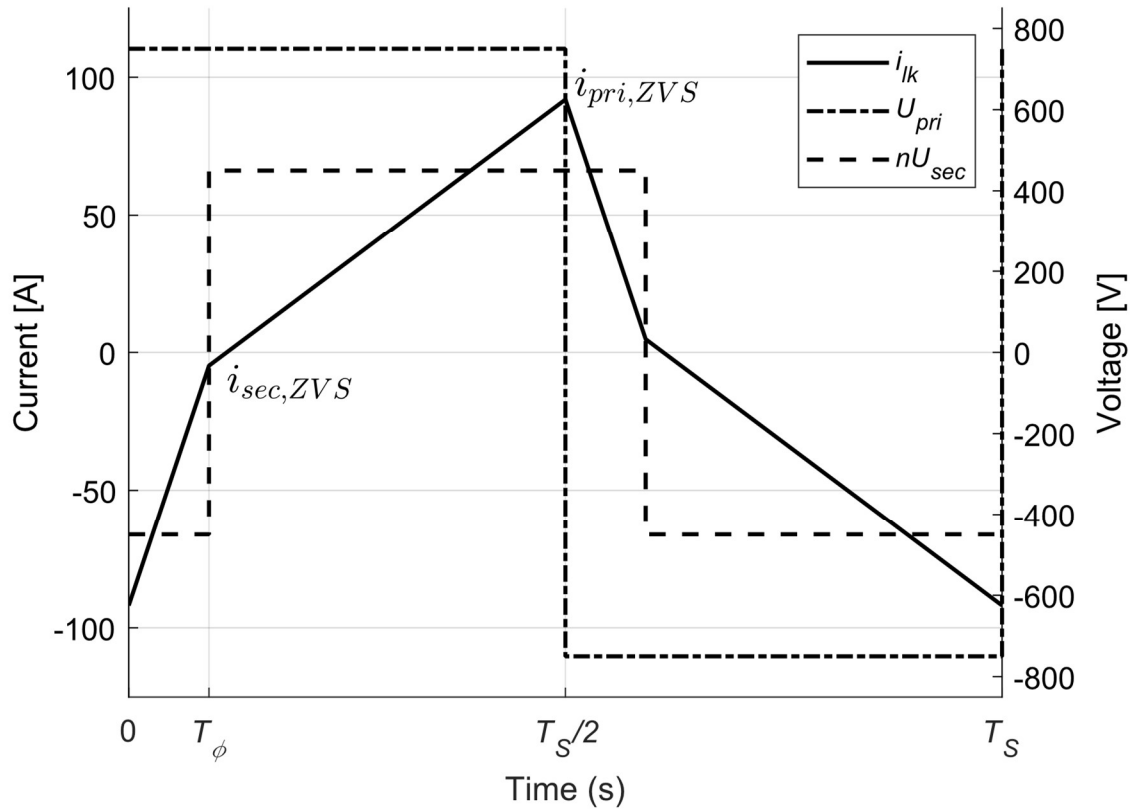
Figure 4.2. Current through leakage inductance when secondary voltage is at its minimum value and primary voltage at its maximum. Power is 20 kW. Current $i_{pri,ZVS}$ is the current when primary side transistors switches and $i_{sec,ZVS}$ is the current when secondary side transistors switches.

Soft switching region for the whole power range can be calculated as described in the chapter 3.2.1. This region is presented in figure 4.3 as a function of power P and voltage ratio d, which is defined as

$$d = \frac{U_1}{nU_2}. \tag{4.3}$$

It shows that if inductance is sized this way, the high efficiency area will be very narrow at lower power levels. Taking the capacitance into account will make the region even smaller.
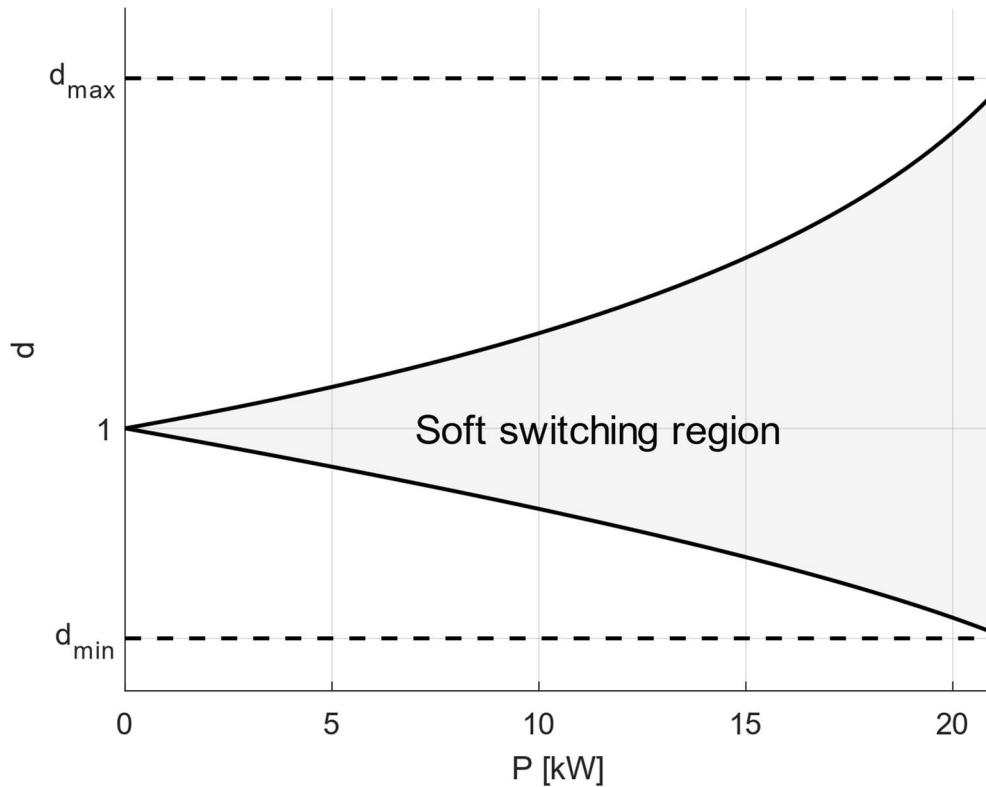
Figure 4.3. Soft switching region calculated with a leakage inductance value at which the converter can achieve required power level at any voltage. Minimum voltage ratio d_{min} is 0.6 and maximum ratio d_{max} is 1.67.

This leakage inductance value is used for initial component selection at this point of design. The inductance value, switching frequency or modulation method can be changed in the prototyping phase if soft switching region needs to be adjusted. More precise estimation would of course allow selecting transistors and other components with smaller safety margins, but if components are selected wisely, the electrical values of the circuit can be changed in some extent without big and expensive chances to the prototype.

4.4 Maximum peak current

Maximum current peaks $i_{pri,max}$ for primary side and $i_{sec,max}$ for secondary side can be found when the voltage ratio d is at its end points. Values for these currents can be calculated using the same equations (3.1)–(3.4), but following equation for primary side peak current derived by Zhao et al. (2014b) can be used instead

$$i_{\text{pri,max}} =$$

$$
max \begin{cases} \dfrac{nU_{\text{sec,max}} - U_{\text{pri,min}}\sqrt{1 - \dfrac{8P_{\text{max}}f_s L_{\text{lk}}}{nU_{\text{sec,max}}U_{\text{sec,min}}}}}{4f_s L_{lk}}, d < 1 \\[4ex] \dfrac{U_{\text{pri,max}} - nU_{\text{sec,min}}\sqrt{1 - \dfrac{8P_{\text{max}}f_s L_{\text{lk}}}{nU_{\text{sec,min}}U_{\text{pri,max}}}}}{4f_s L_{lk}}, d \geq 1 \end{cases} . \tag{4.4}
$$

Secondary side current can be calculated using equation

$$i_{\text{sec,max}} = ni_{\text{pri,max}}. \tag{4.5}$$

Peak current at the primary side is $i_{\text{pri,max}} = 92$ A and at the secondary side $i_{\text{sec,max}} = n \cdot i_{\text{pri,max}} = 138$ A.

4.5 RMS current

Estimation of the maximum inductor RMS currents $i_{\text{pri,RMS}}$ and $i_{\text{sec,RMS}}$ are also needed for transistor selection. Zhao et al. (2014b) introduced following equation for the primary side current when voltage ratio d is 1

$$i_{\text{pri,RMS}} = \frac{\sqrt{3}}{12f_s L_{\text{lk}}} \cdot$$
$$\sqrt{2U_{\text{pri,min}}^2 - (2U_{\text{pri,min}}^2 + 8P_{\text{max}}f_s L_{\text{lk}})\sqrt{1 - \frac{8P_{\text{max}}f_s L_{\text{lk}}}{U_{\text{pri,min}}^2}}} \tag{4.6}$$

and for primary side

$$i_{\text{sec,RMS}} = ni_{\text{pri,RMS}}. \tag{4.7}$$

The RMS current for primary side is $i_{\text{pri,RMS}} = 73$ A and for secondary side $i_{\text{sec,RMS}} = 109$ A.

4.6 Transistors

Selecting correct semiconductor switches is an important task when lifetime of the converter is considered. In practice, this means that rated values of the transistors should not be exceeded and should preferably have some margin.

Rated peak current can be directly defined as the peak current $i_{lk,max}$ of the inductor. It involves 1/3 margin added to the nominal power P_N, which should be enough. Worst case current waveforms for the diagonal transistor pairs T1-T4 and T2-T3 for PV side are presented in figure 4.4.
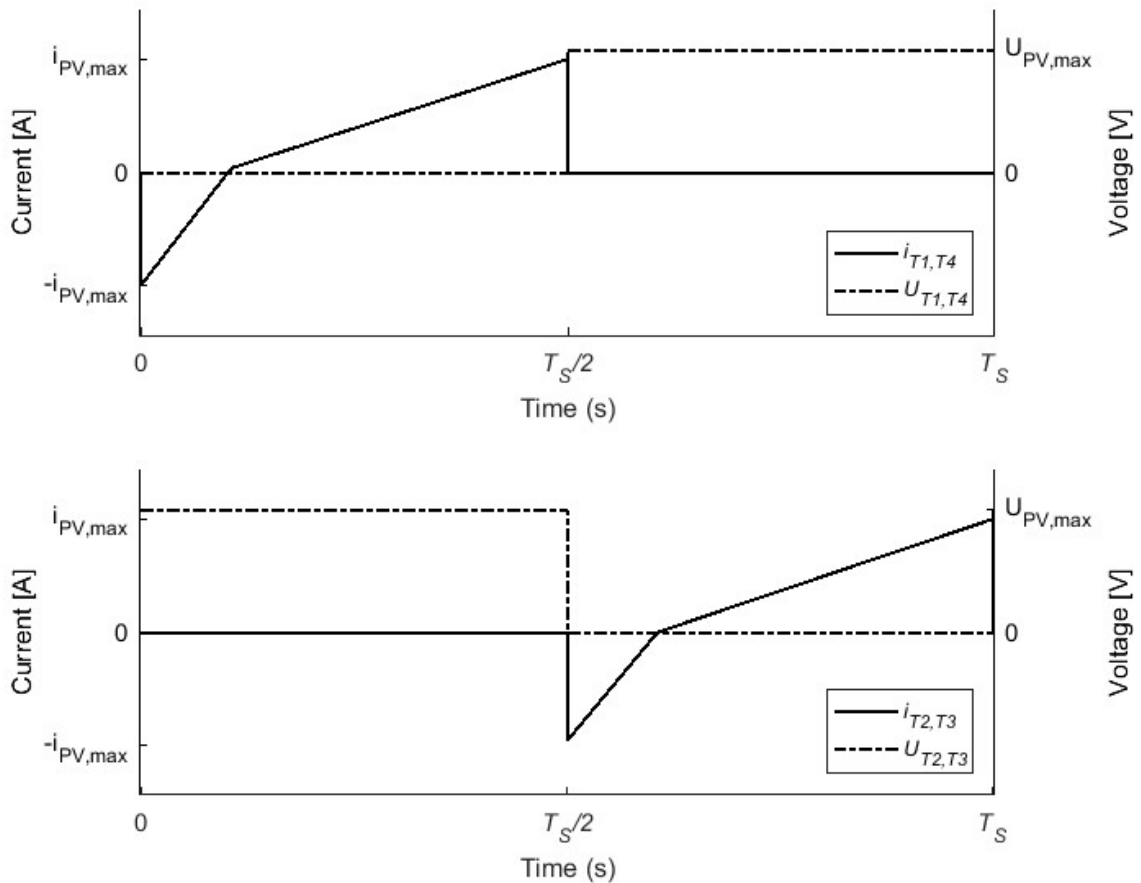
Figure 4.4. Worst case peak current and voltage waveforms running through PV side transistors.

Each transistor is conducting half of the switching period, which means that only half of the inductor RMS current is flowing through these devices. RMS current has also 1/3 margin, but the problem is that maximum allowed current of the MOSFET depends heavily on the junction temperature T_j. Estimating T_j accurately at this point is challenging without knowing

anything about the cooling system to be used. Maximum rated currents are usually presented at two case temperatures $T_c = 25°C$ and $T_c = 100°C$. Temperature of the case will be somewhere between these two values, so using the higher temperature value for the rated current is a safe and easy option.

The internal capacitances of the MOSFET transistor and stray inductances of the circuit attached to it forms a resonant circuit, which can cause harmful voltage spikes. Wide margin of around 50–100 % should be used to prevent exceeding maximum breakdown voltage of the semiconductor switches. Minimum margin of 50 % is selected for this design, because wider margin causes problems with availability and price of the components especially at the PV side where maximum rated voltage is 750 volts. Minimum rated voltage for transistors at the PV side is then $U_{ds,PV} = 1.5 \cdot U_{PV,max} \approx 1100$ V and at the BESS side $U_{ds,BESS} = 1.5 \cdot U_{BESS,max} = 750$ V. Minimum rated values for the transistors are summarized in the following table.

Table 4.1. Minimum values for primary and secondary side voltage, RMS current and peak current.

Value	Primary (PV)	Secondary (BESS)
Min. drain to source voltage U_{ds}	1100 V	750 V
Min. drain to source RMS current ($T_c = 100°C$) i_{ds}	36 A	54 A
Min. rated peak current $i_{ds,pulse}$	92 A	138 A

These values are only used for initial selection of the components and ratings can be lowered if measurements done with the prototype shows that components are oversized. Important thing is to select components with a common package, like TO-247, to be able to change transistors with different ratings without changes to printed circuit board.

Required high switching frequency, high voltage and high current ratings makes SiC MOSFET the most attractive option for this application. Availability of low-cost silicon (Si) MOSFETs is poor at these voltage and power levels and silicon IGBT transistors are slow and therefore can't be switched at 145 kHz without significant switching losses. Cost of the

IGBT transistors is a lot less than SiC MOSFETs', but implementing IGBTs would require at least following changes compared to a design with SiC transistors, which compensates the cost difference:

1. IGBT transistors typically have a long current tail at turn-off and minimal internal output capacitance, which means that big external snubber capacitors must be added to keep turn-off losses low.

2. Switching frequency must be lowered, which increases size of the transformer and EMI filters.

3. Cooling must be more powerful, because of the increased switching losses due to slow transitions and possibly higher on-state losses.

SiC MOSFET from ROHM Semiconductor with a model name SCT3040KLGC11 is selected for the primary side, because it fulfils the requirements. For example, following variations presented in the table 4.2 with drain to source voltage U_{ds} = 1200 V are available from ROHM, if changes need to be made in prototyping phase

Table 4.2. SiC MOSFETs with different current ratings and same voltage rating and package. Output capacitance C_{oss} affecting soft switching region and on-state resistance $R_{ds,on}$ are also presented.

Model	Package	U_{ds} [V]	i_{ds} [A] (T_c=100°C)	$i_{ds,pulse}$ [A]	C_{oss} [pF]	$R_{ds,on}$ [mΩ] (T_j=125°C)
SCT3080 KLGC11	TO-247	1200	22	77	75	120
SCT2080 KEC	TO-247	1200	28	80	77	125
SCT3040 KLGC11	TO-247	1200	39	137	76	60
SCT3030 KLGC11	TO-247	1200	51	180	180	45

Availability of MOSFETs with such a high voltage and RMS current ratings are very limited, so two parallel transistors must be used to double the current capability. The same ROHM transistors are selected for the secondary side, which were selected for the primary side.

Combined rated RMS current is $i_{ds} = 2 \cdot 39$ A $= 78$ A, which is much more than required value $i_{ds} = 49$ A and voltage rating is more than required $U_{ds} = 750$ V, but price difference to SCT2080KEC is so marginal that possibility to use only one type of transistor in the prototype justifies the decision. If optimized prototype will end up in production, using similar MOSFETs at both sides of the converter, might lead to additional cost savings due to economies of scale in purchasing and assembly.

Now all necessary values for the main circuit of the DAB are calculated and transistors are selected. Transformer must be often custom made for each application, like in this design, and amount of leakage inductance in the transformer must be known before the external inductor can be selected, which is why selection of these components will not be presented in this thesis. The EMI filters will be designed next.

5 EMI FILTER DESIGN

Commercially sold devices must not interfere other devices with electromagnetic interference (EMI) or be affected by them as will be discussed more in depth later in this chapter. The DAB converter has a high ripple currents at both sides of the converter, which means strong conductive emissions. The EMI filters should be part of every DAB design, which is why an example filter topology and component selection is presented in this thesis. However, the topic is quite complex so keeping the main focus of the thesis in the DAB design requires that only one basic topology can be introduced, which is suitable for most applications. This presented topology might not be enough for the example application due to very high ripple currents. The final filter design requires standardised measurements of the converter, which are introduced next.

5.1 Introduction

Manufacturers placing products on the market inside the European Economic Area are responsible for checking that their products meet European Union's (EU) safety, health, and environmental protection requirements. In practice, this is done by identifying the applicable directives and harmonised standards, verifying product specific requirements, identify whether an independent conformity assessment is necessary, test the product and check its conformity, draw up and keep available the required technical documentation and finally affix the CE marking and draw up the EU Declaration of Conformity. (European Commission 2017a)

Designed DC-DC converter falls under EMC Directive 2014/30/EU, which is intended to ensure that equipment liable to generate or to be affected by electromagnetic disturbance can be used in the electromagnetic environment for which it has been designed without causing disturbances to other equipment or being affected by them (European Commission 2017a).

Annex I of directive 2014/30/EU defines following essential requirements:

- The electromagnetic disturbance generated does not exceed the level above which radio and telecommunications equipment or other equipment cannot operate as intended.

- It has a level of immunity to the electromagnetic disturbance to be expected in its intended use which allows it to operate without unacceptable degradation of its intended use.

(Official Journal of the European Union 2014)

There is no EU's harmonized standard defining allowed levels of generated electromagnetic disturbances for DC-DC converters. Instead, old standard for information technology equipment EN 55022, which is based on International Electrotechnical Commission's (IET) CISPR 22 standard, is usually applied (Absopulse Electronics LTD, XP Power, Powernet 2016). EN 55022 was replaced by a new harmonized standard for multimedia equipment EN 55032 on 5th of March 2017. This new standard did not change the test requirements defined in EN 55022 (TDK-Lambda 2017).

The testing method for conducted emission is defined in standard CISPR 16. Measurement is done using 50 Ω Line Impedance Stabilization Network (LISN) and spectrum analyser. EN 55022 divides devices in two categories, class A and class B, which have different limits for allowed interference. Class B devices are intended for domestic environments where the use of broadcast radio and television receivers may be expected within 10 meters of the apparatus. Class A category includes all other devices which satisfies the class A limits but not the class B limits. Warning text about possible radio interference must be included in the instructions of the class A device. (CENELEC 2010)

Manufacturer determines the class of the device and must be able to proof that the requirements are fulfilled if problems occur. Designed converter will be mainly installed in places like garages and HVAC plant rooms where radio interference can't be expected to be a problem so class A limits for conducted emissions presented in the table 5.1 are probably adequate. Conducted emissions are measured using quasi-peak detection and averaging.

Table 5.1. Limits for Conducted disturbance for class A device. (CENELEC 2010)

Frequency range MHz	Limits [dB(µV)]	
	Quasi-peak	Average
0.15 to 0.50	79	66
0.50 to 30	73	60

Measurements can be made by the manufacturer using the guidelines presented in the standard EN 55022 and other related standards, but it is preferable to let a notified body to carry out the tests or use it for consultation. The notified body is an organisation designated by an EU country to carry out tasks related to conformity assessment procedures set out in the applicable legislation (European Commission 2017b).

5.2 Filter topology

To meet the requirements for conducted emissions, low pass filters must be used to attenuate the high frequency harmonics. Commonly used filter for this purpose is a LC-filter, which consist of a series inductor and a parallel shunt capacitor (figure 5.1). This topology is power efficient because it does not have other resistive elements than small Equivalent Series Resistances (ESR) of the inductors and capacitors.
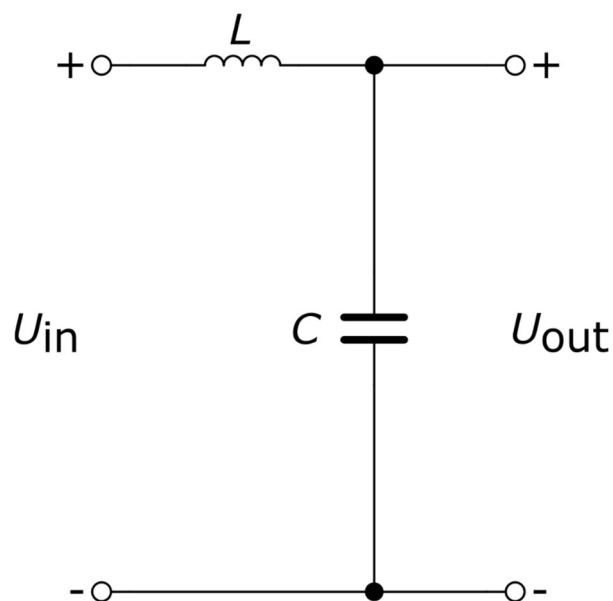

Figure 5.1. Schematic of a LC-filter.

Transfer function L(s) of the filter is

$$L(s) = \frac{U_{out}(s)}{U_{in}(s)} = \frac{Z_{out}(s)}{Z_{in}(s)} = \frac{\frac{1}{sC}}{Ls + \frac{1}{sC}} = \frac{1}{LCs^2 + 1}, \qquad (5.1)$$

where s is a Laplace variable, C is the amount of capacitance, U_{out} is the output voltage and U_{in} is the input voltage of the filter.

Connecting inductor and capacitor virtually in series forms resonant circuit, which tends to drive gain of the filter towards infinity in ideal circuit at resonant frequency

$$f_o = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}}, \qquad (5.2)$$

where f_0 is the resonance frequency and ω_0 is angular resonance frequency. Because of this, the filter needs additional damping components which are presented later in this chapter. Sizing of the filter is started from the capacitor.

5.3 Capacitors

In the case of ideal LC low-pass filter, the current of the converter would be perfect DC current without any ripple and all the AC currents inside the converter would be taken from the filter capacitors. This simplification can be used to estimate the required capacitance for the filters to keep the voltage ripple at certain level by assuming that all the current flowing through for example at the PV side is taken from the filter capacitor C_{PV} during single switching period $T_s = 1/f_s = 6.9$ μs. In reality, just the AC ripple current is flowing through the capacitor and therefore this estimation does add some margin to the design.

Smooth DC voltage should be maintained at the input of the converter to give the feedback controller a stable voltage reference. In this design, voltage ripple of 1 % is allowed, which corresponds to a voltage change $dU_{r,PV} = 0.01 \cdot U_{PV,min} = 0.45$ V at the PV side and $dU_{r,BESS} = 0.01 \cdot U_{BESS,min} = 0.30$ V at the BESS side. Minimum voltage values are used,

because allowed voltage ripple dU_r is smallest and current flowing through the capacitor is highest at this point, which means that the amount of required capacitance is biggest at these conditions.

The DC currents I_{PV} and I_{BESS} should be calculated next in the operation conditions where the voltages are at the minimum values $U_{PV,min}$ and $U_{BESS,min}$ and power is at the maximum value $P_{max} = 20$ kW. The PV side current is $I_{PV,max} = P_{max} / U_{PV,min} = 67$ A and BESS side current is $I_{BESS,max} = 44$ A. Now capacitances C_{PV} and C_{BESS} can be solved using following equation

$$C = \frac{dq}{dU} = \frac{It}{dU}, \tag{5.3}$$

where dq is the change of charge during voltage change dU, which is the same as the voltage ripple $dU_{r,PV}$ or $dU_{r,BESS}$ in this case. Time t corresponds to the switching time T_s and current I is PV side current $I_{PV,max}$ or BESS side current $I_{BESS,max}$. Therefore, capacitance C_{PV} is 68 µF and C_{BESS} is 153 µF.

The PCB traces between the transistors of the bridge and filtering capacitors should be as short as possible to minimize ringing caused by a parasitic inductance. Multi-Layer Ceramic Capacitors (MLCC) are physically small components and can be therefore placed close to the transistors, which is why they are often used in the filtering circuits. However, maximum capacitance of single reasonably priced ceramic capacitor is often low for applications like the DAB converter, which is why additional electrolytic or film capacitors are added to fulfil the capacitance requirements.

The capacitance value of MLCCs used in these kind of filtering circuits change significantly as a function of temperature and DC voltage (ROHM 2013). This behaviour supports the idea of not using only this kind of ceramic capacitors in the filtering circuit, because performance of the filter would change significantly when DC voltage or power of the converter changes. Electrolytic and film capacitors have much more stable behaviour, which

is why a design rule used for this converter is that 1–5 % of the total capacitance is from MLCC and the rest is from the film capacitors. Film capacitors are more expensive than electrolytic and have relatively lower capacitance, but they are more stable and reliable and have better ripple current ratings, higher voltage ratings and lower ESR (Wang 2014), which is why they are more suitable for this application with long expected life time.

The currents $I_{PV,max}$ and $I_{BESS,max}$ can be used as a minimum rated RMS current value for the capacitors, because it already includes safety margin from the margin added to the nominal power P_N and margin from not removing the DC current from the current flowing through the capacitors. Same goes for the peak current when transistor's peak currents $i_{PV,max}$ and $i_{BESS,max}$ are used. Voltage ratings can be the same as was used with the transistors in chapter 4.6. Frequency of the current affects the impedance of the capacitor, which is why it must be also defined. As can be seen from figure 4.4, the ripple frequency with highest magnitude is clearly two times the switching frequency f_s. Nominal ripple frequency f_r is therefore 290 kHz.

Because relative amount of MLCCs is kept low in this design, a detailed information of the behaviour of capacitance as a function of temperature and voltage is not necessarily needed. The capacitance value can be a lot lower than the nominal, which is why 50% of the nominal value is used as a design value. These characteristics of the MLCCs are discussed more in depth by Prymak et al. (2008).

Current ratings are usually not given for the MLCC components and only thing limiting the current is temperature limits (Tse 2006). Temperature of these capacitors must be measured from the prototype to ensure that it stays under the maximum limit. Film capacitors do have a current limit and current flowing through these components must be estimated by calculating it using the impedance of the capacitors. Impedance Z for each component is calculated based on the ESR and capacitance values using equation

$$Z = \sqrt{\left(\frac{1}{2\pi f_r C}\right)^2 + ESR^2}. \qquad (5.4)$$

Ripple current flowing through each capacitor is calculated by first solving voltage over the whole primary and secondary side capacitor banks using total impedance of the parallel capacitors and RMS currents $I_{PV,max}$ and $I_{BESS,max}$. The current flowing through a single capacitor can be then calculated using the impedance of the capacitor and this voltage.

Following table summarizes the design values for selecting the capacitors.

Table 5.2. Design values for selecting capacitors.

Value	Primary side (PV)	Secondary side (BESS)
Capacitance	68 µF (MLCC 0.68–3.4 µF, Film 64.6–67.3 µF)	153 µF (MLCC 1.53–7.65 µF, Film 145.4–151.5 µF)
Minimum total RMS current	44 A	67 A
Minimum peak current	92 A	138 A
Minimum rated voltage	1100 V	750 V
Nominal voltage	600 V	400 V
Nominal ripple frequency	290 kHz	290 kHz

Number of ceramic capacitor models at the PV side voltage level is limited and prices are high. Placing two capacitors in series would be a good option in terms of availability, price and capacitance, because voltage rating could be halved, but required footprint area increases significantly. Power density is prioritised in this design and only single capacitor will be placed in series at both sides of the converter.

Flexibility for optimisation is created with the film capacitors, which are selected in such way that there are multiple known options fitting the same footprint. For example, manufacturer Kemet provides three capacitance options with a same footprint for the PV side of the converter; 20 µF, 25 µF and 27 µF (Kemet 2017). Placing three of the 20 µF capacitors in parallel gives 60 µF of total capacitance, which is close to the required 64.6 – 67.3 µF, but current is over the rated value and therefore fourth capacitor must be added. Capacitance can be then changed in a range of 80 – 108 µF and by removing one capacitor the range is 60–81 µF, if current is not too high. It would be preferable to be able to go lower in capacitance, but product series with wider range using the same footprint and suitable current rating could not be found.

Same goes for the BESS side of the converter, where Kemet provides two film capacitors with high enough current rating, which are 30µF and 40µF versions (Kemet 2017). Five of the 30µF capacitors must be connected to parallel to have a 150 µF of total capacitance and ripple current below the rated value. Capacitance range with five capacitors is then 150 – 200µF and with four capacitors 120 – 160 µF.

The selected components and key characteristics are presented in the table 5.3.

Table 5.3. Selected capacitors for primary and secondary side and the most important characteristics.

	Primary side (PV)		Secondary side (BESS)	
	MLCC	Film	MLCC	Film
Manufacturer	Knowles Syfer	Kemet	Knowles Syfer	Kemet
Part number	2220Y1K5015 4KXTWS2	C4AEQBW52 00A3MJ	2220Y1K0047 4KXRWS2	C4AEOBW53 00A3MJ
Capacitance	0.075 µF (50%)	20 µF	0.24 µF (50%)	30 µF
Quantity	10	4	7	5
Total Capacitance	0.75 µF	80 µF	1.7 µF	150 µF
Rated voltage	1500 V	1100 V	1000 V	900 V
Rated RMS current	-	13 A	-	15 A
ESR	0.09 Ω	0.007 Ω	0.03 Ω	0.005 Ω
Impedance	3.7 Ω	0.03 Ω	1.2 Ω	0.01 Ω
Ripple Current	0.05 A	11 A	0.15 A	13 A
Dissipated Power	0.1 mW	800 mW	0.7 mW	900 mW

5.4 DC Inductors

The LC filter should have adequate attenuation A at the EMI measurement range which starts from 150 kHz. The amount of attenuation needed could be roughly estimated by simulating the DAB circuit connected to the Line Impedance Stabilization Network, but without taking account all the non-idealities of the converter, it will most probably be far from reality. Most efficient approach is to just select some high attenuation value like for example A = -80 dB which corresponds to ratio of 1:10000 and optimize the filters based on prototype measurements. The damping circuit mentioned before will reduce the amount of attenuation, which must be also considered when selecting the initial value.

Required amount of inductance can be now solved from the transfer function (5.1) by first adding the attenuation and replacing Laplace variable with $s = j(2{\cdot}\pi{\cdot}f)$

$$|L(s)| = \left|\frac{1}{LCs^2 + 1}\right| = \left|\frac{1}{LC(j2\pi f)^2 + 1}\right| = A. \tag{5.5}$$

Rearranging this function leads to

$$L = \left|\frac{1 - A}{-AC4\pi^2 f^2}\right|, \tag{5.6}$$

Inserting attenuation of A = 1/10000, total capacitance for each side C_{PV} = 80.75 μF and C_{BESS} = 151.7 μF and the frequency f = 150 kHz gives inductance value of L_{PV} = 140 μH for PV side and L_{BESS} = 74 μH for BESS side.

These inductance values are very high for the required current ratings, which means that inductors must be most probably custom made and will be big and expensive. There are a few ways to solve this problem. First option is to lower the attenuation A to -60 dB, but the damping circuit will reduce it even lower, which might not be enough to pass the EMI requirements. Second option is to increase amount of capacitance, but number of big film capacitors is already high and decreasing power density further is not preferable. Third option is to use higher order filtering circuit, which would decrease the power density, but could be otherwise viable option.

This last option seems to be the most obvious choice, but the first option is first considered, because the flexibility of the DAB converter, high safety margins and analysing the normal operation conditions makes the selection of lower attenuation acceptable. The ripple currents will be lower than the designed values, because the design value for the input power is 25 % more than rated output power and the power loss should be less than this. And if the ripple current is still too high, the modulation method can be changed to more advanced one, which produces lower peak currents at the extremes of the voltage operation points. Other thing which helps to justify the decision is that PV side voltage will be virtually always close to the nominal voltage point when maximum power is flowing through the converter and therefore the magnitude of the peak current will be lower. After all these things are considered and the ripple currents are still too high, the capacitance values of the film capacitors can be increased.

New values for the inductances when the attenuation is $A = 1/1000$ are $L_{PV} = 14$ µH for PV side and $L_{BESS} = 7.4$ µH for BESS side. Even with these values, ready-made commercial components are hard to find. Volume of the inductor should be low enough with these values, but pricing of custom inductors will finally determine if this filter topology is feasible or should for example LCL-filter, also known as pi-filter, be used instead. According to Tarateeraseth (2012) the basic LC-filter provides 40 dB/decade of attenuation and the pi-filter provides 60 dB/decade, which is significantly more.

5.5 Damping

According to Sokal (1973), a feedback regulated converter acts like a negative resistance –
when input voltage increases, input current decreases. This negative input resistance of the
converter connected to insufficiently damped LC filter can lead to oscillation. (Sokal 1973)
Erickson (2010) presented multiple damping topologies for LC filters and their optimal
sizing procedures. The series RL damping topology presented in figure 5.2 is chosen for this
converter, because additional components R_d and L_d do not need to be rated for high currents,
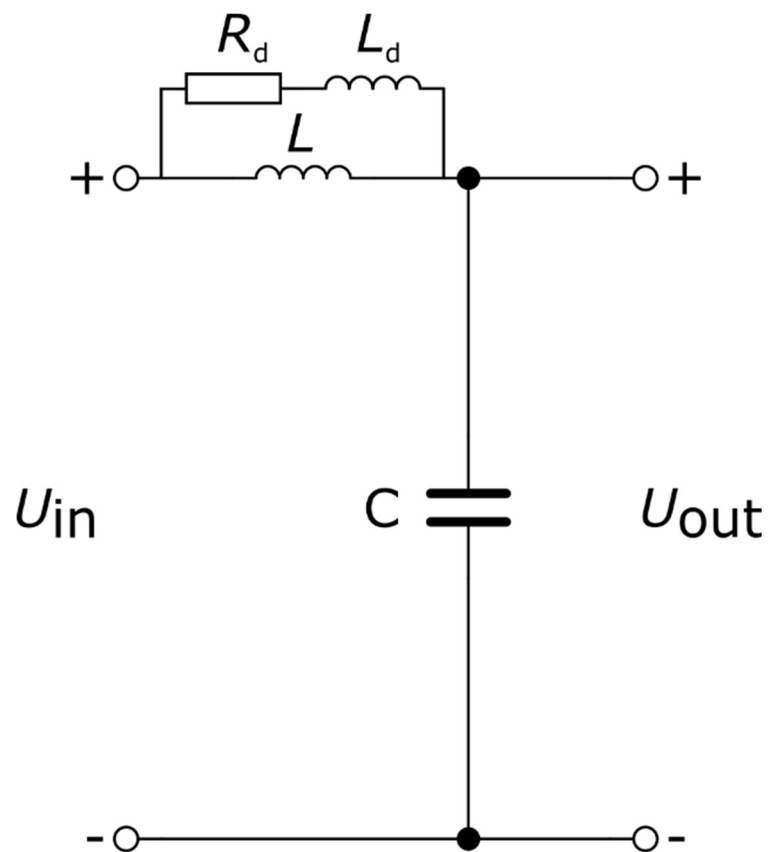which leads to physically compact design.

Figure 5.2. LC filter with damping circuit.

Following the optimization procedure presented in detail by Erickson (2010) with
$n = L_d/L = 0.5$ gives following values for the damping components, when inductor values
$L_{PV} = 14$ µH and $L_{BESS} = 7.4$ µH are used.

Table 5.4. Values for damping inductors and resistors.

	Primary	Secondary
L_d	7.0 μH	3.7 μH
R_d	380 mΩ	200 mΩ

Because the resistance of the damping circuit is much higher than the ESR of the main inductor will be, these values can be rated for low current. Component selection is therefore trivial and will not be presented in this thesis.

Frequency response of the PV side LC-filter with and without damping is presented in the figure 5.3. Attenuation with the damping is around -50 dB.
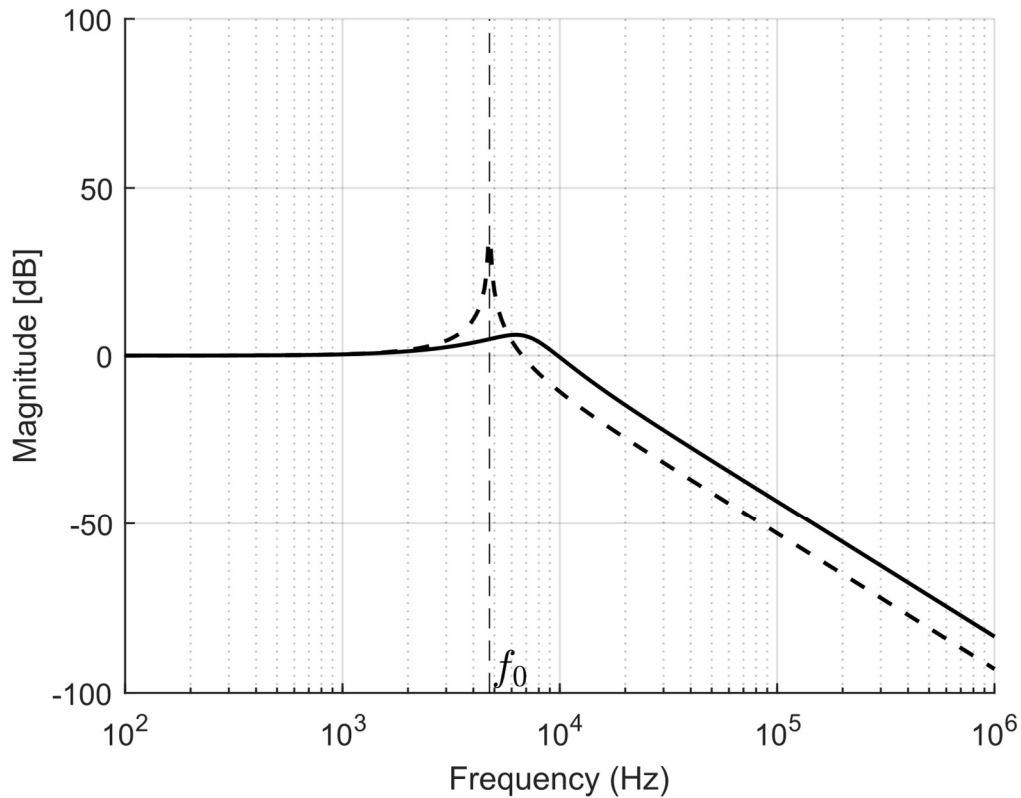

Figure 5.3. Frequency response of the undamped (dotted line) and damped (solid line) LC-filter at the PV side of the converter.

6 DISCUSSION AND CONCLUSIONS

This thesis was an attempt to provide an easy and fast procedure for designing first prototype of the Dual Active Bridge converter including the EMI filters. This topic was selected, because author noticed the lack of publications related to design of the DAB, which could be used directly as a guide in a practical converter design.

The design procedure is based on the ideal model of the converter and therefore generous safety margins must be used to be sure that the prototype will achieve the requirements. The ideal circuit is relatively simple and the related equations have been used since 1990s, which means that the prototype designed by following this thesis will most probably achieve the requirements. Unfortunately, this could not be proven, because the project of which this thesis is a part of was not progressed yet in the prototyping phase at the time when this was written. Results could have been obtained using a simulator, but it would have provided just another rough estimation, because the simulator should be first compared to some real design before it can be fully trusted.

The EMI filter design section was included to the main circuit design, because filtering circuits should be part of every DAB converter. The presented filtering topology can be recommended to be used in DAB converters with maximum power of around 10 kW, because availability of suitable components becomes a problem with high currents as was noticed with the example design. Higher order filter should be used in the designed converter, but to keep main circuit of the DAB as a primary focus of the thesis, other filtering topologies were not discussed.

This thesis can be used as a rough guide for the design, but there is no certainty before the methods are fully tested. Even if these presented methods were tested to be working, some of the important things like for example dead time and requirements for the transformer were discussed only very briefly and the designer should study these topics separately.

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