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Aleksi Mattsson

DESIGN OF CUSTOMER-END CONVERTER SYSTEMS FOR LOW VOLTAGE DC DISTRIBUTION FROM A LIFE CYCLE COST PERSPECTIVE

LUT
Lappeenranta
University of Technology

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Thesis for the degree of Doctor of Science (Technology) to be presented with due permission for public examination and criticism in the Auditorium of the Student Union House at Lappeenranta University of Technology, Lappeenranta, Finland on the 15th of June, 2018, at noon.

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Abstract

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Over the recent years, a lot of effort has been put into improving the efficiency and power density of power electronic converters, and efficiencies exceeding 99% and power densities of 10 W/cm^3 have been reported. While it could be argued that the system cost is also minimized when these two parameters are maximized, the result is often a compromise between the different parameters. High values for either efficiency or power density are often achieved by applying some state of the art technology such as wide bandgap semiconductors, which can potentially increase the cost if the technology is not yet mature for high-volume production. If the system is evaluated based on figures of merit such as power density or weight, the analysis is typically done only for the nominal power of the system as this mainly dictates the design in these two cases. However, in an application such as the low voltage DC system, the load can vary on a large scale, whereas only a small amount of time is spent at or near the nominal point. In such a case a system optimized for power density or weight can potentially lead to a suboptimal result because typically some of the performance at partial load is sacrificed in favor of a higher performance near the nominal point.

In this doctoral dissertation, a life-cycle-cost-driven design methodology of power electronic converters is investigated. The converter is designed to be a part of a low voltage DC system supplying a residential customer. The behavior of an average residential customer as a load is used as one of the inputs for the design process, and therefore, a detailed analysis of the load is carried out. In the analysis, the life cycle cost is defined as the sum of the main components of the power stage of the converter and the losses during the utilization period of the system. Power stage components such as output filtering, semiconductor switches, heat sink, gate drivers, and DC link capacitance are included in the analysis whereas their parameters are freed in the design process. The selection of the switching frequency, the nominal power, and the option of dividing the nominal power among several parallel converter modules are also analyzed.

It is shown that using the load behavior of actual customers is clearly beneficial when the target is to find a cost optimal design of a converter used to supply a residential customer. Although significant drawbacks can be present if the converter has to supply a high current, required by either the protection devices on the customer's premises or the dynamic properties of the load, they can be, to some degree, mitigated by using parallel converter modules instead of one high-powered module.

Keywords: Low-voltage direct current, LVDC distribution, smart grid, power electronics, DC-AC conversion, DC-DC conversion, life cycle cost, optimization

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Aleksi Mattsson
May 2018
Lappeenranta, Finland

Contents

List of publications

Publication I
Mattsson, A., Lana, A., Nuutinen, P., Väisänen, V., Peltoniemi, P., Kaipia, T., Silventoinen, P., and Partanen, J. (2014). "Galvanic Isolation and Output Filter Design for the Low-Voltage DC Customer-End Inverter." *IEEE Trans. Smart Grid*. 5(5), pp. 2593–2601.

Publication II
Mattsson, A., Nuutinen, P., Peltoniemi, P., Kaipia, T., Karppanen, J., Väisänen, V., Partanen, J., and Silventoinen, P. (2015). "Life-Cycle Cost Analysis for the Customer-end Inverter Used in Low Voltage DC Distribution." In *IEEE First International Conference on DC Microgrids (ICDCM).* Atlanta, GA, 7–10 Jun. 2015, pp. 148–153.

Publication III
Mattsson, A., Väisänen, V., Nuutinen, P., Peltoniemi, P., Kaipia, T., Silventoinen, P., Partanen, J. (2015). "Evaluation of Isolated Converter Topologies for Low Voltage DC Distribution." In *41st Annual Conference of the IEEE Industrial Electronics Society.* Yokohama, 9–12 Nov. 2015, pp. 003301–003307.

Publication IV
Mattsson, A., Nuutinen, P., Kaipia, T., Peltoniemi, P., Karppanen, J., Tikka, V., Lana, A., Pinomaa, A., Silventoinen, P., and Partanen, J. (2018). "Design of Customer-End Converter Systems for Low Voltage DC Distribution from a Life Cycle Cost Perspective." In *The 2018 International Power Electronics Conference -ECCE Asia-(IPEC-Niigata 2018)*, Niigata, 20–24 May 2018, pp. xx–xx.

Nomenclature

Latin alphabet

A	area	m^2
a	core dimension; constant	m, –
B	flux density	T
b	core dimension; constant	m, –
C	capacitance; cost	F, €
c_p	specific heat capacity at constant pressure	J/(kgK)
D	duty cycle	–
d	core dimension; diameter; constant	m, m, –
E	energy; energy consumption	J, MWh
f	frequency	Hz
I, i	current	A
K	fill factor	–
k	Steinmetz coefficient	–
L	inductance	H
l	length	m
m	mass; number	kg, –
n	number	–
M	modulation index	–
N	number of turns	–
p	interest rate	
P	power; number of primary-secondary intersections	W, –
RF	ripple factor	–
r	radius	m
T	temperature; period	K,s
t	time	s
V	volume	m^3
W_a	window area	m^2
Z	impedance	–

Greek alphabet

α	(alfa) Steinmetz coefficient
β	(beta) Steinmetz coefficient
Δ	(capital delta) change
δ	(delta) skin depth
η	(eta) porosity factor; efficiency
μ	(mu) permeability
π	(pi)
ρ	(rho) resistivity
Σ	(capital sigma) sum
φ	(phi) phase shift

Ω	resistance
ω	angular frequency

Superscripts

t	time
p	partial layer
^	peak

Subscripts

1p	one-phase
3p	three-phase
a	area
ag	air gap
amb	ambient
avg	average
c	case; cut-off
calc	calculated
cond	conduction
D	diode
ds	drain-source
e	electricity
eff	effective
ext	external
f	forward
g	gate
h	harmonic
hs	heat sink
i	number
ind	inductor
int	interruption
inv	investment
j	junction
l	layer
lk	leakage
lim	limit
loss	losses
mag	magnetic; magnetizing
main	maintenance
max	maximum
min	minimum
mult	multiplier
n	number
nom	nominal

o	overload
op	operating
oss	small-signal output
oss(tr)	time related small-signal output
out	output
pk	peak
pp	peak-to-peak
ϕ	(phi) phase shift
pri	primary
rep	replacement
RMS	root mean square
r	ripple
res	resonance
s	sampling; period
sec	secondary
sw	switching
T_ϕ	time T at the phase shift ϕ
th	thermal
tot	total
U	voltage
u	utilization
w	wire

Abbreviations

AC	Alternating current
AMR	Automatic meter reading
CEC	California Energy Comission
CEI	Customer-end inverter
DAB	Dual active bridge
DC	Direct current
EEL	Equivalent elliptical loop
GaN	Gallium nitride
GSE	General Steinmetz equation
IGBT	Insulated-gate bipolar transistor
iGSE	Improved generalized Steinmetz equation
i^2GSE	Improved improved general Steinmetz equation
LVDC	Low voltage direct current
MLT	Mean length turn
MOSFET	Metal-oxide-semiconductor field-effect transistor
MSE	Modified Steinmetz expression
NSE	Natural Steinmetz extension
PSFBVD	Phase-shifted full-bridge with a voltage doubler type rectifier
PV	Photovoltaic
PWM	Pulse width modulation

SiC	Silicon carbide
THD	Total harmonic distortion
WBG	Wide bandgap
WcSE	Waveform coefficient Steinmetz equation
ZCS	Zero-current switching
ZVS	Zero-voltage switching

1 Introduction

The low voltage DC distribution has been researched for several use cases such as data centers, commercial and telecommunication buildings, microgrids, and public utility grid distribution (Kaipia et al., 2006), (Babasaki et al., 2009), (Fukui et al., 2010), (Kakigano et al., 2010), (Boroyevich et al., 2010), (Yu et al., 2014), (Hakala, 2015). Although all of these application areas use DC as the medium for supplying energy, the focus and optimization targets in the system design may vary, and consequently, similar approaches and solutions may not be optimal when moving from one application to another. For example, a preferred DC voltage level might be a result of some application-specific advantage, which seems to be the main reason for the popularity of the 380–400 VDC voltage range in data centers as it enables the removal of the power factor correction stage from the server power supply while maintaining the internal DC voltage level and almost identical structure of the original power supply (Pratt et al., 2007), (Kwasinski et al., 2009). The focus of this dissertation is on public utility grid distribution (Kaipia et al., 2006), (Kaipia et al., 2013), (Nuutinen et al., 2014) where DC is used as part of the low voltage distribution network and replaces sections of the 20 kV medium voltage network as well as part of the 400 V low voltage AC networks. Owing to the standards and regulations, the customers are not supplied with DC but with 3-phase 230/400 VAC_{RMS} using a customer-end inverter (CEI), and no modifications are made to the electrical installations on the customer's premises. A simplified diagram of the DC system discussed in this dissertation is depicted in Figure 1.1.

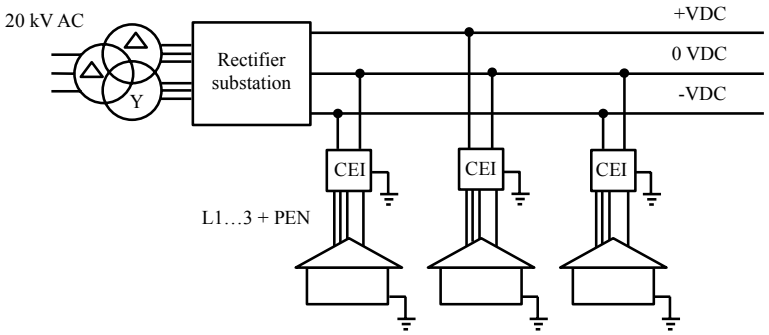

Figure 1.1 Simplified diagram of the LVDC system. The LVDC network connects to the medium voltage network through a step-down transformer and a bidirectional rectifier. The rectifier can feed either a bipolar (as depicted) or a unipolar DC network, and the customers are supplied with 3-phase inverters (Mattsson et al., 2014).

As shown in Figure 1.1, the 20 kV AC voltage of the medium-voltage network is stepped down using a double-tier transformer and the stepped-down AC voltage is then fed to a rectifier substation. The rectifier substation is implemented with two series-connected line converters, which generate an isolated three-wire bipolar DC voltage of ±VDC. The customers are connected either between +VDC and 0 or between 0 and –VDC, and the 230/400 VAC_{RMS} 3-phase supply is produced using a CEI. The low voltage directive LVD 2014/35/EU (LVD, 2014) allows the usage of voltages up to 1500 VDC, whereas the values of 400 VDC and 750 VDC are mainly considered in this work.

1.1 Motivation

Over the recent years, a lot of effort has been put into improving the efficiency and power density of power electronic converters, and efficiencies exceeding 99% and power densities of 10 W/cm^3 have been reported (Rabkowski, 2013), (Gu, 2013), (Hayashi, 2013), (Wu, 2014), (Hayashi, 2015). While it could be argued that the system cost is also minimized when these two parameters are maximized, the result is often a compromise between the different parameters. High values for either efficiency or power density are often achieved by applying state-of-the-art wide bandgap (WBG) semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) based devices. Using state-of-the-art components, however, can potentially increase the cost (Rabkowski, 2013) if the technology is not yet mature for high-volume production. If the system is evaluated based on figures of merit such as power density or weight, the analysis is typically carried out only for the nominal power of the system as this mainly dictates the design in these two cases. Further, emphasis is often put on the peak efficiency at a certain load value rather than over a typical load cycle. Nevertheless, in an application such as the low voltage DC system, the load can vary on a large scale, whereas only a small amount of time can be spent at or near the nominal point. In such a case, a system optimized for power density or weight can potentially lead to a suboptimal result because typically some of the performance at partial load is sacrificed in favor of a higher performance near the nominal point.

For example in the case of photovoltaic (PV) inverters, the European or the California Energy Commission (CEC) weighted average efficiency definitions are widely used (Sandia, 2004). These definitions are derived based on the irradiance and temperature data representative of the Southwest US in the case of the CEC, and the Middle European climate in the case of the European efficiency (Energy Star, 2013). Based on the climate data, different weights are given for the efficiency of the PV inverter at different output power levels to better approximate the efficiency of the transferred energy during solar production. However, to the author's knowledge, little effort has been put to investigate the load profile of a power electronic converter in the case of the low voltage DC (LVDC) distribution and the question of how the load profile could be used to optimize the design of the converter, even though these are among the crucial points that have to be addressed when optimizing the LVDC system. Further, because the LVDC system is considered as a replacement for parts of the medium- and low voltage AC distribution networks, in which the decisive factor for feasibility is the life cycle cost, we also need to consider the various cost factors that are involved when evaluating whether a particular converter design is optimal or not. Past works regarding the usage of power electronic converters in the LVDC system have mainly considered the control and filtering (Peltoniemi, 2010), communication (Pinomaa, 2013), computational modelling (Lana, 2014), implementation (Nuutinen, 2015), and efficiency (Rekola, 2015), whereas the questions regarding the cost, the loading of the converter, and its effect on the design are yet to be answered.

1.2 Objective of the work and research methods

The objective of this dissertation is to analyze how typical loads, in this case a residential customer, behave as a load for a power electronic converter and show how the profile of the load affects the design of the converter when the objective is to minimize the life cycle cost. The major power stage components, being the semiconductor switches, the gate drivers, the heat sink, the output filtering, the isolation transformer, and the DC capacitance are included in the analysis. Design variables such as the selection of the nominal power, the switching frequency, and the key components of the CEI are addressed. The option of dividing the nominal power among several parallel CEI modules of lower nominal power instead of using a single high-powered module is also considered in the analysis to determine whether a decentralized structure could solve some of the challenges posed by the application requirements. Even though the emphasis is laid on the design from the perspective of the LVDC system, the methodology is still valid in other applications if application-specific parameters, such as the load profile, are adjusted accordingly.

The doctoral dissertation focuses on the design methodology and the behavior of the result as a function of the main design variables. Therefore, for example the selection of the optimal topology and control strategy of the converter is not within the research objectives. Instead, a single topology, in this case a hard-switched full-bridge inverter, is used as an example case to illustrate the life-cycle-cost-based design methodology as well as the behavior of the result as a function of the main design variables. Even though the selection of the optimal topology is beyond the scope of this work, the presented methodology can be easily used to evaluate different converter topologies if the current waveforms are known, whereas topology-specific properties, if present, have to be included in the workflow.

Because of the structure of the DC network in Figure 1.1, galvanic isolation is required between the customer-end AC network and the DC network. Therefore, two different types of solutions for the implementation of this galvanic isolation, namely a passive and an active one, are compared with each other. In the case of the active solution, which is implemented using an isolated DC-DC converter, two fundamentally different topologies are analyzed and compared.

The research is carried out by using analytical calculations and simulations, whereas the main focus is put on analytical methods, and simulations are mainly used as a tool to verify the analytical calculations. In the cases in which an analytical method could not be verified by simulation, a method that was already empirically proven to provide high accuracy was used.

The converter topologies covered in this dissertation are analyzed using a purely resistive load, whereas the derivations of the conduction and switching loss equations are mainly based on the value of the load current. Because of the high switching speeds of the components considered in this dissertation, the effect of the dead time is not included in

the analysis. The supplying DC network, or intermediate DC circuit, is considered as a voltage source to simplify the analysis.

1.3 Outline of the work

This doctoral dissertation consists of an introductory section (Part I) and four appended original publications (Part II). The contents of the introductory section are divided into five chapters, which are as follows.

Chapter 1 gives an introduction to the LVDC distribution system concept and briefly introduces different cases in which LVDC is being used worldwide. The motivation of the dissertation, the objectives, and the scientific contributions are also described.

Chapter 2 focuses on defining the requirements set by the load, in this case a residential customer, which is being supplied by using a power electronic converter. Several key factors of the load, which must be taken into account when designing a power electronic converter for the application, are discussed. AMR measurements for two different types of customers are presented as an example of the load, and the differences between the two load profiles and the reasons for them are discussed. Averaged load profiles representing a larger group of customers of the similar type are then introduced and used in the analyses of the appended publications. The dynamic properties of the load and the overcurrent supply during a short-circuit, not visible in the load profiles because of their limited resolution, are also taken into consideration.

Chapter 3 defines the different constraints, variables, and equations that are required in order to formulate the optimization problem, which in this case is the minimization of the life cycle cost of a power electronic converter supplying a residential customer. The chapter is divided into different subsections, which focus on the general variables and constraints, power stages, magnetic components, price data, and the description of the calculation algorithm.

Chapter 4 gives an overview of the appended publications and summarizes their key results.

Chapter 5 concludes the dissertation and gives suggestions for future work.

1.4 Summary of publications

This doctoral dissertation consists of four publications, two of which are refereed conference publications and two are refereed journal publications. The primary author of each publication is the author of this dissertation. The primary author carried out the research presented in the publications and wrote the manuscripts, whereas the coauthors provided comments on the manuscripts. Coauthor Dr. Vesa Väisänen provided a basic structure for the litz wire calculation algorithm, which was used in the isolation transformer calculations of **Publication I** and **Publication II**.

Publication I discusses the drawbacks of implementing the galvanic isolation of the CEI using a 50 Hz transformer and makes a comparison against an alternative solution in which the isolation is implemented using an isolated DC-DC converter. The publication also gives a preface to the dissertation and introduces the usage of the customer load profile in the design process of the CEI. A methodology of designing the output LC filter of the CEI by minimizing the life cycle cost is introduced, whereas the dimensioning is carried out only for the nominal power of the CEI.

Publication II extends the design methodology presented in Publication I to cover the rest of the inverter power stage of the CEI, whereas the main semiconductor switches, the gate drivers, the output filtering, and the DC capacitance are considered in the analysis. The option of dividing the nominal power of the inverter among several parallel modules of lower nominal power is also addressed. Two different types of customer load profiles are introduced and CEIs for both types are designed. The resulting designs and their life cycle costs are then compared with each other. The effect of the input voltage value of the CEI on the life cycle cost is also investigated. The dimensioning is carried out only for the nominal power.

Publication III compares two types of isolated DC-DC converter topologies for the implementation of the galvanic isolation in the low voltage DC system. Two fundamentally different topologies were purposely selected for the comparison to determine which of the two approaches would seem most fitting to the task. The advantages and problems of the two topologies are compared and both converters are then designed using a similar methodology as presented in Publications I and II. The resulting life cycle costs are then compared with each other. Results are calculated for two output voltage levels of 750 VDC and 400 VDC to complement the study of Publication II. The dimensioning is carried out only for the nominal power.

Publication IV extends the design methodology of Publication I and Publication II to incorporate the effect of an overload situation. Requirements of the protection devices on the customer's premises and the dynamic properties of the load are included in the analysis. Therefore, a more detailed analysis of the load is conducted using recent AMR data, averaged load profile models, and measurements carried out on typical household appliances. The calculation algorithms are updated to include methods with improved accuracy for the calculated losses of the various components of the power stage. Additional components not yet available during the writing of the previous publications are incorporated in the input libraries that are used in the calculation. A sensitivity analysis is also performed on the main input variables to determine their significance in the final result. The converters designed using the load profiles are also compared with a case in which the converter is designed to run at its rated power to determine the significance of the load profiles in the design phase.

1.5 Scientific contributions

The scientific contributions of this doctoral dissertation are:

- Analysis of how a residential customer behaves as a load for a power electronic converter and identification of the challenges posed by the application requirements.
- Demonstration of how the load behavior of a residential customer can be used to optimize the design of the converter supplying the customer.
- Showing that it is clearly beneficial to use the load behavior of residential customers as one of the inputs in the design phase of a customer-end converter if the target is to find a cost optimal design.
- Showing that a power electronic converter designed to supply a residential customer can significantly differ from the industry norm in which the performance near the nominal power is typically emphasized during the design phase as this mainly dictates the resulting power density.
- Showing that despite the current trend of pushing the switching frequencies to increasingly higher levels to decrease the size of the output filtering, the cost caused by the additional switching losses can be cost prohibitive depending on the application.

2 Residential customer as a load for a power electronic converter

In order to fully understand the key factors in the design optimization of the CEI, we must first understand how a residential customer behaves as a load for a power electronic converter. This chapter introduces several key factors of the load, which must be taken into account when designing a power electronic converter for this application. Recent AMR measurements for two different types of customers are introduced as an example of the load. The differences between the two customer's load profiles and their reasons are discussed. Averaged load profiles representing a larger group of customers of similar types are then introduced as they are also used in the analyses of the appended publications and can be considered to better represent an average residential customer. Because the load profiles contain data with an hour-based resolution, they do not adequately represent the dynamic properties of the load. Therefore, additional factors, which affect the dimensioning of the CEI, but are not visible in the hour-based data are also investigated.

2.1 Customer load profiles

In Finland, LVDC is considered to be a feasible alternative to AC in rural areas (Kaipia et al., 2006), (Hakala, 2015). Typical customers in these areas are households residing in detached dwellings and having either electricity, district heating, oil, or a ground source heat pump as their main source of heating. As discussed in (Adato, 2011), the average yearly energy consumption of a single customer in the case of electrical heating is 19.6 MWh being 7–11 MWh in the cases in which some other heating system is used. When we consider how the customer behaves as a load for a power electronic converter, we are also interested in identifying the magnitudes of the peak powers of the customer and analyzing how the load changes as a function of time, or to be more exact, the amount of time that is spent at different load values. However, looking only at the power levels and time can also be somewhat misleading as the electricity cost is based on energy consumption. An hour spent at a load value of 1 kVA is not equal to an hour spent at a load value of 2 kVA. Therefore, the analysis will mainly consider the questions of how the supplied energy is distributed among the different load values and how they compare with the nominal rating of the CEI.

AMR data of two customers which have different types of heating systems are depicted in Figure 2.1 to illustrate an example of how the load of a residential customer behaves during a one-year period. The same graphs are also introduced in **Publication IV**. The top graph of Figure 2.1 is a customer residing in a detached dwelling and using electricity for heating (CUST1). CUST1 also has a 300 L electric water heater. The bottom graph of Figure 2.1 is a customer residing in a detached dwelling with modern facilities including a heat recovery ventilation and uses a ground source heat pump as the source for heating (CUST2). CUST2 has an electric sauna stove, whereas CUST1 has a wood-burning sauna stove. The yearly energy consumption of CUST1 is E = 23.9 MWh, whereas for CUST2

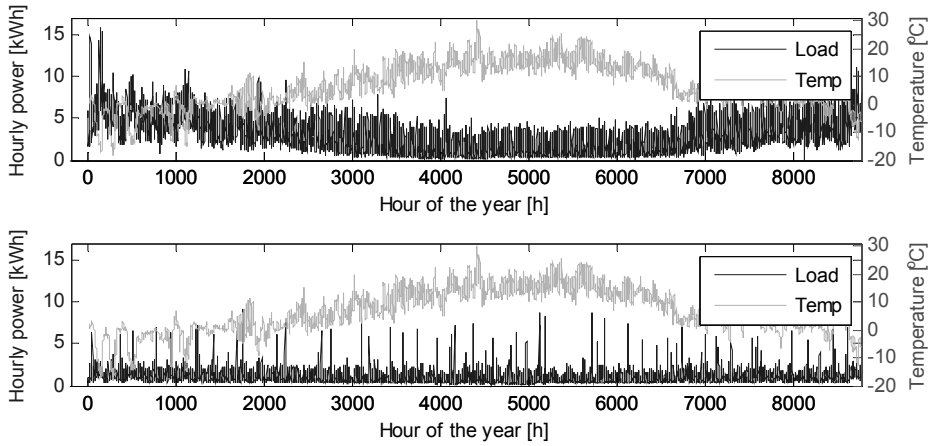

Figure 2.1 Hourly AMR measurements and outside temperatures for a period of one year (1 Jan. 2015–31 Dec. 2015) from a customer (CUST1) that has electrical heating and a yearly energy consumption of 23.9 MWh (upper graph) and from a customer (CUST2) that has modern facilities and uses a ground source heat pump as the source for heating and has a yearly energy consumption of 7.9 MWh (lower graph).

E = 7.9 MWh. When we compare the values of E with the values discussed in (Adato, 2011) we can see that E of CUST2 well represents an average value for this customer type whereas E of CUST1 is above a typical value. The peak power with the hour-based resolution of the data is P_{pk} = 15.8 kW for CUST1, being P_{pk} = 9.2 kW in the case of CUST2. In Finland, this type of customers typically have 25 A main fuses, which technically allow a constant three-phase power draw of P_{max} = 17.25 kW. Because the distribution tariff in Finland is fixed to the main fuse size, the maximum power cannot be limited as the customer is paying for the ability to use the power that can be supplied through the fuses. Therefore, P_{max} would be the dimensioning power of the CEI instead of P_{pk} and be the same for both customer types despite the differences in their actual peak loads. Looking at both graphs in Figure 2.1 we can see that the load varies considerably during the year. If we compare the two graphs with each other, we can see that the load curve of CUST1 is heavily dependent on the outside temperature as a result of the electrical heating, whereas the load curve of CUST2 does not significantly change as a result of variations in the outside temperature because electricity is not directly used for heating but instead, to run the compressor of the ground source heat pump. The peaks in the load of CUST2 are mainly caused by the electric sauna stove, whereas the peaks of CUST1 are mainly caused by the increase in the required heating power when the outside temperature decreases far below 0 ˚C. CUST1 also uses a night-time tariff to heat their water in the 300 L hot water supply, and thus, an increase in the hourly power is observed on a daily basis when the tariff changes and the hot water supply is automatically switched on during the night.

In order to better understand how the supplied energy is distributed among the different load values and how they compare with the value of P_{max} = 17.25 kW, the energy supplied

at different load values was calculated as a percentage of the total supplied energy during the year. The percentage of the total supplied energy at different power levels as a percentage of P_{max} is depicted in Figure 2.2.

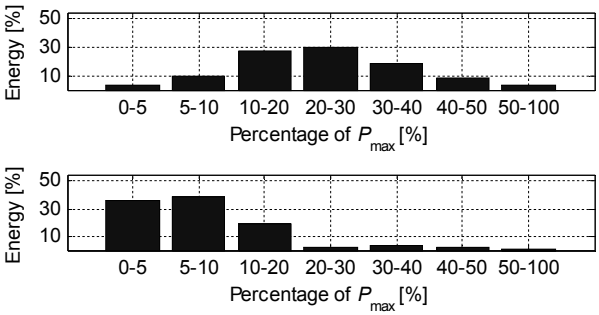

Figure 2.2 Distribution of the supplied energy as a function of percentage of the peak power P_{max} for CUST1 (upper graph) and CUST2 (lower graph).

In the case of CUST2, most of the energy is being supplied at 0–20% of P_{max} being 10–40% of P_{max} in the case of CUST1. When we consider a power electronic converter that would supply the customer and look at these values, we can conclude that in both cases, CUST1 and CUST2, the nominal power $P_{nom} = P_{max}$ of the converter would seldom be used, whereas most of the energy is supplied between the load values of 0–40% of P_{max}. However, while the graphs of Figure 2.1 and Figure 2.2 are good examples of the electricity usage behavior of a single residential customer, they are not good inputs for a design process of a converter that would be used on a wider scale to supply several customers. Despite being of similar type, each customer will have their individual differences in their electricity usage. If a load profile of a single customer is selected as the input for the design process of the CEI and the profile does not well represent an average customer of the same type, design parameters such as the efficiency might be optimized for the wrong power levels. In **Publications I–IV**, averaged load profiles (SLY, 1992) are used as one of the inputs for the analysis. The profiles of (SLY, 1992) have been formulated based on measurements carried out on a group of customers and therefore, better represent an average customer. Owing to the format of the averaged profiles, they allow a lot of flexibility if used in a design process. Instead of actual power levels, the load values in the profile are defined as a percentage of the average hourly power, whereas the average hourly power is calculated from the yearly energy consumption E of the customer by

$$P_{\text{avg,hour}} = \frac{E}{8760}. \tag{2.1}$$

The hourly power P_{hour} for each hour of the year can then be calculated by multiplying the percentage value of each hour of the profile by $P_{\text{avg,h}}$. In **Publications I–IV**, a value of $E = 20$ MWh is used in the case of a customer using electrical heating (from here on type 1), and values of $E = 9$–10 MWh in the case when the customer has some other heating system (from here on type 2), both values being in good agreement with the values

discussed in (Adato, 2011). In order to compare the differences between the data of individual customers in Figure 2.2 and the averaged profiles, the percentage of the total supplied energy at different power levels as a percentage of P_{max} using the averaged profiles was calculated and is depicted in Figure 2.3.

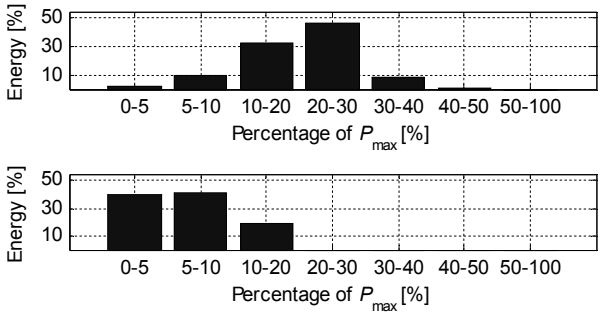

Figure 2.3 Distribution of the supplied energy as a function of percentage of the peak power P_{max} for averaged load profiles of customer types (upper graph: type 1, lower graph: type 2) similar to Figure 2.2.

If we compare Figure 2.3 and Figure 2.2 with each other, we can see that the distribution of the supplied energy for CUST2 actually well represents an average type 2 customer. However, the distribution of the supplied energy of CUST1 deviates from the average type 1 customer. When we consider that the electricity usage of CUST1 will differ from year to year depending on the changes in the outside temperature, which partly explains the differences between Figure 2.2 and Figure 2.3, the fact remains that the load profile of an individual customer is not a good indicator when assessing the overall performance of a power electronic converter that would be used to supply a variety of customers even if the customers were of the same type. Therefore, the averaged profiles were selected as a basis for the analysis.

2.2 Dynamic properties of the load

Although the load profiles can be used to analyze how the load of the converter is distributed at different power levels, the load profile does not necessarily accurately represent the dynamic properties of the load because of the hour-based resolution of the data. If the load changes rapidly and returns to a lower level for a longer period, the resulting value in the load profile could be well below the actual short-term peak load. For example, some of the household appliances, especially motor loads, can potentially have high turn-on currents despite their nominal power being below a few kilowatts. Therefore, a set of measurements were carried out on several household appliances, which could potentially have high turn-on currents to determine their magnitude and duration. The measurements included appliances such as typical power tools, vacuum cleaners, an audio amplifier, and a washing machine. Among the tested appliances, the highest measured turn-on current of 40 A_{pk} was observed on a vacuum cleaner, which was an older model without any soft-start circuit. The peak current lasted for a couple of line

cycles after which the current decreased to its nominal value in under 200 milliseconds. Because a power electronic converter is typically dimensioned for a specific nominal power and therefore, cannot withstand a high overload situation, these rapid changes in the load have to be taken account of in the design phase of the converter to avoid malfunction or a possible destruction resulting from an overcurrent exceeding the ratings of the various components of the converter.

2.3 Requirements set by the protection devices

Even though relatively high turn-on currents were measured on some of the typical household appliances, which are potential loads for the CEI, we also have to consider another situation that potentially requires the converter to supply a high current that exceeds the nominal rating. Because no changes are made to the electrical installations on the customer's premises, we have to take into account the current and trip time requirements set by the protection devices at the customer-end installations. As previously mentioned, a typical main fuse size for detached houses is 25 A in Finland. The fuse in this case is of a gG-type. The required trip times for gG-type fuses are defined in the standard SFS-6000-4-41 (SFS, 2012). In order to fulfill the trip time requirement of ≤ 5 s defined in the standard (SFS, 2012), a minimum current of 110 A_{RMS} is required when a gG25 fuse is used (SFS, 2008). In addition to the main fuses, the customers have circuit breakers protecting the branch circuits of the customer-end installation. Typically, B-type and C-type circuit breakers are used, whereas the breaker type is selected based on the load that is to be connected after the breaker. As discussed in (Nuutinen, 2015), a C16 circuit breaker can be considered the most demanding breaker type regarding the required trip current in branch circuit protection. For a circuit breaker, the required trip time is ≤ 0.4 s. In the case of a C16 breaker, the trip time of 0.4 s is guaranteed with a current value of 160 A_{RMS}. If we compare the requirements of the protection devices with the turn-on currents of the household appliances, we may conclude that the requirements set by the protection devices are far more demanding. This will also result in a significant difference between the nominal current I_{nom} and the overload situation, which can have a serious effect on the design of the CEI and must be taken into account in the design phase.

3 Life-cycle-cost-based design methodology

Design optimization of power electronic converters has been previously discussed in several publications such as (Yu, 1979), (Balachandran, 1981), (Wu, 1982), (Busquets-Monge, 2004), (Teichmann, 2005), (Lai, 2008), (Yu, 2012), (Hayashi, 2013). The main topics have mainly focused on either maximizing the power density or minimizing the weight. In many cases a pareto-front is also used to illustrate the results as it shows the relationship between two main parameters, for instance between efficiency and power density. In applications such as data centers and telecommunication buildings, power density is typically the main concern as the equipment takes up a lot of space. On the other hand, in an application such as aerospace or aviation, one does not want to unnecessarily increase the weight of the aircraft, and thus, the weight is one of the main design objectives. In publications such as (Busquets-Monge, 2004), and (Teichmann, 2005), the cost of the converter is also taken into consideration. In (Busquets-Monge, 2004), the objective function is set to minimize the sum of the component cost of a boost power factor correction, whereas (Teichmann, 2005) tries to minimize the life cycle cost of a converter that is primarily used in the rectifier mode. Typically, when the target design parameter is either power density or weight, the analysis is performed using only the rated power of the converter as this mainly dictates the resulting design when it comes to these two parameters. In (Busquets-Monge, 2004) and (Teichmann, 2005) the optimization is also carried out using the rated power even though the objective function is related to the cost. However, if we look at how a residential customer behaves as a load in Chapter 2, it is obvious that if the analysis is done using only the rated power, in this case P_{max} = 17.25 kW, it could potentially lead to a suboptimal design in the case of the LVDC system. When the converter is optimized using the nominal point, the design is likely to favor a higher silicon area to reduce the conduction losses at the cost of higher switching losses, whereas low copper losses at the cost of higher iron losses might be preferred in the magnetic components. Nonetheless, both approaches effectively reduce the conversion efficiency at lower power levels, where the switching losses and iron losses begin to dominate the conduction losses. On the other hand, in the case of the LVDC system and looking at the load analysis of Chapter 2, it might be feasible to decrease the iron losses and the switching losses at the cost of conduction losses to increase the efficiency at lower power levels.

Because the LVDC system is considered to be a part of the distribution network, in which the decisive factor for feasibility is the life cycle cost, we also need to consider the various cost factors that are involved when evaluating whether a particular CEI design is optimal or not. Therefore, the objective function in the case of the CEI is similar to the one that is commonly used in the techno-economic evaluation of the distribution network and is written as

$$C_{min} = \min \sum_{t=1}^{t_u} [C_{inv}(t) + C_{loss}(t) + C_{int}(t) + C_{main}(t)], \tag{3.1}$$

where C_{inv} is the investment cost, C_{loss} is the cost of the losses, C_{int} is the interruption cost, C_{main} is the maintenance cost and t_u is the utilization period (Lakervi, 2008). Typically, a

value of 40 years is used for t_u as discussed in (Partanen, 2002) and (Willis, 2004). If we compare this value with typical lifetimes of power electronic converters, which can vary between 5 to 30 years depending on the target application as discussed in (Chung et al., 2016), it is obvious that it is likely that the CEI has to be replaced at least once during the utilization period of $t_u = 40$ years of typical distribution network components. In such a case, we need to define a cost for the replacement unit. Because we are projecting future costs, the price for the replacement unit is calculated using the present value, which is defined by

$$C_{inv} = C_{rep}(1 + p)^{-t_{rep}}, \tag{3.2}$$

where C_{rep} is the reference cost of the replacement unit, p is the interest rate, and t_{rep} is the replacement interval. A replacement interval of $t_{rep} = 20$ years and a value of $p = 5\%$ are selected for the calculations of **Publication IV** when the life cycle cost is calculated for $t_u = 40$ years. The replacement unit is assumed identical to the initial unit and no performance factor is used. Only the replacement of whole converter units is considered, and therefore, C_{main}, which includes for example the cost of replacing a single component of the CEI, and C_{int}, which refers to the cost caused by an interruption in the electricity supply, are not included in the calculations. Because these two terms are excluded from the analysis, the expression of (3.1) reduces to

$$C_{min} = \min \sum_{t=1}^{t_u} [C_{inv}(t) + C_{loss}(t)], \tag{3.3}$$

which is used as the objective function in this doctoral dissertation and the appended publications. Because the costs of the losses of the CEI are projected as future costs over a period of several years, C_{loss} is calculated as the present value of an annuity by

$$C_{loss} = P_{tot} C_e \frac{1-(1+p)^{-t_u}}{p}, \tag{3.4}$$

where P_{tot} is the power loss over a period of one year, and C_e is the cost of electricity.

Typical for an optimization problem of a system or a physical device, the objective function of (3.3) has a set of constraints and variables. Although similar constraints and variables are discussed in (Yu, 1979), (Balachandran, 1981), (Wu, 1982), (Busquets-Monge, 2004), (Teichmann, 2005), (Lai, 2008), (Yu, 2012), and (Hayashi, 2013), some of them are different owing to their application-specific nature. The constraints and variables can be divided into three categories and are discussed in more detail in the following subsections.

3.1 General constraints

The CEI is required to meet certain general requirements, which are used as the general constraints for (3.3). The DC voltage levels are limited by the low voltage directive, which states that the maximum allowable voltage level is 1500 VDC (LVD, 2014). However,

owing to the bipolar configuration of the DC network considered in this work, 750 VDC is used as the upper limit for the input voltage of the CEI. The lower limit comes from the required minimum voltage of 325 VDC in order to generate a single-phase 230 VAC_{RMS} output. The values of 400 VDC and 750 VDC were mainly considered in **Publications I–IV**, whereas the LC filter in **Publication I** was also calculated for a DC voltage level of U_{DC} = 1500 V. The minimum requirement for voltage quality is set by the standard SFS-EN 50160 (SFS, 2010), which states that the long-term voltage THD should be below 8%. In (Partanen et al., 2010), nonetheless, a stricter target of a maximum of 5% was set for the LVDC system and was also used in **Publications I**, **II**, and **IV**.

As discussed in Chapter 2, the typical main fuse size in Finland is 25 A. Because it is currently not feasible to alter the customer-end electrical installations, the CEI has to be able to supply the maximum steady state-current defined by the main fuse. Therefore, the minimum value of the nominal power of the CEI is $P_{nom,3p}$ = 17.25 kW for the sum of all the three phases, and $P_{nom,1p}$ = 5.75 kW for a single phase. It should be noted here that the main fuses would allow an intermittent power draw exceeding these values as defined by the characteristic curve of the individual fuse, but it is not considered here. The requirements set by the protection devices introduced in Chapter 2 are also incorporated into the general constraints and were used in the calculations of **Publication IV**. In the analyses of **Publications I–III**, instead, only nominal ratings were used. As discussed in Chapter 2, the requirement set by a gG25 fuse is 110 A_{RMS} for 5 s, being 160 A_{RMS} for 0.4 s in the case of a type-C 16 circuit breaker. To simplify the analysis, a value of 160 A_{RMS} for 5 s was used in the calculations of **Publication IV** as it meets the requirement for both protection devices. However, because the difference between the nominal current of 25 A_{RMS} and the short-circuit current of 160 A_{RMS} is likely to have a significant effect on the final result, the overload was analyzed in the range of 50–160 A_{RMS}, whereas the same duration of 5 s was used for all current values. As discussed in (Nuutinen, 2013), the functionality of the CEI could easily be used to implement an intelligent protection device, but unfortunately, this is currently not allowed by standardization. If the CEI could be used to cut the fault current, the overdimensioning resulting from the high-current requirements set by the protection devices could be mitigated. Nevertheless, in this case it would be crucial to know the maximum turn-on currents of the various household appliances that are used on the customers' premises as the CEI has to be able to supply these currents even if they exceed the nominal rating. The CEI should also be able to distinguish a fault situation from a turn-on current of an appliance even if they were of similar value.

The example cases in **Publications I**, **II**, **and IV** are calculated for a CEI structure in which each of the three phases of the CEI is implemented using a full-bridge inverter with an isolated DC input. The isolation stage is discussed in **Publications I** and **III**. Whereas **Publication I** only considered a single CEI module, the analyses of **Publications II–IV** included an option of dividing the nominal power P_{nom} = P_{max} of the inverter among several parallel modules of lower nominal power. A simplified diagram of the CEI as used in the example cases is depicted in Figure 3.1.

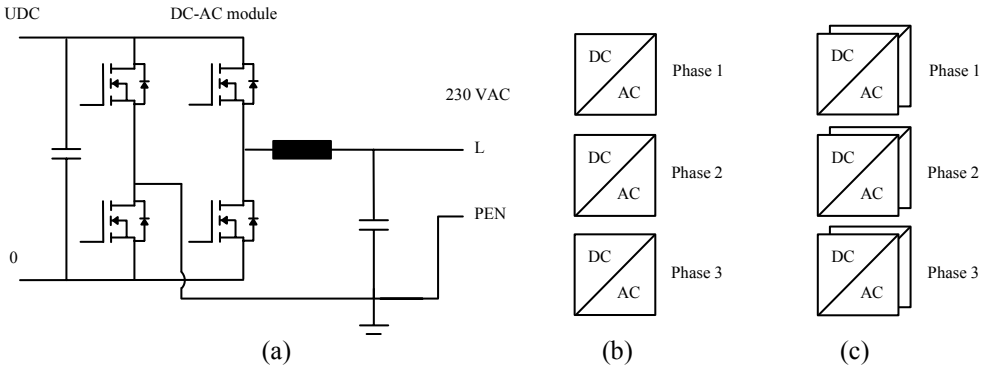

Figure 3.1 Simplified diagram of the example cases in which a full-bridge inverter (a) is used as a building block for the CEI (b) and the option of paralleling several CEI modules (c) is also considered.

In the parallel module cases of Figure 3.1, the nominal power of a single module is calculated by

$$P_{\mathrm{nom},n} = \frac{P_{\max}}{3n}, \quad n \in [1,2,3\ldots6], \tag{3.5}$$

where n is the number of the parallel modules in a single phase. Only a minimum number of the parallel modules required to supply the load are switched on at a given time as defined by

$$n_{\mathrm{op}} = \left\lceil \frac{P_{hour}}{3P_{\mathrm{nom},n}} \right\rceil, \quad n_{\mathrm{op}} \in [3,6,9\ldots18], \tag{3.6}$$

whereas the load is assumed to be evenly distributed among the three phases. The ambient temperature will partly limit the maximum temperature rises of the various components of the CEI. A worst-case temperature inside the CEI cabinet can be considered to be around 50 °C, and therefore, a value of $T_{\mathrm{amb}} = 50$ °C was used as the constraint in the calculations of **Publications I–IV**.

3.2 Power stages

In this doctoral dissertation, the power stage is considered to contain the semiconductor switches and their heat sinking. A high reliability is preferred in the distribution network, and thus, only cooling by means of natural convection is considered. Although adding a fan to the heat sink would considerably decrease its thermal resistance $R_{\mathrm{th,hs}}$, and therefore, also potentially decrease the junction temperature T_{j} of the semiconductors and the size of the heat sink, the relatively high failure rate of fans would also increase the requirement for consecutive maintenance of the CEI. The main constraints that are due to the power stage semiconductors are the breakdown voltage and the maximum junction temperature $T_{\mathrm{j,max}}$ of the semiconductor as increasing the voltage or temperature beyond

these values would destroy the device. A value of two-thirds of the breakdown voltage is typically used for the maximum working voltage of semiconductor switches because of the overvoltage spikes that are induced in hard-switched applications as a result of the parasitic inductances in the circuit. Silicon Carbide (SiC) semiconductors from Wolfspeed, and Gallium Nitride (GaN) semiconductor switches from Gan Systems were used in the calculations of **Publications I–IV**, and their parameters can be found in (Wolfspeed, 2016) and (Gan Systems, 2016). The SiC switches have a breakdown voltage of either 900 V or 1200 V, whereas the GaN switches have a breakdown voltage of 650 V. However, enough data about the 900 V SiC switches and the 650 V GaN switches were not available at the time of writing **Publications I–III**, and therefore, these switches are included only in the calculations of **Publication IV**.

3.2.1 Heat sinking

All of the semiconductors used in **Publications I–IV** have a maximum junction temperature of $T_{j,max}$ = 150 °C. This value was used as the constraint for T_j during the overload in the calculations of **Publication IV**. However, a lower value of $T_{j,max,nom}$ = 100 °C was selected as the constraint for the maximum junction temperature during nominal load, and was used in the calculations of **Publications II–IV**. The steady-state junction temperature of the semiconductor depends on several thermal resistances between the semiconductor junction and the air cooling the heat sink as well as the power loss of the semiconductor and T_{amb}. These thermal resistances are the junction to case thermal resistance $R_{th,j\text{-}c}$, the thermal resistance between the case and the heat sink $R_{th,c\text{-}hs}$, and the thermal resistance of the heatsink $R_{th,hs}$. The thermal pathway and the various thermal resistances and temperatures are illustrated in Figure 3.2.

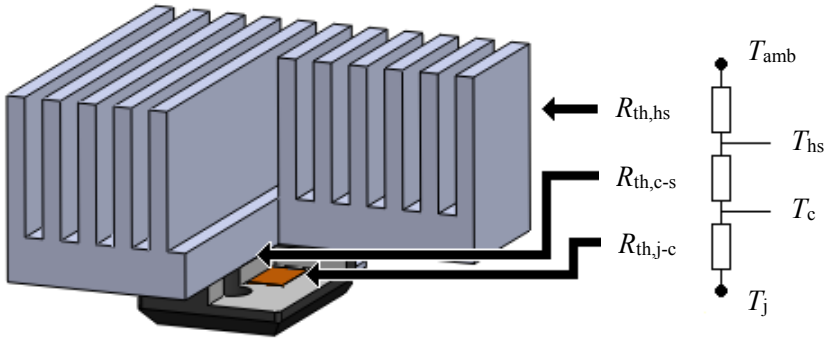

Figure 3.2 Thermal pathway from the semiconductor junction to the cooling air including the various thermal resistances and temperatures of the system.

In reality, the thermal impedance $Z_{th,j\text{-}c}$ of the semiconductor consists of several thermal resistances and capacitances inside the device packaging, but as they are not always given in the datasheet of the device, the information is limited or difficult to read accurately, the semiconductor was analyzed using only the steady-state combined value $R_{th,j\text{-}c}$. Including the behavior of $Z_{th,j\text{-}c}$ would enable a more detailed analysis of T_j especially in a case in which the duty cycle or pulse width, or both, have low values. In such a case,

the thermal capacitances of the device allow the pulsed current to far exceed the nominal rating of the device without T_j exceeding the maximum allowed value $T_{j,max}$. The variation of T_j as a function of an arbitrary pulsed current waveform and $Z_{th,j\text{-}c}$ can be calculated as explained in (NXP, 2012).

It is important to understand that changing only one component in the thermal pathway will affect the whole system. For example, a semiconductor with a higher silicon area is more expensive, but will typically have lower conduction state losses, and at the same time, a lower value of $R_{th,j\text{-}c}$ compared with a semiconductor having a lower silicon area. Therefore, a cheaper heat sink with a higher $R_{th,hs}$ could be used. However, if a semiconductor with a lower silicon area and thus, a higher $R_{th,j\text{-}c}$ and higher conduction losses is equipped with a more expensive heat sink having a lower $R_{th,hs}$, the resulting T_j could be the same for both systems. The semiconductor with a lower silicon area will also be cheaper and have lower switching losses, and therefore, it could be possible to select a higher switching frequency and affect the design of the output filter while potentially making it less expensive. As a result, it is not immediately obvious which of the possible combinations will result in the lowest total cost, including the loss-related cost, especially when the load behaves in a manner described in Chapter 2.

The thermal pathway of Figure 3.2 should fulfill the constraint

$$T_{j,max,nom} - P_{loss,nom}\left(R_{th,j\text{-}c} + R_{th,c\text{-}hs}\right) - P_{loss,nom,tot}R_{th,hs} - T_{amb} \geq 0, \quad (3.7)$$

where $T_{j,max,nom}$ is the maximum allowed junction temperature during the nominal load, $P_{loss,nom}$ is the power loss of a single semiconductor at the nominal load, and $P_{loss,nom,tot}$ the total heat load to the heat sink, which is the sum of all the semiconductors in the same heat sink. However, in a dynamic overload condition, caused either by a load connected to the customer's electrical installations, or by a short-circuit fault, the temperature of the heat sink will not necessarily reach thermal equilibrium because of its high thermal capacitance. The transient temperature rise of the heat sink can be calculated by

$$\Delta T_{hs}(t) = P_{loss}R_{th,hs}\left(1 - e^{\frac{-t}{R_{th,hs}C_{th}}}\right), \quad (3.8)$$

where C_{th} is the thermal capacitance of the heat sink, and t is the time. In the worst-case scenario, the CEI is operating at its rated power when the overload occurs. The total temperature rise of the heat sink during the overload is, therefore, calculated by

$$\Delta T_{hs,o}(t_o) = P_{loss,nom,tot}R_{th,hs} + P_{loss,o,tot}R_{th,hs}\left(1 - e^{\frac{-t_o}{R_{th,hs}C_{th}}}\right), \quad (3.9)$$

where $P_{loss,o,tot}$ is the power loss during the overload situation, and t_o is the duration of the overload. Therefore, the constraint of (3.7) is written as

$$T_{j,max} - P_{loss,o}\left(R_{th,j\text{-}c} + R_{th,c\text{-}hs}\right) - \Delta T_{hs,o}(t_o) - T_{amb} \geq 0, \quad (3.10)$$

where $P_{loss,o}$ is the power loss of a single semiconductor during the overload. For this work, several heat sinks from Fischer Elektronik with different values of $R_{th,hs}$ were selected and models as a function of price and $R_{th,hs}$ were formulated based on the data given in (Fischer Elektronik, 2015), (TME, 2015). Because no data were given for C_{th} in the datasheets of the manufacturer, the values of C_{th} were calculated by

$$C_{th} = c_p m, \tag{3.11}$$

where c_P is the specific heat capacity of aluminium, and m is the weight of the heat sink as given in (TME, 2015). The resulting models for the heat sink price and C_{th} as a function of $R_{th,hs}$, are depicted in Figure 3.3.

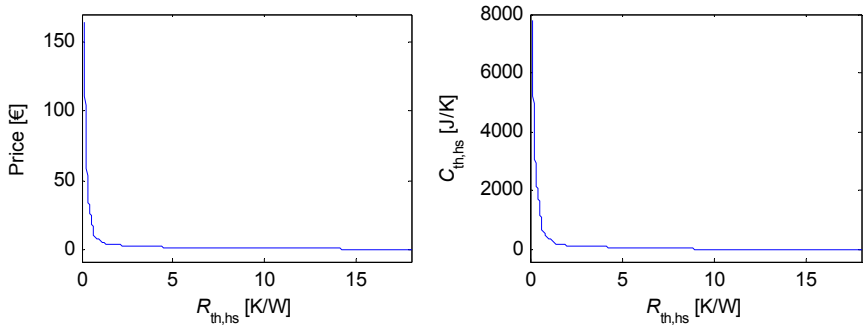

Figure 3.3 Models for the heat sink price (a) and C_{th} (b) as a function of $R_{th,hs}$.

As can be seen in Figure 3.3, the change in price as a function of $R_{th,hs}$ stays fairly linear when $R_{th,hs} > 2$ K/W and begins to increase exponentially when $R_{th,hs} < 2$ K/W. Therefore, it can be concluded that even though the cooling requirement of the semiconductors increased linearly for example as a function of increasing the value of f_{sw}, the cost of the cooling system could make the system cost increase in an exponential manner. The effect is further pronounced when the value $R_{th(j-c)}$ begins to limit the design and the cooling requirement increases exponentially as a function of power loss before we finally reach a situation where $T_{j,max}–T_{amb} = T_j–T_c$ and the required thermal resistance $R_{th,hs}$ of the heat sink would be 0, which is no longer a feasible value. However, the feasibility of the values approaching zero can already be considered questionable in the case of natural convection, when $R_{th,hs} << 0.1$ (Fischer Elektronik, 2015).

3.2.2 RMS currents and conduction losses

In order to calculate the various losses of the semiconductors, descriptions for the RMS current through the semiconductor, and the relationship between current, voltage, and switching energies E_{tot}, E_{on}, and E_{off} are required. In the case of a soft switching topology, the switching energy has to be separated into the turn-on energy E_{on} and the turn-off energy E_{off} as typically only E_{off} is present under zero voltage switching (ZVS). For single-phase inverters, the RMS current for active-stage switches is calculated by

$$I_{\mathrm{RMS,active}} = I_{\mathrm{m}}\sqrt{\frac{2M}{3\pi}}, \tag{3.12}$$

where I_{m} is the peak value of the sinusoidal output current, and M is the modulation index (Gu, 2013). The RMS current for zero-stage switches is calculated by

$$I_{\mathrm{RMS,zero}} = I_{\mathrm{m}}\sqrt{\frac{1}{4} - \frac{2M}{3\pi}} \tag{3.13}$$

(Gu, 2013). In the studied example case, an H-bridge inverter with unipolar modulation using the reverse conduction of the MOSFET channel is used, and therefore, the active-stage MOSFETs also conduct during the zero-stage. The total RMS current through a single switch is, therefore, calculated by

$$I_{\mathrm{RMS,tot}} = \sqrt{I^2_{\mathrm{RMS,active}} + I^2_{\mathrm{RMS,zero}}}, \tag{3.14}$$

which simplifies to

$$I_{\mathrm{RMS,tot}} = \frac{I_{\mathrm{m}}}{2}. \tag{3.15}$$

The conduction loss of a single switch can then be calculated by

$$P_{\mathrm{cond}} = I^2_{\mathrm{RMS,tot}} R_{\mathrm{ds,on}}, \tag{3.16}$$

where $R_{\mathrm{ds,on}}$ is the on-state resistance of a MOSFET switch. Similar conduction loss equations for IGBTs and freewheeling diodes including the voltage drop under zero current are given in (Gu, 2013).

Because the output voltage of the CEI is generated using pulse width modulation (PWM), the output is filtered using a passive filter circuit. In this doctoral dissertation and the appended publications, the filter is assumed to be an LC type filter. Some amount of ripple current flows in the filter circuit, but typically, this current is not included in the power stage loss calculation as the ripple current is negligible compared with the nominal current value. However, as pointed out in (Nge, 2009) the effect of the current ripple on the semiconductor power loss can be significant enough under light load condition, and thus, it should not be left out from the analysis if satisfactory estimation of the power loss under light load is desired. This is especially true in the studied residential customer case, in which the load contains a high amount of partial load as was shown in Chapter 2. Further, as the inductance L of the LC filter is one of the main variables in the filter design and will affect the magnitude of the ripple current, we have to take account of the changes in the losses of the power stage when optimizing the design. If the ripple current is not taken into account, and the high-frequency losses in the core material and the winding of the filter are inherently insignificant, the filter may be optimized for a very low inductance, which increases the ripple current, and as a result, also the light load losses of the power

stage. In such a case it could be possible that the increase in the losses of the power stage outweighs the reduction in the filter cost, but this was not considered in the design phase resulting in a suboptimal design. Therefore, the expressions in (3.12)–(3.16) have to be extended to include the ripple current term. Derivation of the ripple current term in the case of IGBTs and freewheeling diodes is presented in (Nge, 2009). However, the same equations are not applicable to the studied case in which MOSFETs and their reverse conduction are used. The derivation for the filter RMS ripple current for single-phase full-bridge inverters is presented in (Kim, 2008) and is defined by

$$I_{\text{ripple,ind}} = \frac{U_{\text{DC}}}{4Lf_{\text{sw}}}\sqrt{\frac{2M^2}{3\pi}\left(\frac{\pi}{4}\left(1+\frac{3}{4}M^2\right)-\frac{4}{3}M\right)}, \tag{3.17}$$

where L is the inductance of the filter inductor, and f_{sw} is the switching frequency. The ripple current term for a single power stage MOSFET switch can be derived in a similar manner and is calculated by

$$I_{\text{ripple,MOSFET}} = \frac{U_{\text{DC}}}{4Lf_{\text{sw}}}\sqrt{\frac{M^2}{3\pi}\left(\frac{\pi}{4}\left(1+\frac{3}{4}M^2\right)-\frac{4}{3}M\right)}. \tag{3.18}$$

The total RMS current through a single MOSFET switch including the ripple term is then calculated by

$$I_{\text{RMS,tot,r}} = \sqrt{\frac{I_{\text{m}}^2}{4}+I_{\text{ripple,MOSFET}}^2}\,. \tag{3.19}$$

The expression of the ripple current term for a single MOSFET switch in a half-bridge inverter leg with bipolar modulation can be derived similar to (3.18) and is given as

$$I_{\text{ripple,MOSFET,bipo}} = \frac{U_{\text{DC}}}{8Lf_{\text{sw}}}\sqrt{\frac{1}{3}\left(1-M^2+\frac{3}{8}M^4\right)}, \tag{3.20}$$

whereas the total RMS current including the ripple current term can be calculated using (3.19) by replacing $I_{\text{ripple,MOSFET}}$ with $I_{\text{ripple,MOSFET,bipo}}$.

In order to verify the calculated value for $I_{\text{RMS,tot,r}}$, the inverter power stage was simulated in Simulink®. The values of L and capacitance C of the LC filter were varied while keeping the cut-off frequency of the filter and thereby the output voltage THD unchanged. The simulated and calculated values for $I_{\text{RMS,tot,r}}$ of a single MOSFET switch in an H-bridge circuit as a function of the LC filter inductance L are depicted in Figure 3.4.

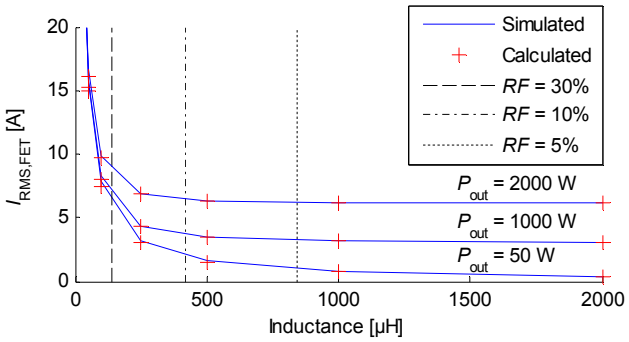

Figure 3.4 Simulated and calculated values for the RMS current $I_{RMS,tot,r}$ of a single MOSFET switch in an H-bridge circuit as a function of the LC filter inductance L and with different values of P_{out}. The limits for three values of the ripple factor RF are also indicated in the figure. Simulation parameters are U_{DC} = 750 V, f_{sw} = 20 kHz, and sampling time t_s = 0.05 µs.

As can be seen in Figure 3.4, the calculated and simulated values are in good agreement. In **Publication IV**, the LC filter is designed by setting the maximum limit for the ripple factor RF_{lim} to either 5%, 10%, or 30% of the nominal RMS current I_{nom} of the CEI. To illustrate how varying the value of RF from 0% to 30% affects the conduction losses of the power stage during partial load, the relative conduction loss $P_{cond,relative}$ of a single MOSFET switch of the H-bridge was calculated as a function of the output power P_{out} of the CEI and is depicted in Figure 3.5.

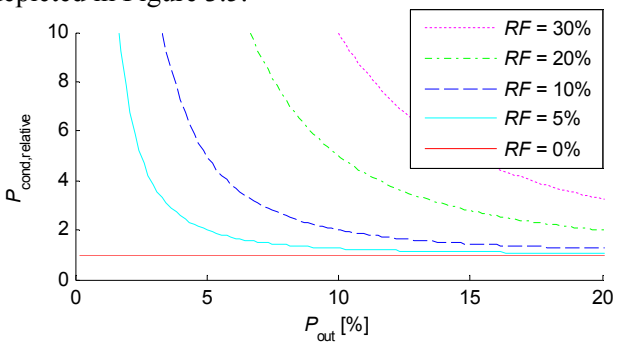

Figure 3.5 Relative conduction loss $P_{cond,relative}$ of a single MOSFET switch in an H-bridge as a function of the output power P_{out} for different values of the ripple factor RF. The results for $RF > 0\%$ are calculated relative to the conduction loss at $RF = 0\%$. The maximum value of P_{out} on the x-axis was selected to correspond to the results of the load analysis of Chapter 2.

As can be seen in Figure 3.5, the effect of the ripple current on the value of P_{cond} is negligible when $RF = 5\%$ and $P_{out} \geq 10\%$. However, when RF is increased to 10% and above, the difference in P_{cond} is considerable when $P_{out} < 20\%$ of P_{nom} and would result in a significant error in the calculated conduction loss with the load profiles of Figure 2.3 and especially in the case of customer type 2. If the analysis is to be carried out using only the nominal power instead, ripple percentages of up to 10% can be considered negligible in terms of the resulting value of P_{cond}.

In **Publications I** and **III**, two types of isolated DC-DC converters, a Phase-Shifted Full-Bridge with a Voltage Doubler type rectifier (PSFBVD) and a Dual Active Bridge (DAB), were analyzed (Lee, 2008), (Kheraluwala, 1992). In the case of the PSFBVD topology, the RMS currents for the primary- and secondary-side semiconductors are calculated by

$$I_{\mathrm{RMS,PSFBVD}} = \sqrt{\frac{1}{T}\int_0^{\sqrt{L_{\mathrm{lk}}C_{\mathrm{res}}}\pi}\left(n\frac{\omega_{\mathrm{res}}I_{\mathrm{out}}}{2}\sin(\omega_{\mathrm{res}}t)\right)^2}, \tag{3.21}$$

where T is the period of the repeating current waveform, L_{lk} is the leakage inductance of the isolation transformer, C_{res} is the resonance capacitance, n is the transformer turns ratio, ω_{res} is the resonance frequency, and I_{out} is the output current (Väisänen, 2012). Selecting the value of n to be either $n_{\mathrm{pri}}/n_{\mathrm{sec}}$ or $n_{\mathrm{sec}}/n_{\mathrm{pri}}$ defines whether the value of $I_{\mathrm{RMS,PSFBVD}}$ is calculated for the primary side or for the secondary side. In the case of the DAB, the basic phase shift modulation that generates a phase shift only between the primary and secondary sides of the transformer was selected as the modulation method, and a similar equation for the various RMS currents was derived based on the equations in (Krismer, 2010). The RMS currents are calculated by

$$I_{\mathrm{RMS,DAB}} = \sqrt{\frac{1}{T}\left(\begin{array}{c}\int_0^{T_\varphi}\left(i_{L,0}\frac{V_1+V_2}{L}\right)^2 dt + \\ \int_{T_\varphi}^{\frac{T}{2}}\left(i_{L,T_\varphi}\frac{(V_1-nV_2)(t-T_\varphi)}{L}\right)^2 dt\end{array}\right)}, \tag{3.22}$$

where V_1 is the input voltage, V_2 is the output voltage, L is the inductance responsible for the energy transfer including either only L_{lk} of the transformer or also an additional external inductance L_{ext}, $i_{L,0}$ is the value of the inductor current $i_L(t)$ at time instant $t = 0$, and $i_{L,T\varphi}$ is the value of the inductor current $i_L(t)$ at time instant $t = T_\varphi$. The current $i_{L,0}$ in (3.22) is defined by

$$i_{L,0} = \frac{\pi(nV_1-V_2)-2\varphi nV_2}{4\pi f_{\mathrm{s}}L}, \tag{3.23}$$

where φ is the value of the phase shift between the primary and secondary sides (Krismer, 2010). The current $i_{L,T\varphi}$ in (3.22) is defined by

$$i_{L,T_\varphi} = i_{L,0} + \frac{(V_1+nV_2)t}{L} \tag{3.24}$$

(Krismer, 2010). The conduction losses of the semiconductor switches for both the PSFBVD and the DAB are calculated by (3.16). The PSFBVD topology uses diodes on the secondary-side rectifier and the conduction losses of the diodes are calculated by

$$P_{\mathrm{cond,D}} = I_{\mathrm{avg,D}}V_{\mathrm{f}} + I_{\mathrm{RMS,PSFBVD}}R_{\mathrm{f}}^2 \tag{3.25}$$

where $I_{avg,D}$ is the average rectified current through the diode, V_f is the zero current voltage drop of the diode, and R_f is the resistance of the diode as read from the IV curve in the diode datasheet. In the case of the PSFBVD topology, $I_{avg,D}$ is identical to I_{out}. Even though the RMS current derivations for the three topologies discussed in this doctoral dissertation are presented above, there are numerous different types of converter topologies, be it an inverter or a DC-DC converter, that have different current waveforms but are not listed here. However, if no simplified derivation is available, the RMS current for any given topology and current waveform can be calculated by (Van den Bossche, 2005)

$$I_{RMS} = \sqrt{\frac{1}{T}\int_0^T [i(t)]^2}. \tag{3.26}$$

3.2.3 Switching losses

For the switching loss calculation, descriptions for the switched current I_{sw} and switching energy are required. The switching energies E_{tot}, E_{on}, and E_{off} for all the SiC switches used in **Publications I–IV** are given in the device datasheets provided by the manufacturer (Wolfspeed, 2016), and are defined as a function of the switched current I_{sw}. In the case of the 1200 V SiC switches, the energies are defined for two voltage levels of 800 VDC and 600 VDC, whereas in the case of the 900 VDC SiC switches, the energies are defined for 600 VDC and 400 VDC. Because it is not trivial to accurately read the curves visually from the datasheet images, a bitmap reader was written in a MATLAB® and then used to import the curves. Polynomial third-order fits were then generated in MATLAB® to represent the relationship between I_{sw} and E_{tot}, E_{on}, and E_{off}. The generated models for E_{tot} as a function of I_{sw} are depicted in Figure 3.6.

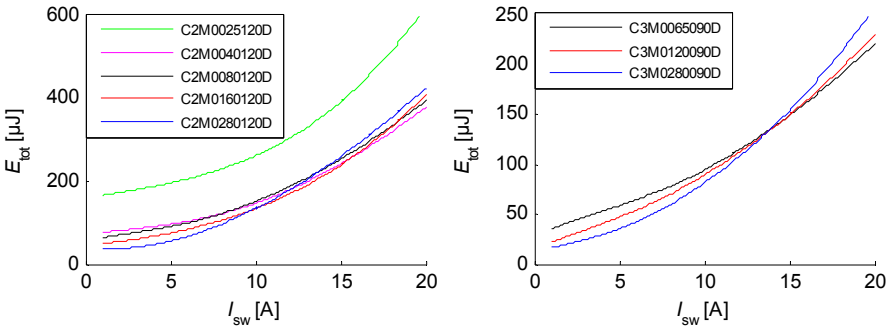

Figure 3.6 Third-order polynomial fits for E_{tot} as a function of the switched current I_{sw} for 1200 V SiC switches (left graph), and 900 V SiC switches (right graph). In the case of the 1200 V switches, the models were generated from the 800 V curves of the datasheet, whereas the 400 V curves were used in the case of the 900 V switches.

As can be seen in Figure 3.6, the value of E_{tot} increases as a function of I_{sw}, but also as a function of silicon area, which is inversely proportional to the $R_{ds,on}$ of the switch. The value of the $R_{ds,on}$ of each switch is indicated in the name of the switch so that for example

in the case of C2M0**280**0120D, the value of $R_{ds,on}$ = 280 mΩ. However, as the value of I_{sw} increases to 10 A and above, the switches with $R_{ds,on}$ < 280 mΩ begin to take over one by one. It is to be noted that the curves for the 1200 V switch CAS120M12BM2 were purposely left out of the graph of Figure 3.6 because of the significant differences in the E_{tot} values (> 1000 µJ) but are available in (Wolfspeed, 2016). Because no curves for the studied voltage levels of 750 VDC and 400 VDC were given in the datasheet for the 1200 V SiC switches, the switching energies for these two voltage levels were calculated by

$$E_{tot,U_{calc}} = E_{tot,800V} \frac{U_{calc}}{800}, \tag{3.27}$$

where U_{calc} is the voltage to which the switching energy is being scaled to, and $E_{tot,800V}$ is the switching energy for a voltage level of 800 V as defined in Figure 3.6. It is pointed out that the relationship between E_{tot} and V_{DS} is not necessarily linear, but owing to the lack of data at V_{DS} = 400 VDC for the 1200 V switches, this approach was selected. Owing to the significant price differences between the 1200 V and 650–900 V switches, the error in the calculated switching losses of the 1200 V switches at V_{DS} = 400 VDC should be considerably underestimated for it to affect the component selection at this input voltage level. Comparing the result of (3.27) with the 600 V curves given in the datasheets of the 1200 V switches, the result of (3.27) overestimates the values by 0–20% rather than underestimates them. Therefore, the expression of (3.27) cannot be thought of as a major error source considering the resulting CEI design at V_{DS} = 400 VDC.

In **Publication IV**, 650 V GaN semiconductor switches (GaN Systems, 2016) were also used in the calculations. However, curves for the relationship between I_{sw} and E_{tot} were not provided in the datasheets of these devices, whereas the values of E_{on} and E_{off} were given only at a single current value. Therefore, the switching instants were simulated in Orcad Pspice using the device models provided by the manufacturer (GaN Systems, 2016) and a double pulse circuit. Models for the switching energies E_{tot}, E_{on}, and E_{off} as a function of I_{sw} were then formulated using third-order polynomial curve fits as was also done in the case of the SiC switches. The generated models for E_{tot} as a function of I_{sw} are depicted in Figure 3.7.

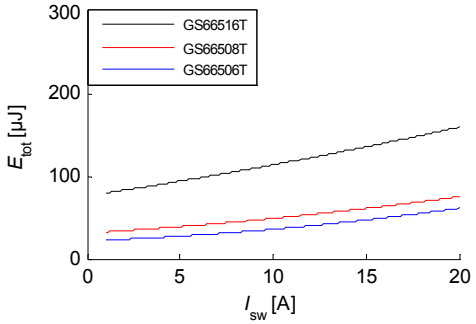

Figure 3.7 Third-order polynomial fits for E_{tot} as a function of the switched current I_{sw} for 650 V GaN switches. The curves are defined for U_{DC} = 400 V.

If we compare the curves of the GaN switches in Figure 3.7 with the curves of the 900 V SiC switches in Figure 3.6, which are defined for the same switched voltage U_{DC}, we can see that the curves of the GaN switches behave more linearly as a function of I_{sw}. Therefore, comparing switches with a similar value of the $R_{ds,on}$, such as GS66508T and C3M0065090D, we can see that the differences in E_{tot} at $I_{sw} < 5$ A are only in tens of percentages, whereas the E_{tot} of the GaN switch is only a third of the E_{tot} of the SiC switch when $I_{sw} = 20$ A potentially bringing significant advantages in terms of selecting a higher switching frequency.

To reduce the complexity of the switching loss analysis and the required computation time, the calculation of the switching loss of an inverter outputting a sinusoidal waveform can be simplified by using the average switched current during a line cycle instead of the actual switched current at each switching instant (Infineon, 2006). When the MOSFET reverse conduction is utilized during the zero-stage, the average current of a single switch of an H-bridge can be calculated by

$$I_{avg} = \frac{2}{\pi} I_m. \tag{3.28}$$

The switching loss of a single switch is then calculated by

$$P_{sw} = f_{sw} E_{tot}(I_{avg}, U_{DC}), \tag{3.29}$$

where E_{tot} is defined as a function of I_{avg} and U_{DC}. However, even though the expression of (3.28) simplifies the analysis, it also introduces some amount of error in the result especially if the value of E_{tot} is not linearly proportional to I_{sw}. Improved accuracy can be obtained by sampling the sinusoidal output current at the switching frequency and by calculating the time-average power loss. However, as already discussed in Section 3.2.2 and in (Nge, 2009), we also have to consider the effect of the ripple current if satisfactory estimation of the power loss under light load is desired. As discussed in the previous chapter, the ripple factor RF was varied between 5% and 30% in the analysis of **Publication IV.** High values for the ripple current can result in significant differences between the sinusoidal output current and the actual value of the switched current thus potentially producing an error in the calculated losses if the effect of the ripple was not considered.

In the case of the H-bridge inverter, the peak-to-peak value of the ripple current in the inductor can be calculated by

$$\Delta i_{pp}(\omega t) = \frac{U_{DC}}{2Lf_{sw}} (1 - M\sin(\omega t)) M\sin(\omega t), \tag{3.30}$$

where $0 < \omega t < \pi$ (Kim, 2008). The magnitude of the inductor current can then be calculated by

$$I_{ind}(\omega t) = \sqrt{2} I_{out} \sin(\omega t) \pm \frac{\Delta i_{pp}(\omega t)}{2}. \tag{3.31}$$

During the positive half cycle of the line current, one pair of switches in the H-bridge turns on at the peak of the inductor current and turns off at the valley of the inductor current, whereas another pair of switches turns on at the valley of the inductor current and turns off at the peak of the inductor current. The order is then reversed during the negative half-cycle. To illustrate the differences between the actual switched currents and the sinusoidal output current, the inverter was simulated in Simulink®; the simulated waveforms of the inductor current and the output current are depicted in Figure 3.8 at two different load values of 20% and 100% of P_{nom}.

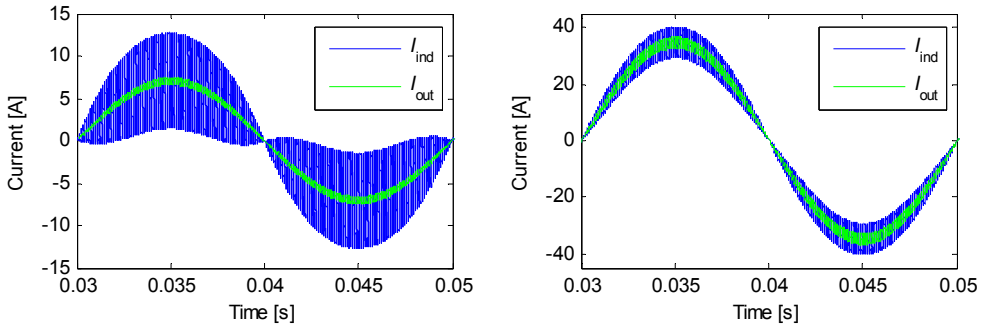

Figure 3.8 Simulated inductor and load current waveforms at 20% (left graph) and 100% (right graph) load, whereas the value of the ripple factor was set to $RF = 10\%$. Simulation parameters are $U_{\text{DC}} = 750$ V, $f_{\text{sw}} = 20$ kHz, and sampling time $t_{\text{s}} = 0.05$ µs.

As can be seen in Figure 3.8, the minimum and maximum values of the ripple current, which represent the switched currents, differ significantly from the value of the load current during partial load, whereas the difference is not as significant at the nominal load. Based on Figure 2.3, most of the energy is being supplied at load values ≤ 30% of P_{nom}, and therefore, it can be concluded that the effect of the ripple current should be taken into account not only when calculating the conduction losses but also when calculating the switching loss. The unfortunate drawback of calculating the switching loss by sampling the current at each switching instant is, however, that despite its higher accuracy, a higher number of calculations is required, whereas the calculation effort is directly proportional to the value of the switching frequency f_{sw}. Therefore, the sampled approach is not very ideal considering an optimization routine in which the switching loss might have to be calculated several times increasing the time that it takes to minimize the problem. Nevertheless, if we consider the fact that $f_{\text{sw}} >> 50$ Hz, we can see that the difference in the switched current I_{sw} of consecutive switching instants, being either consecutive peaks or valleys of the inductor current, can be relatively minor. Therefore, an option of calculating the time-average switching loss by sampling only a part of the output current was considered as this could potentially reduce the calculation effort quite significantly. The time-average switching loss using a number of m samples can be calculated by

$$P_{\text{sw}} = \frac{f_{\text{sw}}}{2m} \sum_{n=1}^{m} \begin{pmatrix} E_{\text{on}}\left(\left|I_{\text{ind,pk},n}\right|, V_{\text{DS}}\right) + E_{\text{off}}\left(\left|I_{\text{ind,v},n}\right|, V_{\text{DS}}\right) \\ + E_{\text{on}}\left(\left|\mathrm{I}_{\text{ind,v},n}\right|, V_{\text{DS}}\right) + E_{\text{off}}\left(\left|I_{\text{ind,pk},n}\right|, V_{\text{DS}}\right) \end{pmatrix}, \tag{3.32}$$

where $I_{\mathrm{ind,pk},n}$ is the peak of the inductor current at the nth sampled switching instant and $I_{\mathrm{ind,v},n}$ is the valley of the inductor current at the nth sampled switching instant. As can be seen in Figure 3.8, the positive and negative half cycles are mirror images of each other, and thus, we only need to sample the positive half cycle. Therefore, the values of E_{on} and E_{off} appear twice in (3.32), whereas the sum is divided by $2m$. The calculation error using a number of $m = 20$ samples instead of using all the switching instants in the time-average switching loss calculation is depicted in Figure 3.9. The resulting calculation error as a function of output current when the simplified expression of (3.28) for the switched current I_{sw} is used in the time-average switching loss calculation instead of using all the switching instants is also shown in Figure 3.9.

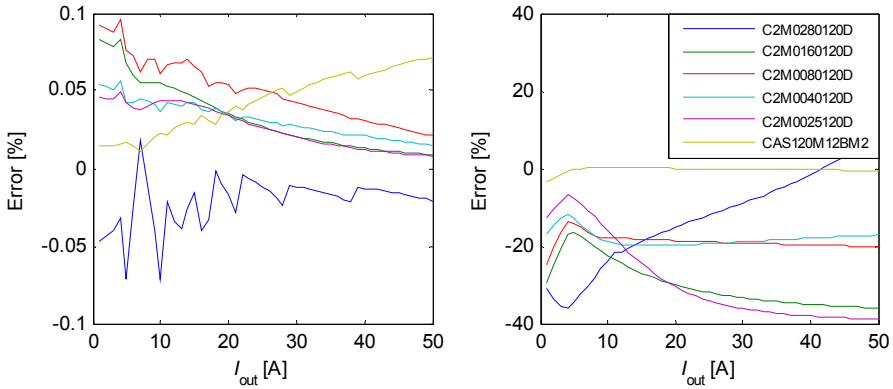

Figure 3.9 Comparison of the resulting calculation error as a function of output current when the time-average switching loss is calculated using $m = 20$ samples of a half cycle instead of using all the switching instants (left graph), and the resulting calculation error as a function of output current when the simplified expression 3.28 for the switched current is used in the time-average switching loss calculation instead of using all the switching instants (right graph). The examples were calculated using parameters $f_{\mathrm{sw}} = 20$ kHz, and $RF = 10\%$.

As can be seen in the left graph of Figure 3.9, using only a number of $m = 20$ samples of the half cycle in the time-average switching loss calculation instead of all the switching instants results in an error of only < 0.1% with all the six transistors used in the example. The results are very similar up to the values of $RF = 30\%$ and $f_{\mathrm{sw}} = 100$ kHz, which are the maximum values considered in this dissertation. Therefore, it can be concluded that the proposed simplification can be used in the calculation of the switching loss without impacting the result. However, looking at the right graph of Figure 3.9, which depicts the resulting error when using the simplified expression of (3.28), it can be concluded that using this type of a simplification can lead to significant deviations in the calculated switching loss if the switching energy curves are not linear, whereas relatively high accuracy can still be achieved with a linear switching energy curve. An example of the relatively small error with a linear switching energy curve can be seen in the result for the switch CAS120M12BM2, which has a very linear relationship between I_{sw} and E_{tot}. An error of less than 10% can still be achieved with the rest of the switches when using the simplified expression of (3.28) if $I_{\mathrm{out}} < 10$ A and $RF < 5\%$. Based on the analysis, the sampled approach using a number of $m = 20$ samples was selected for the calculations of

Publication IV, whereas the simplified expression of (3.28) was used in the calculations of **Publication II**.

To calculate the switching losses of the two DC-DC converter topologies discussed in **Publication III**, we first need to define the conditions for ZVS. The switches are operated under ZVS when

$$\frac{1}{2} I_{\mathrm{sw}}^2 L \geq \sum \frac{1}{2} C_{\mathrm{oss}} V_{\mathrm{DS}}^2, \tag{3.33}$$

where I_{sw} is the turn-off current of the opposite switch, L is the inductance related to the ZVS operation in the circuit, C_{oss} the output capacitance of a single switch, and V_{DS} the voltage across the switch when the switch is in the off-state (Kheraluwala, 1992), (Hiltunen, 2015). In the case of the PSFBVD topology, a certain amount of freewheeling time is required to operate the primary-side lagging leg switches under ZVS. In **Publication III**, the required freewheeling time was determined based on the values of the magnetizing inductance L_{mag}, the magnetizing current I_{mag}, and the time-related output capacitance $C_{\mathrm{oss(tr)}}$ of the switches. The value of I_{mag} was assumed to linearly increase and decrease, and be constant during the ZVS transition similar to (Lee, 2008). The maximum value of the effective duty cycle D_{eff} was then calculated as a function of f_{sw} and $C_{\mathrm{oss(tr)}}$, so that the ZVS condition is always met. The LC resonance was tuned to be identical to the effective duty cycle D_{eff} and therefore, the value of I_{sw} is identical to the value of I_{mag} at the switching instant. The switching losses of the PSFBVD can then be calculated by

$$P_{\mathrm{sw}} = f_{\mathrm{sw}} E_{\mathrm{off}}(I_{\mathrm{sw}}, U_{\mathrm{DC}}), \tag{3.34}$$

where I_{sw} is the value of I_{mag} at the switching instant. In **Publication III**, the voltage conversion ratio of the DAB was assumed to be at its nominal value, and therefore, the value of I_{sw} for all the switches is identical to $|i_{L,0}|$ and can be calculated using (3.23). Because the value of the phase-shift φ in (3.23) changes as a function of the load, it means that the value of I_{sw}, and as a result, the switching losses of the DAB are also load dependent. The value of I_{sw} also depends on the fluctuations of the conversion ratio of the converter, but because the conversion ratio was assumed to be at its nominal value, the effect was not included in the calculations of **Publication III**. If the conversion ratio is assumed to vary, we also need to define $i_L(t)$ at $t = T/2$ because of the resulting difference in the switched current compared with the time instant $t = 0$. The value of $i_L(t)$ at $t = T/2$ can be calculated by (Krismer, 2010)

$$i_{L,\frac{T}{2}} = i_{L,T_\varphi} + \frac{(V_1 - nV_2)\left(\frac{T}{2} - T_\varphi\right)}{L}. \tag{3.35}$$

When the inequality of (3.33) is fulfilled, the switching losses of the DAB can be calculated using (3.34). However, during partial load, the value of I_{sw} gradually decreases and depending on the values of L, C_{oss}, and V_{DS}, the inequality of (3.33) is no longer met. As a result, the converter will operate under hard switching and the switching losses have to be calculated by

$$P_{sw} = \left(E_{on}(I_{sw},V_{DS}) + E_{off}(I_{sw},V_{DS})\right)f_{sw}, \tag{3.36}$$

which also includes the turn-on switching loss due to E_{on}. In addition to the switching loss caused by E_{on} and E_{off}, some amount of power is consumed by the driving of the gate of the transistor. The average gate driving power consumed by a single switch can be calculated by

$$P_{gate} = Q_g V_g f_{sw}, \tag{3.37}$$

where Q_g is the gate charge, and V_g is the gate driving voltage. The value of P_{gate} is typically significantly lower compared with the switching loss caused by E_{tot} in a hard switched case and is likely to have a negligible effect on the calculated losses.

3.3 Magnetics

The magnetics design part of this doctoral dissertation includes the inductor of the output LC filter of the inverter stage of the CEI, and the high frequency (high frequency being tens to hundreds of kHz) isolation transformer of the isolated DC-DC converter stage, which supplies the inverter stage and isolates the customer-end network from the DC network side. Compared with the previous analysis of the power stage, the design of the magnetic components requires more effort as the design process contains a higher number of design variables and thus, a higher number of feasible solutions for the final design. Instead of choosing ready-made components off-the-shelf as was done in the case of the power stage semiconductors and heat sinks, the magnetic components are designed by searching for a combination of an inductor core, and winding wire that does not violate any constraints, and at the same time, results in the minimization of the objective function of (3.3). In the case of the inductor of the LC filter, core material, inductance and air gap length are also considered as variables, whereas the inductance is varied as a function of full winding turns.

3.3.1 Output LC filter of the inverter stage

An extensive explanation of the design constraints, variables, equations, and methodology for the CEI output LC filter is given in **Publication I**. **Publication II** extends the filter analysis of **Publication I** to incorporate the option of paralleling the CEI modules and also adds another magnetic material to the analysis. In **Publication IV**, the loss calculations are updated from the ones used in **Publications I** and **II** to include more accurate evaluation of the core and copper losses. Because the methodology was significantly improved between the writing of the publications, the explanation of the filter calculation as used in **Publication IV** is repeated here for completeness. First, the main constraints for the filter design are introduced, followed by the main design equations and variables. Because two different magnetic materials and core geometries were used in the calculations of **Publications II** and **IV**, the material and geometry-specific factors affecting the design are also discussed. The windings of the inductor are

assumed to be arranged so that the stray flux from the air gap does not significantly affect the AC resistance of the winding and thus, also the copper loss.

The basic constraints affecting the LC filter inductor are the saturation flux density B_{max} of the magnetic material of the inductor core, the window area W_a, and the maximum temperature $T_{max,ind}$ of the inductor. A value of $T_{max,ind} = 80$ °C was used in the calculations of **Publication I**, **II**, and **IV**, whereas the same value of $T_{amb} = 50$ °C as in the power stage analysis was used for the ambient temperature. As previously discussed, a target value of a maximum of 5% for the output voltage THD of the CEI was set in (Partanen et al., 2010). The same value was also used as a constraint in the calculations of **Publications I**, **II** and **IV**. To meet the THD requirement, the cut-off frequency of the LC filter has to be chosen so that the f_{sw} related harmonics are reduced to a sufficient level, whereas the cut-off frequency of the LC filter is defined by

$$f_c = \frac{1}{2\pi\sqrt{LC}}. \tag{3.38}$$

In this doctoral dissertation, the voltage THD definition for the CEI output covers the first 50 Hz harmonics as defined in the standard EN50160 (SFS, 2010) as well as three switching-frequency-induced harmonic groups near the frequencies $2f_{sw}$, $4f_{sw}$, and $8f_{sw}$ as found in the Fourier analysis of the output voltage. The THD is then calculated by

$$THD_U = \frac{\sqrt{\sum U_{h,n}^2}}{U_{out}}, \tag{3.39}$$

where $U_{h,n}$ is the RMS value of the nth harmonic voltage and U_{out} the output voltage at the fundamental frequency. An example of the simulated output voltage harmonic content of the CEI inverter stage is depicted in **Figure 3.10**.

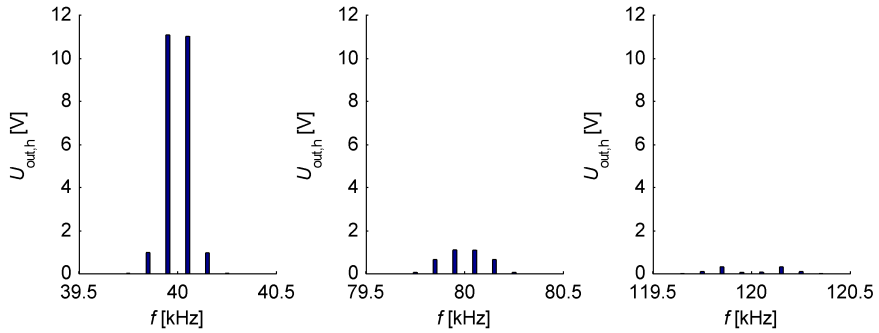

Figure 3.10 Example simulation of the CEI inverter stage output voltage harmonic content using simulation parameters $U_{DC} = 750$ VDC, $f_{sw} = 20$ kHz, $L = 380$ µH, $C = 1$ µF, and sampling time $t_s = 0.1$ µs.

As can be seen in Figure 3.10, the second-order slope of the LC filter effectively reduces the high-order harmonics of f_{sw} and therefore, considering only the three first f_{sw} related

harmonic groups in addition to the low-order 50 Hz harmonics will result in a sufficient estimation of the output voltage THD.

The nominal power P_{nom} of the CEI module, f_{sw}, the inductance L of the inductor, the inductor core material, the core model, the number of turns N, the airgap length l_{ag}, and the winding wire diameter d are considered as the main design variables. While the capacitance C of the filter can also be taken as a variable, the design process is carried out by using the value of L as the main variable and solving (3.38) for C, whereas f_{c} in (3.38) changes as a function of f_{sw}. The values of f_{sw} = 10–100 kHz were considered in **Publications I**–**II**, and **IV**. Typically, the manufacturers of inductor cores give a variable A_{L}, which describes how the resulting value of L of a finished inductor behaves as a function of N, in the datasheet. The A_{L} value is often also given as a function of l_{ag} as in (Hitachi Metals, 2012b), (TDK, 2016). However, in some cases, no information about the relationship between l_{ag} and A_{L} is available or the information is limited. The designer might also want to consider the option of stacking several smaller cores to produce the finished inductor instead of using a larger core as the pricing of the cores with different sizes does not necessarily behave in a linear manner as a function of core volume. When the size and geometry of the air gap changes, the information regarding the A_{L} value of a single core is no longer valid. In such a case, the 3D approach proposed in (Mühlethaler, 2011) can be used to determine the A_{L} value for different air gap geometries. The method has been empirically proven to provide a high accuracy compared with the "classical method", in which the fringing flux is not taken into account, or the more typical 2D method that uses a simplified approximation of the fringing effect.

The A_{L} value can be used to calculate the inductance of a wound inductor by

$$L = A_{\mathrm{L}} N^2. \tag{3.40}$$

The maximum value of N is limited by the constraint W_{a}, whereas the window fill W_{fill} is a function of N and the cross-sectional area of the winding wire A_{w}, and is calculated by

$$W_{\mathrm{fill}} = \frac{NKA_{\mathrm{w}}}{W_{\mathrm{a}}}, \tag{3.41}$$

where K is the fill factor of the winding wire. In this work and **Publications I**, **II**, and **IV**, only round winding wires are considered, and a value of $K = 0.6$ is used in the calculations. N is also limited by B_{max}, whereas the flux density of the inductor can be calculated by

$$B = \frac{NI}{A_{\mathrm{c}}} A_{\mathrm{L}}, \tag{3.42}$$

where A_{c} is the cross-section of the inductor core. To accurately determine the peak flux $\hat{B}$ in the inductor, we also have to include the ripple current in the value of I in (3.42). In the case of the H-bridge inverter, the peak-to-peak value of the ripple current in the inductor can be calculated using (3.30). The magnitude of the inductor current can then

be calculated by (3.31). As can be seen from (3.30), the amplitude of the ripple is dependent on the modulation index M and changes as a function of time t. Therefore, with high values of Δi_{pp}, the peak current of the inductor $\hat{I}_{ind}$ does not necessarily occur at the peak of the sinusoidal output current $\hat{I}_{out}$ of the inverter when $M > 0.5$. This has to be checked separately to avoid saturating the core in case the optimized design were to favor a very low value of L, and therefore, a high value of Δi_{pp}. To show how varying the ripple factor RF affects the amplitude of the inductor current at the nominal load, the amplitude of the inductor current at different values of RF is depicted in Figure 3.11.

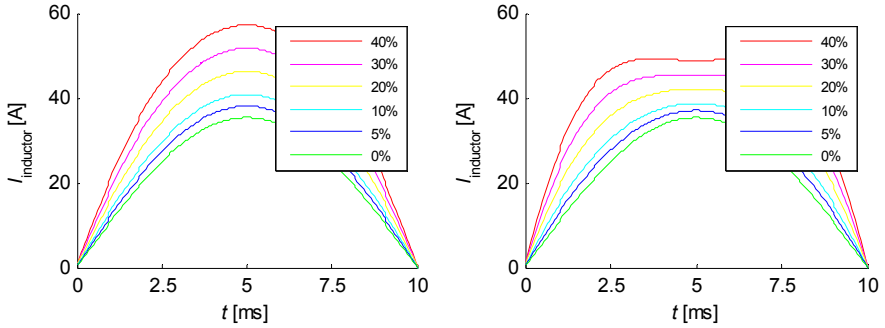

Figure 3.11 Effect of the inductor ripple current factor RF on the inductor current value at the nominal load $P_{nom,1p}$ = 5.75 kW, when U_{DC} = 750 V (left graph) and U_{DC} = 400 V (right graph), and RF is varied between 0% and 40% of I_{out}.

In **Publication IV**, the effect of the ripple factor limit RF_{lim} on the life cycle cost of the CEI was analyzed in the range of 5–30% of I_{out} using two input voltage levels of 400 VDC and 750 VDC. As can be seen in Figure 3.11, the peak value of I_{ind} for both voltage levels occurs at the peak of the sinusoidal output current, and no extra measures are required up to a value of RF = 30%. However, if values of RF > 30% were allowed in the design when U_{DC} = 400 V, the value of $\hat{I}_{ind}$ would no longer occur at the peak of the sinusoidal output, and should be calculated by solving the maximum of (3.31). As mentioned in **Publication IV**, it is emphasized that the value of RF should not be increased considerably because a part of the ripple current will begin to flow to the customer network if a highly capacitive load is connected, and the limit for the current THD might be exceeded. If the inverter is implemented with a grid-side inductor instead, the value of RF can naturally be increased even further as the grid-side inductor will limit the amount of ripple current that can flow to the customer network.

In **Publication I**, only a single magnetic material, namely amorphous alloy 2605SA1 (Hitachi Metal, 2012a), was used in the example calculations. The selection of the material was based on its suitability for the required power levels and values of f_{sw}, the availability of the necessary data to carry out the research (Hitachi Metal, 2012a), (Hitachi Metal, 2012b), and the findings in the previous research by the coauthors (Peltoniemi, 2008). However, during the writing of **Publication II**, which extended the analysis to include significantly lower values of P_{nom} because of the inclusion of the parallel CEI modules, it was noted that the smallest core model from the line-up of

(Hitachi Metals, 2012a) was selected as the optimum. In other words, the design of the inductor began to saturate as an even smaller core was no longer available in the input library. Therefore, it was decided that another magnetic material, more suitable for lower power levels, should also be included in the analysis to determine whether the inductor design could be optimized even further. Similar to the reasons why the amorphous alloy was selected for **Publication I**, a line-up of N87 ferrite ETD cores from TDK (TDK, 2016) was selected as the second material. A comparison of the main parameters of the two materials, 2605SA1 and N87, is presented in Table 3.1.

Table 3.1 Comparison of the main properties of the two magnetic materials, namely amorphous alloy 2605SA1 and ferrite N87, used in **Publications II** and **IV**. The A_L range is defined based on the datasheet information for gapped cores. The average price is calculated for 1000 quantities of the available core models.

	2605SA1	N87
B_{max} at 100 °C [T]	1.5	0.39
P_{core} [W/kg]	~15 (100 mT, 25 kHz)	~3 (100 mT 25 kHz)
A_L range [μH/N^2]	0.082–3.006	0.124–0.525
Mass [g]	99–7109	28–260
Avg. price [€/kg]	~27	~20

Looking at Table 3.1, we can see that the main properties of the two materials, 2605SA1 and N87, differ considerably from each other. The amorphous alloy 2605SA1 has a significantly higher B_{max} and this in combination with large core sizes makes it more suitable for higher power levels. On the other hand, the losses of the N87 ferrite are only a fraction of the losses of the amorphous alloy 2605SA1 making it suitable for higher values of f_{sw} and f_{sw} related ΔB if high power levels are not required.

To calculate the losses of the inductor, definitions for the core loss and copper loss are required. The manufacturers of magnetic materials typically include a simple formula for the core loss, which is defined by

$$P_{core} = k f^{\alpha} B^{\beta}, \tag{3.43}$$

where k, α, and β are parameters found by curve fitting against measured losses of the magnetic material. Because a similar equation without the frequency dependence was proposed by Steinmetz (Steinmetz, 1892), the expression of (3.43) is typically referred to as the Steinmetz equation (Venkatachalam, 2002) and parameters k, α, and β as the Steinmetz parameters (Mühlethaler, 2012). In **Publications I**–**III**, the core losses of the different magnetic components were calculated using (3.43). As mentioned in **Publication I**, though, (3.43) is only valid for sinusoidal excitations, and therefore, some deviation is expected in PWM converter calculations because the waveforms are not sinusoidal. Therefore, it was decided that a more sophisticated core loss calculation method would be used for the calculations of **Publication IV**. To overcome the limitations of (3.43), several alternative methods, such as the Modified Steinmetz Expression (MSE) (Reinert, 2001), General Steinmetz Equation (GSE) (Li, 2001),

Improved Generalized Steinmetz Equation (iGSE) (Venkatachalam, 2002), Equivalent Elliptical Loop (EEL) (Lin, 2004), Natural Steinmetz Extension (NSE) (Van den Bossche, 2004), Waveform coefficient Steinmetz Equation (WcSE) (Shen, 2006), and Improved Improved General Steinmetz Equation (i^2GSE) (Mühlethaler, 2012) have been proposed. In all of the above methods, the original Steinmetz coefficients k, α, and β, typically provided in the manufacturer datasheet, are used in the calculation. Moreover, the i^2GSE method requires additional parameters, which have to be determined by making measurements on the material in question (Mühlethaler, 2012). A comparison of the MSE, GSE, iGSE, EEL, NSE, and WcSE methods was carried out in (Villar, 2009). The results in (Villar, 2009) show that among the modified methods, the iGSE and MSE provide the best estimate of the core loss under nonsinusoidal excitation. The iGSE method, however, copes better with different waveforms and is consistent with (3.43) for sinusoidal waveforms (Villar, 2009). Although the i^2GSE method proposed in (Mühlethaler, 2012) is able to calculate the core loss more accurately compared with the iGSE, especially when the duty cycle is very low or very high, the requirement for additional measurements makes this method more difficult to use in practice compared with the iGSE if the necessary equipment or the magnetic material under study is not easily available. Therefore, it was decided that a method not requiring additional measurements, in this case the iGSE method, would be used for the calculations of **Publication IV**.

The iGSE defines the expression for time-average loss in a magnetic material by

$$\overline{P}_{\mathrm{v}} = \frac{1}{T}\int_{0}^{T}\left|\frac{dB}{dt}\right|^{\alpha}(\Delta B)^{\beta-\alpha}dt, \tag{3.44}$$

where

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\theta|^{\alpha}2^{\beta-\alpha}d\theta}. \tag{3.45}$$

In the case of the CEI, the high-frequency component of the LC filter inductor is triangular and the expression of (3.44) reduces to

$$P_{\mathrm{v}} = \frac{k_i}{T}\left(DT\left(\frac{\Delta B}{DT}\right)^{\alpha}(\Delta B)^{\beta-\alpha} + (1-D)T\left(\frac{\Delta B}{(1-D)T}\right)^{\alpha}(\Delta B)^{\beta-\alpha}\right), \tag{3.46}$$

where T is the switching period, and D is the duty cycle of the triangle wave. D is defined by

$$D = M\sin(\omega t). \tag{3.47}$$

The ith value of D in the case of a full-bridge inverter over a half cycle of the sinusoidal 50 Hz output is calculated by

$$D_i = M\sin\left(\frac{\omega i}{2f_{\mathrm{sw}}}\right), \quad i = 1,2,3\ldots 2T_{\mathrm{s}}f_{\mathrm{sw}}, \tag{3.48}$$

where T_s is the period of a half cycle, in this case 10 milliseconds. The value of ΔB in (3.46) can be calculated by first solving Δi_{pp} by using (3.30) and (3.48), and then calculating B by using (3.42). The result of (3.46) is calculated at every switching instant over a half cycle, and the average power loss is then calculated by

$$P_{v,avg} = \sum_i P_{v,i} \frac{T}{T_s}, \tag{3.49}$$

where $P_{v,i}$ is the value of the ith instantaneous power loss during a switching instant (Venkatachlam, 2012). The Steinmetz parameters k, α, and β in (3.45) and (3.46) are typically given in manufacturer datasheets as was the case for the amorphous alloy 2605SA1. Nevertheless, even though the manufacturer of the N87 ferrite also defines the values of k, α, and β in their specifications, the parameters are a function of B, f, and the core temperature T_{core}. Because the core loss has to be evaluated at different values of B and f, a definition for k, α, and β as a function of B and f is required. To simplify the analysis, it was decided that a fixed value of T_{core} = 60 °C, corresponding to an estimate of the average inductor temperature, would be used in the calculations. If the actual temperature were to deviate from the estimate, a lower temperature would result in an increase in the core loss, whereas a higher temperature up to the selected maximum temperature of $T_{max,ind}$ = 80 °C would result in lower losses. Based on the manufacturer data (TDK, 2015), the value of α is a function of B and does not depend on the value of f, whereas the value of β is a function f and does not depend on the value of B. However, k changes as a function of both f and B. A MATLAB® interpolation function interp1, with the 'linear' method, was used to interpolate the values α and β, whereas the 'spline' method was used for k. The core loss density calculated using the interpolated values for k, α, and β as a function of B and f is depicted in Figure 3.12. As can be seen in Figure 3.12, the calculated values for the core loss density P_{vsin} using the interpolated values for k, α, and β well correspond to the manufacturer data.

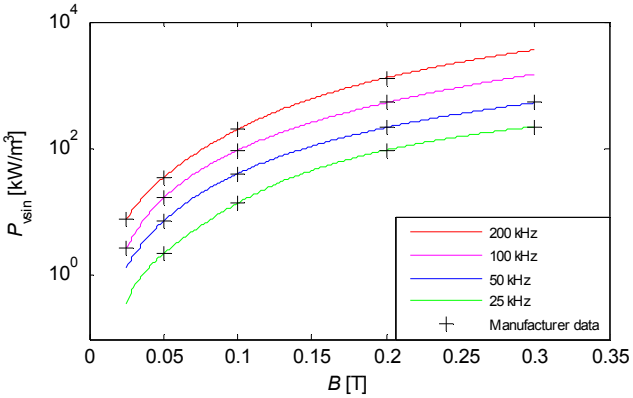

Figure 3.12 Core loss density P_{vsin} as a function of B with different values of f for the N87 ferrite calculated by using interpolated values for k, α, and β.

The copper loss of the winding consists of two parts, the high-frequency loss caused by the switching-frequency-induced high-frequency currents, and the low-frequency loss

caused by the 50 Hz load current. Because winding wires with only small diameters of 1–6 mm were included in the analysis, the copper loss caused by the 50 Hz load current can be calculated using the DC resistance of the winding. However, because the switching-frequency-induced high-frequency currents no longer use the whole cross-sectional area of the selected winding wires, the power loss has to be calculated by using the AC resistance of the winding. Whereas the calculations of **Publications I** and **II** only considered the skin effect, in **Publication IV**, the AC resistance of the winding is calculated by using the AC-to-DC winding resistance ratio, which takes into account both the skin and proximity effects, and is defined by

$$F_{\mathrm{R}} = \frac{R_{\mathrm{w}}}{R_{\mathrm{w,DC}}} = A\left[\frac{\sinh(2A)+\sin(2A)}{\cosh(2A)-\cos(2A)} + \frac{2\left(N_{\mathrm{l}}^2-1\right)}{3}\frac{\sinh(A)-\sin(A)}{\cosh(A)+\cos(A)}\right], \tag{3.50}$$

where R_{w} is the AC resistance of a solid round wire, $R_{\mathrm{w,DC}}$ is the DC resistance of a solid round wire, N_{l} is the number of the winding layers, and A is the effective cross-sectional area of the winding wire (Wojda, 2013). The DC resistance of a solid round wire is calculated by

$$R_{\mathrm{w,DC}} = \frac{4\rho N \cdot MLT}{\pi d^2}, \tag{3.51}$$

where ρ is the resistivity of the conductor, N is the number of turns in the winding, MLT is the mean length turn, and d is the diameter of the wire. In the case of the AMCC C-cores, MLT is defined as

$$MLT = 2(a + 2b + d), \tag{3.52}$$

where a, b and d are different dimensions of the core and are given in (Hitachi Metals, 2012a). In the case of the ferrite ETD core and the ferrite PM core, MLT is calculated by

$$MLT = \frac{\pi(d_1+d_2)}{2}, \tag{3.53}$$

where d_1 is the diameter of the center leg, and d_2 is the distance between the outer legs of the core. The effective cross-sectional area A in (3.50) is defined by

$$A = \left(\frac{\pi}{4}\right)^{0.75}\frac{d}{\delta_{\mathrm{w}}}\sqrt{\eta}, \tag{3.54}$$

where δ_{w} is the skin depth of the wire, and η is the porosity factor (Wojda, 2013). The skin depth δ_{w} in (3.54) is calculated by

$$\delta_{\mathrm{w}} = \sqrt{\frac{\rho}{\pi\mu_0 f}}, \tag{3.55}$$

where μ_0 is the permeability of free space. Because the resistivity ρ is typically given at a temperature of 20 °C but varies as a function of the temperature, the values of ρ in (3.51) and (3.55) were multiplied by

$$T_{\text{mult}} = 1 + \alpha(T_{\text{calc}} - 20), \tag{3.56}$$

where α is the temperature coefficient of the winding material. The porosity factor η in (3.54) is defined by

$$\eta = \frac{d}{p}, \tag{3.57}$$

where p is the distance between adjacent conductors (Wojda, 2013). The power loss in the inductor winding can then be calculated as a sum of the low- and high-frequency loss components by

$$P_{\text{wire}} = R_{\text{w,DC}} I_{\text{out}}^2 + \sum_{n=1}^{3} R_{\text{w,DC}} F_{\text{R},n} I_{\text{h},n}^2, \tag{3.58}$$

where $F_{\text{R},n}$ is the AC-to-DC winding resistance ratio of the wire at the nth harmonic frequency, and $I_{\text{h},n}$ the RMS current at the nth harmonic frequency of f_{sw}.

In this doctoral dissertation and in **Publications I**, **II**, and **IV**, the switching-frequency-related harmonic currents $I_{\text{h},n}$ in the LC filter inductor were calculated using a model for the relationship between the values of f_{sw}, L, and $I_{\text{h},n}$. The model was generated by carrying out simulations on an H-bridge inverter circuit and calculating the FFT spectrum from the resulting current waveform. An example of the harmonic content of the current waveform in the LC filter inductor is depicted in Figure 3.13.

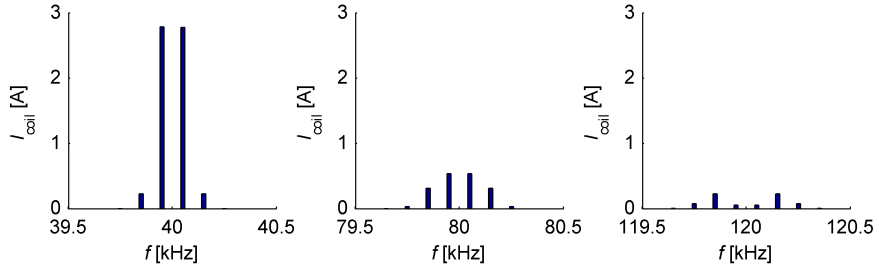

Figure 3.13 Simulated harmonic current content in the LC filter inductor with simulation parameters U_{DC} = 750 V, f_{sw} = 20 kHz, L = 380 µH, C = 1 µF, and sampling time t_{s} = 0.1 µs.

As can be seen in Figure 3.13, the harmonics appear as sidebands near the frequencies

$$f_{\text{h}} = 2nf_{\text{sw}}, \quad n = 1,2,3\ldots m. \tag{3.59}$$

Because the RMS value of the harmonics quickly decreases after n = 2, only the three first harmonic groups, that is, n = 1–3 in (3.59), were included in the analysis of the high-frequency-related copper loss in the inductor winding. Even though the values of the higher-order harmonics, n > 3, increase inversely proportionally to L, the first two to three

harmonic groups dominate the resulting total high-frequency RMS current, and therefore, also the high-frequency-related copper loss. The values of $I_{h,n}$ were simulated while varying the values of L and C. The value of the cut-off frequency f_c of the LC filter was kept at a fixed value, which was selected as a function of f_{sw} to meet the THD requirement of $THD_U \leq 5\%$, which was discussed in Section 3.1. Because the difference in the frequencies between the sidebands inside a single harmonic group is insignificant compared with f_h and would result in nearly identical AC resistances, the models for $I_{h,n}$ were defined for the RMS sum (cf. e.g. (3.14)) of the values of the harmonic sidebands inside a harmonic group near a single frequency f_h as defined by (3.59). The models are defined by

$$I_{h,n} = a(f_{sw},n)L^{b(f_{sw},n)}, \quad n = 1,2,3, \tag{3.60}$$

where a and b are the model coefficients defined as a function of f_{sw} and n.

The temperature rise of the inductor was evaluated based on the equation provided by the manufacturer, which is defined by

$$T_{ind} = T_{amb} + \left(\frac{P_{tot,ind}}{SA}\right)^{0.833}, \tag{3.61}$$

where $P_{tot,ind}$ is the total power loss of the inductor in milliwatts, and SA is the total dissipation surface area of the inductor in square centimeters (Metglas, 2009), (Magnetics, 2013). A value of $T_{ind,max} = 80$ °C was used as a constraint for the design. As previously mentioned, the resistivity ρ of the winding material depends on the temperature and thus, the inductor temperature T_{ind} is calculated using an iterative process, which is described in more detail in Section 3.5. Because of the added complexity to the calculations, the variation in the core loss of ferrite as a function of temperature is not considered in the iteration, but instead, the losses are calculated using a fixed value of $T_{core} = 60$ °C. However, if we compare the values of $T_{ind,max} = 80$ °C and $T_{amb} = 50$ °C with the behavior of the core loss as a function of temperature, in the worst case, this simplification will slightly overestimate the core loss rather than underestimate it.

3.3.2 Isolation transformer of the isolated DC-DC converter stage

As discussed in Chapter 1, the calculation of the isolation transformer in **Publications I** and **III** was implemented as an extension to a transformer calculation algorithm written by one of the coauthors of **Publications I** and **III**. The algorithm calculates the AC resistances of the litz wire windings in the transformer with the option of interleaving or paralleling the windings, the power loss of the transformer at a fixed power level, and the values of the leakage inductance L_{lk} and magnetizing inductance L_{mag}, and selects the optimum winding based on the minimization of the winding losses. The reader can refer to the original work in (Väisänen, 2012) and (Väisänen, 2013) for a more detailed description of the methodology applied in the original algorithm.

To accommodate the work required for **Publications I** and **III,** the algorithm was modified to include the necessary evaluations of the different costs of the isolated DC-DC converter and the calculation of the losses and their cost when the converter is supplying a residential customer having a load profile discussed in Section 2.1. The selection of the winding configuration was also changed so that the winding and the winding–core combination is selected based on the minimization of the life cycle cost instead of the minimization of the losses. Further, the algorithm was extended to evaluate different converter designs, in this case the PSFBVD and the DAB, whereas in the case of the DAB also the different combinations of half and full bridges on both sides of the transformer were considered as discussed in **Publication III**.

Similar to the analysis carried out on the LC filter, the definitions for the RMS currents in the transformer are required for the winding loss calculation, whereas the definitions for the calculations of the various losses of the power stages can be found in Sections 3.2.2 and 3.2.3. In the case of the PSFBVD topology, the definition for the RMS current in the transformer winding is similar to (3.21) and is calculated by (Väisänen, 2012)

$$I_{\mathrm{RMS,PSFBVD,T}} = \sqrt{\frac{2}{T}\int_0^{\sqrt{L_{\mathrm{lk}}C_{\mathrm{r}}}\pi}\left(n\frac{\omega_{\mathrm{r}}I_{\mathrm{out}}}{2}\sin(\omega t)\right)^2 dt}. \tag{3.62}$$

Selecting the value of n to be either $n_{\mathrm{sec}}/n_{\mathrm{pri}}$ or $n_{\mathrm{pri}}/n_{\mathrm{sec}}$ defines whether the value of $I_{\mathrm{RMS,PSFBVD}}$ is calculated for the primary side or for the secondary side. In the case of the DAB and the basic phase shift modulation, the definition for the primary-side RMS current in the transformer winding is similar to (3.22) and is calculated by

$$I_{\mathrm{RMS,DAB,T}} = \sqrt{\frac{2}{T}\left(\begin{array}{c}\int_0^{T_\varphi}\left(i_{L,0}\frac{V_1+V_2}{L}\right)^2 dt + \\ \int_{T_\varphi}^{\frac{T}{2}}\left(i_{L,T_\varphi}\frac{(V_1-nV_2)(t-T_\varphi)}{L}\right)^2 dt\end{array}\right)}. \tag{3.63}$$

The secondary-side RMS current can be calculated by multiplying the result of (3.63) by the turn ratio $n_{\mathrm{pri}}/n_{\mathrm{sec}}$ of the transformer. Again, even though the RMS current derivations for a limited number of topologies are presented, the RMS current for any given topology and current waveform can be derived using (3.26). The value of L_{lk} for (3.62) and (3.63) is calculated by

$$L_{\mathrm{lk}} = \frac{\mu_0 N^2 l_{\mathrm{w}}}{P^2 h_{\mathrm{w}}}\left(\frac{1}{3}\sum_{p=1}^{2P} h_p + \sum_{i=1}^{P} h_i\right) \tag{3.64}$$

where N is the number of turns in the winding, l_{w} is the winding length, P is the number of primary-secondary intersections, h_{w} is the winding width, h_{p} is the height of the pth winding portion, and h_{i} is the height of the ith primary-secondary insulation layer (Väisänen, 2012). In **Publications I** and **III**, the interleaving of the primary-secondary windings was not considered as this would have unnecessarily complicated the analysis

without significantly improving the outcome considering the scope of the study. However, because of the analyzed conversion ratios of 1:1 and 2:1, a maximum of two parallel winding wires on the secondary side were considered in the calculations.

In **Publication III**, some of the evaluated DAB designs required a high value of leakage inductance, which was not easily achieved using only the leakage of the transformer itself. Therefore, additional external inductors were also designed. In such cases, the total leakage inductance $L_{lk,tot}$ was formed by the sum of the leakage of the transformer L_{lk} and the inductance of the external inductor L_{ext}. The external inductors were designed using a similar methodology for the litz wire as in the transformer case by altering the transformer algorithm to calculate an inductor instead of a transformer. Because the external inductor is connected in series with the transformer primary, the RMS current in the inductor can also be calculated by (3.63), whereas the value of B for the core loss calculation can be calculated by (3.42).

A selection of litz wires with strand diameters of 18–52 AWG and a number of 1–11250 strands (HMWire, 2015) were used as the input library for the winding wire of the transformer of both DC-DC topologies and the external inductor of the DAB. Ungapped N97 ETD and N87 PM ferrite cores (TDK, 2016) were used for the transformer calculations, whereas gapped N87 ETD ferrite cores (TDK, 2016) were used in the calculations for the external inductor of the DAB.

3.4 Price data

In order to carry out the necessary calculations for the life cycle cost of the CEI, we also have to define the price data for the evaluation of C_{inv} and C_{loss} in the objective function of (3.3). The price data required for C_{loss} are the price of electricity $C_{e.}$ A value of C_e = 40 €/MWh was used in the calculations as it well represents an average market price for electricity in Finland in the past five to ten years (Nord Pool, 2016). Nevertheless, because the electricity price can be considered as one of the main variables affecting the result, the effect of a higher electricity price of C_e = 80 €/MWh was also included in the calculations.

For $C_{inv,}$ the prices of the various components of the CEI have to be defined. As discussed in Chapter 1, the analysis of this dissertation was limited to the main power electronic components of the CEI. The main power electronic components are the main semiconductors, the gate drivers, the heat sink, the LC filter, the DC capacitance, and the isolation transformer. The price data for the main semiconductors, the heat sinks, the different types of filter cores that were used in the LC filter and the isolation transformer, and the solid round wires that were used in the LC filter are given in Appendix A: Price data. Most of the price data were gathered from sources (Digikey, 2015), (Farnell, 2015), (Mouser, 2015a), (Mouser, 2015b), (TME, 2015), (Wires, 2015), whereas prices for the amorphous cores were obtained from a magnetic part supplier. Because price data were not easily obtained for the huge litz wire database, which was used in the calculations of the isolation transformer and the DAB inductor in **Publications I** and **III**, the price of the

litz wire was estimated using the amount of copper in the winding and the price of copper per ton (LME, 2015). The gate driver cost was estimated based on the price of a gate driver IC and the price of an isolated low voltage DC-DC converter (Farnell, 2015), (Digikey, 2015), (Mouser, 2015a). A value of 15–16.9 €, depending on the date of the reference publication, was used for the total cost of the gate driver for a single H-bridge. Because of the high uncertainty in the component price data, especially when compared with high-volume pricing if the CEI were to be mass produced, the sensitivity of the final result on the component prices was analyzed in **Publications II–IV** by calculating an additional set of results using 50% discounted prices for all the components.

3.5 Description of the calculation algorithm

In order to solve the optimization problem of (3.3), several calculation algorithms were formulated in MATLAB® and used to calculate the results presented in **Publications I–IV**. The objective of the dissertation was not to generate or find the most mathematically effective solver for the problem, and thus, comparisons of different types of solvers were not included in the work. However, because the target of the optimization is a physical device, technical understanding of the problem was effectively used to reduce the amount of calculation points. Therefore, the calculation effort and the time required for the algorithm to minimize the problem could be significantly reduced despite the high number of the possible designs that can be designed as a combination of the input variables. A simplified flowchart of the algorithm of the inverter stage optimization as used in **Publication IV** is depicted in Figure 3.14. The calculation begins in a main function, where the user can input the desired values for the input voltage U_{DC}, the switching frequency f_{sw}, the total nominal power P_{max} of the three phases, the number of the parallel modules n, the overload current I_{over}, the ripple factor upper limit RF_{lim}, the CEI unit replacement interval t_{rep}, the utilization time t_u, and the price of electricity C_e. The input variables f_{sw}, n, RF_{lim}, and I_{over} are handled as vectors, and therefore, several alternative values can be given as inputs and are automatically considered in the calculation. The algorithm then loads the necessary input libraries, namely the load profile data, magnetic core data, winding wire data, semiconductor data, and heat sink data. If desired, the user can also select among several alternative customer load profiles and then define a suitable value for the annual energy consumption E for the load profile in question. After the input data have been loaded, the algorithm enters a subfunction that handles the power stage calculations. The subfunction begins by selecting the first semiconductor switch from the semiconductor library. At this point, the value of the ripple factor RF is handled as 0.1 A increments between 0.1 A and RF_{lim} to avoid calculating the semiconductor database with all the possible inductor designs and the exact value of RF that can potentially vary with increments as small as the 16-decimal resolution of MATLAB®, which is not of particular interest. We then calculate the power losses of the semiconductors at the nominal load P_{nom} and the overload situation, if present, by using (3.19), (3.16), and (3.32). Next, we must determine whether it is possible to cool down the semiconductor with a realistic heat sink. If the constraint $T_{j,max}$ is already violated

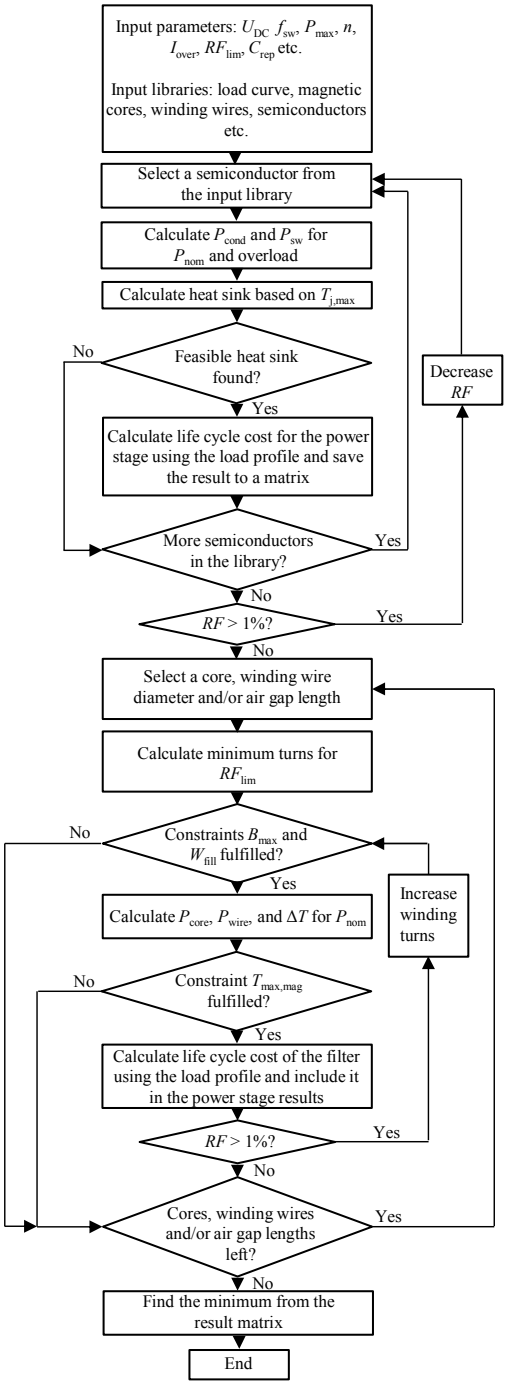

Figure 3.14 Simplified flowchart of the basic principle of the calculation. If the user inputs a number of i alternative values for U_{DC}, f_{sw}, n, I_{over}, and RF_{lim}, the flowchart is run i times.

inside the semiconductor packaging or an unrealistic heat sink is required to cool the semiconductor, we move on to the next higher-rated component in the database until a feasible combination of a semiconductor and a heat sink is found, whereas (3.7)–(3.11) are used in the thermal dimensioning. The heat sinks are handled using a variable step size for $R_{th,hs}$ to reduce the calculation effort especially when calculating the transient thermal properties, whereas the step sizes are determined based on Figure 3.3. For each feasible design that does not violate any constraints, the value of RF is looped from 0.1 A to $RF_{lim,}$ whereas the life cycle cost is calculated by using (3.3) (without the *min* term) and saved into a matrix. When no feasible combinations are left in the database, the algorithm exits the function and returns the result matrix into the main function that is responsible for calculating the filter parameters.

The main function continues the calculation by selecting the first magnetic core, the shortest air gap length l_{ag}, and winding wire diameter from the database. The minimum inductance to meet the RF_{lim} requirement is then calculated by solving (3.17) for L, whereas the value of $I_{ripple,ind}$ in (3.17) is replaced by RF_{lim} multiplied by the output current RMS value. The minimum number of turns required for L with the core and air gap length in question is then calculated by solving (3.40) for N. After this, the constraints for B_{max} and W_{fill} are checked for violations by first calculating the value of B by using (3.42) and W_{fill} by (3.41). If a violation occurs, the algorithm moves on to the next combination of N, magnetic core, l_{ag}, and the winding wire diameter until a feasible combination is found. The power losses and temperature rise at the nominal load are calculated by using (3.44)–(3.61) for all the designs fulfilling the constraints B_{max} and W_{fill}. Because of the temperature sensitivity of the copper resistivity ρ, the temperature of the inductor T_{ind} is calculated using an iterative process, in which T_{ind} is assumed to be 1 °C over the ambient temperature T_{amb} at the start of the iteration. After each iteration we arrive at a new value for T_{ind} and calculate ρ and copper loss at this new temperature for the next iteration. After the difference in T_{ind} between consecutive iterations has satisfied a user-defined error margin, the algorithm decides that it has converged and stops the iteration. If the calculated temperature exceeds the value of $T_{ind,max}$ after ten iterations, the calculation is stopped, the inductor design in question is tagged as nonfeasible, and the algorithm moves on to the next design. After the constraint $T_{ind,max}$ is also fulfilled, the life cycle cost for the filter design in question is calculated and added to the power stage life cycle cost by first rounding the actual value of RF of the inductor design to the nearest 0.1 A increment and then selecting the corresponding result from the semiconductor result matrix. By doing this, the semiconductor function has to be run only once and the amount of calculation effort is significantly reduced while not impacting the accuracy of the result. For example, if the current increment is decreased from 0.1 A to 0.01 A, the difference in the calculated life cycle costs is less than 0.2%. However, the current increment is user-definable and can, therefore, be made even smaller at the cost of computation time if desired. After the life cycle costs for all the feasible designs have been calculated, the matrix containing the feasible results is minimized and the algorithm prints out and saves the design parameters that result in the minimization of (3.3). All the feasible designs are also saved and thus, enable further analysis of the feasible designs near the optimal solution.

A similar algorithm without the variables $I_{over,}$ RF, and RF_{lim} was used in **Publication II**, and without the semiconductor and heat-sink-related variables in **Publication I**. The inverter stage calculation algorithm contains approximately 3500 lines of MATLAB® code, out of which 70% are related to the magnetics design. The algorithm is able to minimize the optimization problem of (3.3) in 3–15 minutes, depending on the user defined input variables, using a computer equipped with a core i7-3770 processor and 16 GB of RAM when the initial design space contains 1.5–3.1 billion possible solutions for the design. The initial design space is a combination of 24 magnetic cores, ten air gap lengths, a maximum of 200 winding turns, eleven winding wire diameters, six values for the switching frequency, 6–12 different semiconductor switches (depending on the value of U_{DC}), and 81 heat sinks, which are defined either in the input libraries or in the user-defined input vectors. In reality, the heat sink thermal resistance $R_{th,hs}$ can have an infinite number of values when the calculation is carried out for the nominal power of the CEI, but the iterative process used in the overload dimensioning is limited to 81 values as a result of the variable step size. The time that it takes to minimize the problem depends on the user-defined input variables, because for example the number of the feasible designs can be significantly higher when no overload requirement is defined or when the value of RF_{lim} is set to a higher value, for instance from 5% to 30%. The size of the input library is also larger when $U_{DC} = 400$ V. In the course of developing the algorithm, the MATLAB® profiler was extensively used to find the parts of the code that consume the highest amount of CPU time. Alternative solutions that can be run faster were then implemented to reduce the total calculation time. For example, vector multiplication is used where applicable to avoid the usage of 'for' loops as much as possible, whereas the power stage subfunction is executed using a parallel pool with four workers. In its current form, the most time-consuming part of the algorithm is the switching loss calculation, as it samples the current waveform and uses the third-order fit coefficients to calculate the switching energies E_{on} and E_{off} as a function of switched current. Because the losses are calculated for the whole load profile, the routine has to be executed 8760 times for each feasible design. The calculation of the core loss is also a somewhat time-consuming process as sampling of the inductor waveform is required. Although both operations are carried out analytically, the high number of the required calculations significantly increases the execution time, whereas the CPU time consumed by the rest of the code is negligible.

4 Summary of the appended publications and their key results

This chapter gives a summary of the objectives and key results of the four appended publications that constitute Part II of this doctoral dissertation.

4.1 Publication I

The first publication, entitled "*Galvanic Isolation and Output LC Filter Design for the Low-Voltage DC Customer-End Inverter*" is organized into two parts. In the first part, two distinct solutions for the implementation of the galvanic isolation between the AC and DC networks, namely a 50 Hz transformer placed on the output side of the CEI and an isolated DC-DC converter placed on the input side of the CEI, are compared. Based on calorimetric measurements conducted with a system using the former solution, the minimum requirements for the isolated DC-DC converter are described. Replacing the 50 Hz transformer with an isolated DC-DC converter should result in a reduction in the life cycle cost for the system to be cost effective.

The publication concludes that potential improvements can be achieved if the designs of the galvanic isolation and the output filter are optimized. Replacing the 50 Hz isolation transformer with an isolated DC-DC converter shows high potential in terms of loss minimization and increased power density. Based on calorimetric measurements, the 50 Hz transformer was shown to have high no-load losses, and as a result the efficiency during a typical load cycle can be very low. Based on the calculated results, the isolated DC-DC converter analyzed in the publication was shown to have lower no-load losses, and therefore, the efficiency during a typical load cycle can be significantly higher compared with the 50 Hz isolation transformer.

In the second part of the publication, a design method for an LC filter that is based on the minimization of the life cycle cost is presented. The analysis is carried out using C-cores made of amorphous alloy, whereas solid round copper winding wire is used for the winding. The effect of the main design parameters such as the input DC voltage level, the selection of the switching frequency, and the nominal current on the life cycle cost and the filter design are analyzed. Requirements such as the output voltage quality, saturation of the inductor core, and the maximum temperature of the inductor are used as constraints for the design, whereas parameters such as inductance, capacitance, diameter of the winding wire, core size, and air gap length are freed in the design process. Among the possible combinations of the different variables, a design resulting in the minimization of the life cycle cost and fulfilling all the constraints is selected as the optimum solution.

The input DC voltage level is found to have the highest effect on the resulting life cycle cost of the output LC filter. By increasing the switching frequency of the CEI, the cost of the filter is found to decrease to a certain level, after which the cost begins to increase due to the exponential relationship between core loss and frequency. Calculating the filter

using a reduced electricity price showed only a minor effect on the resulting parameters when a value of t_u = 10 years is used as the utilization period.

4.2 Publication II

The second publication, entitled "*Life-Cycle Cost Analysis for the Customer-End Inverter Used in Low Voltage DC Distribution*" extends the life cycle cost analysis carried out on the LC filter in **Publication I** to include the rest of the inverter power stage of the CEI. In addition to the LC filter components, the semiconductor switches, the gate drivers, the DC capacitance, and the heat sink are included in the analysis. An option of connecting several low-power CEI modules in parallel instead of one high-power CEI module is also considered. In the analysis, the modules are switched on and off depending on the load value. Partly because the filter results in **Publication I** show no significant advantages when the switching frequency is increased beyond 40 kHz and partly because of the inclusion of the low-power parallel modules, the filter calculations are extended to include another magnetic material, in this case ferrite, to determine whether the life cycle cost could be further reduced as a function of switching frequency and power level of a single module. Compared with the analysis conducted in **Publication I**, an additional load profile representing a different type of a customer is introduced, and life-cycle-cost-minimized CEIs for both types of customers are designed. The resulting CEIs and their life cycle costs are compared with each other to determine whether the customer type has an effect on the design. The results are calculated for two input DC voltage levels of 750 VDC and 400 VDC.

The publication concludes that in most of the studied cases, a single high-powered CEI module per phase results in the lowest life cycle cost. However, in some cases the cost difference between two parallel modules and a single high-powered module per phase was almost negligible. Even though the calculations were done using state-of-the-art SiC switches, the cost of the switching losses during the utilization period was found to be a significant factor of the life cycle cost and limited the selection of the switching frequency to relatively low values. Life cycle costs relative to either the nominal power or the delivered energy of the CEIs for both types of customers were found to be very similar despite the significant differences in the load behavior and the nominal power rating.

4.3 Publication III

The third publication, entitled "*Evaluation of Isolated Converter Topologies for Low Voltage DC Distribution*", compares two isolated DC-DC converter topologies for the implementation of the galvanic isolation in the DC network. Two fundamentally different topologies, namely the PSFBVD and the DAB, are selected for the analysis to determine which of the two approaches would result in the minimization of the life cycle cost. The fundamental properties of the topologies are discussed and their problems and advantages are compared. The topologies are then designed and analyzed for two voltage conversion ratios of 1:1 and 2:1 that result in output voltage levels of 750 VDC and 400 VDC to

complement the input voltage levels of the CEI in **Publication II**. In the case of the DAB, the primary- and secondary-side bridges can be implemented either using half bridges, full bridges, or a combination of both, and therefore, all the possible combinations of the two bridges are included in the analysis. Similar to the analysis conducted in **Publication II**, the option of connecting several converter modules in parallel instead of a single high-powered module is considered, whereas only the minimum amount of parallel modules is switched on depending on the load value. The selection of the switching frequency of the converter and its effect on the life cycle cost is also analyzed.

The publication concludes that of the two studied topologies, the PSFBVD topology results in the lowest life cycle cost with the input parameters used in the analysis. Changing the conversion ratio of the converter from 1:1 to 2:1, and thereby, the output voltage from 750 VDC to 400 VDC results in a 2–9% increase in the life cycle cost depending on the topology, whereas the PSFBVD results in the minimum cost in both cases. Even though the DAB requires a relatively high value of the leakage inductance with the studied application parameters and in most cases results in the usage of an external inductor, the inductor is not found to be a significant factor in the life cycle cost of the converter. Based on the results, the PSFBVD or a similar topology seems to be a good candidate for the application if bidirectional power flow and output voltage regulation are not required. However, if both of these properties are set as requirements, a compromise regarding the life cycle cost might be necessary and the selection will lean towards a topology such as the DAB.

4.4 Publication IV

The fourth and final publication included in this doctoral dissertation is entitled "*Design of Customer-End Converter Systems for Low Voltage DC Distribution from a Life Cycle Cost Perspective*". The publication extends the analyses of **Publication I** and **Publication II** to incorporate the requirements defined by the protection devices that are used at the electrical installations on the customer's premises. In the case of a short-circuit fault at the customer-end installation, the CEI is required to supply a high amount of current far exceeding its nominal rating in order to trip the protection devices in the trip times set in the relevant standards (SFS, 2008), (SFS, 2012). Because the maximum duration of the short-circuit is relatively short, the transient thermal properties of the CEI are included in the analysis. Similar to **Publication II**, the power stage components and the LC filter are included in the calculations, whereas additional SiC and GaN switches that have been released since the writing of **Publication II** were also entered in the input libraries. Load profiles representing two different types of customers are used in the loss calculation similar to **Publication II**. The loss calculations are updated to incorporate more accurate methods for the calculation of the inductor core loss, the winding conduction loss, and the power stage semiconductor losses. Compared with **Publications I–III**, the utilization period is extended to 40 years, which is a typical value in distribution network analyses (Partanen, 2002), (Willis, 2004). Because a power electronic converter is not expected to operate for such a long period without some kind of a failure and is

likely required to be replaced at least once during the utilization period, a value of 20 years is selected for the expected lifetime of the converter after which it is replaced with an identical one. The cost for the replacement unit is calculated using the present value. Similar to **Publications II–III**, two input voltage levels of 400 VDC and 750 VDC are considered in the calculations.

The conclusions of the publication are that using the load behavior of actual customers is clearly beneficial if the target is to minimize the life cycle cost of a converter used to supply a residential customer. Significant differences in the resulting converter designs were observed when averaged load profiles of residential customers were used as an input for the design process compared with a case in which the optimization was carried out using only the rated power of the converter even though the rated power was the same in both cases. When the objective function is set to minimize the life cycle cost of a customer-end inverter, a preference for relatively low values of the switching frequency, and relatively high values of inductance in the output LC filter is observed even when the current state-of-the-art SiC and GaN switches are used as the input for the calculations. Even though the material cost of the output filter could be further reduced by increasing the switching frequency, the cost of the additional switching losses during the utilization period is found to outweigh the benefit in the studied application.

When the electricity price is assumed to be 40 €/MWh and component prices are based on 1000 quantities, the resulting design of the CEI for a 20 MWh customer with electrical heating is found to be nearly identical to the design of the CEI for a 9 MWh customer having some other heating system. Therefore, a similar CEI structure could be used to supply both customers without major drawbacks. In the case of the 9 MWh customer, however, the energy efficiency will be somewhat lower compared with the 20 MWh customer as a result of the higher unbalance between the nominal power of the CEI and the actual load. Even though the energy efficiency in the case of the 9 MWh customer could be increased by altering the design of the CEI, it can be cost prohibitive because the loss-related cost is not as significant. Instead, if the electricity price is assumed to be 80 €/MWh or the components can be bought at least 50% cheaper compared with the 1000 quantities as a result of volume pricing, investments toward increased energy efficiency can be profitable in the case of both customer types.

On average, the results for the input voltage level of 400 VDC show an increase in the life cycle cost of the CEI compared with the cases with an input voltage of 750 VDC. On the other hand, if no overloading of the converter is required, the result for 400 VDC shows a reduction in cost compared with the result for 750 VDC. Because a significantly higher amount of DC capacitance is needed to suppress the DC voltage ripple when the input voltage level is 400 VDC instead of 750 VDC, the cost increases especially in the cases in which overload capability is required. Nonetheless, the energy efficiency of the 400 VDC designs is found to be 1% higher on average compared with the 750 VDC designs, whereas the increase is notably larger in the case of the 9 MWh customer.

Based on the results, the primary factor affecting the life cycle cost of the CEI is the substantial overdimensioning if required either by the protection devices on the customer's premises or by the dynamic properties of some of the typical loads. However, some of the drawbacks resulting from the overdimensioning such as an increase in the cost or low energy efficiency can, at least to some extent, be mitigated by using parallel modules of a lower nominal power instead of a single high-powered module.

5 Conclusions

In this doctoral dissertation, a life-cycle-cost-driven design methodology of power electronic converters was investigated, whereas the emphasis was laid on the design of customer-end converters in an LVDC system supplying residential customers. Because the LVDC system is considered to be part of the distribution network, in which the decisive factor for feasibility is the life cycle cost, the different cost factors have to be taken into account when evaluating whether a particular converter design is optimal or not. In the dissertation, the investment costs of the main power electronic components of the converter, the cost of the converter losses during a typical utilization period, and the cost of a replacement converter unit were taken into account. Unlike the typical analyses conducted for power electronic converters in which the losses are considered as the power loss at a certain output power level, the dissertation addressed the losses as lost energy and its monetary value during the utilization period and when using a typical load cycle. The behavior of an average residential customer was used as one of the inputs for the design process, and therefore, a detailed analysis of the load was carried out. The main power stage components of the customer-end converter such as the output filtering, isolation transformer, semiconductor switches, heat sink, gate drivers, and DC link capacitance were included in the analysis, whereas their parameters were freed in the optimization process. The selection of the main design parameters such as switching frequency and nominal power were also addressed. Because the protection devices on the customer's premises set demanding requirements for a power electronic converter, the impact of meeting these requirements on the design of the converter and its life cycle cost was investigated. The option of using several parallel converter modules of lower nominal power instead of a single high-powered module was also considered in the analysis to determine whether a decentralized structure of the converter could solve some of the challenges posed by either the requirements of the load or the protection devices.

It was shown that it is clearly beneficial to use the load behavior of residential customers as one of the inputs in the design phase of a customer-end converter if the target is to find a cost optimal design. Significant differences in the resulting converter designs were observed when averaged load profiles of residential customers were used as an input for the design process compared with a case in which the optimization was made using only the rated power of the converter even though the rated power was the same in both cases. When the objective function was set to minimize the life cycle cost of a hard-switched customer-end inverter, a preference for relatively low values of f_{sw} and relatively high values of inductance in the output LC filter was observed. Even though the current industry trend is to push the switching frequencies to increasingly higher levels to decrease the size of the output filtering and as a result the physical size and weight of the converters, the results of the dissertation showed that the cost of the additional switching losses over the utilization period can outweigh these advantages in the studied application. Based on the results calculated for two different types of residential customers having significant differences in their annual energy consumption and electricity usage profile, a similar design of the customer-end inverter could be used to

supply a variety of customers without major drawbacks. Even though the energy efficiency was shown to be lower in the case of the customer having a lower annual energy consumption, the required structural changes to the converter to increase the energy efficiency can be cost prohibitive. When the design requirements of the converter were extended to incorporate the requirements set by the protection devices at the customer-end installations, significant drawbacks such as up to fourfold cost and reduced energy efficiency were observed. It was shown, however, that both of these disadvantages can be, to some extent, mitigated if the customer-end converter is implemented as a decentralized unit consisting of multiple low-powered modules rather than a high-power centralized one.

In addition to the hard-switched inverter stage of the customer-end converter, the properties of two different types of isolated DC-DC converter topologies for the implementation of the galvanic isolation between the customer-end installation and the DC network were analyzed. Two fundamentally different topologies were considered in the analysis to determine whether a preference for a certain property in the converter could result in an advantage in the application under study. It was shown that the topology having a lower semiconductor count and lower switching losses resulted in the minimization of the life cycle cost. However, owing to some of the drawbacks of the cost optimal topology such as unidirectional power flow and unregulated output, it does not necessarily provide all the desired functionalities required in a smart grid environment. If some or all of these properties are set as requirements, a compromise has to be made between functionality and cost.

5.1 Generality of the results

Because the DC network was considered a voltage source in the analyses of this dissertation, the results can be generalized to different types of DC systems such as microgrids, in which electricity is being supplied to residential customers or a load that has similar properties to the load profiles presented in this dissertation. Even though the emphasis was put on the load behavior of a residential customer, the presented methodology can still be used in a different application if application-specific inputs such as the load profile is replaced. If a specific application does not have a cost related to the losses of the converter, one can simply set the cost term for the losses to zero in the objective function and effectively minimize the investment cost of the converter instead of its life cycle cost. In such a case, however, it may be preferable to have an additional constraint for the minimum desired efficiency to avoid anomalies in the results. Even though the volume of the converter was not considered in this dissertation, the input libraries used in the analyses also contain the dimensions of the different components. Therefore, if desired, the algorithm could easily be set to minimize the volume of the converter with small modifications.

5.2 Suggestions for future work

Because of the scope of this doctoral dissertation, the analysis was mainly done on a single converter topology and a single modulation method. Even though a limited analysis was also performed on two isolated DC-DC converter topologies, the effect of the over current supply during a short-circuit at the customer-end installation was not considered in this case. One of the two isolated DC-DC converter topologies can also be modulated using several different modulation methods, which can be applied to decrease the conduction losses and also to extend the ZVS region especially in the cases in which the voltage conversion ratio differs from its nominal value. Nevertheless, only a single modulation method was considered in the analysis of this dissertation. Therefore, several interesting research questions requiring further analysis have been identified.

In the case of the inverter stage, the analysis could be extended to include other basic topologies such as the three- and four-leg inverters. In this case, the effective switching frequency at the output is halved, which will potentially increase the cost of the output filtering compared with the case that was studied in this dissertation. The four-leg inverter will also require an additional inductor in the fourth inverter leg. On the other hand, the number of the power stage semiconductors decreases, which potentially decreases the semiconductor-related losses and cost. All the three phases of the inverter stage can also easily be supplied from the same intermediate circuit, which further simplifies the design. In the cases in which several inverter modules are connected in parallel, it would also be interesting to study how much the system cost can be decreased by interleaving the parallel modules. It has been shown in the literature that the filter size can be significantly decreased with this method, which can have a significant effect on the cost of the output filtering. Then again, some challenges are posed by the circulating currents between the interleaved modules and have to be taken account of either in the filter design or by altering the modulation.

In the past work related to the LVDC system, a relatively small effort has been put on analyzing the rectifier substation that was briefly introduced in the introduction part of this dissertation, and thus, several interesting research questions still remain. The rectifier substation on the research site is currently implemented using off-the-shelf components not designed for this application, and several drawbacks in terms of energy efficiency, physical size, and controllability were identified during the research, whereas some of the deficiencies have been remedied in a newer generation of the same components. However, even though effort could be put on further improving the off-the-shelf components by considering changes to their design, there also remains another interesting alternative, which introduces a replacement for the whole rectifier substation. Instead of combining a distribution transformer with a line converter, one could use an AC-DC multilevel converter, which is directly connected to the medium-voltage AC network. A similar solution, namely a solid state transformer, has already been researched worldwide, but the power and voltage levels in these analyses are typically not of interest or not applicable to the system considered in this dissertation, and thus, the results are not directly comparable.

While significant effort was put to implement the various calculation algorithms that were used in the analyses of this dissertation, room for improvement regarding the efficacy of the calculations still remain. The input libraries for the semiconductor parameters could be further improved by introducing more detailed data for the measured switching energies. As previously mentioned, some of the components lacked data at the analyzed voltage levels and some simplifications regarding the calculation of the switching energies had to be made.

The inductor calculations could be further improved to cover detailed calculations of the effect of the air gap stray flux on the winding AC resistance when the air gap is enclosed by the winding. Different types of winding wires, such as square, flat, foil, or litz, in addition to the round winding wires could be incorporated in the analysis. The thermal analysis can be further enhanced by using a resistor network to describe the heat exchange between the winding, core, and the air cooling the component as this will improve the accuracy in the cases in which the copper and core losses and surface areas are not of equal value.

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Appendix A: Price data

Table A.1 Price data for the semiconductor switches that were used in the calculations of **Publications II–IV.** Please note that the module CAS120M12BM2 contains two switches.

Part	quantity	unit price [€] (**II–III**)	unit price [€] (**IV**)
650 V GaN HEMT			
GS66506T	250	-	13.88
GS66508T	250	-	16.48
GS66516T	250	-	47.24
900 V SiC MOSFET			
C3M0065090D	250	-	8.89
C3M0120090D	250	-	5.73
C3M0280090D	250	-	3.09
1200 V SiC MOSFET			
CAS120M12BM2	1	340.52*	340.52*
C2M0025120D	250	63.08	63.08
C2M0040120D	250	30.36	30.36
C2M0080120D	250	14.83	14.83
C2M0160120D	250	7.42	7.42
C2M0280120D	250	4.82	4.82

Table A.2 Price data for the ferrite inductor and transformer cores that were used in the calculations of **Publications II–IV**

Part	quantity	set price
Ferrite		
ETD29 (**II–IV**)	1000	0.752
ETD34 (**II–IV**)	1000	0.95
ETD39 (**II–IV**)	1000	1.31
ETD44 (**II–IV**)	1000	1.89
ETD49 (**II–IV**)	1000	2.22
ETD54 (**II–IV**)	1000	3.56
ETD59 (**II–IV**)	1000	5.06
PM50 (**III**)	100	11.56
PM62 (**III**)	100	15.54
PM74 (**III**)	100	34.52
PM87 (**III**)	100	48.1
PM114 (**III**)	100	112.84

Table A.3 Price data for the amorphous inductor cores that were used in the calculations of **Publications I**, **II**, and **IV**. Prices for the core models not included in the quotes were interpolated based on the available price data as a function of the mass of the core.

Part	quantity	set price [€] (**I**)	set price [€] (**II**,**IV**)
AMCC4	1000	-	12
AMCC10	1000	-	14
AMCC25	1000	14.5	16
AMCC50	1000	18.8	20
AMCC100	1000	32.2	33
AMCC200	1000	38.5	-
AMCC250	1000	-	53
AMCC500	1000	-	77
AMCC1000	1000	-	158

Table A.4 Price data for the enamelled copper solid round winding wires when bought in 1 kg quantities. The data was used in the calculations of **Publications I**, **II**, and **IV**

wire diameter [mm]	price [€/m] (**I–II**)	price [€/m] (**IV**)
1	0.11	0.11
1.5	-	0.24
2	0.46	0.44
2.5	-	0.70
3	1.01	0.96
3.55	-	1.49
4	2.00	1.91
4.5	-	2.39
5	2.82	2.70
5.5	-	3.62
6	4.44	4.26

Table A.5 Price data for the heat sinks that were used in the calculations of **Publications II–IV**

Part	R_{th}	Quantity	Unit price [€]
Fischer Elektronik			
2*SK157/150	0.125	1	149.5
SK157/150	0.25	1	74.75
SK56/150	0.34	10	37.29
SK57/100	0.7	100	9.25
SK04/100	1.5	100	3.54
SK514	2.2	100	3.25
SK185-37	6.0	100	1.06
SK104-38	11	100	0.92
SK09-20	15	100	0.55

Publication I

Mattsson, A., Lana, A., Nuutinen, P., Väisänen, V., Peltoniemi, P., Kaipia, T., Silventoinen, P., and Partanen, J. (2014).

Galvanic Isolation and Output Filter Design for the Low-Voltage DC Customer-End Inverter

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Galvanic Isolation and Output LC Filter Design for the Low-Voltage DC Customer-End Inverter

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***Abstract*—In this paper the need for a better design of the galvanic isolation and the output filter inductor in the customer-end inverter (CEI) of the low voltage DC (LVDC) network is discussed. The galvanic isolation can be implemented either with a 50 Hz transformer after the CEI or with an isolated DC-DC converter between the DC network and the CEI. However, the 50 Hz transformer solution adds a significant amount of volume and mass to the system. Based on calorimetric measurements conducted with the current system in which the galvanic isolation is implemented with the former method, the minimum requirements for the isolated DC-DC converter are presented and a comparison is carried out. For the system to be cost efficient the DC-DC converter should result in reduced lifetime cost compared with the transformer solution. In the output filter part a design method for an amorphous core filter inductor based on minimization of the lifetime cost is presented.**

***Index Terms*—Converter, efficiency, inverter, LC filter, low voltage direct current (LVDC), output filter, power distribution.**

I. Introduction

THE LVDC system is an emerging power distribution technology under intense research and development globally. The LVDC power distribution has been proposed for various applications from datacenters [1] to public utility grid distribution [2]–[5]. The LVDC distribution research network [6] uses voltage levels of ± 750 VDC. The end-customers are connected to either between $+750$ VDC and 0 VDC or between -750 VDC and 0 VDC and the customer-end 50 Hz AC voltage of 230/400 $\mathrm{VAC_{RMS}}$ is produced using the customer-end inverter (CEI). The power demand in the user-end installations, and thus the load of the CEI varies in a wide range [7], which separates the distribution system application of inverters from the common industry applications.

Besides the inverter bridge topology and the semiconductor technology, the galvanic isolation and output filter play a significant role in the design and efficiency of the CEI. In this paper both of these issues are addressed. A design method for minimizing the lifetime cost of the output LC filter is presented and comparisons are carried out for different values of the DC network voltage, CEI switching frequency and the nominal current of the CEI to determine their effect on the design of the output filter.

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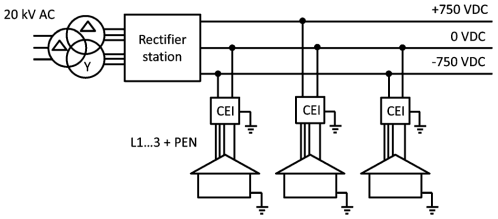

Fig. 1. Overview of the LVDC distribution network. The rectifier substation is connected to the 20 kV distribution network by a double-tier transformer Ddy5 connection. The DC network is an IT network and the CEIs have 50 Hz isolation transformers at the AC output to allow customer-end earthing owing to protection and safety regulations.

II. Galvanic Isolation

The system under study applies a functionally unearthed (IT) DC network. The customer-end AC network is a functionally earthed (TN) network and therefore, the two networks have to be galvanically isolated from each other. Overview of the LVDC distribution network is depicted in Fig. 1.

The galvanic isolation can be implemented either with a 50 Hz transformer at the customer-end AC-side after the CEI output filter or with an isolated DC-DC converter between the DC network and the CEI. In the latter configuration the same inverter bridge configuration cannot be used as the six-pack bridge does not provide a ground connection and only generates the three-phases that are further connected to the delta-configured transformer primary. Therefore, a virtual ground point should be implemented by changing the inverter DC capacitors to a series connected pair and then connecting the middle point of the two capacitors to the customer-end AC network ground. However, this will result in excessive values of the required DC capacitance as the power is transmitted through the capacitors in asymmetrical load conditions. The output filter capacitors should also be configured so that the capacitors are not connected between each phase but from phase to ground instead. Separate single-phase inverter bridges with individual DC-DC converters can also be used. In the sixpack configuration the minimum required DC-voltage level would be 565 VDC. In the separate single-phase converter-inverter configuration a

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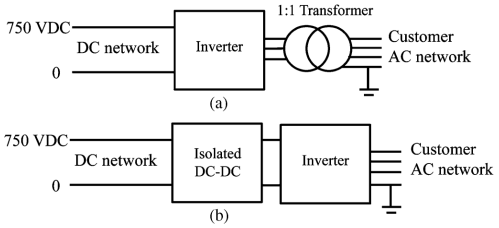

Fig. 2. Block diagram of the customer-end galvanic isolation: isolated with a 1:1 ratio 400 VAC 50 Hz transformer after the CEI (a) and with an isolated DC-DC converter (b).

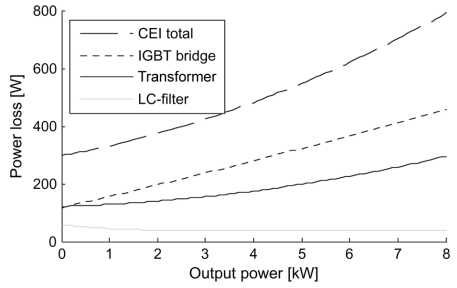

Fig. 3. Total losses and losses per component measured with a calorimeter for a 16 kVA nominal power CEI operated at a switching frequency of $f_{\mathrm{sw}} = 16\ \mathrm{kHz}$.

minimum of 325 VDC is required as the converter outputs are floating. Block diagrams for both of the isolation methods are depicted in Fig. 2.

The current field test platform [6] and the laboratory test setup have been implemented by applying the 50 Hz transformer solution. However, this adds a significant amount of volume and mass to the CEI. The transformer also contributes to a high percentage of the total losses of the CEI as shown by the calorimetric measurement results in Fig. 3.

To achieve a higher power density and a higher power to weight ratio a galvanically isolated DC-DC converter would be more feasible for the implementation of the galvanic isolation in the system. As a result the introduction of wide bandgap (WBG) switching devices utilizing Silicon Carbide (SiC) and Gallium Nitride (GaN), high efficiency power converter systems with high power densities can be constructed [8]–[11].

DC-DC converters have been studied in direct customer-end DC-distribution for datacenters and households for instance in [1], [12], [13]. Implementation of the galvanic isolation in the studied research platform with a DC-DC converter has also been proposed [14] and it will be the next step in the development of the system. In this paper a comparison of the characteristics against the 50 Hz transformer is carried out and the requirements for the isolating DC-DC converter are described.

A. Volume and Mass

The isolation transformer in the current system is a 400 V 1:1 ratio 16 kVA unit weighing in at 93 kg and measuring $42.5\ \mathrm{cm} \times 37.0\ \mathrm{cm} \times 18.5\ \mathrm{cm}$. The power density and power to weight ratio of the transformer are thus relatively poor. An isolated converter with a nominal power of 19.2 kW and a power density of 10 $\mathrm{W/cm^3}$ applying WBG devices was studied in [13]. The converter in [13] is designed for a voltage level of 384 VDC but the rating is reached by series-parallel connection of several 48 VDC modules. Therefore it would be feasible to configure it for a 750 VDC system by doubling the series connected modules and halving the paralleled modules while maintaining the power density and nominal power ratings.

The 16 kVA transformer has a power density of only 0.55 $\mathrm{W/cm^3}$ making the power density of the converter 18 times higher in comparison. Replacing the 16 kVA transformer with a converter solution would therefore result in a significant reduction of the CEI volume and mass.

B. Losses

As previously depicted in Fig. 3. the transformer contributes to a high percentage of the total CEI losses. However, Fig. 3. also shows that the IGBT bridge losses are even higher than the transformer losses and therefore a similar hard switching topology cannot be used in the isolated converter as a reduction in losses is required. The measured losses of the transformer set the requirement for the minimum efficiency of the isolated converter. This means that the efficiency of the converter should exceed the values of $\eta = 0.92$ at 10% load and $\eta = 0.96$ at 50% load.

The WBG devices would enable a significant increase in the switching frequency and thereby an increase in the converter power density as a result of the reduction of the passive component values and the size of the high-frequency transformer. A comparison of output inductor volumes when different switching frequencies are used is presented in [8] and [10].

In addition a ZVS switching scheme enables an increase in the switching frequency while retaining a high efficiency value. The ZVS resonance circuit requires a specific amount of added capacitance C_{r} and inductance L_{r} in the circuit depending on the transformer leakage inductance L_{s}, magnetization inductance L_{m}, winding capacitance C_{w}, and the switching component output capacitance C_{o}. However, instead of separate components the required values of C_{r} and L_{r} can be included in the transformer design to obtain equivalent values of L_{s}, L_{m} and C_{w} [15], [16].

Integration can also be taken even further in the form of integrated power electronic modules (IPEM). With the increasing switching frequencies, the effects of the parasitic components of the circuit have to be evaluated and the loop inductances minimized. In addition to the power electronic switching components, the IPEM can include for example gate drivers, a portion of the DC-link capacitance and sensors [16], [17].

C. Reliability

Even though the power density of the transformer is low and its losses are high, it has an advantage in reliability. Being a passive design, the transformer does not have many potential failure points. The utility network transformers are typically expected to have a lifetime of 40 years [18], [19]. However, this value is defined as a profitable utilization time and does not necessarily reflect the technical lifetime of the component, which can reach even higher values.

On the other hand, the power electronic converters have a lot of potential failure points. Especially, the lifespan of the electrolytic capacitors is degraded rapidly by elevated temperatures. A study of the expected lifetimes of different components of an inverter was carried out in [20]. It was shown that the major part of system failures were due to the failure of the electrolytic capacitors of the inverter. The second component most prone to failure were cooling fans.

The reliability of the power electronic converters can be significantly improved by using polypropylene capacitors. However, this affects the cost and power density of the system as the polypropylene capacitors suitable for the application are much bulkier and more expensive than electrolytic capacitors. If the design applies WBG devices, the electrolytic capacitors are not a feasible option as they have a high amount of parasitics compared with their polypropylene and ceramic alternatives.

D. Possibilities

Besides reduced losses and higher power density the DC-DC converter provides many possibilities to the connectivity of the customer-end network. Distributed generation has become increasingly popular over recent years especially in the form of domestic installed solar power plants. However, the solar panels require an interface to the public network as they generate DC current. If the panels are connected to the existing AC distribution network, an inverter is required as the interface. The customer DC-DC converter would enable a more direct connectivity for the solar panels as the customer would already have the DC interface. As the output of the converter is isolated from the DC network, it could also be used to supply DC loads, for example, charging of an electric vehicle (EV).

E. Topology of the Converter

An in depth study of different types of isolated converter topologies has been previously carried out in [21]. The main focus in [21] was put on high-current and low-voltage applications, but many of the studied topologies are also suitable for the voltage levels in the DC network studied in this paper. Because the same principles are applied in the lifetime cost analysis of the DC network as in the AC network, the most feasible solution is found when the total lifetime cost of the converter is at its minimum. Therefore, even if the converter has an outstanding efficiency but is very complex in design and therefore also expensive, it is not a good alternative for the DC network. Taking this into consideration, the most interesting of the converters studied in [21] is a phase shifted full-bridge with a voltage doubler type secondary-side rectifier (PSFBVD). It is a soft-switched converter that has a wide ZVS range compared with the more typical phase shifted full-bridge converter [22]. According to the operating principle, the converter is not required to have an output inductor which further simplifies the design. The primary switches of the converter are operated with ZVS and ZCS, and the secondary side rectifier with ZCS [21].

F. Converter Loss Analysis

LVDC-distribution is considered to be a feasible solution in rural distribution to replace the existing vulnerable overhead lines of the MV network branches and to enhance the voltage quality experienced by the end-customers [2]. Therefore, a typical customer connected to the LVDC network would be a detached house. A profile for a household with electrical heating and a 300 l water heater was thus selected to represent the power demand of a potential LVDC-customer. The load profile for the selected customer type is given in Fig. 4.

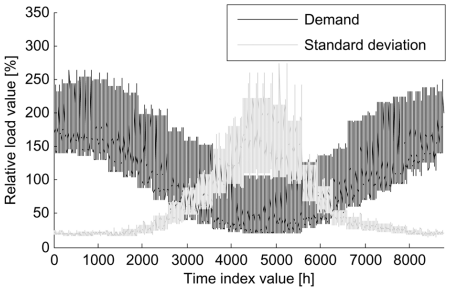

Fig. 4. Measured average load profile for detached households with electrical heating and a 300 l water heater [7]. The relative load value is a percentage of the average hourly power of the customer.

The load profile in Fig. 4. represents an averaged load value for every hour of the year relative to the average hourly power of the end-customer. The average hourly power of the customer is calculated as

$$P_{avg,h} = \frac{E_{tot,a}}{8760}, \tag{1}$$

where $E_{\mathrm{tot,a}}$ is the yearly energy consumption of the customer. A value of $E_{\mathrm{tot,a}} = 20\ \mathrm{MWh}$ was selected for this study as it represents the typical annual energy consumption of a detached house with electrical heating and a 300 l water heater. After calculating the value of $P_{\mathrm{avg,h}}$, the load profile of Fig. 4 can be used in the loss calculations. The power is assumed to be evenly distributed among the three phases of the CEI.

The PSFBVD converter was designed for a nominal power rating of $P_{\mathrm{nom}} = 16\ \mathrm{kW}$ and its calculated losses were compared against the measured losses of the 16 kVA three-phase transformer shown in Fig. 3. The converter is implemented with transistors also on the secondary side to enable bidirectional power flow. The transistor parameters are as in [23]. The switching loss is assumed negligible because of the ZVS and ZCS switching of the transistors and the fact that the selected components also have low switching losses even in a hard switched case. RMS currents of the switches for the loss calculations are calculated by

$$I_{\mathrm{RMS}} = \sqrt{\frac{1}{T}\int_{0}^{\sqrt{L_{\mathrm{lk}}C_{\mathrm{r}}}\pi}\left(n\frac{\omega_{\mathrm{r}}I_{\mathrm{out}}T}{2}\sin(\omega_{\mathrm{r}}t)\right)^{2}dt}, \tag{2}$$

where L_{lk} is the leakage inductance of the transformer, C_{r} the resonance capacitance of the voltage doubler, ω_{r} the resonance frequency, n the turn ratio of the transformer, and I_{out} the output current [21]. The converter is operated near its maximum duty cycle and a value of $D = 0.43$ was selected. With the selected parameters and $P_{\mathrm{out}} = 16\ \mathrm{kW}$, the value of I_{RMS} of a single switch is $I_{\mathrm{RMS,T,pri}} = 18.1\ \mathrm{A}$ on the primary side

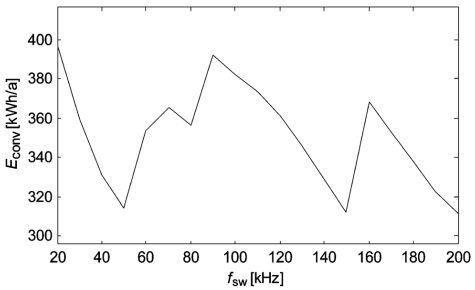

Fig. 5. Annual losses for a 16 kW PSFBVD isolated DC-DC converter as a function of the switching frequency f_{sw}. The converter is designed for voltage levels of $U_{\mathrm{in}} = U_{\mathrm{out}} = 750$ VDC.

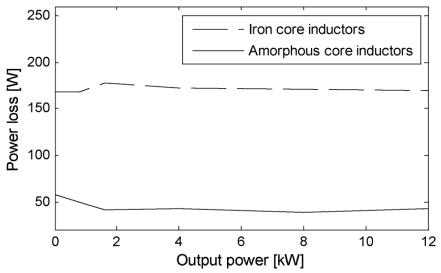

Fig. 6. Calorimetric losses for iron core and amorphous core three-phase CEI output LC filter inductors with an inductance value of $L = 500$ μH. The Switching frequency was $f_{\mathrm{sw}} = 16$ kHz and the filter capacitance $C = 5$ μF.

and $I_{\mathrm{RMS,T,sec}} = 36.1$ A on the secondary side, respectively. The peak current is $I_{\mathrm{pk,T,pri}} = 39.0$ A on the primary side and $I_{\mathrm{pk,T,sec}} = 77.9$ A on the secondary side, respectively. The switching components [23] were selected based on conditions $T_{\mathrm{j}} = 150°\mathrm{C}$ and $T_{\mathrm{c}} = 50°\mathrm{C}$. One transistor per switch is used on the primary side and two in parallel on the secondary side, respectively.

The auxiliary losses caused by cooling, gate drivers and control board are estimated at $P_{\mathrm{aux}} = 20$ W, which corresponds to the measured power consumption of the auxiliary equipment of the laboratory prototype CEI rated for $P_{\mathrm{nom}} = 16$ kVA. The converter is designed with a PM114 ferrite core [24] and foil windings. The annual losses of the converter as a function of the switching frequency f_{sw} are depicted in Fig. 5.

As shown in Fig. 5 the loss minimums are at points $f_{\mathrm{sw}} = 50$, 150, and 200 kHz. However, the differences are negligible. The shape of the curve is due to the changes in the transformer design, and each of the points in which the losses increase significantly represent a point in which the number of primary- and secondary-side turns are decreased resulting in an increase in the value of B as defined by

$$B_{\mathrm{ac,trans}} = \frac{U_{\mathrm{pri}} \cdot 10^4}{kN_{\mathrm{pri}}A_{\mathrm{c}}f}, \tag{3}$$

where U_{pri} is the maximum primary voltage, k a waveform coefficient, A_{c} the transformer core cross-sectional area, and N_{pri} the number of primary turns [21]. The increase in the value of B results in an increase in the core losses of the transformer. However, because the value of N_{pri} remains constant to some extent when the value of f_{sw} is increased further, the value of B decreases until the value of N_{pri} is required to be changed again. If we also consider the fact that some amount of switching loss is present in the converter, the minimum loss is achieved when $f_{\mathrm{sw}} = 50$ kHz. Because the supplied load is $E = 20$ MWh/a, the converter is operated at an average efficiency of $\eta = 98.4\%$. In comparison, the 16 kVA transformer is operated at an average efficiency of $\eta = 93.5\%$, and therefore, a significant reduction in the losses is observed if the transformer is replaced with the selected converter. The lower average value of η in the 16 kVA transformer case is due to the high amount of no-load losses as demonstrated in Fig. 3.

III. Output LC Filter Design

In a previous study [14], it was noticed that the output filter of the CEI would benefit from a higher inductance value. Based on the results, the parameters affecting the filter inductor design are studied in this paper. The load profile of the CEI, the cost of the filter components, the switching frequency and the losses in the filter are included in the study. Physical limitations such as excessive temperature caused by high losses, core saturation, and window fill are also addressed. The proposed model calculates a lifetime-cost-minimized combination of the inductance L, the filter inductor core model, the air gap length l_{a}, the winding wire diameter d, and the capacitance C of the filter capacitor.

Amorphous metal was chosen for the inductor core material as it has been shown to have significant benefits over iron [25]. The conclusion in [25] is further backed up by the calorimetric measurements carried out for the CEI studied in this paper. Two sets of inductors designed with the same parameters but having a different core material were measured. The iron core inductors were found to have significantly higher losses than the amorphous core inductors as depicted by Fig. 6.

A. Description of the Model

The design process begins by selecting the required nominal current of the CEI. For this study, nominal currents of $I_{\mathrm{nom}} = 16$ A and $I_{\mathrm{nom}} = 25$ A were selected as 16 A represents a typical circuit breaker rating and 25 A a typical main fuse rating in Finland. The dimensioning of the inductor is based on these ratings as the CEI is installed before the protection devices in the customer connection point. The nominal current value is used to find the combinations of L, l_{a}, and d that are not limited by the magnetomotive force NI, and the selected maximum operating temperature T_{max}.

Switching frequencies of 10, 20, 40, 60, and 80 kHz were selected for the study. For the selection of the output filter cut-off frequency f_{c}, the requirements for the output voltage quality have to be set. The upper limit for the output voltage THD has been defined in the Finnish network standards to be below 8% throughout the year [26]. A target level of less than 5% for the THD has been previously proposed in [27]. Therefore, the same value was selected for the study. However, the definition in [26] is only defined for the 50 Hz harmonics up to a value of

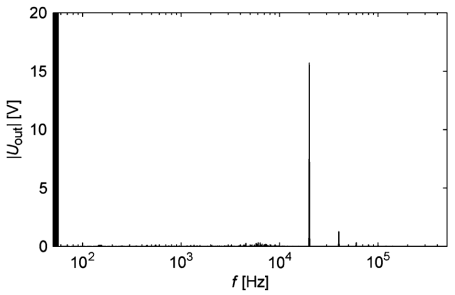

Fig. 7. FFT spectrum of the simulated output voltage when $U_{\rm DC} = 400$ V, $f_{\rm sw} = 10$ kHz, $L = 280$ μH, and $C = 2$ μF. Sampling time 0.1 μs.

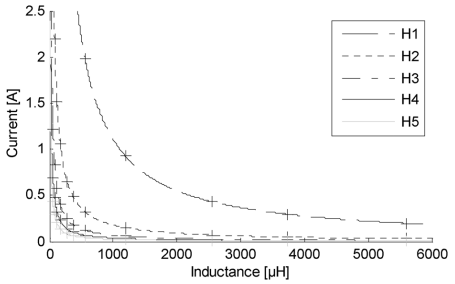

Fig. 8. Simulated harmonic currents in the LC filter inductor as a function of inductor inductance. $U_{\rm DC} = 400$ V and $f_{\rm sw} = 10$ kHz.

2 kHz, and therefore, does not include the CEI switching-frequency-generated harmonics. As an application specific standard is not available, the definition in [26] is extended to include the first five switching-frequency-generated harmonics in the output voltage. The second-order slope of the LC filter effectively reduces the level of the high-order harmonics of $f_{\rm sw}$ to an insignificant level as shown in Fig. 7.

After the switching frequencies and output voltage quality were selected, a simulation of the switching-frequency-induced harmonic currents in the inductor was carried out with different values of $f_{\rm sw}$, L, C, and $U_{\rm DC}$. Three values of $U_{\rm DC}$ were selected. A value of $U_{\rm DC} = 750$ V was selected as the base level as it is the nominal DC voltage level in the research platform. Values of $\rm U_{DC} = 1500$ V and $\rm U_{DC} = 400$ V were selected for comparison. 1500 VDC is the maximum obtainable voltage level in the current system if the CEI is connected between the positive and negative DC poles. 400 VDC represents a similar voltage level that has been studied for DC distribution worldwide [1], [5], [28], [29].

Based on the simulation, models for the first five harmonic currents as a function of the inductance L were defined as given by

$$I = a \cdot L^b, \tag{4}$$

and they are depicted in Fig. 8.

Similar models were defined for the switching frequencies $f_{\rm sw} = 10, 20, 40, 60$, and 80 kHz and input voltages $U_{\rm DC} = 750$ and 1500 V. Gapped AMCC C-cores manufactured by Metglas [30] were selected as the inductor cores. The manufacturer defines different values of $A_{\rm L}$ for the cores depending on the air gap length [31]. The $A_{\rm l}$ value is given by

$$A_l = \frac{L}{N^2}, \tag{5}$$

where the unit of L is [μH]. The required number of winding turns for a given inductance value is, therefore, calculated by

$$N = \sqrt{\frac{L}{A_{\rm L}}} \tag{6}$$

The flux density B in the gapped core is calculated by

$$B = \frac{NI}{A_{\rm c}} \cdot A_{\rm L} \cdot 10^{-6} \tag{7}$$

where $A_{\rm c}$ is the cross-sectional area of the inductor core.

Limits for the NI values before core saturation are defined in [31] and are used in the design process as one of the physical limitations. The filter inductor has to be designed to have the same inductance at all load values as otherwise the requirement for the voltage quality is not met. Therefore, the combinations of inductance, core model, and air gap length which result in excessive values of the magnetomotive force NI, and thus a decrease in the $A_{\rm L}$ value as seen in [31], are excluded.

The core losses for the model are calculated by using the manufacturer-provided equation [30]

$$P_{\rm core} = 6.5 f^{1.51} \cdot B^{1.74}, \tag{8}$$

Values of B are calculated by (7) using the simulated values of the harmonic currents at frequencies $f = f_H$, in which the subscript H denotes the order of the harmonic current depicted in Fig. 8. However, because (8) is based on the Steinmetz equation, it is only valid for sinusoidal excitations. Therefore, some amount of deviation is expected in PWM converter calculations. Improved calculation methods for non-sinusoidal waveforms have been proposed in [32]–[34].

Winding losses are calculated based on the AC resistance of the copper. The 50 Hz load current uses the whole cross-sectional area of the wire. However, the switching-frequency-induced harmonic currents only use a portion of the area which is calculated by

$$A = \pi \left(r^2 - (r - \delta)^2\right), \tag{9}$$

where δ is the skin depth of the conductor at a certain frequency f and is defined as

$$\delta = \frac{1}{\sqrt{\pi f \mu \frac{1}{p}}}. \tag{10}$$

The length of an average winding turn is calculated by [35]

$$MTL = 2(a + 2b + d) \tag{11}$$

where a, b and d are dimensions defined in [30] and depend on the core model. The resistance of the whole winding can therefore be calculated by

$$R = \frac{N \rho MTL}{A} \tag{12}$$

Because A is dependent on the frequency of the current, R is calculated for the 50 Hz load current and the switching harmonics. The total losses of the inductor are calculated as a sum of the core and winding losses at the 50 Hz load current and the switching induced harmonic currents by

$$P_{\mathrm{tot}} = \sum \left(P_{\mathrm{core}} \left(I(f) \right) + P_{\mathrm{wire}} \left(I(f) \right) \right) \tag{13}$$

The calculated total losses P_{tot} are used to estimate the operating temperature of the inductor. The operating temperature is calculated by [35]

$$T = T_{\mathrm{amb}} + \left(\frac{P_{\mathrm{tot}}}{SA} \right)^{0{,}833}, \tag{14}$$

where SA is the total dissipation surface area of the inductor. SA is calculated by [34]

$$SA = 2f(b+d) + 2(b+d)(b+e) + 2f(b+e), \tag{15}$$

where a, b, d, e and f are dimensions defined in [30]. A value of $T_{\mathrm{amb}} = 50^{\circ}\mathrm{C}$ was selected as it closely represents the maximum cabinet temperature of the CEI in summer. A value of $T_{\mathrm{max}} = 80^{\circ}\mathrm{C}$ was selected for the maximum operating temperature of the inductor. The inductor designs that exceed the value of T_{max} during nominal load will be eliminated in the design process.

The core losses P_{core} are mainly caused by the high-frequency harmonic switching currents. The 50 Hz load current does not cause any significant core losses as can be seen from [30]. In contrast, the 50 Hz load current is the main cause for the winding losses P_{wire}. P_{core} can be reduced by increasing the inductance L of the filter as it reduces the amplitude of the high-frequency harmonic currents. However, increasing the value of L also increases the investment cost. As L is increased, the value of NI also increases and a larger core may be needed to avoid core saturation. If the same core is used and the air gap length is increased, NI can be linearized further. However, increasing the air gap length decreases the A_{L} value, and a higher number of winding turns N is required to produce the same inductance value. If a wire of the same diameter is used, the winding losses increase as a result of an increase in the resistance. The window area might also become a limiting factor as the number of winding turns N is increased or a larger diameter wire is selected to reduce winding losses. The distribution of the losses between P_{core} and P_{wire} also highly depend on the application. For example, in the LVDC network the nominal power of the CEI is rarely used as can be seen in Fig. 4.

Thus, the selection of the filter configuration becomes an optimization problem, which is commonly used in distribution network techno-economic analyses and is written as

$$\begin{aligned} &\min \int_0^T \left(C_{\mathrm{inv}}(t) + C_{\mathrm{loss}}(t) + C_{\mathrm{interr}}(t) + C_{\mathrm{main}}(t) \right) dt \\ &\approx \min \sum_{t=1}^{T} \left[C_{\mathrm{inv}}(t) + C_{\mathrm{loss}}(t) + C_{\mathrm{interr}}(t) + C_{\mathrm{main}}(t) \right] \end{aligned} \tag{16}$$

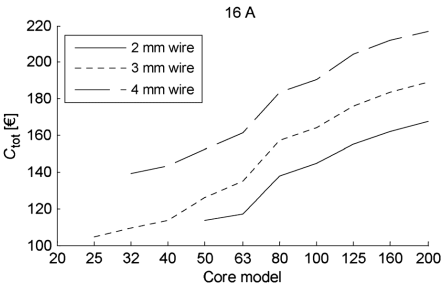

Fig. 9. Output of the model with input parameters $U_{\mathrm{DC}} = 400\ \mathrm{V}$, $f_{\mathrm{sw}} = 10\ \mathrm{kHz}$, $I_{\mathrm{nom}} = 16\ \mathrm{A}$, and $C_{\mathrm{a}} = 4,93\ \mathrm{cent/kWh}$. The output represents the minimum lifetime cost C_{tot} for each of the core models given any combination of inductance, air gap length, and three winding wire diameters.

where C_{inv} is the investment cost, C_{loss} the loss cost, C_{int} the interruption cost, and C_{main} the maintenance cost [36]. Utilization period of $t_{\mathrm{u}} = 10$ a was selected for the study as this roughly estimates the lifetime of the inverter. Therefore, for the purpose of this paper only C_{inv} and C_{loss} are included in the calculations as C_{interr} and C_{main} represent the cost caused by failure and replacement of the component and downtime of the system, respectively.

C_{inv} is based on retail prices for the different components. 1000 pcs quantities for the inductor cores, 500 pcs quantities for the filter capacitors [37], [38], and 1 kg quantities for the winding wire [39]. C_{loss} is calculated as the present value of an annuity by

$$C_{loss} = P_{tot} C_e \frac{1 - (1+p)^{-t_{\mathrm{u}}}}{p} \tag{17}$$

where p is the interest rate and C_{e} the electricity market price. A value of $p = 5\%$ was used in the calculations. Values of $C_{\mathrm{e}} = 4.930\ \mathrm{cent/kWh}$ and $C_{\mathrm{e}} = 3.664\ \mathrm{cent/kWh}$ were selected for the electricity market price as these represent the yearly averages in 2011 and 2012 in Finland [40]. Two values were selected because of the significant difference between the years 2011 and 2012 to determine how the price of electricity affects the design. However, the value of 4.930 cent/kWh better reflects the long-term average of the electricity market price in Finland as the average of the last five years is closer to that value.

B. Model Output

An output of the model with input parameters $U_{\mathrm{DC}} = 400\ \mathrm{V}$, $f_{\mathrm{sw}} = 10\ \mathrm{kHz}$, $I_{\mathrm{nom}} = 16\ \mathrm{A}$, and $C_{\mathrm{e}} = 4.930\ \mathrm{cent/kWh}$ is illustrated in Fig. 9.

As Fig. 9 shows, the configuration having the lowest lifetime cost C_{tot} is achieved by the AMCC25 core. The inductor parameters are $L = 800\ \mu\mathrm{H}$, $l_{\mathrm{a}} = 2.5\ \mathrm{mm}$, and $d = 3.0\ \mathrm{mm}$. The AMCC20 and smaller core models do not have any feasible solutions for the selected input parameters.

Fig. 10 depicts the model output with the same input parameters when the nominal current value is increased to a value of $I_{\mathrm{nom}} = 25\ \mathrm{A}$.

As can be seen in Fig. 10 the increase in the nominal current rating changes the results significantly. The core models AMCC25 and AMCC32 no longer have feasible solutions.

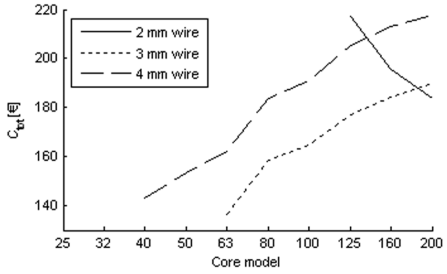

Fig. 10. Output of the model with input parameters $U_{\mathrm{DC}} = 400$ V, $f_{\mathrm{sw}} = 10$ kHz, $I_{\mathrm{nom}} = 25$ A, and $C_{\mathrm{a}} = 4,93$ cent/kWh. The output represents the minimum lifetime cost for each of the core models given any combination of inductance, air gap length, and three winding wire diameters.

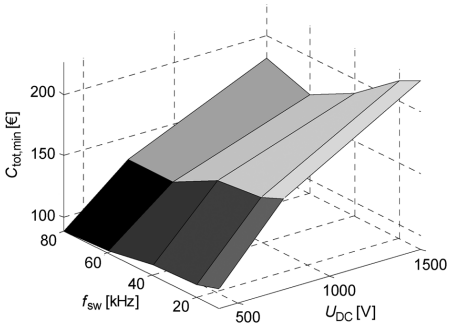

Fig. 11. Minimum lifetime cost $C_{\mathrm{tot,min}}$ as a function of the DC-voltage U_{DC} and the switching frequency f_{sw}. $I_{\mathrm{nom}} = 16$ A in all cases.

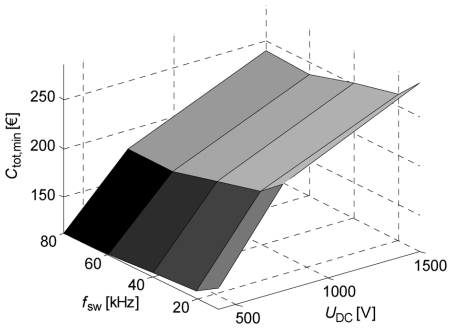

Fig. 12. Minimum lifetime cost $C_{\mathrm{tot,min}}$ as a function of the DC-voltage U_{DC} and the switching frequency f_{sw}. $I_{\mathrm{nom}} = 25$ A in all cases.

The configuration having the lowest C_{tot} is achieved by the AMCC63 core and parameters $L = 700$ μH, $l_{\mathrm{a}} = 3.0$ mm, and $d = 3$ mm. The difference in the curve of the $d = 2$ mm winding wire clearly indicates the increase in the copper losses with the higher nominal current, which makes the wire diameter unsuitable for the design. The different shape of the curve compared with its $d = 3$ mm and $d = 4$ mm counterparts is explained by the increase in the dissipation surface area by the larger core model which lowers the estimated inductor temperature calculated by (14), and a higher number of feasible solutions are found. Therefore, the slope of the curve is in the opposite direction.

The relation between U_{DC}, f_{sw}, and minimum lifetime cost $C_{\mathrm{tot,min}}$ is depicted in Fig. 11. The figure shows that the selection of the DC voltage level has the highest effect on $C_{\mathrm{tot,min}}$. Increasing the switching frequency to a value of $f_{\mathrm{sw}} \geq 60$ kHz increases the minimum lifetime cost $C_{\mathrm{tot,min}}$ if $U_{\mathrm{DC}} \geq 750$ V. This indicates that the core material becomes a limiting factor as a result of the increase in iron losses. A higher DC voltage results in higher amplitudes of the harmonic currents, and therefore, the effect on iron losses begins to be noticeable with lower switching frequencies compared with a case in which $\mathrm{U_{DC}} \ll 750$ V. As can be seen from [30] and (8), the losses of the core material increase exponentially as a function of f_{sw} and B. When the DC voltage level is increased, the value of the high-frequency induced B also increases generating more losses in the core material. Therefore, a point after which the value of $C_{\mathrm{tot,min}}$ starts to increase as the value of f_{sw} is increased is to be expected. If the objective is to significantly increase the switching frequency value beyond $f_{\mathrm{sw}} = 60$ kHz to gain advantage in power density without a drawback in $C_{\mathrm{tot,min}}$, different core materials should be evaluated for the design to determine if the reduction in total cost can be extended further as a function of f_{sw}.

Increasing the switching frequency from a value of $f_{\mathrm{sw}} = 10$ kHz to a value of $f_{\mathrm{sw}} = 40$ kHz decreases the value of L by a factor of two in the $U_{\mathrm{DC}} = 400$ V case. However, in the $U_{\mathrm{DC}} = 750$ V and especially in the $U_{\mathrm{DC}} = 1500$ V case, a similar reduction of L is not observed. This is caused by the significant increase in the high-frequency current amplitude as the input DC voltage is increased which requires higher attenuation to achieve reasonable values of C_{loss}. Because the design calculates the total lifetime cost of the filter for a period of $t_{\mathrm{u}} = 10$ a, the cost caused by the losses has a high weight factor. In contrast, an increase in the investment cost of the filter has a lower weight factor. The model proposes a higher value for the inductance as this significantly reduces the value of C_{loss} and as a result, also the value of $C_{\mathrm{tot,min}}$ in the studied application.

Fig. 12 illustrates the difference in $C_{\mathrm{tot,min}}$ when the design parameter I_{nom} is changed to a value of $I_{\mathrm{nom}} = 25$ A.

Increasing the nominal current requirement has a significant impact on the shape of the plane. The relative difference in $C_{\mathrm{tot,min}}$ between the voltage levels 400 VDC and 750 VDC is much higher whereas the difference between the values of f_{sw} is lower. The higher I_{nom} requirement results in the selection of a larger core model and a higher value of d in most of the cases, which results in higher core losses and investment cost but lower winding losses. As the low-load losses are mostly caused by the core losses and the nominal power is rarely used, this combined with the higher value of C_{inv} results in an increase in $C_{\mathrm{tot,min}}$. The increase in $C_{\mathrm{tot,min}}$ was in the range of 20–40% compared with the $I_{\mathrm{nom}} = 16$ A case.

When the electricity price C_{e} is changed the ratio between C_{loss} and C_{inv} is different. With the selected value of $C_{\mathrm{e}} = 3.664$ cent/kWh the resulting inductor parameters are very similar if compared with the $C_{\mathrm{e}} = 4.930$ cent/kWh case.

The lower value of C_{e} leads to a reduction in the value of C_{loss} and therefore, solutions of $C_{\mathrm{tot,min}}$ in which the value of L is smaller can be found in some of the cases. The resulting values of $C_{\mathrm{tot,min}}$ are reduced in all of the cases as expected. However, the reduction is only in the range of 5–9% over the 10 a utilization period.

IV. Conclusions

Potential improvements can be achieved by optimizing the designs of the galvanic isolation and the output filter inductor of the CEI. The isolated DC-DC converter shows high potential in the optimization of losses and power density of the galvanic isolation. However, there are some issues in reliability compared with the passive transformer alternative that need to be addressed. A selection for the converter topology and a comparison of the losses against a passive three-phase transformer with the same nominal power rating was carried out. It was concluded that the converter can be operated at a significantly higher average efficiency, and therefore, the losses of the system can be decreased.

Design of the output filter inductor has many variables that affect the filter lifetime cost. A lifetime-cost-minimized design method was presented and comparisons were carried out with different combinations of the input DC voltage level, switching frequency, and nominal current requirement. The input DC voltage level was found to have the highest effect on the lifetime cost of the filter. Increasing the switching frequency decreased the cost to a certain level, after which the cost began to increase as a result of the exponential relation between frequency and core loss. A 26% reduction in the electricity price had only a minor effect on the resulting inductor parameters and the minimum lifetime cost when the utilization period was 10 a.

Further research topics will include a more thorough study of the selected converter type. A laboratory prototype will be built and measurements carried out to enable a more valid comparison against the measured losses of the passive three-phase transformer. For the filter design, verification of the simulated inductor high-frequency current and the calculated core losses will be carried out by electrical and calorimetric measurements. The model parameters will be adjusted if deviations between the calculations and the measurements are found.

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Publication II

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Life-Cycle Cost Analysis for the Customer-end Inverter Used in Low Voltage DC Distribution

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***Abstract*—This paper analyses the life-cycle cost of a customer-end inverter that is used in a low voltage DC distribution system. Cost of the losses during the utilization period of the system and the investment cost of the main components is included in the study and the distribution between them is analyzed to determine the dominating cost factors. A sensitivity analysis is carried out to determine how variations in the cost of electricity, the cost of the hardware and the selected switching frequency affect the life-cycle cost.**

Keywords— Pulse width modulation inverters; Smart grids;

I. INTRODUCTION

The low voltage direct current (LVDC) system is an emerging power distribution technology under intense research and development globally. LVDC distribution has been proposed for various applications from datacenters [1],[2] to public utility grid distribution [3]-[6]. The LVDC research network [7],[8] discussed in this paper uses voltages levels of ±750 VDC. The end customers are connected to either between +750 VDC and the middle pole or between -750 VDC and the middle pole. The middle pole is defined as 0 VDC when referenced to either +750 VDC or -750 VDC but is not necessarily 0 VDC when referenced to ground because the network is implemented as a functionally unearthed network (IT). The customer-end network is a functionally earthed network (TN) and the customer-end 50 Hz AC voltage of 230/400 VAC_{RMS} is produced using a customer-end inverter (CEI). The user-end power demand and therefore, the load of the CEI varies in a wide range [9], which separates the distribution system application of converter systems from the common industry applications.

In Finland, LVDC distribution is considered as an alternative to AC in rural areas where for example a part of the overhead lines is to be replaced with underground cabling to increase the security of supply. In the worst scenario, a part of the medium voltage as well as a part of the low voltage network needs to be replaced if AC is used. By using DC instead of AC, the power capacity of the cables increases making it possible to use only low voltage cabling and decrease the cabling cost by a significant margin. However, by using DC, converters at each end of the DC network are required which decreases the difference in the required investment. The converters also generate losses which decreases the efficiency of the system. From the distribution system operator point of view, the life-cycle cost of the network is the driving factor and therefore, the life-cycle cost of the DC network requires research to determine the most cost efficient solution. The purpose of this paper is to determine how different parameters affect the life-cycle cost of the CEI and to find out how the life-cycle cost of the CEI can be minimized and therefore, increase the feasibility of the implementation of DC distribution on a wider scale. The objective is defined by

$$\min \int_0^T (C_{\text{inv}}(t) + C_{\text{loss}}(t) + C_{\text{int}}(t) + C_{\text{main}}(t))dt$$

in which C_{inv} is the investment cost, C_{loss} the cost of the losses, C_{int} the interruption cost, C_{main} the maintenance cost and T the utilization time [10]. This paper focuses on the minimization of the sum of C_{inv} and C_{loss} of the CEI during a utilization period of $T = 10$ years.

II. MODULAR CUSTOMER-END INVERTER

Because the LVDC system is considered as a potential alternative to AC in the Finnish rural areas, a typical customer group that would be supplied by the DC network are households that use electrical heating. An averaged load profile of this type of a customer group is depicted in Fig. 1. If a power based tariff is assumed, the selection of the nominal power of the CEI can be carried out by calculating the theoretical peak power of a single customer of the selected

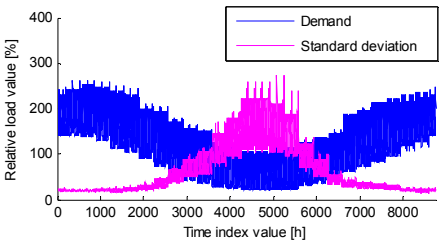

Fig. 1. An averaged load profile of a customer group that consists of households that have electrical heating and a 300 liter water heater [9]. The x-axis defines each hour of the year and the y-axis the load value relative to the average hourly power P_{avg}.

customer group by using the curve of Fig. 1 [10]. A value of $E = 20$ MWh is selected for the yearly energy consumption as this well represents an average value of a single customer of the selected customer group. Using a confidence level of 99%, the peak power of a single customer becomes $P_{max} = 15.3$ kVA. The load value for each hour is calculated by multiplying the percentage value depicted in Fig. 1 with the average hourly power of $P_{avg} = 20\text{MWh}/8760 = 2.28$ kVA. By comparing the value of P_{max}, which is used as the dimensioning value for the nominal power of the CEI, to the resulting load values defined by P_{avg} and Fig. 1, it can be seen that the load of the CEI contains a high value of partial load. A similar conclusion can be drawn from the efficiency curves [11] of two 16 kVA CEIs of the research network [8]. The curves presented in [11] were calculated using calorimetric power loss measurements carried out for the CEI and by comparing the measurement results against the actual load values of two customers that are supplied using similar CEIs in the research network [8]. The loads were measured with one minute resolution during a four week period. As can be seen from the results in [11], the high amount of partial load leads to poor utilization of the CEIs and they operate at a reduced efficiency. Typically the efficiency of converters begins to decrease when the load is below 20—30% of the nominal power. In case of a 16 kVA CEI, this would mean load values that are below 3.2—4.8 kVA. Looking at the curve of Fig. 1 and the measured customer load values in [11], a high amount of the load of the CEI is located below 30% of P_{max}. To address the problem of reduced efficiency during partial load, a modular CEI has been proposed [12],[13]. The modular CEI is implemented using single-phase H-bridge inverters with LC-filters and the galvanic isolation between the AC and DC networks is implemented using an isolated DC-DC converter [12],[13]. As concluded in [13], the minimum cost of the modular CEI is achieved with the least amount of over dimensioning and therefore, the nominal power of a single inverter module can be defined by

$$P_{nom} = \frac{P_{max}}{3m}, m \in [1,2,3...], \quad (1)$$

in which m is the number of inverters connected in parallel in a single phase. The load is assumed to be evenly distributed among the three phases and the minimum amount of inverter modules to supply the load are switched on as defined by

$$N_{modules,on} \geq \frac{P_{load}(t)}{3P_{nom}}, N_{modules,on} \in [3,6,9...], \quad (2)$$

in which P_{load} is the load value at time instant t [13].

III. Life-cycle cost analysis

A preliminary life-cycle cost analysis of the modular CEI was carried out in [13]. It was concluded that increasing the switching frequency f_{sw} decreased the life-cycle cost of the output filter. However, because the increase of the life-cycle cost of the inverter bridge was more dominating, the total life-cycle cost of the CEI increased as a function of f_{sw}.

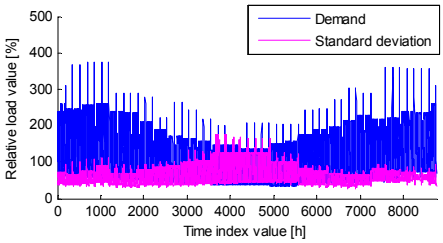

Fig. 2. An averaged load profile of a customer group that consists of households that have district heating and an electric sauna stove [9]. The x-axis defines each hour of the year and the y-axis the load value relative to the average hourly power P_{avg}.

A. Extended study

In this paper the analysis of [13] is taken a step further. In addition to the load profile depicted in Fig. 1, we examine how the results change if the customer group is changed to a group of households that do not use electrical heating. An averaged load profile of this type of a customer group is depicted in Fig. 2. The typical value of E for a single customer of this type when the household is equipped with modern facilities is $E = 10$ MWh. Therefore, $P_{avg} = 10\text{ MWh}/8760 = 1.14$ kVA, and $P_{max} = 6.1$ kVA. Again, P_{max} is used as the dimensioning value of the CEI. The filter results in [13] were calculated for amorphous core [14] inductors only and no significant gains were observed when the value of f_{sw} was increased beyond $f_{sw} = 40$ kHz. Therefore, in this paper, the filter calculations were extended to include gapped ferrite cores to determine if further reduction of the cost could be achieved. Gapped ETD ferrite cores [15] made out of N87 ferrite [16] were chosen for the study as the data required for the calculations as well as the cores themselves are easily available. If a ferrite ETD core can be selected instead of an amorphous C-core, the cost reduction is significant as the price of the largest ETD core is only 42% of the smallest amorphous C-core. Because the cost due to semiconductor switching loss was found to be a significant limiting factor of the life-cycle cost [13], the selection of semiconductors was revised to include different types of 1200 V silicon carbide MOSFETs [17], some of which were not yet available when the research in [13] was carried out. In addition to the SiC switches, a next generation 1200 VDC GaN switch [18] not yet available on the market was also included in the calculation to determine how the utilization of switches with further reduced switching losses would affect the life-cycle cost and the design of the CEI. Due to the possibility of lowering the intermediate voltage of the CEI with the DC-DC converter, two input voltage levels of 400 VDC and 750 VDC similar to [13] are studied. However, the structure and cost of the DC-DC converter is not analyzed in this paper and will be left for future publications. The conduction losses P_{cond} of the switches are calculated based on the conduction times of the switches, the load RMS current, and the switch on-state resistance $R_{ds(on)}$. The junction temperature as well as the value of $R_{ds(on)}$ is estimated to increase linearly as a function of the load so that $T_j = 25$ °C at 0% load and $T_j = 100$ °C at 100% load

and the value of $R_{ds(on)} = R_{ds(on)}(T_j(P_{load}))$. The heat sinks are dimensioned so that $T_j = 100$ °C at 100% load taking into consideration the value of the thermal resistance of the device packaging $R_{th(j-c)}$ and the insulation material between the packaging and the heat sink $R_{th(c-hs)}$. A value of $R_{th(c-hs)} = 0.09$ K/W [19] is used in the calculations. The switching energies are determined by using curve fits from the manufacturer's datasheets and the switching losses are calculated by

$$P_{sw} = (E_{on}(I_{sw}) + E_{off}(I_{sw})) \cdot f_{sw}, \quad (3)$$

in which E_{on} is the turn-on energy, E_{off} the turn-off energy and I_{sw} the switched current. I_{sw} is often defined as an average of the sinusoidal output current [20]. In the case of unipolar switching, in which each of the switches conducts during both of the half-cycles of the output voltage, I_{sw} is calculated by

$$I_{sw} = \frac{2}{\pi}\hat{I}_{load}, \quad (4)$$

in which $\hat{I}_{load}$ is the peak of the sinusoidal load current. The gate driving power of a single switch is calculated by

$$P_{gate} = Q_g V_g f_{sw}, \quad (5)$$

in which Q_g is the gate charge, V_g the gate driving voltage. The LC-filters are calculated similar to a previous study [21], with the exception of the modular CEI structure that has multiple LC-filters and the inclusion of the ferrite cores that have different material properties compared to the amorphous metal. The number of different winding wire diameters is also extended to include diameters 0.5 and 1 mm in addition to 2, 3, and 4 mm. The results are calculated for a maximum number of modules as defined by (1) while $m = 4$ and for switching frequencies of 10, 20, 40, 60 and 80 kHz. Due to unipolar switching, the frequency seen by the LC-filter is $2f_{sw}$. The three first harmonic frequencies are used in the core and copper loss calculation. The winding is assumed to be implemented in a way that the fringing flux of the air gap does not induce a significant amount of additional losses. If most of the winding is located directly over or near the air gap, the effect of the fringing flux needs to be taken into account as it can significantly increase the copper loss [22]. The costs of the filter components are defined for 1000 pcs quantities for the cores and 1 kg quantities of the winding wire. Semiconductor prices are referenced for the minimum discounted quantities from [23] and ferrite prices for 1000 pcs from [24]. Because no price data is available for the GaN switch, its price is assumed to be similar to a SiC switch with similar current and voltage ratings. The required DC-capacitance is calculated by

$$C = \frac{P_{nom}}{2\omega U_{DC}\Delta U_{ripple}}, \quad (6)$$

in which ω is the output voltage frequency, U_{DC} the intermediate DC voltage, and ΔU_{ripple} the allowed ripple voltage in the intermediate circuit. A value of $\Delta U_{ripple} = 0.1 U_{DC}$ is used in the calculations. The capacitor prices per µF are referenced from [25],[26], which represent low average prices for film capacitors. The required heat sinks are determined from the required value of the thermal resistance R_{th} to keep the junction temperatures of the semiconductor switches below $T_{j,max} = 100$ °C at nominal load. In addition, the value of $T_{j,max}$ is varied between $T_{j,max} = 100$—150 °C while $T_{j,max} = 150$ °C is the maximum allowed value for the switches [17]. A value of $T_{amb} = 50$ °C is used as the ambient temperature for the dimensioning as this roughly represents the maximum cabinet temperature of the CEI during summer. However, because the average value of T_{amb} is much lower, a value of $T_{amb} = 25$ °C and therefore, $T_j = 25$ °C at 0% load is assumed when the cost of the losses are calculated. The prices for the heat sinks are calculated by curve fitting the required R_{th} values against prices for a set of heat sinks that have values of $R_{th} = 0.12$—21 K/W [27]-[33]. Isolated supplies are assumed only for the high-side switches and the cost of the gate drivers for a single H-bridge is estimated to be 16.9 € [34],[35]. However, a gate driver with an integrated high side supply [36] is assumed in the GaN switch case making the gate driver cost only 2.6 €. Each of the CEI modules are assumed to have one current sensor [37] and one processor [38] and the cost of the control is estimated to be 5 €. The auxiliary power is assumed to be supplied by the DC-DC converter that also supplies the intermediate voltage and is therefore, not included in the calculation. However, a solution such as [39] could be used without significantly affecting the cost with small values of m. The cost of the losses is calculated by

$$C_{loss} = P_{loss} C_e \frac{1-(1+p)^{-t_u}}{p}, \quad (7)$$

in which C_e is the cost of electricity, P_{loss} the total power loss, p the interest rate, and t_u the utilization time. P_{loss} is defined as the sum of P_{cond}, P_{sw} and P_{gate} for all the switches during a period of one year. The customer group described in section I and values of $C_e = 0.05$ €/kWh, $p = 0.05$, and $t_u = 10$ years were used in the calculations as the base case. The selected values of C_e and p are typical values used in network analysis in Finland. However, in order to determine how variation in the input cost parameters affect the final results, the electricity price is varied between $C_e = 0.04$—0.08 €/kWh, and the cost of hardware between -50—0%. The ranges are selected based on the recent trend of increasing electricity price over the past ten years and a significant reduction in the hardware cost if the CEIs were mass produced. It can also be said, that the curves presented in Fig. 1 and Fig. 2 do not well represent the load values inside each hour. The load of a single customer can in reality be momentarily ($t \ll 1$ h) higher than the curve would indicate. If a power based tariff is not used, the CEIs are required to be over dimensioned to accommodate a case in which for example the sauna stove and the oven are switched on at the same time which would then exceed the value of $P_{max} = 6.1$ kVA that was calculated for a single customer based on Fig. 2. Therefore, the results are also analyzed in a case in which the value of P_{max} is assumed to be 50% higher than what was calculated based on Fig. 1 and Fig. 2. Because the two customer types have a significant difference in their values of P_{max}, it is therefore obvious that the CEI of the customer of Fig. 2 will be significantly cheaper. In order to carry out a meaningful comparison between the two customer types, the results are normalized to E and P_{max}.

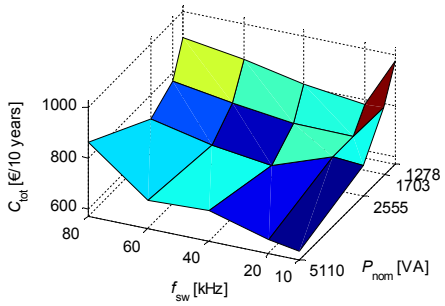

Fig. 3. Life-cycle cost of the CEI for a 10 year utilization period as a function of P_{nom} and f_{sw} when base case values of $P_{max} = 15.3$ kVA, $U_{DC} = 750$ V, $C_e = 0.05$ €/kWh, and 0% difference in hardware cost are used. The load curve of Fig. 1 is used in the loss calculation.

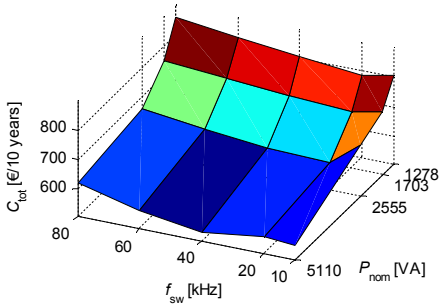

Fig. 4. Life-cycle cost of the CEI for a 10 year utilization period as a function of P_{nom} and f_{sw} when base case values of $P_{max} = 15.3$ kVA, $U_{DC} = 400$ V, $C_e = 0.05$ €/kWh, and 0% difference in hardware cost are used. The load curve of Fig. 1 is used in the loss calculation.

B. Results

First, the results for the base cases were calculated in order to determine the base values for the sensitivity analysis. Fig. 3 depicts the minimum life-cycle cost as a function of P_{nom} and f_{sw}, when the base case values of $U_{DC} = 750$ V $P_{max} = 15.3$ kVA, $C_e = 0.05$ €/kWh and 0% difference in hardware cost are used and the curve of Fig. 1 is used in the loss calculation. The minimum value of C_{tot} in Fig. 3 is found with module size $P_{nom} = 5.1$ kVA ($m = 1$) while $f_{sw} = 10$ kHz. However, the difference between the result with module size $P_{nom} = 2.6$ kVA ($m = 2$) while $f_{sw} = 40$ kHz is negligible. In the combinations of P_{nom} and f_{sw} where the lower saturation flux density B_{max} of ferrite is not a limiting factor and a ferrite core can be selected instead of the more expensive amorphous core, the cost of the CEI decreases quite significantly. Due to the shape of the ETD core, the winding wire cost also decreases as less wire is required to implement a single winding turn if compared to the amorphous C-cores. However, looking at the results, the increase in the switching loss is still more dominating and a reduction in the total cost could not be extended much further as a function of f_{sw} when compared to the previous study which included only the more expensive amorphous cores [13]. The reason for the rapidly increasing cost when $P_{nom} < 2.6$ kVA is that the cheapest SiC switch is already selected in all cases and therefore, the cost increases as a function of m as the number of gate drivers and switches increases. Fig. 4 depicts the minimum life-cycle cost as a function of P_{nom} and f_{sw}, when the base case values of $U_{DC} = 400$ V, $P_{max} = 15.3$ kVA, $C_e = 0.05$ €/kWh and 0% difference in hardware cost are used and the curve of Fig. 1 is used in the loss calculation. With the lower intermediate voltage of $U_{DC} = 400$ V, the switching losses decrease significantly compared to the $U_{DC} = 750$ V case and as a result the differences as a function of f_{sw} are smaller compared to Fig. 3. Because the losses are decreased and the same 1200 V switches are used in both cases, the hardware cost becomes more dominating and the increase in C_{tot} as a function of P_{nom} is more pronounced.

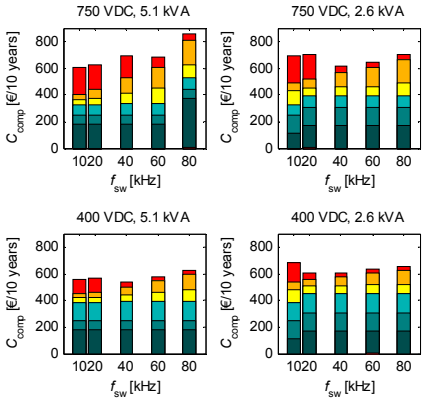

Fig. 5. Costs of the CEI per component for a 10 year utilization period. The different colors of the bars are from top to bottom: filter cost, semiconductor loss cost, heat sink cost, DC capacitance cost, gate drivers and control cost, and semiconductor switch cost. Dimensioning power of $P_{max} = 15.3$ kVA is used in all cases.

The minimum cost is found with module size $P_{nom} = 5.1$ kVA (m = 1) while $f_{sw} = 40$ kHz. Fig. 5 depicts the distribution of the cost components in the minimum cost points of Fig. 3 and Fig. 4. By comparing the results in Fig. 5, it can be seen that the semiconductor switching loss is limiting the design when $U_{DC} = 750$ VDC and $f_{sw} > 20$ kHz. The filter begins to limit the design when the ferrite cores are no longer usable i.e when $P_{nom} = 5.1$ kVA while $f_{sw} < 60$ kHz and when $P_{nom} = 2.6$ kVA while $f_{sw} < 40$ kHz. When the intermediate voltage is lowered to $U_{DC} = 400$ VDC, the hardware cost begins to dominate in all the studied combinations of P_{nom} and f_{sw}. Because the same value of $\Delta U_{ripple} = 0.1 U_{DC}$ is used with both intermediate voltage levels, the DC capacitance cost is higher in the

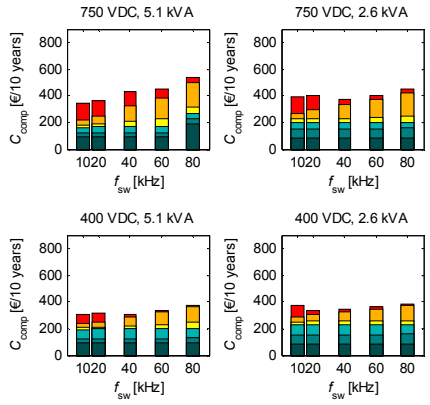

Fig. 6. Costs of the CEI per component for a 10 year utilization period when the hardware costs are reduced 50% in the design process. The different colors of the bars are from top to bottom: filter cost, semiconductor loss cost, heat sink cost, DC capacitance cost, gate drivers and control cost, and semiconductor switch cost. Dimensioning power of $P_{max} = 15.3$ kVA is used in all cases.

$U_{DC} = 400$ VDC case and forms a significant portion of the total cost. In order to get a better understanding what the costs might be if the CEIs were mass produced, the CEIs were also designed with a 50% reduction in the hardware cost. Again, the configuration resulting in the minimum life-cycle cost is selected in each case. The results with the reduced hardware costs are depicted in Fig. 6 for two values of module sizes P_{nom} and both values of U_{DC}. When the price of electricity is varied between $C_e = 0.04$—0.08 €/kWh the minimum cost increases linearly with both of the studied U_{DC} values. However, what is more interesting when looking at the results is that the resulting combination of P_{nom} and f_{sw} with the lowest value of C_{tot} are the same independent of the 50% reduction in hardware cost or changes in the electricity price. Looking at individual results, parameters such as the filter core model and the number of winding turns changes as a function of C_e and the reduction in hardware price, but as the ferrite filter is not a dominating cost component, it has no major effect on the total result. It can therefore, be concluded that with the components included in the study, the selection of P_{nom} and f_{sw} that results in the minimum life-cycle cost is limited more by major technical factors such as the semiconductor type or inductor core material than realistic differences in the cost of hardware or the cost of electricity. For example, when the 1200 VDC GaN switch with its preliminary data is included in the calculation, the technical aspect changes. Due to the less steep E_{tot}/I_D curve, the requirement for heat sinking is reduced but the loss cost with the load curve does not change significantly due to low values of the average load current. The gate driver cost also reduces. The combination of these two factors changes the minimum result in favor of a higher value of f_{sw} and the minimum value of C_{tot} is achieved with $P_{nom} = 5.1$ kVA while $f_{sw} = 60$ kHz when $U_{DC} = 750$ V. With the lower value of $U_{DC} = 400$ V, the minimum remains at $P_{nom} = 5.1$ kVA while $f_{sw} = 40$ kHz even though the value of C_{tot} decreases. However, when the hardware price is decreased to 50%, the result with $U_{DC} = 750$ V changes back to the base case values $P_{nom} = 5.1$ kVA while $f_{sw} = 10$ kHz with a slightly lower total cost C_{tot} than with the SiC MOSFETs. If the heat sinks are dimensioned using a value of $T_{j,max} = 150$ °C instead of $T_{j,max} = 100$ °C at nominal load, the heat sink cost is reduced in all cases. However, the resulting minimum value of C_{tot} is still achieved using the same values of P_{nom} and f_{sw}. Changing the customer type to the one in Fig. 2, the minimum cost for $U_{DC} = 750$ V is achieved with $P_{nom} = 2.0$ kVA ($m = 1$) while $f_{sw} = 40$ kHz and for $U_{DC} = 400$ V with $P_{nom} = 2.0$ kVA ($m = 1$) while $f_{sw} = 20$ kHz. However, the differences between $f_{sw} = 20$—40 kHz are negligible in both cases. If we compare the minimum base case costs of the CEIs of the two different customer types, the cost of the CEI for the customer type in Fig. 1 is 2.7 €/MWh and 35 €/kVA. The same values for the customer type in Fig. 2 are 2.6 €/MWh and 42 €/kVA. The higher value per kVA for the latter customer type is mostly due to the lack of the selection of SiC switches with lower ratings, which increases the cost. However, it is interesting to note that the cost per MWh is nearly identical in both cases despite the significant differences in the load behavior and the dimensioning power. Increasing the dimensioning power by 50% changes the results for customer of Fig. 1 to 3.7 €/MWh and 31.9 €/kVA. The same values for the customer in Fig. 2 are 3.3 €/MWh and 35.8 €/kVA. Therefore, it can be concluded that over dimensioning the CEIs by 50% to better accommodate the customer's instantaneous peak load requirements can result in a significant increase in the cost per delivered energy. However, it is to be noted that the cost per kVA is slightly distorted by the previously mentioned problem in the selection of available SiC switches when the dimensioning power of the CEI is lower. If we compare the resulting values of m and f_{sw} when C_{tot} is at its minimum, the results are similar to the cases in which the base case values of P_{max} were used in the dimensioning of the CEI.

IV. Conclusion

In this paper, the life-cycle cost of a customer-end inverter that is used in a low voltage DC distribution network was analyzed. Due to the properties of the load, emphasis was put on a CEI structure that uses several single-phase modules that can also be connected in parallel and only switched on depending on the load. It was concluded that in most of the cases, a single module per phase resulted in the lowest life-cycle cost. However, because the security of the supply increases by using parallel modules, some kind of estimate for the interruption cost should be evaluated in further research as in some cases the difference in cost with two parallel modules compared to a single module was almost negligible. Even with the state of the art SiC switches, the cost of the switching losses still remain a significant factor of the life-cycle cost and limit the selection of a higher switching frequency if life-cycle cost minimization is the driving factor. It is therefore, essential to verify the calculated losses in a real world application to reach a more definite conclusion of the optimal selection of the switching frequency in this application. This will be addressed in future research topics using a laboratory prototype of the modular CEI.

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Publication III

Mattsson, A., Väisänen, V., Nuutinen, P., Peltoniemi, P., Kaipia, T., Silventoinen, P., Partanen, J.

Evaluation of Isolated Converter Topologies for Low Voltage DC Distribution

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Evaluation of Isolated Converter Topologies for Low Voltage DC Distribution

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***Abstract*— In this paper, two types of isolated converter topologies for the implementation of the galvanic isolation of a low-voltage DC network is discussed. Advantages and problems of the topologies are compared and a selection for the suitable topology for two conversion ratios, 1:1 and 2:1 is carried out. The selection is carried out by comparing the life-cycle costs of the converters if used in the low voltage DC system.**

***Keywords*— DC-DC power converters, Silicon carbide, Smart grids.**

I. INTRODUCTION

The low-voltage direct current (LVDC) system is an emerging power distribution technology under intense research and development globally and has been proposed for various applications from datacenters [1] to public utility grid distribution [2]-[5]. The LVDC distribution research network [6], [7] under study is a 1.7 km long bipolar network utilizing voltage levels of ±750 VDC. The customer-end 50 Hz AC voltage of 230/400 VAC_{RMS} is produced using a customer-end inverter (CEI), which is connected to either +750 VDC and 0 VDC or between -750 VDC and 0 VDC. The power demand in the user-end installations, and thus the load of the CEI varies in a wide range [8], which separates the distribution system application of converter systems from the common industry applications.

The DC network under study [6], [7] is implemented as a functionally unearthed (IT) network. However, the typical customer-end AC network in Finland is a functionally earthed network (TN) and therefore, the two networks have to be isolated from each other. The isolation between the two networks is one the key components of the system and therefore, requires a detailed analysis in order to find the most cost effective solution. Two types of isolation methods, namely passive and active, have previously been compared in [9]. A preliminary theoretical analysis of the suitability of one converter topologies has also been carried out in [9], [10]. However, the analysis was carried out only for a 1:1 conversion ratio. Because the CEI consists of the galvanic isolation and the AC voltage generating hard-switched inverter, the losses and cost of the inverter can be affected by adjusting the level of the intermediate DC voltage if an active isolation i.e an isolated converter, is used. Clear advantages can also be observed in the parameters and cost of some of the semiconductor switches if the voltage rating is reduced from 900-1200 VDC to 600 VDC. With a lower input voltage, the requirement for output voltage filtering of the inverter is also reduced and therefore, the losses, size, and cost of the output inductor can be reduced. The effect of the supplying DC-voltage on the life-cycle cost of the inverter was studied in [11] and it was concluded that the life cycle cost can be reduced by using a lower input voltage. However, in [11] the effect of stepping down the DC voltage on the converter was left for further study. Therefore, the purpose of this paper is (1) to evaluate the suitability of two different isolated converter topologies for the implementation of the galvanic isolation between the DC and AC networks and (2) to determine how the voltage conversion ratio of the converter affects the life-cycle cost of the converter. The losses of the converters are evaluated using an averaged load profile of a customer group that could potentially be supplied with the LVDC network. The load profile and its effect on the design of the CEI is discussed in more detail in [9]-[11].

II. CONVERTER TOPOLOGIES

Two converter topologies with slightly different advantages and disadvantages were selected for the comparison as a different topology might be suitable for the 1:1 conversion ratio but not well suited for the 2:1 step-down ratio and vice versa. Both of the selected topologies are soft switched converters which utilize the leakage inductance of the transformer either by itself or with a combination of additional capacitance to form an LC resonance circuit.

A. Phase-shifted full-bridge with a voltage doubler type secondary side rectifier

The first of the selected topologies is a phase-shifted full-bridge which has a voltage doubler type secondary side rectifier (PSFBVD) [12]. A simplified schematic of the topology is depicted in Fig. 1. The voltage doubler capacitance in combination with the leakage inductance of the transformer forms an LC resonator that shapes the current waveform and enables zero current switching (ZCS) for all the primary switches and rectifier diodes if the resonance period is selected accordingly. If the resonance period is selected to be longer than the switching period, the lagging leg switches and the rectifier diodes are still switched with ZCS but the leading leg switches are turned off with partial primary current. Zero voltage switching (ZVS) is also easily achieved for the primary switches [12]. The ZVS of the lagging leg switches can only be achieved using the magnetizing current and therefore, a certain amount of magnetizing current and freewheeling time depending on the value of the input voltage and output capacitance C_{oss} of the switches is required. A preliminary theoretical study of the PSFBVD topology for a 1:1 conversion

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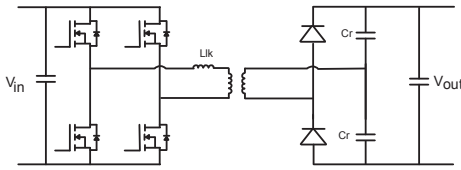

Fig. 1. Simplified schematic of the PSFBVD topology.

ratio was carried out in [9],[10], and it was concluded that the topology has some advantages that are favorable in terms of the LVDC system. Because of the utilization of the magnetizing current, ZVS can be extended to low loads and the ZVS condition is independent of the value of the load current. If the resonance period is also tuned accordingly to achieve ZCS for all the switches and rectifier diodes, the switching losses can be almost negligible and independent of the load current value. The load of the CEI contains a lot of partial load and due to the usage of a relatively high voltage of 750 VDC, a wide ZVS range as a function of the load is preferred. Because the voltage doubler in combination with the leakage inductance of the transformer acts as an LC filter, a bulky output inductor like in the conventional phase-shifted full-bridge topology (PSFB) is not required [12] which potentially decreases the cost. The output voltage is clamped to the output voltage and no snubbers are required for the output semiconductors. The number of semiconductors is low and the control of the system is simple. However, there are also some drawbacks. Due to the voltage doubler, the secondary side current stresses are comparatively high. As such, the topology does not seem well suited for a high step-down or a high current application. The output voltage regulation highly depends on the effective duty cycle D_{eff} and the resonance circuit parameters and therefore, a low value of D_{eff} will result in high fluctuations of the output voltage as a function of the load [12]. Because only the magnetizing current is responsible for the ZVS of the lagging leg switches, a high value of the magnetizing inductance might reduce the operation to partial ZVS as the output capacitances of the lagging leg switches are not fully discharged. A higher voltage and low current application such as the LVDC is more susceptible to high values of the magnetizing inductance as a high number of primary winding turns is required to reduce the value of the magnetic flux to prevent core saturation as well as get acceptable values for the core loss of the transformer. If the resulting magnetizing inductance of the transformer is high, the value of D_{eff} might be required to be decreased significantly when ZVS for the lagging leg switches is desired. A case example of the required dead time as a function of the magnetizing inductance is presented in [12]. Decreasing the value of D_{eff} will also further increase the current stresses as the same amount of energy is transferred in a shorter period of time and increases the RMS and peak currents of the semiconductors and the transformer. Because the ZVS of the lagging leg switches cannot be affected by the primary current and therefore, the stored energy in the leakage inductance, the maximum usable switching frequency f_{sw} is also limited by the amount of required freewheeling time when ZVS for the lagging leg switches is desired.

B. Dual active bridge

The second topology selected for the study is a dual active bridge (DAB) [13] that uses semiconductor switches on both the primary and secondary sides of the transformer. A simplified schematic of the topology with full-bridges on both the primary and secondary sides is depicted in Fig. 2

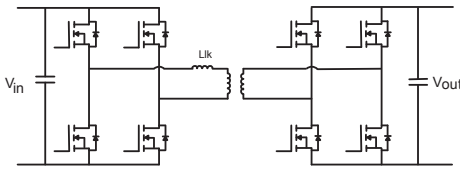

Fig. 2. Simplified schematic of the DAB topology with full-bridges.

The topology is well known and has been researched for many different types of applications such as high powered aerospace [13], energy storage systems [14], front-end interface for photovoltaic systems [15], automotive applications [16], and distribution systems [17]-[19]. The two bridges of the DAB are operated in phase shift from each other to control the amount of power flow between the primary and secondary sides of the converter. The bridges can be implemented either with full-bridges, half-bridges or a combination of both. Due to the utilization of active bridges on both sides of the transformer, the topology is capable of bi-directional power flow, which is a desirable feature in the LVDC system because it enables the customers to transfer power to the network if small-scale distributed generation, e.g. photovoltaic panels are installed on the customer side of the CEI. The two active bridges enable a variety of different types of control as the phase-shifts and the duty cycles between the two bridges and also between the bridge arms can be altered. However, if half-bridges are used on either side of the transformer, the selection of the modulation method will be limited. Different types of modulation strategies are discussed in [16], [20]-[24]. The modulation methods differ in their usable ZVS range, current stresses and dynamic performance. Among the modulation methods, the basic phase-shift modulation is the simplest but results in a reduced ZVS range if the conversion ratio differs from its nominal value especially with partial load [13]. Because ZVS turn-on is achieved using the stored energy in the leakage inductance of the transformer and the stored energy in the leakage inductance is achieved with the current at switch turn-off, a certain amount of primary current, depending on the switch output capacitance C_{oss} and the value of the leakage inductance, is required at switch turn-off. Therefore, turn-off switching loss is always generated. The ZVS turn-on as a function of the load will also be limited due to insufficient stored energy in the leakage inductance when the turn-off current is below a certain value. The selection of f_{sw} is not limited in the same way as it might be in the PSFBVD topology because the ZVS condition for all switches can be affected by the turn-off current and the energy stored in the leakage inductance. However, the limitations will come from the increased turn-off switching losses as a function of f_{sw}, feasible values for the phase-shift control, and the required dead time between the opposite switches of a switching leg. If

the complexity of the converters is compared, a clear winner cannot be so easily declared. In terms of the required number of semiconductor switches, both topologies are similar if half-bridges are used in the DAB. However, the PSFBVD will be the simpler of the two if the DAB is implemented with full-bridges. Depending on the application parameters, the DAB might require a high amount of leakage inductance and therefore, an external inductor is required in addition to the leakage inductance of the transformer making the design more complicated. If the DAB is implemented with full-bridges, the current stresses of the PSFBVD will be higher due to the current doubling effect of the voltage doubler as well as a smaller value of D_{eff}. Because the PSFBVD topology has poor output voltage regulation as a function of D_{eff}, the DAB can be more suitable for the lower intermediate voltage case of 400 VDC in which better voltage regulation as a function of the load is a requirement in order for the inverter to be able to generate the 230 VAC_{RMS} output under variable load conditions.

III. Evaluation of the Topologies

The topologies are evaluated with two voltage conversion ratios, 1:1 and 2:1. In both cases the input voltage of the converter is 750 VDC and the converter is supplying a single phase inverter that generates 230 VAC_{RMS}. A simplified diagram of the isolated single-phase CEI is depicted in Fig. 3.

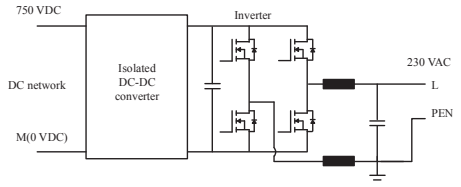

Fig. 3. Simplified diagram of the isolated single phase CEI

Because the customers are supplied with three phase AC, a minimum of three single-phase inverters and therefore, three isolated converters, are required. As previously discussed in [11], cases in which the nominal power is divided between parallel CEIs is also considered due to the properties of the load. The total required nominal power of the converters can be defined by looking at the supplied load. A typical customer group that would be supplied with the LVDC network are households that use electrical heating. An averaged load profile of such a customer group is depicted in Fig. 4. By using a confidence level of 99% we can calculate a value of $P_{\text{max}} = 15.3$ kVA for the peak power of a single customer. Therefore, if a power based tariff is assumed, the nominal power of a single converter can be calculated by

$$P_{\text{nom}} = \frac{P_{\text{max}}}{3m}, m \in [1,2,3..n], \qquad (1)$$

in which m is the number of the parallel converters. Values of $m = 1$—3 were used in the calculations. Therefore, the resulting module sizes are 5.1 kW, 2.6 kW, and 1.7 kW. The parallel converters are operated in a way that only the minimum amount of converters to supply the load are switched on. As the

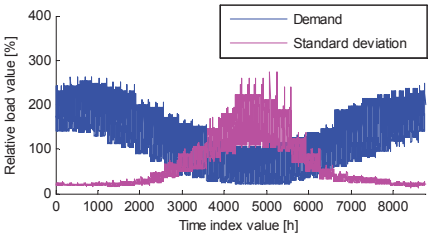

Fig. 4. An averaged load profile of a customer group in which the customers use electricity for heating and have a 300 liter water heaters [8]

CEI does not necessarily require the converter to be operated under a variable voltage conversion ratio, both converters are studied with fixed input and output voltages. Consequently, the analysis of the DAB is carried out using the basic phase-shift modulation in which only the phase-shift between the primary and secondary sides is controlled. However, if high variations in the input voltage is expected, usage of the more advanced modulation methods should be investigated due to the previously discussed drawbacks of the phase-shift modulation. The load profile of Fig. 4 is used in the loss analysis to determine the load currents for each hour of the year. The losses are calculated for a 10 year utilization period and therefore, cost of the losses is evaluated by the present value of an annuity by

$$C_{\text{loss}} = P_{\text{loss}} C_{\text{e}} \frac{1-(1+p)^{-t}}{p}, \qquad (2)$$

in which P_{loss} is losses of the converter, C_{e} the cost of electricity, p the interest rate and t the utilization period in years [25]. Values of $C_{\text{e}} = 0.05$ €/kWh, $p = 5\%$ and $t = 10$ are used in the calculations. In order to calculate the losses we first define the RMS currents of the converters. The RMS currents of the PSFBVD topology are calculated by

$$I_{\text{RMS}} = \sqrt{\frac{k}{T}\int_0^{\sqrt{L_{\text{lk}}C_{\text{r}}}\pi}\left(n\frac{\omega_{\text{r}} I_{\text{out}} T}{2}\sin(\omega_{\text{r}} t)\right)^2 dt}, \qquad (3)$$

in which I_{out} is the output current of the converter, C_{r} the resonance capacitance, ω_{r} the resonance frequency, n the turns ratio of the transformer and k a variable that denotes if the value is calculated for the transformer ($k = 2$) or the semiconductors ($k = 1$) [26]. The RMS currents of the DAB with the basic phase-shift modulation are calculated by

$$I_{\text{RMS}} = \sqrt{\frac{k}{T}\left(\int_0^{T_\varphi}\left(i_{L,0} + \frac{(V_1 + nV_2)t}{L}\right)^2 dt + \int_{T_\varphi}^{\frac{T}{2}}\left(i_{L,T_\varphi} + \frac{(V_1 - nV_2)(t - T_\varphi)}{L}\right)^2 dt\right)}, \qquad (4)$$

in which V_1 is the input voltage, V_2 the output voltage, L the inductance responsible for the energy transfer, $i_{L,0}$ the value of

the inductor current at time instant $t = 0$ and $i_{L,T\phi}$ the value of the inductor current at time instant $t = T_\phi$. Again, the variable k denotes if the RMS current is calculated for the semiconductors or the transformer. (4) is derived from the general RMS current equation presented in [27] by integrating the current waveform. The current $i_{L,0}$ is defined by

$$i_{L,0} = \frac{\pi(nV_1 - V_2) - 2\varphi nV_2}{4\pi f_s L}, \tag{5}$$

and the current $i_{L,T\phi}$ by

$$i_{L,T_\phi} = i_{L,0} + \frac{(V_1 + nV_2)t}{L} \tag{6}$$

[28]. For The DAB loss calculation, the current at the switch turn-off is also required. If the voltage conversion ratio of the DAB is at its nominal value, the current at which the transistors are turned off is also calculated by (5). If the conversion ratio starts to differ from its nominal value, $i_L(t)$ at $t = T/2$ needs to be calculated due to the resulting differences in the turn-off currents at these two time instants. Because the DAB topology relies on the value of L to realize the power transfer between the primary and secondary sides, the required values of L were evaluated. The required L as a function of f_{sw}, P_{nom} and the DAB primary and secondary side bridge configuration with a nominal conversion ratio of 1:1 is depicted in Fig. 5. As depicted by Fig. 5, using a full-bridge on the primary side results in high values of L and a high value of external inductance in addition to L_{lk} becomes necessary. Because the turn ratio of the transformer also changes when the bridges are changed from a full-bridge to a half-bridge, the results are independent of the configuration of the secondary side bridge. Consequently, the results are the same for the 2:1 conversion ratio. However, it is worth noting that the resulting current stresses and ZVS conditions differ in each case. The transformers for both of the studied converter topologies were calculated from a selection of AWG 18—52 litz wires with 1—11250 strands [29] and ETD and PM cores made out of N87 and N97 ferrite [30]. Prices of the cores are referenced from [31] and the cost of the litz wire is estimated by the price of copper per ton [32]. Because of the high values of L that are required for the DAB, external high frequency AC inductors were also designed using gapped N87 ETD ferrite cores [30]. The same selection of litz wires as in the transformer design was used in the inductor winding calculation. The AC resistance of the litz wires were calculated similar to [33] in both cases. Both the transformer and the inductor were dimensioned for a maximum temperature rise of $\Delta T = 50$ ˚C. The configurations of the transformer and the inductor were then selected based on the minimum life-cycle cost when all the possible combinations of the included cores and winding wires were considered. The switches of the DAB are operated under ZVS while

$$\frac{1}{2} I_{ZVS}^2 L \geq \Sigma \frac{1}{2} C_{oss} V_{DS}^{\ 2}, \tag{7}$$

in which I_{ZVS} is the current at turn-off, C_{oss} the output capacitance of a single switch and V_{DS} the voltage across the switch when it is in the off-state. However, even if the inequality of (7) is fulfilled, some amount of switching losses are still generated because the switches are always turned off with current that changes as a function of the load current value. The turn-off current also depends on the fluctuations in the conversion ratio but as the conversion ratio was assumed to be constant this effect is not included in the analysis. Therefore, the switching losses under ZVS are calculated by

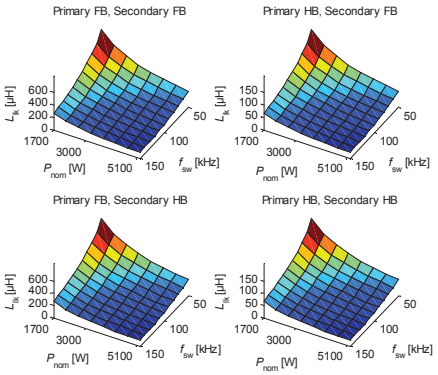

Fig. 5. Required values of L as a function of f_{sw} and P_{nom} for all the four possible combinations of full-bridges and half-bridges of the DAB with a nominal conversion ratio of 1:1. The inductances are calculated so that the nominal power is delivered when $\phi = 0.20$, i.e. 20% of T. Abbreviation FB denotes a full-bridge and HB a half-bridge.

$$P_{sw} = E_{off}(I_{zvs})) \cdot f_{sw}, \tag{8}$$

in which E_{off} is the turn-off energy of the switch. During partial load the value of I_{ZVS} gradually reduces and depending on the values of L, C_{oss} and V_{DS}, the inequality of (7) is no longer fulfilled and as a result the converter will operate under hard switching. The switching losses under hard switching are calculated by

$$P_{sw} = (E_{on}(I_{zvs}) + E_{off}(I_{zvs})) \cdot f_{sw}, \tag{9}$$

in which E_{on} is the turn-on energy of the switch. 1200 VDC SiC MOSFETs [34] are used in the primary side bridge calculations of both converters. However, in the 2:1 conversion ratio case, a selection of 600 V switches [35] were also included in the DAB secondary side bridge calculations due to a significant reduction in semiconductor price. Because no switching energy curves were available for the 600 V switches, the switches were modeled in Orcad Pspice and the switching energies were simulated using a half-bridge double pulse tester. The required freewheeling time for ZVS in the PSFBVD topology was determined based on the values of L_m, I_m and time related output capacitance $C_{oss(tr)}$ of the switches while I_m was assumed to be constant during the ZVS transition. The maximum effective duty cycle D_{eff} was then calculated as a function of f_{sw} and $C_{oss(tr)}$ so that the ZVS condition is always fulfilled for all the switches. The LC resonance is tuned to be identical to D_{eff} and consequently the switches are turned off with almost zero current equal to I_m at the switching instant.

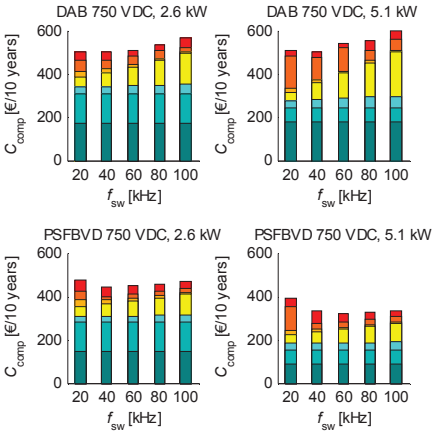

Fig. 6. Total life-cycle costs of the DAB and PSFBVD topologies as a function of P_{nom} and f_{sw} while P_{nom} is calculated as a function of the parallel modules as defined by (1). The input voltage is 750 VDC and the output voltage is 750 VDC in each case. The different colors of the bar graphs are from top to bottom: transformer loss cost, transformer material cost, external inductor (DAB) or resonance capacitor (PSFBVD) cost, semiconductor loss cost (switching and conduction), heatsink cost, gate drivers and control cost, and semiconductor cost. Results for the P_{nom} = 1.7 kW case are not plotted as the results increase compared to the P_{nom} = 2.6 kW case with both converter topologies.

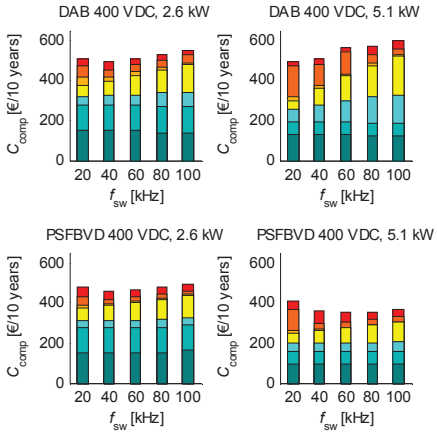

Fig. 7. Total life-cycle costs of the DAB and PSFBVD topologies as a function of P_{nom} and f_{sw} while Pnom is calculated as a function of the parallel modules as defined by (1). The input voltage is 750 VDC and the output voltage is 400 VDC in each case. The different colors of the bar graphs are from top to bottom: transformer loss cost, transformer material cost, external inductor (DAB) or resonance capacitor (PSFBVD) cost, semiconductor loss cost (switching and conduction), heatsink cost, gate drivers and control cost, and semiconductor cost. Results for the P_{nom} = 1.7 kW case are not plotted as the results increase compared to the P_{nom} = 2.6 kW case with both converter topologies.

Therefore, the switching losses in the PSFBVD case consist only of turn-off losses as defined by (8) while $I_{zvs} = I_m$ and are not affected by the load current value. Because D_{eff} affects the RMS currents, $C_{oss(tr)}$ discharge time is taken into consideration also in the transformer design. The conduction losses of the switches are calculated based on the values of the on-state resistance $R_{ds,(on)}$ and RMS currents defined by (3) and (4) while the load current is defined by the curve in Fig. 4. The junction temperature T_j and $R_{ds,(on)}$ is estimated to increase linearly as a function of the load so that $T_j = 25$ °C at 0% load and $T_j = 100$ °C at 100% load and $R_{ds(on)} = R_{ds(on)}(T_j(P_{load}))$. A selection of SiC diodes [36] are used in the calculations for the secondary side rectifier of the PSFBVD topology and the diode losses are calculated by

$$P_{diode} = I_{avg} V_f + I_{RMS} R_f , \qquad (10)$$

in which I_{avg} is the average rectified current, V_f the diode forward voltage and R_f the resistance of the diode. Prices for all the semiconductors are referenced from [37],[38]. Prices for heat sinks were determined as a function of the required thermal resistance when the maximum allowed junction temperature at nominal load is $Tj = 100$ °C while the ambient temperature is $T_{amb} = 50$ °C as this roughly represents the maximum cabinet temperature of the CEI during summer. Prices for the resonance capacitors of the PSFBVD are referenced from [39]. Because the selection of the amount of output capacitance is affected more by the inverter and the amount of input capacitance by the network impedance and network stability criteria and therefore, result in similar bulk capacitance values independent of the converter topology and f_{sw}, the cost of the DC capacitors is not included in the calculations. Isolated power supplies are assumed for the high-side switch gate drivers only and the gate driver cost for a single H-bridge is estimated to be 16.9 € [40][41]. From the calculated results, the solutions that result to the minimum life-cycle cost i.e. the minimum sum of the component and loss costs during the 10 year utilization period were selected. Fig. 6 depicts the total costs of the converter as a function of P_{nom} and f_{sw} for the 1:1 conversion ratio when the topology and its configuration resulting in the minimum life-cycle cost during the 10 year utilization period is selected in each case. As depicted by Fig. 6, the minimum cost in the DAB case is found with a module size of $P_{nom} = 2.6$ kW while $f_{sw} = 40$ kHz and when half-bridges are used as the primary and secondary side bridges. However, if we compare the minimum values between module sizes $P_{nom} = 2.6$ kW and $P_{nom} = 5.1$ kW, the differences are negligible. The PSFBVD results in a lower value of the life-cycle cost compared to the DAB and the minimum cost is found with a module size of $P_{nom} = 5.1$ kW while $f_{sw} = 60$ kHz. The main reason for the significant differences between the two topologies in the $P_{nom} = 5.1$ kW case is that MOSFETs with a higher current rating are selected for the DAB due to the half bridge design. However, the resulting total cost is still lower compared to the cases in which the DAB is implemented with full-bridges mostly due to the increased total gate driver and semiconductor cost when higher number of switches is used. Fig. 7 depicts the total costs of the converter as a function of P_{nom} and f_{sw} for the 2:1 conversion ratio when the topology

and its configuration resulting in the minimum life-cycle cost during the 10 year utilization period is selected in each case. When the converters are designed to the lower output voltage of 400 VDC, the minimum cost in the DAB case is found with a module size of P_{nom} = 2.6 kW while f_{sw} = 40 kHz. Again, the PSFBVD results in a lower value of the life-cycle cost and the minimum cost is found with a module size of P_{nom} = 5.1 kW while f_{sw} = 80 kHz. With the lower output voltage of 400 VDC, MOSFETs with a lower voltage rating can be selected on the secondary side of the DAB decreasing the cost. In the PSFBVD topology, higher current rating diodes are selected but because at the same time the breakdown voltage is lowered to 650 VDC, the cost of the diodes remains similar. Based on the results, decreasing the output voltage from 750 VDC to 400 VDC increases the minimum life-cycle cost of the PSFBVD converter by 9% but decreases the life-cycle cost of the DAB by 2% mostly because cheaper switches with a lower voltage rating can be used on the secondary side bridge of the DAB. However, the PSFBVD still results in a lower total cost compared to the DAB. It is worth mentioning that because the resonance capacitors of the PSFBVD conduct relatively high RMS currents, the selection of the capacitors might become problematic in the 400 VDC output voltage case when the required nominal power and capacitor RMS current increase. Because component prices quoted in [31],[37]-[39] do not well reflect the production cost if the converters were mass produced, the converters were also designed using a 50% reduction in component cost to determine how a significant reduction in component cost affects the results. Interestingly, the combinations of P_{nom} and f_{sw} resulting in the minimum life-cycle cost are very similar. However, if we look at individual results, for example the configuration of the transformer resulting in the minimum life-cycle cost changes quite considerably. In the hardware cost reduced 750 VDC output voltage case the minimum life-cycle cost is found using the PSFBVD with a module size of P_{nom} = 5.1 kW while f_{sw} = 60 kHz. In the hardware cost reduced 400 VDC output voltage case the minimum is also found using the PSFBVD with a module size of P_{nom} = 5.1 kW while f_{sw} = 60 kHz. When the hardware prices are reduced by 50%, decreasing the output voltage increases the life-cycle cost of the PSFBVD by 8% but the life-cycle cost of the DAB remains almost identical. Looking at individual cost components the inductor in the DAB case and the resonance capacitors in the PSFBVD case do not seem to be significant cost factors. Using the prices quoted in [31],[37]-[39], the hardware cost is clearly the most dominating cost factor in all cases. However, when the hardware cost is reduced further by 50%, the loss cost starts to be a significant cost factor especially when the value of f_{sw} is increased. Based on the results, the PSFBVD topology seems more suitable to be used with higher value of f_{sw} mostly due to the high ZVS range as well as low turn-off loss compared to the DAB. If bidirectional power flow and output voltage regulation under variable input voltage is not a requirement, the PSFBVD topology is a good candidate for the studied application. However, if these properties are required, a compromise in the life-cycle cost might become necessary and the selection will lean toward the DAB.

CONCLUSIONS

In this paper, two different types of isolated converter topologies were compared in order to determine their feasibility for the implementation of the galvanic isolation in a low voltage DC distribution network. Because of the properties of the load, cases in which several converters can be connected in parallel and switched on depending on the load were also considered. The life-cycle costs of the converters during a 10 year utilization period were compared to determine which of the two topologies could result in a lower total cost. Both of the topologies were considered for two different voltage conversion ratios, 1:1 and 2:1 while the input voltage was 750 VDC in both cases. With the assumption that the converters are operated with a fixed conversion ratio while the converter is supplying a single phase inverter which has a regulated output, it was concluded that the PSFBVD topology resulted in the lowest life-cycle cost in both conversion ratio cases. Lowering the output voltage from 750 VDC to 400 VDC increased the life-cycle cost of the PSFBVD by 9% while the life-cycle cost of the DAB decreased by 2%. Even though the DAB requires a relatively high amount of inductance with the studied application parameters and therefore, in most cases an external inductor, the inductor was not found to be a significant cost factor. The hardware cost dominated the life-cycle cost of both converters and was higher in the DAB case. However, when the hardware cost was reduced by 50% in the design process to better approximate production prices the loss cost became a significant factor especially when the switching frequency was increased. Based on the results the PSFBVD topology is a good candidate for the studied application if bidirectional power flow and output voltage regulation under variable input voltage are not required. Further research topics will include characterizing both converters with laboratory prototypes and comparing their life-cycle costs when the inverter is included in the analysis. The calculated and simulated switching losses also need to be verified in practice as they significantly affect the results especially in the DAB case when the switching frequency is increased.

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Publication IV

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