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Heat Flux Sensor Measurement Electronics System Design for Wearable Electronics Application

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MSc Thesis
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Abstract

In this thesis, the development process of instrumentation for a heat flux sensor in human measurement application is documented. The system includes amplification with adjustable gain for a low frequency signal in μV range, data conversion from analog to digital and data bus for saving and processing the data. The system was implemented using a SAR ADC with preceding instrumentation amplifier and an analog low-pass filter. A LTC6915 instrumentation amplifier was used for its good DC performance and large range of SPI programmable gain. Low-pass filter with Sallen-Key topology and Butterworth response was implemented using a LTC2066 operational amplifier. An OPA835 wide band operational amplifier was used as a SAR ADC driver. The SAR ADC is 14-bit ADS7056, which was selected for its small footprint and very low power consumption at the selected 120 Hz sampling rate. A temperature measurement was included using a LMT70 analog temperature sensor IC and another ADS7056 for the data conversion. The system is controlled by Atmel ATtiny87 microcontroller and the data is sent for processing and saving via I2C bus. A MAX14959 logic level shifter was included on the I2C bus to accomodate 3 V - 5 V logic levels. The analog amplifiers are powered from a 3.0 V ISL21010 low power voltage reference, the ADC reference is established with a 2.5 V REF3325 low power reference and digital supply is generated using a 3.0 V LP5907 regulator. The system is powered from 2032 sized rechargeable 3.6 V lithium battery. System calibration function was included to compensate for temperature drift of all circuit components. The circuit was fitted on two layer PCB and on stacked design with two PCBs. Performance of the final design was evaluated by measuring the offset voltage drift in 5 °C to 50 °C temperature range and noise performance was assessed by measuring and calculating ENOB of the system. The drift performance without system calibration was found to be within the specifications of the voltage references and with system calibration enabled, the drift was reduced to less than 1 LSB. The noise performance was found to be worse than expected with ENOB of $\simeq$ 11-bits for system gains < 512. Cause for the noise was deduced to be the signal routing extending to the ground plane in bottom layer of the PCB thus affecting the current paths in the ground plane. Also, the ADC driver was found to be unnecessary in the application adding to the noise further.

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Lämpövuoanturin mittauselektroniikan suunnittelu puettavan elektroniikan sovellukseen

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Hakusanat: lämpövuoanturi, instrumentointi, puettava elektroniikka

Tiivistelmä

Opinnäytetyössä dokumentoidaan ihmisen mittaamiseen soveltuvan lämpövuoanturin liityntäelektroniikan suunnittelu. Järjestelmä koostuu μV tasoisille tulosignaaleille soveltuvasta DC-vahvistimesta, A/D-muuntimesta ja dataväylästä datan muokkaammista ja tallentamista varten. Toteutuksessa käytettiin instrumentointivahvistinta, aktiivista alipäästösuodinta ja SAR arkkitehtuurin A/D-muunninta. Instrumentointivahvistimeksi valittiin LTC6915 sen hyvien DC-spesifikaatioiden ja ohjelmallisesti säädettävän vahvistuksen perusteella. Alipäästösuodin toteutettiin Sallen-Key kytkentätopologiaa ja Butterworth vastetta käyttäen LTC2066 operaatiovahvistimella. Laajakaistainen OPA835 operaatiovahvistin valittiin A/D-muuntimen puskurivahvistimeksi. A/D-muuntimeksi valittiin 14-bittinen ADS7056 sen pienen fyysisen koon ja asetetulla 120 Hz näytteistystaajuudella saavutettavan erittäin pienen virran kulutuksen vuoksi. Kytkentään sisällytettiin lämpötilan mittaus käyttäen analogista mikropiirisensoria LMT70 ja toista ADS7056 A/D-muunninta LMT70-piirin lämpötilan funktiona muuttuvan lähtöjännitteen A/D-muunnokseen. Mikrokontrolleriksi valittiin Atmelin ATtiny87, jota käytetään A/D-muuntimien lukemiseen SPI väylästä ja datan edelleen lähettämiseen I2C väylälle. I2C väylään lisättiin myös MAX14595 logiikkatasomuunnin, joka mahdollistaa 3 V - 5 V logiikkatasojen käytön I2C väylään liitettävissä laitteissa. Käyttöjännitteet analogiavahvistimille luodaan 3.0 V ISL21010 jännitereferenssillä, A/D-muuntimen referenssinä käytetään 2.5 V REF3325 jännitereferenssiä ja digitaalisten piirien 3.0 V käyttöjännitteet toteutettiin LP5907 jänniteregulaattorilla. Teholähteenä toimii 3.6 V akku 2032 nappipariston koteloinnilla. Kytkentään toteutettiin kalibrointitoiminto, jolla kytkentäkokonaisuuden lämpötilan muutoksesta johtuva ryömintä voidaan kompensoida. Kytkentä toteuttiin kahdelle päällekäin asennettavalle kaksikerrospiirilevylle. Kytkennän suorituskyky todennettiin mittaamalla asettelujännitteiden ryömintä lämpötila-alueella 5 °C - 50 °C. Kytkennän kohina todennettiin mittaamalla ja laskemalla järjestelmän efektiivinen resoluutio (ENOB). Mitattu ryömintä ilman kalibrointitoimintoa todettiin olevan kytkennän komponenteille annettujen raja-arvojen sisällä ja kalibrointitoimintoa käyttämällä ryöminnän vaikutus saatiin eliminoitua kokonaan, eli alle 14-bitin resoluution. Efektiiviseksi resoluutioksi saatiin alle 512 vahvistuksilla noin 11-bittiä. Kohinan lähteeksi epäiltiin maatasoa, jota ei pystytty tiheän komponenttisijoittelun vuoksi pitämään riittävän yhtenäisenä. A/D-muuntimen puskurivahvistin todettiin sovelluksen taajuusalueella tarpeettomaksi.

Contents

Nomenclature

ppm	parts per million
τ	RC-circuit time constant
AV_{DD}	Analog supply voltage
DV_{DD}	Digital supply voltage
f_s	Sampling frequency
f_{-3dB}	-3 dB filter roll-off frequency
f_{CPU}	Microcontroller clock frequency
q	heat flux
S_0	Heat Flux Sensor volt-watt-sensitivity
V_0	Input voltage zero level
v_M	$v_{HFS} + V_0$
V_{BIAS}	Analog circuit reference voltage
v_{HFS}	Heat Flux Sensor voltage
V_{os}	Offset voltage
v_{out}	System calibrated voltage output
V_{REF}	Analog-to-Digital Converter reference voltage
ADC	Analog-to-Digital Converter
BP	Biopotential
CMMR	Common Mode Rejection Ratio
DFT	Discrete Fourier Transform
DNL	Differential Nonlinearity
EMI	Electromagnetic Interference
ENOB	Effective Number of Bits
FSR	Full Scale Range

GBW Gain Bandwidth Product

HF Heat Flux

HFS (Gradient) Heat Flux Sensor

I2C Inter-Integrated Circuit (I^2C) Serial Data Bus

IA Instrumentation Amplifier

INL Integral Nonlinearity

LSB Least Significant Bit

NAD Noise and Distortion

OA Operational Amplifier

PCB Printed Circuit Board

SAR Successive Approximation Register

SINAD Signal to Noise and Distortion Ratio

SPI Serial Peripheral Interface bus

SPS Samples Per Second

Chapter 1

Introduction

1.1 Background

Heat flux sensors (HFS) have found applications for example in industrial boilers [1] and electric machines [2]. Gradient heat flux sensors produce a transverse electric field that is proportional to the heat flux through the sensor. HFSs based on thermocouples, which generate electric field that is colinear to the heat flux, also exists [3]. In this thesis only the transverse type sensors are dealt with and the abbreviation HFS is used to imply to gradient heat flux sensors.

Qhealth, a research project implemented in collaboration by Lappeenranta University of Technology and University of Jyväskylä and funded by Business Finland (formerly Tekes), aims for commercialization of heat flux sensors for human measurements. The proprietary heat flux sensor developed for the application and also currently commercially available heat flux sensors require instrumentation for signal conditioning and data conversion to be usable for data gathering. The development process of the electronics design for a prototype is documented in this thesis. The mechanical design and other aspects of the prototype device are not in the scope of this work and are not discussed here. The prototype is used for research purposes to establish the information obtainable from the heat flux data.

HFSs in human heat flux measurement are assumed to produce DC or very low frequency voltages at μV levels. The sensor and the connecting electronics are expected to operate in varying environmental conditions during different human activities. The electronics for the application requires thus DC accuracy independent of operating temperature, low power consumption, small size & weight and tolerance for differing levels of electromagnetic interference (EMI). Some of these requirement are conflicting (for example DC accuracy and low power) and neccessitate careful component selection. The conflicting requirements make also compromises unavoidable.

1.2 The Objective

The goal of this thesis project is to design electronics for a wearable human heat flux measurement system using commercial and proprietary HFSs. The system must include

- amplification for signal in μV range

- data conversion from analog to digital
- a communication bus for saving and processing the data.

The system is designed for a human heat flux research application aimed to determine what kind of information can be actually extracted from the data. Where possible, design solutions are chosen so that the design could be used with small adjustments for a commercial measurement system. Electronic characteristics of the proprietary HFS are currently unknown and the circuit is designed for specified characteristics of GreenTEG HFSs[4]. The software development is not reported in detail to keep the scope of the thesis manageable.

1.3 Research Methods

The general approach for the thesis was design science oriented, although the goal was to design a circuit based on known characteristics of the sensors and general requirements of the application instead of improving existing solution, as is often the case in design science.

1.3.1 Literary Sources

Design choices were made based on information obtained from component manufacturer datasheets & application notes and applicable textbooks. Peer reviewed scientific literature was relied on mainly for establishing the electrical properties of the signal source – a gradient heat flux sensor. Literary review of academic articles was also used to estimate the applicability of instrumentation solutions related to biopotential measurements.

The general requirements for the measurement system were composed based on discussions with Heikki Kyröläinen, Heikki Peltonen and Mika Silvennoinen from Sport and Healt Sciences faculty in University of Jyväskylä responsible for conducting the research on relationship between heat flux measurements and physical activity & various human physiological responses.

1.3.2 Circuit & PCB Design

Literary review was done to establish applicable methods for minimizing DC error sources and increasing EMI tolerance. LTspice circuit simulation software was used to simulate critical subcircuits and PCB design was designed using National Instruments Multisim & Ultiboard software packages. PCB assembly was outsourced to a professional small scale manufacturer. Microcontroller programming was done using Atmel AVRISP MK2 and Atmel ICE programming tools & Atmel Studio 7.0 sofware package.

The measurement setups for the final circuit design are described in detail in chapter 5.

1.4 Structure of the Thesis

The thesis is structured as follows: The general & technical requirements, analysis of the signal source properties and applicability of the design methods used in medical instrumentation are discussed in the next chapter. In chapter 3, component specifications of semiconductors and passive components relevant for the application are established and the details of the circuit design solutions are documented. Design solutions for the PCB design are discussed in the following chapter 4. The final design and results of the circuit performance measurements are presented in chapter 5. Finally, the circuit performance is further analyzed and final conclusions are drawn in chapter 6. The Appendix includes the selection tables for applicable SAR ADCs, operational amplifiers, instrumentation amplifiers & voltage references and schematic of the final circuit design.

Chapter 2

Characteristics of the Measurement System

In this chapter, the general & technical requirements set by the application, the electrical characteristics of the signal source and applicability of design solutions in medical instrumentation are evaluated.

2.1 General Requirements

From a practical perspective, following properties are required for the measurement system:

- Wearable: i.e. small sized & light
- Continuous battery powered operation for > 24 hours
- Adjustable gain for sensors with different output voltage levels
- Output: Serial communications bus for saving the acquired data

2.1.1 Operating Conditions

Temperature Range

Assuming the device is held on direct contact to skin, the temperature range is limited compared to many other applications. To avoid a damage to the skin, absolute extreme temperatures must be 10 °C - 45 °C [5]. In a hot environment, temperature inside the enclosure could rise higher than 45 °C but the stated range can be used to estimate performance of the electronic components.

Other Environmental Considerations

The skin contact to the device enclosure can cause moisture to condense on the PCB when operated in low temperature or high moisture conditions. Any moisture on the PCB will affect negatively the measurement precision by increasing leakage currents on the PCB creating voltage offset. To prevent the leakage currents, the PCB should be covered with epoxy or silicon to seal the

board from moisture ([6] page 11). Care must be taken to ensure proper cooling for power dissipating components. Sealing is not an option for a first draft prototype since measurements must be made to verify the designed operating specifications.

2.2 Technical Requirements

Several technical requirements for the electronics are currently unknown. Following boundary conditions derived from the general requirements above that can be set at this time are

- $V_{DD} < 3.0\,\mathrm{V}$ single supply operation and low supply currents for active components to enable battery operation
- Low temperature dependent drift of circuit parameters (offset voltages & currents, impedances, etc.)
- Low noise (limiting value set by chosen ADC resolution)

Dynamic range and frequency range of the measured signal are currently unknown. The frequency range was assumed to be < 50 Hz to enable efficient low pass filtering to prevent mains noise contamination of the data.

2.3 Heat Flux Sensor Equivalent Circuit

Physics of HFS operating principles are not discussed in detail here, for which detailed treatment can be found from several other sources [3, 7, 8, 9]. From electronics design point of view, knowledge of electrical properties of a HFS is essential.

The form of equivalent circuit can be deduced from known physical properties and previously obtained HFS measurement results. At temperatures around 0 °C, any conducting medium has an intrinsic series resistance > 0 ohms. For the GreenTEG HFSs, the series resistance is in the range of tens or hundreds of ohms [4]. Every physical source has also a finite shunt resistance but this is assumed to be large enough to neglect. Heat flux through a HFS produces a voltage v_{HFS} based on equation

$$v_{HFS} = q_z S_0 A, \tag{2.1}$$

where q_z is the heat flux in z-direction, S_0 is empirically obtainable volt-watt-sensitivity of a HFS and A is area of the sensor [10]. Equation (2.1) implies that the equivalent circuit cannot contain series capacitance or shunt inductance since that would result zero output (a series capacitance would block DC and shunt inductance would short DC-voltage) for a constant q_z – a contradiction to modeling equation (2.1). A shunt capacitance formed between different parts of the thermopairs is unavoidable and should be included in the equivalent circuit. Also, a series inductance can be formed along the conducting path.

Based on the deduction above, the complete equivalent circuit for HFS comprises of voltage source with series resistance followed by series inductance & shunt capacitance. The same form was derived in [2] (page 41) with the measured capacitance values in the order of pF and inductance in nH. With frequency range of < 50Hz in the current application, reactances of such order of magnitude can be safely neglected. Therefore, applicable equivalent circuit consists of a voltage source v_{HFS} with series resistance of tens or hundreds of ohms.

2.4 EMI Considerations in Human Measurements

2.4.1 Medical Instrumentation

Electronics design for a biomedical measurement systems was considered closely related to the required instrumentation in heat flux measurements. The established equivalent ciruits for skin-electrode interface of biopotential electrodes was considered beneficial to anticipate possible coupling routes for EMI in the HFS application. Also, electronics design solutions for very low level signals and EMI prevention for example in ECG measurement was considered applicable to HFS instrumentation. To this end, a literary review was done.

Biopotentials

Biopotential (BP) electrodes are transducers in a sense that they transform body current consisting of ions to electron current in the electrode, wires and the following electronics [11]. Equivalent circuits for a electrode-skin interfaces for different electrodes are shown in figure 2.1.

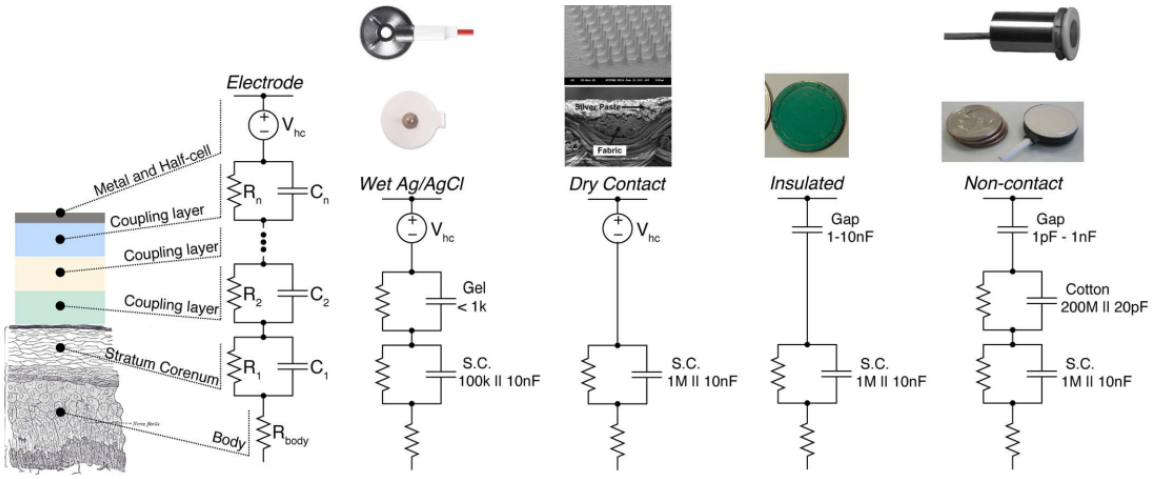


Figure 2.1: Equivalent circuits for biopotential sensor electrode-skin interfaces [12].

In figure 2.1, the equivalent circuits correspond to a half-potentials and to form a complete circuit, two points are needed to measure the potential difference between the half-potentials. This is implied by the fact, that the lower terminal to which the load should be connected if using one electrode is seen in 2.1 to be inside the body – clearly impossible connection to be physically possible. The signal source is thus a series connection of equivalent circuits presented in figure 2.1 and the measured voltage is the difference in the half-potentials of the two points.

The equivalent circuits in figure 2.1 reveal the EMI coupling paths associated with BP measurements. The first aspect that makes the EMI prevention difficult are the high source impedances. High series resistance and low capacitance values of the signal source require a very high input impedance from the amplifier input circuit. For the capacitively coupled non-contact electrodes input impedances as high as > 1 Tohm are required to achieve needed low frequency response for ECG measurements [13]. This makes the input circuit susceptive to capacitively coupled EMI [14].

The first stage used to amplify the weak voltage signal in BP measurements is usually differential amplifier or instrumentation amplifier to establish effective common mode rejection. This approach is common in instrumentation in general and also applicable to HFS instrumentation.

As stated above, in electric circuit terms, human body is connected in series with the voltage source in BP measurements. This notion is important when considering a HFS operating unintentionally as BP sensor. Since the equivalent circuit of BP sensor cannot be formed accidentally when using a single HFS, by appearing in series with the HFS voltage source v_{HFS} and its internal resistance, application of the BP equivalent circuits to modelling EMI coupling in HFSs is not feasible. The signal source being formed by two parts in BP measurements with separation measured in tens of centimeters and large differences in the electrode impedances, destroys the input circuit impedance & layout symmetry essential for rejection of common mode and RF & mains frequency interference. This type of design problems can be avoided more easily in measurement setups for heat flux sensors.

Motion artifacts in measurements using BP electrodes are result of mechanical disturbance in the electrode-skin interface, affecting the charge distribution of the interface [11]. According to [11], motion artifacts in BP electrodes are largely on the low frequency range. The frequency range is not specified but it is mentioned to affect most the ECG measurement, which in figure 2.2 can be seen to reach DC. Based on this, the referred 'low frequencies' in this case are close to DC. The generation mechanism is physically different from HFS application where the possible motion artifacts are result from changes in thermal energy transfer of the skin-sensor interface or just handling noise of analog signal cables. Reliable conclusions about the frequency range of the motion artifacts in HFS application thus cannot be made based on research on BP electrodes.

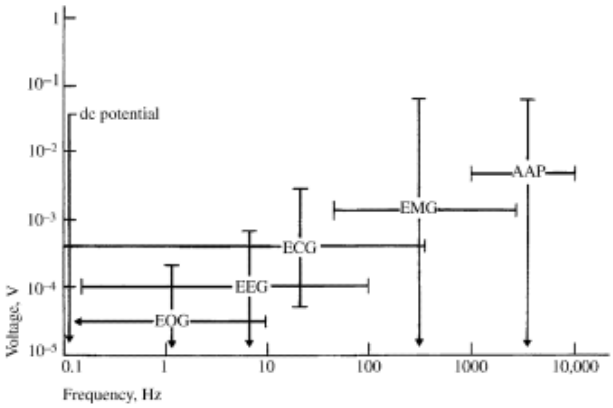


Figure 2.2: Frequency ranges of different biopotential measurements. [11]

Additionally, electronics used in BP measurements are generally grounded, whereas HFS instrumentation in the current application is to be battery powered and thus floating. Methods to prevent common mode interference in BP measurements are thus not applicable to HFS instrumentation.

From the above discussion, it can be concluded that applicability of circuits and equivalent mod-

els of electrode-skin interface used in ECG, EEG, EMG applications are very limited since HFS operates on different principles in many respect.

Chapter 3

Circuit Design

Based on the stated general and technical requirements in the previous chapter, the general goal is thus to design a low power, temperature independent DC-amplifier with data conversion. Details of the component selection and circuit design are presented in the following sections. For schematic presentation of the designed subcircuits, refer to the complete circuit schematic in appendix B figures B.1 and B.2

3.1 General Structure

For a system with possibly several simultaneously operating sensors, the general system structure most tolerant to EMI was considered to be the following: Multiple enclosures containing HFS + Amplification + ADC with I2C lines connecting to separate unit with communications for data saving based on development board with GSM/Bluetooth/etc. This structure avoids long low level analog signal cables, which are susceptive to EMI and cable handling noise. Also, interference from the Bluetooth or GSM antenna is reduced when the antenna is placed to a separate unit. Designing an antenna (to avoid using separate device for communications) to the outer surface of the HFS enclosure is not possible in the scope of the current project.

Sigma-delta and SAR ADC architectures require different approach for the surrounding circuit design. The current design uses SAR (see next subsection for selection criteria) and requires external filtering and design solutions for accomodating the ADC sampling capacitor currents. Block diagram built around SAR ADC is shown in figure 3.1.

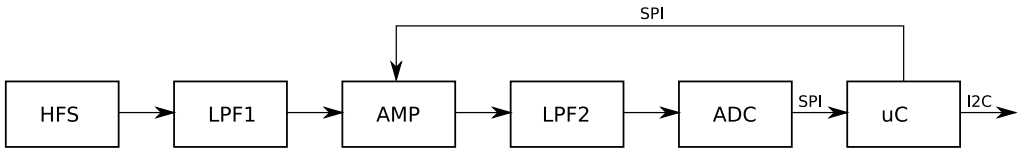


Figure 3.1: Block diagram of system with SAR ADC. LPF1 is the passive IA input filter and LPF2 is combined active filter and ADC driver. AMP contains instrumentation amplifier with gain programmable via SPI bus. The captured data is made available on I2C bus.

To avoid aliasing of 50 Hz mains interference, sampling rate should be > 100 Hz. Thus, sampling

frequency f_s = 120 Hz was selected for the system. In an environment with 60 Hz mains frequency, sampling rate should be increased accordingly.

The system is powered from 2032 size coin cell rechargeable Li-ion battery with 80 mAh capacity [15], selected for its small physical size. Also, nominal voltage of 3.6 V and cut off voltage of 3.0 V was considered improvement from button cell batteries that have 3.0 V nominal voltage and 2.0 cutoff voltage. Lower voltages of batteries are problematic for analog amplifiers, because accurate devices require frequently > 2.7 V supply voltages.

3.2 Subcircuits

Details of the component selection and circuit design solutions for the subcircuits in figure 3.1 and powering (not shown in figure 3.1) of the device are reported in this section.

3.2.1 ADC

In [16], the widely used ADC architectures are compared. In summary, sigma-delta architecture is from many respects the most suitable choice for low frequency and high resolution data acquisition. The main caveat in the current application with sigma-delta architecture is that it requires more time invested in software development compared to SAR ADCs. The SAR architecture can be used succesfully in many applications and offers higher sample rates than sigma-delta. Main benefit of SAR architecture in the current application is very low power consumption when used in one shot mode i.e. conversion is performed with frequency significantly lower than maximum samples per second (SPS) rate. With maximum sampling rates in excess of 1 MSPS, the chosen 120 Hz sampling rate in the current application lowers the current draw to < 10 μV range.

The relevant ADC specifications for DC-measurements are offset error & offset error temperature drift, gain error & gain error temperature drift, differential nonlinearity (DNL) and integral nonlinearity (INL). Definitions of these specifications can be found at semiconductor manufacturer application notes [17, 18, 19].

SAR or sigma-delta ADCs with resolution > 14-bits were considered more suitable than 12-bit or lower resolution devices. In addition to diminished resolution, the linearity specifications of 12-bit were found to be inferior to 14-bit or higher resolution ADCs. 24-bit sigma-delta converter AD7124-4 [20] was considered to be the best option of the topology. Due to extensive software development requirement for using AD7124-4 and sigma-delta ADCs in general and since very low current draw can be achieved with duty cycled SAR ADCs, SAR architecture was chosen over sigma-delta. Relevant specifications of the contending 16-bit SAR devices are tabulated table A.4 in appendix A.

16-bit SAR ADC would provide high resolution (LTC2364 with the best specifications, as can be seen from table A.4) but the resolution sets requirements for voltage references that are difficult to fulfill simultaneously with low current draw. Price is also high at approximately 15 €. With V_{REF} = 2.5 V, the 16-bit resolution is 38 μV.

ADS7056 was found to be promising very small footprint 14-bit SAR ADC with price of ≃ 4.00 € for small quantities. With V_{REF} = 2.5 V, the resolution is 153 μV. A possible con is the internally

connected ground pin, which could make the separation of noisy digital signals more difficult and adding thus noise. Although, many of the 16-bit options are implemented with the same common ground method.

ADS7056 was chosen over the 16-bit options for its small footprint, low current consumption and low price. 14-bit resolution also relaxes the voltage reference requirements mentioned above.

The details of the powering and ADC reference voltage creation are discussed in the section Voltage References & Regulators below.

3.2.2 Relevant Specifications for Amplifier ICs

As a general requirement for all operational amplifiers (OA) and instrumentation amplifiers (IA), low noise in 0.1 Hz - 10 Hz frequency range, low supply current, single low supply voltage operation and small footprint are required for all devices.

The specified offset voltage of an OA/IA is refered to the input [21]. As a consequence, the output offset voltage is a function of the closed loop gain – larger the gain, larger the output voltage offset. The voltage levels of HFS in the μV range require large gains which makes OAs with low offset voltages essential.

The specified offset voltage is also a function of temperature. Since accurate DC-measurements are required in the HFS application, independence from temperature variations is an important parameter. Offset voltage drift is usually specified on datasheets in Volts per Kelvin. The best offset voltage drift performance is achieved using auto-zero or chopper OAs & IAs [22, 23].

OA/IA input bias currents are the currents drawn by the input pins and the offset refers to the offset of this current between the input pins. Both of these parameter affect the output offset voltage. The effect of bias currents can be compensated by keeping the resistance seen by the input pins equal thus creating equal voltage drop. The offset in the bias currents is more difficult to deal with since it varies from device to device. The offset voltages caused by offset input bias currents cannot be thus improved by circuit design but can be kept at minimum by using as low resistance values in the circuit as possible.

3.2.3 Selection Criteria for Passive Components

Resistors

Low temperature coefficient resistors should be used to avoid drift in circuit performance to reach the specified amplifier performance as well as possible. Vishay MCx-series resistors were found to have the best drift specification with ±10 ppm/°C on range 100 ohm - 130 kohm and tolerance of 0.1%, but availability was found to be very poor. Based on availability and price, Vishay 1 %, 100 ppm/K CRCW-series resistors in 0402 package were chosen as the general choice and where accuracy and as small as possible drift is needed, Yageo RT-series in 0603 package with 0.1 % 25 ppm/K specification was used.

Capacitors

The low corner frequency (< 50 Hz) required in the application poses problems for capacitor selection. Ceramics with C0G dielectric in small packages have capacitance values of only a few nF. This would require very large resistances, which would introduce offsets and noise. Small footprint capacitors with capacitances at μF range can be realized with polymer tantalum types [24, 25, 26] or ceramic X7R types. Tantalums are polarized and series connection of two capacitors is required when bipolar voltages are expected over the component. Also, available tolerances are 20 %, which is generally unacceptable for filter application. Capacitance value temperature dependency is significantly lower for tantalum compared to ceramic types [27]. Capacitance value of ceramic capacitors is strongly dependant from voltage over the component and over temperature. In the current application, the effects of voltage and temperature are significantly lower than the maximum ΔC of 15 % since the operating voltage is low and the operating temperature span is narrow compared to the specified -55 °C - 125 °C range [28] for X7R type. The main caveat for X7R type ceramics are that they are microphonic whereas tantalum types are not [27].

3.2.4 Pre-Amplifier

IA was chosen as the most applicable amplifier topology for the first stage due to the inherent layout symmetry of the input circuit and thus more easily realizable CMMR. Also programmable gain of some IAs was considered beneficial since the voltage levels of the proprietary HFS are currently unknown. As stated in the previous chapter, the best amplifier specifications for the application are achieved using auto-zero and/or chopper IAs. Specifications for the contending IAs are presented in table A.1 in appendix A.

LTC6915 IA was selected based on the large range of SPI programmable gain. Current draw is higher than for example INA333, but the programmable gain was considered more important property for the research application. Once the voltage output of the proprietary HFS is established, lower current draw amplifier with gain selectable with fixed resistor can be replaced with appropriate PCB layout changes. The system offset calibration discussed in the next section removes the stringent requirement for the voltage offset, but low offset is needed to achieve zero level close to the V_{REF} midpoint for adequate headroom with large gains. In addition to tolerable offset specification a low noise performance is essential parameter. For reduced power dissipation, the IA cannot be duty cycled, because long RC-filter settling times required for the application ruins the measurement at 120 Hz sampling frequency.

LTC6915s initial offset is max. $\pm 10\,\mu$V and offset drift of $\pm 0.05\,\mu$V/°C gives drift of 2 μV for 40 °C temperature range. Even this small drift can affect the measurement accuracy since with large gains, the error grows can amplify to mV range. For example, with system gain of 4096, the drift is amplified to $\simeq 8$ mV.

To minimize noise coupling to IA input traces from the SPI clock signal for IA programming, the DIN and CLK traces are isolated from other devices using 2-channel analog switch. The IA SPI connection is enabled only when IA gain is changed. Applicable low power analog switches with small footprint are ADG824 [29] and TS5A21366 [30]. ADG824 has maximum current draw of 1 μA whereas for TS5A21366 the corresponding figure of merit is 10 μA. Also, ADG824 has SPDT switch configuration, which enables operation of the switch from LTC6915 CS' line without any additional components. The part is available in 1.3 mm * 1.6 mm LFCSP-10 package. ADG824 was selected based on these characteristics. The connections are shown for logic 1 in figure 1 on page 1 of the

ADG824 datasheet [29]. Since LTC6915 is active when its CS pin is driven low, connections to DIN and SCK pins via ADG824 must be made to pins labeled B on both channels S1 & S2 with output taken from D1 & D2. The both logic inputs IN1 & IN2 are connected to CS line of LTC6915.

The IA is powered from 3 V low drop-off voltage reference to be able to operate as close as possible to the discharge cut-off voltage limit of 3 V of the RJD-series battery [15]. The 2.5 V reference of ADC cannot be used for the purpose since LTC6915 supply voltage low limit is 2.7 V. Also, the voltage reference used to generate the ADC V_{REF} should not be used to power the IA and OA since the SAR reference has current spikes that could couple to the amplifiers. For the details of selected IA voltage reference, see subsection 'Voltage References' below.

Input Filter

Input filter is needed to prevent rectification of radio frequency noise in the IA internal circuitry, which would introduce offset to the output. The input frequency must be bandlimited below 1.5 kHz because LTC6915 has internal sampling frequency of 3 kHz.

The conventional bridge circuit shown in figure 3.2 and discussed for example in [31] was used.

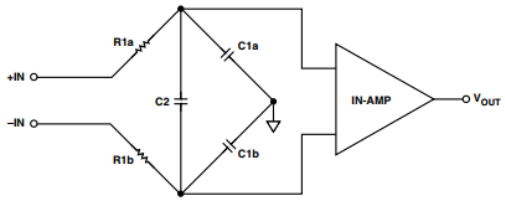


Figure 3.2: IA input filter [31].

The differential pole location is calculated from

$$f_{-3dB,diff.} = \frac{1}{2\pi R_1(2C_2 + C_1)} \tag{3.1}$$

and common mode corner frequency from

$$f_{-3dB,CM} = \frac{1}{2\pi R_1 C_1}. \tag{3.2}$$

From equations (3.1) and (3.2), it can be seen that the differential corner frequency is considerably lower than the corresponding common mode frequency. Effective common mode noise filtering is thus not realizable simultaneously and must be dealt with in later stage. High resistances add to the noise of the circuit and should be kept in a few kohm range.

Setting resistor value to 2 kohm, neglecting the value of $C1$, using corner frequency $f_{-3dB,diff.}$ = 200 Hz and solving (3.1) for C_2 gives nearest standard value C_2 = 220 nF. Setting C_1 to one tenth of C_2 gives C_1 = 22 nF. With these values the corner frequencies are $f_{-3dB,diff.}$ = 172 Hz and $f_{-3dB,CM}$ = 3.6 kHz. A small tolerance is important for C_1 to retain impedance symmetry and TDK CGA Series C0G type ceramic with 5 % tolerance in 0805 package was chosen. Panasonic ECPU Series film capacitor with 20 % tolerance in 1206 package was chosen for C_2.

3.2.5 Signal Conditioning

All OAs for signal conditioning are powered from the same 3 V supply as the IA. Mid-supply reference voltage creation is discussed below in the subsection Voltage References.

Low-pass Filter

The signal must be low-pass filtered as steeply as possible to attenuate possible 50 Hz mains interference efficiently. To this end, an active filter was included on the signal path. The used OA is required to fulfill the general component requirements of the application: low current draw and low offset voltage & drift. Although with small closed loop gains required for the filter OA, the offset voltage performance is relaxed compared to IA with high closed loop gains. As with IAs, the best specifications for the application are achieved using auto-zero and/or chopper OAs. Specifications for the contenders are presented in table A.2 in appendix A.

LTC2066 was chosen for the filter stage for its very low current draw and low offset & drift parameters. LTC2066s maximum offset drift of $\pm 0.03\,\mu$V/°C gives drift of 1.2 μV for 40 °C temperature range. With max. 10 μV initial offset, contribution of LTC2066 to system offset would not be measureable even with 16-bit ADCs LSB resolution of 38 μV, since the following driver stage has only gain of 2.

Low component count Sallen-Key topology and flat pass band Butterworth response was deemed best suited for the application. To create 3rd order response, RC-stage with adjustable gain is included for steeper roll-off and more flexibility in gain settings. Altering the gain of the Sallen-Key circuit alters also the Q and is not ideal for modifications. Summary of filter design with Sallen-Key topology is given in [32]. Using unity gain buffer for the Sallen-Key stage shown in figure 3.3

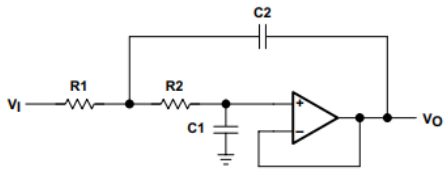


Figure 3.3: Sallen-Key low-pass filter with unity gain buffer [32].

the design equations for circuit Q and pole location reduce to

$$Q = \frac{\sqrt{mn}}{m+1} \tag{3.3}$$

and

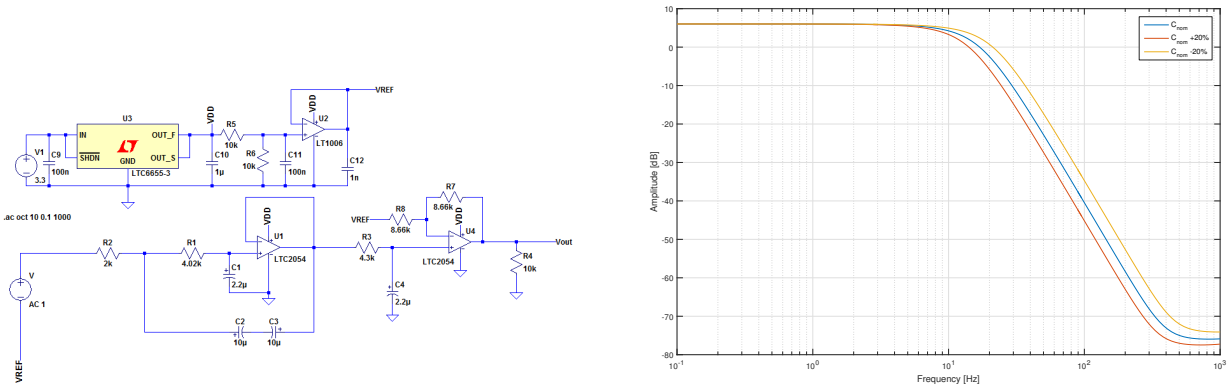
$$f_{-3\text{dB}} = \frac{1}{2\pi RC\sqrt{mn}}. \tag{3.4}$$

Ratios of resistors and capacitors are given by $R_1 = mR$, $R_2 = R$, $C_1 = C$ and $C_2 = nC$.

Based on the better temperature stability and immunity for microphonics, the polymer tantalum types were selected for the filter application and AVX F38 series for their small footprint. Capacitance values of 1.10 times nominal are used for corner frequency calculations to ensure adequate

bandwidth. Available capacitance values for F38 series 0603 size are 2.2 μF, 4.7 μF and 10 μF [26]. Since C_1 in figure 3.3 can be referenced to circuit ground instead of V_{BIAS} single capacitor can be used without polarity issues. For C_2 series connection of two capacitors is needed. Selecting $C_1 = 2.2\,\mu$F and $C_2 = 5\,\mu$F (series connection of two 10 μF capacitors) gives ratio $n = 2.273....$ Since for Butterworth response $Q = 1/\sqrt{2}$, from equation (3.3) $m = 0.485$.

Setting $f_{-3\text{dB}} = 15$ Hz and using maximum values for the capacitances, equation (3.4) gives nearest standard values of $R_2 = 4.02$ kohms and $R_1 = 0.485 \cdot R_2 = 2.0$ kohms. The following RC stage values were set using the same 2.2 μF capacitor and 15 Hz corner frequency, which gives nearest standard value of 4.3 kohms for the resistor. The OPA835 driving the ADC has feedback network with equal value 8.66 kohm resistors, a value selected twice the 4.3 kohm input resistor to compensate for offset voltage generated by OA bias currents, giving gain of 2. The resistors are included mainly to enable easy modification of gain if necessary. With nominal values for the capacitors the circuit has attenuation of 29 dB with respect to pass band at 50 Hz. The simulation circuit schematic and its amplitude response in shown in figure 3.4.



(a) Test circuit schematic

(b) Amplitude response

Figure 3.4: 3rd order Sallen-Key Circuit amplitude response with $C_{nominal}$ & ± 20 % for worst case analysis. The -3 dB corner frequencies and attenuation at 50 Hz for the nominal and the two C tolerance worst case scenarios (all capacitors $C_{nominal}$± 20 %) are: $C_{nominal}$; f_{-3dB} = 12.5 Hz, attenuation @ 50 Hz = -28.9 dB, $C_{nominal}$+ 20 %; f_{-3dB} = 10.4 Hz, attenuation @ 50 Hz = -33.5 dB, $C_{nominal}$− 20 %; f_{-3dB} = 15.6 Hz, attenuation @ 50 Hz = -23.3 dB.

To ensure that the preceding LTC6915 can drive the Sallen-Key stage effectively (load > 1 kohm required), the input impedance of the Sallen-Key circuit must be determined. In [33], the input impedance of Sallen-Key circuit was found to be equal to the reactance of C_1 below the -3 dB corner frequency f_0 approaching asymptotically the value of R_1 in 3.3 for $f >> f_0$. Based on this, it can be concluded that the input impedance of the designed circuit with $R_1 = 1.8$ kohm is large enough.

ADC Driver

According to SAR ADC datasheets and application notes [34, 35, 36], a wide band OA is required to drive the ADC due to fast current spikes generated by the sampling circuit of the ADC. Settling time of the amplifier driving the SAR ADC and its input circuitry is an important design parameter in the current application. In TI application note [36], several issues with SAR ADC input drive are discussed. The settling time specification given on OA datasheets is defined as the time required for the output to settle within an error band. In SAR ADC driver application the ADC sampling

capacitors connected to the ADC inputs during aquisition phase generate current spikes that are seen by the driving amplifier. The requirement for the driving amplifier is thus similar to load regulation capability of voltage regulators but settling time specification applicable to load variations is not available for OAs. Also, simulation models of OAs may have difficulties reaching a solution. In [36], a rule of thumb type equations for calculating the required gain bandwidth product (GBW)

$$GBW > 2\frac{1}{2\pi RC} \tag{3.5}$$

and current drive capability

$$I_{drive} = \frac{0.05 V_{REF}}{R} \tag{3.6}$$

are given to achieve the required settling time. Here R and C are the ADC input filter values. In ADS8887 datasheet [35] and other TI publications, the required GBW is twice the value of equation (3.5).

Selection table of OAs suitable for ADC driver application is presented in table A.3 in appendix A. OPA835 was considered the best compromise between performance and current draw. The offset voltage drift for the OPA835 is specified at $\pm 8.5\,\mu$V/°C max. giving maximum drift of 340 μV for 40 °C temperature range. This is 3 LSBs for 14-bit ADC with V_{REF} = 2.5 V. The low frequency noise performance (0.1 Hz - 10 Hz) of the wide bandwidth OAs designed for ADC driver application is generally not specified on the datasheets. For OPA835, the noise spectral density graph (OPA835 datasheet [37] page 16, figure 16) ends at 10 Hz but can be seen to rise towards the low frequencies. Thus, the low frequency noise performance cannot be estimated reliably for the ADC driver OA. On ADS7056 datasheet [34], design example of DC measurement circuit without a driver OA is given but only 12-bit resolution is achieved. For this reason, it was assumed that to achieve the full 14-bit resolution, a wide bandwidth driver OA should be included.

A charge kickback filter or flywheel circuit composed of RC-filter is connected between the driving amplifier and ADC input to act as a charge storage for the ADC sampling capacitors. The circuit also filters noise and attenuates the current spikes from the driving OAs perspective. Design guidelines are given in ADS7056 datasheet and TI application note discussing SAR ADC input drive circuitry [34, 36]. As a rule of thumb capacitance of 20 times the sampling capacitor value (16 pF for ADS7056) is recommended giving minimum value of C = 320 pF. The resistor is required to ensure driver OA stability but must be as low as possible to keep the RC time constant from affecting the measurement. The required time constant is dependant on the ADC resolution and acquisition time t_{acq} and time constant $\tau = t_{acq}/18$ is recommended in [36]. By selecting the value of C, R can be calculated from $R = t_{acq}/18 \cdot C$ since $\tau = RC$. For ADS7056 t_{acq} = 95 ns [34]. Selecting C = 330 pF would give thus R = 16 ohms. Based on equation (3.5), these values set 60 MHz GBP requirement for the driving amplifier which his higher than specified for OPA835. The recommendations in [36] are given without details about ADC resolution or any references to sources that validate these rules of thumb. Simulating the input circuit with C = 330 pF and full scale input voltage of 2.5 V, reveals that for the sampling capacitor voltage to settle within the LSB = 153 μV, the resistor value is required to be $R < 46.9$ ohms. Also, simulated circuit seems to work accurately or even more so with C = 16 pF (equal to sampling capacitance) than with larger capacitances and the reasoning for the 20 times the sampling capacitance rule of thumb could not be deduced.

Setting the resistor value to R = 43 ohms gives GBP requirement of 22.4 MHz, which is achievable

with OPA835 in gain of 2 configuration. The design was simulated using the circuit shown in figure 3.5. Ideal voltage sources is used as a signal source and thus the simulation does not take into account the effects of driving OA performance. The basic idea of the simulation circuit is derived from a Linear application note describing a circuit for simulating differential SAR input [38].

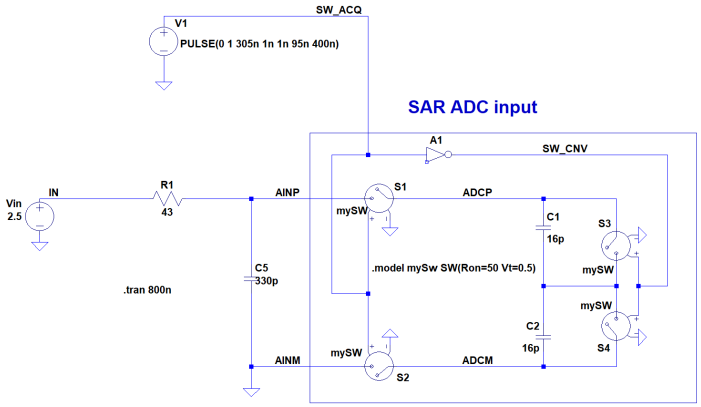


Figure 3.5: Circuit schematic of SAR input circuit simulation. Ideal voltage sources is used as a signal source and thus the simulation does not take into account the effects of driving OA performance, which cannot be reliably simulated in the current application as described above. The basic idea of the simulation circuit is derived from a Linear application note describing a circuit for simulating differential SAR input [38] and is modified here to single ended configuration. The accuracy of the voltage over sampling capacitors at the end of acquisition phase can be inspected most easily by plotting the difference between nodes IN and ADCP. For 14-bit ADC the difference should be $< 153\,\mu$V.

ADS7056 in input is protected from higher than V_{REF} voltages by including reverse biased schottky diode CDBQR0130L from input to V_{REF}. The diode voltage drop is below 0.3 V with currents < 40 mA, thus keeping the input below ADS7056 absolute maximum rating of $AV_{DD} + 0.3\,\text{V} = V_{REF} + 0.3\,\text{V}$.

3.2.6 System Offset Calibration

Accuracy of the system can be increased by including functionality for system calibration. By shorting out the HFS using microcontroller operated analog switch, system calibration can be performed during power-up initializations, when IA gain is changed or when temperature changes. Offset measurement was implemented by sampling 60 values and calculating the average to diminish the effect of noise. Threshold temperature difference for re-calibration during operation was set to 0.5 °C.

Calculation of zero level was implemented as follows: The zero level V_0 is measured with HFS shorted as

$$V_0 = \frac{V_{BIAS}}{2} \pm V_{os}, \tag{3.7}$$

where V_{os} is the offset voltage. The output v_{out} relative to the measured zero level can be then calculated using the measured reading with signal source included, $v_M = v_{HFS} + V_0$, from

$$v_{out} = v_M - V_0. \tag{3.8}$$

Thus zero heat flux $v_{HFS} = 0$ would give $v_{out} = 0$, positive heat flux $v_{HFS} > 0$ and negative heat flux $v_{out} < 0$.

Shorting of HFS was implemented with semiconductor switch. AS11P2TLR low voltage single channel switch was chosen for the application for its low threshold voltage and on-resistance [39]. The switch capacitance can be neglected since the frequency range of the application and source resistances are low.

3.2.7 Controller

The microcontroller reading the ADCs and operating as the communications gateway for the data, must have sufficient number of I/O pins, I2C and SPI communications, low current draw and small footprint. ATtiny167 has all the stated characteristics available in small 32 pin VQFN (5mm * 5mm) package [40] and was thus chosen for the application.

As low as possible digital supply voltage would be ideal for low power consumption but the LTC6915 digital interface is powered from the $AV_{DD} = 3$ V supply requiring controllers DV_{DD} to be close to the same level since LTC6915 uses TTL logic levels. ATtiny167 has an internal 128 kHz oscillator clock option which allows very low power consumption. The 128 kHz oscillator frequency vs. temperature is given on datasheet page 268 [40]. The frequency changes from approximately 111 kHz at 0 °C to 108 kHz at 50 °C with $DV_{DD} = 3$ V. The accuracy is more than adequate for the application. Exclusion of external oscillator saves also pins and real estate on the PCB.

Time budget for using the low operating frequency was estimated. According the ADS7056 datasheet [34], time needed for ADS7056 conversion is $18 \cdot t_{SCLK}$. Minimum aquisition time is given only for the ADS7056 calibration sequences as 90 ns. Conversion time for power up calibration is $24 \cdot t_{SCLK}$ and for calibration during normal operation $64 \cdot t_{SCLK}$. To estimate time budget for conversion, $f_{CPU} = 110$ kHz (worst case estimate) and maximum SPI clock of $f_{CPU}/2$ gives conversion time of 327 μs for normal operation and 436 μs & 1.16 ms for the power up and normal operation calibrations, respectively. The system calibration by taking average of 60 samples (to compensate for the effect of noise) with input shorted requires time interval of 20 ms. With the chosen 120 Hz sampling frequency, the time available for the sampling is $1/120\,\text{s} - 180.09\,\mu\text{s} = 8.15\,\text{ms}$, which is more than enough for normal operation. The system calibration takes considerable time interval but can be assumed to be realizeable with interrupt driven software implementation.

Series resistors are included on SPI lines to isolate other devices during in-system programming and to reduce possible ringing. The resistors should be placed near the ATtiny167 pins but not on the lines connecting to controller programming device as shown in figure 3.6. ADS7056 datasheet shows 33 ohm resistors on the SPI lines and that value was used for all pins of ATtiny167. According to ADS7056 datasheet page 19, the SDO pin is tri-stated when CS is high and should thus prevent problems during in-system programming. LTC6915 DOUT pin is never tri-stated in serial mode and was for this reason left unconnected. External pull-up resistors were connected to all CS lines to ensure that devices connected to SPI lines are tristated during ATtiny167 programming.

The ATtiny167 internal 10-bit ADC is used to measure the battery voltage to detect a low voltage. The battery voltage is measured from resistive voltage divider composed of two 1 Mohm resistors to limit the measured voltage within the ATtiny167 V_{CC} voltage used as the reference.

Gain selection is implemented with a momentary push button switch. Debounce circuit comprised of a resistor and capacitor is included along the switch. Functionality of the debounce cir-

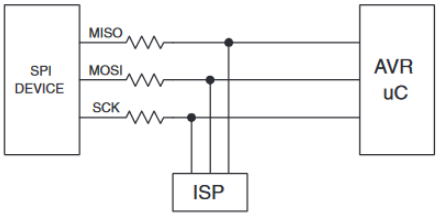


Figure 3.6: ISP isolation scheme according to [41].

cuit has been extensively tested with 5 V supply voltage during other project and simulation was used to further confirm the design. ATtiny167 pin PB6 reserved for external interrupt is assigned for the switch so that both interrupt and polling implementation is possible.

Connection of USB voltage is sensed with MOSFET operating as a inverting switch. With USB voltage present, the circuit drives a ATtiny167 pin low. This knowledge can be used then to halt operation during charging or other functions deemed necessary.

3.2.8 Logic Level Shifter

Logic level shifter at the I2C output line of the board was included to allow possibly different logic levels of the following circuits.

Maxim MAX14595 is a low power I2C bus optimized logic level translator which allows also same voltage levels on both sides ($1.65\,\text{V} \leq V_{CC} \leq 5.5\,\text{V}$, $0.9\,\text{V} \leq V_L \leq V_{CC}$). External devices connected can thus have 3 V - 5 V logic levels. Caveat of MAX14595 is that the specification are given for a maximum load capacitance of 100 pF. The maximum I2C bus capacitance is 400 pF [42]. For long buses an extender can be used but the current draw is too high for battery operation [43].

3.2.9 Voltage References & Regulators

In addition to good temperature stability, also low noise, low dropout voltage and low quiescent current are required from the voltage references. Relevant specifications are thus initial accuracy, temperature coefficient, dropout voltage, noise in 0.1 Hz - 10 Hz range and quiescent supply current.

ADS7056 resolution with 2.5 V reference (153 μV) sets the boundary conditions for noise and drift performance of the voltage reference. Using temperature range of 50 °C, 1 ppm/°C drift with 2.5 V output voltage produces a change of 125 μV at the reference output. This implies to limiting value of 1.2 ppm/°C to keep the drift inside 1 LSB of the 14-bit ADC. As can be seen from table A.5 and the listed devices in appendix A, low current draw, low price and good performance coexists rarely. REF3325 reference was chosen for its low current draw, small footprint, noise less than ADC resolution and manageable price. The drift performance is far from 1 LSB but the system calibration function removes the strict drift performance requirement. The max. drift of REF3325 is 30 ppm/°C [44] giving 3 mV drift on 40 °C temperature range.

In addition to the specification requirements listed above for the 2.5 V reference, low voltage drop is required for the voltage reference for generating the 3.0 V supply voltage for IA and OAs to ensure operation as close as possible to the battery 3 V cut-off voltage [15]. ISL21010 was chosen for its

low voltage drop and manageable current draw & temperature coefficient. The maximum offset voltage drift in 40 °C temperature range is 5 mV.

LP5907 in SOT23-5 package was chosen for 3.0 V digital supply regulator for its low supply current. Smaller DSBGA package is also available but its 0.35 mm pitch requires smaller PCB tolerances that would raise the PCB manufacturing cost.

Reference voltage V_{BIAS} for the IA and OAs was set to 1.25 V to create zero input level to midpoint of the 2.5 V ADC reference. Best suited implementation of this reference is resistive voltage divider with bypass capacitor followed by a OA buffer. This solution avoids the use of another low noise and thus generally high supply current voltage reference. Also, noise generated by the 3.0 V voltage reference is filtered out simultaneously by the RC-filter. A fairly large resistance values are needed to avoid excessive current draw. With 3.0 V supply, 1.25 V output from a voltage divider can realized with resistors values of 100 kohm and 140 kohm. Resistors with 0.1 % tolerance and 25 ppm/K drift were used for the purpose. With total resistance of 240 kohms, the current draw of the divider is 12.5 μA. The bypass capacitor value was chosen to be 100 nF, which gives time constant of 14 ms allowing the reference voltage to reach nominal value in 70 ms at power-up. The selected OA should be low input current, low noise & low power type. A suitable OA in TSOT-5 package is AD8603[45]. AD8603 can drive load capacitances as high as 2 nF and using the snubber circuit shown on datasheet page 12, the ringing can be minimized. Ringing can worsen the noise performance and should be thus dealt with. In AN148 from Linear [46], the details of the snubber circuit are discussed on pages 5 - 7 (details of component value selection on page 7). All capacitors in the 1.25 V reference are C0G type to avoid microphonics.

The reference trace is bypassed at the corresponding OA and IA pins with 470 pF ceramic capacitors and snubber circuit is added to improve the transient response of 1 nF load capacitance as described on the datasheet. C0G type ceramics are used here to minimize interference from microphonics generated by capacitors with X7R type dielectric.

For all other bypass capacitors in μF range, X7R types in 0603 package are used.

The system voltage offset drift is dominated by REF3325 and ISL21010 unless very high gains of the IA are used, as calculated in the previous section.

3.2.10 Temperature Measurement

Temperature measurement near the HFS might be required at least during prototyping stage. IC solutions were considered the most convenient solution for their small size and small number of additional components needed. ICs with SPI or I2C buses are available but these were considered unwise choice for placement near the HFS due to possible RF noise coupling to the most sensitive part of the circuit. Based on this, analog LMT70 [47] temperature sensor with very small footprint (DSBGA4) and low current draw was chosen for the purpose with second ADS7056 for converting the analog voltage output to digital format. The LMT70 output is capable of driving a capacitance of ≤ 1 nF without external resistor and its output resistance is 28 - 80 ohms. It was assumed that LMT70 can thus directly drive the 330 pF input capacitor of the ADS7056 so that accurate enough AD-conversion for the purpose is obtained.

3.2.11 Battery Management

Battery management IC is needed for recharging the Li-ion battery. LTC4065 was chosen for its small footprint, low battery current draw and simple implementation with minimal number of additional components. The charging current is set by connecting resistor to the pin labeled PROG and the resistance value is calculated from equation $R_{PROG} = 205/I_{bat}$ [48]. The charging current I_{bat} for RJD2032 is 40 mA, requiring resistor value of 5.125 kohm. To be on the safe side, a resistor with standard value 5.23 kohm was chosen.

3.2.12 Connectors

Li-ion battery charging was implemented via micro USB connector with ground and 5 V lines connected only.

The I2C bus requires four lines (two for data + V_{DD} and GND of the following circuit). Since the measurement system must tolerate heavy vibration during use, the connector must be such that the electrical connection is secure. Standard PCB power connectors are not sufficient for the application for this reason. To this end, Hirose 4-pin SMD connector [49] with small footprint was chosen.

For ATtiny167 in-circuit programming, 2*3 header with 1.27 mm pitch was chosen for its small size.

3.3 Estimated Current Draw

The maximum current draw of the circuit was estimated using maximum values where available. The currents in the internal load resistances are neglected in the estimate.

- ADS7056 @ 3.3 V, 10 kSPS: 5 μA typical
- LTC6915: 1.65 mA
- AD8603: 50 μA
- LTC2066 & OPA835: 12.5 μA + 340 μA $\simeq$ 350 μA
- REF3325: 3.5 μA
- ISL21010: 80 μA
- LP5907: $\simeq$ 30 μA
- MAX14595: 6 μA
- ATtiny87/167: 50 μA
- Power LED: 1 nA (duty cycled 8 μs/4s)
- Battery management: 1 μA

The total maximum current draw is 2.23 mA with LTC6915 dominating. At minimum, RJD 2032 rechargeable battery gives thus 80 mAh / 2.5 mA ≃ 32 hours minimum operating time (neglecting cold environments).

Chapter 4

PCB Layout Design

PCB design related error sources and interference prevention methods were investigated and their applicability to the current design was then evaluated. In this chapter offset voltage minimization and EMI prevention methods are reviewed and finally the selected PCB design solutions are presented.

4.1 Offset Voltage Minimization

4.1.1 Paracitic Thermocouples

Seebeck voltages are generated from thermocouples due to component-solder & solder-copper interfaces shown in figure 4.1. Differing temperatures at component leads generate voltage, which can be modelled as series connected voltage source with the component [6]. Examples of gradient compensating PCB layouts for standard OA circuits can be found also in [6]. Thermal gradients are generated by power dissipating components or by large temperature differences near the electronic device. In human HFS measurements, close contact to skin was considered to balance the possible temperature gradients, making the paracitic thermocouple effects less prominent. In the current design, component with the most power dissipation is the battery management IC, although there is no dissipation during measurement. This IC was placed as far as possible from first stage to avoid thermal gradients. The input filter components were positioned symmetrically to ensure that components connected to both LTC6915 inputs are subject to similar thermal gradient in direction of longer board dimension. In later stages the paracitic thermocouple effects were neglected since the signal is already amplified at those stages significantly from tens of μV levels.

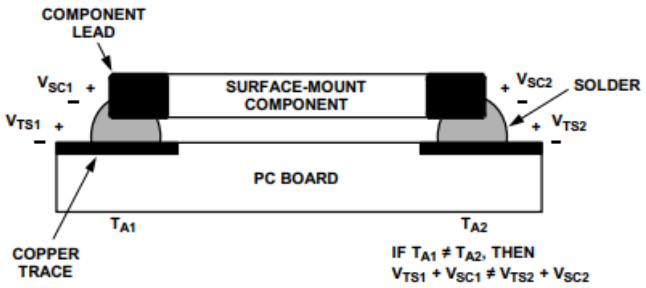


Figure 4.1: (Component lead thermocouple [50])

4.1.2 Leakage Currents

PCB Cleaning & Sealing

As stated in chapter 2, the PCB surface should remain clean and free of moisture [6]. To minimize leakage currents, the PCB should be covered with epoxy or silicon to seal the board from moisture.

Guardrings

Guardrings are used around amplifier inputs to diminish leakage currents. Guardrings are continuous loops of copper trace surrounding the critical circuit nodes.

In [6], the most comprehensive treatment on guardring design is given. In non-inverting OA arrangement (page 12), only the OA input nodes are enclosed and the guard is connected to non-inverting pin. The solution depends on low source impedance since the guardring is essentially driven by the source. It was concluded, that this method might introduce coupling path for EMI and thus reduce the circuits CMMR since the layout symmetry is reduced.

In [51] OA buffer is used to keep the guard at V_{BIAS}. All amplifier circuit components are enclosed by the guardring. Solder mask is advised to be omitted for reducing surface charges.

In AD8551 datasheet [50] the guardring is connected in inverting arrangement to V_{BIAS} and the OA input nodes are enclosed only.

In LTC2063 datasheet [52], the solder mask is omitted only over the guardring and only the input node is enclosed. Also design example is for minimizing leakeage current due to high impedance sources, which is not applicable to current HFS design. Only inverting circuit layout is demonstrated in the example.

In summary, all available information on guardrings is related to OAs. As the current design has an IA as the first stage, the methods presented were not considered directly applicable. Omitting the solder mask as presented in some sources, especially for large areas, was considered unwise in the current application as the PCB material would be more susceptible for absorpting moisture, which could lower the resistivity of the board neutralizing the benefits of guardrings. Also, adding copper to the input traces in form of the guardrings was considered unbeneficial for EMI rejection since the symmetry of the IA input would be compromised. Susceptibility to EMI was considered more severe error source than leakage currents especially with source impedances in the range of tens or hundreds of ohms. Also, the current design incorporates ICs in very small package sizes, which make routing of the guardring between the IC pins difficult or even impossible.

4.2 EMI

EMI prevention methods were researched for from application notes in addition to the classic textbook [14].

In [53] (pages 27 - 28), general methods to improve noise rejection are listed as

1. Filtering (low-pass) the signal
2. Use of integrating ADC with conversion cycle equal to mains frequency
3. Guardrings to reduce noise from common mode noise sources
4. Reduce signal trace resistance & inductance to reduce the noise coupling (short and wide traces)
5. Reduce magnetic coupling to sensor leads by using twisted pair.

RF-noise can cause offset voltages by rectification in the p-n junctions of the amplifier [31]. To prevent this, low pass filter should be placed at amplifier inputs to prevent the noise from entering the IC.

To avoid RF-interference

1. Include passive filter in the input circuit
2. Minimize trace length
3. Design the input circuit PCB layout symmetric
4. Keep the impedances of the inputs symmetric
5. Keep impedances as low as possible

Last three methods of the above list have limited efficiency with RF-noise since CMMR of OAs and IAs is reduced for high frequencies.

Common mode noise can be reduced by designing symmetric layout for the input circuit of OA or IA and maintaining symmetric impedances for the inputs since the amplifiers are differential. Symmetricity of the traces keep the coupled noise as common mode, thus preserving CMMR of the amplifier. Unsymmetric layout transforms the common mode noise to differential signal allowing it to be amplified. Short traces have small parasitic capacitance and small loop area and thus reduce also the coupled noise amplitude.

To avoid common mode interference

1. Minimize trace length
2. Design the input circuit PCB layout symmetric
3. Keep the impedances of the inputs symmetric
4. Keep impedances as low as possible
5. Use twisted pair cable for the sensor leads to reduce magnetic coupling

4.2.1 Summary of PCB EMI Design

From the listings above, it can be concluded that the "standard" methods introduced in [14] and other textbooks apply to minimization of all interference sources in the current application. The applicability of guardrings were discussed in the previous section and is thus left out of this summary. Also, usage of twisted pair does not apply since the HFS is on the PCB. In summary, the applicable methods are

1. Minimize trace length
2. Design the amplifier input circuit PCB layout symmetric
3. Keep the impedances of the inputs symmetric and as low as possible

4.3 General Design Solutions

A goal was set to fit the design on 2-layer PCB to minimize the costs with the consumer grade final product in mind. The design was fitted on two stacked PCBs to enable efficient use of space on the main board. The lower board has only the HFS pads & temperature sensor LMT70 and the upper board has all the circuitry on top layer with battery & connectors on the bottom layer. Footprint for LMT70 with 100 nF bypass capacitor was included on both boards but only one unit can be installed at once i.e. LMT70 must be placed on sensor board only and left empty on main board or vice versa.

The stacked design allows placing the battery holder and connectors on the bottom layer of the board and between the main board and sensor board. This way HFS sensor can be placed close to the skin without other components coming in the way. Also, heat sink for the HFS can be fixed between the boards. The two PCBs are electrically connected together with header pins or with pieces of copper wire. Boards are fixed together with 5 mm cylindrical standoffs (if heat sink is not used) and size M2.5 bolts. The lower board is shorter by the space required for the battery holder and accessibility for battery insertion. For flexibility, HFS bonding pads are included on both boards and on top and bottom layers.

ENIG surface finish was used for the pads to ensure good solderability and to accomodate for bonding of the HFS wires. For the HFS, 10 mm * 10 mm pads were drawn on both sides of the board connected with thermal vias and grounded via 0 ohm resistors to allow separation from ground if necessary. Pads for the HFS wires were placed on bottom and top layer near the HFS pad on nearest side of the HFS pad to IA input. The pads for HFS wires were placed close to each other to minimize magnetic EMI coupling.

For the high speed OPA835 ADC driver, the ground and power planes were omitted underneath the device and its input and output pins to avoid oscillation due to paracitic capacitance as per the instructions on the datasheet (pages 41-42) [37]. Also, to minimize loading by paracitic capacitance between output traces and ground plane all components connected to the output pin should placed as close as possible for realizing as small as possible area of the output pin trace.

Separate ground planes for digital and analog circuits were not possible to realize since the ADS7056 has the grounds internally connected. To minimize noise coupling from the digital circuits to the

sensitive analog subcircuits, the digital and analog components were placed to different parts of the board.

Chapter 5

Results

Two PCBs were assembled for the performance testing. Results for the offset voltage drift and noise measurements are presented in this chapter.

5.1 The Final Design

The subcircuits described in the previous chapter are unified in the complete schematic of the final circuit design shown in Appendix B figures B.1 and B.2. The PCBs are shown in figure 5.1 and the assembled PCB in figure 5.2. Fitting the design on two layer board with dimension as small as possible was found to be a difficult task and the final PCB layout was inescapably crowded. Routing on the top board was forced to extend also to the bottom layer and the ground plane was broken in several places around the board. The digital and analog components were succesfully placed on different parts of the board but this forced to extend the routing to the bottom layer also. Vias for connecting the top and bottom layer ground planes were distributed lavishly in effort to compensate for the lack of continuous bottom ground plane. Due to these compromises, estimating the routing of current paths on the board was rendered difficult.

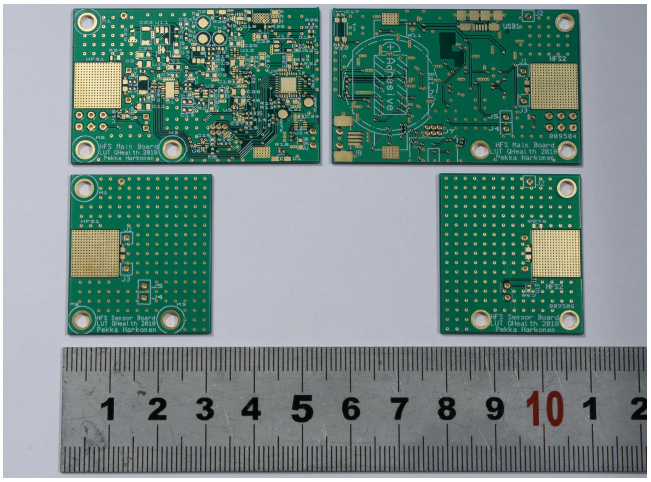
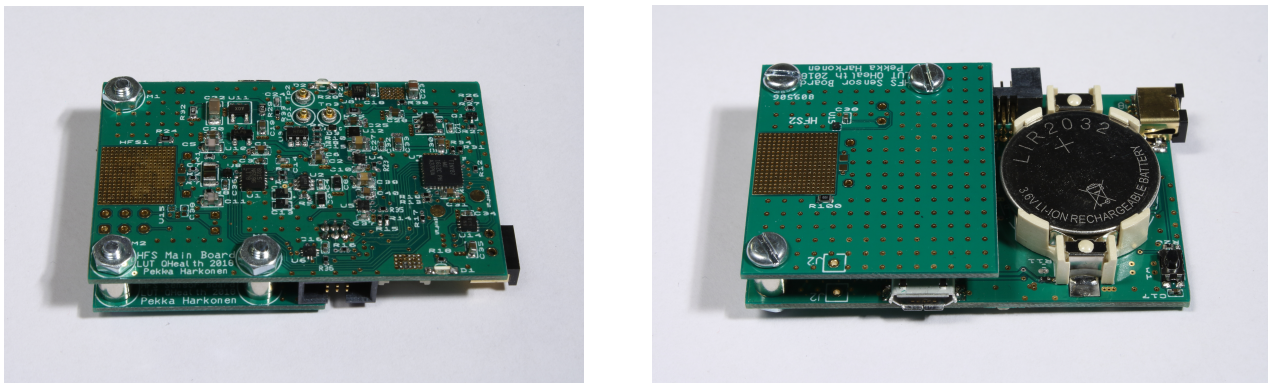


Figure 5.1: The PCBs with all layers shown for reference. On the left are the top layers and on the right the bottom layers of both PCBs.

The chosen RJD 2032 rechargeable battery was not available because of the new air mail restrictions for Li-ion batteries. Non-branded 2032 Lipo batteries were used instead with 60 mAh capac-



(a) PCB Top

(b) PCB Bottom

Figure 5.2: The assembled PCB. Dimensions for the top board are 34 mm * 53 mm and for the bottom board 34 mm * 30 mm. The HFS and the wires connecting the boards are not installed in these images.

ity specified by the vendor. During testing, the actual capacity was found to be only ≃ 30 mAh. With measured ≃1.6 mA average current draw for both boards, the batteries provided only 12-18 hours of operation.

5.2 Design Verification

For all verification measurements, the measured circuit board fixed to metal standoffs was placed in closed aluminum enclosure to eliminate external noise sources. BNC connectors were installed for connecting a input signal and for three test points connectable to the PCB via snap-in sockets [54]. Tightly fitted hole was drilled also for the cable used for the I2C data bus. The ground pins of BNC connectors for Tp2 and Tp3 (see schematic in figure B.1 for the test point locations) were connected to the enclosure via single wire and ring connector for connecting the enclosure to earth ground via oscilloscope BNC connector. The enclosure is shown in figure 5.3.

5.2.1 Measured Circuit Performance

The performance of the circuit was verified by measuring the offset voltage drift as a function of temperature. Also, a noise measurement was done to establish the resolution of the system.

Noise Performance

The measurements of the system noise performance was done following the guidelines given in [55] using the DFT method. 3 Hz sine wave from OWON AG 151 signal generator was used as an input with peak amplitude of 1.2 V. The ADC data was sent to MATLAB via I2C bus using Arduino Uno board as a converter from I2C to USART. 120 Hz sampling rate was used on the measured board. The measurement was repeated for all system gain settings 2,4,8,...,8192. RF attenuators with 50 ohm impedance built inside BNC connectors were used to attenuate the signal level for the high system gains. Attenuator with -20 dB attenuation was used for G = 512 and G = 1024 and another -10 dB attenuator was connected in series to achieve -30 dB attenuation for measurements

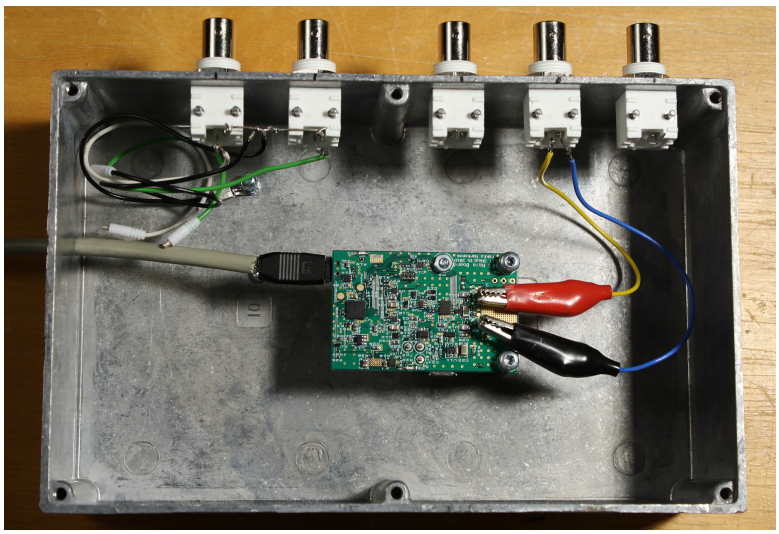


Figure 5.3: The enclosure used in all performance measurements. The PCB is installed on 15 mm standoffs for placing the board equally far from all sides of the box to ensure the PCBs warms up evenly during offset voltage drift measurements. Overlength wires were left to the through holes for connecting the HFS input from the lower PCB to the upper PCB to enable fast replacement of the tested board with crocodile clips used for connecting the signal input for the noise measurements. The grey cable carries the I2C bus to Arduino Uno board.

with G = 2048, G = 4096 and G = 8192. The signal level was confirmed at the input with 6 1/2 digit Keysight 34465A multimeter.

Sample with length of approximately 30 second was saved for each gain setting to ensure that coherent (i.e. integer multiple of test signal cycle) sample can be extracted from it. The coherent sample was selected by writing a MATLAB script that finds zero crossing points (within a tolerance of 0.01) on the positive slope of the measured signal. Because of this, samples used for the calculations had differing lengths. It was ensured manually that all samples selected by the algorithm were at least 10 seconds in length. NAD and SINAD was calculated using MATLAB functions from Signal Processing Toolbox. Power spectrum density was first computed and then used as an input for function sinad(), which outputs SINAD and NAD. ENOB was calculated substituting the NAD result to equation

$$\mathrm{ENOB} = \frac{\mathrm{FSR}}{\mathrm{NAD}\sqrt{12}} \tag{5.1}$$

[55]. The systems noise performance of both PCBs is summarized in figure 5.4, which presents the system ENOB as a function of system gain.

For system gains of 2 - 512, the system ENOB is approximately 1-bit down at 11-bits from the specified 12-bit ENOB [34] for the ADS7056 only. Above G = 512 ENOB falls to ≃ 10-bits and the result was suspected to originate from the signal source since the -20 dB attenuator was added for G = 512 and G = 1024. The results for G = 4096 and G = 8192 were not considered reliable because the signal source was found to fluctuate when measured with the multimeter. Similar fluctuation was seen on the MATLAB waveform during recording. As noted earlier, the attenuation was increased to -30 dB by adding another -10 dB attenuator for gains 2048, 4096 and 8192, which seems to play a part in the result.

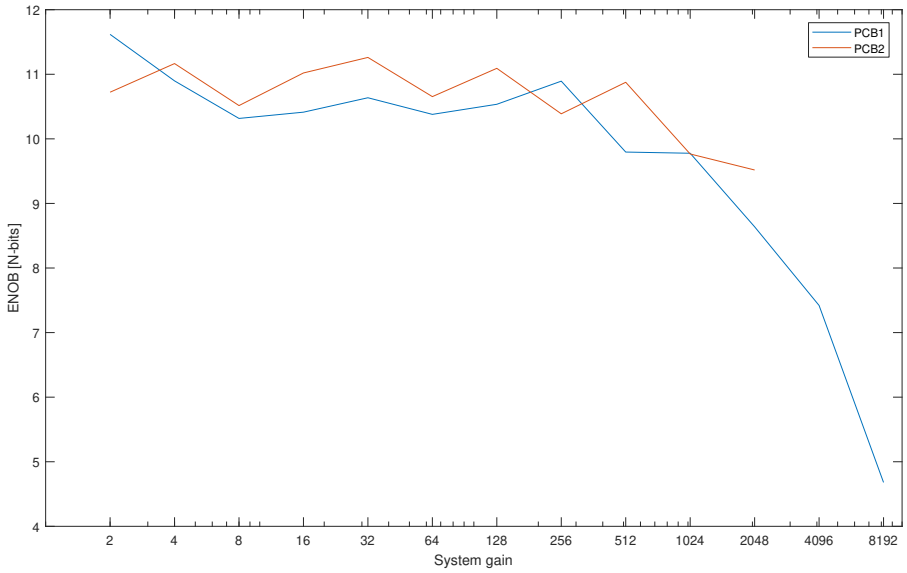


Figure 5.4: ENOB of PCB1 and PCB2. Measurements for G = 4096 and G = 8192 were not done for PCB2 since the reliability of the signal source was found to be compromized during the PCB1 measurements. The corresponding SINAD for system gains of 2 - 512 is approximately 32 dB. The SINAD plot was excluded because the shape of the curve is identical to ENOB (due to equation (5.1)).

Output Offset Voltage & Drift

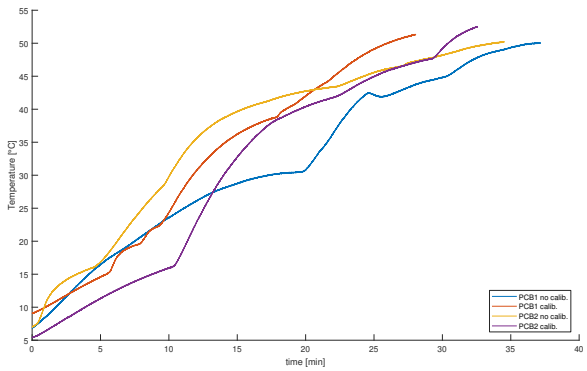
Measurements for the offset voltage drift as a function of temperature was planned to be realized using Vötsch VC 4018 temperature and climate test chamber. Due to technical malfunction, the test chamber could not be used and alternative method to create a temparature ramp from 5 °C to 50 °C degrees was devised. The measured circuit board was placed in a refridgerator for an hour to cool the PCB to approximately 5 °C. The PCB was then placed to the enclosure shown in figure 5.3 with the lid closed, and placed first in room temperature to warm up. After reaching 15 °C, the box was heated with a hot air gun to reach 50 °C degrees. Warming the enclosure instead of blowing hot air over the PCB, was used to ensure that the PCB warms up evenly.

The IA input was shorted using the analog switch AS11P2TLR on the PCB for system calibration. The sampling rate on the measured circuit board was set to 4 Hz to limit the amount of data stored. The measurement was done with system gain of 2 to measure the drift due to voltage references and repeated with G = 1024 to reveal the effect of the IA offset voltage drift more clearly. HF data and on-board temperature reading obtained from LMT70 was sent to MATLAB via I2C bus using Arduino Uno board as a converter from I2C to USART. The measured data was low-pass filtered in MATLAB to reveal the trend more clearly from the noisy signal.

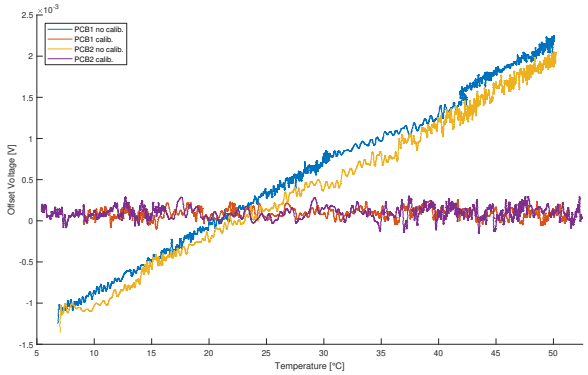
With system gain of 2, the measured offset voltage drift, with and without the calibration function, is shown as a function of temperature in figure 5.5b for both PCBs. The temperature profile is shown also in figure 5.5a for reference since the achieved temperature ramp was far from ideal straight line.

When repeating the drift measurements with system gain of 1024, it was noticed from the result that PCB1 had a malfunction increasing the noise to significantly higher level compared to PCB2. The offset voltage as a function of time during a similar temperature ramp as shown in figure 5.5a is presented in figure 5.6 with calibration disabled in 5.6a and enabled in figure 5.6b.

Due to the malfunction described above, the results for PCB1 with G = 1024 were left out from the



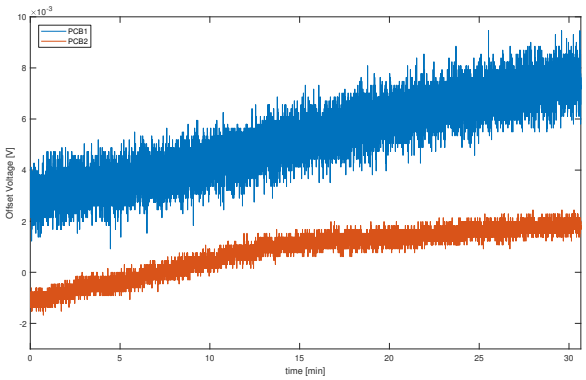
(a) Temperature profiles for offset voltage drift measurements with G = 2.



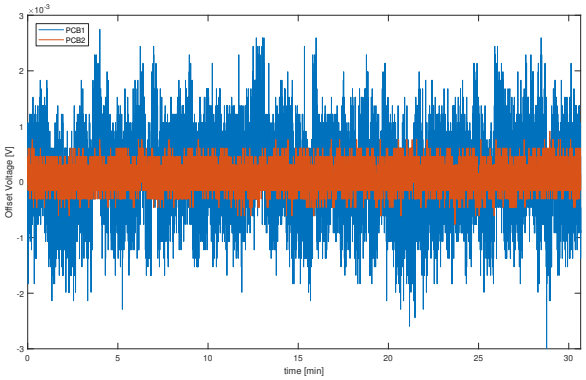
(b) Offset voltage drift as a function of temperature with G = 2.

Figure 5.5: The voltage offset result shown in figure (b) were low-pass filtered with pass band frequency at 0.05 Hz (corresponding to 20 second period) to reveal the trend more clearly from noise. In figure (b), the system calibration can be seen to work well as the positive slope of the non-calibrated results is straightened to flat line when the calibration is enabled. The standard deviation was calculated to quantify the difference in performance. For PCB1, the standard deviation calculated from the filtered data without calibration is 935 μV and with calibration 63 μV. For PCB2, the standard deviation is 904 μV and with calibration 76 μV. Based on these results, the offset error stays within 1 LSB of 153 μV.

final offset voltage drift measurement results shown in figure 5.7.



(a) PCB1 & PCB2 offset voltage drift with calibration disabled.



(b) PCB1 & PCB2 offset voltage drift with calibration enabled.

Figure 5.6: Comparison of noise levels for PCB1 & PCB2 with G = 1024. For unknown reason, the zero level is offset in figure (a) for PCB1 even though the calibration is performed once when the board is powered regardless of the temperature calibration function enable/disable.

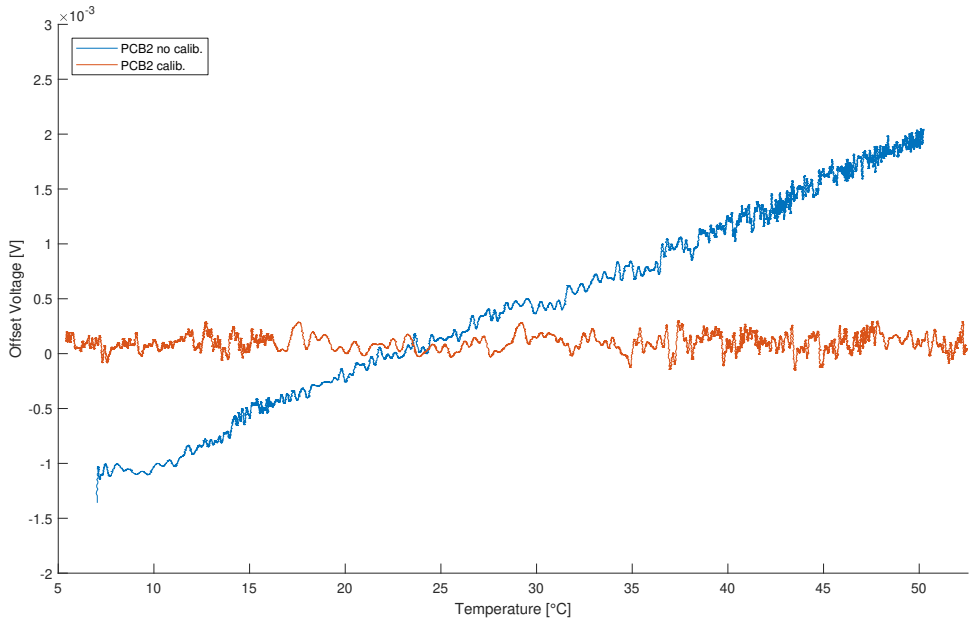


Figure 5.7: Offset voltage drift as a function of temperature with G = 1024 for PCB2. The voltage offset result shown was low-pass filtered with the same paramaters as the results for G = 2 in figure 5.5. The standard deviation calculated from the filtered data without calibration is 904 μV and with calibration 76 μV. Comparing the results in figure 5.5b and the results presented here, the calibration can be seen to work equally well with G = 2 and G = 1024.

Chapter 6

Discussion & Conclusions

6.1 Assessment of the Design Solutions & Circuit Performance

The system calibration function was proved to work as designed and the drift could be eliminated to less than 1 LSB on the 5 °C to 50 °C temperature range. Without calibration, the drift was found to be in order of millivolts which could interfere the results when measuring low levels of heat flux. The main source for the drift seems to be the voltage references, since the results in figures 5.5b and 5.7 are very similar, despite the widely differing system gains.

The noise performance was found to be far from the expected as the 14-bit resolution was not reached. Although the main reason might be the non-continuous ground plane due to crowded PCB layout, the ENOB figure of $\simeq$ 12 bits for the ADS7056 was not noticed in the design stage. The datasheet was found to be misleading, since ENOB is not clearly tabulated on the datasheet along the other specifications but shown only as a graph legend along FFT graph specifying SNR and THD without input signal ([34] page 8, figure 3). In this context the measured $\simeq$ 11-bit is a tolerable result since the implementation (component selection & PCB design) sacrifices only 1-bit from achievable accuracy. If the ENOB figure of ADS7056 had been noticed during component selection, ADC choice would have been one of the 16-bit alternatives instead. It should be also noted, that during calculating the ENOB, it was found that the result was very sensitive to the success of the coherent sampling. Even when using tolerance of < 0.01 for the deviation from mean value of the measured sine wave, the result could change as much as $\pm$1-bit when different, but still within the tolerance, zero crossing points were used for the sample.

To improve the noise performance by redesigning the PCB, only two options are possible: enlarge the PCB or extend the design to 4-layer PCB. Larger board size is not an option since the current design is already too large for a commercial product. Cost increase could also prohibit implementing the 4-layer PCB option. Based on this, it seems that for a commercial product the only option would be to implement the the complete instrumentation on single integrated circuit. The AD7124-4 comes close to this solution but requires still additional circuitry.

The make do measurement setup for drift measurements was laborious and seemed unreliable but the final results were found to be suprisingly usable. The offset voltage changes simultaneously with temperature which implies that the temperature was fairly even on the top and bottom boards i.e. the temperature of LMT70 on the bottom layer of the lower PCB seems to be very close to the temperature on the top layer of the upper PCB with other components of the circuit.

Realizing the measurement setup for the noise performance was found to be problematic, as was expected, since the signal source voltage levels required for the measurement with high gains are beyond many standard laboratory equipment. Results for gains < 512 seem to be nevertheless reliable. The dismall ENOB results for PCB1 at gains > 512 (and also at lower gains compared to PCB2) are partly explained by the malfunction found during drift measurements.

At the < 10 Hz input frequency range, charging currents of the sample capacitors or current spikes in the V_{REF} pin were not measureable. Using driver amplifier with wide frequency response seems to be thus unneccessary in the application. Omitting OPA835 from the circuit using the current PCB is possible but direct connection from the preciding RC-filter with R = 4.3 kohm and C = 2.2 μF to ADC input might introduce errors due to high source resistance. Bypassing the RC filter is obviously also an option but would reduce the attenuation of the stop band.

The current consumption of the circuit was found to be in the expected range at $\simeq$ 1.6 mA. Since the programmable IA dominates the power consumption, replacing it in the consumer grade product for example with very low power INA333 (50 μA typical), extremely low current draw could be achieved. Also, as described above, the ADC driver OPA835 could possibly be excluded which would lower the currrent draw even further.

6.2 Conclusions

Many of the requirements set for the devise were realized in the final circuit design, but due to compromises made in PCB design and in selection of the ADC and the voltage references for reducing size, cost and power consumption, the noise performance was found to be worse than desired. Also, with a consumer grade product in mind, the physical size of the circuit layout was proven to be too large even when using the smallest possible package sizes with acceptable performance. Although, in mass produced circuit the connector and traces for the microcontroller programming interface could be omitted saving some space on the board. Replacing the SAR ADC and analog low-pass filter with sigma-delta ADC with high level of integrated functions, would be probably more space efficient solution.

Despite the discussed shortcomings, information about many important details in the circuit design was revealed during course of the project. These observations are valuable in development of the next revision of the instrumentation for the application.

Appendix A

Appendix

A.1 Component Specifications

This appendix contains the relevant IA, OA, ADC and voltage reference & regulator specifications for the current application.

A.1.1 Instrumentation Amplifiers

Summary of relevant IA specifications in table A.1

	ISL2853xx	LMP8358	MAX4208	INA326	INA333
Spec. @ V_{DD}	2.5	3.3	5	2.7 - 5.5	1.8 - 5.5
V_{os} [μV]	0.6/9.0 + 2/45 [b]	**1/10**	3/45	20/100	$\pm 10 \pm 25$/G / $\pm 25 \pm 75$/G [e]
V_{os} drift [nV/C]	150/500 [c]	**-/50**	100/450	100/400	$- / \pm 100 \pm 500$/G [e]
V_{noise} [μVpp] [a]	1.5	0.9	2.5	4	1
Gain drift [ppm/C]	10/-	3/16	50/180	6/25	15/50
I_{bias} [pA]	50/400	6/1200	1/-	200/2000	70/200
I_{os} [pA]	50/350	**0.1/112**	1/-	200/2000	50/200
I_{DD} [mA]	2.9/3.4	1.8/2.1	0.75/2.3	2.4/3.4	**0.05/0.075**
V_{DD} range	2.5 - 5.5	2.7 - 5.5	2.85 - 5.5	2.7 - 5.5	1.8 - 5.5
Footprint	TSSOP-14	TSSOP-14	muMAX-8	MSOP-8/10	VSSOP-8/WSON-8
Gain set.	Prog.	Prog.	2*R	2*R	1*R [d]
Price	≃ 4.30 €	≃ 5.50 €	≃ 1.80 €	≃ 4.00 €	≃ 3.70 €

	AD8237	AD8420	AD8557	LTC6915
Spec. @ V_{DD}	5	5	2.7	3
V_{os} [μV]	30/75	-/125	2/12	-3/±10
V_{os} drift [nV/C]	-/300	1000	-/65	-/±50
V_{noise} [μVpp] [a]	1.5	1.5	**0.5**	2.5
Gain drift [ppm/C]	-/0.5	-/10	15/40	-
I_{bias} [pA]	250/1000	20000/30000	18000/25000	5000/10000
I_{os} [pA]	250/1000	-/1000	1000/4000	1500/3000
I_{DD} [mA]	0.115/0.150	0.07/0.11	1.8/-	0.88/1.65
V_{DD} range	1.8 - 5.5	2.7 - 36	2.7 - 5.5	2.7 - 10
Footprint	MSOP-8	MSOP-8	SOIC-8/LFCSP-16	DFN-12
Gain set.	2*R	2*R	Prog.	Prog.
Price	≃ 2.00 €	≃ 2.20 €	≃ 5.00 €	≃ 4.50 €

[a] @ 0.1 Hz - 10 Hz
[b] given separately for input & output stage
[c] output stage only
[d] with internal 100 kohm resistance
[e] G = set gain

Table A.1: IA specifications (typ./max.) [56, 57, 58, 59, 60, 61, 62, 63, 64]

A.1.2 Operational Amplifiers

Auto-zero & Chopper OAs

Summary of relevant auto-zero/chopper OA specifications in table A.2.

	ADA4051-1	AD8551	LTC2063	LTC2054I/C	LTC2066
Spec. @ V_{DD}	1.8	2.7	1.8	3 - 5	1.8
V_{os} [μV]	2/27	1/10	**1/5**	**1/5**	**1/5**
V_{os} drift [nV/C]	20/100	5/40	**-/30**	**20/30**	30/50
V_{noise} [μVpp] [a]	1.96	**1.6**	4.8	**1.6**	1.9
I_{bias} [pA]	5/200	1000/1500	0.5/±30	**1/3**	2/30
I_{os} [pA]	10/150	150/200	**1/30**	2/150	4/30
I_{DD} [μA]	15/18	750/1000	**1.3/2.5**	140/175	7.4/10
V_{DD} range	1.8 - 5.5	1.8 - 5.5	1.7 - 5.25	2.7 - 6	1.7 - 5.25
Footprint	SOT-23/SC-70	8-MSOP/SOIC	TSOT-23	TSOT-23	SOT-23/SC-70
Price	≃ 2.00 €	≃ 2.40 €	≃ 2.80 €	≃ 2.40 €	≃ 2.40 €

[a] @ 0.1 Hz - 10 Hz

Table A.2: Auto-zero/chopper OA specifications (typ./max.) [50, 52, 65, 66, 67]

ADC Driver Opamp

Summary of relevant OA specifications for ADC driver are tabulated in table A.3.

	LTC6261	OP162	ADA4805-1	ADA4692-2 [b]	AD8601A	OPA835	OPA837
Spec. @ V_{DD} [V]	1.8 [a]	3	3	2.7	3	2.7	3
GBP [MHz]	28	15	**30**	3.6 [c]	8.2	24	**30**
V_{os} [μV]	100/1000	50/1000	**7/125**	500/3500	80/1100	100/880	30/200
V_{os} drift [nV/C]	400/-	1000/-	**200/1500**	1000/4000	2000/-	1400/8500	400/2000
I_{bias} [nA]	±10/ ± 150	360/650	440/690	0.0005/0.36	**0.0002/0.1**	200/410	320/659
I_{os} [nA]	-/150	**2.5/25**	500/-	0.001/0.25	**0.0001/0.05**	13/100	6/52
I_{load} [mA]	±20	±30	±**40**	±15	±30	±35	±**40**
I_{DD} [μA]	240/300	600/1000	470/495	**165/240**	680/1300	245/345	570/817
V_{DD} range	1.8 - 5.25	2.7 - 12	2.7 - 10	2.7 - 5	2.7 - 5.5	2.5 - 5.5	2.7 - 5.4
Footprint	DFN-6	SOIC-8	SOT23-6/SC70-5	LFCSP-8	SOT23-5	SOT23-6	SOT23-6/SC70-5
Price	≃ 3 €	≃ 3 €	≃ 2 €	≃ 1.30 €	≃ 1.30 €	≃ 1.5 €	≃ 1.8 €

[a] $V_{CM} = V_{out} = 0.4$ V
[b] Only dual package available
[c] Given for $R_{load} = 1$ Mohm

Table A.3: OA specifications for ADC Driver (typ./max.) [37, 68, 69, 70, 71, 72, 73]

A.1.3 SAR ADC

Summary of relevant 1-channel 16-bit SAR ADC specifications in table A.4.

A.1.4 Voltage References & Regulators

References

Specifications for 2.5 V references are summarized in table A.5

	AD7680B	ADS8317IB	LTC2383-16	LTC1864LA
Spec. @ AV_{DD}/V_{REF}	2.5/2.5	2.7/1.25	2.5/2.5	2.7/2.5
Channels	1	1	1	1
Input type	Uni.	Pseud.	Diff.	Uni.
Bit res.	16	16	16	16
NMC[a][bits]	15	16	16	15
Offset Error [mV]	-/ ± 1.098	±0.5/ ± 1	/ ± 0.01 ± 0.229	±2/ ± 5
Offset drift [μV/°C]	-	±0.4/-	**±0.114/-**	-
Gain Error [%/FSR]	-/ ± 0.038	±0.024/ ± 0.048	±0.005/ ± **0.021**	-/ ± 0.8
Gain Drift [ppm/°C]	-	±0.15/-	±**0.1**/-	-
DNL [LSB]	-	±1/ − 1 + 2	±0.4/ ± 1	-
INL [LSB]	-/ ± 3	±1.5/ ± 2	±0.8/ ± 2	-/ ± 6
I_{DD} [c][μA]	1900/300	85 awg	6500/40	1000/10
AV_{DD} range [V]	2.5 - 5.5	2.7 - 5.5	2.375 - 2.625	2.7 - 3.6
V_{REF} range [V]	2.5 - 5.5	1 - AV_{DD}/2	2.4 - 2.6	1 - 3.6
Footprint	SOT23/MSOP8	MSOP8/SON8	DFN16/MSOP16	MSOP8/SO8
Price	≃ 10 €	≃ 11 €	≃ 17.43 USD [b]	≃ 13 €

	LTC2364-16CDE	AD7988-1	AD7683B	AD4000
Spec. @ AV_{DD}/V_{REF}	2.5/2.5	2.5/5	2.7/2.5	1.8/5
Channels	1	1	1	1
Input type	Pseud.	Pseud.	Pseud.	Pseud.
Bit res.	16	16	16	16
NMC[a][bits]	16	16	16	16
Offset Error [mV]	**0**/ ± **0.153**	±0.08/ ± 0.5	±0.7/ ± 3.5	-/ ± 0.34
Offset drift [μV/°C]	0.153/-	0.54/- [e]	0.3/- [e]	0.55/- [e]
Gain Error [%/FSR]	**0.003**/0.031	**0.003**/-	**0.003**/0.023	0.005/0.03
Gain Drift [ppm/°C]	±**0.1**/-	±0.35/-	±0.3/-	-/0.92
DNL [LSB]	±**0.1**/ ± **0.5**	±0.4/ ± 0.9	-	±0.15/ ± 0.5
INL [LSB]	±**0.1**/ ± **0.75**	±0.65/ ± 1.25 [d]	±1/ ± 3	±0.2/ ± 0.8
I_{DD} [c][μA]	1700/90	55 [f]/-	**560/0.05**	70 μW [g]
AV_{DD} range [V]	2.375 - 2.625	2.375 - 2.625	2.7 - 5.5	1.71 - 1.89
V_{REF} range [V]	2.5 - 5.1	2.4 - 5.1	0.5 - 5.8	2.4 - 5.1
Footprint	DFN16/MSOP16	LFCSP10	LFCSP8/MSOP8	LFCSP10
Price	≃ 12.10 USD [h]	≃ 10 €	≃ 10 €	≃ 22.50 €

[a] No Missing Codes
[b] directly from Linear (Digikey LTC2383-16CMS 21.26 €)
[c] (Conv./PwrDwn) max.
[d] max. value specified only for V_{REF} = 5 V
[e] typical value given in ppm/C, which was interpreted meaning μV/°C
[f] average @ 10 kSPS
[g] @ 10 kSPS, current draw not specified & dissipations of individual supplies not given for 10 kSPS operation
[h] directly from Linear (Digikey LTC2364-16IDE 17 €)

Table A.4: 16-bit SAR ADC specifications (typ./max.)

Regulators

LP5907 very small footprint voltage regulator [81]

- Output Voltage Accuracy: ±2 %
- Output drift 0 - 50 °C (from datasheet graph page 8): ±0.1 %
- Noise @ 0.1 Hz - 10 Hz (estimated from page 9 graph): 3.5 μV
- Load current: 250 mA max
- No load supply current: 25 μA
- Available voltages: 1.2, 1.5, 1.8, 1.9, 2.2, 2.5, 2.7, 2.75, 2.8, 2.85, 2.9, 3, 3.1, 3.2, 3.3, 3.7, 4, 4.5
- Footprint: 4-pin DSBGA (0.675mm * 0.675mm) and SOT23-5

	ISL21010	LTC6652A	LT6656ACDC	ADR361B	MAX6133	ADR291E	REF3325	REF2125
Init. accuracy [%]	±0.2	±**0.05**	±**0.05**	±0.12	±0.06	±0.08	±0.12	±**0.05**
Temp. coef. [ppm/°C]	15/50	2/5	5/10	-/9	**1/5**	3/8	9/30	2.5/6
Drop out V [mV]	60/150 [a]	300 [b]	370 [c]	300 [d]	20/200 - 200/400 [e]	300 [d]	-/70 - 110/160 [f]	-/500 [a]
V_{noise} @ 0.1 - 10 Hz [μVp−p]	67/-	5.25/-	75/-	8.25/-	16/-	8/	70/-	**5/-**
I_q [μA]	46/80	350/560	**0.85/1**	150/190	40/60	9/12	3.9/6.5	72/95
I_L [mA]	±**25**	±5	+5	+5/-1	+15	+5	±5	±10
Footprint	SOT23-3	MSOP8	DFN6	TSOT5	uMAX8	SOIC8	UQFN8	SOT23-5
Price	**1.35** €	≃ 5.7 €	≃ 5.5 €	≃ 2.7 €	≃ 3.8 €	≃ 10 €	≃ 1.67 €	≃ 3.2 €

[a] @ I_L = 10 mA
[b] @ I_{source} = 5 mA
[c] @ I_L = 5 mA
[d] only minimum value given
[e] @ I_L = 1 mA - @ I_L = 10 mA
[f] @ I_L = ±2 mA - @ I_L = 5 mA

Table A.5: 2.5 V voltage reference specifications (typ./max.) [44, 74, 75, 76, 77, 78, 79, 80]

Appendix B

Appendix

B.1 Complete Circuit Schematic

The complete circuit schematic is shown in figures B.1 & B.2

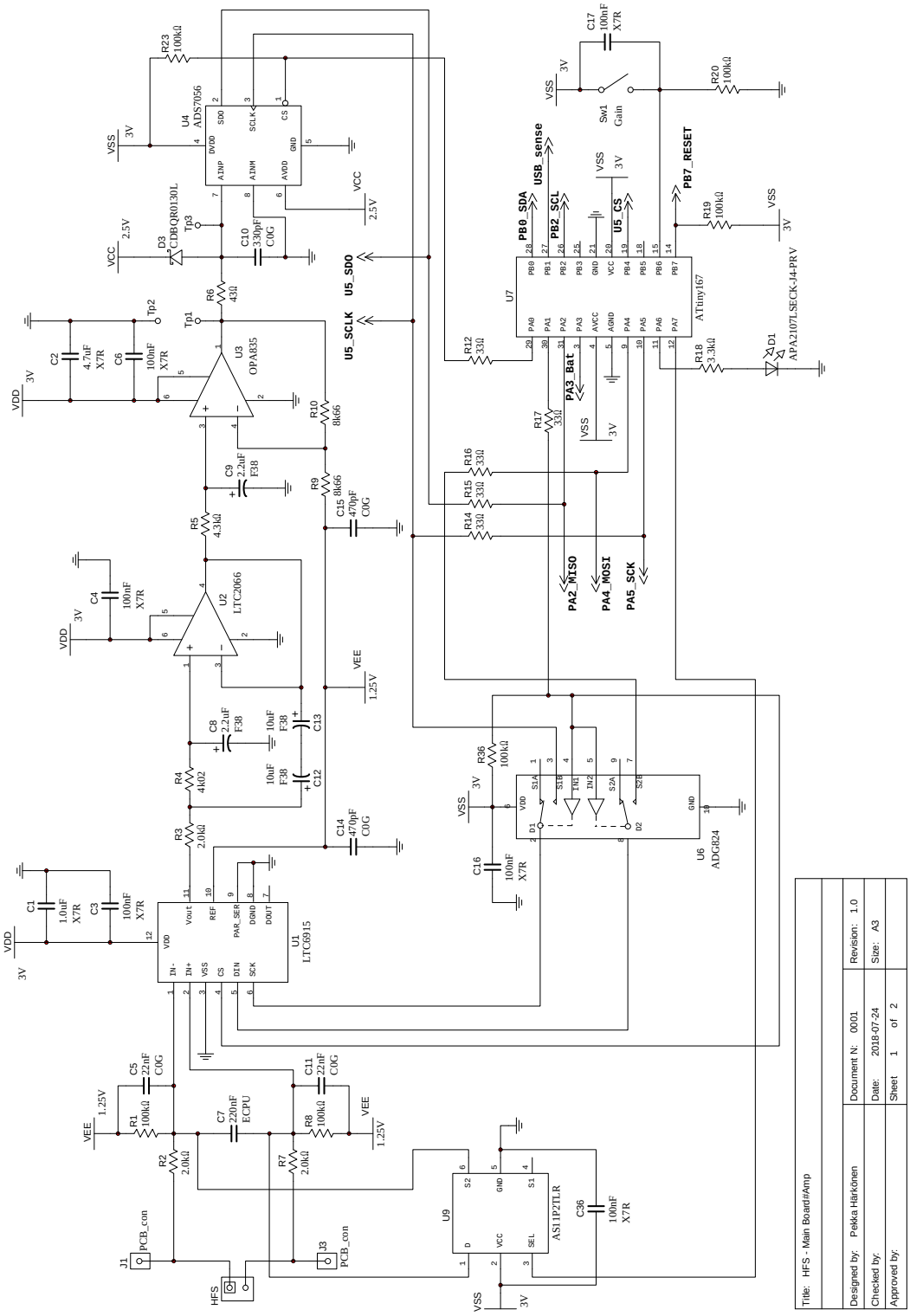
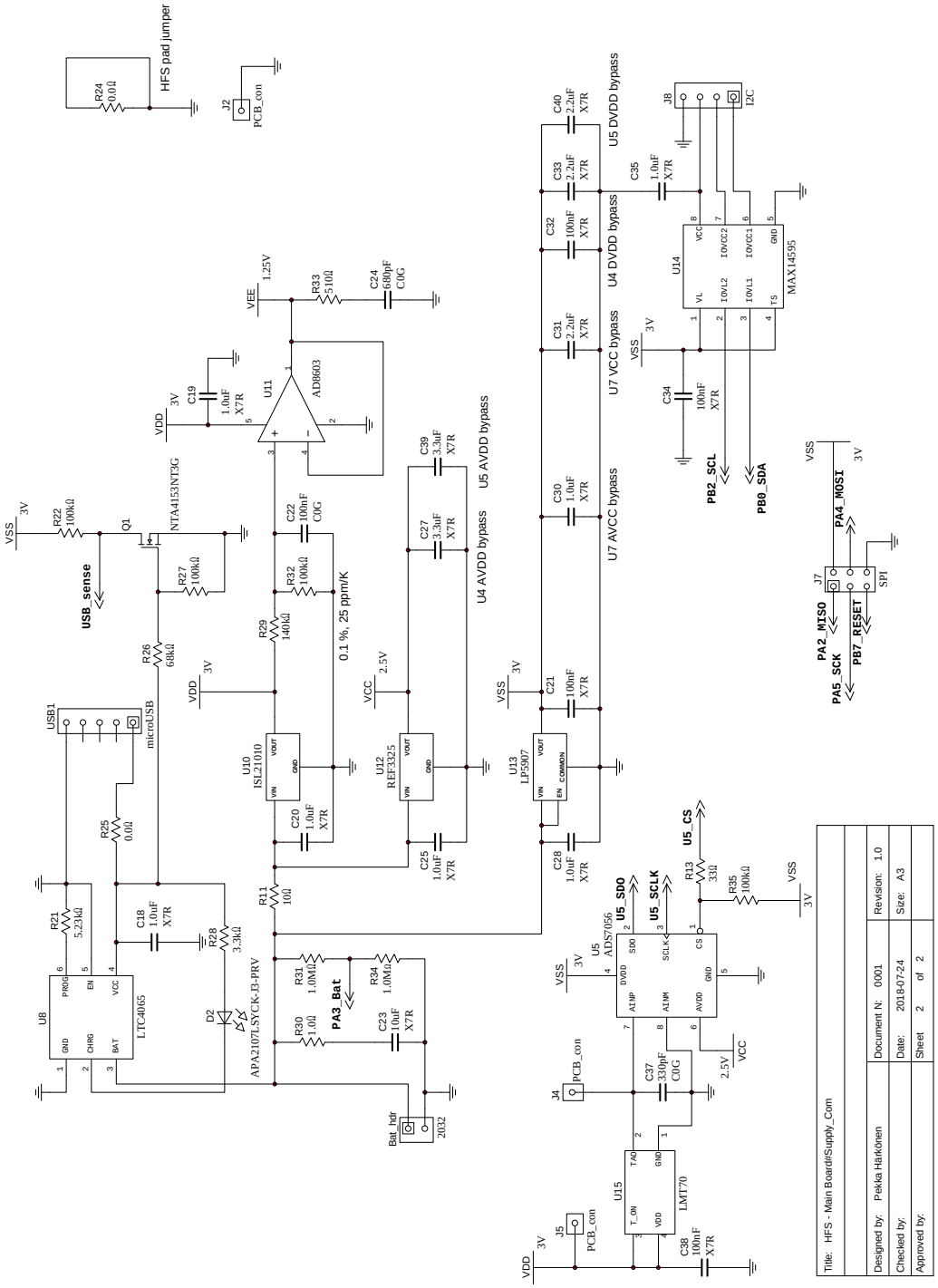


Figure B.1: Page 1 of circuit schematic.



Title: HFS - Main Board#Supply_Com			
Designed by: Pekka Härkönen	Document N: 0001	Revision: 1.0	
Checked by:	Date: 2018-07-24	Size: A3	
Approved by:	Sheet 2 of 2		

Figure B.2: Page 2 of circuit schematic.

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