Nonlinear PI-control approach for improving the DC link voltage control performance of a power factor corrected system

Honkanen Jari, Hannonen Janne, Korhonen Juhamatti, Nevaranta Niko, Silventoinen Pertti

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Jari Honkanen, *Student Member, IEEE*, Janne Hannonen, Juhamatti Korhonen, *Member, IEEE*, Niko Nevaranta, *Member, IEEE*, Pertti Silventoinen, *Member, IEEE*

***Abstract*—When fast voltage control is used in a power factor control, the ripple of the DC link causes current harmonics. This paper proposes a method to reduce the harmonic content of a fast voltage loop in a power factor correction (PFC) which can both produce low distortion during steady state operation and fast recovery from a load transient. The performance is achieved by using a Takagi-Sugeno (T-S) type nonlinear controller for DC link voltage control. The proposed nonlinear control is compared with linear PI control, which is tuned to meet the standardized regulations for harmonic content in a 3 kW single phase power supply. The results show that the presented nonlinear voltage controller can maintain the dynamic performance of the linear control with reduced current harmonics. It is also shown that the used nonlinear control method requires only marginally more complex control algorithm compared to commonly used linear PI control.**

***Index Terms*—AC-DC power converters, Digital control, Fuzzy control, Voltage control**

NOMENCLATURE

A_i	state transition matrix in T-S model
C	DC link capacitance
$e\,(t)$	error between DC link voltage and reference
i_1, i_2	Inductor 1 and 2 current measurement.
$i\,(t)$	DC link input current
K_i	ith state-feedback gain vector
K_I	integral gain in PDC
K_{I_1}	integral gain in slow PI control
K_{I_2}	integral gain in fast PI control
K_P	proportional gain in PDC
K_{P_1}	proportional gain in slow PI control
K_{P_2}	proportional gain in fast PI control
$L_{1,2}$	primary inductances of the boost converter
LMI	linear matrix inequality
m_1	error level for low gain PI control
m_2	error level for high gain PI control
M_i	membership function i of nonlinear controller
P	common positive definite matrix
PDC	parallel distributed compensator
PFC	power factor correction
PI	proportional integrating (control)
r	number of weighting functions
R	load resistance
T-S	Takagi-Sugeno (model)
u_{DC}	DC link voltage measurement
u_{AC}	rectified AC input voltage measurement
u_{ref}	DC link voltage reference
$V\,(x\,(t))$	Lyapunov function
$x\,(t)$	state vector of a state-space model
$z\,(t)$	weighting variable in weighting function
$\omega\,(t)$	integrator state in PI controller

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J. Honkanen, J. Korhonen, N. Nevaranta and P. Silventoinen are with the School of Energy systems, Lappeenranta University of Technology, 53850 Lappeenranta, Finland, (e-mail: jari.honkanen@lut.fi; juhamatti.korhonen@lut.fi; niko.nevaranta@lut.fi; pertti.silventoinen@lut.fi).

J. Hannonen is with the Powernet Oy, 01720 Vantaa, Finland

I. INTRODUCTION

Power factor is essentially a measure related to the quality of currents in AC power lines. Having a low power factor indicates inefficient utilization of electrical power as a result of the increased current stress with the given power level. In particular, the power factor is reduced when the load is either reactive or nonlinear, as is common when diode rectifiers are used. In general, the inherent drawback related to the nonlinear loads is the increased peak load current, but also the increased harmonic distortion of currents in the mains. The harmonic currents can degrade the mains voltage quality, and therefore, interfere with other equipment connected to the same main power supply. In order to limit the interference in the mains voltage, there are standards such as IEC-61000-3-2 [1] where limits for the maximum allowed harmonic content of grid currents are defined. As a result, the effects of the low power factor have to be corrected in most applications.

In single-phase systems, power factor correction (PFC) is most commonly achieved with a boost converter. In some cases, also Cúk, flyback, and single-ended primary-inductor (SEPIC) converters are used to provide the PFC function [2] [3], [4]. With wide bandgap devices, totem-pole converter can also be effectively used for PFC [5]. When the power is significantly higher, for instance in industrial three-phase systems, a bridge configuration is common, and in these applications, the PFC is commonly referred to as an active front end or active rectifier. Bridge configurations are also used when the direction of the power has to be reversed, for example in motor inverter applications.

The PFC converter is operated in either a discontinuous (DCM) or continuous current mode (CCM). The current mode operation of the converter describes whether the switching current decreases to zero during the switch cycle. The DCM operation is typically applied in low-power and low-cost systems as it can be used without current measurement, thereby resulting in a significantly simpler control circuitry. However, the DCM operation has a limited power range because of the high peak currents, and therefore, the maximum power range within which power supplies are typically designed to operate in the DCM is about 150–300 W. Systems designed to operate in CCM may operate in DCM at low power and this increases the THD of the current. In order to circumvent the increase of current distortion, the authors in [6] propose a modulated carrier control to improve the current shape when systems goes into DCM allowing for improved power factor in low power operation.

The standard method for controlling the current and DC link voltage is to use PI controllers for both the voltage and current control loops. When the PFC is working as intended, the current waveform follows the grid voltage feeding full-wave-rectified sine current to the DC link. This is common to all single phase PFC converters regardless of the actual topology. The PFC can be used for reducing the effects harmonic currents of nonlinear loads from the mains as was done in [7].

The input current control has been actively studied and several methods have been proposed in the literature. In [8] the authors used an input voltage feed forward with a tuned phase lead circuit to improve the current waveform of the PI-controlled current loop. Nonlinear optimal control of PFC current has been studied for example in [9], where the authors designed an optimal control based on Sontag's method. In [10] the authors compared PI, notch filter and nonlinear current control methods. In [11] authors used digital sliding mode control for the current loop. In all current loop control designs the goal is to have the measured current closely follow the reference current waveform which then can act as control variable to the voltage loop.

Since the voltage control loop directly controls the peak current drawn from the mains, the DC link ripple is also introduced to the mains current waveform. This causes distortion in the reference of the current control and thereby ripple in the grid current. In order to limit the distortion, the voltage controller has to have limited gain in the frequency range of the DC link ripple. The maximum achievable gain of the DC link voltage under PI control with the given harmonic current levels has been studied in [12]. With the interaction of the DC link ripple and the grid current, the main trade off in the voltage loop control design is balancing the allowable current distortion and the voltage loop dynamics.

Broadly speaking, the methods to increase the voltage dynamics can be categorized into two main groups. The DC link voltage ripple is filtered out or canceled by the estimation of the ripple, or the control parameter is chosen in a way not to include the DC link ripple. The DC link ripple estimation filtering is studied in [13] and [14]. The authors used additional analog circuitry to accurately estimate and cancel the DC link ripple from the voltage control loop thus allowing higher gains for the control. The method provides fast recovery in about three mains cycles from load transient, but requires significant signal processing to obtain an accurate estimate of the ripple. In [15] the authors estimated the ripple, but the required signal processing was done with using a PLL and a digital controller. With the ripple estimation the converter was able to stabilize in about two mains cycles.

In [16], the voltage loop was studied under a control based on a discrete energy function. The idea of the energy function method is to measure the peak power of the load and then use this information to determine a feed forward term to improve the response of the voltage control loop to load changes. The discrete energy function approach was shown to recover approximately within two mains cycles. A nonlinear controller based on a discrete energy Lyapunov function was designed in [17]. The controller in question is a nonlinear state-space controller and regulates both the voltage and the sinusoidal current. The control system manages to stabilize the control loop in two to three main cycles. In addition, in [18] and [19], fuzzy logic has been studied for the voltage loop control. The authors in [20] used extended state observer to estimate the load current of 3-phase rectifier. The load current estimate is used in place of load current measurement feed forward to improve the regulation of the DC link during load transient.

This paper presents a nonlinear PI control method for voltage control in a PFC system, which can provide a fast step response and low current loop distortion. Compared with foregoing papers [9], [12], [13], [16], [17], the proposed approach has several advantages; the approach is simple to tune as the tuning procedure is similar as in a standard linear PI-controller, while the overall controller complexity is kept to a minimum. With the proposed control, the obtained load transient dynamics are at least as good as can be obtained by 'best' linear control [12] or nonlinear control with more complex structure, such as used in [17]. Finally, a major improvement in the harmonic peformance is obtained by control gain scheduling. The nonlinear control allows the DC link voltage loop to be designed to recover from a load step in approximately two mains cycles while still performing within the harmonic current standards. The nonlinear control system is implemented using a PI controller with variable control gains, which depend on the error between the measured DC link voltage and the DC link reference. This allows to speed up the DC link dynamics when the system voltage error is higher than the DC link voltage ripple but the gain for the DC link ripple is low at a constant load. The presented controller performance is shown experimentally, and a simple tuning method is provided. The controller is implemented with digital hardware and shown to be only marginally more complicated when compared with a PI control.

The experimental setup used for this study has an interleaved boost circuit providing the PFC operation. The main circuit of the applied PFC is presented in Fig. 1. The control system measures the mains voltage u_{AC}, the DC link voltage u_{DC}, and the switch currents i_1 and i_2. The controller uses the mains voltage for current reference generation and feedforward control of the current loop. The DC link voltage is used as a

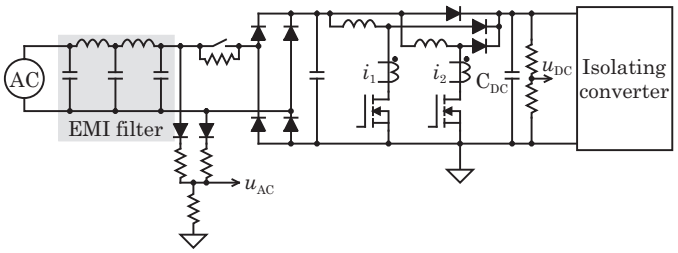

Fig. 1. Structure of the parallel boost PFC. The PFC has two identical boost converters in parallel, and the boost switches are controlled with switchings 180 degrees out of phase. This effectively doubles the apparent switching frequency and reduces the switching ripple from the input current.

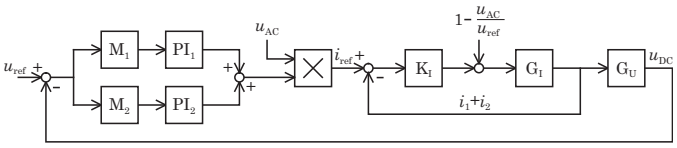

Fig. 2. Controller structure of the nonlinear controller. The scaling functions M_1 and M_2 are used to weigh the output of slow and fast controllers. G_I and G_U describe the current loop and voltage loop dynamics, respectively.

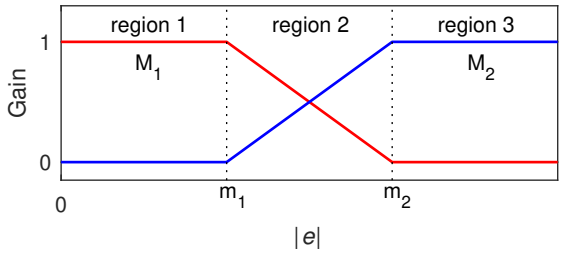

Fig. 3. Interpolating functions M_1 and M_2. Absolute value of the error is used as the interpolating functions are symmetric about the origin.

feedback for the voltage control. The objective of the entire PFC system is to shape the grid current to follow the grid voltage waveform and to keep the DC link voltage at 405 V.

The paper is organized as follows. Section II discusses the problem statement and introduces the nonlinear controller. After that, Section III discusses the calculation burden and effective implementation of the proposed controller. Finally, in Section IV, the performance of the nonlinear control is experimentally evaluated and compared with a linear PI controller.

II. Problem Statement

The voltage control loop in a PFC system provides the current reference for the current control. The inner current controller is needed for the current to track the mains voltage waveform. In practice, the inner loop has a significantly higher bandwidth than the mains frequency, and therefore, the cascaded current and voltage control loops can be designed separately. In this paper, only the outer voltage loop is considered. This paper addresses issues in the voltage control loop design of a PFC system, and particular attention is paid to reduce the harmonic content and improve the dynamic performance. It is emphasized that, owing to specific design aspects of the voltage loop performance and the fact that the control loop can be designed separately, this paper focuses exclusively on the voltage control loop design. In practice, for the current control loop, any conventional current controller that can be used with a PI-controlled voltage loop works with the nonlinear voltage controller. The chosen design method for the nonlinear PI voltage controller is studied in state-feedback representation, and the method is based on a Takagi-Sugeno (T-S) type nonlinear model. The control structure is depicted in Fig. 2. The T-S type nonlinear model consists of linear submodels and the output is a weighted sum of the linear models. A controller that has a parallel structure and weighting functions is referred to as a parallel distributed controller (PDC). The PDC is commonly given in a state-feedback form

$$u = \sum_{i=1}^{r} M_i K_i x(t)\,, \quad i = 1, 2, 3 \ldots r, \tag{1}$$

where r is the number of weighting functions, M_i are the weighting functions used to calculate the output, and K_i are the corresponding control gains. In the fuzzy control literature, the weighting functions are traditionally called membership functions.

Fig. 3 shows the interpolating functions, where m_1 and m_2 are the boundaries of the different operating regions of the controller. When the error is in region 1, the system uses the low-bandwidth controller to ensure low distortion, and correspondingly, when the error is in region 3, high gains are used to provide fast convergence from the load disturbance. When the error is in region 2, the control signal is a weighted sum of the high and low gains.

The most important behavior of the gains is observed when the error is in region 2. In this case, the control signal is a weighted sum of the high- and low-gain PI outputs with the weight depending on the error size. The weighting in region 2 allows smooth transition from low to high gains, which eliminates discontinuity in the control signal that would otherwise occur in the boundary if gains were abruptly increased. The basic idea of the nonlinear PDC with the resulting gain of the controller is shown in Fig. 4, where the dashed lines represent the linear gains and the solid line the nonlinear gain. Note that, the proportional and integral gain functions of the controller have the same overall shape as both the proportional and integral parts are scheduled with the same scaling functions M_1 and M_2.

In this paper, the width of the regions of the different gains is designed so that with the full load the DC link voltage ripple can fit in region 1, which means that the ripple amplitude is less than the chosen voltage level m_1. This ensures that in the steady state the system has linear gains, and thus, the controller nonlinearity does not produce extra harmonics to the current. The size of region 2 was experimentally chosen to be the same as the ripple voltage amplitude.

A. Controller stability

Stability of a system comprised of several subsystems can be proved if a common positive definite matrix P, which is a

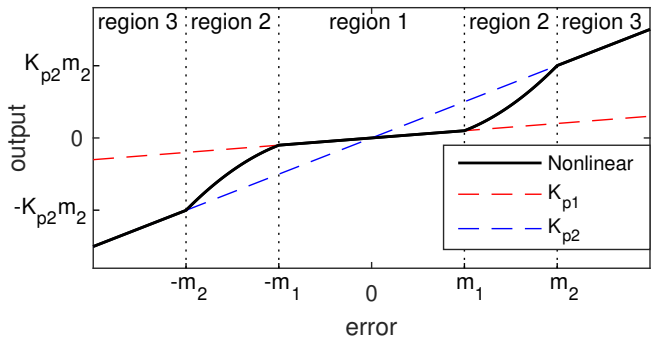

Fig. 4. Linear and nonlinear gains of the controller. The nonlinear gain is indicated by the solid line, and the linear gains are presented with the dashed lines, where red represents low gain and blue high gain.

solution to the Lyapunov inequality (2), can be found. When the system is described with more than one linear model, i.e. $r > 1$ in (1). Lyapunov inequality can be written in the form

$$A_i^T P + P A_i < 0, \quad i = 1, 2...r \tag{2}$$

where A_i are the state matrices for all subsystems. Then, the matrix P forms a quadratic Lyapunov function

$$V(x(t)) = x(t)^T P x(t). \tag{3}$$

Stability can be guaranteed if a common P can be found that fulfills (2) for all i. The benefit of the Takagi-Sugeno type control over direct Lyapunov-function-based designs is that the common positive matrix P can be found straightforwardly using numerical solvers [21]. The numerical solution of (2) is accomplished with linear matrix inequalities (LMIs). Since many control optimization problems in control design can be represented in the LMI framework, the PDC controller can be used as optimization and automation of the nonlinear control design. For example robustness or performance limits can be designed as additional restrictions. These can be designed into the system with robust control methods based on the H_∞ theory [22]. In this paper, the following weighting functions and control gains are considered

$$M_1 = \frac{m_2 - z(t)}{m_2 - m_1}, \quad M_2 = \frac{z(t) - m_1}{m_2 - m_1} \tag{4}$$

$$K_1 = [K_{P_1}, K_{I_1}], \quad K_2 = [K_{P_2}, K_{I_2}], \tag{5}$$

where $z(t)$ is chosen as the absolute value of the error between the measurement and the reference, and m_1, m_2 are the voltage limits for error values that are used to weight the controllers. The closed loop state matrices and common P, which proves stability, are given in Appendix. Note that, the continuous time versions of the equations are be used for the stability analysis of the voltage loop, due to the fact that the control frequency (see Table I) is several decades faster than the bandwidth of the voltage controller. Thus, the effects of the sampling and calculation becomes insignificant.

III. Nonlinear voltage control implementation

The voltage loop bandwidth of the PFC is limited to be less than the mains frequency and the current is controlled with high bandwidth controller relative to the voltage. Since the current is controlled with the inner loop as seen in Fig. 2, the controlled parameter is the input current. The control model for the DC link voltage is then made with the current as input and the the DC link voltage as output. The model is

$$C \cdot \dot{u}_{DC}(t) = i(t) - \frac{u_{DC}(t)}{R} \tag{6}$$

where u_{DC} is the controlled DC link voltage, C is the DC link capacitance, $i(t)$ is the controlled current and R models the load as a resistance. As the control object is to regulate the error between measured DC link voltage and reference to zero, the system is represented with controlled state being the error between DC link voltage $u_{DC}(t)$ and reference u_{ref}.

$$e(t) = u_{DC}(t) - u_{\text{ref}} \tag{7}$$

The DC link is modeled with error as the state and controlled current as the input. The control model can then written as

$$\dot{e}(t) = \frac{1}{C} \cdot \left(i(t) - \frac{e(t)}{R} \right) \tag{8}$$

Since the system is to be controlled with integrating controller, the model is augmented with the integrator state, which is represented by ω. Using a standard PI controller

$$i(t) = -K_P e(t) + \omega(t) \tag{9}$$

$$\dot{\omega}(t) = -K_I e(t) \tag{10}$$

and combining (8) and (9)–(10) PI controlled DC link dynamic in state-space form is obtained

$$\dot{e}(t) = e(t) \cdot \left(-\frac{K_P}{C} - \frac{1}{RC} \right) + \frac{1}{C}\omega(t) \tag{11}$$

$$\dot{\omega}(t) = -K_I e(t) \tag{12}$$

With the defined form (11)–(12) the voltage loop control can be in practice tuned using any any well-established control design methods like pole placement possibly with optimization, and analyzed with bode diagrams.

When the PDC controller (1) is used, the PI controller (9)-(10) is replaced with

$$u(t) = e(t) \cdot (M_1 K_{P_1} + M_2 K_{P_2}) + \omega(t) \tag{13}$$

$$\dot{\omega}(t) = e(t) \cdot (M_1 K_{I_1} + M_2 K_{I_2}) \tag{14}$$

The interpolating functions M_1 and M_2 determines the control behavior so that when the error is less than m_1 or more than m_2, only a single PI controller is used. Therefore the controller implementation differs from the traditional PI control only in the region where the gains are interpolated.

In order to make the implementation to more convenient form the controller (13)–(14) is brought to simpler form. As stated above, in the case of the PI controlled DC link voltage, the measured signal $z(t)$ is the absolute value of error $|e(t)|$ between measured DC link voltage and reference and m_i are the voltage levels which are used to schedule the gains of the controllers. Substituting (4) to (13)–(14) yields

$$u(t) = e(t) \cdot \left((m_2 - |e(t)|) \frac{K_{P_1}}{m_2 - m_1} + (|e(t)| - m_1) \frac{K_{P_2}}{m_2 - m_1} \right) + \omega \tag{15}$$

$$\dot{\omega} = e(t) \cdot \left((m_2 - |e(t)|) \frac{K_{I_1}}{m_2 - m_1} + (|e(t)| - m_1) \frac{K_{I_2}}{m_2 - m_1} \right). \tag{16}$$

By rearranging the terms (15)–(16) following form for the controller is obtained

$$u(t) = \frac{K_{P_1} m_2}{m_2 - m_1} e(t) - \frac{K_{P_2} m_1}{m_2 - m_1} e(t) + \left(\frac{K_{P_2}}{m_2 - m_1} - \frac{K_{P_1}}{m_2 - m_1} \right) e(t) \, |e(t)| + \omega \tag{17}$$

$$\dot{\omega} = \frac{K_{I_1} m_2 e(t)}{m_2 - m_1} - \frac{K_{I_2} m_1 e(t)}{m_2 - m_1} + \left(\frac{K_{I_2}}{m_2 - m_1} - \frac{K_{I_1}}{m_2 - m_1} \right) e(t) \, |e(t)| \tag{18}$$

Defining the constants in (17)–(18) as

$$K_p = (pK_{P_1} m_2 - pK_{P_2} m_1) \tag{19}$$

$$K_i = (pK_{I_1} m_2 - pK_{I_2} m_1) \tag{20}$$

$$K_{p^2} = (pK_{P_2} - pK_{P_1}) \tag{21}$$

$$K_{i^2} = (pK_{I_2} - pK_{I_1}) \tag{22}$$

$$p = \frac{1}{m_2 - m_1} \tag{23}$$

the controller (17)–(18) can be then simplified to

$$u(t) = e(t) \cdot K_p + e(t) \cdot |e(t)| \cdot K_{p^2} + \omega(t) \tag{24}$$

$$\dot{\omega}(t) = e(t) \cdot K_i + e(t) \cdot |e(t)| \cdot K_{i^2} \tag{25}$$

Note that the small subscript terms now denote gain terms of the nonlinear controller.

The full nonlinear PI controller is achieved by scheduling the gains with the error term

$$\begin{aligned}
&\text{if } |e(t)| < m_1 \\
&\qquad u(t) = e(t) \cdot K_{P_1} + \omega \\
&\qquad \dot{\omega} = e(t) \cdot K_{I_1} \\
&\text{else if } |e(t)| > m_2 \\
&\qquad u(t) = e(t) \cdot K_{P_2} + \omega \\
&\qquad \dot{\omega} = e(t) \cdot K_{I_2} \\
&\text{else} \\
&\qquad u(t) = e(t) \cdot \left(K_p + |e(t)| \cdot K_{p^2} \right) + \omega(t) \\
&\qquad \dot{\omega}(t) = e(t) \cdot \left(K_i + |e(t)| \cdot K_{i^2} \right)
\end{aligned} \tag{26}$$

It is important to notice from the implementation of the full controller increases the complexity of the standard PI controller only by a maximum of 2 comparison operations, 2 multiplications, 2 sums and an absolute value calculation.

A. Controller tuning

Since the nonlinear controller is a composite of 2 PI controllers and the voltage regions, the authors suggest the following control design method with following design steps for the presented high performance PFC voltage control.

1) Tune a standard PI controller for desired DC link voltage dynamics. The tuned gains are the fast gains K_{P_2}, K_{I_2}
2) The steady state gains K_{P_1}, K_{I_1} are then scaled down with a factor of 2 from the first set of gains.
3) The voltage range for the low gains m_1 is set to match half of the peak to peak ripple amplitude of the DC link voltage at full load
4) High gain voltage level m_2 is set to $2 \cdot m_1$
5) The full controller from equation (26) is used with the gains calculated from (19)- (23)

Using these definitions the proposed nonlinear controller has the exact same tuning method that is used with standard PI control of the DC link voltage with improved steady state performance. Therefore the presented controller can directly replacing existing PI controller and improve the steady state performance while maintaining the dynamic performance.

The DC link ripple, which is used for the voltage levels where gains are scheduled, can be either measured with the tuned fast PI controller or calculated from simple relation between input power and DC link capacitor size [23].

IV. Experimental results

The system performance is validated by experimental tests using a digitally controlled AC/DC converter prototype shown in Fig. 5. The main components of the system are illustrated; 1) inductor coils, 2) current transformers, 3) DC-link capacitor, 4) EMI-filter, and 5) digital control board. The converter input stage consists of a diode rectifier and a parallel boost stage for the PFC operation. The PFC is loaded with a 3 kW 24 V / 125 A phase-shifted full bridge converter. The converter is controlled using XynergyXS digital control board. The board has a STM32F407 floating point microcontroller and Xilinx Spartan-6 FPGA which is used for system timing

TABLE I
CONVERTER PARAMETERS

Symbol	Quantity	Value
$L_{1\&2}$	boost inductors	500 µH
C	DC link capacitance	1500 µF
K_{P_1}	Proportional gain (slow)	0.3919
K_{I_1}	Integrator gain (slow)	34.0741
K_{P_2}	Proportional gain (fast)	0.7837
K_{I_2}	Integrator gain (fast)	68.1481
f_{ctrl}	control calculation frequency	5 kHz

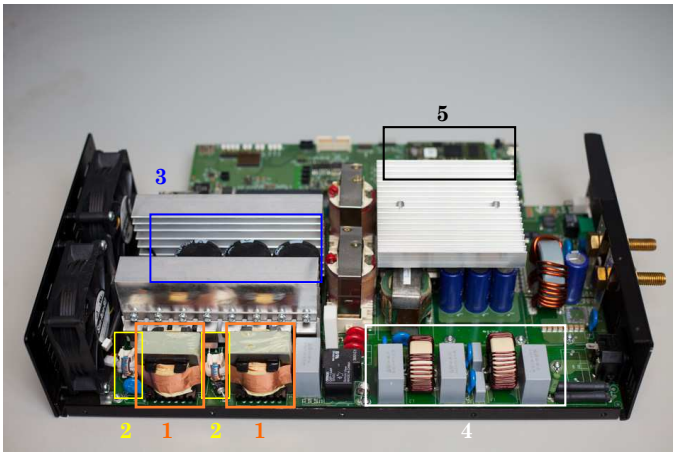

Fig. 5. Power supply used for the experimental measurements. The inductors (1) in the lower left corner are the boost inductors, and the toroidal coils (2) in the lower right corner are the common-mode EMI filter inductors. The current transformers that are used for the switch current measurement are also visible between the PFC inductors.

and modulation. The load steps are applied to the full bridge converter that loads the PFC converter. Since the full bridge converter has a significantly faster settling time than the DC link voltage, the converter is effectively a constant power load to the DC link. The PFC converter parameters are given in Table II. In the experimental tests, the input current and the DC link voltage are measured using an Agilent DSO 6104A oscilloscope. A Tektronix PS5210 differential voltage probe is used for voltage measurements, and Agilent Technologies N2781A 150A/10MHz current probes for current measurements.

The system dynamic operation is tested by applying a 150 W to 2.4 kW and 2.4 kW to 150 W load steps. Figs. 6(a) and 6(b) show the DC link voltage and input current dynamics using linear and nonlinear controllers during the load transient from 150 W to 2.4 kW. It is noted that the nonlinear gain is used when the error is more than 7.8V from the set value of 405 V and the voltages on the Y-axis represent the gain regions of the nonlinear controller. The transient is applied at t = 150 ms, and the system can be seen to stabilize after the load step in roughly two mains cycles. It can be also noticed that the dynamics are practically equivalent in both controllers despite the nonlinear gains being used during the load transient. It is worth mentioning that the current waveform has a significant zero cross distortion which can be seen in Fig. 10. This distortion is caused by limitation of the duty cycle, which is limited by the software to maximum value of 0.8. The hard limit is imposed in order to ensure that the current transformers that are used to measure the feedback current from the switches have enough time to reset in all possible operating conditions.

In Figs. 7(a) and 7(b) the results from the other load step test is shown. Again, similar performance between the controllers can be seen and the control behaves as intended. Since the PFC hardware cannot feed power back to the grid, the PFC operation is simply halted when the DC link voltage goes above 420 VDC. The nonlinear controller has lower overshoot, but this is not caused by the dynamics of the controller, and instead depends on the phase of the grid voltage at which the load is stepped down.

The effect of the nonlinear controller on the grid current quality is evaluated by applying a harmonic current analysis, that is, the total harmonic distortion (THD) is studied. The current harmonics are used to calculate the total harmonic distortion at a 2.4 kW load. The THD calculation is done by taking into account the RMS values of the first 40 current harmonics. In Fig. 8, the input current RMS harmonics are illustrated for both control configurations: the linear PI control and the nonlinear PI control. In addition, the applicable limits for odd harmonics specified in the IEC 61000-3-2 standard for Class A devices are shown with a red curve for both control configurations with the calculated harmonics. Note that, the harmonic limits are slightly different between linear and nonlinear controllers as the fundamental RMS currents are different. Evidently, both controllers have a dominating third harmonic and low amounts of higher-order harmonics. More importantly, it can be observed that the third harmonic is significantly reduced when the nonlinear controller is applied. It can be noticed from the steady-state currents in Figs. 6(a) and 7(a) that the linear voltage controller produce a higher current peak with a higher distortion when compared with the nonlinear control.

Moreover, Fig. 8 shows that in the case of the linear controller, the calculated THD of the input current is 12.36 %, which is mostly due to the elevated third harmonic. Correspondingly, the THD decreases significantly, to 6.13 %, when the nonlinear controller is employed. Thus, the nonlinear controller can achieve an over 50% improvement in the current THD. The measurement was taken with the system input current following the actual mains voltage waveform, and therefore, some of the distortion is caused by the distortion in the mains voltage itself. The mains voltage harmonics with the converter turned off are presented in the bottom Fig. 8. Note that, the mains voltage has noticeable 5th and 7th harmonics, which can be seen in both current harmonics as the PFC current waveform is set to follow the mains voltage.

To further validate the performance of the nonlinear voltage control, in Fig. 9 the measured curve of the power factor with respect to the load power is shown. It can be noticed that with load power above 0.75 kW the PFC system power factor is close to unity. The power factor was measured using Yokogawa PZ4000 power analyzer and a HITEC B2000 current transformer was used for current sensing. Moreover, the steady state waveforms of grid current and voltage at 9.6

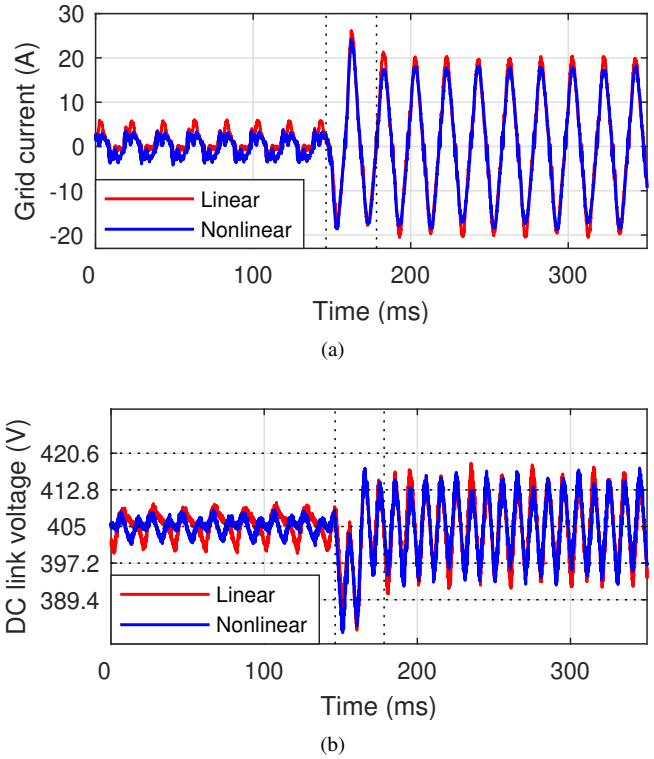

Fig. 6. (a) Input current waveform during a load step from 150 W to 2.4 kW. The load step is applied to the system at t = 150 ms. (b) The voltage of DC link. The settling time of the load step for both control methods is 32 ms.

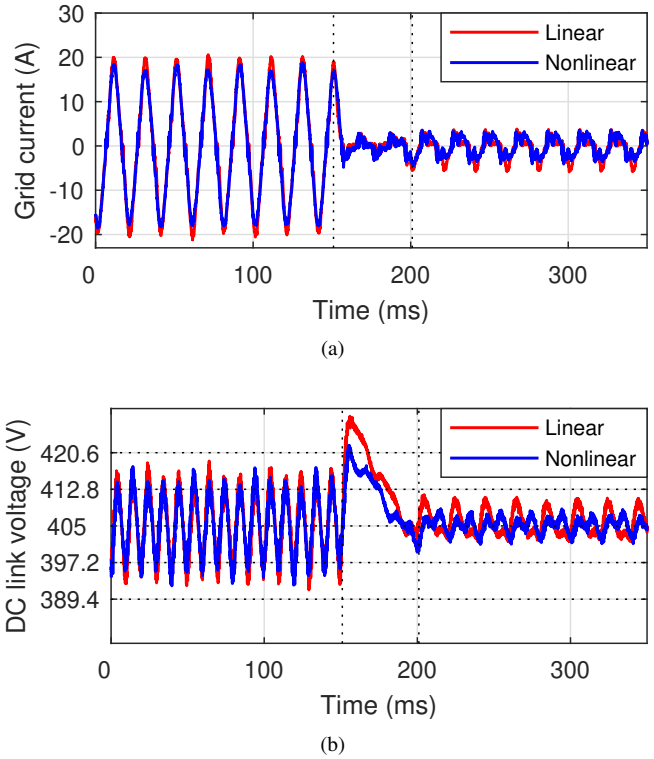

Fig. 7. (a) Input current waveform and (b) the voltage of DC link during a load step from 2.4 kW to 150 W. The load step is applied to the system at t = 150 ms. The voltages on the Y axis represent the gain regions of the nonlinear controller. The settling time of the load step for both control methods is 50 ms.

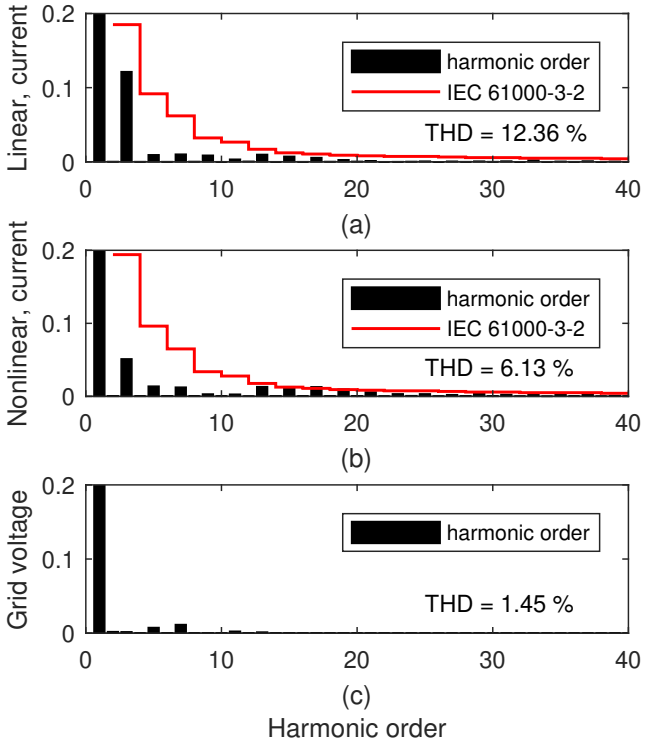

Fig. 8. Comparison of the input current harmonic content with the linear a) and nonlinear b) controllers. The figure c) shows the harmonic content of the mains voltage when the converter is turned off.

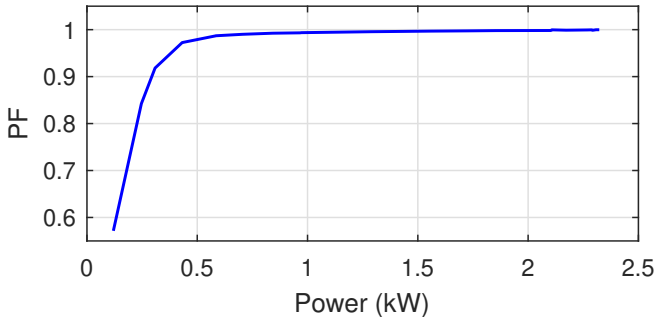

Fig. 9. Power factor with respect to load power using the nonlinear voltage control.

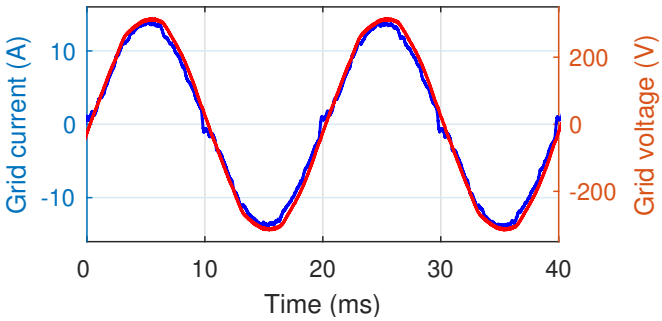

Fig. 10. Steady state waveforms at 9.6 A RMS current with the proposed nonlinear voltage controller regulating the DC link voltage.

A RMS current are shown in Fig. 10 that shows the they are closely to same phase with each other, thus the current follows the mains voltage. The comparison of the linear and nonlinear controllers is given in Table II,where the settling times of load steps test and input current THDs.

TABLE II
CONTROLLER COMPARISON

Input current THD with PI control	12.36 %
Input current THD with proposed Nonlinear control	6.13 %
PI settling time of load step from 150 W to 2.4 kW	32 ms
Nonlinear settling time of load step from 150 W to 2.4 kW	32 ms
PI settling time of load step from 2.4 kW to 150 W	50 ms
Nonlinear settling time of load step from 2.4 kW to 150 W	50 ms

V. CONCLUSIONS

This paper presented a nonlinear controller for the DC link voltage control of a PFC converter. The controller was shown to effectively improve the quality of the mains current when compared with a linear PI controller. It was shown that the proposed nonlinear controller has a simple structure, viz. the complexity is only marginally more complex than a traditionally used linear PI controller. Thus, the simple structure provides benefits for the practical implementation of the algorithm. More importantly, the control can also be tuned straightforwardly with the same method as would be used with the traditional PI controller. The effectiveness of the nonlinear controller was verified by experimental tests using harmonic current analysis and by comparing the time-domain performance of the nonlinear controller with the linear counterpart. The time domain requirement was fulfilled as the proposed nonlinear controller can stabilize the system within two to three mains cycle agains load transient. Note that, this result is comparable to the results obtained with more complex control structures, like in [17]. Moreover, the nonlinear controller was shown to effectively improve the THD of the input current from 12.36 % to 6.13 % without affecting the dynamics of the DC link. The limits for odd harmonics content according to IEC 61000-3-2 were used to show that the proposed controller meet the harmonic requirement for Class A devices.

APPENDIX

Since the controller is known, the proof of stability for the closed loop is the problem of finding common P for the closed loop systems A_i such that that the Lyapunov inequality given in (2) holds. Assuming a no load condition, ie $R = \infty$ the system (11)–(12) can be written in matrix form as

$$A_1 = \begin{bmatrix} -\frac{K_{P1}}{C} & \frac{1}{C} \\ -K_{I1} & 0 \end{bmatrix} = \begin{bmatrix} -261.267 & 666.667 \\ -34.074 & 0 \end{bmatrix}, \quad (27)$$

$$A_2 = \begin{bmatrix} -\frac{K_{P2}}{C} & \frac{1}{C} \\ -K_{I2} & 0 \end{bmatrix} = \begin{bmatrix} -522.467 & 666.667 \\ -68.148 & 0 \end{bmatrix}. \quad (28)$$

The positive definite matrix

$$P = \begin{bmatrix} 16.3972 & -6.6741 \\ -6.6741 & 285.5394 \end{bmatrix} \quad (29)$$

can be verified to prove the stability by substituting A_1 and A_2 and the common P (29) to the Lyapunov inequality (2).

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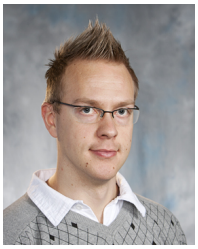
Jari Honkanen (SM'18) was born in Savonlinna, Finland. He received received both the B.Sc. and M.Sc. degrees in electrical engineering from Lappeenranta University of Technology (LUT), Lappeenranta, Finland in 2014. He is currently working towards a D.Sc degree as a Researcher at LUT. His areas of interest include embedded systems, robust and digital control of DC/DC and AC/DC converters.

Janne Hannonen received the D.Sc. degree in electrical engineering from the Lappeenranta University of Technology (LUT), Lappeenranta, Finland, in 2016. His research contributes to digital control of ac/dc and dc/dc power supplies, condition monitoring, and fault detection. Currently he works with power converter R&D in Powernet Oy, Vantaa, Finland



Juhamatti Korhonen (M'17) received the M.Sc. degree in electrical engineering, and the D.Sc. degree from Lappeenranta University of Technology (LUT), Lappeenranta, Finland, in 2008, and 2012, respectively.

He is currently a Postdoctoral Researcher with the School of Energy Systems at Lappeenranta University of Technology. His research interests are in the field of power electronic converters, control and modulation of power electronics, multilevel inverter, and electric drives.

Niko Nevaranta (M'17) received the B.Sc., M.Sc. and D.Sc degrees in electrical engineering from the Lappeenranta University of Technology (LUT), Lappeenranta, Finland in 2010, 2011 and 2016, respectively, where he is currently working as a Post-Doctoral Researcher. During 2018 he also worked as a visiting Post-Doctoral Researcher at the KTH Royal Institute of Technology, Stockholm, Sweden.

His research interest includes modeling and control of electrical drives, motion control, system identification, parameter estimation, system monitoring, and diagnostics. Currently he is also researching control approaches for active magnetic bearings and methods for rotor dynamics identification.

Pertti Silventoinen (M'09) was born in Simpele, Finland, in 1965. He received the D.Sc degree from Lappeenranta University of Technology (LUT), Lappeenranta, Finland, in 2001. He became a professor of applied electronics in 2004. His current research interests include power electronics systems in various applications.