LUT UNIVERSITY
LUT School of Energy Systems
Degree Program in Electrical Engineering

Maarit Peltomäki

DESIGN OF A LIMITING AMPLIFIER FOR A MILLIMETER-WAVE RECEIVER BASEBAND

Examiners: Professor Pertti Silventoinen
M. Sc. Sami Vilhonen

TIIVISTELMÄ

LUT-YLIOPISTO
LUT School of Energy Systems
Sähkötekniikan koulutusohjelma

Maarit Peltomäki

Rajoittavan vahvistimen suunnittelu millimetriaaltoalueen vastaanottimen kantataajuudelle

Diplomityö

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88 sivua, 74 kuvaa, 9 taulukkoa ja 1 liite

Tarkastajat: Professori Pertti Silventoinen
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Maailmanlaajuisesti lisensioimaton 60 GHz:n taajuuskaista tarjoaa mielenkiintoisen tutkimuskohteen langattomien sovellusten kehittäjille. Nykyään saatavilla olevat puolijohdeteknologiat mahdollistavat tämän taajuusalueen käytön edullisilla lyhyen kantaman laitteilla. Tässä diplomityössä esitetään rajoittavan vahvistimen suunnittelu 60 GHz:n integroidun mikrosirun vastaanottimen kantataajuudelle. Rajoittavan vahvistimen vahvistuksen kaistanleveyden tulee olla satoja gigahertsejä, mikä yhdessä kohinavaatimusten ja komponenttiasettelun pinta-alarajoitusten kanssa asettaa haasteita vahvistintopologialle.

Sopiva topologia valitaan kirjallisuustutkimuksen ja matemaattisen mallinnuksen avulla. Valittu topologia toteutetaan yksityiskohtaisella piirikaavio- ja asettelusuunnittelulla. Tällä taajuusalueella sirun parasiittisilla komponenteilla on suuri merkitys vahvistimen toimintaan. Suorituskyky varmistetaan simuloimalla komponenttien asettelusta tehtyä mallia, joka huomioi parasiittiset komponentit. Tyypillisten olosuhteiden lisäksi simuloinnit tehdään esimerkiksi matalilla ja korkeilla lämpötiloilla sekä prosessin ääriolosuhteissa. Simulointitulosten perusteella saavutetaan yli 10 GHz:n kaistanleveys sekä lähes 30 dB:n vahvistus, mikä täyttää vahvistimelle asetetut vaatimukset.

ABSTRACT

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Design of a limiting amplifier for a millimeter-wave receiver baseband

Master's Thesis

2019

88 pages, 74 figures, 9 tables and 1 appendix

Examiners: Professor Pertti Silventoinen
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The globally unlicensed frequency band at around 60 GHz provides an interesting area of research for wireless communications device developers. The semiconductor technologies available nowadays make this frequency range usable for low-cost, short-range devices. This thesis presents the design of a limiting amplifier for a 60 GHz integrated-circuit receiver's baseband. A gain-bandwidth product of hundreds of gigahertz is required from the limiting amplifier, which together with the noise floor requirements and layout area limitations impose a challenge to the topology.

A suitable topology is chosen based on literature study and mathematical modelling. The chosen topology is then implemented with detailed schematic and layout design. In this frequency range, the parasitic components produced in the layout have a significant influence on the performance of the amplifier. The performance is verified by simulating the layout extractions, which contain the parasitic components. Simulations in typical conditions as well as in extreme conditions, such as high and low temperatures and process corners, are conducted. The simulation results show that the limiting amplifier has a bandwidth of over 10 GHz and a gain of almost 30 dB, which fulfill the requirements set for the amplifier.

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In Turku, 3.4.2019

Maarit Peltomäki

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LIST OF SYMBOLS AND ABBREVIATIONS

AC	alternating current
ASK	amplitude shift keying
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio
CS	common-source
DC	direct current
FET	field-effect transistor
FSK	frequency-shift keying
HPF	high-pass filter
IC	integrated circuit
LA	limiting amplifier
LNA	low-noise amplifier
LPF	low-pass filter
NMOS	n-channel metal-oxide semiconductor
OOK	on-off keying
PMOS	p-channel metal-oxide semiconductor
Q	transistor
RF	radio frequency
S	switch
VCCS	voltage-controlled current source

A	gain
A_i	intrinsic gain
BER	bit-error rate
BW	bandwidth
C	capacitance
D	input dynamic range
e	difference signal (in feedback circuit)
F_n	noise factor

f	frequency
f_T	unity-gain frequency
fb	feedback signal (in feedback circuit)
g_m	transconductance
GBW	gain-bandwidth product
GM	gain margin
H	transfer function
I	direct current
i	small-signal current
K	Boltzmann's constant
k_n	MOSFET transconductance parameter
k_n'	process transconductance parameter for the n-channel transistor
k_p'	process transconductance parameter for the p-channel transistor
L	transistor length
m	order of gain stage
n	number of cells
NF	noise figure
P	power
PM	phase margin
R	resistance
R_{cs}	current source resistance
r_o	transistor output resistance
s	complex-frequency variable
SNR	signal-to-noise ratio
T_0	room temperature
V	voltage
v	small-signal voltage
V_A	Early voltage
V_{DD}	supply voltage
W	transistor width
W/L	width-to-length ratio

x	input signal (in feedback circuit)
y	output signal (in feedback circuit)
Z	impedance

A	ampere
˚C	Celsius
dB	decibel
F	farad
Gb	gigabit
Hz	hertz
J	joule
K	kelvin
m	meter
S	siemens
s	second
V	volts
W	watt
˚	degree
%	percentage

β	feedback factor
Δ	difference
Ω	ohms
ω	angular frequency
ω_T	unity-gain angular frequency

Footnotes

cl	closed-loop
CM	common-mode
core	amplifier core

cs	current source
D	drain
dcoff	direct current offset cancellation circuit
DD	supply/operating
DS	large-signal drain-to-source
ds	small-signal drain-to-source
e	difference
fb	feedback
ff	feedforward
gd	small-signal gate-to-drain
GS	large-signal gate-to-source
gs	small-signal gate-to-source
H	high
in	input
L	low
M	midband
max	maximum
min	minimum
ni	noise in
no	noise out
out	output
OV	overdrive
p	pole
SD	large-signal source-to-drain
SG	large-signal source-to-gate
th	threshold
tn	thermal noise
tot	total
z	zero

1 INTRODUCTION

1.1 Background

The frequency band from 30 GHz to 300 GHz is known as the millimeter-wave band according to the wavelength over these frequencies (FCC 2013). Deployed earlier almost exclusively by government and non-consumer products, over the past years the millimeter-wave band has experienced a growing interest to be used in short-range wireless communications. The development of semiconductor technology has made it possible to create low-cost solutions to be utilized in frequencies above 30 GHz (Bosco et al. 2006).

There is a globally unlicensed band available at around 60 GHz, which is now subject to research in order to provide commercial products using this frequency band. The propagation range of signals at 60 GHz is quite low because of their sensitivity to oxygen and water vapor in the atmosphere (FCC 2013). In addition, wall materials, such as concrete, attenuate signals at 60 GHz substantially. These attenuation factors could be considered as a disadvantage, but in fact, they make the millimeter-wave frequency band optimal for short-range, unlicensed devices. The company LG Electronics Finland Lab, Inc. has their own research project relating to wireless communications in the 60 GHz range. The chip is implemented with a nanometer-scale integrated-circuit (IC) process. In this thesis, a limiting amplifier (LA) is designed and simulated for this project's receiver's baseband.

The modulation scheme used in the receiver is on-off-keying (OOK), which can be defined as a special case of amplitude-shift keying (ASK) (Anthes 2017). OOK modulation is employed for its simplicity; a carrier wave in the received signal represents a binary one, and when no carrier wave is present, a binary zero is received. An example of a constellation diagram of the OOK modulation is shown in Figure 1.1. As depicted in Figure 1.1, the phase of the signal is not relevant, only the magnitude.

From the transfer point-of-view, the OOK modulation technique decreases power consumption since the transmitter can idle while a zero is transmitted. From the receiver's point-of-view, a simpler topology is applicable when compared to frequency-shift keying (FSK). Darrell (1992) found the OOK receiver's performance to be equal to or better than that of the FSK receiver's in the presence of amplitude flicker. Drawback of the OOK modulation is its sensitivity to

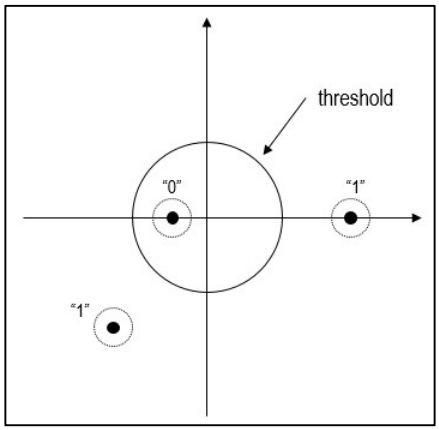

Figure 1.1. A constellation diagram of the OOK modulation. The threshold is depicted as a solid circle around the origin. Received data is presented as black dots and the dashed circles around them represent the additive noise.

interference, since difference between received ones and zeros is simply defined by the threshold voltage. In Figure 1.1, the interference is shown as the dashed circle around the black dot that represents the actual signal. The lack of a reference level can lead to faulty receiving should the signal strength fall below the threshold defined for the receiver (Carr & Winder 1994). However, Darrell (1992) showed that under certain conditions, the sensitivity and performance in the presence of co-channel interference might prove better for the OOK modulation than for the FSK modulation.

1.2 Goals and delimitations

A block diagram of the receiver is presented in Figure 1.2. A low-noise amplifier (LNA) receives the incoming radio-frequency (RF) signal from the antenna. This signal is then fed to a mixer, which converts it to the baseband frequency of about 5 GHz. The limiting amplifier then amplifies the signal before it is fed through the output buffer to an analog-to-digital converter.

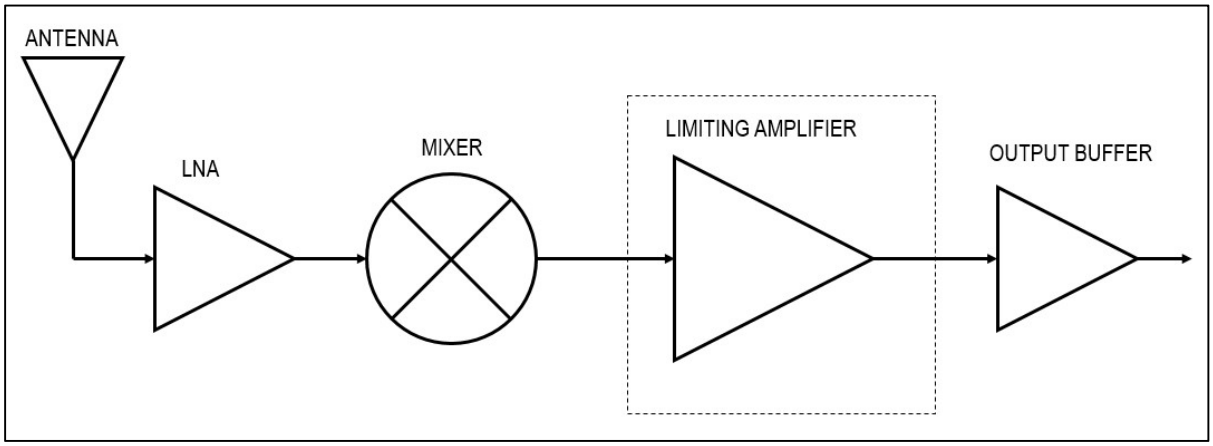

Figure 1.2. A block diagram of the receiver topology. The received signal travels from the antenna through the LNA, mixer and limiting amplifier to the output buffer.

In the system design phase of this project, it is concluded that the baseband LA should be able to receive a data rate of at least 6 Gb/s for which the bandwidth target is set to a minimum of 10 GHz. Similarly, in the system design, it is concluded that with the noise floor requirements of the receiver, the limiting amplifier should have a maximum available voltage gain of 30 dB.

The limiting amplifier limits the output power as the input power increases. A typical plot of the peak-to-peak output voltage V_{out} versus peak-to-peak input voltage V_{in} is shown in Figure 1.3.

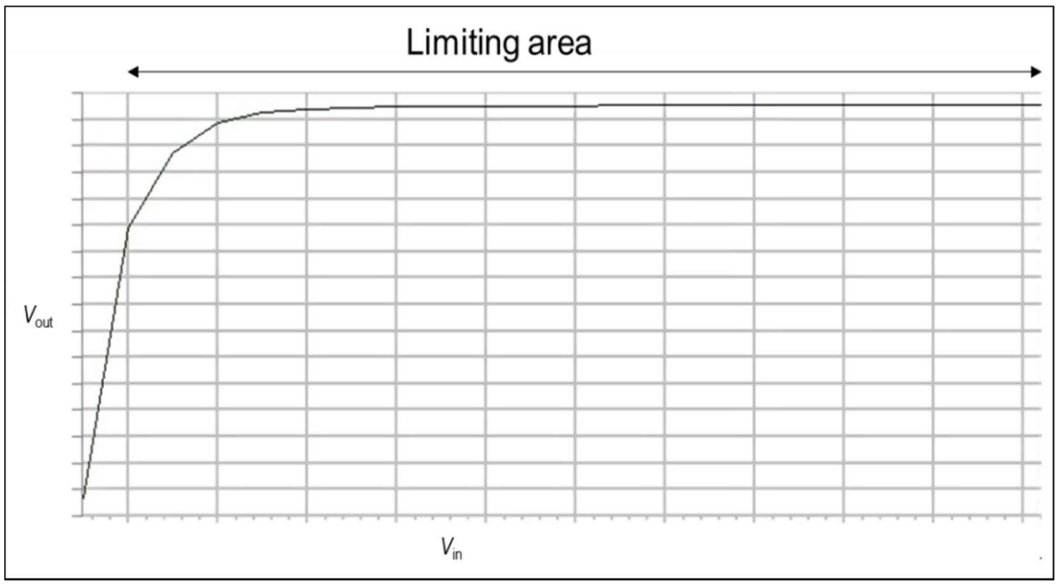

Figure 1.3. A typical output voltage as a function of input voltage curve for a limiting amplifier.

The area of the maximum available voltage gain is found at the small values of V_{in}, where the slope of the curve is at its highest. The advantage of the limiting amplifier topology is the performance in the limiting area; while the input voltage's amplitude increases, the output voltage's amplitude is limited to a value usually below the operating voltage. Hence, there is room for the input voltage to increase without slew rate increasing in the output signal. In other words, the LA is able to maintain its bandwidth even with high input voltages. This is a significant feature with the OOK modulation technique. One of the important performance figures of a LA is its input dynamic range (*D*) which is the ratio of the highest possible input voltage and the smallest input voltage with which the limiting range commences.

Another important feature of the LA, when using the OOK modulation, is its ability to reject unwanted direct current (DC) signal caused by non-idealities in the receiver. To achieve this, the limiting amplifier should attenuate signals under the range of few tens of megahertz. In addition to the aforementioned requirements, an important measure of performance for the amplifier is its noise figure. Table 1.1 lists the initial requirements for the LA.

Table 1.1. Initial requirements for the limiting amplifier.

Parameter	**Requirement**
Maximum midband gain	30 dB
Bandwidth lower corner frequency	20 – 70 MHz
Bandwidth upper corner frequency	10 GHz
Signal-to-noise ratio	> 20 dB
Data rate	6 Gb/s
Noise figure	< 20 dB

The challenge of the design is to find an optimal LA topology to achieve the required gain and bandwidth, while keeping the power consumption as low as possible. It is known that in general, to improve the gain-bandwidth product of an amplifier, multiple cascaded stages need to be used. However, every stage increases the power consumption and adds to the noise floor. In addition, a complex design brings challenges to the layout implementation. When operating in the gigahertz range, the signal paths of the layout introduce significant parasitic components.

1.3 Structure of the thesis

The thesis is divided as follows. In chapter 2, the general performance considerations of an amplifier are discussed. Chapter 3 introduces earlier studies about limiting amplifier topologies and a topology decision for the amplifier to be designed is made. In chapter 4, the implementation of the amplifier is presented in detail. The chapter goes through different sub-circuits of the amplifier, and the layout implementation is also presented. Chapter 5 includes the simulations of the basic operation of the amplifier as well as multiple validation simulations in possible occurring operating conditions. The key parameters describing the performance of the amplifier are obtained. Chapter 6 concludes the thesis with analysis of the correlation between the originally set targets and the simulated performance of the amplifier.

2 PERFOMANCE OF AN AMPLIFIER

2.1 The frequency response

The frequency response of an amplifier is divided into three frequency bands; the low-frequency band, the midband and the high-frequency band. The distinction between the bands is made by the lower corner frequency, f_L and higher corner frequency, f_H. The corner frequencies are defined as the frequencies where the midband gain has decreased by 3 dB and are referred to as the 3-dB frequencies or the cut-off frequencies. An amplitude response curve with voltage gain V_{out}/V_{in} as a function of frequency is shown in Figure 2.1.

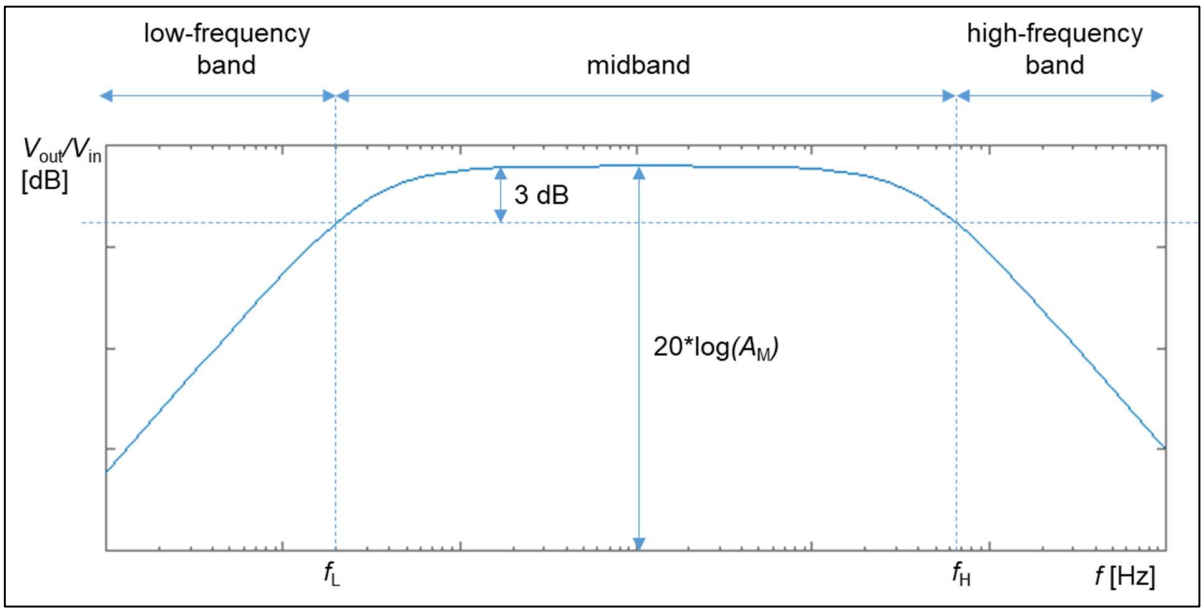

Figure 2.1. An example of an amplitude response curve with the low-frequency band, midband and high-frequency band distinguished.

The midband of the amplifier is also referred to as the bandwidth (*BW*) or 3-dB bandwidth of the amplifier, and it is the difference of f_H and f_L as shown in equation (2.1).

$$BW = f_H - f_L \tag{2.1}$$

At low frequencies, the gain falls due to the large capacitances of the circuit, such as coupling capacitors between the amplifier stages. At high frequencies, the bandwidth is limited by the internal, small parasitic capacitances of the circuit. With the large and small capacitances taken

into account, the amplifier gain as a function of the complex-frequency variable *s* is expressed as (Sedra & Smith 2004)

$$A(s) = A_{\mathrm{M}} H_{\mathrm{L}}(s) H_{\mathrm{H}}(s) \tag{2.2}$$

where A_{M} is the midband voltage gain, $H_{\mathrm{L}}(s)$ is the low-frequency transfer function and $H_{\mathrm{H}}(s)$ is the high-frequency transfer function of the system, respectively. The frequency-dependent transfer functions are expressed as

$$H_{\mathrm{L}}(s) = \frac{(s+\omega_{\mathrm{z1L}})(s+\omega_{\mathrm{z2L}}) \dots (s+\omega_{\mathrm{ziL}})}{(s+\omega_{\mathrm{p1L}})(s+\omega_{\mathrm{p2L}}) \dots (s+\omega_{\mathrm{piL}})} \tag{2.3}$$

$$H_{\mathrm{H}}(s) = \frac{\left(1+\frac{s}{\omega_{\mathrm{z1H}}}\right)\left(1+\frac{s}{\omega_{\mathrm{z2H}}}\right) \dots \left(1+\frac{s}{\omega_{\mathrm{ziH}}}\right)}{\left(1+\frac{s}{\omega_{\mathrm{p1H}}}\right)\left(1+\frac{s}{\omega_{\mathrm{p2H}}}\right) \dots \left(1+\frac{s}{\omega_{\mathrm{piH}}}\right)} \tag{2.4}$$

$$H(s) = H_{\mathrm{L}}(s) H_{\mathrm{H}}(s) \tag{2.5}$$

where ω is the angular frequency, ω_{z1}, ω_{z2}, …, ω_{zn} represent the angular frequencies of the transmission zeros and ω_{p1}, ω_{p2}, …, ω_{pn} represent the angular frequencies of the poles. From equation (2.5), the poles and zeros can be solved by solving the roots of the numerator and denominator. The poles and zeros are either real or appear in complex conjugate pairs. After solving the poles and zeros, the system dynamics can be represented graphically with a pole-zero plot on the *s*-plane, as shown in **Error! Reference source not found.**.

Solving the poles and zeros of the transfer function also allows to draw the Bode plots of the system. The Bode plots are idealized plots of the frequency response, named after their developer Henrik Bode. They describe the frequency response of the system in terms of amplitude and phase response. Every pole and zero contribute to the plots above their break point, and the break point is the absolute value of the pole or zero, hence their distance from the origin on the *s*-plane.

Each zero contributes a change of +20 dB per decade in the amplitude response, and each pole contributes a change of -20 dB per decade. Hence, a zero of pole complex conjugate pair will contribute a change of ±40 dB per decade. A pole or a zero at the origin defines the initial slope of the Bode plot.

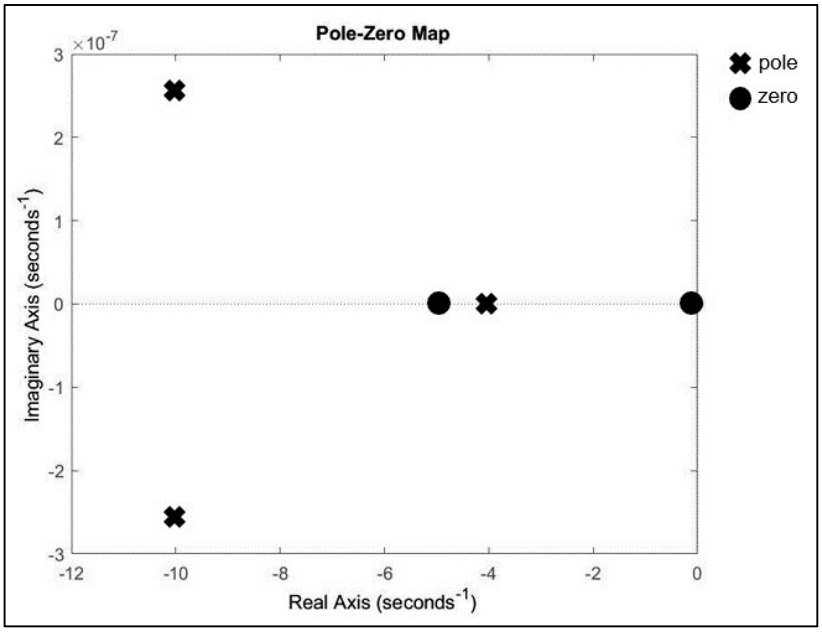

Figure 2.2. A pole-zero map of a system.

In the phase response plot, a pole at the origin contributes an initial phase of -90˚ and a zero at the origin contributes an initial phase of +90˚. Mathematically, the phase shift by the poles and zeros is expressed as

$$\measuredangle H(s) = \tan^{-1}\left(\frac{\omega}{\omega_{z1}}\right) + \cdots + \tan^{-1}\left(\frac{\omega}{\omega_{zm}}\right) - \tan^{-1}\left(\frac{\omega}{\omega_{p1}}\right) - \ldots - \tan^{-1}\left(\frac{\omega}{\omega_{pn}}\right) \qquad (2.6)$$

From the expression of equation (2.6), it can be derived that each break point contributes a phase shift of ±45˚ per decade starting one decade before the break point. A complex conjugate pair in the *s*-plane will contribute a phase shift of ±90˚ starting a decade before the corresponding break point.

2.2 The negative feedback

Negative feedback is introduced in amplifiers to extend the bandwidth, desensitize the gain to variations in the values of the circuit components and to improve the linearity of the amplifier. The general structure of the negative feedback is show in Figure 2.2.

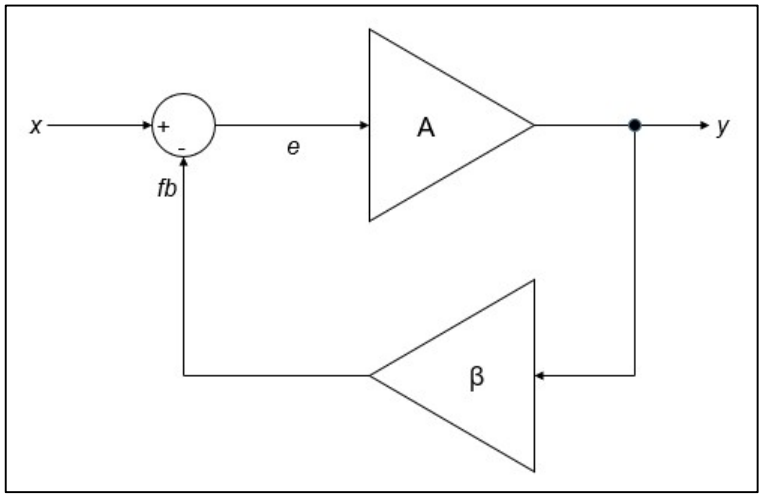

Figure 2.2. Block diagram of a system with negative feedback. The input signal is denoted with *x*, the output signal with *y* and the feedback signal with *fb*. The difference between the input and feedback signals is *e*.

In Figure 2.2, A is the open-loop gain of the amplifier and β is the feedback factor. The input is denoted with x and the output with y, fb is the feedback signal and e is the difference of x and fb. A block diagram analysis of Figure 2.2 gives

$$y = A \cdot e \tag{2.7}$$

$$fb = \beta \cdot y \tag{2.8}$$

$$e = x - fb \tag{2.9}$$

$$A_{\mathrm{cl}} = \frac{y}{x} = \frac{A}{1 + A \cdot \beta}, \tag{2.10}$$

where A_{cl} is the closed-loop gain of the system in Figure 2.2. The multiplication $A \cdot \beta$ is known as the amount of feedback. From the expression of equation (2.10), it can be concluded that if the loop gain $A \cdot \beta$ is much larger than 1, then $A_{\mathrm{cl}} \approx 1/\beta$ and only the feedback circuit determines the gain of the amplifier.

The effect of negative feedback on gain sensitivity is found by derivation of both sides of equation (2.10).

$$dA_{\mathrm{cl}} = \frac{dA}{(1 + A \cdot \beta)^2} \tag{2.11}$$

Dividing this result with equation (2.10) results in

$$\frac{dA_{\mathrm{cl}}}{A_{\mathrm{cl}}} = \frac{1}{1 + A \cdot \beta} \cdot \frac{dA}{A}, \tag{2.12}$$

which shows that the closed-loop gain is much less sensitive to, for example, process- and temperature-related variations than the open-loop gain. The distinction between these two is equal to $1 + A \cdot \beta$. It is assumed here that the feedback factor is constant.

Negative feedback affects the lower and upper 3-dB frequencies by a factor equal to the amount of feedback. For example, an amplifier with a dominant low-frequency pole ω_{L} and a midband gain A_{M} has a transfer function

$$A(s) = \frac{A_{\mathrm{M}} \cdot s}{s + \omega_{\mathrm{L}}} \tag{2.13}$$

Substituting this to equation (2.10) yields

$$A_{\mathrm{cl}}(s) = \frac{\frac{A_{\mathrm{M}} \cdot s}{s + \omega_{\mathrm{L}}}}{1 + \frac{A_{\mathrm{M}} \cdot s}{s + \omega_{\mathrm{L}}} \cdot \beta} \tag{2.14}$$

Manipulating equation (2.14) results in

$$A_{\mathrm{cl}}(s) = \frac{\frac{A_{\mathrm{M}}}{1 + A_{\mathrm{M}} \cdot \beta} \cdot s}{s + \frac{\omega_{\mathrm{L}}}{1 + A_{\mathrm{M}} \cdot \beta}} \tag{2.15}$$

Hence while the midband gain in decreased by the amount of feedback, the bandwidth is increased with the same factor. Similar affect can be shown for the high-frequency transfer function; the midband gain reduces by a factor equal to the amount of feedback while the upper cut-off frequency is increased by the same amount. It should be noticed that the gain-bandwidth product (*GBW*) remains constant.

There are four basic feedback topologies categorized by whether the feedback circuit's input and output are current or voltage mode. The terminology used by Sedra and Smith (2004) defines the feedback input (hence, the amplifier output) as a sample and the feedback output (the amplifier input, respectively) as a mix. To avoid confusion with the term sampling usually related to e.g. signal processing, the terms used by Sedra and Smith are replaced with input and output, referring to the feedback circuit (nodes *y* and *fb* in Figure 2.2). With this notation, the four feedback topologies are (Sedra & Smith 2004, pp. 814-822)

- voltage output and voltage input (also known as the series-shunt topology)

- current output and current input (the shunt-series topology)
- voltage output and current input (the series-series topology)
- current output and voltage input (the shunt-shunt topology).

The feedback can be implemented as active or passive, or as combinations of these two. Active feedback contains active components, such as transistors, whereas passive feedback is implemented with passive components. Choosing the feedback implementation is a design trade-off, for example resistors and transistors in the feedback circuit degrade the overall noise performance of the amplifier, but implementing capacitors or coils require large chip area.

2.3 Stability

As mentioned in chapter 2.2, negative feedback can be used to relax the amplifier's requirements for accuracy, bandwidth and noise figure. On the contrary, introducing a positive feedback will increase the difference between amplifier's inputs and eventually cause the output to saturate and the loop to become unstable. At high-frequencies, the amplifier may introduce a phase-shift that causes negative feedback to become positive, which again leads to instability of the amplifier.

The transfer function of the system contains information about the stability. A basic criterion for the stability of the system is that its transfer function's numerator is lower order than its denominator. Another criterion states that all poles of the closed-loop system should be in the left half-plane of the real-imaginary co-ordinates. Both criteria are difficult to calculate accurately in the design phase, but the stability can be verified by simulating the amplitude and phase responses of the system. The poles of the system that cause the amplitude response to decrease, also introduce negative phase shift (Carusone, Johns & Martin 2012, p. 209). The point of interest, when examining the amplitude and phase responses, is the frequency at which the magnitude response is 1, or 0 dB. At this frequency, the phase should have shifted no more than 180° for the system to be stable. Important parameters of performance are the phase margin (*PM*) and the gain margin (*GM*), which are depicted in Figure 2.3.

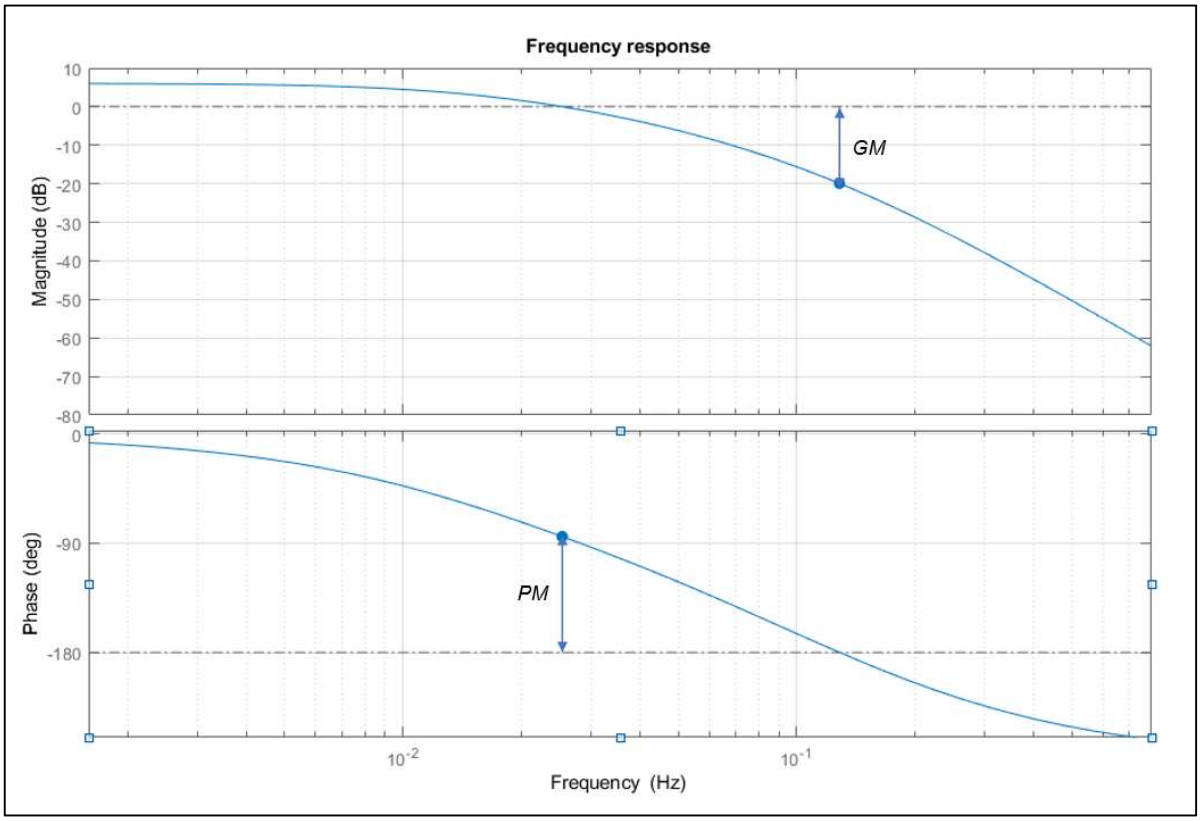

Figure 2.3. A representation of the gain margin (*GM*, upper plot) and the phase margin (*PM*, lower plot).

Phase margin is defined as the difference of the phase shift at the unity-gain frequency to a phase shift of 180°, which would cause the system to become unstable. The phase margin is obtained with

$$PM = \measuredangle H(\omega_T) + 180°, \tag{2.16}$$

where $H(\omega_T)$ is the transfer function of the system as a function of unity-gain angular velocity ω_T. To ensure the system stability in different operating conditions, a phase margin between 45° and 90° is usually required (Carusone, Johns & Martin 2012, p. 211). The gain margin indicates the difference of the gain at a frequency where phase has shifted 180° to the gain of 0 dB.

The stability of the system can be examined in the time plane with the help of a step response curve. This can be simulated by feeding the input of the system with a unit step function and examining the output's response. Figure 2.4 shows possible outcomes of this test.

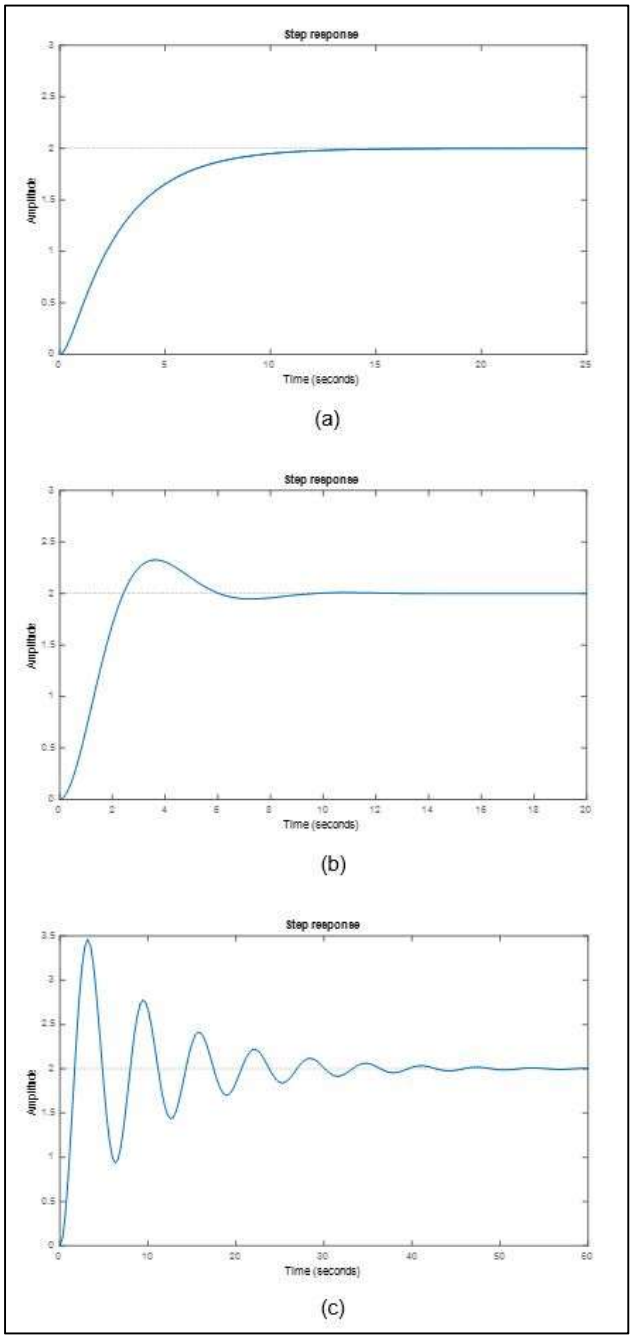

Figure 2.4. Outputs resulting from a step function input for different transfer functions.

The highest value of the output before settling is known as the overshoot of the response. In Figure 2.4 (a), no overshoot is presented, and the system response is stable, though slow. The oscillation before settling in Figure 2.4 (c) calls for instability in the system, and a suitable target response would be the one of Figure 2.4 (b) with only a small overshoot and quick settling time.

An unstable system would show an oscillation with an increasing amplitude, and a system that responses with a constant amplitude oscillation, is called marginally unstable.

2.4 Noise

In an electronic circuit, above the absolute zero temperature (0 K or -273 ˚C), there is always noise present in the form of thermal noise caused by the random movement of the electrons in the material. Thermal noise is part of the internal noise in the circuit, and in addition there is the external noise from outside the circuit. A radio receiver must be able to detect the actual signal in the presence of noise, and since there is not much a designer can do about the external noise, it is important to minimize the internal noise of the circuit. This can be done for example by (Carr 2002, pp. 31-32):

- keeping the source and amplifier input resistances as low as possible
- matching the bandwidth to the frequency response of the signal so that the bandwidth is kept as low as possible
- using grounding, shielding and filtering to minimize the effects of external noise

A low-noise amplifier is usually employed in the input stage of the receiver as a means to improve the signal-to-noise ratio (*SNR*). In addition to *SNR*, the noise factor (F_n) and noise figure (*NF*) describe the noise of a system and are set by the system design to ensure a proper operation of the system. The noise factor of a system is the ratio of the output noise power P_{no} to equivalent input noise power P_{ni} (Carr 2002, p. 29). In terms of equations:

$$F_n = \frac{P_{no}}{P_{ni}}, \tag{2.17}$$

where

$$P_{ni} = A \cdot K \cdot BW \cdot T_0 \tag{2.18}$$

In equation (2.18), K is Boltzmann's constant ($1{,}38 \cdot 10^{-23}$ J/K) and T_0 is room temperature, usually 290 K or 300 K in calculations. To study the noise generated by an individual block, the input noise is the thermal noise P_{tn} of the band,

$$P_{ni} \equiv P_{tn} = K \cdot T_0 \cdot BW, \tag{2.19}$$

which is then normalized to one hertz by dividing equation (2.19) with the bandwidth. The output noise is usually given by the simulator in a noise voltage - frequency plane with the noise voltage unit of $\frac{\mathrm{V}}{\sqrt{\mathrm{Hz}}}$, as in Figure 2.5.

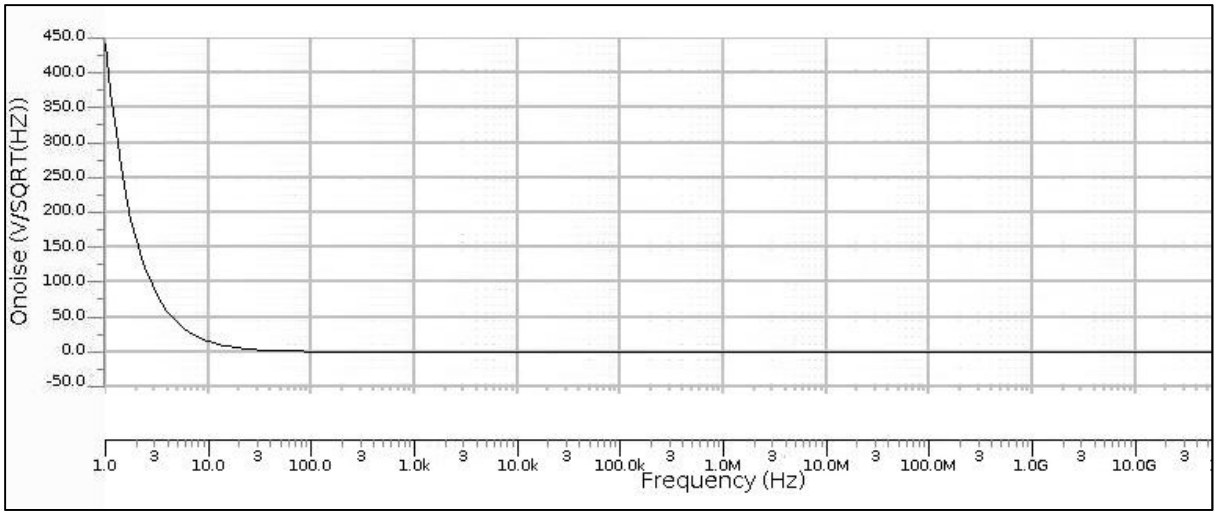

Figure 2.5. An example of an output noise voltage as a function of frequency.

The noise voltage as a function of frequency is not constant but typically increases in the lower frequencies. This is due to flicker noise, also known as the 1/*f* noise. The origin of flicker noise in metal-oxide semiconductor transistors is generally explained to be dominated by number fluctuation noise due to traps in the gate oxide, but also bulk mobility fluctuations' and substrate bias's effect has been suggested (Haartman & Östling 2007).

The noise voltage is obtained by measuring the average value from the curve in Figure 2.5 in the bandwidth of interest. To compare the result with the input noise, the result is divided by the gain of the block to obtain the input-referred noise. After the average input-referred noise voltage V_n is obtained, the resulting noise power is obtained with

$$P_\mathrm{no} \equiv \frac{V_\mathrm{n}^2}{Z}, \tag{2.20}$$

where Z is the impedance level of the amplifier. The noise figure is the noise factor converted to decibels:

$$NF = 10 \cdot \log_{10} F_\mathrm{n} \tag{2.21}$$

The overall noise factor of the receiver constitutes from the noise factor of different stages, and can be calculated with the Friis' noise equation (Carr 2002, p. 31):

$$F_{\mathrm{tot}} = F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 A_2} + \cdots + \frac{F_{\mathrm{N}} - 1}{A_1 A_2 \ldots A_{\mathrm{N}-1}} \tag{2.22}$$

$$NF_{\mathrm{tot}} = 10 \cdot \log_{10} F_{\mathrm{tot}}\,, \tag{2.23}$$

where F_{N} is the noise factor of the *N*th stage and A_{N} is the gain of the *N*th stage, respectively. From equation (2.22), it is clear that if the gains of the first stages of the receiver are sufficiently large, the later stages do not contribute substantially to the noise.

The output signal-to-noise ratio is the signal output power's ratio to the output noise power. Since the noise power is given by the simulator in volts per square root of hertz, the power ratio needs to be divided by the bandwidth:

$$SNR = \frac{P_{\mathrm{out}}}{P_{\mathrm{no}}} \cdot \frac{1}{BW} \tag{2.24}$$

3 LIMITING AMPLIFIER TOPOLOGY CONSIDERATIONS

The limiting amplifier is implemented in an IC with a complementary metal-oxide-semiconductor (CMOS) technology process. While this process offers advantages such as low implementation cost and system integration (Huang, Chien & Lu 2007), the inherent parasitic capacitances of the technology generate challenges in broadband applications. To enhance the bandwidth of a CMOS LA, techniques such as active inductors, negative capacitance and active feedback have been proposed. Different topologies to enhance the *GBW* and to compensate the DC offset of the limiting amplifier are presented in this chapter. In addition to the aforementioned, qualities such as power consumption and the simplicity of a topology are of interest.

3.1 Review on limiting amplifier topologies

Säckinger and Fischer (2000) stated that most of the parasitic capacitance effecting the gain stage is produced by the load. Using an inductive load, this capacitance is partly compensated, and the gain stage's pole is moved to a higher frequency.

The inductive load could be implemented with spiral inductors or active inductors. Using spiral inductors in IC's has a drawback in the large chip area required. In addition, keeping the self-resonance frequency of an on-chip spiral inductor above the passband might prove difficult. Therefore, an active inductor consisting of an n-channel MOS field-effect transistor (MOSFET) and a resistor, as shown in Figure 3.1 (a), is conventionally implemented.

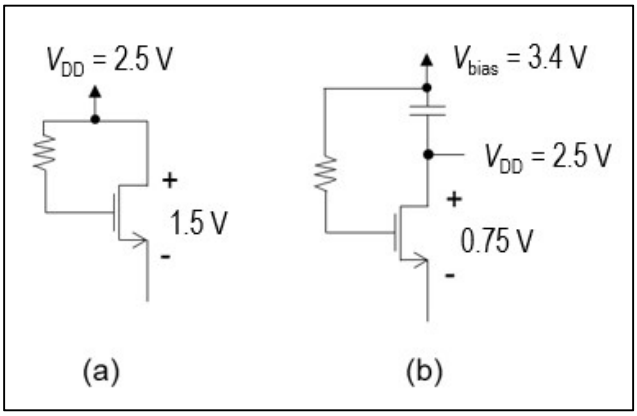

Figure 3.1. A schematic circuit of (a) a conventional active inductor and (b) a novel active inductor topology. (Säckinger & Fischer 2000)

The active inductor topology imposes a problem with low supply voltages (denoted in Figure 3.1 with V_{DD}), since it introduces a large DC voltage drop. In (Säckinger & Fischer 2000), this voltage drop is halved by biasing the active inductor's resistor above the supply voltage with a capacitive voltage converter, as shown in Figure 3.1 (b). With this topology implemented in the 0.25µm CMOS technology, a gain of 32 dB and a bandwidth of 3 GHz are achieved with a 2.5 V supply voltage.

A folded active inductor topology is used to realize a circuit in the 0.25µm technology with only 1 V supply voltage by Wu, Liao and Liu (2000). In (Wu, Liao & Liu 2000) a bandwidth of 1.75 GHz and a voltage gain of 39.9 dB is achieved. The folded active inductor consists of a p-channel and an n-channel MOSFET as shown in Figure 3.2.

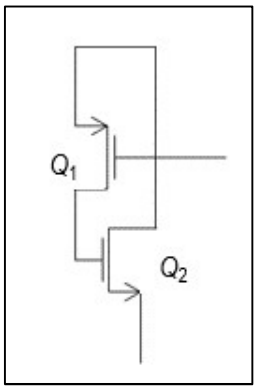

Figure 3.2. A schematic circuit of a folded active inductor topology. (Wu, Liao & Liu 2000)

The p-channel MOSFET Q_1 in this circuit is biased to perform as a resistor. Since no voltage-boosting technique is required, the power consumption is reduced compared to other active inductor LA implementations (Wu, Liao & Liu 2000). Another advantage of the topology is the low chip area required. However, in general, using active inductors increase power consumption and noise, and decrease the linearity of the amplifier.

The inductive loading technique is also integrated by Galal and Razawi (2002), but it is used together with active feedback and negative capacitance. The resulting limiting amplifier topology achieves a gain of 50 dB and a bandwidth of 9.4 GHz, with a 1.8 V supply voltage and 0.18µm CMOS technology. The schematic circuit of the gain stage is shown in Figure 3.3.

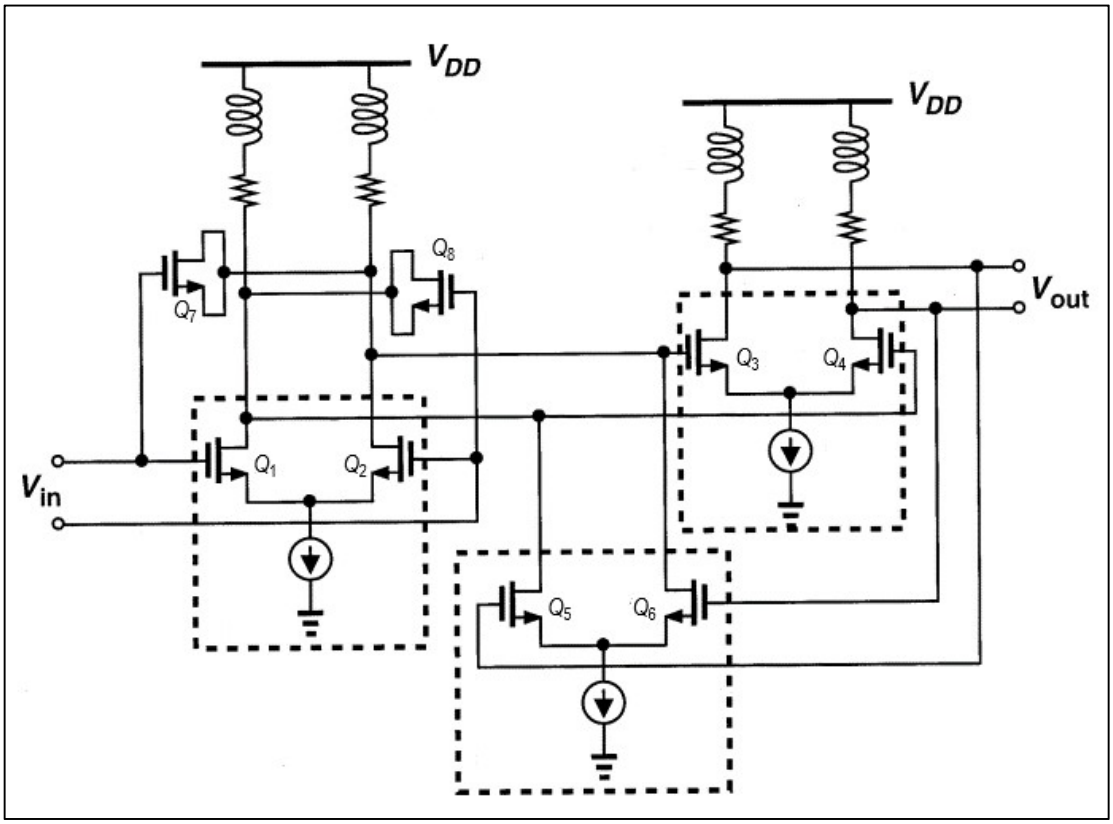

Figure 3.3. A schematic circuit of a gain stage implementing active inductors, negative capacitance and active feedback as means to improve the bandwidth. (Galal & Razawi 2002)

The amplifier core is realized with differential common-source amplifiers (transistors Q_1 to Q_4). Transistors Q_5 and Q_6 provide the active feedback whereas Q_7 and Q_8 decrease the Miller capacitance of the circuit. According to Galal and Razawi (2002), the active feedback's advantage over conventional solutions, such as the Cherry-Hooper amplifier presented in 1963 (Cherry & Hooper 1963), is that it does not resistively load the gain stage. It is also shown by Galal and Razawi (2002), that the active feedback topology increases the *GBW* beyond the unity-gain frequency f_T of the process technology. The unity-gain frequency is the maximum frequency at which the amplitude of the output small-signal current exceeds the amplitude of the input small-signal current (Carusone, Johns & Martin 2012, p. 38).

An inductorless broadband limiting amplifier is implemented by Huang, Chien and Lu (2007) in the 0.18µm process by using third-order active feedback gain stages. It is concluded that by increasing the feedback factor of the active feedback, the bandwidth of the gain stage is enhanced but also the gain peaking is increased. While some gain peaking in the limiting amplifier is

welcomed, it should be kept moderate. Figure 3.4 shows ideal amplitude responses for the limiting amplifier and for the receiver's input stage (the LNA), with the latter converted to baseband frequencies.

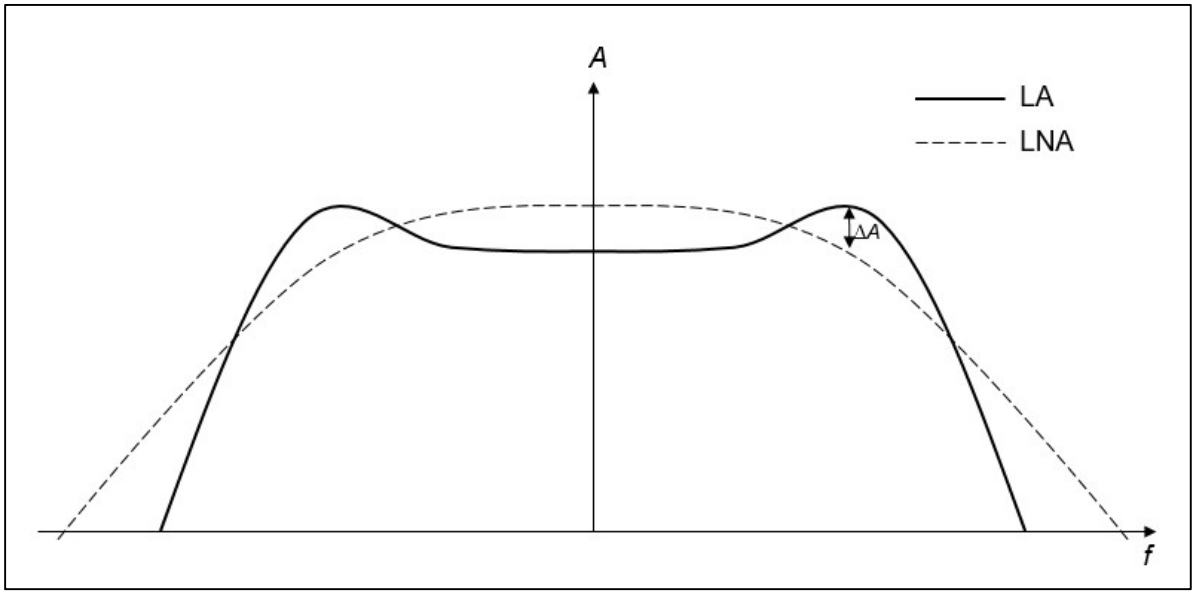

Figure 3.4. An ideal frequency response for an LA and LNA in the complex-frequency plane. The LNA's amplitude response is converted to baseband frequencies.

Ideally, if a gain peaking (ΔA) of 3 dB is introduced at the same frequency as the LNA's cutoff frequency, the total gain response would be flat. Hence, the gain peaking of the limiting amplifier should be kept at a few decibels at maximum. A higher peaking easily produces instability issues in the amplifier and is seen in the time domain as significant overshoot and possible oscillation.

To achieve a bandwidth in the gigahertz range, multiple third-order gain stages need to be cascaded, which would further increase the gain peaking. Huang. Chien and Lu (2007) proposed and interleaving feedback topology, presented in Figure 3.5, as a solution.

The purpose of the interleaving feedback is to obtain a non-uniform architecture, which causes the poles of the third-order gain stages to deviate from their original locations. Along with the poles, also the gain peaking deviates and the overall gain becomes flatter. Figure 3.6 shows this effect simulated with the topology of Figure 3.5.

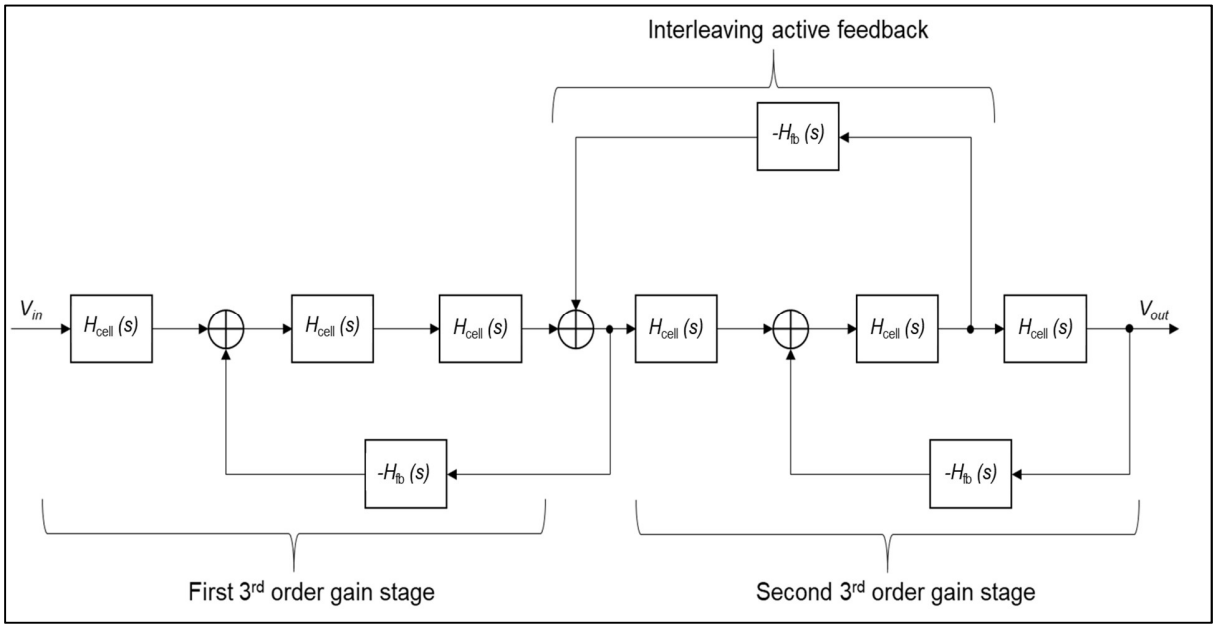

Figure 3.5. A proposed third-order interleaving feedback topology for a limiting amplifier. (Huang, Chien & Lu 2007)

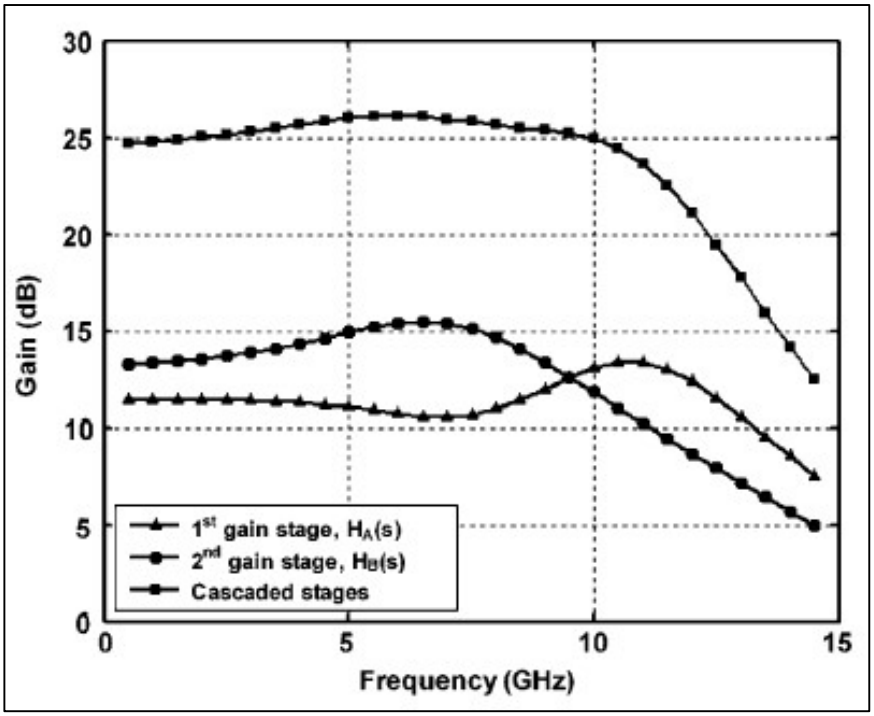

Figure 3.6. The resulting frequency responses for the individual gain stages and the cascaded stages of Figure 3.5. (Huang, Chien & Lu 2007)

The limiting amplifier implemented by Huang, Chien and Lu (2007) obtains a voltage gain of 42 dB with a bandwidth of 9 GHz. This topology is used successfully by Lee et al. (2016) in an OOK receiver with a 20 Gb/s data rate and a power consumption of only 46 mW.

All the wideband limiting amplifier solutions presented here use the MOSFET differential common-source (CS) configuration in their amplifier core, and based on this, the differential CS is selected to be used in the amplifier core of the design described in this thesis.

3.2 Review on DC offset cancellation topologies

An undesirable DC offset voltage can be produced in the signal by the preceding stages and a mismatch between the components in the amplifier itself. In practical MOSFET IC differential pair configurations, there is mismatch in load resistances, in MOSFETs' width-to-length ratio *W/L* and in threshold voltages. If this offset voltage makes its way through the amplifier, it is naturally also amplified along with the actual desired signal. This can lead to reduced peak signal level, weaker sensitivity, pulse width distortion (Galal & Razawi 2002) and saturation of the output signal. In Figure 3.7 (a), the vertical shift of the signal (ideally, dashed line) reduces the peak signal level, leading to a weaker sensitivity. In Figure 3.7 (b), the ideal pulse ratio would be 50 %, but the offset distorts the pulse width.

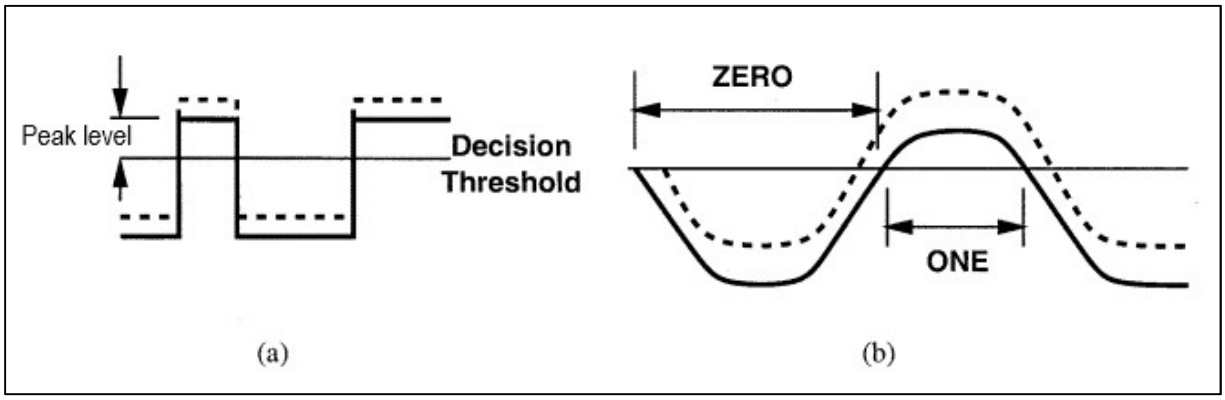

Figure 3.7. A signal with DC offset (solid line) compared to ideal signal (dashed line), leading to (a) sensitivity degradation and (b) pulse-width distortion. (Galal & Razawi 2002)

To avoid the offset voltage at the output of the limiting amplifier, a DC offset cancellation circuit is implemented in the design. An offset cancellation circuit implemented in a feedforward path is presented in Figure 3.8.

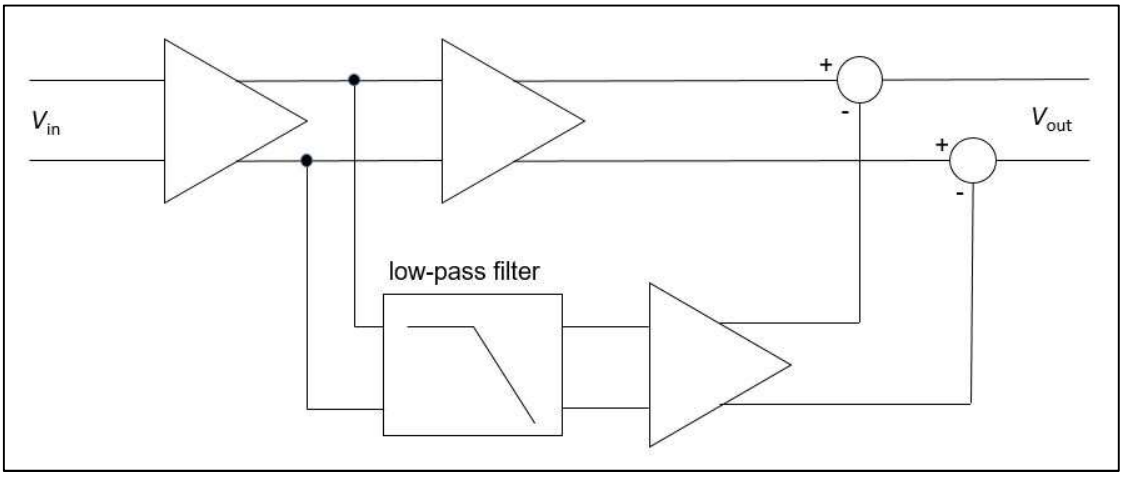

Figure 3.8. A block diagram of a topology of a feedforward DC offset cancellation technique. (Pham et al. 2009)

This topology was studied by Pham et al. (2009). Pham et al. concluded that the advantages of the feedforward topology are small passive components needed to achieve the required lower cut-off frequency and avoiding the potential stability issue caused by the feedback path. When using a feedforward technique, the corner frequency $f_{L,ff}$ of the low-pass filter is obtained from

$$f_{\mathrm{L,ff}} = \frac{1}{2 \cdot \pi \cdot R \cdot C} \tag{3.1}$$

where *R* and *C* are the resistance and capacitance of the low-pass filter.

It was proposed by Pham et al. (2009) that the passive components in the filter could be replaced with MOSFETs. To replace the filter resistor, a p-channel MOSFET could be used. For the capacitor replacement, an n-channel MOSFET with its drain and source connected (a topology known as the diode-connected transistor) is applicable. Using transistors to replace the passive components has the advantage of reducing the chip area significantly. However, employing MOSFETs in this manner can be highly inaccurate and the effective resistance and capacitance values of the circuit can easily vary along with conditions such as temperature.

Although even with passive components, the feedforward technique would require smaller chip area, it still has a significant disadvantage when compared to the feedback technique; the feedforward control cannot react to changes in the behaviour of the amplifier itself, or changes in the load. An offset cancellation circuit implemented in a feedback loop is presented in (Galal & Razawi 2002) and (Huang, Chien & Lu 2007). In the topology by Galal and Razawi

(2002), the offset cancellation network consists of a low-pass filter and a feedback amplifier. This topology is presented in Figure 3.9.

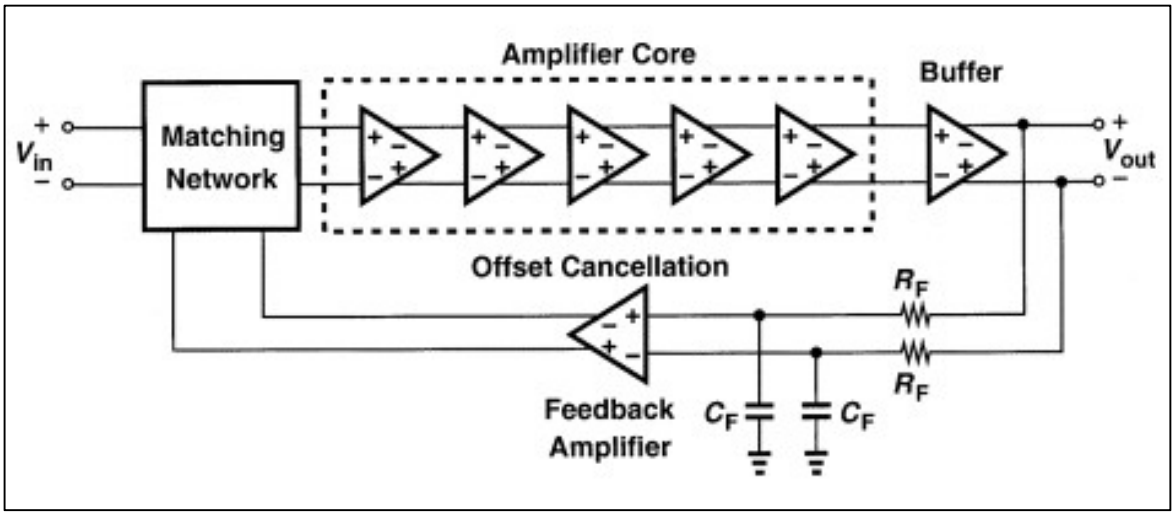

Figure 3.9. An amplifier topology with an offset cancellation circuit consisting of a low-pass filter implemented with passive components R_F and C_F, and a feedback amplifier. (Galal & Razawi 2002)

When determining the corner frequency of the low-pass filter in a feedback loop, the effect of the feedback gain A_{fb} of the feedback amplifier needs to be considered (Huang, Chien & Lu 2007):

$$f_{\mathrm{L,fb}} = \frac{A_{\mathrm{M}} \cdot A_{\mathrm{fb}} + 1}{2 \cdot \pi \cdot R_{\mathrm{F}} \cdot C_{\mathrm{F}}}, \tag{3.2}$$

where R_F and C_F are the resistance and capacitance of the low-pass filter in the feedback path, as shown in Figure 3.9.

Comparing equations (3.1) and (3.2) shows that to obtain an equally low corner frequency for the filter, the feedback topology requires larger resistance and capacitance values than the feedforward topology.

The corner frequency of the filters should be set at few tens of megahertz to satisfy the requirements for signal droop and settling time. This frequency range gives a good tolerance when considering possible layout-introduced parasitic components and hence the variation of the corner frequency in the final design. The lower the corner frequency is, the longer is the settling time of the signal. However, a high corner frequency produces a droop, also known as the baseline wanderer, shown in the time domain after long runs. Figure 3.10 shows the effect of a low corner frequency to the settling time (a) and a high corner frequency to the signal droop (b).

An *SNR* of about 20 dB and a bit error-rate (BER) close to zero with a 10 MHz f_L was simulated in the system design phase, hence the settling time would still be short enough. On the other hand, should the corner frequency increase up to 100-200 MHz, the signal droop would still be sufficiently small.

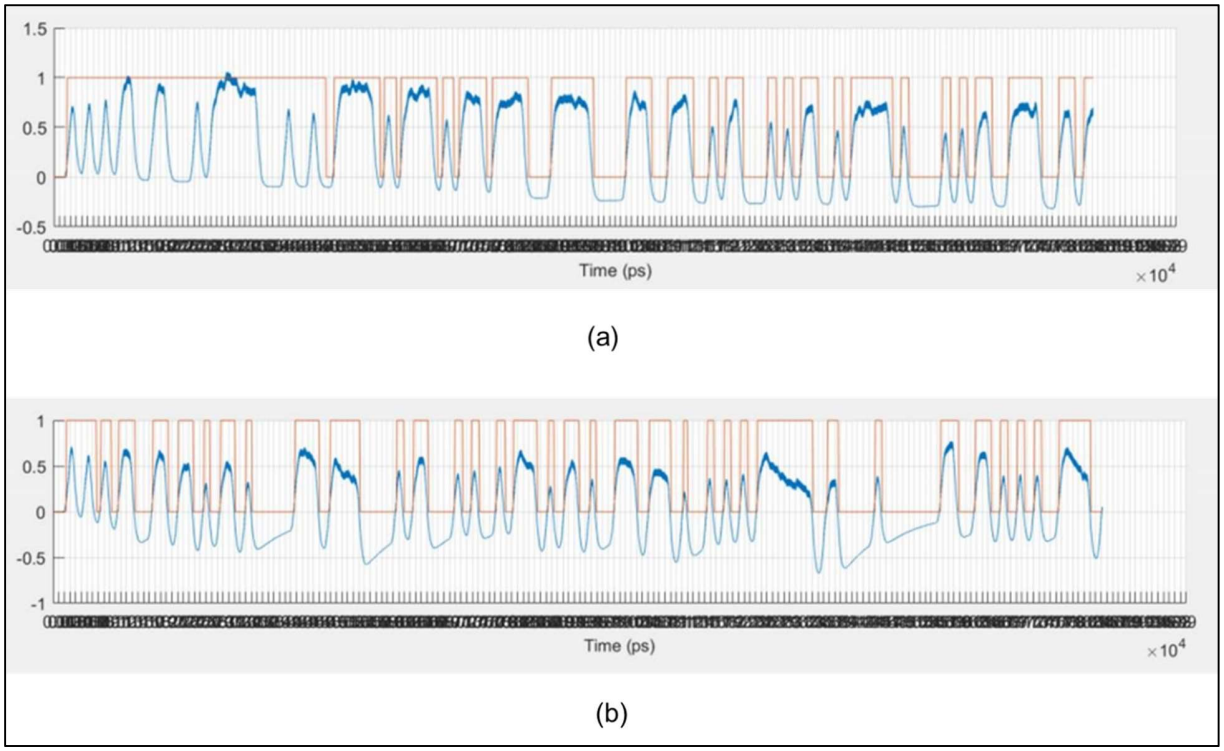

Figure 3.10. The effect of the lower corner frequency of the limiting amplifier to the signal settling time and droop. Orange plot is the data read from the signal (blue plot). Figure (a) shows the slow settling time of the signal with f_L = 10 MHz. Figure (b) shows the signal droop with f_L = 200 MHz.

3.3 Choosing the topology of this work

To achieve a required gain-bandwidth product for the limiting amplifier, the active feedback as the bandwidth enhancement technique is studied in more detail. According to Huang, Chien and Lu (2007), using similar gain stages in cascade results in a total bandwidth of

$$BW_{\text{tot}} = BW_{\text{cell}} \cdot \sqrt{\sqrt[n]{2} - 1}^{2 \cdot m}, \tag{3.3}$$

where *n* is the number of gain stages and *m* is the order of one gain stage. From this, the required *GBW* of a gain cell, GBW_{cell}, can be derived as (Huang, Chien & Lu 2007)

$$GBW_{\text{cell}} = \frac{BW_{\text{tot}}}{\sqrt[2m]{\sqrt[n]{2}-1}} \cdot \sqrt[n]{A_{\text{M}}}, \tag{3.4}$$

where A_{M} is the required total midband gain. The required gain from the amplifier is 30 dB with a 10 GHz upper 3-dB frequency. Figure 3.11 shows the required GBW_{cell} as a function of n for m = 1, 2 or 3, respectively.

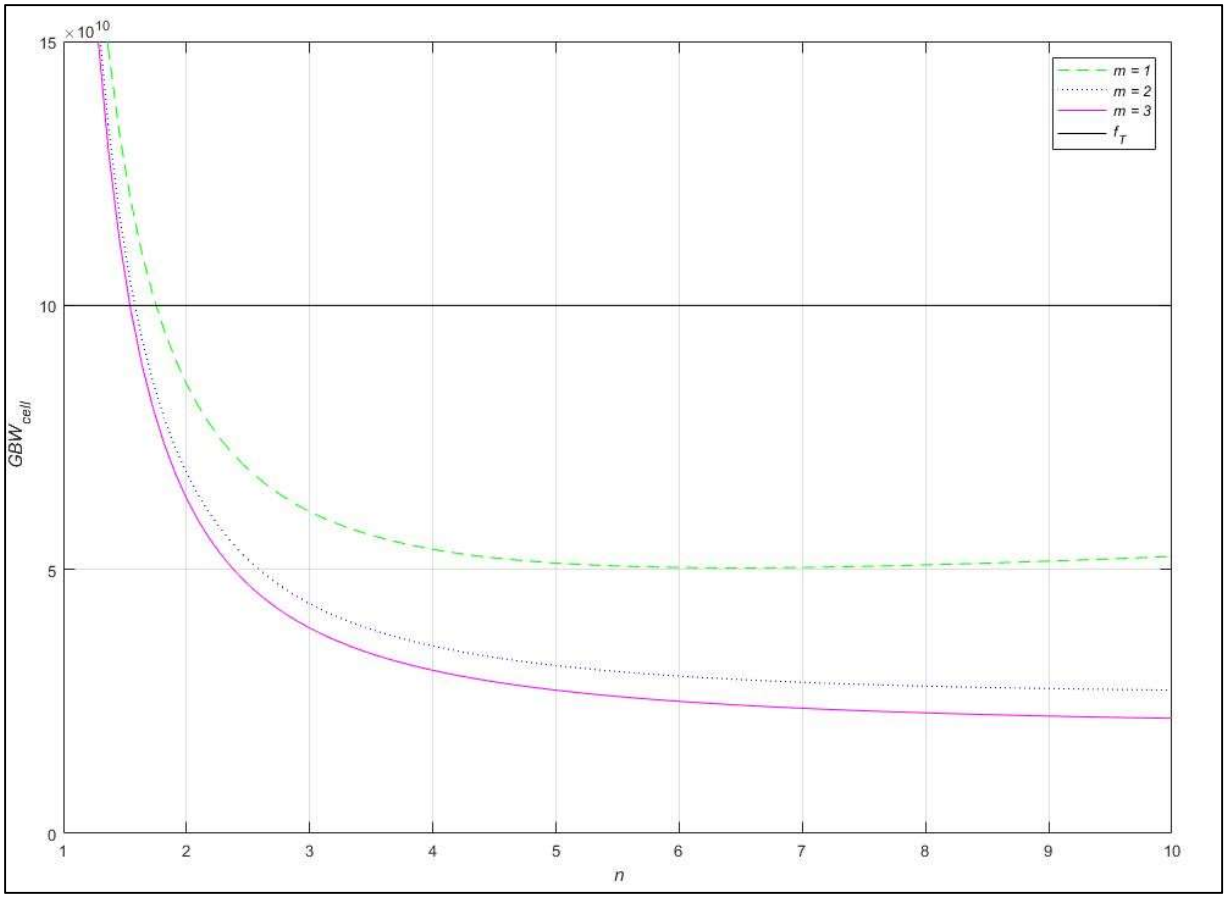

Figure 3.11. The required cell gain-bandwidth product (GBW_{cell}) as a function of number of stages (n) with different stage orders (m). The black line represents the unity-gain frequency f_{T}.

The unity-gain frequency in the process used is estimated to be around 100 GHz, hence a cell with 10 dB gain could theoretically reach a 3-dB bandwidth of

$$BW_{10\text{dB}} = \frac{100\ \text{GHz}}{10^{\frac{10}{20}}} \approx 30\ \text{GHz} \tag{3.5}$$

As shown in Figure 3.11, the more there are gain stages cascaded, the less is required for the cell *GBW*. However, the number of gain stages is delimited by the power consumption and noise requirements of the limiting amplifier (Huang, Chien & Lu 2007). Figure 3.11 also shows that the implementation with one gain stage would be impossible due to the unity-gain frequency limitation. The achieved benefit from adding gain stages tends to diminish rapidly after *n* reaches 3-4, hence the reasonable number of stages would be less than or equal to 3. Based on the results of Figure 3.11, an implementation with two cascaded third-order gain stages is studied in more detail.

According to Galal and Razawi (2002), a better *GBW* for the amplifier can be achieved by implementing active feedback. The bandwidth improvement, compared to passive feedback, is studied in more detail by modelling both topologies with circuits shown in Figure 3.12. In Figure 3.12, the transfer function of the gain stage, A_v, is the same for both circuits. Figure 3.12 (a) is the circuit for the active feedback, and Figure 3.12 (b) for passive feedback, respectively. In figure (a), g_{m1} and g_{mfb} are voltage-controlled current sources (VCCS).

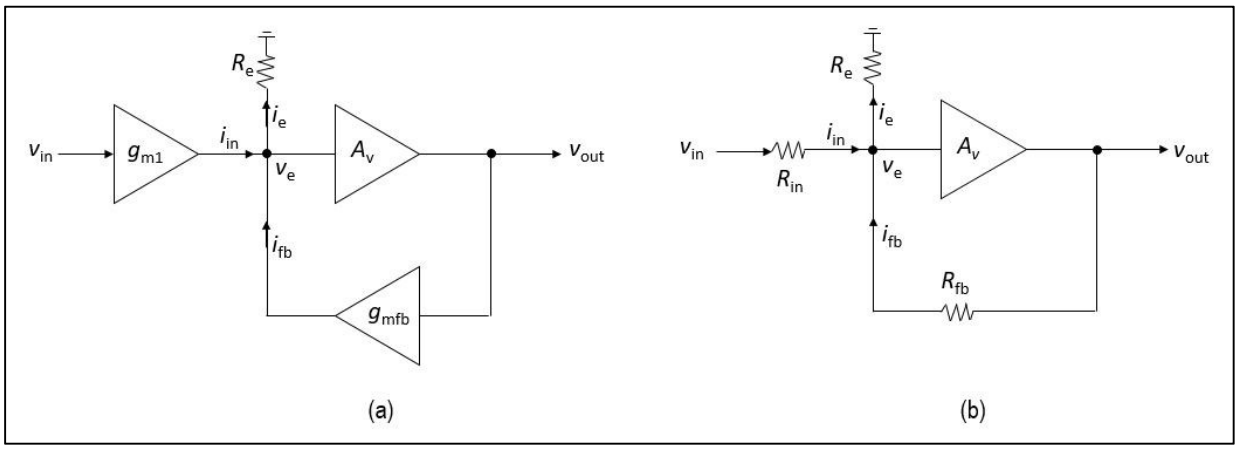

Figure 3.12. Circuits to derive the transfer functions v_{in}/v_{out} for (a) active feedback with voltage-controlled current sources g_{m1} and g_{mfb} and (b) passive feedback with input resistance R_{in} and feedback resistance R_f.

A detailed derivation of transfer functions for circuits in Figure 3.12 is presented in Appendix 1. By choosing the circuit values so that the low-frequency gain is the same for both topologies, the simulation result of Figure 3.13 shows clearly a wider bandwidth with the active feedback. For the passive feedback, the 3-dB frequency is 2.7 GHz while for the active feedback, it is 8.2 GHz.

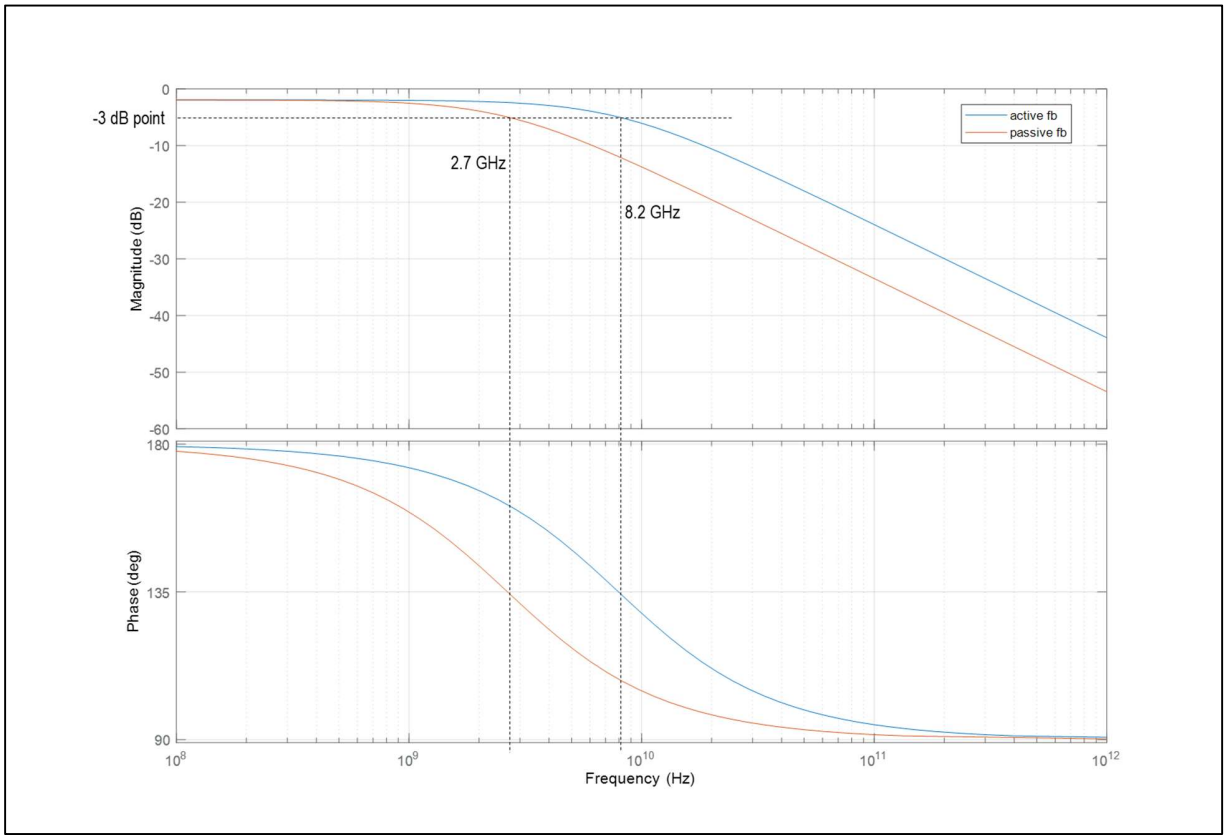

Figure 3.13. A comparison of the frequency responses of circuits in Figure 3.12. Blue line is the frequency response of the active feedback circuit and orange line is the response of the passive feedback circuit.

A critical node in the feedback topology is the node v_e shown in Figure 3.12. For both topologies, the amplitude of this node starts to increase at some frequency as shown in Figure 3.14. When the amplitude of the gain stage A_v starts to decrease, this increase in v_e keeps the total response v_{out}/v_{in} still flat. However, as seen in Figure 3.14, the increase is significantly higher in amplitude and faster for the active feedback.

The phenomenon described above is mainly because the input current i_{in} for the passive feedback is directly proportional to the subtraction of v_{in} and v_e. Hence, while v_e increases, i_{in} decreases. For the active feedback, the input current depends only on the input voltage and the multiplier g_{m1} of the VCCS in the input. Based on this comparison of the active and passive feedback, the active feedback topology is chosen to be used in the limiting amplifier.

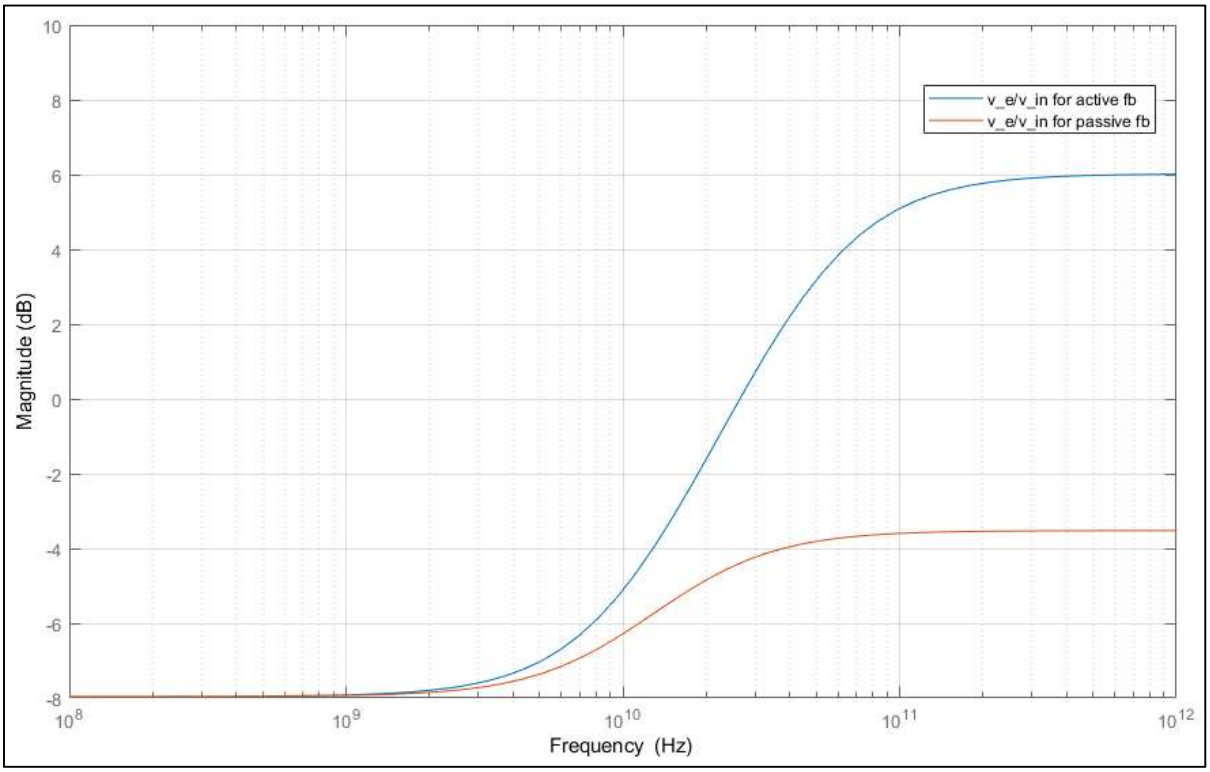

Figure 3.14. The amplitude response of v_e/v_{in} as a function of frequency.

Next, a suitable value for the feedback factor needs to be resolved. In (Huang, Chien & Lu 2007), the negative effects of increasing β (reduced gain and increased gain peaking) were minimized by adding an interleaving feedback to make the amplifier architecture non-uniform. In this work, the architecture non-uniformity is realized with differences between the gain stages rather than varying β or adding more feedback loops. This solution is chosen for simplicity and to avoid the possibly occurring stability issues caused by the additional feedback. A block diagram of a third-order gain stage is shown in Figure 3.15. In Figure 3.15, H_{cell} represents the transfer function of a gain cell and H_{fb} the transfer function of the feedback path.

By implementing three similar gain cells and noting their low-frequency gain with A_0, the closed-loop low-frequency gain A_{cl0} of the gain stage in Figure 3.15 can be derived from equation (2.10):

$$A_{\mathrm{cl0}} = A_0 \cdot \frac{A_0^2}{1 + A_0^2 \cdot \beta} = \frac{A_0^3}{1 + A_0^2 \cdot \beta} \tag{3.6}$$

To investigate the effect of the feedback factor to the 3-dB frequency of the gain stage, a numerical method was used by Huang, Chien and Lu (2007).

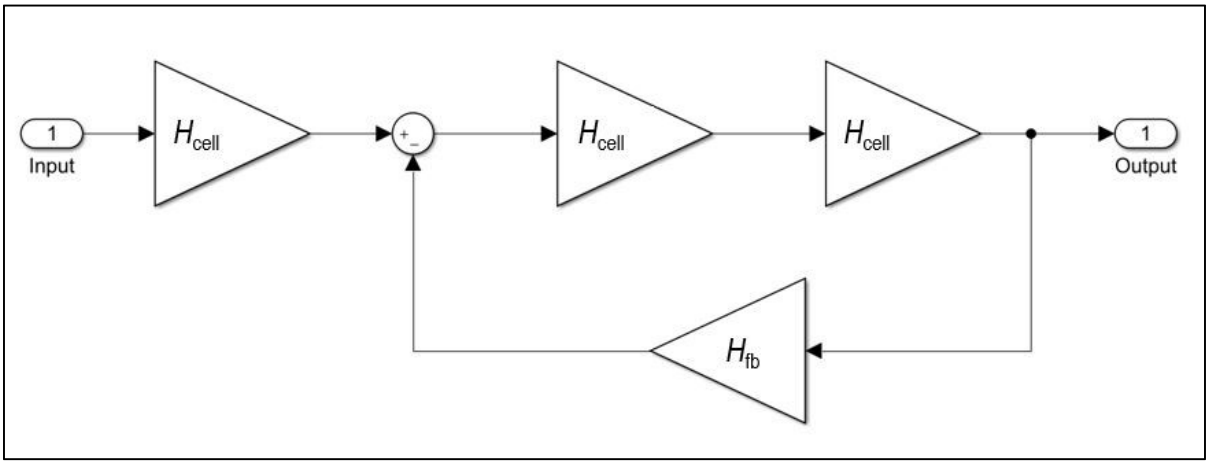

Figure 3.15. A block diagram of a third order gain stage. H_{cell} represents the transfer function of a gain cell and H_{fb} the transfer function of the feedback path.

The cut-off frequency $f_{3\text{-dB}}$ is solved with different values of β from

$$\frac{A_0^3}{\sqrt{\left[1 + A_0^2\beta - 3 \cdot \left(\frac{f_{3-\mathrm{dB}}}{f_0}\right)^2\right]^2 + \left[3 \cdot \left(\frac{f_{3-\mathrm{dB}}}{f_0}\right) - \left(\frac{f_{3-\mathrm{dB}}}{f_0}\right)^3\right]^2}} = \frac{A_{\mathrm{f0}}}{\sqrt{2}}, \tag{3.7}$$

where f_0 is the 3-dB frequency of one gain cell. Figure 3.16 shows the results for varying β with 10 dB, 30 GHz gain cells.

The initial value for the feedback factor is chosen from the intersection of these two plots, hence β = 0.3. The same feedback factor will be used for both gain stages, and the non-uniformity is realized by implementing the first gain stage with 10 dB gain cells and the second stage with 5 dB cells. In addition to these gain stages, a cell with a 5-dB gain is added in the input of the amplifier. This cell produces a low input capacitance to the limiting amplifier, which eases the matching with the preceding mixer, and thus improves the obtained bandwidth.

A gain cell can be modelled with a single-pole transfer function, hence by using equations (2.2) and (2.4), we obtain the transfer function of a gain cell:

$$H_{\mathrm{cell}} = A_0 \cdot \frac{1}{1 + \frac{s}{\omega_0}}, \tag{3.8}$$

where ω_0 is the 3-dB angular frequency of a gain cell.

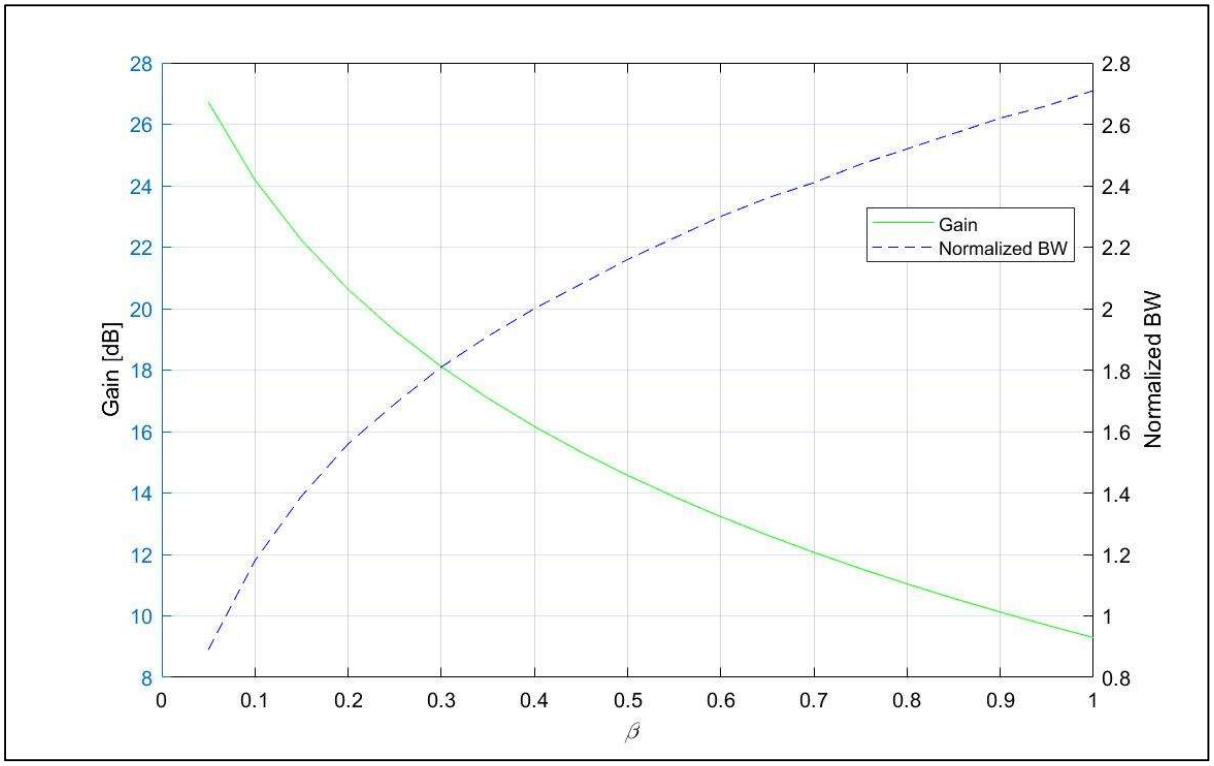

Figure 3.16. The low-frequency gain and normalized bandwidth as a function of the feedback factor β.

For the feedback cell, the transfer function is similar with A_0 replaced by the feedback factor and ω_0 defined by the output resistance of the first gain cell in the gain stage, and the input capacitance of the second gain cell. Hence, ω_0 of the feedback cell will be in the same range as ω_0 of the gain cells. The transfer function of a third-order gain stage shown in Figure 3.15 is

$$H = \frac{H_{\text{cell1}} H_{\text{cell2}} H_{\text{cell3}}}{1 + H_{\text{fb}} H_{\text{cell2}} H_{\text{cell3}}} \tag{3.9}$$

In the initial simulations, the input 5 dB gain cell is excluded and only the frequency response of the third-order stages is studied. Hence the targeted low-frequency gain is in the range of 25 dB. The estimated cut-off frequencies for the 5 dB gain cells is 56 GHz and for the feedback cells 30 GHz, respectively. Figure 3.17 shows the amplitude response of the first simulation.

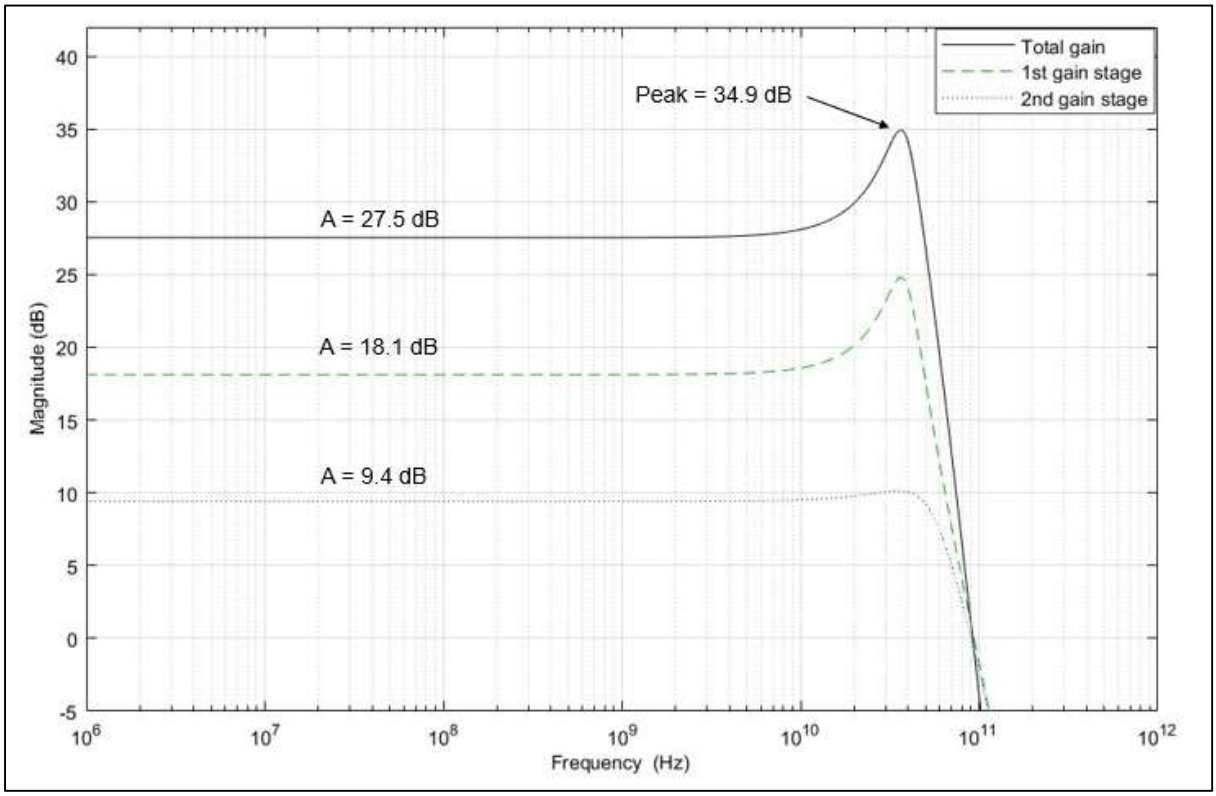

Figure 3.17. The amplitude response as a function of frequency for the first and second gain stages and the total gain for the initial simulation of the circuit.

The gain peaking of the total gain is very large, over 7 dB. The peaking frequencies of the first and second gain stages are very near each other. The peaking frequency is at about 36 GHz and the 3-dB frequency of the total gain is at 53 GHz. Although there is a fair margin to the targeted bandwidth of 10 GHz, it should be noted that this result is based on a somewhat intuitive estimate of a cell bandwidth. If the bandwidth of a 10 dB gain cell is only 15 GHz instead of the estimated 30 GHz, the 3-dB frequency of the total response falls under 30 GHz. The inherent parasitic capacitances that decrease the upper 3-dB frequency are difficult to predict, hence at this point of the design a margin this large is profitable.

The first simulation result shows that there is some headroom in the total low-frequency gain, and the non-uniformity of the gain stages should be increased to reduce the gain peaking. The first gain stage is modified to include one 10 dB cell together with two 8 dB cells. In addition, the last gain cell of the core is changed to a 0 dB cell. This will decrease the output impedance of the limiting amplifier and enables a better matching with the following stage, the output buffer. To

maintain the gain of the second gain stage at about 10 dB, the first gain cell is replaced with a 10 dB cell. Table 1.1 presents the values used in the second simulation.

Table 1.1. The values used in the second simulation of the gain stages.

	A_0	f_0
H_{0dB}	1	100 GHz
H_{5dB}	1,8	56 GHz
H_{8dB}	2,5	40 GHz
H_{10dB}	3,2	30 GHz

The block diagram for the second simulation is shown in Figure 3.18.

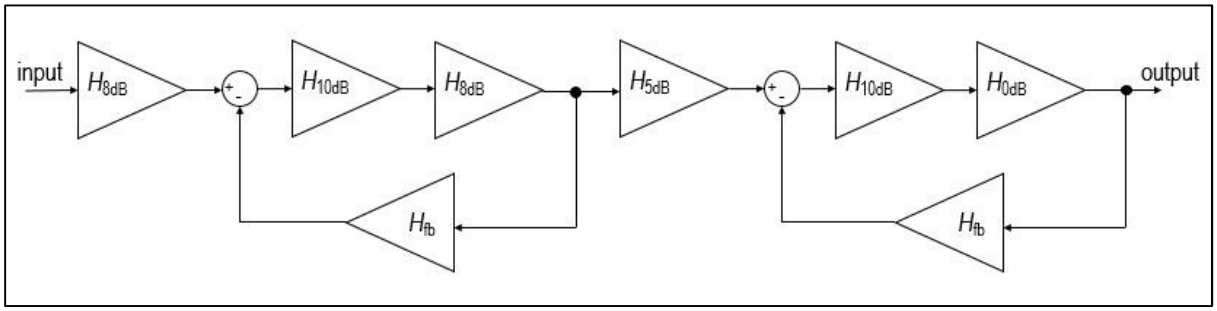

Figure 3.18. A block diagram of the circuit used in the second simulation.

The results of the second simulation in Figure 3.19 show that the low-frequency gain is decreased to 24.8 dB with gain peaking of only about 4 dB.

The peaking frequency is 39 GHz and the 3-dB frequency is at 53.9 GHz. By adding the 5 dB gain cell with a cut-off frequency of 56 GHz at the input, the total low-frequency gain is 29.9 dB and the 3-dB frequency 50 GHz, with a gain peaking of only 2.5 dB. This result is satisfactory compared to the targets, hence the described topology will be used for the amplifier.

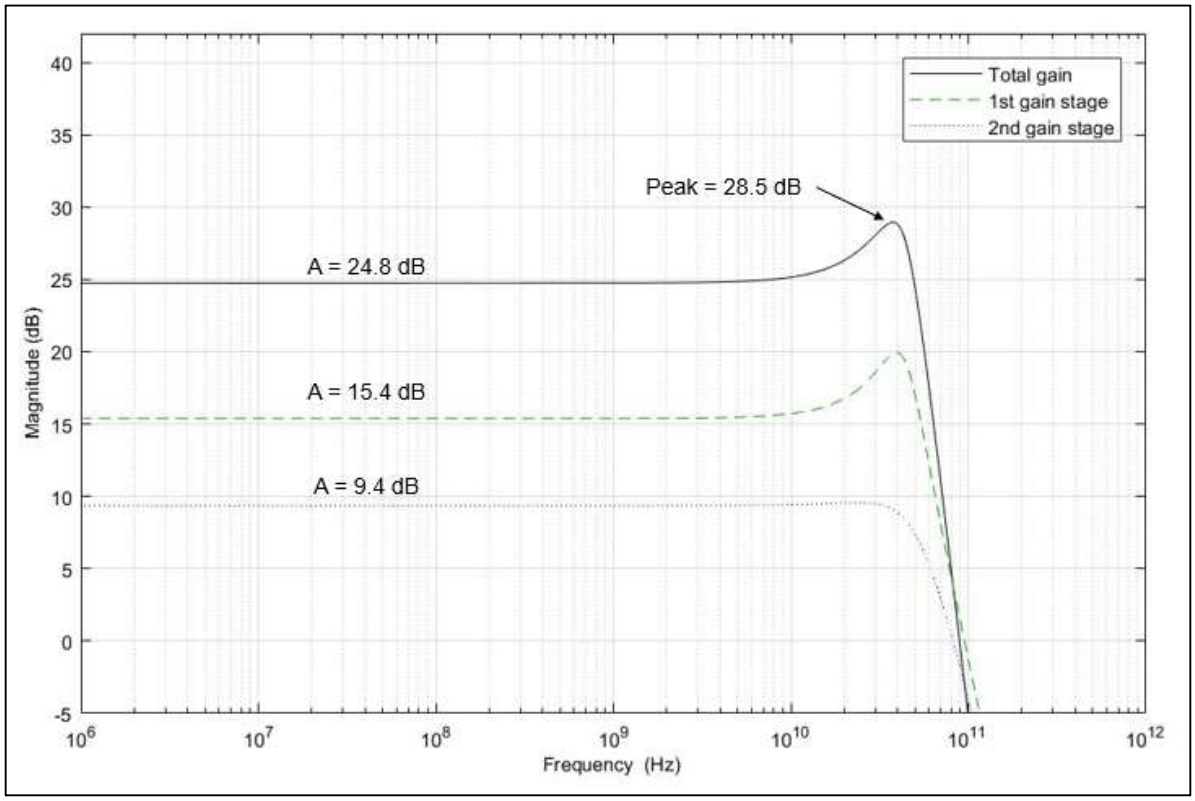

Figure 3.19. The amplitude response as a function of frequency for the first and second gain stages and the total gain for the second simulation of the circuit.

Next, the input filter's and the DC offset cancellation circuit's transfer functions are added to the model. The feedback topology is chosen for this design to achieve a circuit that can react to changes in the amplifier core or load. In addition to the offset cancellation circuit in the feedback path, a high-pass filter is implemented at the input of the limiting amplifier, as a means to filter out the DC from the input signal.

As mentioned earlier, the lower 3-dB frequency of the amplifier should be at few tens of megahertz. A cut-off frequency of 30 MHz is chosen to be used in the model. The input filter will have a gain of 0 dB, and the transfer function of the high-pass filter (HPF) is

$$H_{\mathrm{HPF}} = \frac{s}{s + \omega_{\mathrm{c}}} = \frac{s}{s + 2 \cdot \pi \cdot 30\ \mathrm{MHz}} \tag{3.10}$$

As described in chapter 3.2, in the dimensioning of the low-pass filter implemented in the feedback path, one needs to consider the effect of the feedback factor. The low-pass filter's cut-off frequency needs to be designed lower than would be the case without the feedback gain. Here,

the feedback factor is set to double compared to the β of the gain stages, hence $\beta_{\mathrm{dcoff}} = 0.6$. With this value, the cut-off frequency of the low-pass filter should be about a decade lower than for the high-pass filter, hence a default value of 3 MHz is used. The transfer function of the low-pass filter (LPF) is

$$H_{\mathrm{LPF}} = \frac{1}{1 + \frac{s}{\omega_{\mathrm{c}}}} = \frac{1}{1 + \frac{s}{2 \cdot \pi \cdot 3\ \mathrm{MHz}}} \tag{3.11}$$

The offset cancellation circuit will be connected between the input gain cell and the first gain stage. It is estimated that the upper cut-off frequency for the DC offset feedback cell is the same as for the input gain cell, 56 GHz.

With the offset cancellation added, the amplifier topology is as follows: the input stage consists of the high-pass filter and the 5 dB gain cell, the amplifier core contains the two non-uniform gain stages and the DC offset cancellation circuit consists of the low-pass filter together with the feedback gain. The block diagram of the limiting amplifier is shown in Figure 3.20.

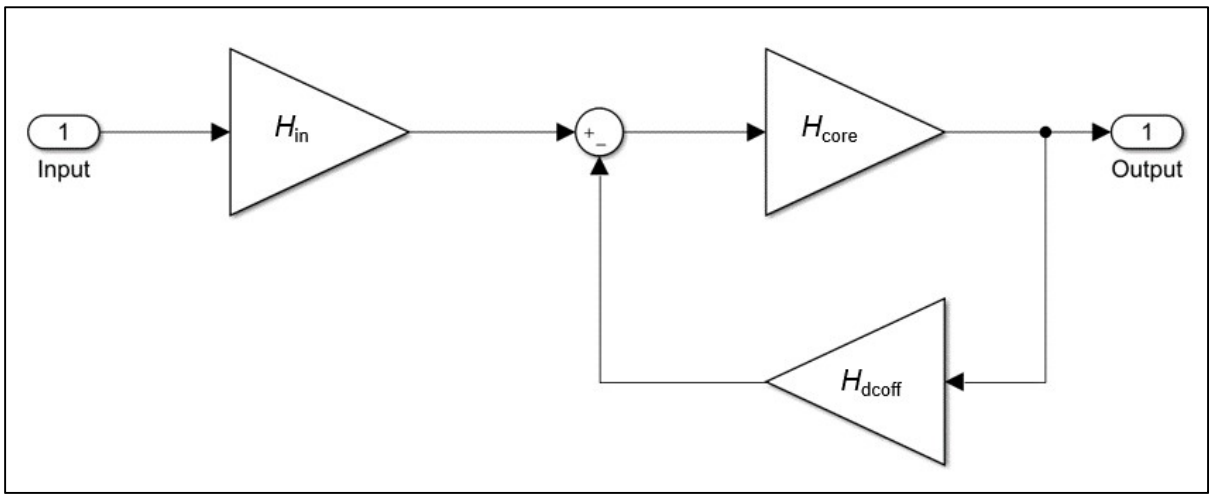

Figure 3.20. A block diagram of the limiting amplifier with the input stage H_{in} consisting of the high-pass filter and a gain cell, H_{core} consisting of the two non-homogenous gain stages and H_{dcoff} consisting of the low-pass filter and a feedback cell.

In Figure 3.20, H_{in} is the transfer function of the input stage, H_{core} the transfer function of the amplifier core and H_{dcoff} the transfer function of the DC offset cancellation circuit. The transfer function of the amplifier is

$$H_{\text{tot}} = \frac{H_{\text{in}}}{\frac{1}{H_{\text{core}}} + H_{\text{dcoff}}} \tag{3.12}$$

Figure 3.21 shows the amplitude response for the limiting amplifier.

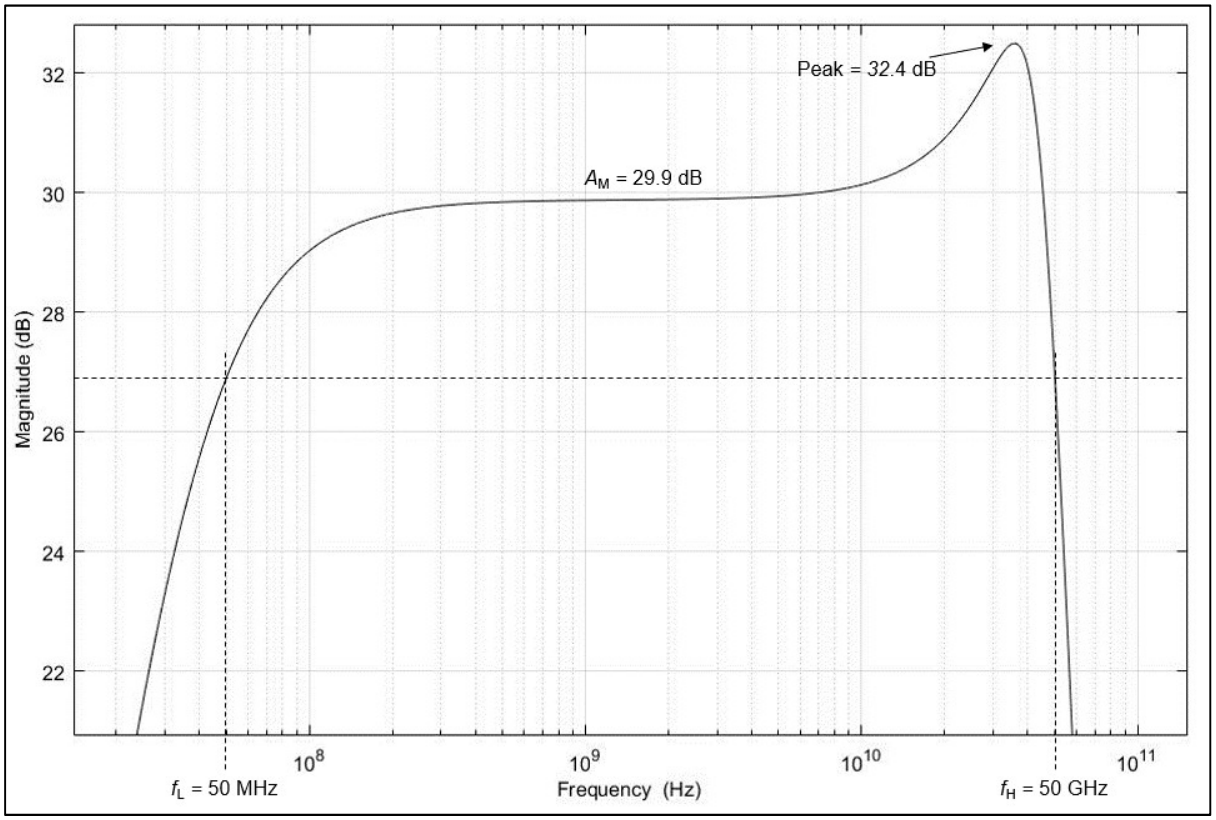

Figure 3.21. The amplitude response as a function of frequency for the circuit of Figure 3.20.

Adding the HPF and the offset cancellation circuit only affected the low-frequency response, as expected. The lower 3-dB frequency is at 50 MHz, which falls in the targeted range. Table 2.2 lists the essential values obtained from the limiting amplifier model. Taking account that the upper cut-off frequency might fall radically in the implementation of the amplifier, the results indicate that the simulated topology works well for the design.

Table 2.2. The values obtained from the modelling of the limiting amplifier.

Quantity	**Obtained value**
A_M	29.9 dB
Gain peaking	2.6 dB
Peaking frequency	35.9 GHz
f_L	50 MHz
f_H	50 GHz

4 IMPLEMENTATION OF THE AMPLIFIER

The limiting amplifier topology is presented in Figure 4.1. It consists of a HPF at the input, the input gain stage and the amplifier core to provide the actual gain of the amplifier, and a DC offset cancellation network consisting of a LPF and a feedback gain cell.

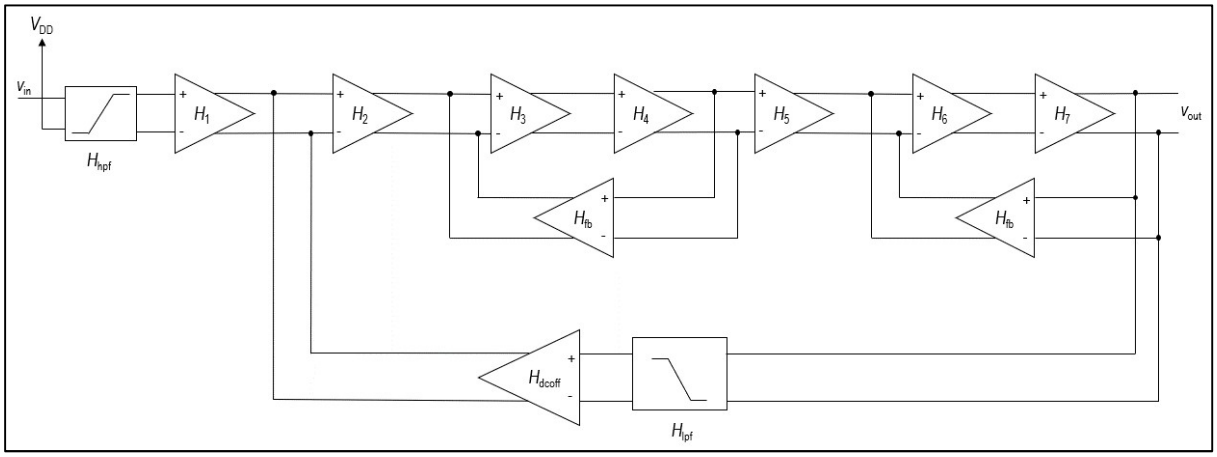

Figure 4.1. A block diagram of the limiting amplifier topology, based on the circuit of Figure 3.20.

In chapter 3.3, the limiting amplifier was modelled as single-ended, but the actual implementation will be double-ended. This chapter goes through the theory and implementation techniques related to the design of different building blocks of the amplifier: the common-source amplifier, the feedback cell, the high-pass and low-pass filters and the biasing of the blocks. The layout implementation and its effects on the functionality of the amplifier are also presented.

4.1 The common-source amplifier

The common-source amplifier is used as the basic building block in the baseband amplifier. Figure 4.2 shows the basic circuit of the CS amplifier. In Figure 4.2, the drain resistance is referred to as R_D and the supply voltage is noted V_{DD}.

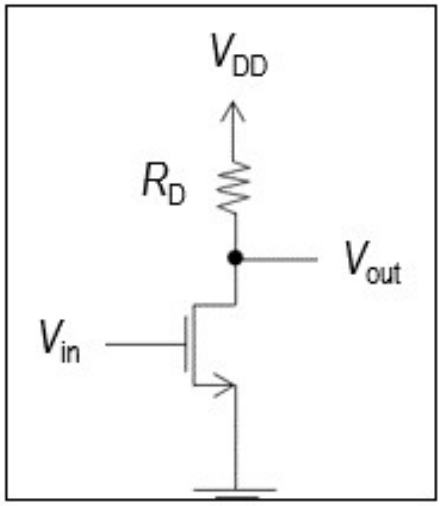

Figure 4.2. The schematic circuit of a common-source amplifier. V_{in} is the input voltage, V_{out} is the output voltage, R_D is the drain resistance and V_{DD} is the operating voltage.

The input signal is fed to the gate of the transistor, and output signal is taken from the drain, hence the source is referred to as the common node. In Figure 4.2, the load is resistive with a load resistance R_D. Another option would be an active load, such as a current mirror. In the case of the LA designed, the lowest passband frequency (few tens of megahertz) is multiple decades lower than the highest passband frequency, hence the use of an active load is not a viable solution. The impedance level of an active load is higher than what can be implemented with a passive component, which leads to a decreased achievable bandwidth. In addition, the value of the impedance is easier to design accurately with a passive load.

The MOSFET has three regions of operation; the cut-off region, the triode region (also known as the linear or ohmic region) and the saturation region (also known as the active region). Since mainly n-channel MOSFETs are used in this work, the following analysis focuses on their characteristics. However, the DC bias points are presented for both n-channel and p-channel MOSFETs.

The region where the MOSFET operates depends on the relations of its node voltages, and Figure 4.3 shows the idealised characteristic curve for the n-channel MOSFET with the triode and saturation regions. I_D is the DC drain current, and since the gate resistance is very large (ideally, infinite), the drain current is equal to the source current. V_{DS} is the DC source-to-drain voltage of the transistor, V_{GS} stands for the DC gate-source voltage and V_{th} for the transistor's threshold voltage.

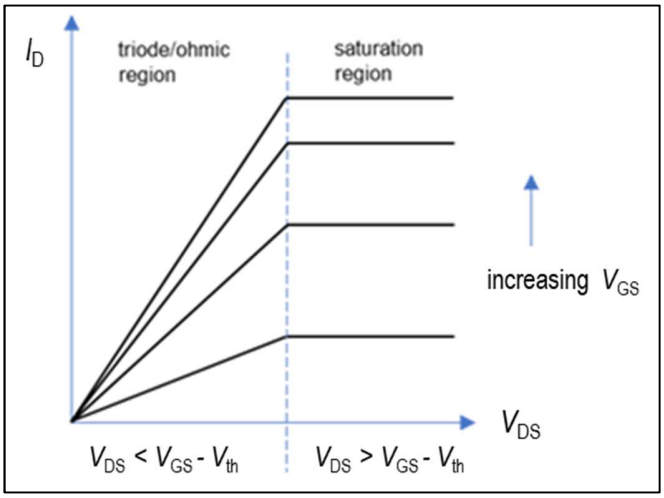

Figure 4.3. The idealized characteristic curves for an n-channel MOSFET. As V_{GS} in increased, the slope is higher in the triode region and following this, the resulting drain current is higher in the saturation region.

The transistor is in cut-off, or subthreshold region, when V_{GS} is below the threshold voltage. Ideally in this region, the current I_D from drain to source is zero, however in reality there is some subthreshold leakage current present. For the PMOS, the threshold voltage is negative, and the transistor is in the subthreshold region as long as V_{GS} is above V_{th}. In triode region, the transistor acts as a resistor. When a transistor is operated as a switch, the subthreshold and triode regions are used. Equation (4.1) depicts the idealized voltage relations of the n-channel transistor in the triode region.

$$V_{DS} < V_{GS} - V_{th} \tag{4.1}$$

The expression $V_{GS} – V_{th}$ can also be referred as the overdrive voltage V_{OV}, which is a design parameter either fixed by other requirements of the design or chosen by the designer. For the p-channel MOSFET, the corresponding expression is the triode region is

$$V_{SD} < V_{SG} - |V_{th}|, \tag{4.2}$$

where the right side of the equation is the overdrive voltage and V_{SG} is the source-to-gate voltage corresponding to the absolute value of the V_{GS} used in the equations for the n-channel transistor.

To operate the MOSFET as an amplifier, the saturation region is used. In this region, the ideal node voltage relation for the NMOS is

$$V_{DS} > V_{GS} - V_{th} \tag{4.3}$$

In saturation mode, the MOSFET acts as a voltage controlled current source where the gate-to-source voltage controls the drain current I_D as depicted by equation (4.4).

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{th})^2 \tag{4.4}$$

In equation (4.4), k_n' is the process transconductance parameter, and W and L are the width and length of the MOSFET. The process transconductance parameter is a constant determined by the process technology used to fabricate the n-channel MOSFET (Sedra & Smith 2004, pp. 237-238). Here, we define the MOSFET transconductance parameter k_n as

$$k_n = k_n' \frac{W}{L} \tag{4.5}$$

The corresponding node voltage and drain current equations for the p-channel MOSFET in saturation region are

$$V_{SD} > V_{SG} - |V_{th}| \tag{4.6}$$

$$I_D = \frac{1}{2} k_p' \frac{W}{L} (V_{SG} - |V_{th}|)^2 \tag{4.7}$$

where k_p' is the process transconductance parameter for the PMOS. Hence, in the DC bias point calculations as well as in the following small-signal analysis, the equations for the NMOS apply for the PMOS by using the following replacements (Sedra & Smith 2004, p. 281):

$$V_{GS} = |V_{GS}| \tag{4.8}$$

$$V_{th} = |V_{th}| \tag{4.9}$$

$$V_{OV} = |V_{OV}| = V_{SG} - |V_{th}| \tag{4.10}$$

$$k_n' = k_p' \tag{4.11}$$

Next, a small-signal model for the n-channel MOSFET is derived. When applying a small signal in the gate of the transistor of Figure 4.2, the instantaneous gate-to-source voltage v_{GS} becomes

$$v_{GS} = V_{GS} + v_{gs} \tag{4.12}$$

where v_{gs} is the small signal applied. The total instantaneous drain current i_D is then

$$\begin{aligned} i_D &= \frac{1}{2} k_n \left(V_{GS} + v_{gs} - V_{th}\right)^2 \\ &= \frac{1}{2} k_n (V_{GS} - V_{th})^2 + k_n (V_{GS} - V_{th}) v_{gs} + \frac{1}{2} k_n v_{gs}^2 \end{aligned} \tag{4.13}$$

In equation (4.13), the first term is the DC bias current of the transistor, the second term represents a signal current component directly proportional to v_{gs}, and the last term represents the undesirable nonlinear distortion component. The small-signal condition of the MOSFET states that the signal applied should be kept so small that the second term of equation (4.13) is significantly larger than the nonlinear distortion term (Sedra & Smith 2004, pp. 277-278),

$$k_n(V_{GS} - V_{th})v_{gs} \gg \frac{1}{2}k_n v_{gs}^2 \tag{4.14}$$

$$\rightarrow v_{gs} \ll 2(V_{GS} - V_{th}) \tag{4.15}$$

When this condition is satisfied, the last term of equation (4.13) can be neglected and the instantaneous total drain current becomes

$$i_D = \frac{1}{2}k_n(V_{GS} - V_{th})^2 + k_n(V_{GS} - V_{th})v_{gs} = I_D + i_d \tag{4.16}$$

where i_d is the drain signal current. The parameter relating the drain signal current and small-signal gate-to-source voltage is called the transconductance, g_m, of the MOSFET and can be expressed as (Sedra & Smith 2004, p. 282)

$$\begin{aligned} g_m &= \frac{i_d}{v_{gs}} = k_n(V_{GS} - V_{th}) \\ &= k_n' \frac{W}{L} V_{OV} \\ &= \sqrt{2k_n'}\sqrt{\frac{W}{L}}\sqrt{I_D} \\ &= \frac{2I_D}{V_{OV}} \end{aligned} \tag{4.17}$$

All expressions above are obtained by manipulating equations (4.4) and (4.5). The different expressions for g_m show that the design parameters for determining its value are the width-to-length ratio of the MOSFET, the DC bias drain current and the overdrive voltage.

The ideal small-signal model of a MOSFET assumes that the drain current is independent of the drain voltage, however this is not the case in reality. The dependence of drain current and drain-to-source voltage is depicted with a finite resistance r_o, which can be expressed as

$$r_o = \frac{|V_A|}{I_D}, \tag{4.18}$$

where V_A is known as the *Early* voltage and is dependent on the process technology used and the length L chosen for the transistor (Sedra & Smith 2004, p. 281). Two different small-signal equivalent models of the MOSFET are shown in Figure 4.4: the hybrid-pi model in (a) and the T-model in (b).

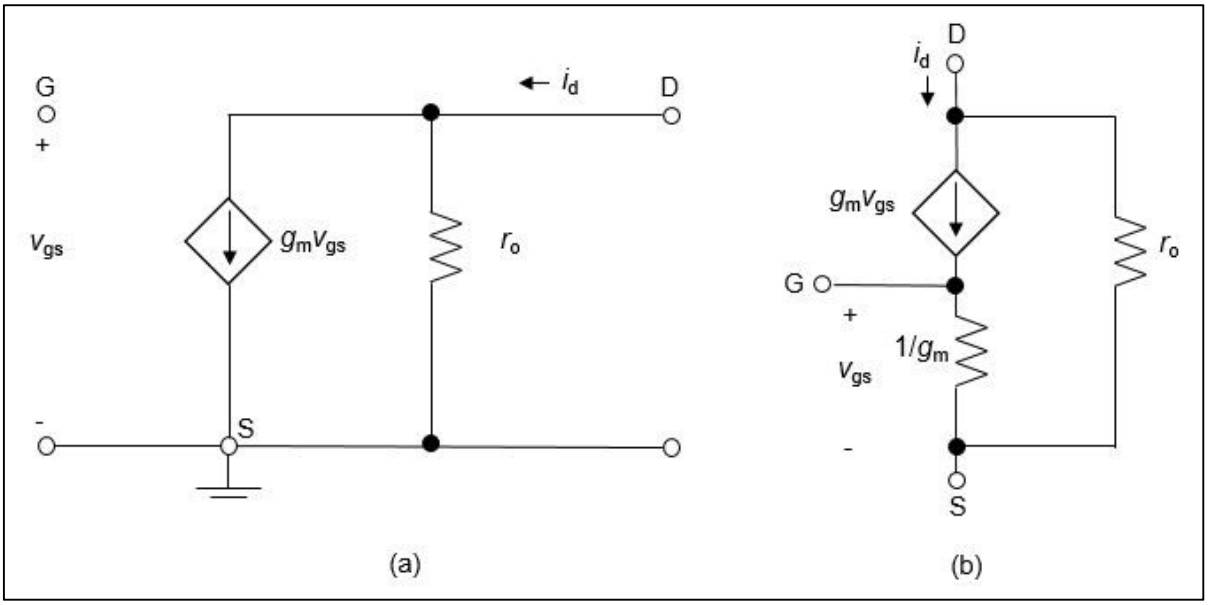

Figure 4.4. The small-signal models for an n-channel MOSFET: (a) the hybrid-pi model and (b) the T-model.

An important figure of performance of a transistor is its unity-gain frequency. The internal capacitances that affect most the high-frequency response of the transistor are the gate-to-source and gate-to-drain capacitances, denoted C_{gs} and C_{gd}, respectively. Figure 4.5 shows the high-frequency equivalent circuit of the MOSFET.

The unity-gain frequency f_T is defined by g_m, C_{gs} and C_{gd} according to the following equation (Sedra & Smith 2004, p. 705):

$$f_T = \frac{g_m}{2 \cdot \pi \cdot (C_{gs} + C_{gd})} \tag{4.19}$$

In addition to C_{gs} and C_{gd}, there are multiple other parasitic capacitances forming in the transistor as well as, for example, the signal paths of the circuit. Therefore, the actual high-frequency response is difficult to predict accurately, but the unity-gain frequency gives a good evaluation.

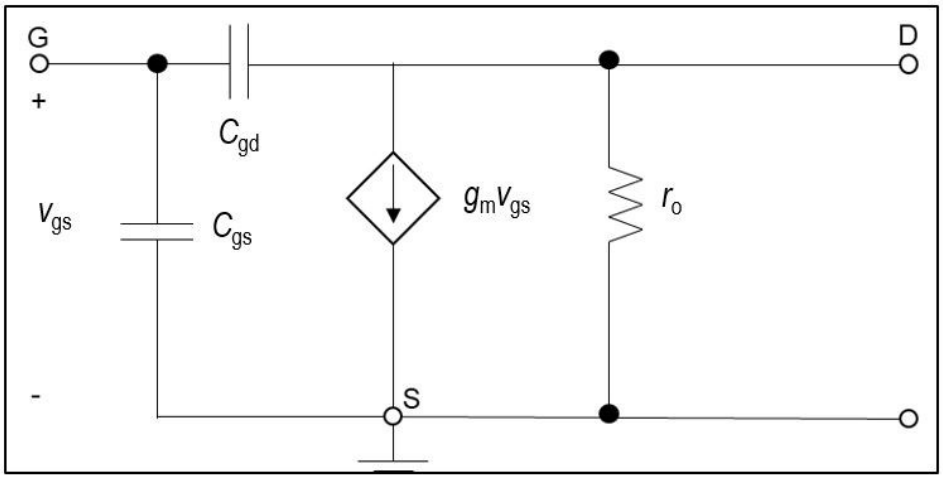

Figure 4.5. The high-frequency equivalent model of an n-channel MOSFET with the most significant parasitic capacitances C_{gd} and C_{gs}. (Sedra & Smith 2004, p. 705)

For the derivation of the low-frequency voltage gain of the common-source amplifier, the parasitic capacitances are ignored. By accounting for the load resistance R_D of Figure 4.2, the equivalent circuit of Figure 4.6 is obtained for the small-signal analysis.

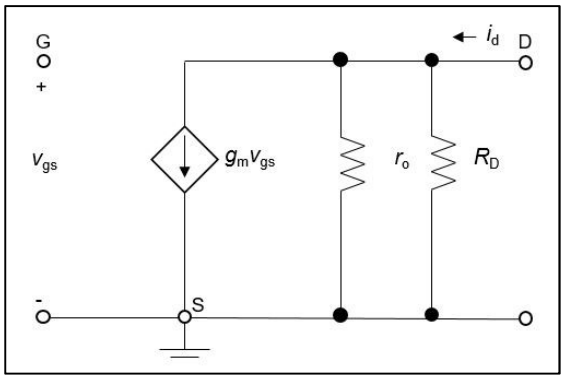

Figure 4.6. The hybrid-pi small-signal model of the CS configuration with the load resistance R_D taken into account.

The overall voltage at the drain is

$$v_{DS} = V_{DD} - (R_D||r_o) \cdot i_D = V_{DD} - (R_D||r_o) \cdot (I_D + i_d), \tag{4.20}$$

where V_{DD} is the supply DC voltage and i_D is the instantaneous drain current. The supply voltage can be expressed as

$$V_{DD} = V_{DS} + (R_D||r_o) \cdot I_D \tag{4.21}$$

Substituting equation (4.21) to equation (4.20) gives

$$v_{\mathrm{DS}} = V_{\mathrm{DS}} - (R_{\mathrm{D}}||r_{\mathrm{o}}) \cdot i_{\mathrm{d}}, \tag{4.22}$$

where the second term is the small-signal drain-to-source voltage v_{ds},

$$v_{\mathrm{ds}} = -(R_{\mathrm{D}}||r_{\mathrm{o}})i_{\mathrm{d}} = -(R_{\mathrm{D}}||r_{\mathrm{o}})g_{\mathrm{m}}v_{\mathrm{gs}} \tag{4.23}$$

Hence the small-signal voltage gain A_{V} of the circuit in Figure 4.6 is obtained:

$$A_{\mathrm{V}} = \frac{v_{\mathrm{ds}}}{v_{\mathrm{gs}}} = -g_{\mathrm{m}}(R_{\mathrm{D}}||r_{\mathrm{o}}) \tag{4.24}$$

The output resistance r_{o} is proportional to the channel length L and inversely proportional to the drain current I_{D}, hence both g_{m} and r_{o} depend on the bias point of the MOSFET. When designing a CS amplifier for a specified voltage gain, after the bias point has been chosen, the voltage gain is specified by varying the load resistor R_{D} and the MOSFET W/L.

The voltage gain without the load resistance R_D gives an expression for the transistor's intrinsic gain A_{i}:

$$A_{\mathrm{i}} = -g_{\mathrm{m}}r_{\mathrm{o}} \tag{4.25}$$

The intrinsic gain of the transistor depicts the maximum possible voltage gain it can provide at small frequencies (Carusone, Johns & Martin 2012, p. 36), i.e. at frequencies where the internal parasitic capacitances do not affect the gain. In addition to the unity-gain frequency, the intrinsic gain is one important measure of performance of the transistor.

A more detailed analysis of equations (4.24) and (4.25) reveals that high gain requires long gate lengths and biasing with low effective gate-source voltage V_{gs}-V_{th} whereas for high f_{T} short gate lengths and high V_{gs}-V_{th} would be desirable. This sums up the basic design trade-off for MOSFET amplifiers: one must find a compromise between the gain and the bandwidth of the amplifier.

4.2 The differential CS amplifier

The amplifier's input gain cell and core are implemented with differential MOSFET pairs with resistive loads. Figure 4.7 shows the basic configuration of this topology. It consists of two matched n-channel MOSFETs and load resistors R_{D}. The current source biasing the transistor pair is considered ideal at this point, meaning that it has an infinite resistance and a virtual ground is formed at the sources of the transistor.

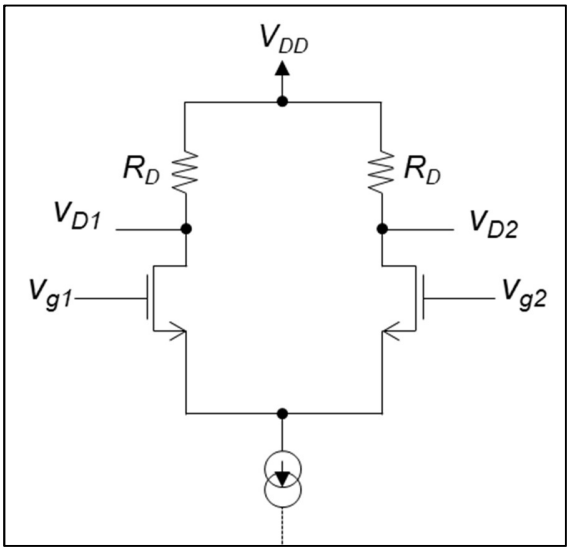

Figure 4.7. The schematic circuit of a differential CS amplifier with an ideal current source biasing the transistors.

A common-mode dc biasing voltage V_{CM} and a signal v_{in} is applied to the gates, hence their total voltages are

$$v_{g1} = V_{CM} + \frac{1}{2}v_{in} \tag{4.26}$$

$$v_{g2} = V_{CM} - \frac{1}{2}v_{in} \tag{4.27}$$

In order to act as an amplifier, the MOSFET needs to maintain the saturation mode. To satisfy this requirement, the maximum value of V_{CM} is

$$V_{CM,max} = V_{th} + V_{DD} - \frac{I_D}{2}R_D \tag{4.28}$$

The minimum value of V_{CM} is defined by the voltage needed across the non-ideal current source for it operate properly. If we denote the voltage required across the current source with V_{CS}, the lowest value of V_{CM} is

$$V_{CM,min} = V_{CS} + V_{GS} \tag{4.29}$$

Equations (4.28) and (4.29) define the input common-mode range of the differential amplifier.

Equations (4.26) and (4.27) assume that the input signal v_{in} is fed in balanced manner, i.e. v_{g1} is increased by $v_{in}/2$ and v_{g2} is decreased by $v_{in}/2$. This is the case for example when the amplifier

is fed from the output of another differential amplifier. This is how the amplifiers are connected in the design, apart from the inputs of the first amplifier stage. The output of the differential amplifier can either be taken single-ended of differentially. In the case of single-ended outputs, the small-signal output voltages will be superimposed with the DC voltages in the drains. Taking the output differentially means taking it between the two drains, and the resulting signal will ideally not have a DC component. The magnitude of the differential output signal is twice the magnitude of a single-ended output signal, hence the gain difference between these two is 6 dB.

From the circuit of Figure 4.7, the circuit of Figure 4.8 (a) can be derived to conduct the small-signal analysis of the differential CS amplifier. The transistors and resistors are assumed to be ideally matching, hence the analysis of the circuit can be conducted with a differential half-circuit shown in Figure 4.8 (b). With these assumptions, the small-signal analysis presented in chapter 4.1 applies.

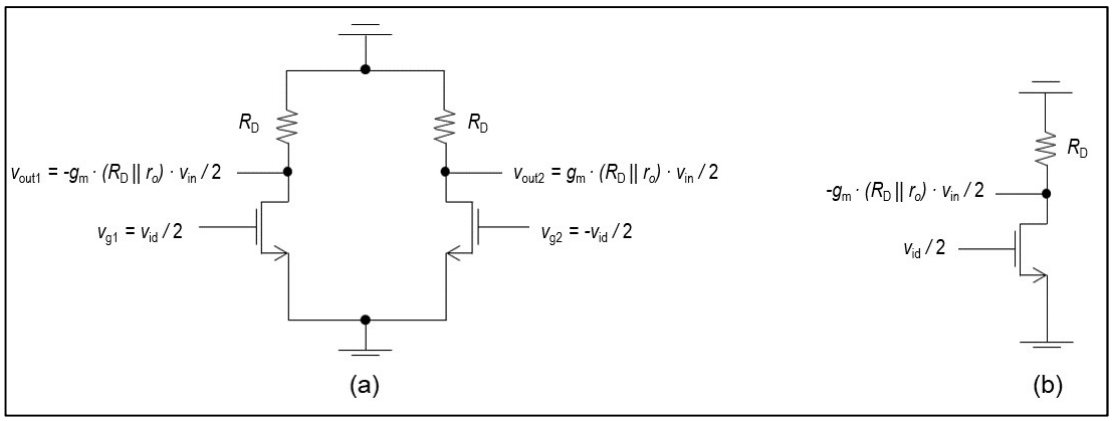

Figure 4.8. The circuits to conduct the small-signal analysis of the differential amplifier of Figure 4.7: (a) the equivalent small-signal model of the circuit of Figure 4.7 and (b) a differential half-circuit derived from figure (a).

The analysis above assumed the biasing current source to be ideal, hence its impedance would be infinite. Another assumption was made that the load resistors R_D would be ideally matching. In practise, the biasing network has a finite impedance, and there might be some mismatching between the load resistors. The effect of the current source's finite resistance R_{cs} to the resulting output voltage, when introducing a common-mode interference signal in the input, can be reviewed with the circuits of figure. Figure 4.9 (a) represents the small-signal equivalent model with the transistors replaced with their T-model and r_o neglected. Figure 4.9 (b) is the circuit of Figure 4.9 (a) divided into common-mode half-circuits (Sedra & Smith 2004, p. 606).

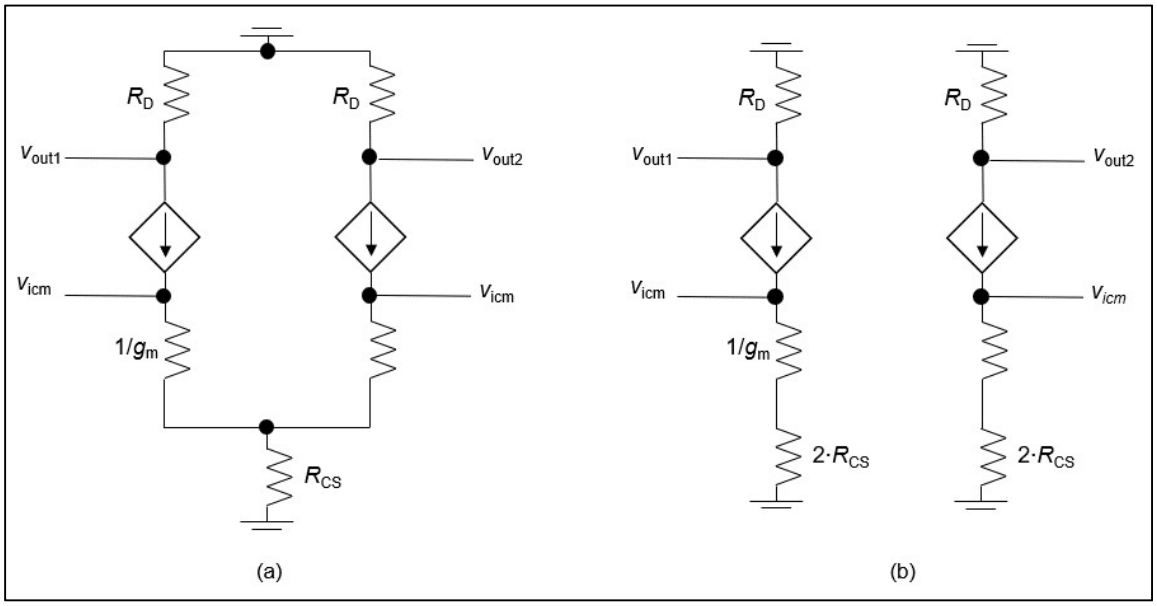

Figure 4.9. The small-signal equivalent T-model of the differential CS amplifier with r_o neglected and (a) the ideal current source replaced with a finite resistance R_{cs} and (b) the circuit of (a) divided into common-mode half-circuits.

From Figure 4.9, the voltage gains are obtained as

$$\frac{v_{\text{out1}}}{v_{\text{icm}}} = \frac{v_{\text{out2}}}{v_{\text{icm}}} = -\frac{R_{\text{D}}}{\frac{1}{g_{\text{m}}} + 2 \cdot R_{\text{cs}}}, \tag{4.30}$$

which can be simplified to

$$\frac{v_{\text{out1}}}{v_{\text{icm}}} = \frac{v_{\text{out2}}}{v_{\text{icm}}} = -\frac{R_{\text{D}}}{2 \cdot R_{\text{cs}}} \tag{4.31}$$

assuming that $1/g_m$ is significantly smaller than R_{cs}. With an ideal matching of R_D, the differential output voltage $v_{o1} - v_{o2}$ is still free of common-mode interference. However, with a mismatch of ΔR_D between the load resistors, the resulting differential voltage $v_{out,d}$ is

$$v_{\text{out,d}} = v_{\text{out1}} - v_{\text{out2}} = -\frac{R_{\text{D}}}{2 \cdot R_{\text{cs}}} \cdot v_{\text{icm}} - \left(-\frac{R_{\text{D}} + \Delta R_{\text{D}}}{2 \cdot R_{\text{cs}}}\right) \cdot v_{icm} = -\frac{\Delta R_D}{2 \cdot R_{cs}} \cdot v_{icm} \tag{4.32}$$

From this, the common-mode gain A_{cm} can be defined with

$$A_{\text{cm}} = \frac{v_{\text{out,d}}}{v_{\text{icm}}} = -\frac{\Delta R_{\text{D}}}{2 \cdot R_{\text{cs}}} \tag{4.33}$$

An important figure of performance of the differential amplifier is the common-mode rejection ratio *CMRR*, defined as the ratio of the magnitude of the common-mode gain and the magnitude of the differential gain (Sedra & Smith 2004, p. 71)

$$CMRR = 20 \cdot \frac{|A_{\mathrm{v}}|}{|A_{\mathrm{cm}}|} \tag{4.34}$$

From this analysis, it can be concluded that to obtain a high *CMRR*, the load resistors should be highly matching, and the biasing current source should have a high output resistance. In the cascaded gain cell topology used, the input stage mainly defines the common-mode rejection abilities of the limiting amplifier. The input to the amplifier is fed single-ended, and the input stage converts the signal to double ended. The signal then flows in a double-ended fashion through the amplifier, until it is finally taken out differentially. A connection between two gain cells is presented in Figure 4.10.

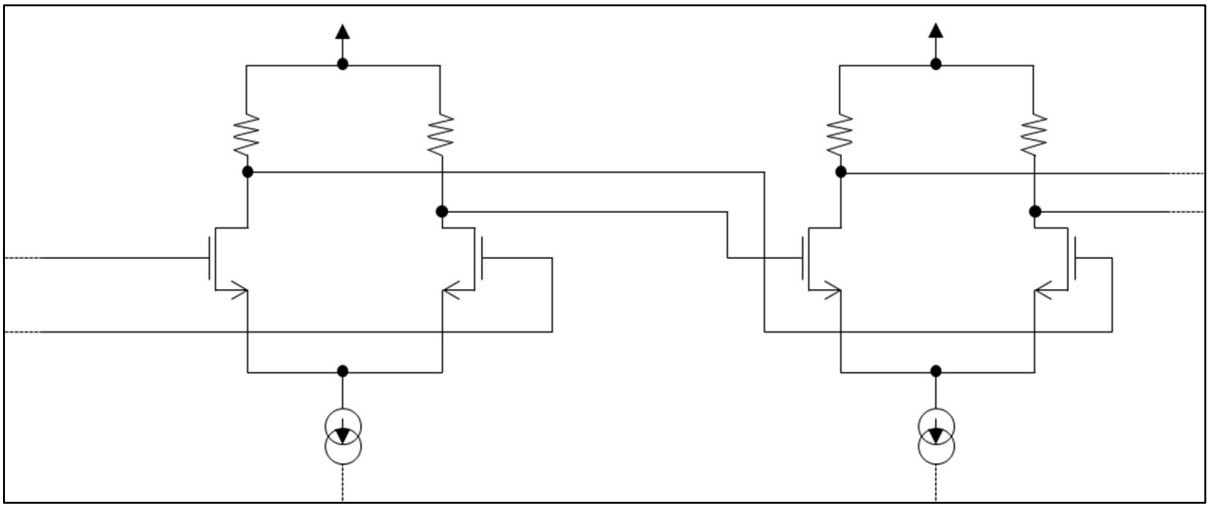

Figure 4.10. The connection of two consecutive CS gain cells with the biasing circuits presented as ideal current sources.

The midband gains of the gain stages are calculated according to equation (4.24) and are presented in Table 2.1. The values for r_o and g_m are obtained from simulations.

Table 2.1. Calculated midband gains for gain cells.

	R_D [Ω]	r_o [kΩ]	g_m [mS]	A_M [dB]
H_1	150	1,43	14,1	5,64
H_2	150	1,24	18,4	7,83
H_3	200	1,02	18,7	9,90
H_4	150	1,36	18,4	7,91
H_5	150	1,36	14,2	5,66
H_6	200	1,03	18,7	9,92
H_7	135	3,30	7,61	-0,1

4.3 The feedback

The feedback topology used in this design is the shunt-shunt topology, i.e. the sample is taken from the output voltage of the gain stage, and the feedback is fed to the input as current. An identical active feedback is used in both gain stages of the amplifier core. The active feedback circuit consists of an n-channel MOSFET connected in common-source configuration, shown in Figure 4.11.

The feedback factor β of this topology is the transconductance g_m of the feedback MOSFET (Keerthana et al. 2014) multiplied by the resistance that the feedback circuit sees. This resistance in both gain stages is 150 Ω, and the transconductance of the feedback MOSFET is 2 mS. Hence, the resulting feedback factor is

$$\beta = g_m \cdot R = 0{,}002\ \mathrm{S} \cdot 150\ \Omega = 0{,}3. \tag{4.34}$$

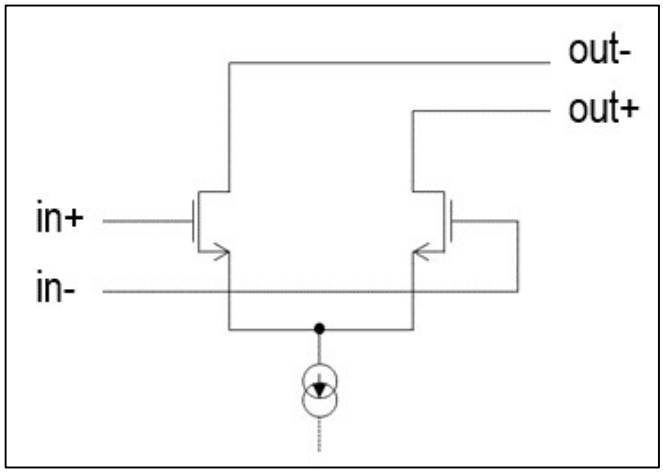

Figure 4.11. The active feedback circuit consisting of an n-channel MOSFET connected in common-source configuration.

4.4 Biasing

The gain stages are biased with an n-channel MOSFET as a constant current source. To simplify the design, every gain stage and feedback block will receive their bias voltage from the same source. The enabling or disabling of the amplifier is implemented with the circuit shown in Figure 4.12.

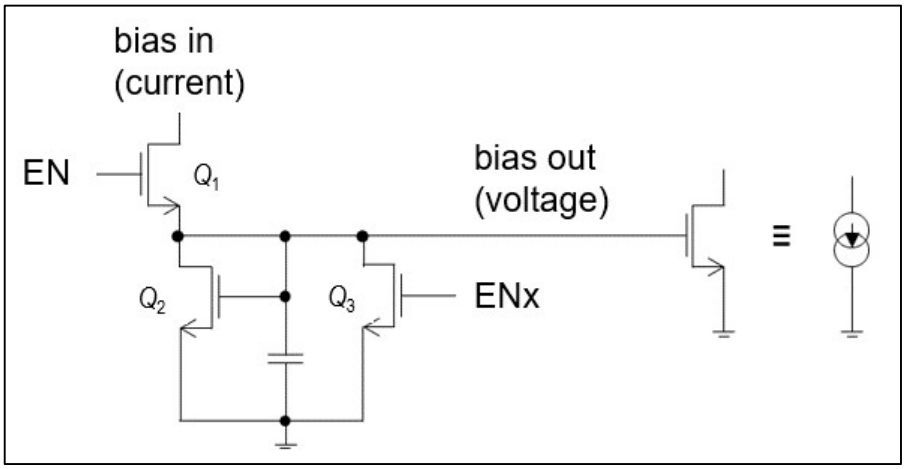

Figure 4.12. The circuit to enable or disable the amplifier. When enable bit is high, transistor Q_1 conducts and a non-zero bias voltage is formed to node bias out. When enable is low, Q_1 does not conduct and Q_3 connects the bias out node to ground.

When enable control EN is 1, its inverted value ENx is 0, the top transistor Q_1 conducts and transistor Q_3 is in cut-off. A bias current is fed to the drain of Q_1, transistor Q_2 produces a bias voltage at the node *bias out*, which is then fed to the gate of the bias transistor in the gain stages. The bias block is designed to provide a bias voltage of about 540 mV with a bias current of 200 µA. When EN is 0, ENx is 1, the upper transistor does not conduct, and transistor Q_3 connects the output bias node to ground.

A common mode voltage is required to bias the inputs of the first gain stage. This voltage is produced from the operating voltage with a simple resistor-based voltage divider circuit shown in Figure 4.13.

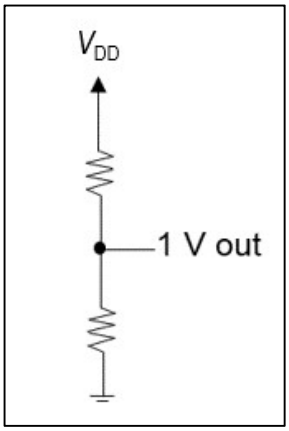

Figure 4.13. The voltage divider circuit to create a 1 V voltage for the transistor of the first gain cell.

The operating voltage V_{DD} is 1.35 V and the resulting bias voltage is 1 V. This voltage divide circuit is implemented in the same block as the gain stage biasing circuit.

4.5 The input filter and the dc offset cancellation circuit

As concluded in chapter 3.3, the DC offset is compensated with a high-pass filter at the input of the amplifier, and a feedback path with a low-pass filter. The block diagram of this topology is shown in Figure 4.14.

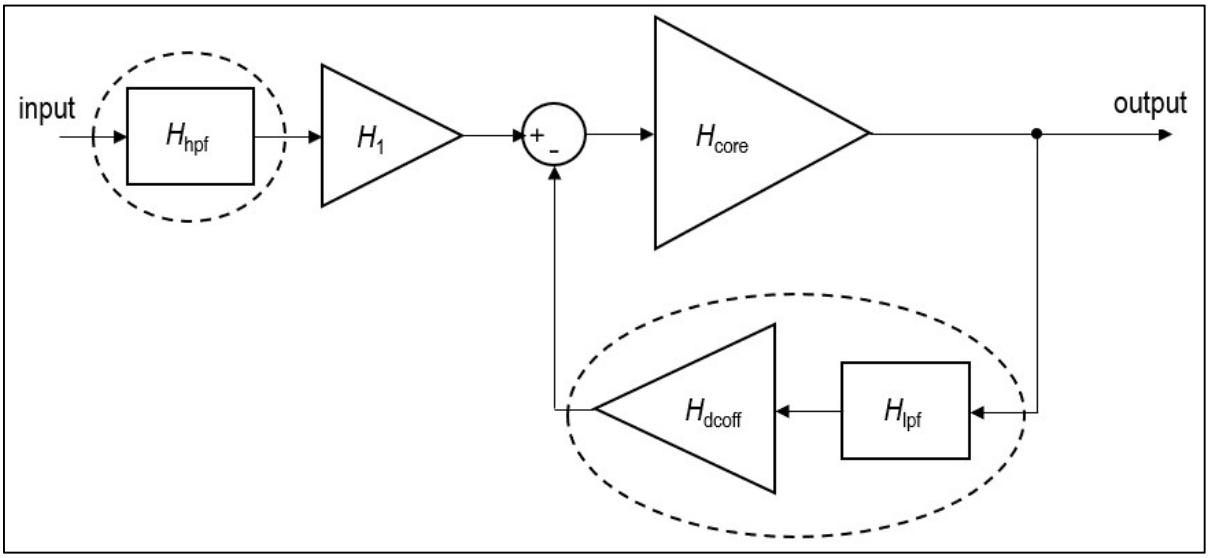

Figure 4.14. A simplified block diagram of the limiting amplifier with the input filter and the feedback filter circuit.

When choosing components for the filters, the chip area requirements for resistors and capacitors are noteworthy. For accuracy of the lower corner frequency, passive components will be used in the filter. Capacitors in general require significantly larger chip area compared to resistors, hence it is reasonable to use as small capacitances and as large resistors as possible. A tuning possibility is required for the filters, which requires more circuit components.

Tuning is implemented in the HPF with three resistor branches, of which two have a transistor as a switch. A two-bit control word enables the use of four different tuning steps, but only three of them is required. The tuning range is designed with 6-dB steps in the resistor values of the circuit. The circuit schematic for one signal path is shown in Figure 4.15, and the circuit for the other signal path is similar. The switches are denoted as S_i in Figure 4.15.

The outputs of the filter are connected to the inputs of the first gain stage, which requires a DC voltage bias of 1 V. The transistor switches need to operate in the triode region, hence p-channel MOSFETs are employed to achieve suitable biasing for the transistors. Table 4.2 contains the resistor and capacitor values along with calculated corner frequencies with different control words. The corner frequency for the high-pass filter is obtained with

$$f_c = \frac{1}{2 \cdot \pi \cdot R \cdot C} \tag{4.35}$$

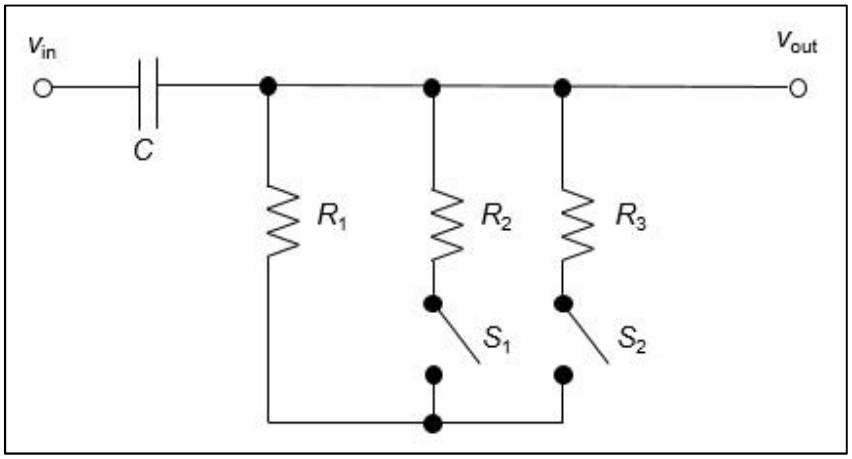

Figure 4.15. The schematic diagram of the high-pass filter. S_1 and S_2 are the switches with which the cut-off frequency of the filter can be tuned.

Table 4.2. The resistor and capacitor values, and the calculated cut-off frequency for each control word for the high-pass filter.

Control	R [kΩ]	C [fF]	f_c [MHz]
00	12.5	208	61.2
10	25	208	30.6
11	50	208	15.3

The low-pass filter is implemented with passive components in a similar manner with the high-pass filter. The schematic circuit of the low-pass filter is shown in Figure 4.16. As with the high-pass filter, the low-pass filter is controlled with a two-bit control word with three different corner frequency steps.

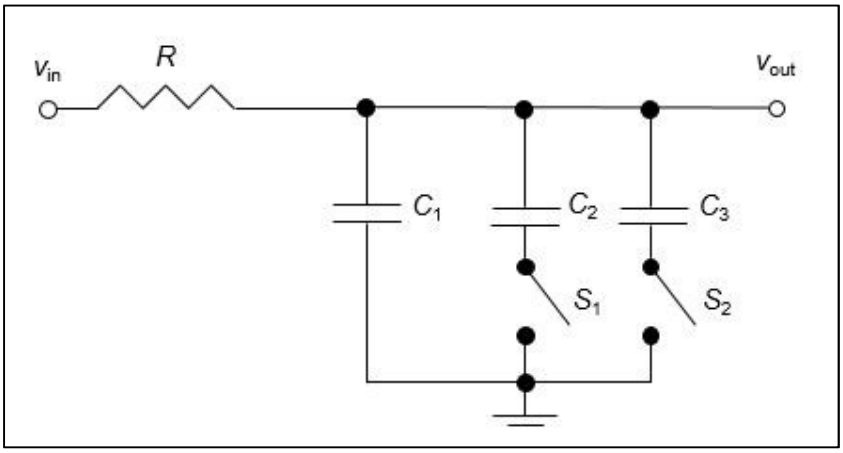

Figure 4.16. The schematic diagram of the low-pass filter. S_1 and S_2 are the switches with which the cut-off frequency of the filter can be tuned.

As explained in chapter 3.3, for a feedback factor of 0.6, the corner frequency of the low-pass filter should be about a decade lower than for the high-pass filter. In this design, the final feedback factor of the DC compensation circuit is close to this simulated value being 0.7. The calculated corner frequencies with the chosen resistance and capacitance values are presented in Table 4.3. The corner frequency for the low-pass filter is obtained with equation (3.2).

Table 4.3. The resistor and capacitor values, and the calculated cut-off frequency for each control word for the low-pass filter.

Control	R [kΩ]	C [fF]	f_c [MHz]
00	300	181	66.2
10	300	363	33
11	300	725	16.5

4.6 Layout implementation

In addition to the parasitic capacitances introduced by the components, the design of the layout introduces parasitic resistance and capacitance to the circuit, defined mostly by the signal paths. The parasitic resistance affects the midband gain of the amplifier, and the small parasitic capacitances reduce the bandwidth.

The layout should be designed to minimize these effects, but at the same time, an unplanned engagement between the sub-blocks of the circuit need to be avoided. Hence the design trade-off of the layout implementation is to keep the signal paths as short as possible, while maintaining the distance between sub-blocks not less than the minimum defined by the design tool. With the design consisting of several sub-blocks, another challenge in the layout implementation is the connections of the supply voltage and ground node to each sub-block.

With these layout rules in mind, the resulting total area of the layout implementation is

$$155\ \mu\text{m} \cdot 83\ \mu\text{m} = 12865\ \mu\text{m}^2 \approx 0.013\ \text{mm}^2$$

It was stated earlier that the filters with passive components require a large area from the chip. The area required by the high-pass and low-pass filters in total covers over 2700 mm^2, corresponding to over 20 % of the total area required by the limiting amplifier. For comparison, a single gain cell covers an area of 460 mm^2 (3.6 %). Figure 4.17 shows the principal blocks of the layout with the signal path also drawn forth. The block names in figure correspond to those of Figure 4.1.

After the layout implementation is done, the parasitic capacitances and resistances of the circuit are extracted with the design tool. These extractions are used in the simulations of the amplifier, if not otherwise mentioned. Although simulations with schematics are fast and useful during the early design phase, simulating with the parasitic extractions is the only manner to acquire a realistic result of the performance of the amplifier.

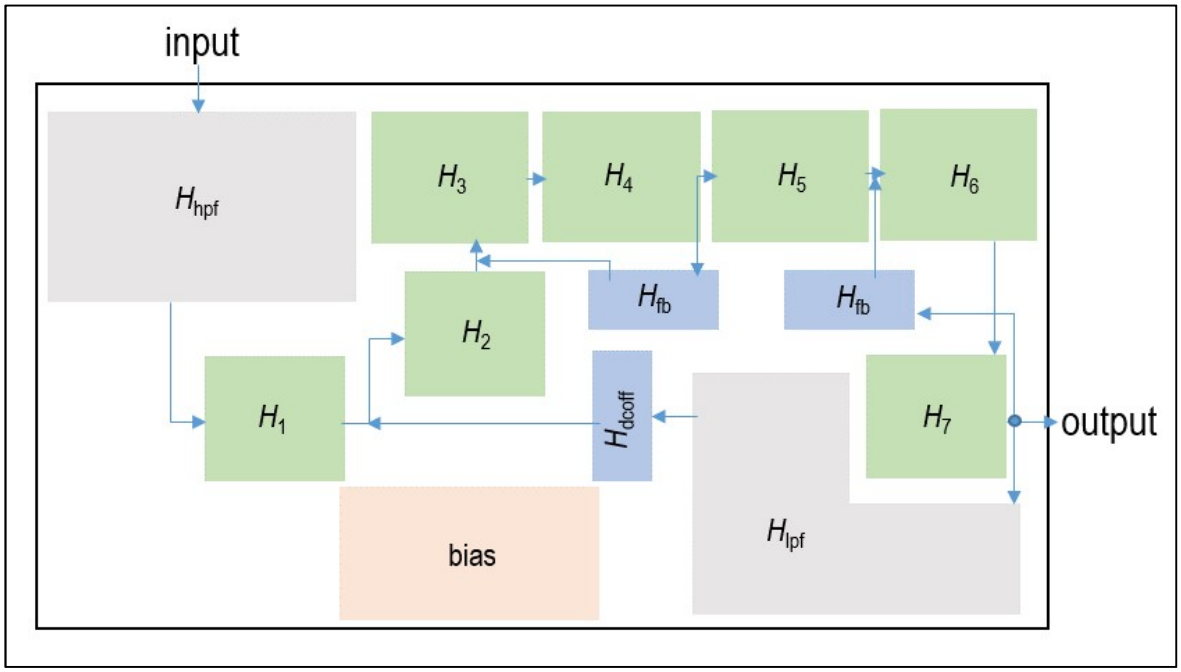

Figure 4.17. A simplified representation of the layout. The blue lines represent the signal paths in the layout.

5 SIMULATION RESULTS

The design is verified and simulated with a test arrangement shown in Figure 5.1. The preceding and the following stages of the amplifier are included to the testbench to verify the matching of the stages. Input signal for the baseband amplifier comes from the mixer, and the mixer is driven from an external file. The output buffer serves as the load for the baseband amplifier.

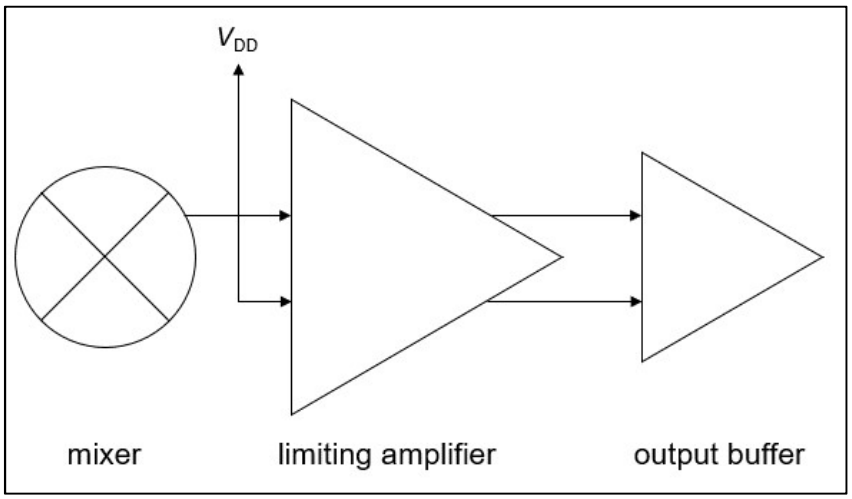

Figure 5.1. A block diagram of the testbench used in the simulations. The mixer is included to provide a real input impedance and signal, and the output buffer is included to provide a real output impedance.

The input to the limiting amplifier is single ended, hence the other input is connected to operating voltage V_{DD}. The operating voltage along with other control signals, such as the control bits for the amplifier's high- and low-pass filters are fed from ideal DC voltage sources, but a real regulator is used to feed the bias currents for the limiting amplifier and the output buffer. The default values for the amplifier are shown in Table 5.1.

In addition to typical process corner simulations in room temperature (27˚C in simulator), some simulations were conducted in worst-case scenario corners and temperatures between -10 ˚C and 90 ˚C. A process corner refers to the variation of parameters used in production of integrated circuits. It represents the extremes of the parameter variations, for example in resistors the applied tolerance is usually ±20 % of the nominal value. To achieve an adequate design margin, the design needs to be verified to function at some level in these corners. The corners are referred

Table 5.1. The default values used in the simulation of the limiting amplifier.

Input name	Default value
operating voltage, V_{DD}	1.35 V
bias current	200 uA
limiting amplifier enable	1
low-pass filter control	01
high-pass filter control	10
low-pass filter enable	1

to as the slow corner, where the carrier mobility in the devices are lower than normal, and the fast corner, where the mobility is higher than normal, respectively.

5.1 Gain and bandwidth

The gain and bandwidth are simulated first with the default control values from Table 5.1. The midband gain is defined from the frequency of 1 GHz. Figure 5.2 shows the result of the alternating current (AC) analysis, with the schematic simulation result in dashed line and extraction result in solid line. The simulated midband gain is 27.5 dB, lower corner frequency 37 MHz and higher corner frequency 11.4 GHz. There is gain peaking of about 1.3 dB at 7 GHz. With the schematic simulation, the midband gain is 30.9 dB and the 3-dB bandwidth ranges from 38 MHz to 19.5 GHz.

According to this simulation, the corner frequencies f_L and f_H seem to set very well where they were designed. In the design phase, the gain was decreased 2-3 dB in order to improve the stability of the amplifier. It was seen in early simulations, that the phase margin for one of the feedback loops was lower than what was desirable. However, a midband gain of over 27 dB with the desired bandwidth and nominal bias current is an approvable result with the extraction simulation.

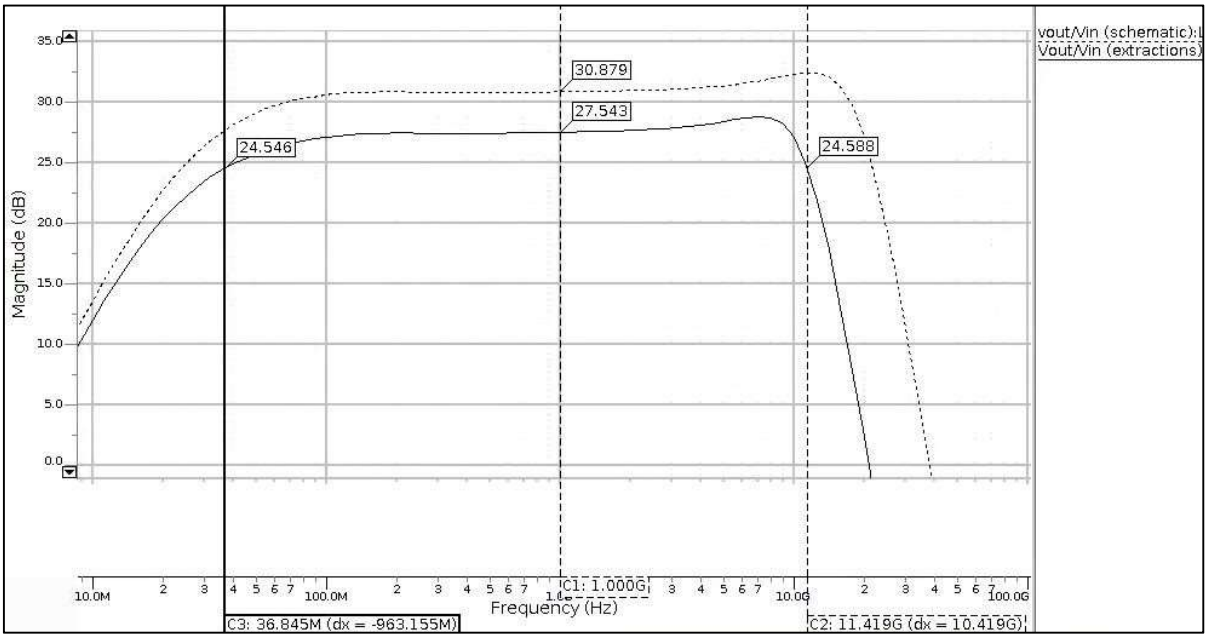

Figure 5.2. The amplitude response of the limiting amplifier as of function of frequency for the schematic simulation (dashed line) and extraction simulation (solid line).

Figure 5.3 shows the transient simulation result for the differential output voltage (*V*out_diff, upper plot), single-ended input voltage (*V*in, middle plot) and operating current (*I*_dd, lower plot*)*. There is no significant overshoot or offset seen in the transient simulation result. According to this simulation, the voltage gain is

$$A = 20 \cdot \log_{10}\left(\frac{756.625\ \text{mV}}{39.418\ \text{mV}}\right) \approx 25.7\ \text{dB}$$

and the current through the operating voltage node is approximately 25 mA. With an operating voltage of 1.35 V, the power dissipation of the amplifier is hence

$$P_{\text{tot}} = I_{\text{dd}} \cdot V_{\text{DD}} = 25\ \text{mA} \cdot 1.35\ \text{V} = 33.75\ \text{mW}$$

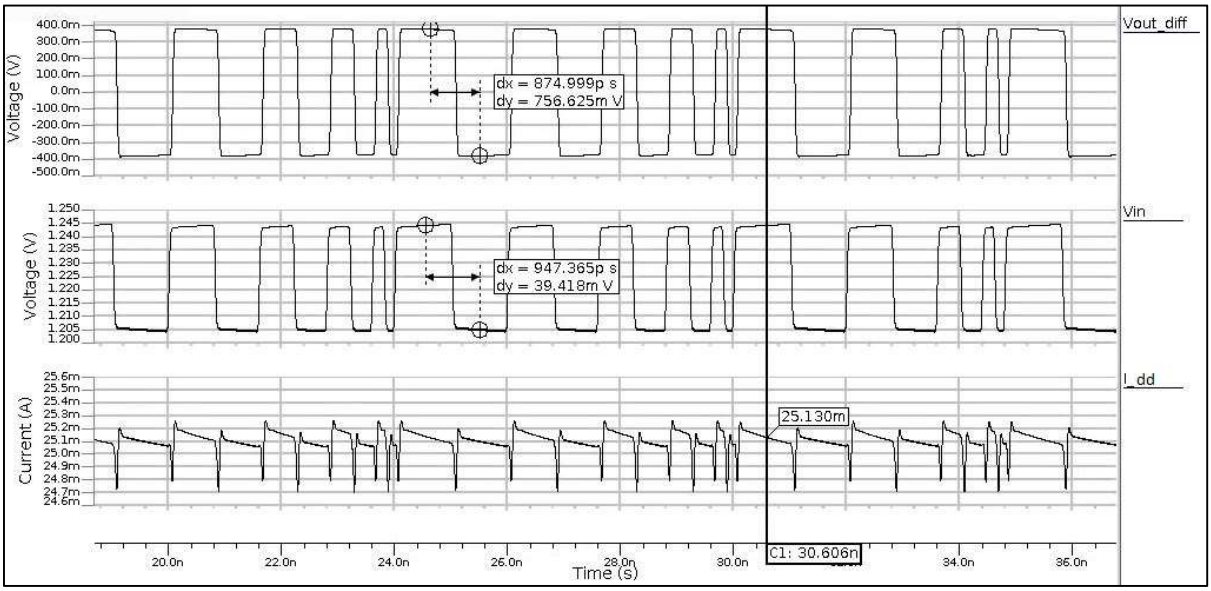

Figure 5.3. The transient simulation of the limiting amplifier, presenting the differential output voltage (upper plot), the single-ended input voltage (middle plot) and the supply current (lower plot).

The effect of the bias current magnitude to the gain at 1 GHz and gain peaking is simulated by sweeping the bias current from 50 µA to 600 µA with increments of 50 µA. The gain peaking at different bias points is calculated as the difference between the highest gain and the gain at 1 GHz. These results are presented in Figure 5.4.

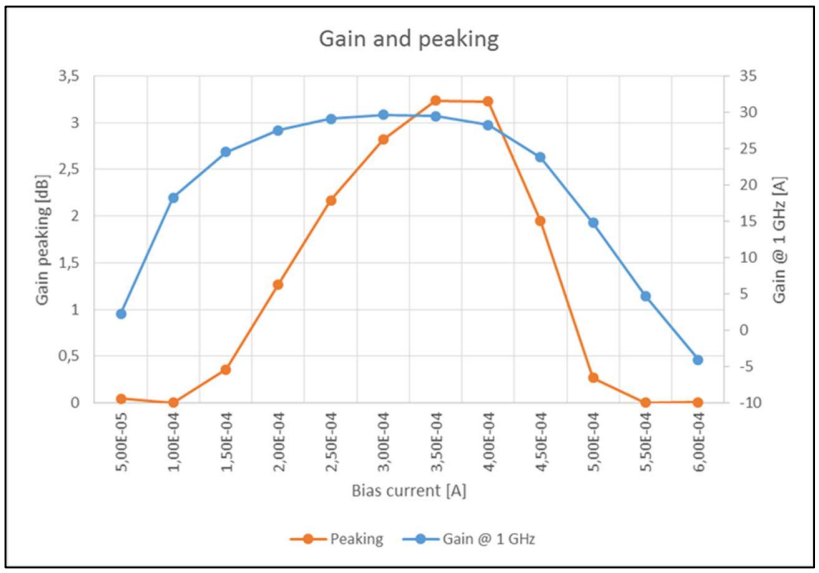

Figure 5.4. The simulation results of the gain (blue line) and gain peaking (orange line) as a function of the bias current.

With nominal bias current, gain peaking is approximately 1.3 dB and occurs at a frequency of 7.1 GHz. The gain peaking is at its highest, over 3 dB, with bias current 350 µA and 400 µA. If the bias current is further increased, both gain and gain peaking decrease due to the bias MOSFET's transition from saturation region to ohmic region.

The point of highest gain point is found with a steady-state simulation and sweeping of the bias current with increments of 10 µA. The magnitude of the differential output voltage is plotted as a function of the bias current. This result is seen in Figure 5.5. Highest gain is obtained with a bias current of 310 µA. Next, the output voltage as a function of input voltage is simulated in steady-state with the bias current of 310 µA. The differential output voltage $v_{out,diff}$ as a function of input voltage is presented in Figure 5.6.

Figure 5.5. The magnitude of the differential output voltage as a function of the bias current to determine the bias current with which the gain is at its highest.

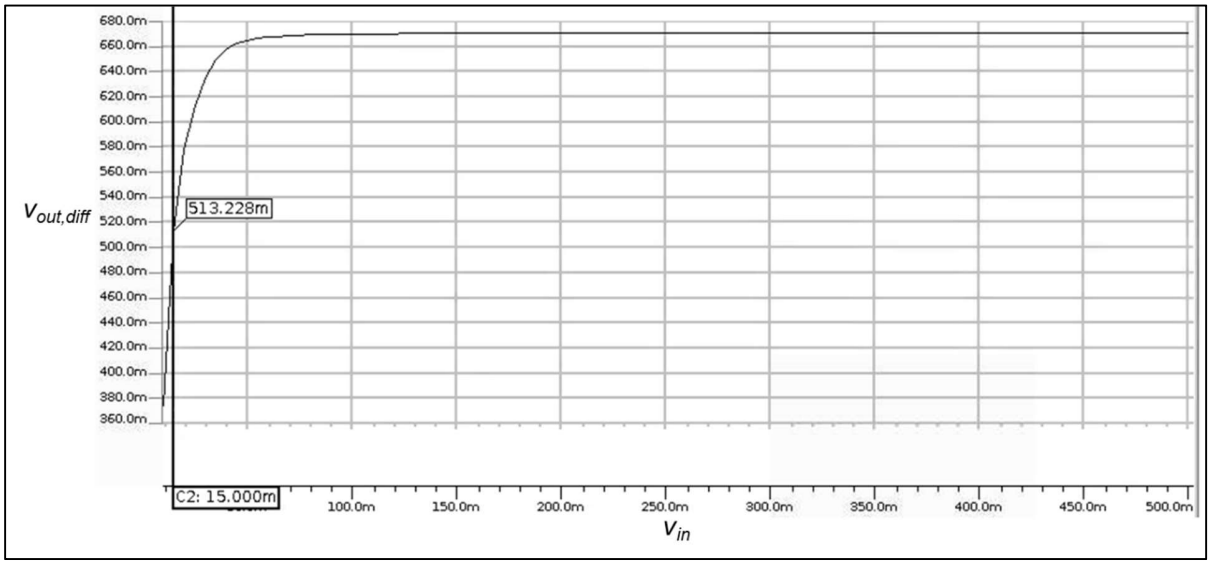

Figure 5.6. The differential output voltage $v_{out,diff}$ as a function of input voltage with a bias current of 310 µA.

The limiting range of the amplifier starts from 15 mV input voltage, and the maximum input voltage of the amplifier is 500 mV. The input dynamic range *D* of the amplifier in decibels is

$$D = 20 \cdot \log_{10}\left(\frac{500\ \text{mV}}{15\ \text{mV}}\right) = 30.46\ \text{dB}$$

The maximum gain of the amplifier is

$$A_{\max} = 20 \cdot \log_{10}\left(\frac{513.228\ \text{mV}}{15\ \text{mV}}\right) = 30.7\ \text{dB},$$

hence the target of 30 dB gain is achieved with a bias current of 310 µA.

5.2 Performance in temperatures and process corners

In addition to the typical conditions, the gain and bandwidth simulations were performed in temperatures of -10 ˚C and 90 ˚C, as well as in slow and fast corners. The amplitude response of the amplifier's differential output in extreme temperatures is presented in Figure 5.7.

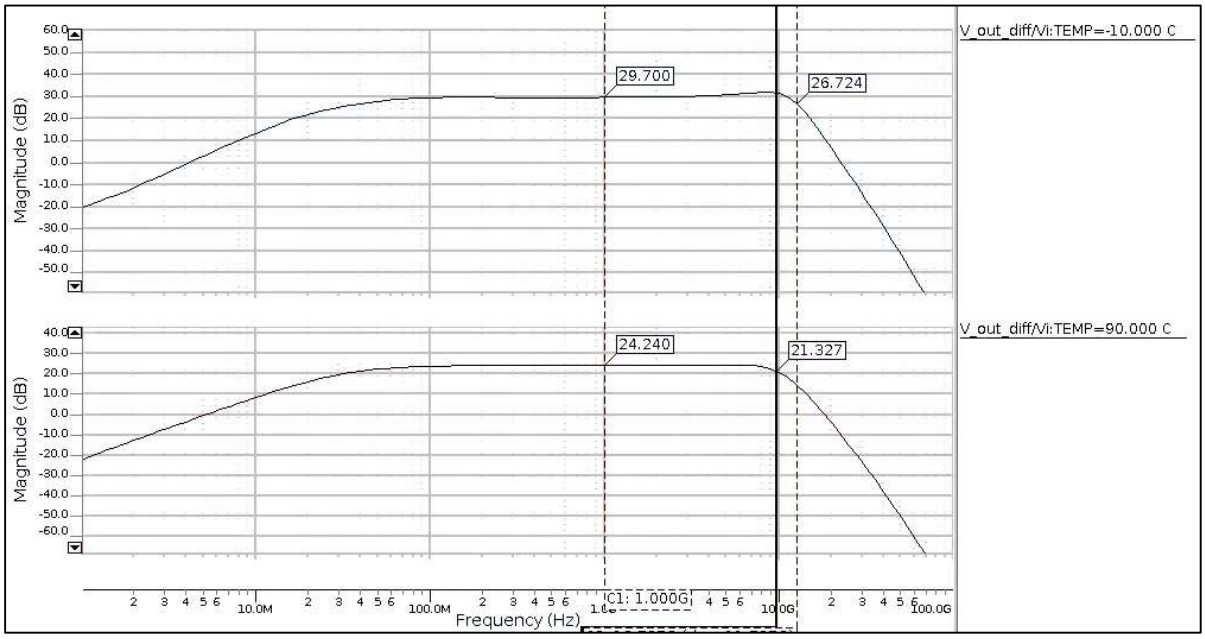

Figure 5.7. The amplitude response of the amplifier as a function of frequency in temperatures of -10 °C (upper plot) and 90 °C (lower plot).

In -10 ˚C (upper plot in Figure 5.7), the midband gain rises to 29.7 dB with a bandwidth of 12.7 GHz. Considering that the gain peaking in this condition is under 2 dB, the frequency domain analysis result is excellent. In 90 ˚C (lower plot in Figure 5.7), both the gain and bandwidth fall being 24.2 dB and 9.6 GHz, respectively. Results from the transient simulation in Figure 5.8 show that in low temperature, the gain is 24.5 dB and in high temperature, the gain is 23.7 dB. As in typical simulations, there is less gain seen in the time domain, but the gains and bandwidths achieved here are sufficient to verify that the design margin is good considering varying temperature conditions.

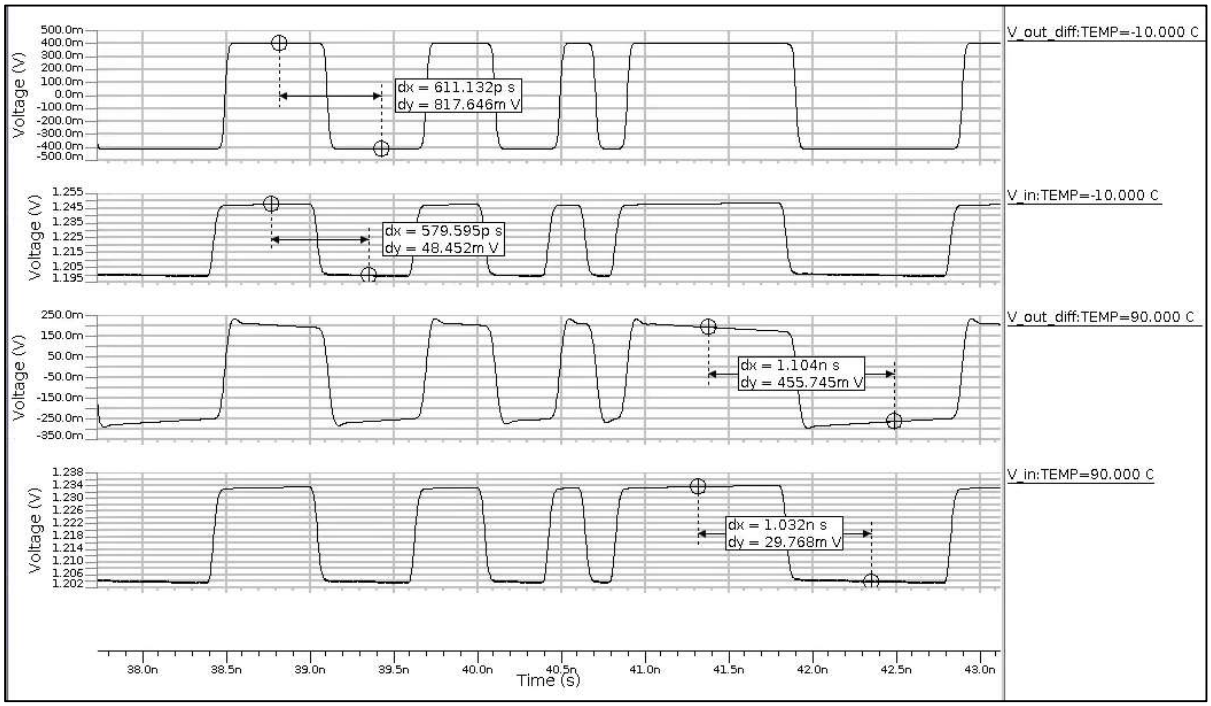

Figure 5.8. The transient simulation in temperatures of -10 °C and 90 °C, presenting the differential output voltage and single-ended input voltage.

The amplitude response of the amplifier in slow and fast corners is presented in Figure 5.9. The 3-dB bandwidth remains in over 10 GHz in both corners. The gain in slow corner simulation increases to 31.3 dB, and there is a gain peaking of 2.5 dB at a frequency of about 7 GHz. The fast corner gain decreases down to 21.6 dB.

Figure 5.10 shows the transient simulation result in process corners. In the slow corner, the gain according to the transient simulation is 27.4 dB. The signal does not experience any baseline wondering, and there is no significant overshoot. In the fast corner, the gain falls to 21.4 dB, and the transient shows clearly some signal distortion. However, there is no significant offset in the signal, which would prevent the receiving of the signal.

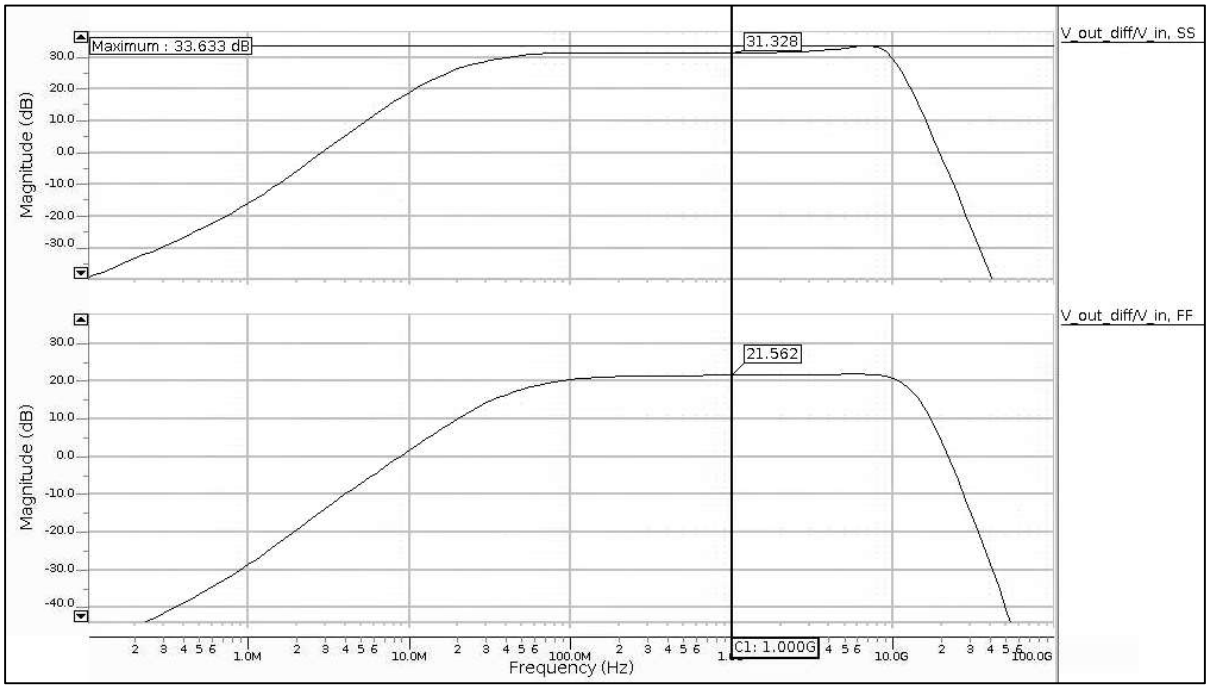

Figure 5.9. The amplitude response of the differential output voltage in slow (upper plot) and fast (lower plot) process corners.

Some of the lost performance in the fast corner can be fixed by increasing the bias current. Increasing the bias current from 200 µA to 300 µA improves the midband gain with a little over 2 dB as shown in Figure 5.11. The transient simulation under these conditions shows that the gain has improved, being 23 dB. There is some baseline wondering seen in the output voltage, but difference to the reference level of 0 V is still well achieved. The result of the transient simulation in the fast corner with a bias current of 300 µA is shown in Figure 5.12.

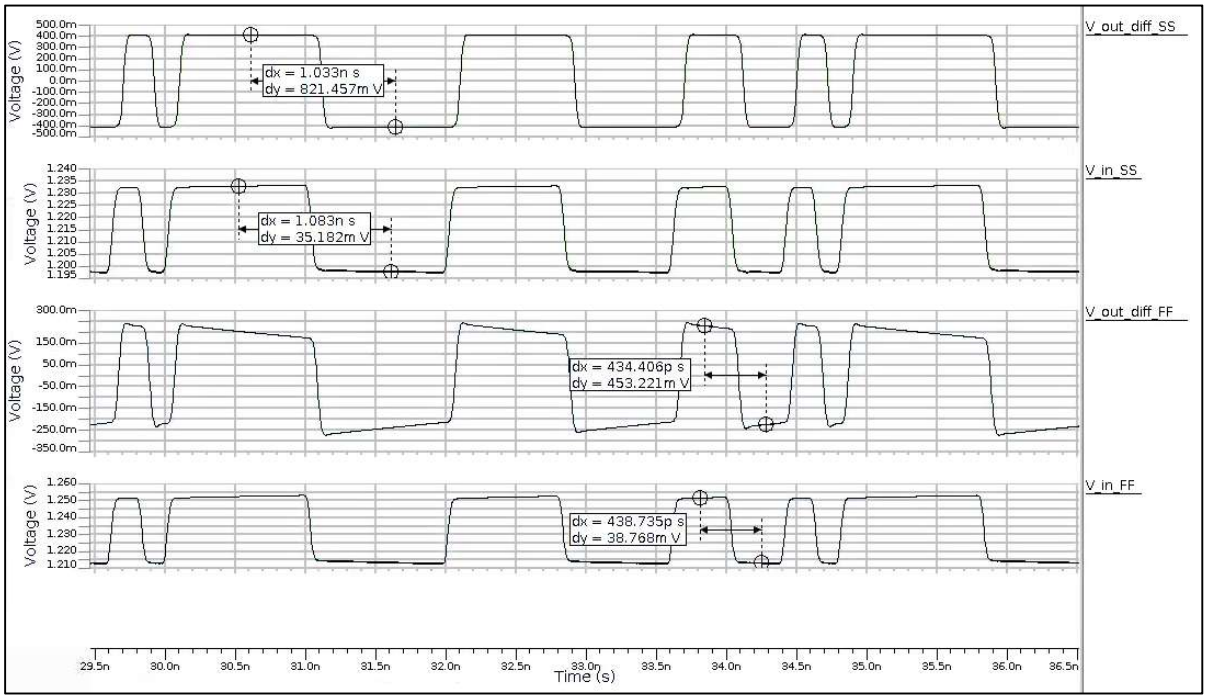

Figure 5.10. The transient simulation of the differential output voltage and single-ended input voltage in slow process corner (two upper plots) and fast process corners (two lower plots).

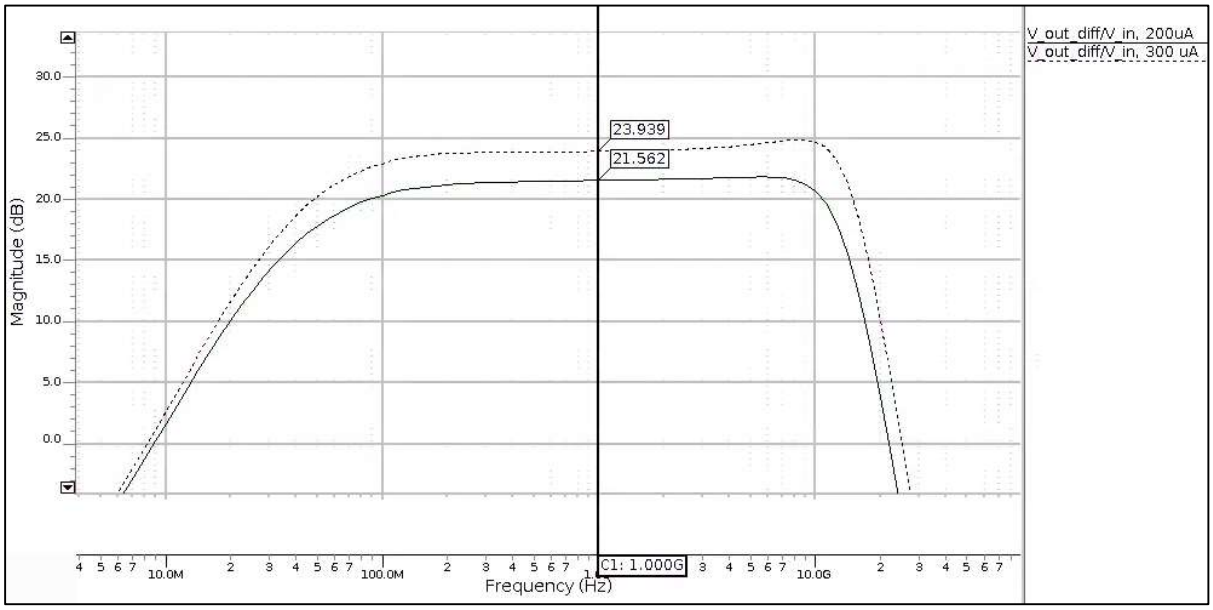

Figure 5.11. The amplitude response in the fast process corner with a bias current of 300 µA (dashed line) and 200 µA (solid line). Increasing the bias current results in a midband gain improvement of over 2 dB.

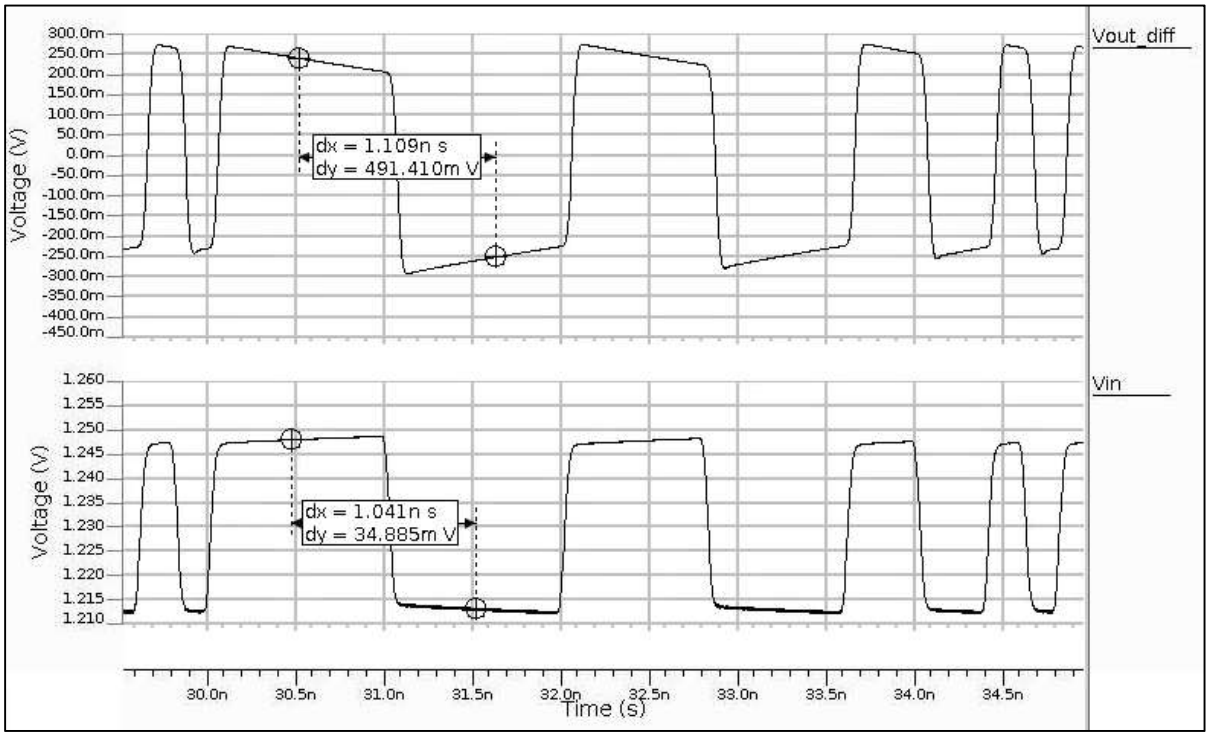

Figure 5.12. The transient simulation results of the differential output voltage (Vout_diff, upper plot) and input voltage (Vin, lower plot) in the fast process corner with a bias current of 300 µA.

5.3 Start-up and shut-down simulations

A start-up and shut-down simulation were performed in order to verify the functionality of the enabling block and to simulate the idle current consumed by the amplifier. The result of the start-up simulation is presented in Figure 5.13. The upper plot is the differential output voltage, the middle plot shows the enable bit and the lower plot shows the result for the operating current.

The enable bit goes up at the time of 15 ns. The simulation results show that there is a delay of about 2 ns before the signal is seen at the amplifier's output. However, the total settling time of the amplifier's output is only about 5 ns. In idle mode, the current consumption of the amplifier is about 30 nA. This is traced back to the bias block which contains the resistive voltage divider circuit and provides the bias voltage to the gates of the first gain stage.

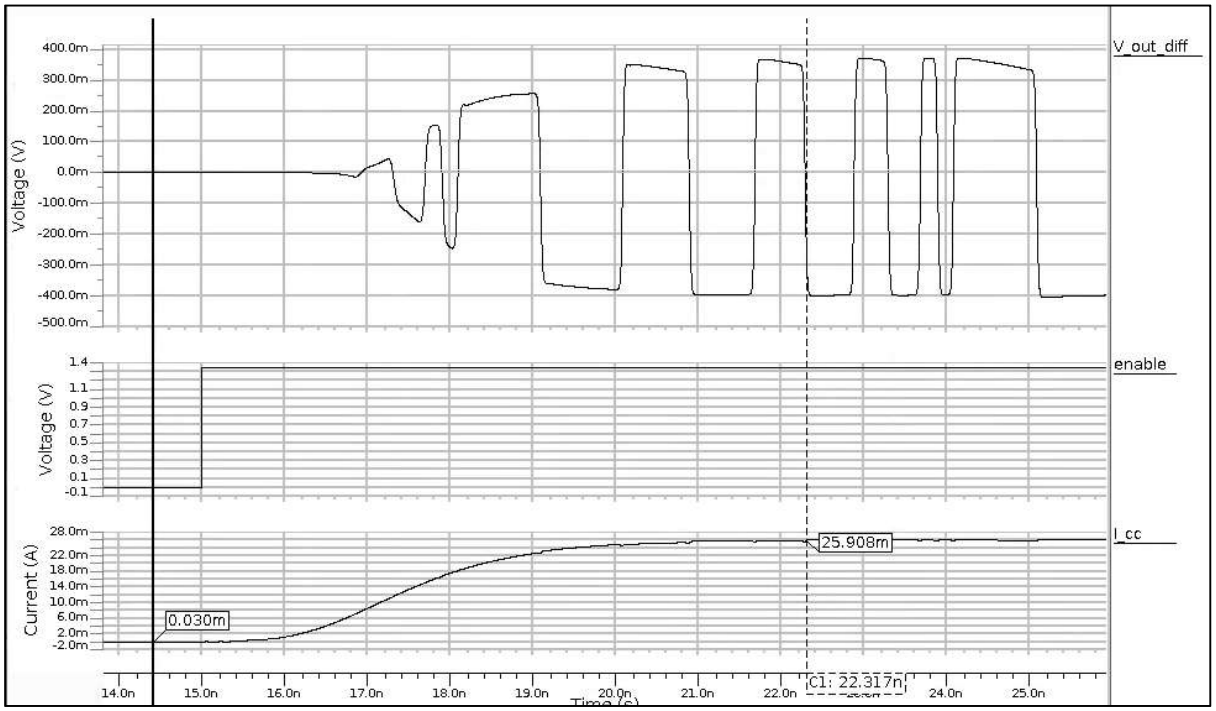

Figure 5.13. The start-up simulation of the amplifier: the differential output voltage (V_out_diff, upper plot), the enable bit (enable, middle plot) and the supply current (I_cc, lower plot).

To reduce the amplifier's idle current consumption close to zero, an external regulator could have been used to provide the bias voltage. On the other hand, a regulator also has some idle current flowing through it, and it would have required its own chip area in the layout implementation. In addition, the bias voltage coming from a resistive voltage divider circuit and connected directly between the operating voltage and ground is stable.

Figure 5.14 shows the same voltages and operating current in the shut-down situation. The enable bit goes low at time 30 ns, and there is a delay of about 2,5 ns for the amplifier's output to go to zero.

As a summary, the startup and shutdown simulations show that the enabling and disabling of the amplifier works as was designed, and the current consumption in idle state is tolerable.

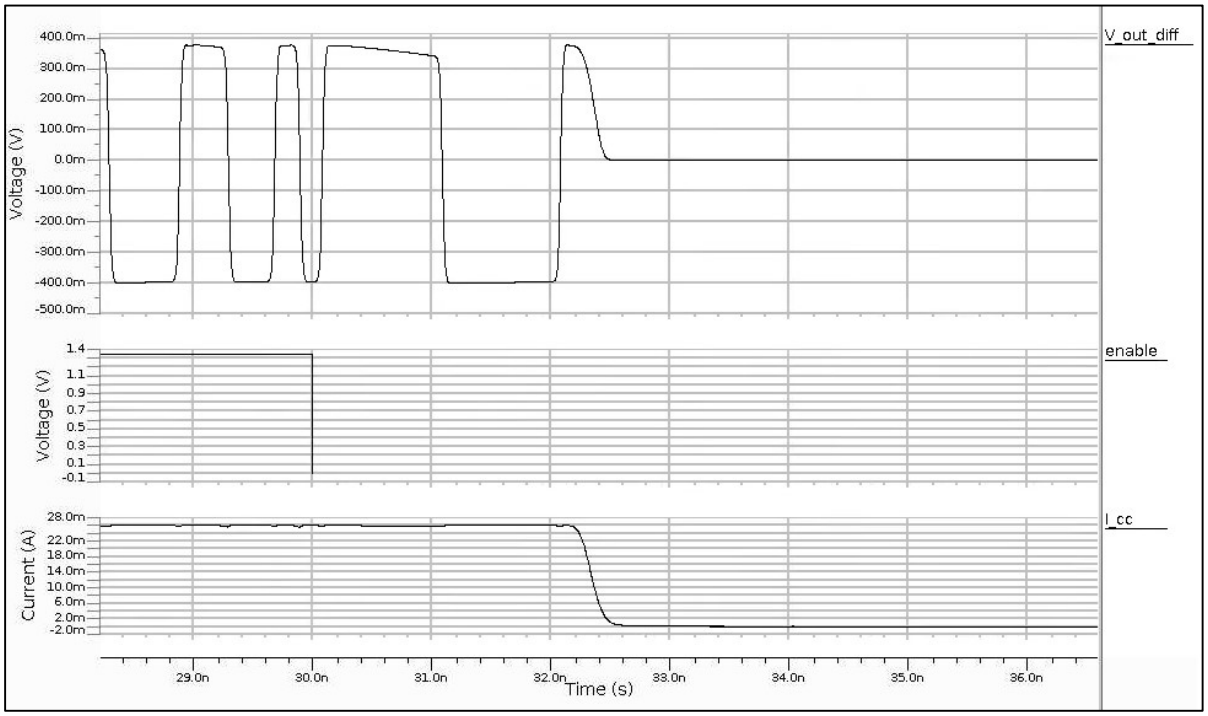

Figure 5.14. The shut-down simulation of the amplifier: the differential output voltage (V_out_diff, upper plot), the enable bit (enable, middle plot) and the supply current (I_cc, lower plot).

5.4 Stability

For the stability analysis, the circuit was divided into three sub-circuits: loop 1, loop 2 and loop 3. The loops are presented in Figure 5.15. In Figure 5.16 the results from the differential mode loop stability simulations are presented. The following phase margins can be read from the plots:

- Loop 1: 76.2˚
- Loop 2: 135.7˚
- Loop 3: 89.4˚

The result shows that there is a sufficient phase margin for every loop. The gain of loop 1 was decreased in the design phase, when it was seen in early simulations that it would have had a low phase margin. It still has the lowest phase margin of the loops; hence it is simulated separately to see how the bias current affects its stability.

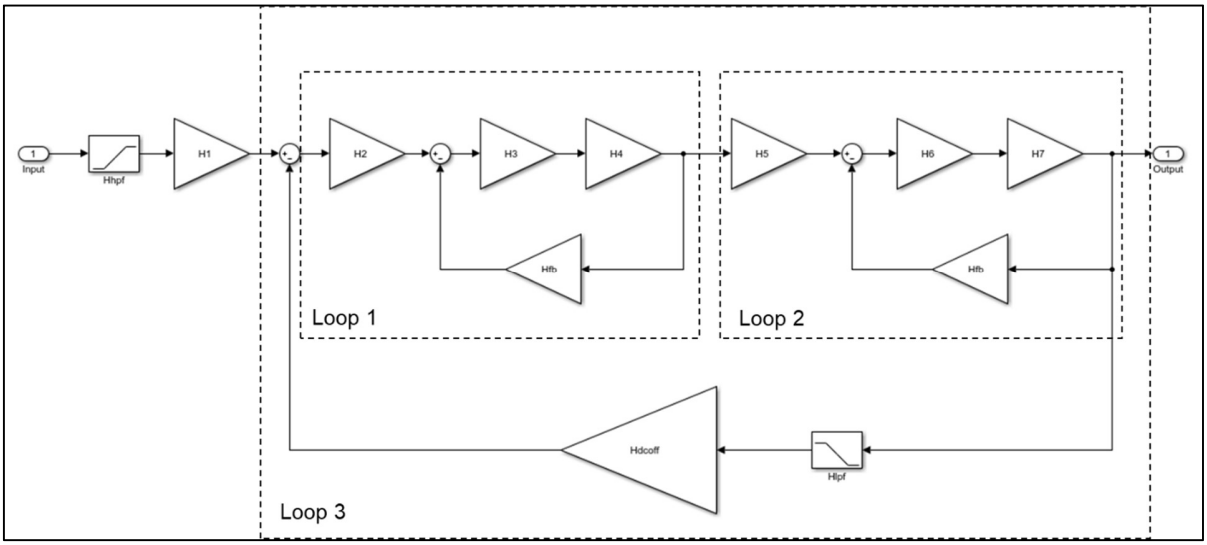

Figure 5.15. The block diagram of the limiting amplifier with the feedback loops presented.

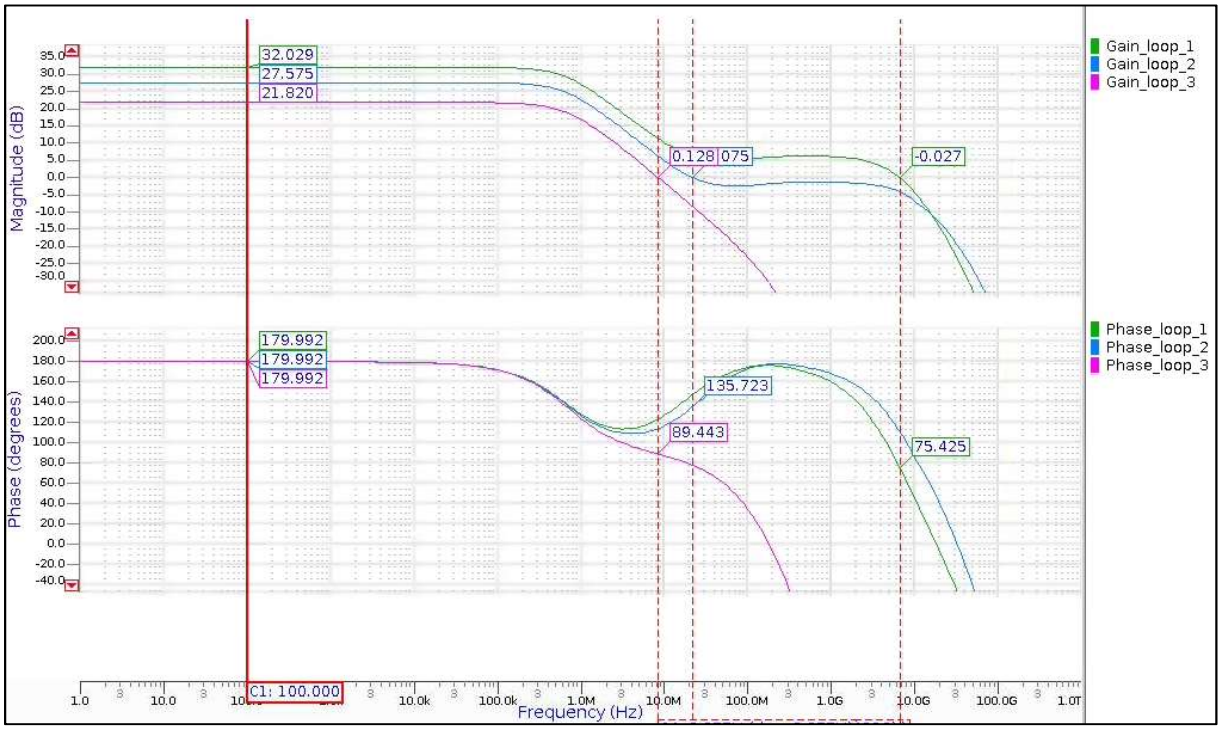

Figure 5.16. The loop stability simulations for the feedback loops presented in Figure 5.15. The upper window shows the gains of the loops (loop 1: green, loop 2: blue and loop 3: pink). The lower window shows the phases of the loops with the same color scheme.

The result of the phase margin of loop 1 as a function of the bias current is presented in Figure 5.17. At its lowest, the phase margin is about 48˚ with a bias current of 400 µA. This margin is still sufficient to keep the amplifier stable.

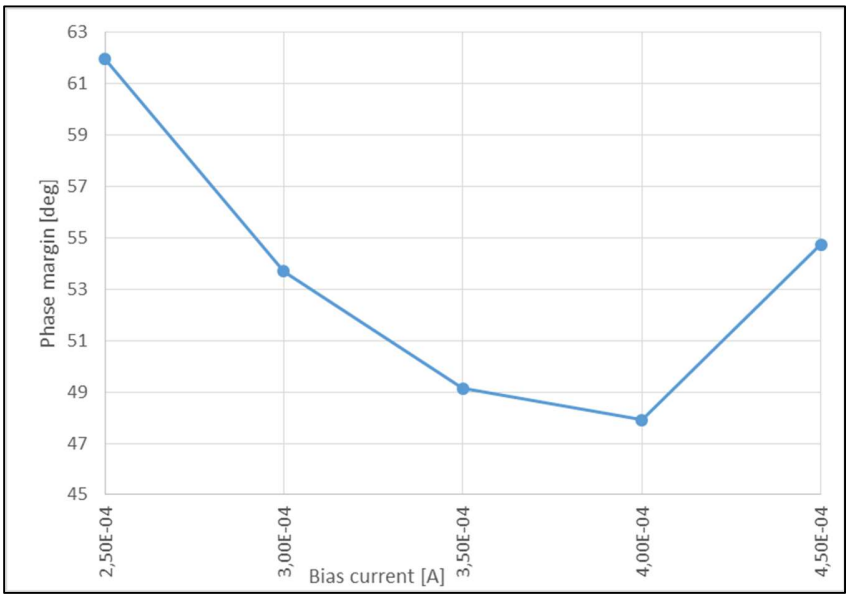

Figure 5.17. The gain margin for loop 1 as a function of the bias current.

The stability of loop 1 was also simulated in slow and fast corners. It was seen that the phase margin is at its lowest in the slow corner simulation, 52.6˚. In addition, the loop gain increased up to 39 dB. The bias current was lowered from the nominal value of 200 µA to 150 µA, and this resulted in the improvement of the phase margin to over 70˚ as seen in Figure 5.17.

From the differential mode loop stability simulations, it can be concluded that the phase margin does not approach zero in any conditions. In addition, in conditions where the limiting amplifier might become unstable, the stability can be regained by varying the bias point.

A similar loop stability simulation was done concerning the common mode stability. Differential amplifiers should naturally have a good common-mode rejection ratio, and this is also seen in the simulation results shown in figure 62. The maximum common mode gains for loops 1, 2 and 3 are -26.4 dB, -29.8 dB and -52 dB, respectively. Since the gains are clearly under 0 dB in all frequencies up to 1 THz, the common mode stability of the loops is inherent.

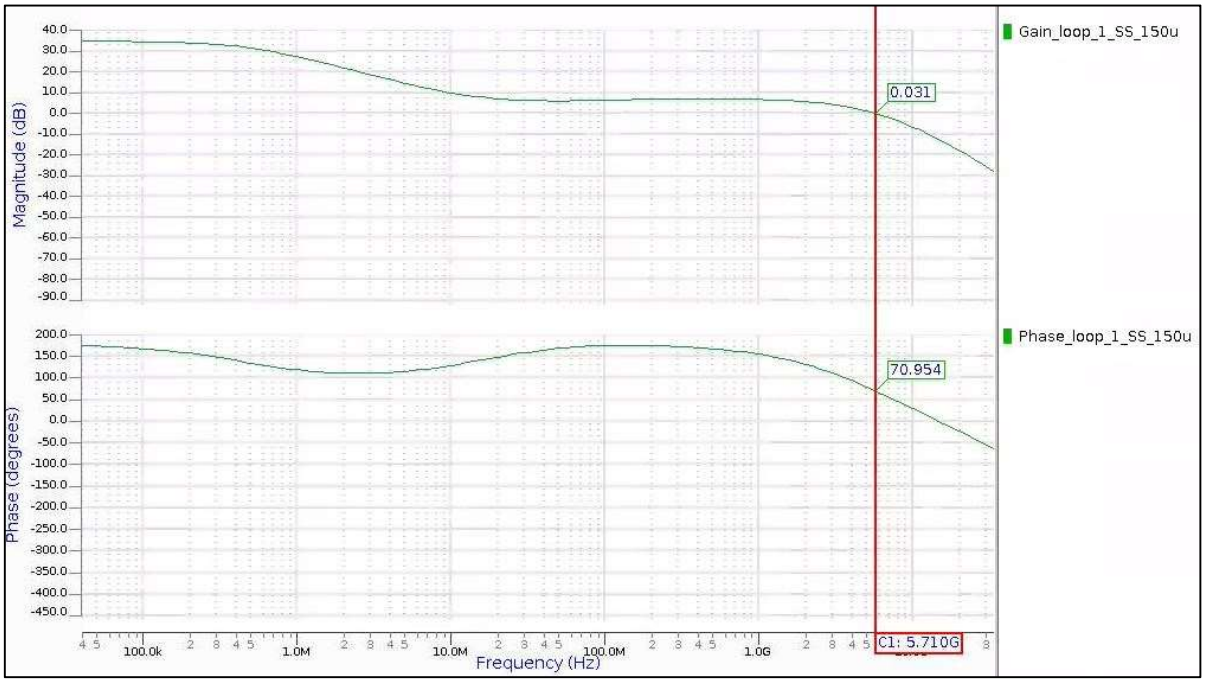

Figure 5.18. The loop stability simulation for loop 1 in slow process corner with a bias current of 150 µA.

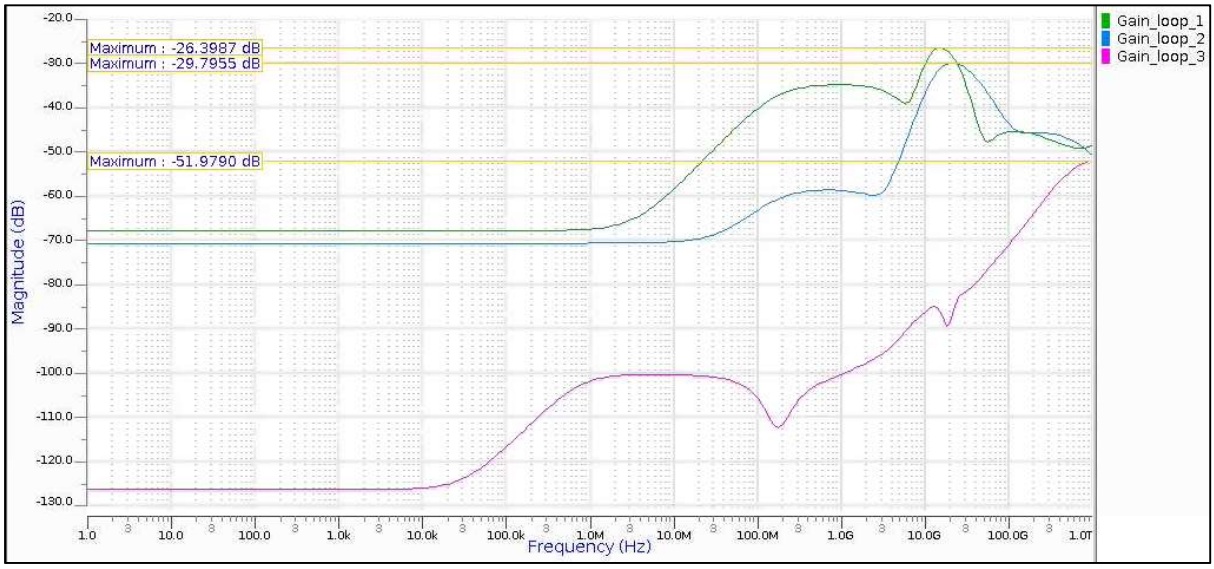

Figure 5.19. The common-mode loop stability simulations for feedback loops of Figure 5.15 (loop 1: green, loop 2: blue and loop 3: pink).

Another simulation was performed to verify the stability of the limiting amplifier; a quick disturbance signal was fed in a single-ended fashion to one of the internal nodes of the amplifier.

Figure 5.20 shows the resulting output signal (upper plot) and the voltage at the node where the disturbance is fed (lower plot). It is seen that the amplitude of the output does not change dramatically due to the disturbance, and the settling time is under 0.1 ns.

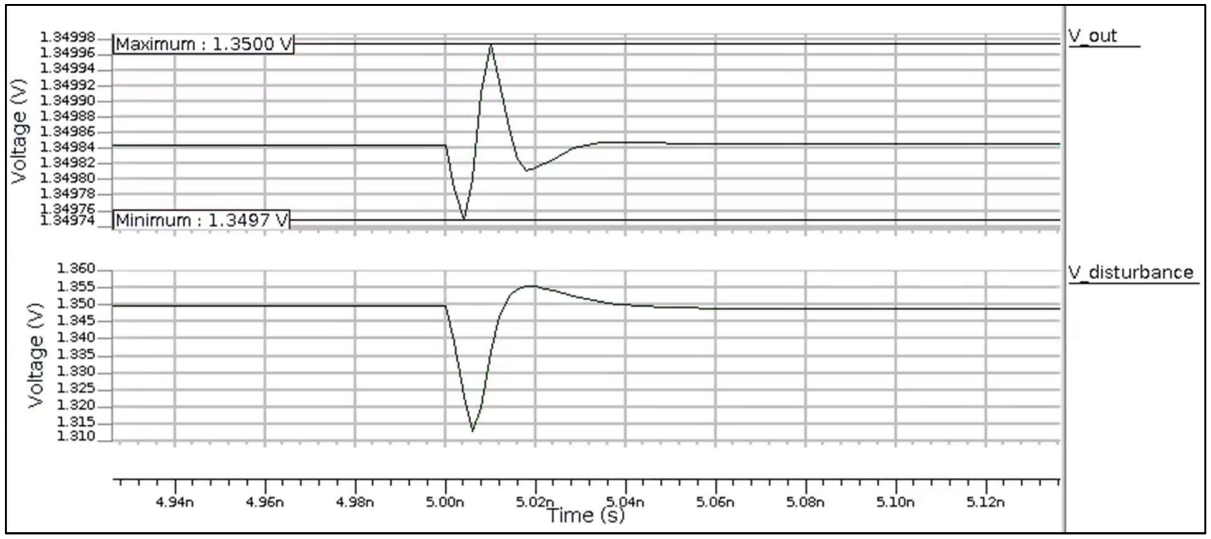

Figure 5.20. The output voltage settling (V_out, upper plot) with a disturbance signal (V_disturbance, lower plot) fed to one signal path of the amplifier.

5.5 DC offset cancellation and common-mode rejection

The effect of the DC offset cancellation circuit was simulated with the schematic of the design. A DC voltage source with a value of 30 mV was inserted in one of the input signal paths after the high pass filter, as shown in Figure 5.21. By inserting the offset voltage in this node, only the effect of the low-pass filter feedback path would show in simulations.

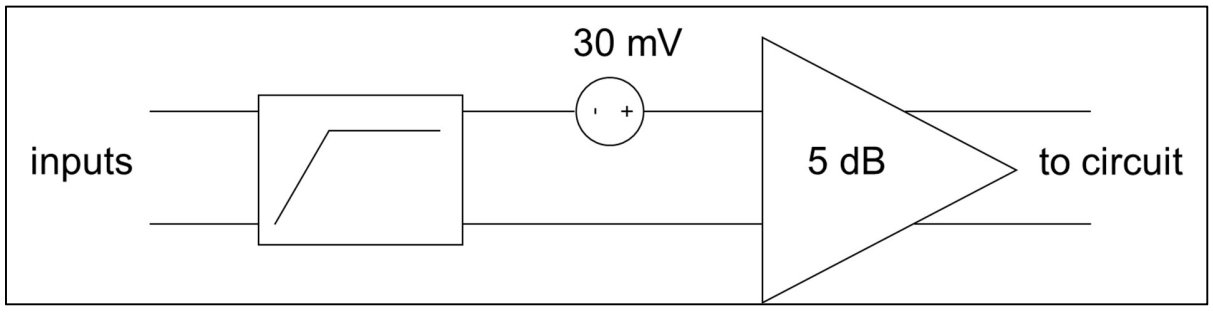

Figure 5.21. A part of the schematic circuit to simulate the effect of the DC offset cancellation circuit. A DC voltage of 30 mV is fed to one signal path.

The simulations were conducted with the low-pass filter enable bit high and low. Table 5.2 lists the results of these simulations. The DC level of the amplifier's outputs are measured. As the results in Table 5.2 show, the DC offset cancellation circuit works as designed; with the cancellation circuit enabled, the outputs only have a DC voltage difference of 80 mV. When the cancellation circuit is disabled, the DC voltage difference between outputs is almost 400 mV with the other output saturated to the operating voltage 1.35 V.

Table 5.2. The effect of the DC offset cancellation circuit to the DC offset voltage seen at the output of the limiting amplifier.

LPF_ENABLE	DC at output 1 [V]	DC at output 2 [V]	Difference [V]
1	1.21	1.13	0.08
0	1.35	0.951	0.399

In Figure 5.22, the upper plot presented the saturation of the output in the time domain, when the DC offset cancellation is not enabled, and the lower plot shows how the circuit fixes the DC level, when it is on.

The common-mode rejection of the amplifier was simulated by feeding the high-pass filter's input with a common-mode signal and examining the resulting response at the outputs of the first gain cell. A Monte-Carlo simulation was conducted to find the worst-case scenario. The resulting common-mode rejection ratio was 40 dB at highest, corresponding to a magnitude of 10000, which is a very satisfying result.

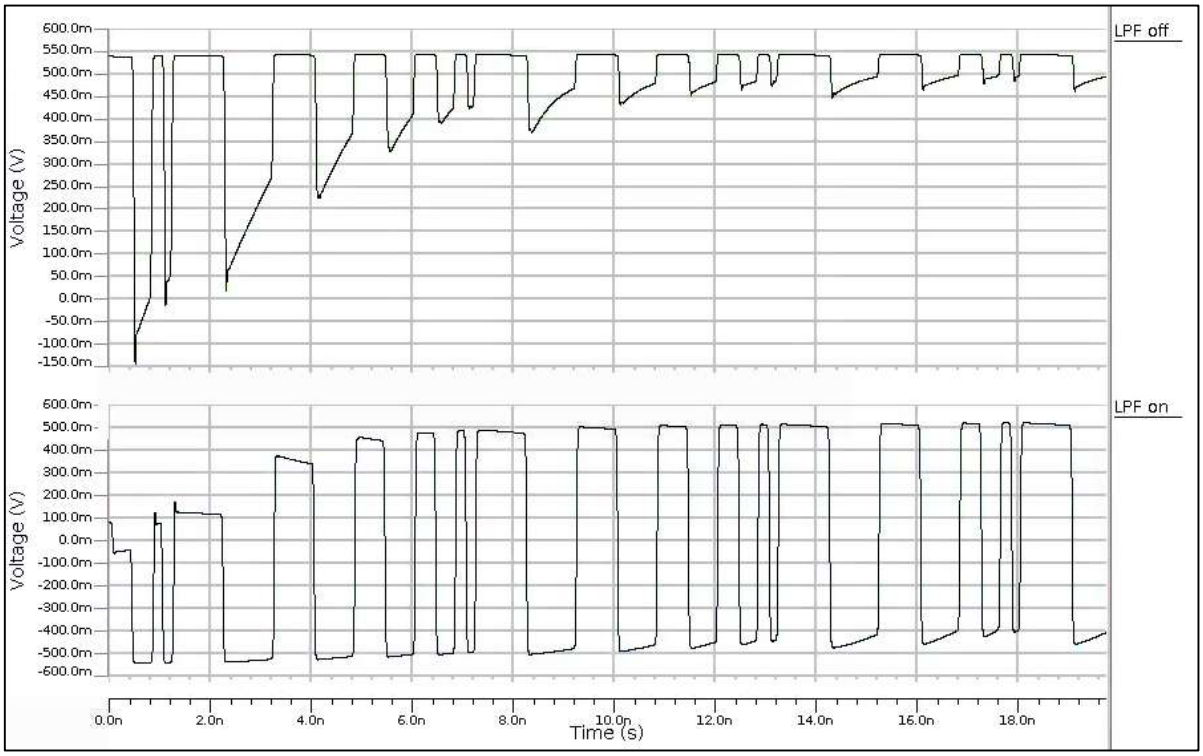

Figure 5.22. The transient simulation results of the output voltage with the DC offset cancellation circuit disabled (upper plot) and enabled (lower plot).

5.6 Noise

The contribution of the limiting amplifier to the noise figure of the receiver was determined by simulating the amplifier noise with no other noise sources. Figure 5.23 shows the simulated input-referred noise plot. The average input-referred noise obtained in the band between 30 MHz and 10 GHz is 2.94 $\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$.

The impedance level of the amplifier is 150 Ω, hence the resulting noise power generated by the amplifier, calculated with equation (2.20) is

$$P_{\mathrm{no}} = \frac{\left(2.94\ \frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}\right)^2}{150\ \Omega} = 57.624\ \cdot 10^{-21}\,\frac{\mathrm{W}}{\mathrm{Hz}}$$

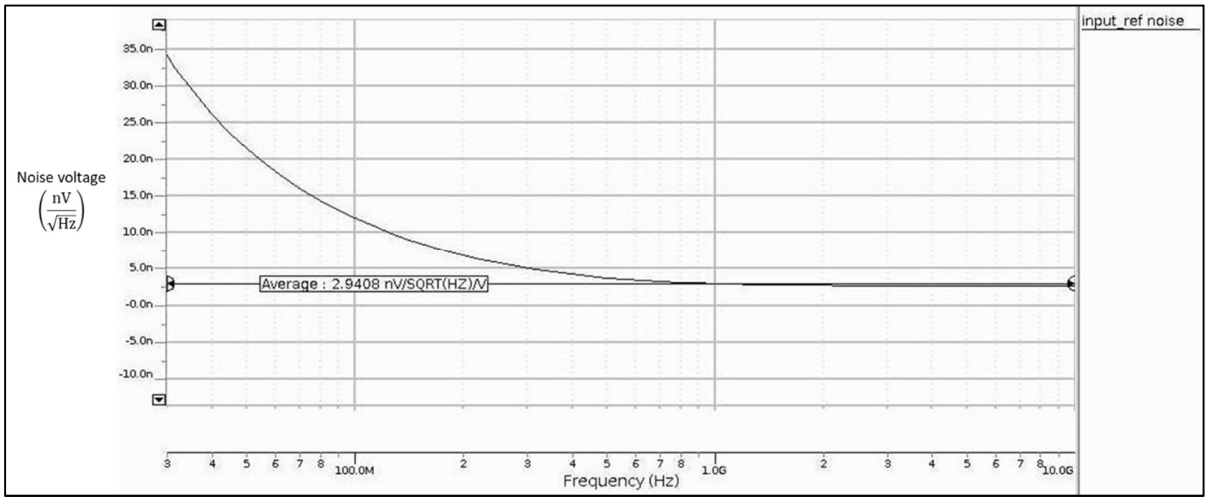

Figure 5.23. The simulated input-referred noise of the limiting amplifier.

The thermal noise normalized to one hertz is

$$P_{\mathrm{ni}} = 1.38 \cdot 10^{-23} \frac{\mathrm{J}}{\mathrm{K}} \cdot 300\ \mathrm{K} \cdot \frac{9.97\ \mathrm{GHz}}{9.97\ \mathrm{GHz}} = 4.14 \cdot 10^{-21} \frac{\mathrm{W}}{\mathrm{Hz}},$$

which is calculated with equation (2.19) and divided with the bandwidth. The resulting noise figure of the limiting amplifier, calculated with equations (2.17) and (2.21), is

$$F_{\mathrm{n,la}} = \frac{P_{\mathrm{no}}}{P_{\mathrm{ni}}} = \frac{276.23 \cdot 10^{-21}\ \frac{\mathrm{W}}{\mathrm{Hz}}}{4.14 \cdot 10^{-21}\ \frac{\mathrm{W}}{\mathrm{Hz}}} = 13.92$$

$$NF_{\mathrm{la}} = 10 \cdot \log_{10} 13.92 = 11.44\ \mathrm{dB}$$

The noise figure target for the limiting amplifier is less than 20 dB, hence the obtained result is well within the target.

The output *SNR* of the limiting amplifier will be calculated with the minimum possible input voltage value, which is 5 mV. With this input amplitude value, the output amplitude according to the results of Figure 5.6 is about 370 mV. The average output noise voltage in the band from 30 MHz to 10 GHz is 81.34 $\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$. The root mean square value of the output signal amplitude is used in the output power calculation, hence the *SNR* calculated with equation (2.24) is

$$SNR = \frac{P_{\text{out}}}{P_{\text{no}}} = \frac{\frac{v_{\text{out}}^2}{\sqrt{2}} \cdot \frac{1}{Z}}{v_{\text{n}}^2 \cdot \frac{1}{Z}} = \frac{\frac{(370\ \text{mV})^2}{\sqrt{2}} \cdot \frac{1}{150\ \Omega}}{\left(81.34\ \frac{\text{nV}}{\sqrt{\text{Hz}}}\right)^2 \cdot \frac{1}{150\ \Omega}} \cdot \frac{1}{9.97\ \text{GHz}} = 1.04 \cdot 10^3 \equiv 30.16\ \text{dB}$$

The resulting *SNR* corresponds well to the required minimum output *SNR* of 20 dB.

6 CONCLUSIONS

A limiting amplifier for the baseband of a millimetre-wave frequency band receiver was designed and verified with simulations in this thesis. The targets for the limiting amplifier were set in the introduction of the thesis, and Table 6.1 lists the required and simulated values of the most substantive parameters.

Table 6.1. The comparison of the required and simulated values for the amplifier.

Parameter	**Requirement**	**Simulated**
Maximum midband gain	30 dB	30.7 dB
Lower -3-dB frequency	20 – 70 MHz	37 MHz
Upper -3-dB frequency	10 GHz	11.4 GHz
Noise figure	< 20 dB	11.44 dB
SNR	> 20 dB	30.16 dB

The results of Table 6.1 show that the simulated values correspond well to the required values. A parasitic extraction was made for the top level of the amplifier, which was then used in the simulations. The simulation results indicate that in addition to achieving the required performance, the challenge of keeping the LA topology as simple and compact as possible was overcome. In addition to nominal conditions, the simulations were done in extreme conditions such as process corners and varying temperatures. These simulations show that the LA performance is still sufficient for the receiver's overall operation.

In the time frame of writing this thesis, no empirical results were possible to obtain by measuring the design. However, the simulation models of the design tool used are very accurate up to few tens of gigahertz, which should be more than enough for the frequency range required from the LA. Hence, it is assumed that the measured performance of the limiting amplifier will correspond well to that simulated.

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APPENDIX 1. A comparison of active and passive feedback.

The ideal model of the active feedback circuit is presented in Figure A.1. It includes voltage-controlled current sources g_{m1} and g_{mfb}. In the common node with voltage v_e, there is a resistance to ground with value R_e through which a current i_e flows.

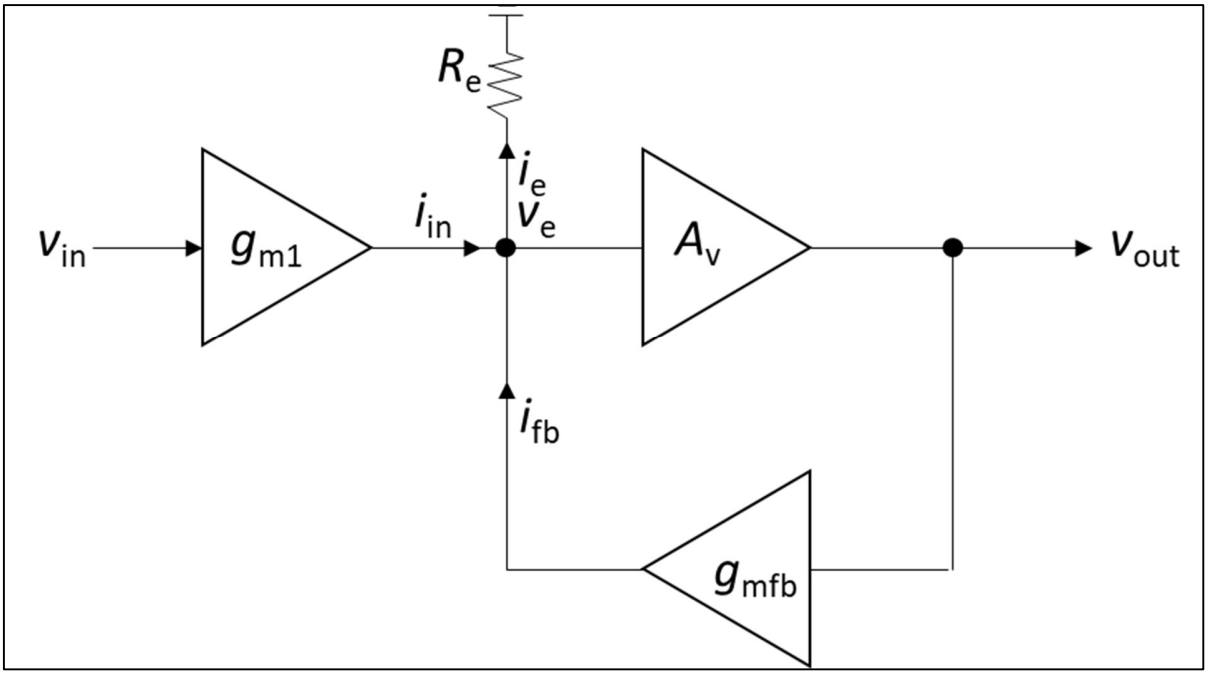

Figure A.1. The circuit to derive the transfer function v_{in}/v_{out} for active feedback with voltage-controlled current sources g_{m1} and g_{mfb}.

The derivation of the transfer function of output voltage versus input voltage is as follows:

$$i_{\mathrm{in}} = v_{\mathrm{in}} \cdot g_{\mathrm{m1}}$$
$$i_{\mathrm{fb}} = v_{\mathrm{out}} \cdot g_{\mathrm{mfb}}$$
$$i_{\mathrm{e}} = i_{\mathrm{in}} + i_{\mathrm{fb}}$$
$$v_{\mathrm{out}} = -v_{\mathrm{e}} \cdot A_{\mathrm{v}}$$

$$v_{\mathrm{e}} = i_{\mathrm{e}} \cdot R_{\mathrm{e}} = (i_{\mathrm{in}} + i_{\mathrm{fb}}) \cdot R_{\mathrm{e}} = v_{\mathrm{in}} \cdot g_{\mathrm{m1}} \cdot R_{\mathrm{e}} + v_{\mathrm{out}} \cdot g_{\mathrm{mfb}} \cdot R_{\mathrm{e}}$$
$$v_{\mathrm{out}} = -v_{in} \cdot g_{m1} \cdot R_e \cdot A_v - v_{out} \cdot g_{mfb} \cdot R_e \cdot A_v$$

(Continues)

$$\rightarrow v_{out} \cdot \left(1 + g_{mfb} \cdot R_e \cdot A_v\right) = -v_{in} \cdot g_{m1} \cdot R_e \cdot A_v$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1} \cdot R_e \cdot A_v}{1 + g_{mf} \cdot R_e \cdot A_v}$$

$$\rightarrow \frac{v_e}{v_{in}} = \frac{g_{m1} \cdot R_e}{1 + g_{mf} \cdot R_e \cdot A_v}$$

The passive feedback model includes an input resistance with value R_{in}, a feedback resistance with value R_f and a fictitious resistance R_e from the common node to ground. The latter is for derivation purposes only and finally, its value is considered to be infinite (hence i_e will be zero). The circuit of the passive feedback is presented in Figure A.2.

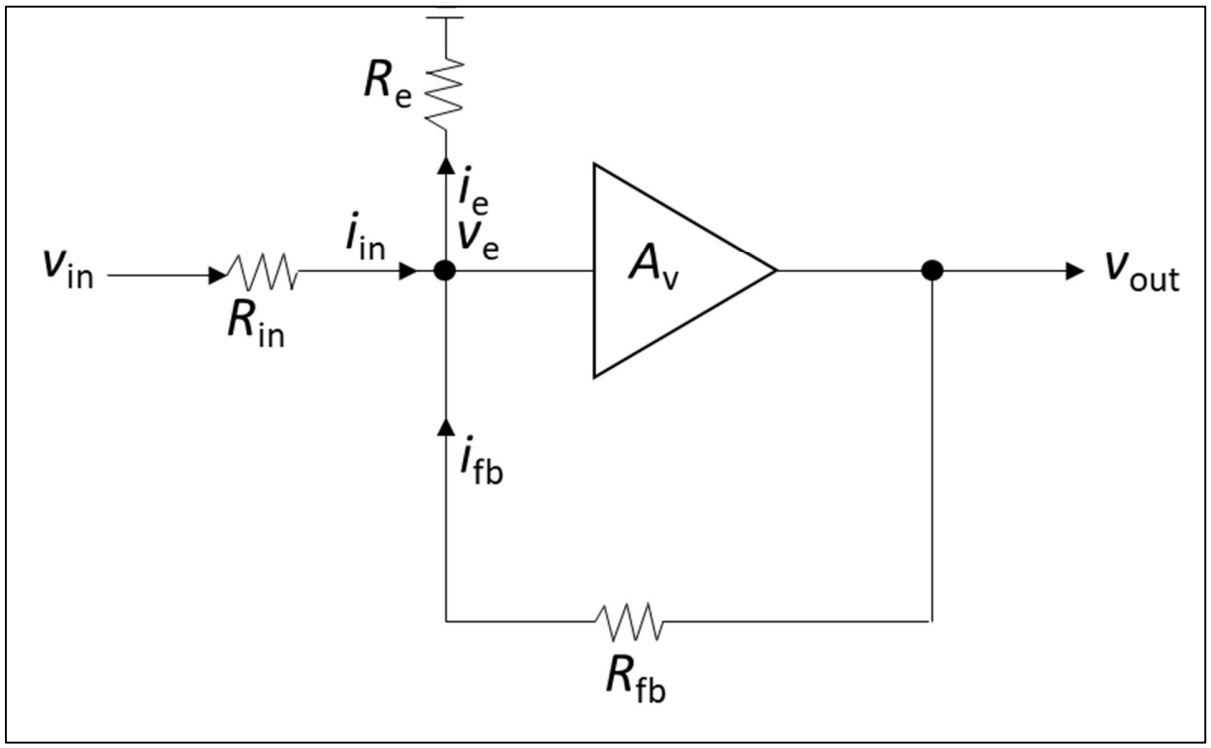

Figure A.2. The circuit to derive the transfer functions v_{in}/v_{out} for passive feedback with input resistance R_{in} and feedback resistance R_f.

The derivation of the transfer function of output voltage versus input voltage is as follows:

$$i_{in} = \frac{v_{in} - v_e}{R_{in}}$$

(Continues)

$$i_{fb} = \frac{v_{out} - v_e}{R_f}$$
$$v_e = i_e \cdot R_e$$
$$i_e = i_{in} + i_{fb}$$
$$v_e = -\frac{v_{out}}{A_v}$$

$$v_e = \frac{v_{in} - v_e}{R_{in}} \cdot R_e + \frac{v_{out} - v_e}{R_f} \cdot R_e$$
$$= v_{in} \cdot \frac{R_e}{R_{in}} - v_e \cdot \frac{R_e}{R_{in}} + v_{out} \cdot \frac{R_e}{R_f} - v_x \cdot \frac{R_e}{R_f}$$

$$v_e \cdot \left(1 + \frac{R_e}{R_{in}} + \frac{R_e}{R_f}\right) - v_{out} \cdot \frac{R_e}{R_f} = v_{in} \cdot \frac{R_e}{R_{in}}$$
$$\rightarrow v_{out} \cdot \left(-\frac{1}{A_v} - \frac{R_e}{R_{in}A_v} - \frac{R_e}{R_f A_v} - \frac{R_e}{R_f}\right) = v_{out} \cdot \frac{R_e}{R_{in}}$$
$$\rightarrow \frac{v_{out}}{v_{in}} = \frac{R_e}{R_{in}} \cdot \left(-\frac{R_{in} \cdot R_f \cdot A_v}{R_e \cdot R_{in} \cdot A_v + R_f \cdot R_{in} + R_f \cdot R_e + R_{in} \cdot R_e}\right)$$

Assuming $R_e \rightarrow \infty$

$$\rightarrow \frac{v_{out}}{v_{in}} = -\frac{R_f \cdot A_v}{R_{in} + R_f + R_{in} \cdot A_v}$$
$$\rightarrow \frac{v_e}{v_{in}} = \frac{R_f}{R_{in} + R_f + R_{in} \cdot A_v}$$

Simulation values:

$$g_{m1} = g_{mfb} = 0.01$$
$$R_e = 200\ \Omega$$
$$A_v = \frac{2}{1 + \frac{s}{10 \cdot 10^9\ \frac{\text{rad}}{\text{s}}}}$$

(Continues)

These values result in a gain of -0.8 dB at low frequencies. For the passive feedback, A_v is the same and resistor values are chosen to achieve the same gain at low frequencies:

$$R_f = 5000\ \Omega$$
$$R_{in} = 2500\ \Omega$$

Figure A.3 shows the frequency response for the active feedback (blue line) and passive feedback (orange line). According to the result, the 3-dB point for active feedback is 8.2 GHz and for passive feedback 2.7 GHz.

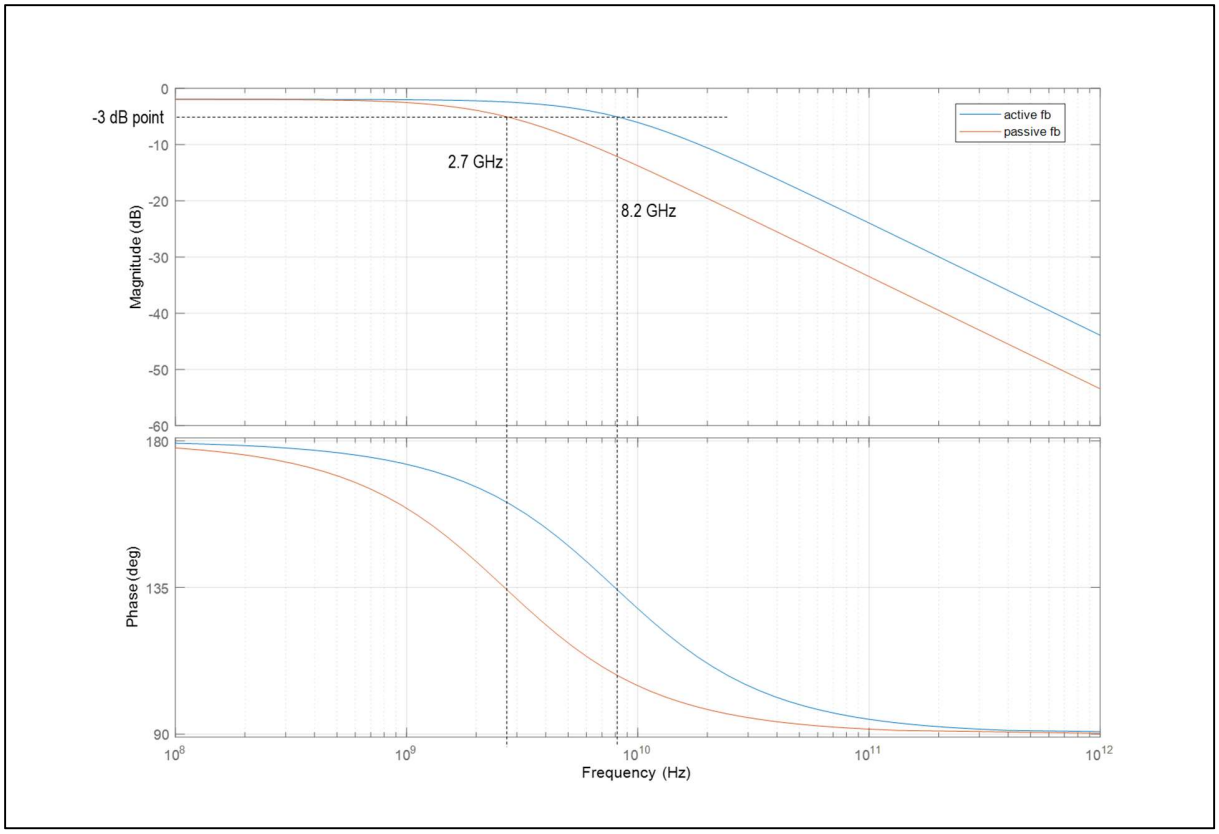

Figure A.3. The frequency response for the active (blue line) and passive (orange line) feedback.

In both active and passive feedback, the voltage at the common node (v_e in Figures A.1 and A.2) starts to increase at some frequency. Because the input current i_{in} of active feedback does not depend on v_e, this does not affect the frequency response. On the contrary, the passive feedback input current does depend on v_e, and it can be seen from the derivation of the transfer function that while v_e increases, the input current decreases. Figure A.4 shows plots for v_e/v_{in} both with active and passive feedback.

(Continues)

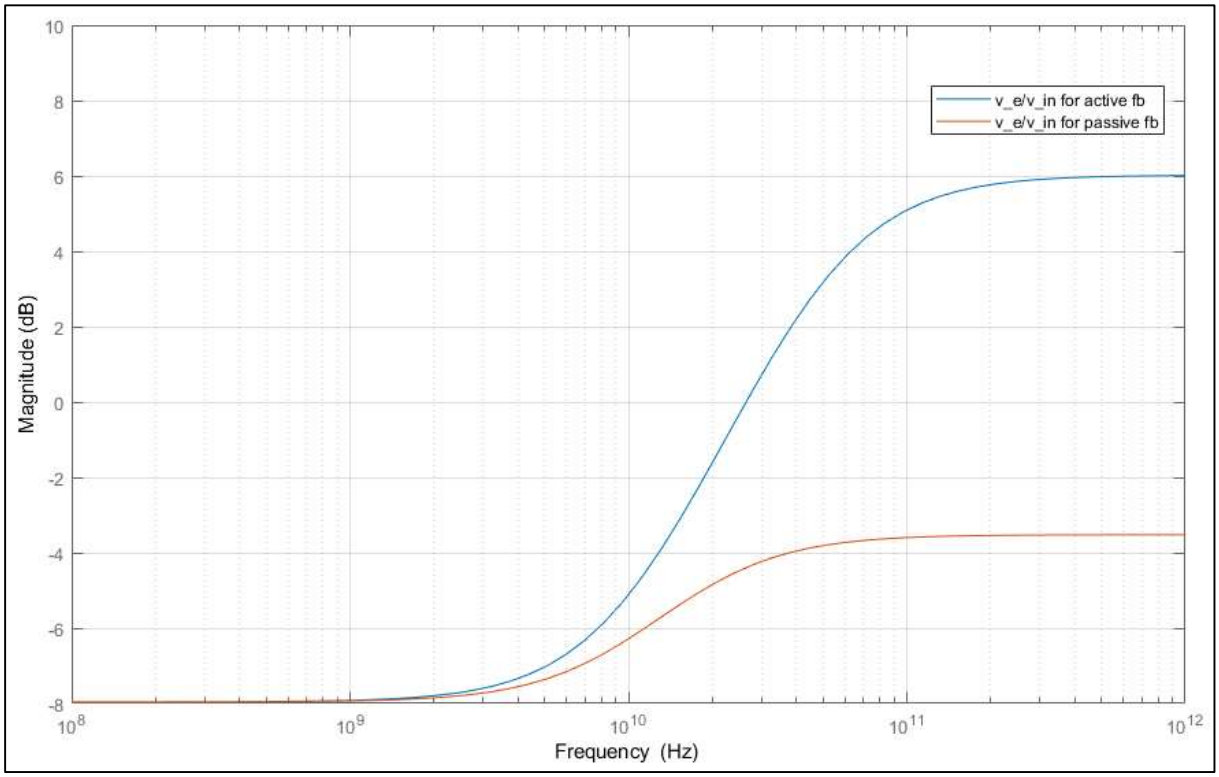

Figure A.4. The amplitude response of the common-node voltage v_e referenced to the input voltage v_{in} for the active feedback (blue line) and passive feedback (orange line).