Jani Hiltunen

IMPROVING THE DC-DC POWER CONVERSION EFFICIENCY IN A SOLID OXIDE FUEL CELL SYSTEM

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Abstract

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The solid oxide fuel cell (SOFC) is a promising technology for combined heat and power generation as it provides low local emissions, high efficiency, and fuel flexibility. However, the unique electrical characteristics of the SOFC present challenges for power conversion efficiency and system reliability. This doctoral dissertation addresses these challenges through the design and modulation of the DC-DC converter.

Safe and reliable operation of an SOFC requires a power conversion unit (PCU) that is capable of interfacing between the different voltage levels and controlling the output current of the fuel cell. The challenge is that the output voltage of an SOFC is dependent on the reactants feed and load current. This voltage-current dependence creates a need for a PCU capable of efficient power conversion with a wide voltage conversion ratio. Moreover, the SOFC is vulnerable to sudden changes in the load and reactants feed, which may arise in a case of an emergency shutdown of the SOFC system. The impacts of an unexpected shutdown can be reduced by applying reverse bias current to the fuel cell during the emergency shutdown. This directs interest to the research of bidirectional power converters and efficiency improvement for a wide voltage conversion ratio.

In this doctoral dissertation, two DC-DC converter topologies and their use in an SOFC system are studied—the objective of this work is to enable efficient bidirectional DC-DC power conversion under varying load conditions. The converter topologies studied are the current-fed resonant push-pull (RPP) and the dual active bridge (DAB). The traditional RPP topology is well suited for SOFC applications but is not capable of bidirectional operation. The DAB topology, however, is bidirectional by nature, but its conversion efficiency is heavily dependent on the input-output voltage conversion ratio and load current.

In this doctoral dissertation, the use of an RPP converter as a bidirectional converter is demonstrated. The power conversion efficiency of the DAB converter is improved by developing a variable-frequency modulation method. Further, the origin of the phase drift phenomenon is determined, a simple phase drift compensation method is developed, and a method for online efficiency maximization of the DAB converter is introduced.

Keywords: DC-DC converter, power conversion, modulation, soft-switching, SOFC

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Jani Hiltunen
August 2019
Tuusula, Finland

Contents

List of publications

This doctoral dissertation is based on the following papers. The rights have been granted by the publishers to include the papers in the dissertation.

I. Väisänen, V., Riipinen, T., Hiltunen, J. et al., 2011. Design of 10 kW resonant push-pull DC-DC converter for solid oxide fuel cell applications. In *Proceedings of the 14th European Conference on Power Electronics and Applications (EPE 2011)*, Birmingham, UK, pp. 1–10.

II. Hiltunen, J., Väisänen, V. & Silventoinen, P., 2013. A bidirectional current-fed resonant push-pull converter for low voltage, high current applications. In *Proceedings of IEEE Energy Conversion Congress and Exposition (ECCE)*, Denver, CO, pp. 4770–4774.

III. Hiltunen, J., Väisänen, V., Juntunen, R. et al., 2015., Variable-Frequency Phase Shift Modulation of a Dual Active Bridge Converter. *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7138–7148.

IV. Väisänen, V., Hiltunen, J. & Juntunen, R., 2015. Phase Drift Phenomenon in Dual Active Bridge Converter – Analysis and Compensation. *International Review of Electrical Engineering (IREE)*, vol. 10, no. 1, pp. 1–11

V. Väisänen, V. & Hiltunen, J., 2015., Maximum efficiency point tracking algorithm for dual active bridge converters, In *Proceedings of IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, pp. 623–629.

Author's contribution

In Publication I, Mr. Hiltunen was the coauthor responsible for the derivation of the equation for component RMS current calculation and the equation for the ripple-based selection of the input inductor. Mr. Hiltunen was responsible for the construction of the laboratory prototype of the experimental setup. Mr. Hiltunen also contributed to the component dimensioning and analysis of the empirical results. Dr. Väisänen was the principal author responsible for the magnetic component design, component dimensioning, and simulations. Dr. Riipinen was in charge of the control system of the experimental setup. The empirical experiments were conducted in collaboration with the authors.

In Publication II, Mr. Hiltunen was the principal author of the paper and the main contributor to its scientific content. Mr. Hiltunen developed the modulation principle, constructed the laboratory prototype, and executed empirical experiments and simulations. Dr. Väisänen participated in the commenting of the paper.

In Publication III, Mr. Hiltunen was the principal author of the paper and the main contributor to its scientific content. Mr. Hiltunen developed the modulation algorithm and analyzed the phase drift phenomenon, dead time, and back commutation. Mr. Hiltunen also constructed the laboratory prototype, executed the empirical experiments, and analyzed the results. Dr. Väisänen provided help with the analysis of the phase drift phenomenon and the technical presentation of the paper. Dr. Juntunen participated in the commenting of the paper.

In Publication IV, Mr. Hiltunen was the coauthor responsible for the development and analysis of the controller-based compensation method. Mr. Hiltunen also contributed to the development of the charge-based compensation method and analysis of the experimental results. Dr. Väisänen was the principal author responsible for the development of the charge-based compensation method and the execution of the empirical experiments. Dr. Juntunen participated in the commenting of the paper.

In Publication V, Mr. Hiltunen was the coauthor inventing together with Dr. Väisänen the concept of the online efficiency maximization of the DAB converter by applying variable-frequency modulation. Mr. Hiltunen constructed the laboratory prototype, illustrated the theoretical waveforms of the dual active bridge converter, and contributed to the analysis of the results. Dr. Väisänen was the principal author responsible for the empirical experiments and the loss distribution analysis.

Nomenclature

Latin alphabet

C	Capacitance	F
D	Duty cycle	%
d	Control variable	–
f	Frequency	Hz
I, i	Current	A
k	Number of switching components	–
L	Inductance	H
n	Transformer turns ratio	–
P	Active power	W
Q	Electrical charge	C
S	Transistor	–
t	Time	s
V	Voltage	V

Greek alphabet

α	(alpha)
β	(beta)
γ	(gamma)
Φ	(phi)

Subscripts

A	Primary-side first leg
B	Primary-side second leg
bridge	H-bridge
c	Clamp
DC	Direct current
dead	Dead time
delay	Time delay
drift	Phase drift
DS	Drain-source
eff	Efficiency
in	Input
L	Inductor
lk	Leakage
max	Maximum
O	Output
out	Output
pri	Primary
r	Resonance

ref	Reference
S	Secondary
S	Secondary-side switch
sec	Secondary
sw	Switching
ZVS	Zero-voltage switching

Abbreviations

AC	Alternating current
BJT	Bipolar junction transistor
CHP	Combined heat and power
DAB	Dual active bridge
DC	Direct current
DPS	Dual phase shift
EMC	Electromagnetic compatibility
EPS	Extended phase shift
FB	Full-bridge
HB	Half-bridge
ICCP	Impressed current cathode protection
IGBT	Insulated-gate bipolar transistor
MEPT	Maximum efficiency point tracking
MOSFET	Metal-oxide-semiconductor field-effect transistor
MPPT	Maximum power point tracking
MPS	Multi-phase shift modulation
OCV	Open circuit voltage
OTM	Optimal transition mode
P&O	Perturb-and-observe
PCU	Power conversion unit
PI	Proportional–integral controller
PSM	Phase shift modulation
PV	Photovoltaic
RMS	Root mean square
RPP	Resonant push-pull
SiC	Silicon carbide
SOFC	Solid oxide fuel cell
SPS	Single phase shift
TCM	Triangular current mode
TPS	Triple phase shift
TZM	Trapezoidal current mode
VFM	Variable-frequency modulation
ZCS	Zero-current switching
ZVS	Zero-voltage switching

1 Introduction

A fuel cell is a device that converts chemical energy directly into electrical energy by chemical reaction. The operating principle of a fuel cell is thus quite different compared with a combustion engine that burns the fuel and uses the expansion of gases to do mechanical work. Because of the fundamentally different operating principle, fuel cells have significant advantages over combustion engines. The fuel cell does not require any moving parts, and it can, therefore, operate silently. Moreover, fuel cells have low local emissions and a higher efficiency than internal combustion engines. Fuel cells are used for a wide range of applications, such as automotive and transportation, uninterruptible power supplies, power backup, heat and power generation, and portable applications. A fuel cell can also be operated in the reverse mode as an electrolyzer to produce hydrogen from water and oxygen. An electrolyzer makes it possible to convert surplus electricity from renewable sources, such as wind and solar, to chemical fuel for storage. Therefore, a fuel cell can help to release the full potential of renewable energy sources.

A fuel cell is an old invention. The operating principle of the fuel cell was first theorized in 1838 by Christian Schönbein, and later, Sir William Grove conducted experiments with a fuel cell (Sasaki et al., 2016). A fuel cell consists of two electrodes and an electrolyte, as shown in Figure 1.1. The electrolyte carries positively charged ions between the anode and the cathode. Electricity in a fuel cell is generated by passing fuel to the anode and oxidant to the cathode. The oxidation reaction at the anode splits the hydrogen molecules into electrons and positively charged ions (protons). The electrolyte carries the electrically charged ions from the anode to the cathode. When electrodes are connected to the load, electrons start to flow from one electrode to another, and the chemical energy is converted into electrical energy. Electrons returning from the electrical circuit will react with ions that have traveled through the electrolyte and the oxidant that is fed to the cathode.

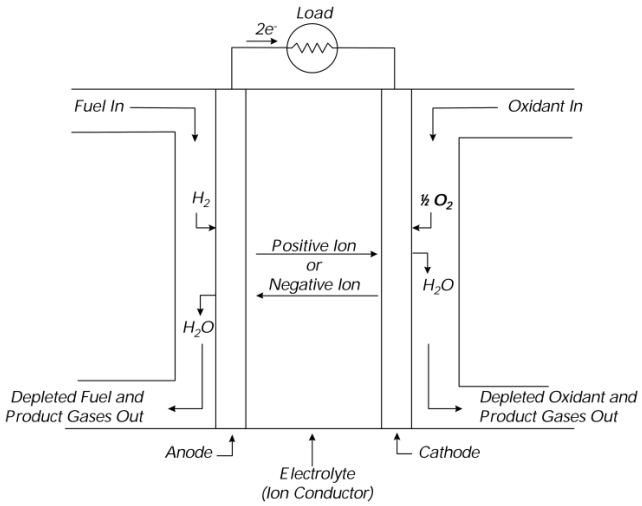


Figure 1.1: Operating principle of the fuel cell (Hirschenhofer et al., 1998).

Hydrogen is the primary fuel for fuel cells, but hydrogen can be generated from other hydrocarbons by reforming. Therefore, a fuel cell equipped with a fuel reformer can use various fuels such as hydrogen, natural gas, methanol, ethanol, landfill gas, and other hydrocarbon fuels. The drawback of fuel reforming is that it leaves impurities, which degrade the performance and durability of the fuel cell. The effects of impurities on fuel cells have been studied for instance in (Yan et al., 2009), (Tewari et al., 2006), and (Chin & Howard, 1986). Some fuel cell types are more tolerant of impurities than others. One such fuel cell type is the solid oxide fuel cell, which has been found to be relatively tolerant of fuel impurities (VTT, 2010). The fuel stream of the SOFC does not have to be as clean of impurities as other fuel cell types (Penner, 1986).

1.1 Solid oxide fuel cell

A solid oxide fuel cell (SOFC) is a high-temperature fuel cell that uses a solid ceramic compound as an electrolyte. SOFCs typically operate at temperatures above 700 °C (Halinen, 2015). Because of the high temperature, no precious metals are needed for catalysis. The high temperature also makes the SOFC capable of internal reforming, which makes it flexible for various fuels. The SOFC can internally reform any mixture of hydrogen, carbon monoxide, and methane (McPhail et al., 2012). One of the advantages of the SOFC is that the high-temperature exhaust gas can be used for heating or converting water into steam. This makes the SOFC an interesting technology for stationary combined heat and power (CHP) generation applications.

The fuel into electricity conversion efficiency of the SOFC can reach over 60% (Peters et al., 2016). If the waste heat is captured, the overall efficiency can rise above 80% (Oates et al., 2002), (Fontell et al., 2004). This is an impressive value when compared with the traditional combustion engine, which typically has a thermal efficiency of less than 50% (Haifeng et al., 2018).

The high temperature of the SOFC is the enabler of many of its key benefits. However, the high temperature poses some significant technical challenges as the materials must be heat resistant. The elevated temperature also complicates the electrical isolation of the solid oxide fuel cell stack. This is one of the reasons for the unique nature of the SOFC as an electrical power source.

1.2 SOFC as an electric power source

The solid oxide fuel cell (SOFC) is not an ideal DC source. The output voltage of an SOFC is dependent on the load current and feed of fuel and oxidants. The theoretical voltage difference between the anode and cathode of an SOFC when no current is drawn from the cell can be calculated with the Nernst equation (Halinen, 2015). This oxidation potential, or open-circuit voltage (OCV), depends on the temperature and partial pressures of the reactants, and for a solid oxide fuel cell, it is about 1 V (Larminie & Dicks, 2003). The low voltage generated by a single fuel cell is not sufficient for most

applications. Therefore, individual fuel cells are generally not used as such but instead as a series connection of several individual cells, constituting a configuration called a fuel cell stack. Unfortunately, owing to material and structural limitations, individual cells cannot be stacked up infinitely. A higher voltage requires better electrical isolation, which is difficult to achieve in a high-temperature environment as in the SOFC. Further, the physical structure of the stack sets certain limitations. Efficient operation of the stack requires a uniform temperature and fuel distribution (Tallgren et al., 2017), which presents challenges when the fuel cell stack is large. For these reasons, the number of cells in a commercial stack is quite low, typically around one hundred cells or less, as can be seen in Table 1.1.

Table 1.1: Some of the commercially available SOFC stacks.

	Cells	Rated power	Reference
Elcogen E1000	39	1 kW	(Elcogen, 2019)
Elcogen E3000	119	3 kW	(Elcogen, 2019)
SOFCMAN-ASC 60	60	1.6–2.0 kW	(SOFCMAN, 2019)
SOFCMAN-ASC 30	30	2–2.2 kW	(SOFCMAN, 2019)

When current is drawn from the fuel cell, the voltage drops from the open-circuit voltage as a result of losses, which can be categorized as activation, ohmic, and mass-transfer losses. When a small current is drawn from the cell, the voltage decreases as a result of activation losses at the electrodes. Activation losses are minimal at high temperatures and are therefore not as significant in the SOFC as in other fuel cells (Lin & Beale, 2006). When current is increased, the voltage drops linearly with the current because of the ohmic losses in the electrodes. The area of ohmic losses is the area where the fuel cell is typically operated. If the load current of the fuel cell is increased further, the voltage declines sharply as the fuel cell enters the mass-transfer region. In this region, the reactants are consumed faster than fresh reactants can be supplied and reaction products exhausted. The operation in the mass-transfer region can cause fuel starvation, which can lead to performance degradation and irreversible damage (Halinen, 2015), (Mazumder et al., 2004). The activation, ohmic, and mass-transfer losses give a fuel cell its characteristic voltage-current behavior, also known as the polarization curve, as shown in Figure 1.2.

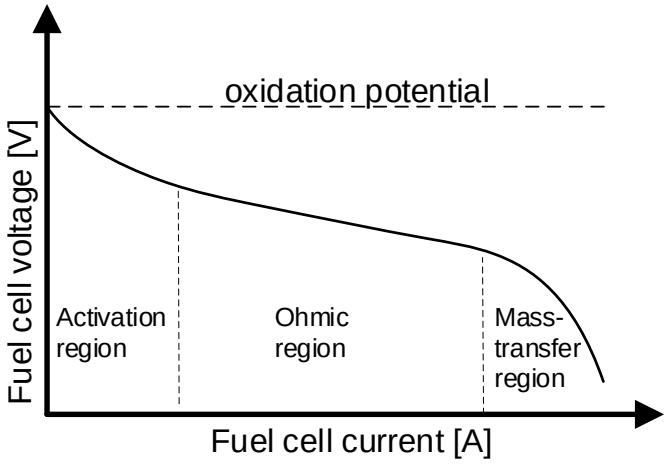


Figure 1.2: Voltage-current behavior of the fuel cell.

In principle, the SOFC is a DC voltage source, but its output voltage varies as a function of load current and reactants feed. As the output voltage of the SOFC is dependent on the reactants feed, its capability to react to load changes is limited by the process delays of the feed system. These delays are typically on the timescale of seconds (Mueller et al., 2009). If the electrical load of an SOFC is changed at a faster rate than at which the adjustments in the reactant feed can be made, the SOFC can enter the mass-transfer mode, which can cause irreversible damage. A sudden load change can also cause an uneven temperature distribution inside the fuel cell stack, which, in turn, can cause thermal fatigue (Mueller et al., 2009). While load changes can damage the SOFC, fast load transients (millisecond timescale) are not that harmful owing to the double-layer charging effect (Wang & Nehrir, 2007). The double-layer charging effect is caused by the electrode-electrolyte boundaries, which constitute a structure that stores energy and makes the SOFC behave like a supercapacitor on a millisecond timescale (Wang & Nehrir, 2007).

Because the voltage of SOFC is dependent on the load current and reactants feed, a system-level method is needed to control and limit its output power. One option is to adjust the reactants feed, as shown in the patent (Mufford & Strasky, 1998). However, the response time of the reactant feed control is limited by the time delays of mechanical actuators, valves, and pumps. The slow response to load changes makes this control method susceptible to fuel starvation. Another option is to use a current-controlled power conversion unit (PCU) to regulate the fuel cell current and limit the maximum allowed current, as shown in the patent (Lacy & Marvin, 1999).

The relatively low output voltage of the SOFC stack and the need for current regulation attract interest in power conversion unit that can boost up the voltage and regulate the current. In a grid-connected SOFC application, additional requirements are set for the PCU by the distribution grid (Riipinen et al., 2011). Therefore, a typical PCU is

constructed from a DC-DC converter and a DC-AC inverter. The DC-DC converter boosts up the low voltage of the SOFC, regulates the current, and provides protection for the cell stack by limiting the load current as needed. Often, a galvanically isolated DC-DC converter is preferred owing to its capability to break the ground loop between the fuel cell and the load, thus protecting the fuel cell from load-side faults. The galvanic isolation also limits the harmful effects caused by the grid-inverter-generated common-mode currents (Gemmen et al., 2003). Moreover, the transformer used for galvanic isolation provides an opportunity to step up the voltage level by adjusting the transformer turns ratio.

While the current-controlled DC-DC converter can provide some protection for the SOFC, several other methods have been presented to protect the SOFC against sudden events, such as an emergency shutdown, fuel shortages, or sealing damage. These methods include inert gas purging (Li et al., 2012) and anode gas recirculation (Halinen et al., 2014). Recently, a protection method using reverse bias current to protect the anode of the SOFC has been studied in (Brunaccini et al., 2017). The study showed promising results for this impressed current cathode protection (ICCP) scheme. The proposed protection system, shown in Figure 1.3, consists of two power conversion units: one interfacing with the load and the other generating the reverse current for protection. The additional power conversion unit increases the complexity and cost of the system. This raises interest in the use of a bidirectional power converter in an SOFC system. A bidirectional DC-DC converter could serve both functions: load interfacing and anode protection. This would potentially reduce the size and cost of the system.

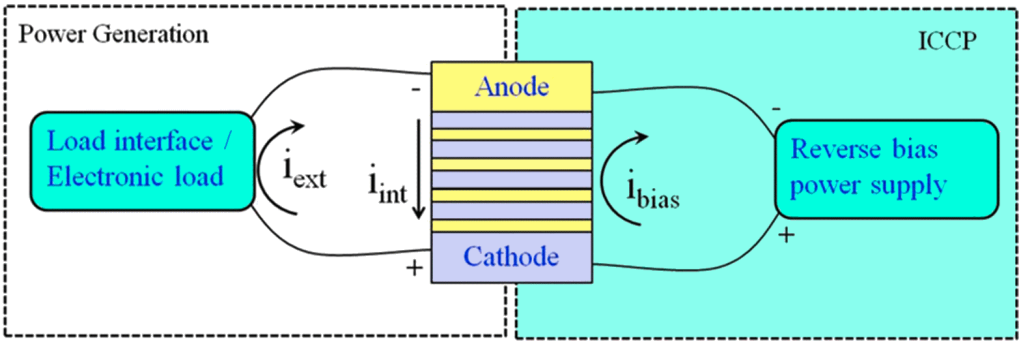


Figure 1.3: Schematic of a fuel cell in power generation and reverse bias application (Brunaccini et al., 2017).

1.3 Motivation of the work

The fuel cell is a technology that could play an essential role in the power generation of the nearly emission-free society of the future. Renewable energy sources, such as solar and wind, cannot produce energy around the clock. Moreover, a significant increase in renewable energy generation requires a method to store energy. The fuel cell is a potential answer to this need. A fuel cell can be used as an electrolyzer to convert the surplus electricity from renewable energy sources to hydrogen. The hydrogen can be stored, transported, and later converted back into electricity with a fuel cell. Furthermore, fuel-flexible fuel cells, such as the SOFC, enable the use of biogas from landfills and wastewater treatment plants to be converted into electricity and heat.

In order to utilize the full potential of fuel cells, an efficient power conditioning unit is needed to interface between the fuel cell and the load and to protect the fuel cell in a case of an emergency shutdown or a similar sudden event. Depending on the type of the load, the power conditioning unit may consist of only a DC-DC converter or have a DC-DC converter connected to a DC-AC converter. The output voltage of the SOFC is typically so low that a step-up DC-DC converter is needed, which attracts particular interest in the study of DC-DC converters in solid oxide fuel cell applications.

The unique nature of SOFC as a source for electric power source presents challenges for the design of a DC-DC-converter. One of the critical characteristics of an SOFC as an electrical power source is that its output voltage is dependent on the load current. This creates a need for a DC-DC-converter that can maintain a high power conversion efficiency throughout a wide voltage and power range. A low efficiency can reduce the converter reliability by the added thermal stress. It also increases the need for cooling and thereby increases the physical size of the system. Further, a low efficiency increases the costs of the system because of the energy lost in the conversion process. The energy that is lost in the conversion process could have been sold to the grid. Thus, an improvement in the power conversion efficiency has a direct impact on the investment payback time.

Another distinctive characteristic of the SOFC is its vulnerability to overloading. This creates a need for a power conditioning unit that can regulate and limit the load current. The power conditioning unit must also be able to protect the fuel cell stack from the dangers of sudden load-side faults. Therefore, galvanic isolation is preferred. In a case of an emergency shutdown the ability to protect the SOFC with the reverse bias current is highly preferable.

The unique characteristics of the SOFC provide an interesting framework for the study of galvanically isolated bidirectional DC-DC converters. Two converter topologies have raised a lot of research interest in the realm of isolated DC-DC power conversion: the current-fed resonant push-pull (RPP) and the dual active bridge (DAB). The RPP has many desirable qualities for an SOFC application but is unidirectional and therefore not directly suited for anode protection purposes. The DAB, on the other hand, is bidirectional

by nature, but is efficiency is heavily dependent on the input-output voltage conversion ratio and the transferred power.

1.4 Objective and scope of the work

The objective of this doctoral dissertation is to investigate two preselected DC-DC converter topologies and to study the opportunities to improve their power conversion efficiency and suitability for solid oxide fuel cell applications. The work is focused on modulation methods and the use of these converters for bidirectional power transfer.

The topic of this doctoral dissertation is the DC-DC power conversion in the solid oxide fuel cell application and efficiency improvement. Part of this work touches on the subject of control design, but the control design and stability analysis are excluded from the scope of this work. The work is limited to the modulation method of two preselected topologies: the current-fed resonant push-pull (RPP) and the dual active bridge (DAB). It is not the objective of this work to compare these topologies with one another, but rather to make remarks on their advantages and disadvantages and improve their performance where possible. Further, evaluation and comparison of various other DC-DC converter topologies and their suitability for SOFC applications are out of the scope of this work.

The results of this work can be applied to various types of switching components. In this doctoral dissertation, however, the terms “switching component,” “switch,” or “transistor” will from here onwards refer specifically to the enhancement-mode N-channel metal-oxide-semiconductor field-effect transistor. The study of the unique aspects of other switching component types is out of the scope of this dissertation.

1.5 Summary of publications

This doctoral dissertation consists of five publications, which are listed in a chronological order. The first two of the publications study the current-fed resonant push-pull converter, and the last three are focused on efficiency improvement of the dual active bridge converter.

Publication I demonstrates and analyzes the operation of the current-fed resonant push-pull converter with a 10 kW laboratory prototype. The publication presents principles for component dimensioning and discusses the advantages and disadvantages of the current-fed resonant push-pull topology.

Publication II studies the use of a current-fed resonant push-pull converter for bidirectional operation. The publication presents the modulation principle and operating waveforms of the proposed converter in a reverse power mode. The publication demonstrates the operation in the reverse power mode with a 5 kW laboratory prototype.

Publication III introduces for the first time a variable-frequency modulation algorithm for a dual active bridge converter. The publication also explains the origins of the phase drift phenomenon and presents a method to estimate the magnitude of the phase drift. The publication also presents guidelines for selecting optimal values for the dead time and the current at the switching instant. Finally, the publication demonstrates the effectiveness of the proposed modulation method with a laboratory prototype.

Publication IV extends the study of the phase drift phenomenon to the hard-switched mode and proposes a charge-based and a controller-based method to compensate for the phase drift. The effects of the phase drift phenomenon are demonstrated by measurements with a laboratory prototype.

Publication V introduces a maximum efficiency point tracking algorithm to improve the performance of the variable-frequency modulation. The effectiveness of the proposed method is demonstrated by measurements with a laboratory prototype. Computer simulations are used for a loss distribution comparison.

Additionally, the following publications are related to the work but are not included in this doctoral dissertation:

1. Hiltunen, J., Väisänen, V., & Silventoinen P., 2014. Input filter damping without external passive components. In *European Conference on Power Electronics and Applications (EPE)*, Lappeenranta, Finland, pp. 1–7.
2. Väisänen, V., Hiltunen, J., Nerg, J. et al., 2013. AC resistance calculation methods and practical design considerations when using litz wire. In *Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Vienna, Austria, pp. 368–375.

3. Väisänen, V., Hiltunen, J., & Silventoinen, P., 2014. Core and air gap influence on the accuracy of inductor AC winding resistance calculation methods. In *European Conference on Power Electronics and Applications (EPE)*, Lappeenranta, Finland, pp. 1–10.

1.6 Scientific contributions

The scientific contributions of this doctoral dissertation are:

- Presentation of component dimensioning principles for the current-fed resonant push-pull converter
- Demonstration of the bidirectional operation of the current-fed resonant push-pull converter
- Development of a variable-frequency modulation method for the dual active bridge converter
- Providing guidelines for selecting an optimal dead time and current value at the switching instant
- Analysis of the phase drift phenomenon in the dual active bridge converter
- Providing evidence that the phase drift phenomenon is a consequence of the charge/discharge times of the transistor parasitic capacitances
- Development of methods to compensate for the phase drift
- Development and demonstration of the online efficiency maximization of the DAB converter by using variable-frequency modulation

2 DC-DC converter topologies under study

The selection of the converter topology is one of the most important design choices to be made when designing a power conditioning unit for a fuel cell system. The choice of converter topology has an impact on the power conversion efficiency, price, electromagnetic compatibility, reliability, and many other factors. Therefore, the topology selection is of great importance, and poor choices cannot be easily unmade later by the hardware design or any other means.

Converter topologies can be classified based on the fundamental design choices: current-fed or voltage-fed, isolated or nonisolated, soft-switched or hard-switched, bidirectional or unidirectional, buck or boost. For fuel cell applications, isolated topologies are often preferred to protect the fuel cell from load-side faults and to break the ground loop between the fuel cell and the load. Soft-switching is of importance owing to the possible increase in the conversion efficiency and reduced electromagnetic interference. Further, bidirectional topologies can provide benefits in terms of anode protection.

Suitable converter topologies for solid oxide fuel cell applications have been studied in (Nymand et al., 2009), (Kwon et al., 2009), (Krykunov, 2007), and (Xiao et al., 2019). In particular, two topologies, the current-fed resonant push-pull (RPP) and the dual-active bridge converter (DAB), have gained popularity in SOFC applications. These two topologies are very different by nature; the RPP is current-fed and the DAB is voltage-fed. Both topologies aim at loss reduction by using soft-switching but with different strategies. While the RPP uses a series resonance circuit to achieve zero-current switching (ZCS), the DAB is using the energy stored in the leakage inductance to achieve zero-voltage switching (ZVS) or zero-current switching.

2.1 Current-fed resonant push-pull

The need for galvanic isolation, a high voltage conversion ratio, and a controllable input current with a low ripple makes the current-fed push-pull converter an attractive choice for fuel cell applications. The current-fed push-pull converter was presented in a patent in 1976 (Clarke, 1976). In the patent, it was stated to have several advantages over the traditional voltage-fed push-pull converter. The input inductor of the current-fed push-pull converter limits the input current and thereby mitigates the inrush current problem present in voltage-fed push-pull. The input inductor also mitigates the flux walking problem caused by switching asymmetry. Like its voltage-fed counterpart, the current-fed push-pull converter utilizes the transformer by magnetizing the core in both directions.

Despite the attractive features of the current-fed push-pull converter, it suffers from serious drawbacks. The input inductor causes inductive voltage spikes because of the switching. The circuit presented in the patent (Clarke, 1976) included an additional clamping arrangement (Figure 2.1) to prevent overvoltage. However, the overvoltage

cannot be prevented entirely because of the component nonidealities of the clamping circuit. This may cause added voltage stress to the switching components and increase the electromagnetic interference. The proposed topology also used a full-wave rectifier secondary, which is simple to implement but suffers from reverse recovery of the rectifying diodes.

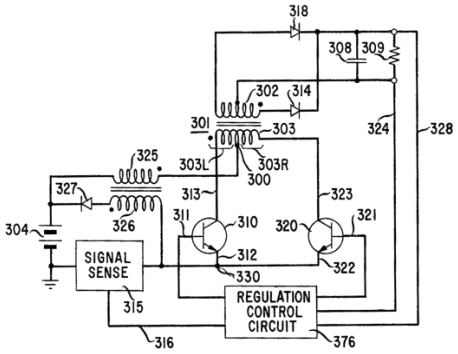


Figure 2.1: Current-fed push-pull converter proposed in the patent (Clarke, 1976).

The current-fed resonant push-pull (RPP) converter, proposed in (Kwon et al., 2009), overcomes the reverse recovery problem of the rectifying diodes by using series resonance to achieve zero-current switching for the diodes. The RPP converter (Figure 2.2) uses a voltage doubler capacitor and the leakage inductance of the transformer to form a resonance circuit. The use of the voltage doubler circuit also increases the voltage conversion ratio of the converter, which is beneficial in fuel cell applications where the stack voltage is typically low and the load-side voltage is high. Voltage doubler capacitors also further improve the tolerance of the converter to the flux walking induced by switching asymmetry (Väisänen et al., 2010). Moreover, the RPP uses active snubbers to limit the inductive voltage spikes over the boost switches.

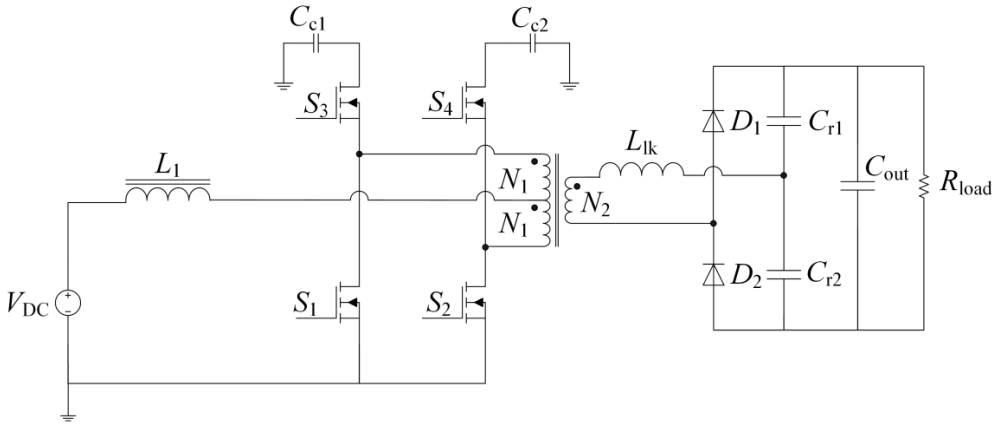


Figure 2.2: Schematic of the resonant push-pull converter (reproduced from Publication I).

One of the benefits of the current-fed resonant push-pull converter is that it can provide a very high voltage conversion ratio as can be seen from the voltage gain equation

$$\frac{V_{out}}{V_{in}} = \frac{2n}{1-D}, \tag{2.1}$$

where n is the transformer turns ratio, and D is the duty cycle defined as the conduction time of switches S_1 and S_2 relative to the length of the switching period. The RPP converter can operate with duty cycles from 0 to 1, which allow operation with a broad input voltage range making it especially interesting for fuel cell applications. However, to gain the benefits of zero-current switching, the size of the voltage doubler capacitor must be aligned with the transformer leakage inductance, switching frequency, and duty cycle. This complicates the design process of the RPP converter.

2.2 Dual active bridge converter

A dual active bridge (DAB) is a bidirectional DC-DC converter that consists of two semiconductor bridges linked together with a high-frequency transformer, as shown in Figure 2.3. The DAB has gained popularity because of its soft-switching and bidirectional power transfer capabilities and the low number of passive components. The dual active bridge converter has been extensively studied since the late 1980s (De Doncker et al., 1988), (Kheraluwala et al., 1990).

One of the key benefits of the dual active bridge converter is that it uses the leakage inductance L_{lk} of the transformer as an energy transfer element. Therefore, no additional reactive components are needed for energy transfer. This makes the dual active bridge converter attractive for applications where a high-power density is preferred. The DAB uses the energy stored in the leakage inductance of the transformer to achieve zero-voltage switching. However, the losses of the DAB are heavily dependent on the load current and the input-output voltage conversion ratio. At light loads, the energy stored in the leakage inductance may not be enough to achieve zero-voltage switching. Moreover, when the DAB is operated outside its nominal input-output voltage conversion ratio, it suffers from reactive and circulating currents, which will increase the conduction losses. In recent years, numerous modulation techniques have been presented to improve the soft-switching capabilities of the DAB and reduce conduction losses.

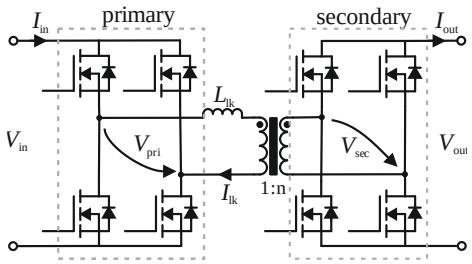


Figure 2.3: Circuit diagram of a dual active bridge converter (Publication III).

The dual active bridge converter can also be constructed by using half-bridges, as shown in Figure 2.4. The use of half-bridges reduces the number of active components, thereby simplifying the design. The half-bridge is an active voltage doubler circuit and thus doubles the voltage from the transformer terminal. This inherent voltage doubling feature can be beneficial in applications such as the SOFC, where a high voltage conversion ratio is needed. Further, the capacitors used in the half-bridge act as a DC blocking element and thus prevent the switching-asymmetry-induced flux walking, in the same way as in the RPP topology. However, the use of half-bridge disables the use of some of the multi-phase shift modulation schemes as the zero-voltage sequence cannot be generated with a half-bridge.

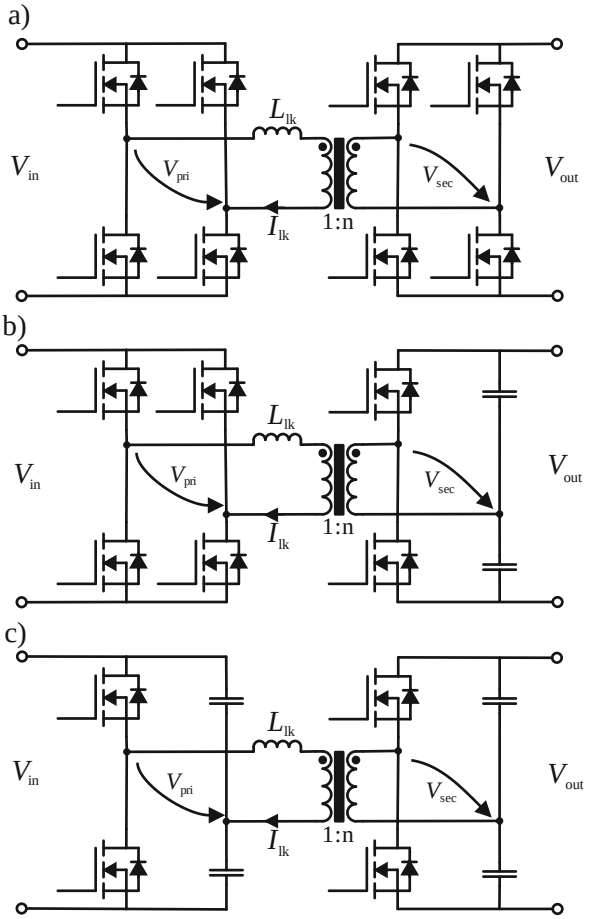


Figure 2.4: Dual active bridge converter can be constructed by using various combinations of full-bridge (FB) and half-bridge (HB): a) FB-FB, b) FB-HB, and c) HB-HB (Publication III).

2.2.1 Single phase shift modulation

The most widely used modulation method for the DAB is the phase shift modulation (PSM), which is sometimes referred to as single phase shift modulation (SPS) to distinguish it from other phase shift modulation schemes. Single phase shift modulation is simple to implement as it controls the power by varying only the phase shift between the primary and secondary H-bridges. The SPS modulation does not use the phase shift between the legs of individual H-bridges, and therefore, it can also be used for half-bridge variants of a dual active bridge converter.

In the traditional phase shift modulation, the power semiconductors are driven in a 180-degree phase shift between the legs of an H-bridge. This modulation constitutes a square-waveform voltage over the transformer winding, as shown in Figure 2.5. Applying a phase shift between these two square-waveform voltages causes a voltage difference between the transformer primary and secondary. This voltage difference causes current to flow. The current flow is limited by the transformer leakage inductance and the duration of voltage, which can be controlled by adjusting the phase shift between the primary and the secondary. This modulation scheme will produce a trapezoidal transformer current waveform, as shown in Figure 2.5.

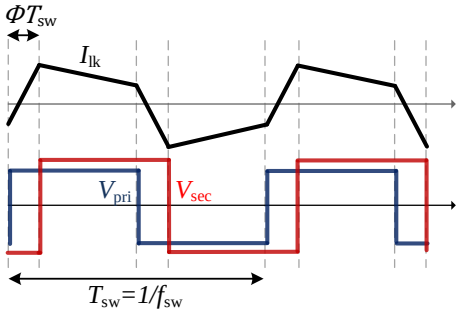


Figure 2.5: Idealized operating waveforms of a dual active bridge converter under single phase shift modulation (reproduced from Publication III).

The power flow of a DAB converter under single phase shift modulation can be analyzed by using the simplified operating model shown in Figure 2.6. The simplified operating model makes some fundamental simplifications: the magnetizing inductance of the transformer is neglected, the switching events are assumed infinitely fast, and the dead time is neglected. Moreover, all the components are assumed ideal and lossless. From the idealized model, the power equation of DAB can be derived into a form

$$P = \frac{V_{\text{in}} V_{\text{out}}/n}{f_{\text{sw}} L_{\text{lk}}} \Phi(1 - 2|\Phi|), \tag{2.2}$$

where Φ is the phase shift in percent, n is the transformer turns ratio, L_{lk} is the transformer leakage inductance, and f_{sw} is the switching frequency. As a consequence of the assumptions made in the derivation of the power equation, Equation (2.2) may give wrong predictions of the power flow at the given phase shift. This causes discrepancies between the idealized power equation and a real DAB converter, which, in turn, leads to difficulties when implementing sophisticated modulation techniques that have been derived from the idealized power equation. Highlighting these discrepancies and developing methods to reduce these harmful effects is one of the key scientific contributions of this doctoral dissertation and is discussed in detail in Sections 3.2.4 and 3.2.5.

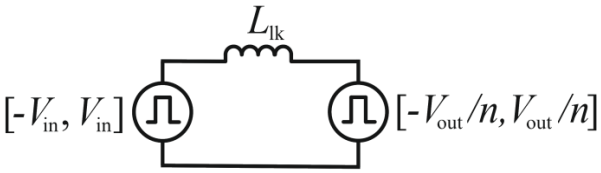


Figure 2.6: Simplified operating model of the dual active bridge converter (Publication III).

Because the dual active bridge converter is symmetrical in structure, it can deliver power equally to both directions, from the primary to the secondary and from the secondary to the primary. The maximum power transfer is achieved at a phase shift of 25 %, as shown in Figure 2.7.

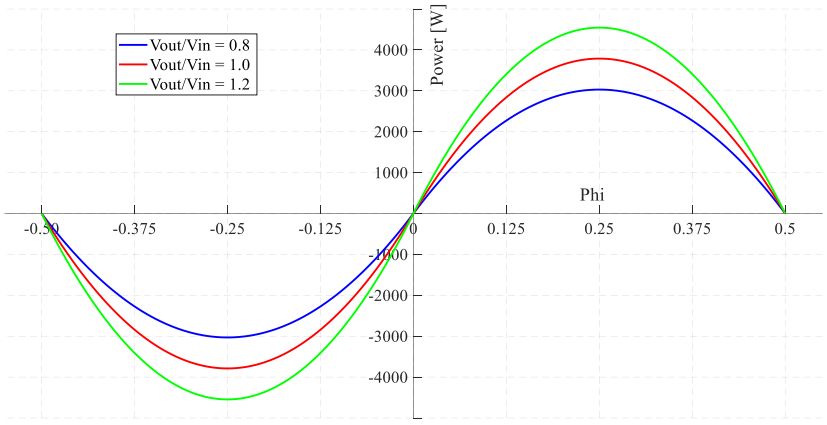


Figure 2.7: Power of the DAB presented as a function of phase shift at different voltage conversion ratios. The power curves are calculated for a converter the parameters of which are n = 1, L_{lk} = 26.4 µH, f_{sw} = 50 kHz, and V_{in} = 200 V.

The leakage inductance of the transformer acts as an energy transfer element in the DAB, making the transformer design a fundamental issue in the design process. The size of the

leakage inductance restricts the maximum power of the converter together with the switching frequency, as can be seen from Equation (2.2). This forces the designer to consider both the switching frequency and the leakage inductance simultaneously, and it can lead to unconventional design principles where a high leakage inductance can be a desired property of the transformer. This is a very characteristic of the dual-active bridge converter compared with other topologies, where the transformer leakage inductance is one of the main obstacles and can force the designer to use a dedicated snubber circuitry to prevent harmful effects of the leakage inductance.

As the leakage inductance acts as the energy transfer element, it is also used to achieve zero-voltage switching. The energy stored in the leakage inductance can be used to charge/discharge the parasitic capacitances of the switching devices. Therefore, the value of the leakage inductance must be chosen correctly also to achieve the desired soft-switching capability. This is another factor that forces the designer to apply unconventional design principles to control the transformer leakage inductance. Various design techniques have been studied to control the leakage inductance of a dual active bridge transformer (Kheraluwala et al., 1990), and the use of a magnetic shunt has been presented in (Zhang et al., 2014).

The downside of intentionally increasing the leakage of the transformer is that it weakens the coupling of transformer windings and thereby increases radiated emissions. Further, the copper loss in the transformer is sensitive to the leakage flux distribution (Kheraluwala et al., 1990), and to minimize copper losses, the leakage field should be distributed as uniformly as possible. Sometimes, a discrete inductor is used in series with the transformer in order to ease the design, extend the soft-switching region, and overcome the harmful effects of the high leakage transformer.

2.2.2 **Reactive current**

A closer analysis of the transformer current waveform of the DAB (Figure 2.8) reveals an essential feature of the dual active bridge converter. When the polarity of the square-wave voltage on the transformer terminal is changed, the transformer leakage inductance prevents current from changing its direction immediately. Therefore, for some amount of time, the current flows in the opposite direction with respect to the voltage applied at the transformer terminal. This causes the energy to be transferred back to the input capacitor of the converter. This reactive power, or backflow power as called in (Xiong et al., 2017), does not do active work for the power transmission but causes additional losses.

Reduction of this reactive current is one of the options to improve the power conversion efficiency of the dual active bridge converter. The traditional method to reduce reactive current is to use multi-phase shift modulation, where a zero-voltage sequence is applied to the transformer terminal by introducing a phase shift between the legs of the corresponding H-bridge.

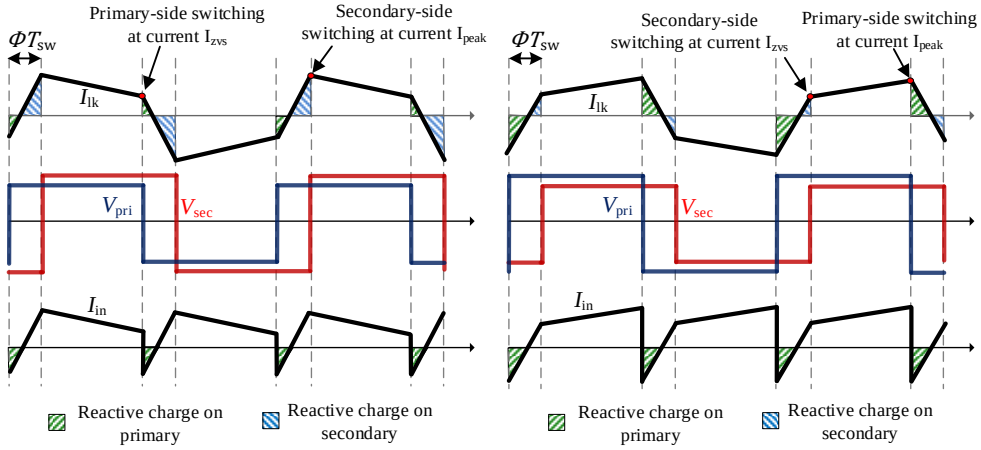


Figure 2.8: Idealized waveforms for the dual-active-bridge converter under traditional phase shift modulation in two cases: a) $V_{in} < V_{out}/n$ and b) $V_{in} > V_{out}/n$. The shaded areas represent the reactive charge, which flows in the reverse direction with respect to the corresponding voltage (reproduced from Publication IV).

2.2.3 Multi-phase shift modulation schemes

The usual method to overcome the problem of reactive power is to introduce a phase shift between the switching legs of an H-bridge. This will produce a zero-voltage sequence to the transformer magnetization voltage, which also allows controlling the current at the switching instant, as shown in Figure 2.9. The zero-voltage sequence can be introduced for one or both H-bridges.

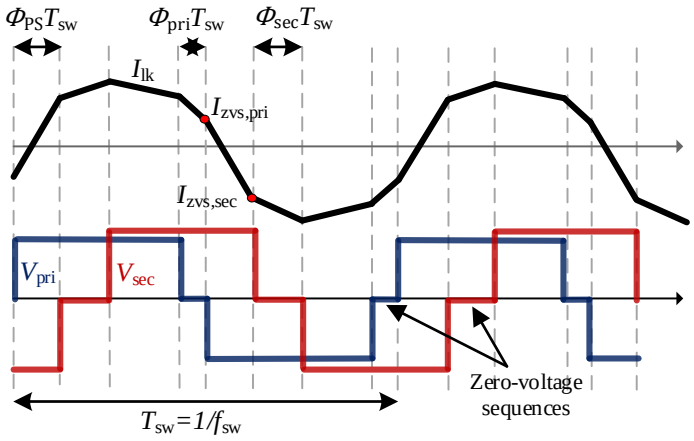


Figure 2.9: Idealized waveform for the dual-active-bridge converter under multi-phase shift modulation.

The use of a phase shift between the legs of the H-bridge gives an additional degree of freedom to control the current at which the power switches are switching. This can be used to produce a small amount of reactive power intentionally so that at the switching instant, the transformer current will be enough to enable zero-voltage switching (ZVS). Alternatively, the current at the switching instant can be controlled to zero to enable zero-current switching (ZCS), which can be more advantageous in some cases.

The multi-phase shift (MPS) modulation schemes have been extensively studied in recent years. Some of the MPS modulation schemes are designed for ZVS, others for ZCS. Sometimes the objective is to minimize the reactive or RMS current. The MPS are known with several different names, which are often based on the number of phase shifts used: dual phase shift (DPS) modulation (Liu et al., 2017) or triple phase shift (TPS) modulation (Huang et al., 2016). Sometimes, modulation schemes are named based on the transformer waveform: triangular current mode (TCM) modulation (Krismer & Kolar, 2012) and trapezoidal current mode (TZM) modulation (Krismer & Kolar, 2012). Moreover, such methods as extended phase shift (EPS) modulation (Zhao et al., 2012) and optimal transition mode (OTM) modulation (Krismer & Kolar, 2012) have been proposed. A common denominator for all these modulation schemes is that they use more than one phase shift in the effort to achieve zero-voltage switching (ZVS), zero-current switching (ZCS), or to minimize current stress.

2.2.4 Circulating current

The multi-phase shift modulation can be used to reduce the reactive current and extend the power and voltage range where soft-switching is achieved. However, the introduction of the zero-voltage sequence to the transformer magnetization voltage creates yet another problem. During the zero-voltage sequence, the transformer winding is effectively short circuited through the H-bridge, while the current is still flowing in the transformer winding. This freewheeling inside the H-bridge will cause losses in the transformer, switching components, and the circuit board. Therefore, the MPS methods do not solve the problems entirely but instead replace the reactive current with circulating current, as shown in Figure 2.10. This point is too often omitted in the discussion of DAB modulation methods.

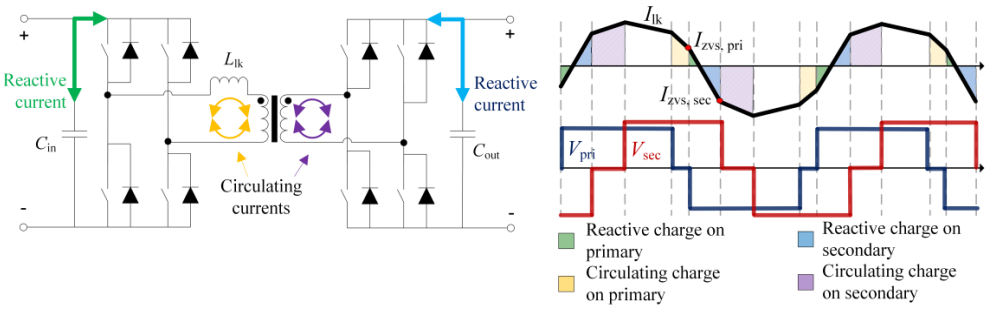


Figure 2.10: Simplified circuit diagram and operation waveforms of the DAB to illustrate how the reactive and circulating currents are formed.

3 Results and discussion

The objective of this doctoral dissertation was to investigate two preselected DC-DC converter topologies and to study the opportunities to improve their power conversion efficiency and suitability for solid oxide fuel cell applications. The research started as a study of the current-fed resonant push-pull (RPP) converter, its efficiency, and the dimensioning of components. Further, its use for bidirectional operation for SOFC anode protection was studied. The study on the RPP converter revealed some challenges in its design and component dimensioning. However, the study also showed its capability for high efficiency and bidirectional operation. The research continued with a study of the dual active bridge (DAB) converter, which seemed to provide more opportunities for efficiency improvement than the RPP. The study on the dual active bridge converter produced many results on modulation and efficiency improvement. The study also pointed out some challenges related to the converter topology and its modulation methods. The key results of the research work are presented in this chapter, and a separate section is dedicated to each key result. The power conversion efficiency results presented in this dissertation were determined by measuring the currents and voltages from the converter input and output terminals with the tools presented in Appendix A.

3.1 Resonant push-pull converter

The design principles and suitability of the resonant push-pull converter for solid oxide fuel cell applications were studied in Publication I. The principles for component dimensioning were analyzed, and the analytic equations for component dimensioning were presented for all the essential components of the RPP: input inductor, transistors, transformer, rectifying diodes, and voltage doubler capacitors. Finally, the efficiency of the resonant push-pull converter was demonstrated with a 10 kW laboratory prototype, shown in Figure 3.1.

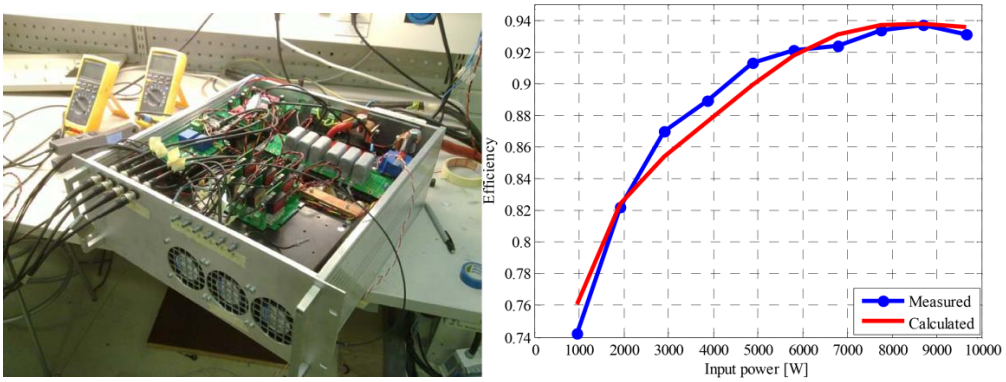


Figure 3.1: Prototype converter with the measured and calculated efficiency sweep over the input power range with the input voltage V_{in} = 50 V. The achieved peak efficiency was 93.7% at 8700 W (Publication I).

The design of the magnetic components turned out to be one of the key design challenges of the RPP converter. The design of the input inductor is challenging in applications where a high current and a low current ripple are needed. For a low current ripple, a high inductance is needed, which, in turn, increases the number of winding turns. The high number of winding turns tends to increase the winding resistance, leading to increased losses. The transformer of the resonant push-pull has a center-tapped structure, which makes its design more complicated than a design of a traditional two-winding transformer. The resonance period of transformer leakage inductance and voltage doubler capacitors must also be aligned to achieve optimal efficiency, as can be seen in Table 3.1. The increase in the primary conduction and switching losses was observed to be higher for shorter resonant periods. Another drawback of the resonance is that the amplitude of the current can get relatively high at the peak of the resonance. The high peak current must be taken into account when selecting the components for the resonant push-pull converter.

Table 3.1: Effect of resonant period length on the resonant push-pull efficiency (reproduced from Publication I).

Input 50.8 V, 3800 W, D = 0.52, R_L = 107 Ω	A	B	C
Leakage inductance [µH]	3.2	3.2	3.2
Resonant capacitor C_r [µF]	1.36	2.72	4
S_1 & S_2 losses [W]	101	100	100
S_3 & S_4 losses [W]	42	32	23
S_3 & S_4 I_{rms} [A]	25	16	14
Diode conduction losses [W]	14	15	16
Diode switching losses [W]	0.8	0.8	6
Transformer losses [W]	30	30	30
Calculated efficiency [%]	94.78	95.03	95.14
Measured efficiency [%]	94.7	95.4	95.7

The current-fed resonant push-pull converter was also observed to suffer from transient voltage overshoots of the switches. This is a fundamental problem of boost-derived topologies, but in the RPP, the active snubbers are meant to mitigate this problem. However, one of the findings of this study was that the recovery delay of the body diode of the snubber transistor causes slowness to the voltage clamping. This slowness will result in the voltage to overshoot over the switch for a brief time. The duration of voltage overshoot is dependent on the switching component, the current value, and the circuit inductance. This seemingly short period may be enough to cause permanent damage to the switch, especially if the switch is not rated to withstand the avalanche energy at hand. This problem can be reduced by using a switching component, such as a silicon carbide MOSFET, with a high-speed intrinsic body diode.

The transient voltage overshoot problem is made even worse by the fact that there occurs a transient voltage in addition to the normal operating voltage. With the RPP topology, the operating voltage of the primary side components is dependent on the duty cycle and

can be significantly higher than the input voltage of the converter. The normal operating voltage of the primary-side components can be calculated from the volt-second balance law of the inductor. As shown in Publication I, the maximum voltage of the primary components is obtained by

$$V_{\mathrm{pri(max)}} = \frac{V_{\mathrm{DC}}}{1 - D} \quad , \tag{3.1}$$

where V_{DC} is the input voltage of the converter, and D is the duty cycle defined as the conduction time of switches S_1 and S_2 relative to the total length of the switching period.

For the 10 kW laboratory prototype, the problem of transient overvoltage was overcome by overdimensioning the voltage rating of the transistors fourfold compared with the nominal input voltage. Furthermore, the selected transistors were rated for avalanche energy of 4 J, providing additional safeguards against voltage overshoots. However, transistors with a higher voltage rating typically have a higher on-state resistance, which results in higher conduction losses. This causes an efficiency penalty for the RPP topology and hinders its attractiveness to the SOFC power conversion.

3.1.1 Bidirectional operation of the resonant push-pull converter

One of the limitations of the resonant push-pull converter is its unidirectional nature. The traditional resonant push-pull converter can deliver power from the primary to the secondary side, but not from the secondary to the primary. Therefore, the conventional resonant push-pull converter is not the best choice for SOFC applications where anode protection with reverse bias current is needed.

In Publication II, the option to modify the conventional RPP converter to enable bidirectional operation was studied. The study resulted in a modification to the RPP topology, in which the secondary rectifying diodes were replaced with active switches, as shown in Figure 3.2. In addition to bidirectional operation, this modification provides an additional benefit that the secondary-side bridge can be used as an active rectifier to reduce the losses related to a forward voltage drop of the rectifying diodes.

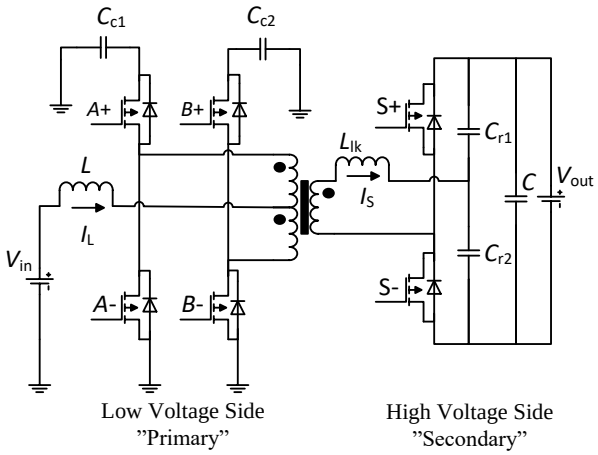


Figure 3.2: Bidirectional resonant push-pull converter (Publication II).

In order to make the reverse power flow possible, the modulation scheme of the RPP had to be modified. The formulation of the modulation scheme was done by using analytic calculations assisted with PSpice simulations. As a result, a modulation scheme was developed where the secondary side switches (S+ and S-) were driven as a complement to the active snubber switches (A+ and B+), as can be seen in Figure 3.3.

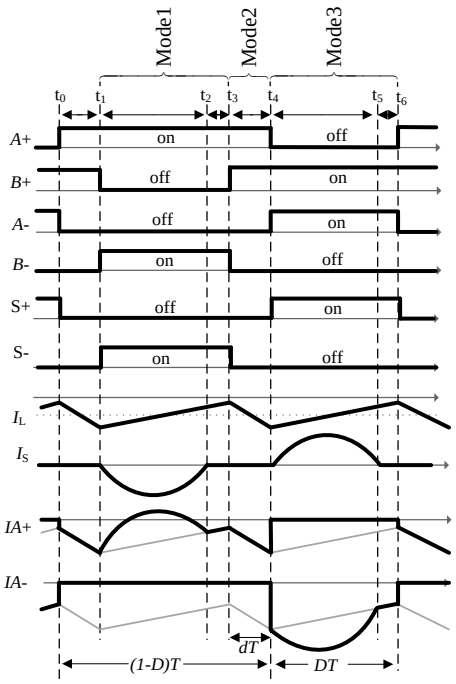


Figure 3.3: Theoretical waveforms of the resonant push-pull converter in reverse power flow operation (Publication II).

The voltage conversion ratio for the converter was derived by applying the volt-second balance law on the input inductor, as shown in Publication II, to a form

$$\frac{V_{\text{in}}}{V_{\text{out}}} = \frac{1-D}{2n}, \tag{3.2}$$

where n is the transformer turns ratio. It was observed that the duty cycle had to be redefined to make a smooth transition from the forward to the reverse power flow possible. As a result, the duty cycle was redefined as

$$D = \begin{cases} d & \text{, when forward power flow} \\ d + 0.5 & \text{, when reverse power flow} \end{cases}, \tag{3.3}$$

where d is the output of a controller, and D is the duty cycle for the modulator. The redefinition of the duty cycle makes the voltage conversion ratio a piecewise continuous function of the control variable d, as shown in Publication II. This allowed a simple implementation of the controller as the power flow can now be controlled with one continuous control variable d, which can have values in the range of $-0.5 < d < 1$. The positive values of the control variable d yield a forward power flow and negative values result in a reverse power flow. With the redefined duty cycle, the voltage gain for the bidirectional push-pull converter was written as

$$G = \begin{cases} \frac{V_{out}}{V_{in}} = \frac{2n}{1-d} & \text{, when } d > 0 \\ \frac{V_{in}}{V_{out}} = \frac{-d+0.5}{2n} & \text{, when } d < 0 \end{cases}. \tag{3.4}$$

In order to verify the feasibility of the proposed bidirectional current-fed resonant push-pull converter, a 5 kW laboratory prototype was built and tested (Figure 3.4). The laboratory tests provided promising results for the reverse power flow with a similar efficiency that what was gained with the 10 kW RPP prototype. However, the fundamental challenges of the RPP topology with the need for component overdimensioning and limited soft-switching capabilities reduce the attractiveness of the topology.

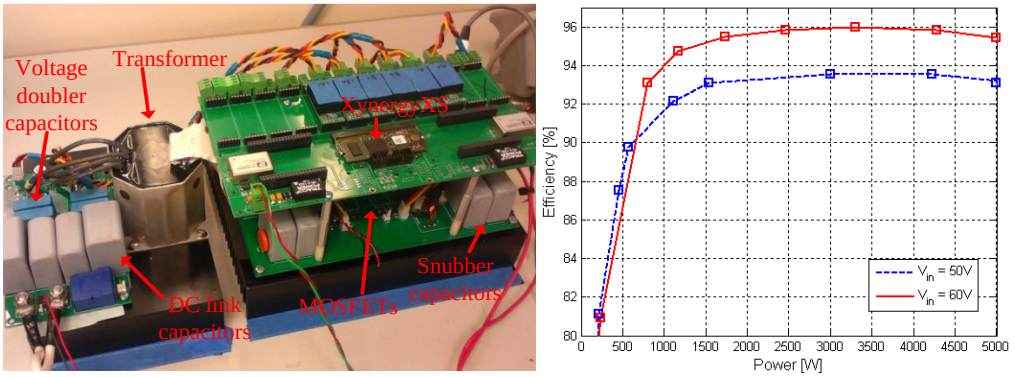


Figure 3.4: Bidirectional resonant push-pull converter prototype and the measured efficiency for 50 V and 60 V primary voltages when the secondary voltage is kept at 660 V (Publication II).

3.2 Dual active bridge

The limitations of the current-fed resonant push-pull converter increase the interest in topologies that have better soft-switching capabilities and do not suffer from voltage overshoots to the same extent as the RPP. The dual active bridge converter is a bidirectional converter topology that is well known for its soft-switching capabilities. Theoretically, with a proper modulation scheme, the DAB can achieve soft-switching with almost all power levels and voltage conversion ratios. In practice, however, these advanced modulation algorithms rely on an idealized power flow equation and voltage and current measurements. Therefore, these advanced modulation schemes are susceptible to circuit nonidealities. Moreover, sophisticated modulation algorithms are typically implemented by using lookup tables or a set of complicated equations and are therefore difficult to implement in practice.

In the course of the study, it was found that while the sophisticated modulation schemes worked in the simulation environment with ideal switching components, they did not work as expected in the laboratory environment. These findings stimulated an interest to study whether it is possible to develop a simple closed-form control algorithm and compensate for the circuit nonidealities. In addition, the discrepancy between the theoretical power flow equation (2.2) and the real converter must be better understood, and its effects must be compensated for to make the modulation schemes useful for real applications.

3.2.1 Variable-frequency modulation

The traditional phase-fixed frequency single phase shift (SPS) modulation, presented in Section 2.2.1, is easy to implement but does not allow control of the reactive current. The

fixed frequency SPS modulation uses only the phase shift to control the power flow of the converter. As this modulation method has only one degree of freedom, it can be used to control the power flow through the converter, but it cannot simultaneously be used to extend the soft-switching region. Therefore, at low loads, the transformer current at the switching instant may not be enough for discharging the output capacitances of the switching components, and the converter may thus end up in hard switching. This will reduce the power conversion efficiency and cause added electromagnetic interference. Furthermore, operating outside the nominal operating point will increase the reactive current and thereby increase the component current stress and losses.

Multi-phase shift (MPS) modulation schemes, presented in Section 2.2.3, aim to solve the problem mentioned above. In the MPS modulation, an additional phase shift is introduced between the switching legs of the H-bridge. This allows controlling the current at the switching instant and limiting the reactive current. However, these multi-phase shift modulation schemes present extra challenges. The introduction of a phase shift inside the H-bridge limits the amount of reactive current but at the same time produces a circulating current inside the H-bridge, which increases the conduction losses. Additionally, the multi-phase shift modulation schemes increase the complexity of the implementation of the modulation.

The operation of single phase shift modulation can be improved by using the switching frequency as a control parameter along with the phase shift. This gives two degrees of freedom, frequency, and phase shift, to control the power flow and the transformer current at the switching instant. This makes it possible to prevent the converter from entering hard switching at light loads while still maintaining the desired power flow. This method provides an additional benefit that while there is now phase shift between the legs of an H-bridge, there is no zero-voltage sequence, and therefore, no circulating currents are formed inside the H-bridge. This is a clear benefit compared with multi-phase shift methods.

Publication III studied the above-described modulation principle and formulated it into a form of modulation algorithm called variable-frequency modulation (VFM). The formulation of the VFM was done by using analytical calculations, and the effectiveness of the proposed modulation method was verified with a laboratory prototype.

The formulation of the VFM algorithm starts from the idealized current waveform shown in Figure 2.8. The waveform is symmetrical about its center line and has two knee points in each half-cycle. One of the knee points is at the peak value of the transformer current, and the other one is less or equal to this peak value. It can be concluded that in the case of an ideal converter with fixed switching leg capacitances, if the current at the lower knee point is enough for providing zero-voltage switching (ZVS), the current at the peak knee point must also be enough for zero-voltage switching. With these assumptions, the equation for the transformer current at the lower knee point can be derived as shown in Publication III and written in the form

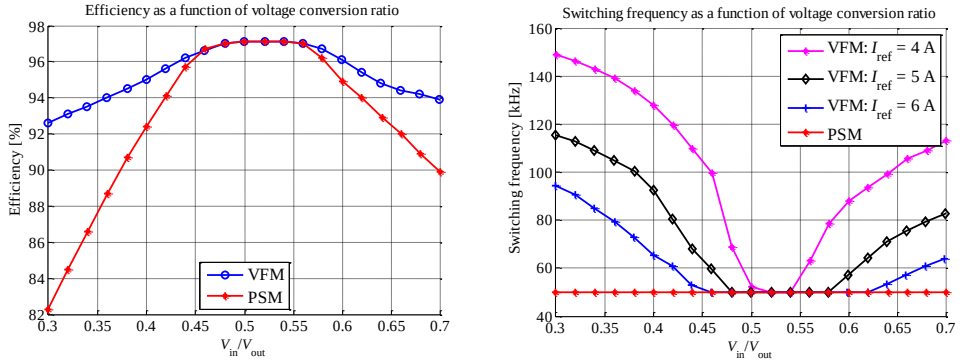
$$I_{\mathrm{zvs}} = \begin{cases} \dfrac{(4|\Phi| - 1)V_2 + V_1}{4f_{\mathrm{sw}}L_{\mathrm{lk}}}, & when\ V_1 \le V_2 \\ \dfrac{(4|\Phi| - 1)V_1 + V_2}{4f_{\mathrm{sw}}L_{\mathrm{lk}}}, & when\ V_1 > V_2 \end{cases}, \tag{3.5}$$

where Φ is the phase shift in percent, and V_1 and V_2 are the equivalent voltages reduced to the same side of the transformer as shown in Publication III. Solving the equation and the power flow equation simultaneously yields a variable-frequency modulation algorithm as shown in Publication III

$$\begin{cases} \Phi = \dfrac{1}{4\gamma}\left(\gamma - I_{\mathrm{ref}}\alpha + \mathrm{sign}(I_{\mathrm{ref}})\sqrt{\alpha^2 I_{\mathrm{ref}}^2 - 2I_{\mathrm{ref}}\gamma\beta + \gamma^2}\right) \\ f_{\mathrm{sw}} = \dfrac{h_{\mathrm{pri}}V_2}{I_{\mathrm{ref}}L_{\mathrm{lk}}}\Phi(1 - 2|\Phi|) \end{cases}, \tag{3.6}$$

where I_{ref} is the desired input current of the converter, h_{pri} is a variable describing the structure of the primary-side bridge, α and β are voltage-dependent variables, and γ is a variable containing the information of the desired current at the switching instant as shown in detail in Publication III. The variable-frequency modulation (VFM) algorithm will result in a higher switching frequency when moving further away from the nominal operating point. Usually, the increase in the switching frequency would result in higher overall losses. With the VFM, this is not necessarily the case as the VFM algorithm will result in nearly lossless switching, which may overcome the drawbacks of the increased switching frequency, as demonstrated in Publication III.

The laboratory experiments showed a significant efficiency improvement with the VFM compared with the traditional phase shift modulation, as can be seen in Figure 3.5. The efficiency was improved up to 10% at the point where the converter was operated far from its nominal voltage conversion ratio. The experiments were conducted with a prototype (Figure 3.6) that had a full-bridge primary and a half-bridge secondary. The efficiency improvement with this converter prototype cannot be generalized. Depending on the converter structure and the selected components, the increased switching frequency can lead to increased losses as a result of the AC resistance and increased gate driving losses. Moreover, the variable switching frequency can cause challenges to compliance with the EMC standards.



a) b)

Figure 3.5: a) Measured efficiency for the traditional phase shift modulation (PSM) and for the proposed variable-frequency modulation (VFM) scheme. b) Switching frequency as a function of voltage conversion ratio for various input current reference values (Publication III).

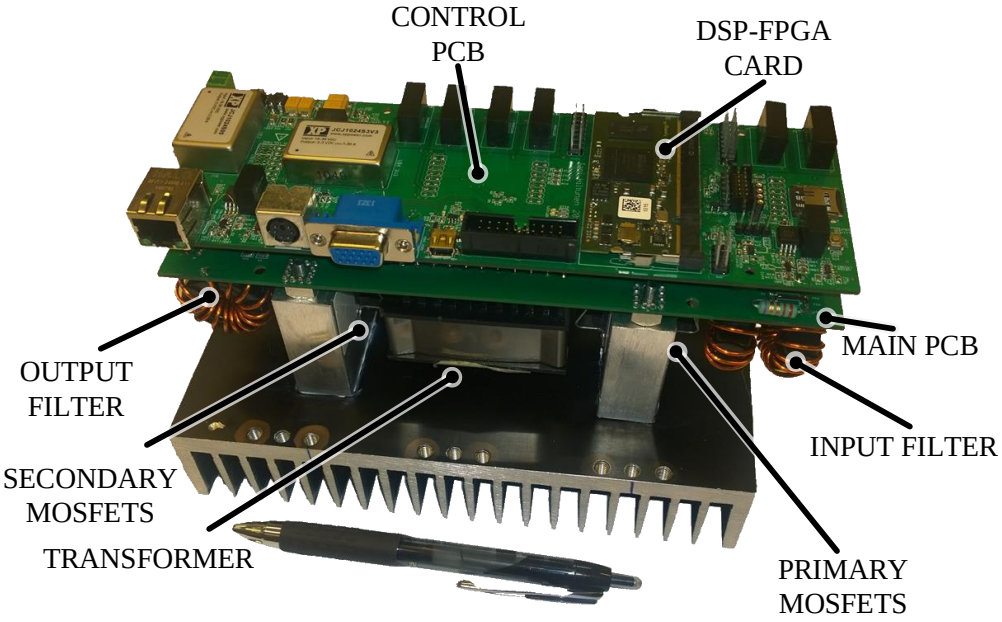


Figure 3.6: Dual active bridge laboratory prototype (Publication III).

3.2.2 Switching current

The variable frequency modulation method provides a method to control the transformer current at the switching instant I_{ZVS} to the desired value. If the current value I_{ZVS} has a negative value, the low-voltage side (smaller of V_1 or V_2) of the converter will be in the hard-switched mode. If this current is set to zero, the low-voltage side of the converter will be zero-current switched, and if the current value is increased far enough to the positive side, the converter will be zero-voltage switched. However, too large a current value at the switching instant I_{ZVS} will result in an excess reactive current, which may overshadow the efficiency improvement gained by the zero-voltage switching. All in all, the selection of I_{ZVS} value has a significant effect on the efficiency improvement gained with the VFM, as shown in Figure 3.7. This raises a question of how to select the current value I_{ZVS} so that it is sufficient for zero-voltage switching but not too large to cause an excess reactive current.

In Publication III, the selection of current value for the switching instant was studied. In the resonance transition, the energy for discharging the output capacitances of the switching components is taken from the transformer leakage inductance L_{lk}. For a complete zero-voltage transition, the energy in the leakage inductance must be at least equal to the energy charged in the output capacitances of the transitioning semiconductor switches, as shown in (Kheraluwala et al., 1990). This leads to a condition presented in Publication III:

$$\frac{1}{2} L_{\mathrm{lk}} I_{\mathrm{ZVS}}^2 \geq k \frac{1}{2} C_{\mathrm{O}} V_{\mathrm{bridge}}^2 , \tag{3.7}$$

where k is the number of switching devices, I_{ZVS} is the transformer current at the switching instant, V_{bridge} is the voltage over switching leg, and C_O is the effective output capacitance of the switching device. Solving I_{ZVS} from Equation (3.7) yields a condition

$$I_{\mathrm{ZVS}} \geq \left|V_{\mathrm{bridge}}\right| \sqrt{\frac{kC_{\mathrm{O}}}{L_{\mathrm{lk}}}}. \tag{3.8}$$

Inequity (3.8) gives the minimum value of the current at the switching instant, which can result in complete zero-voltage switching. If the current value is chosen higher than zero but smaller than what is suggested by inequity (3.8), a partial zero-voltage switching will result.

The difficulty of applying inequity (3.8) in practice is that the effective output capacitance of the switching devices is often not known precisely and may not be easily measured. Moreover, the capacitances of the switching device are nonlinear functions of drain-source voltage, which makes it even harder to estimate the value from typical graphs given in the datasheet (Figure 3.8).

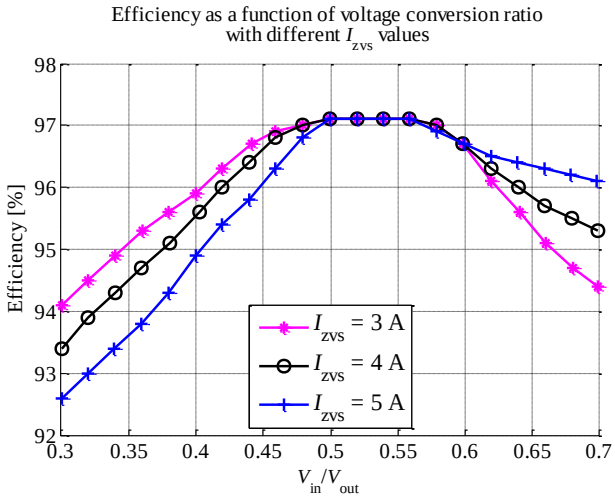


Figure 3.7: Measured efficiency for different switching current values. During the measurements, the secondary voltage was kept constant at 250 V, and the primary-side current (I_{in}) was controlled to 6 A by using a feedback control to compensate for the phase drift. The current required for a complete C_{oss} discharge is higher on the secondary side than on the primary side. Therefore, the larger I_{zvs} values improve the efficiency at higher V_{in}/V_{out} ratios, while the primary side is already zero voltage switched with smaller I_{zvs} values. If the I_{zvs} reference is larger than the current at which the output capacitances are completely discharged, the increasing switching frequency is only causing additional losses in the converter without bringing any further benefits to the zero-voltage switching process (Publication III).

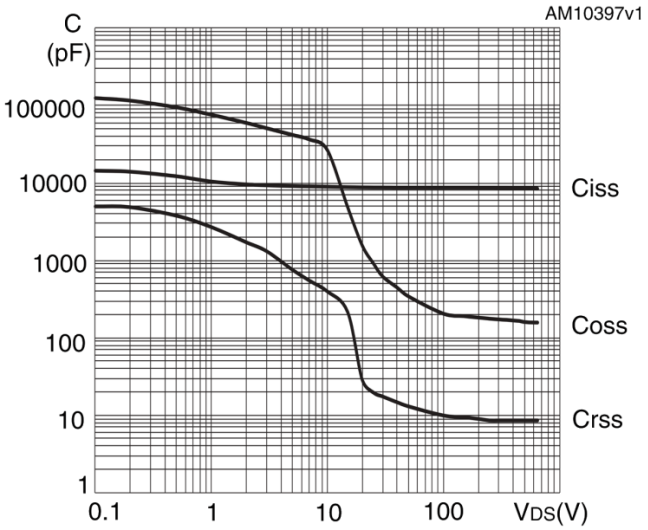


Figure 3.8: Behavior of the input (C_{iss}), output (C_{oss}), and reverse transfer (C_{rss}), capacitances as a function of drain-source voltage for STW88N65M5 MOSFET (STMicroelectronics, 2014).

3.2.3 Dead time and back commutation

A large enough current at the switching instant is the fundamental prerequisite for the zero-voltage switching. However, the switching transition is not infinitely fast because of component and circuit nonidealities. Therefore, some finite amount of time is required to complete the zero-voltage transition. This is one reason why a dead time is needed between the switching components of the same leg. Another reason for the use of dead time is the component tolerances and inaccuracies in the gate driving circuitry. Without a dead time, there is a risk that both switches of the switching leg are conducting simultaneously. This instantaneous short-circuit of the H-bridge could lead to permanent hardware damage.

Publication III studied the dead time and its effects on switching transition. The optimal length of the dead time is related to the length of the resonance time of the transformer leakage inductance and the capacitance of the switching leg. Too short a dead time will result in partial hard switching as the capacitance of the switching leg is not fully charged/discharged. Too long a dead time can cause back commutation, as shown in Figure 3.9, which leads to increased switching losses. The minimum dead time needed for ZVS transition can be estimated as shown in Publication III:

$$t_{\text{dead, min}} = \frac{2V_{\text{ds}}C_{\text{o,tr}}(V_{\text{ds}})}{I_{\text{sw}}}\ , \tag{3.9}$$

where $C_{\text{o,tr}}$ is the equivalent time-related capacitance of the switching device, and I_{sw} is the current of the switching leg at the switching instant.

Complete zero-voltage switching in the DAB can only be achieved when the dead time is selected to match the resonance time of the transformer leakage inductance and the capacitance of the switching leg. This would require a dead time that continually adapts to the prevailing switching conditions. Some study on adaptive dead time has been made in (Li et al., 2012), but adaptive time is hard to implement in practice because of component tolerances and gate driving inaccuracies.

Owing to the difficulties to implement adaptive dead time, a fixed dead time is often used in real applications. A fixed dead time suffers from an efficiency penalty as a result of the incomplete ZVS transition. For many practical applications, this penalty may be justifiable for the sake of simple implementation of the modulator, especially if the dead time is selected in a reasonable vicinity of its optimal value. Guidelines for the selection of dead time are given in Publication III.

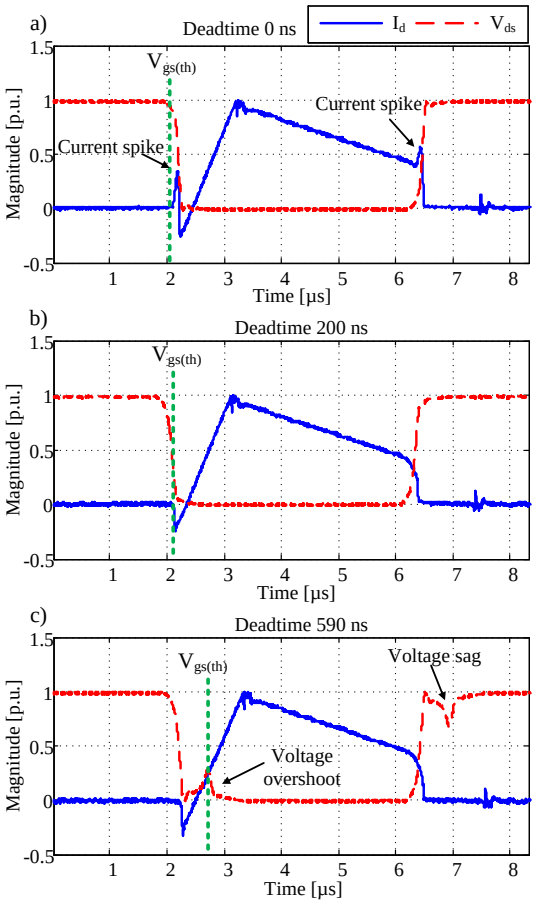


Figure 3.9: Three dead time lengths and their effects on the switching waveforms. a) The dead time is too short, which results in partial hard-switching. b) The dead time is of the right length resulting in zero-voltage switching. c) The dead time is too long resulting in back commutation (Publication III).

3.2.4 Phase drift phenomenon

The non-zero commutation time causes a problem for modulation schemes that have been derived from the idealized power equation (2.2). The idealized power equation was derived with an assumption that the H-bridge can generate ideal square wave voltage. The circuit nonidealities cause the apparent phase shift to differ from the effective phase shift seen over the transformer, as can be seen in Figure 3.10. The existence of a phase-shift-related error has previously been reported in (Xie et al., 2010) and (Zhao et al., 2014). In the previous publications, the phase drift phenomenon was explained by the power loss of the converter and the effects of dead time.

In Publication III, the origins of the phase drift phenomenon in the zero-voltage switched-mode were studied. The measurement results (Figure 3.11) show that the phase drift

varies significantly as a function of drain-source voltage and the current at the switching instant. The results indicate that the phase drift is caused by the charge/discharge times of the transistor parasitic capacitances, not solely by the dead time. The result shows that the phase drift is severest when the voltage difference between the primary and the secondary H-bridge is high. This is explained by the voltage dependence of capacitances of the power switches (Figure 3.8).

In Publication IV, the study of phase drift phenomenon was extended to the hard-switched mode. The measurement results (Figure 3.12) show that the phase drift is significantly smaller in the hard-switched mode, providing further evidence for the conclusion that phase drift is mainly caused by the charge/discharge times of the transistor parasitic capacitances. It is concluded that the phase drift may not be a significant issue when operated in the hard-switched mode. However, operating in the hard-switched mode is usually undesirable because of the increased switching losses and electromagnetic interference.

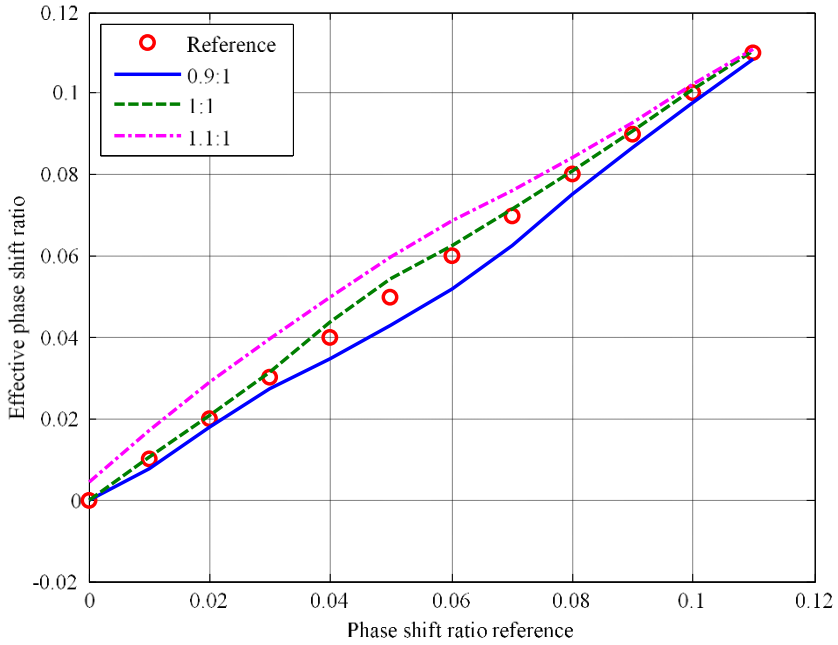


Figure 3.10: Measured phase shift ratios with respect to the reference phase shift ratios at various V_{in}/nV_{out} ratios. The output voltage V_{out} is 160 V and the input voltages are 74.7 V (0.9:1), 83 V (1:1) and 91.4 V (1.1:1). The phase shift ratio is the ratio of the phase shift length to the switching period length (reproduced from Publication IV).

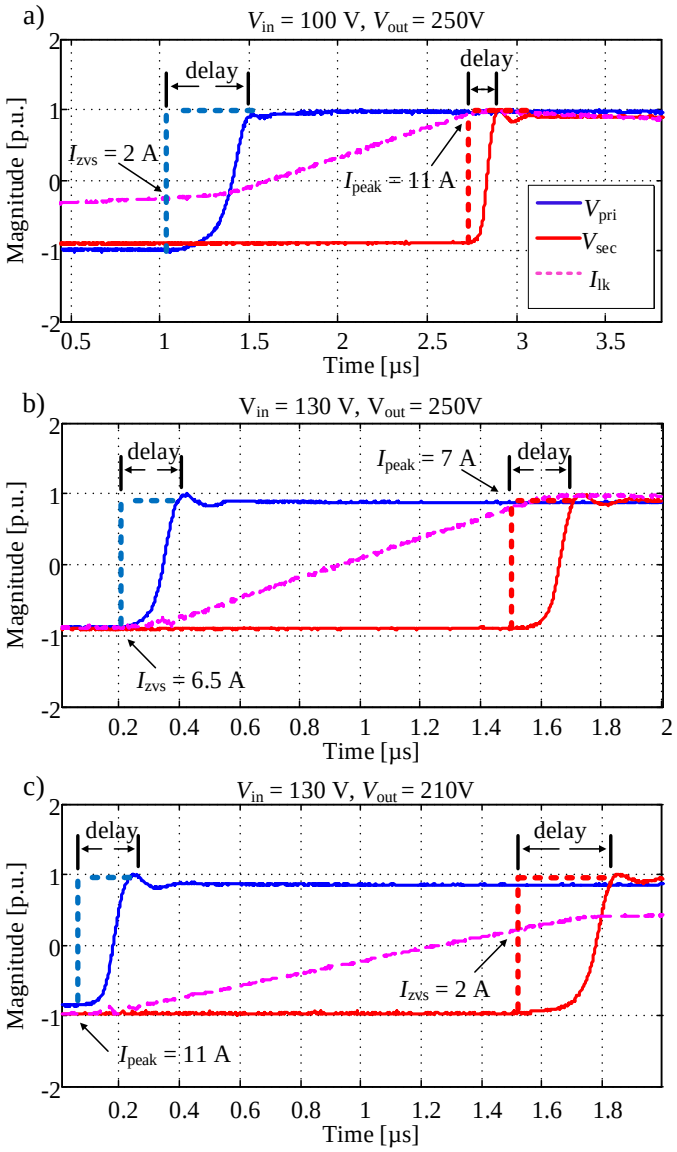


Figure 3.11: Measured phase drifts for a dual active bridge converter with a full-bridge primary, half-bridge secondary, and a transformer with a 1:1 turns ratio. For the measurements, STWA88N65M5 MOSFETs were used. a) The primary-side voltage is smaller than the secondary-side voltage referred to the primary side. The higher voltage and the higher discharging current on the secondary side result in a smaller phase drift on the secondary side. b) The primary-side voltage is similar to the secondary-side voltage referred to the primary side. The discharging currents are also similar, which results in similar phase drifts on both sides. c) The secondary-side voltage referred to the primary side is lower than the primary-side voltage. The higher voltage and the higher discharging current on the primary side result in a smaller phase drift on the primary side (Publication III).

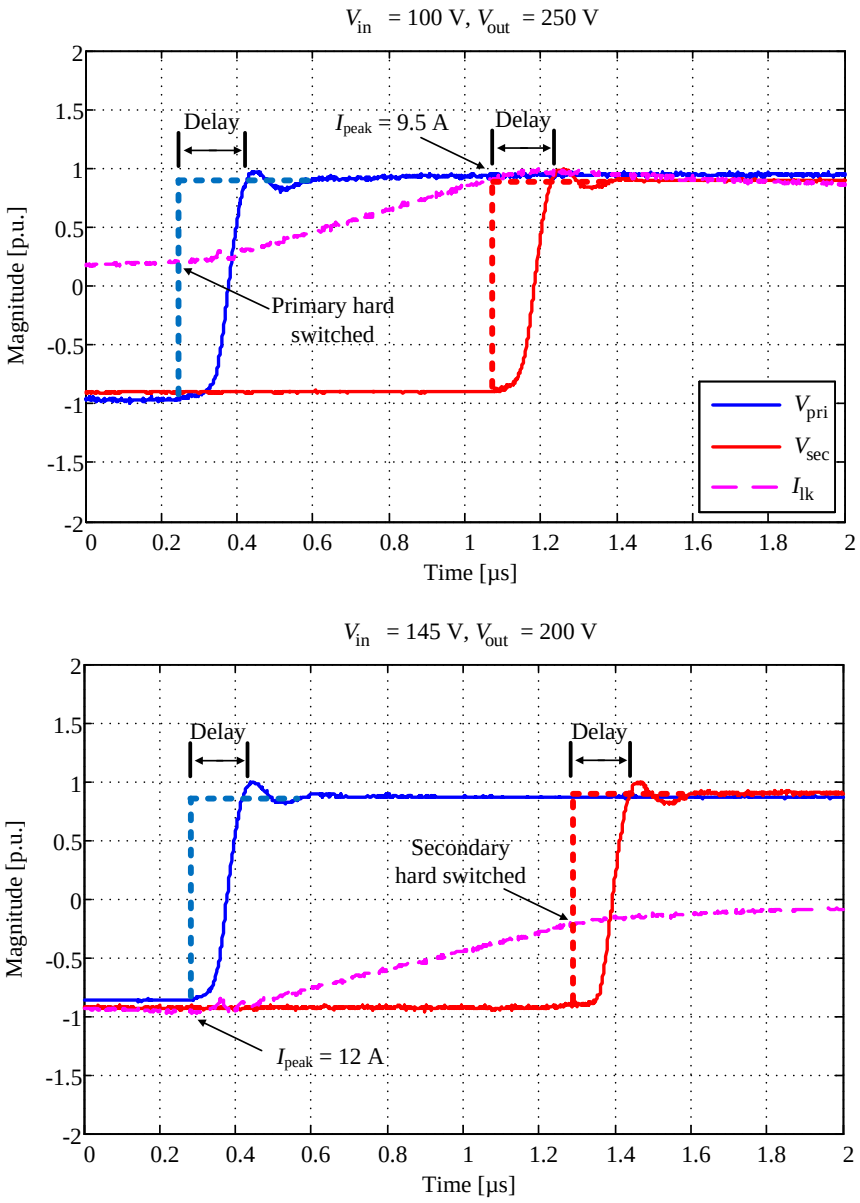


Figure 3.12: Measured phase drifts for two cases: $V_1 < V_2$ (top) and $V_1 > V_2$ (bottom). The input current I_{in} = 4 A in all cases. The references for the primary and secondary voltages are indicated by dashed lines. The converter has an FB-HB configuration, and the converter is in hard-switching in both cases (Publication IV).

3.2.5 Methods to compensate for the phase drift

The phase drift phenomenon complicates the estimation of the current at the switching instant and thus poses a significant drawback for the sophisticated modulation schemes. Some study has been made in (Yanhui et al., 2010) and (Itoh et al., 2018) to compensate for the effects of the phase drift. However, the proposed compensation methods are based on an analytic calculation of correction parameters and are therefore complicated to implement. Moreover, the proposed compensation methods are based on the assumption that the dead time is causing the phase drift. This can lead to wrong phase drift compensation, particularly when the DAB is operated in the zero-voltage switched-mode with very different voltages in the primary and the secondary, as shown in the previous section.

In Publication III, the concept of the controller-based compensation method was introduced in brief. In Publication IV, the operating principle of the controller-based compensation method was explained in comparison with the traditional feedback controller (Figure 3.13). The proposed controller-based compensation method is simple to implement and does not need exact knowledge of the capacitance of the switching leg. The operation of the controller-based compensation method assumes that the phase shift error solely causes a power discrepancy between the power equation and the measured power. The proposed controller-based compensation method can be used with the variable-frequency modulation method where there is only one phase shift to control. With the multi-phase shift modulation schemes, the proposed controller-based compensation may not work correctly as the leading and lagging legs of an H-bridge may switch at different currents (Figure 2.9) and thus have different switching transition times.

In Publication IV, a charge-based compensation method was studied. The idea of a charge-based compensation method is to calculate how long it would take for a certain switching current to discharge the output capacitance of a semiconductor switch. This calculated drift time can then be compensated for with the modulation algorithm. In this method, the effective length of the drift is calculated as a difference of the primary and secondary transition times

$$t_{\mathrm{drift}} = t_{\mathrm{delay,pri}} - t_{\mathrm{delay,sec}} = \frac{Q_{\mathrm{pri}}(V_{\mathrm{ds}})}{I_{\mathrm{sw,pri}}} - \frac{Q_{\mathrm{sec}}(V_{\mathrm{ds}})}{I_{\mathrm{sw,sec}}} \tag{3.10}$$

The phase drift correction can be calculated as

$$\Phi_{\mathrm{drift}} = t_{\mathrm{drift}} f_{\mathrm{sw}} \,. \tag{3.11}$$

The effect of phase drift can be compensated for by adding the calculated phase drift to the desired phase shift value. The difficulty with this method is that for the calculation, equivalent time-related capacitance is needed, which is not usually explicitly given in the component datasheet. Another option is, as proposed in Publication IV, to measure the total capacitive charge in a switching leg with a double-pulse tester (Witcher, 2002). For

practical implementation, the precalculated compensation can be saved as a lookup table to the memory of the processor used for the control of the converter.

The charge-based compensation method can also be used to compensate for the drift between the leading and lagging legs in the multi-phase drift modulation. This would require parametrizing Equation (3.10) with the corresponding current and voltage values, for instance, the leading and lagging leg currents and voltages and calculating the phase drift for each phase shift separately.

The challenge with the charge-based method is how to calculate or measure the total capacitive charge of the switching leg. Moreover, the component parameters may vary between individual components. These challenges undermine the practical value of the presented charge-based compensation method, and the controller-based method seems more promising for practical use with the VFM.

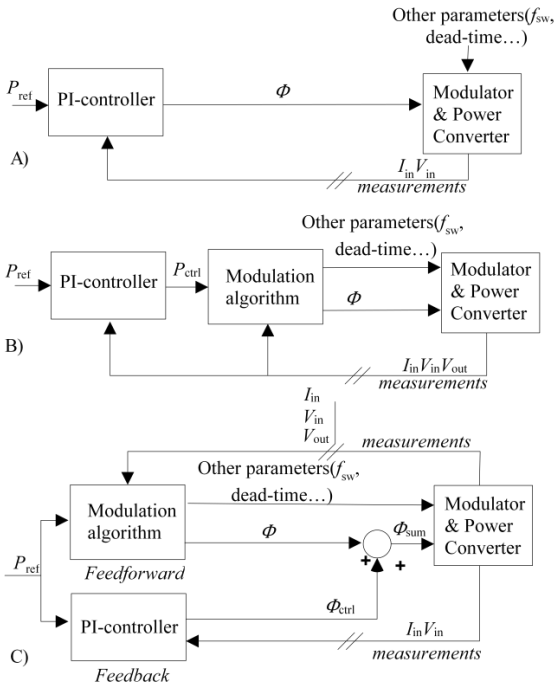


Figure 3.13: Various control approaches for the DAB converter. In approach A, the power is controlled to the desired value by altering the phase shift with a feedback controller. In approach B, the feedback controller controls the power by altering the power reference fed to the modulation algorithm, while the modulation algorithm calculates modulation parameters to achieve the desired current at the switching instant. In approach C, the modulation algorithm is used as the feedforward and the feedback controller controls the power by altering the phase shift. Approach C includes the phase drift compensation, while approaches A and B are feedback control methods that are prone to phase drift effects (reproduced from Publication IV).

3.2.6 Maximum efficiency point tracking

One of the key contributors to the switching losses of a dual active bridge converter is current at the switching instant and the dead time. If the values of these two parameters are large enough and in a right relation to each other, nearly lossless zero-voltage switching will result. The optimal values for these parameters can be estimated as shown in Sections 3.2.2 and 3.2.3. However, exact calculation of optimal values is not an easy task. The circuit nonidealities and measurement inaccuracies can easily cancel out the calculation efforts. The optimal parameters for switching also change constantly as the throughput power and input and output voltages of the converter change. As can be seen in Figure 3.7, a fixed value of I_{ZVS} cannot provide the best efficiency throughout the whole voltage and power range.

In Publication V, the use of maximum efficiency point tracking (MEPT) to improve the performance of variable-frequency modulation (VFM) was studied. The idea of the proposed method is to empirically find the best value for the current I_{ZVS}, while the dead time is kept constant. This is done by using a perturb-and-observe (P&O) algorithm to change the value of I_{ZVS} in the direction in which the efficiency increases. This method is similar to the maximum power point tracking (MPPT) used in photovoltaic (PV) applications, where the operating point is moved in the direction in which the power increases.

In Publication V, the effectiveness of the proposed maximum efficiency point tracking method was evaluated with a laboratory prototype. The performance of MEPT was compared against the traditional VFM with a fixed value of I_{ZVS}. The test results (Figure 3.14) show that the MEPT algorithm improved the efficiency throughout the whole operating region. The efficiency was improved, especially at high voltages where the preselected I_{ZVS} value for traditional VFM was not sufficient for zero-voltage switching.

Based on the measurements (Figure 3.15), the power loss appears to be a nearly convex function of I_{ZVS}, but some local minima and maxima can be observed. The measurement noise was most likely the cause for these local minima and maxima. There is a risk that the MEPT algorithm gets stuck at these points if a large enough perturbation step is not chosen.

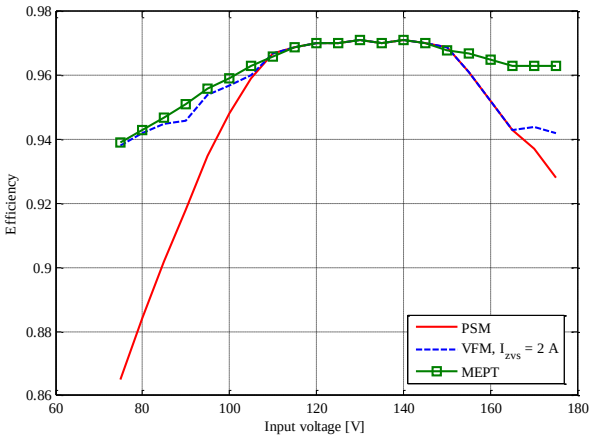
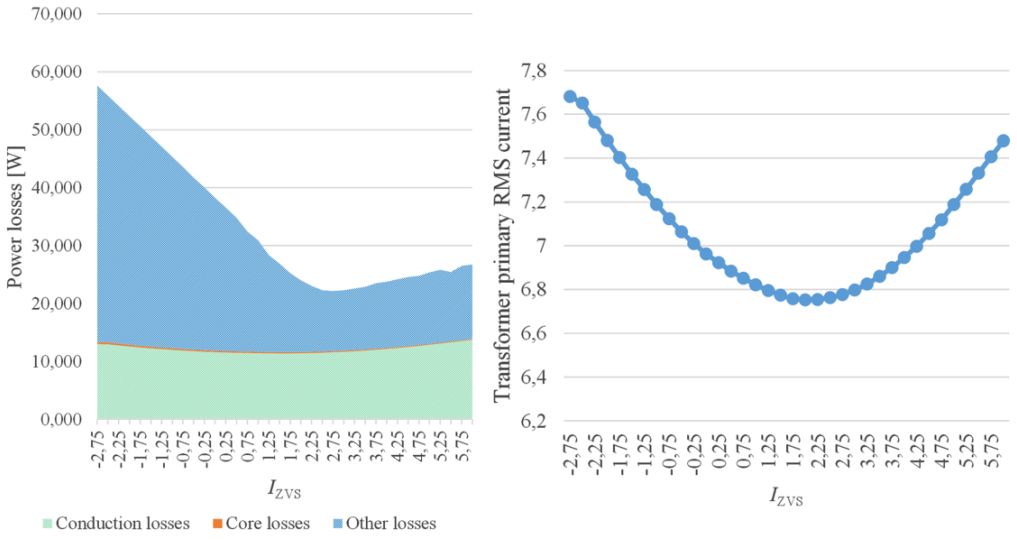


Figure 3.14: Comparison of performance of three different modulation strategies: traditional phase shift modulation, variable-frequency modulation (VFM) with a fixed I_{zvs} value, and variable-frequency modulation with maximum efficiency point tracking (MEPT). The input current is controlled to 6 A and the output voltage is fixed at 250 V. At low input voltages, the preselected value of I_{ZVS} is quite close to an optimal value, and therefore, the performances of VFM and MEPT are similar. At high input voltages, the preselected I_{ZVS} is not large enough for soft-switching as the MEPT algorithm seeks more optimal I_{ZVS} and results in a better performance than VFM (Publication V).



a) b)

Figure 3.15: Conditions in which the converter loss minimum is found. a) Power loss distribution and b) variation of the transformer primary RMS current as a function of I_{ZVS}. Measured in an operating point where V_{in} = 75 V, V_{out} = 250 V and I_{in} = 6 A (reproduced from Publication V).

4 Conclusions

In this doctoral dissertation, two galvanically isolated DC-DC converter topologies were studied. The study was focused on modulation methods, efficiency improvement, and bidirectional power transfer. The power conversion efficiency results presented in this dissertation were determined by measuring the currents and voltages from the converter input and output terminals with the tools presented in Appendix A. The main scientific contributions of this dissertation are demonstration of the operation of the RPP converter in the reverse power mode, development of the variable frequency modulation method for the DAB converter, explaining the birth mechanism of the phase drift phenomenon, and development of the phase drift compensation methods.

In Publication I, operation of current-fed resonant push-pull (RPP) was demonstrated with a 10 kW laboratory prototype, and the principles for dimensioning of the components were given. The advantages and disadvantages of the RPP topology were discussed. The current-fed resonant push-pull converter showed promise for low-voltage high-current applications such as a solid oxide fuel cell. A peak efficiency of 93.7% was achieved with the laboratory prototype. The efficiency was degraded because of the need for overdimensioning the transistor to withstand transient voltage overshoot caused by the boost inductor combined with an insufficient voltage clamping speed of the active snubber. Moreover, the copper losses of the noninterleaved center-tapper transformer degraded the efficiency. It was observed that in the RPP, special attention has to be paid to the snubber transistors and their intrinsic body diodes.

In Publication II, the current-fed resonant push-pull topology and its modulation scheme were modified to enable the bidirectional operation, thereby making the RPP suitable for applications where anode protection of the SOFC is needed. The operation of the RPP in the reverse power mode was evaluated with a 5 kW laboratory prototype, and a peak efficiency of 95.9% was achieved. The bidirectional resonant push-pull converter provides an additional benefit over the traditional RPP that the secondary bridge can be used as an active rectifier, which further reduces the losses in the forward power transfer mode. The drawback is the increased number of active components. The high number of components together with the need to overdimension the transistors turned the research interest toward other topologies. For example, the dual active bridge converter with a full-bridge primary and a half-bridge secondary have the same number of active components but a better soft-switching capability.

In Publication III, a variable-frequency modulation (VFM) algorithm for a dual active bridge (DAB) converter was developed, and its effectiveness was demonstrated with a laboratory prototype. The origins of the phase drift phenomenon were studied, and a method to estimate the magnitude of the phase drift was provided. The study also presented guidelines for selecting an optimal dead time and value for the current at the switching instant. However, it was pointed out that calculations are prone to errors caused by component variances and the highly nonlinear nature of the capacitances of a switching device. It was acknowledged that a single current value at the switching instant with a

fixed dead time could not provide the best efficiency throughout the whole operating region. The proposed VFM method showed a significant efficiency improvement compared with the traditional phase shift modulation despite the increased switching frequency at light loads. The efficiency was improved up to 10 percentage points at a point where the converter was operated far from its nominal voltage conversion ratio. One of the key benefits of the VFM method is that it can extend the soft-switching region without introducing circulating currents as it does not have a zero-voltage sequence unlike multi-phase shift modulation techniques. The drawback of the VFM method is that it will lead to high switching frequencies at light loads. This will increase gate driving losses and conduction losses because of the AC resistance. The changing switching frequency can also cause challenges to compliance with the EMC standards.

In Publication IV, the study on the phase drift phenomenon was extended to the hard-switched mode, and the origins of the phase drift phenomenon were explained in detail. The effects of phase drift on the power transfer of dual active bridge converter were demonstrated with measurements by using several different input-output voltage ratios. The measurement results show that the phase drift phenomenon cannot be explained solely by the dead time, but it is instead a result of the charge/discharge times of the transistor parasitic capacitances. Two methods, a charge-based and a controlled-based one, were introduced to compensate for the phase drift. The proposed controller-based method is effective and easy to implement. However, the controller-based method is limited to modulation methods that are using only one phase shift to control the power flow. The proposed charge-based compensation method can be applied to sophisticated modulation schemes where the zero-voltage sequence is present. The charge-based compensation of the zero-voltage sequence originating phase drift was not studied in this doctoral dissertation. Moreover, the need for detailed knowledge of component capacitances hinders the practical value of the proposed charge-based method.

In Publication V, a maximum efficiency point tracking (MEPT) algorithm was studied to improve the performance of VFM by varying the current at the switching instant. The proposed MEPT method showed a clear efficiency improvement over the VFM with the fixed current value at the switching instant. It was acknowledged that the proposed method might suffer from convergence problems if the current and voltage measurements are noisy. Further, the selection of the perturbation step size was considered one possible source for convergence problems. The clear benefit of the MEPT method is that it provides a holistic approach to the efficiency improvement.

The study showed that both the studied topologies, the current-fed resonant push-pull and the dual active bridge converter, have the potential to be used for power conversion of a solid oxide fuel cell. The dual active bridge converter is a bidirectional converter and, therefore, a potential topology for anode protection of a solid oxide fuel cell with reverse bias current. The study also showed that the resonant push-pull converter can be modified to enable bidirectional operation, and can thus be used for anode protection. The potential need for a transistor overdimensioning hinders the attractiveness of a current-fed resonant push-pull converter. The dual active bridge, on the other hand, has a low number of

passive components, and the soft-switching capability makes it an attractive topology. However, its efficient use in an application where the voltage conversion ratio and the load current are varying may require the use of sophisticated modulation methods. These modulation methods, however, do not come without problems, and solving these problems requires extra design effort.

4.1 Suggestions for future work

The current-fed resonant push-pull converter was selected for the study owing to its attractive features for solid oxide fuel cell applications: a low current ripple, a high voltage conversion ratio, and galvanic isolation. Further, the current-fed resonant push-pull converter was stated to have several advantages over the traditional voltage-fed converter. One of the mentioned advantages is its insensitivity to switching asymmetry. The study led to a thought that the traditional voltage-fed converter might, after all, be worthy of a more in-depth study. The concerns of switching asymmetry may be exaggerated as the modern microcontrollers and gate driving circuits are capable of very accurate gate drive. Moreover, the use of a voltage doubler secondary in voltage-fed push-pull would help to prevent transformer saturation, as shown in (Väisänen et al., 2010). The voltage-fed push-pull converter has the potential for a straightforward converter structure because both of its switches are low-side switches, and a separate isolated high-side gate drive is not needed.

In the variable-frequency modulation scheme presented in this doctoral dissertation, the current at the switching instant was used as an input variable for the modulator. Throughout this study, effort was made to extend this principle to the multi-phase shift modulation. However, extending this method to multi-phase shift modulation faced significant difficulties because of the phase drift phenomenon. The controller-based compensation method presented in this doctoral dissertation was not of any help because the phase drift in the multi-phase shift modulation is distributed into two or three separate phase shifts. The charge-based compensation method could provide an answer to this problem, but the implementation would be complicated because of the number of different parameters. The problems related to the multi-phase shift modulation are not yet overcome, and further study is needed.

Another finding made in the course of the study is the opportunity to alter the dead time to achieve zero-voltage switching. Other authors have already made some studies on this topic but in the context of variable-frequency modulation. As current at the switching instant is controlled to a known value with the VFM, the implementation of a variable dead time could be significantly easier.

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Appendix A: Measurement equipment

The following measurement devices were used in the measurements of this doctoral dissertation:

Resonant push-pull converter:
Tools used for efficiency measurement:

- Multimeter (primary current): Fluke 8840A
- Shunt resistor (primary current): 250A/150mV
- Multimeters: Fluke 187

Other tools:

- Oscilloscope: LeCroy LC574A
- Voltage probe: Tektronix P5200A
- Current probe: LeCroy AP015
- LCR meter: HP 4284A

Bidirectional resonant push-pull converter:
Tools used for efficiency measurement:

- Multimeters: Fluke 8845A
- Shunt resistor: 250A/150mV

Other tools:

- Oscilloscope: Tektronix MSO4104
- Voltage probe: Tektronix P5205
- Current probe: Tektronix A6303

Dual active bridge converter:
Tools used for efficiency measurement:

- Multimeters: Keysight 34461A

Other tools used:

- Oscilloscope: LeCroy LC574A
- Voltage probe: Tektronix P5200A
- Current probe: LeCroy AP015
- LCR meter: HP 4284A

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Design of 10 kW resonant push-pull DC-DC converter for Solid Oxide Fuel Cell applications

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Keywords

«Resonant converter», «ZCS converters», «Design», «Fuel cell system»

Abstract

In this paper, a 10 kW current-fed DC-DC converter using resonant push-pull topology is demonstrated and analyzed. The grounds for component dimensioning are given and the advantages and disadvantages of the resonant push-pull topology are discussed. The converter characteristics and efficiencies are demonstrated by calculations and prototype measurements.

Introduction

Solid oxide fuel cells (SOFC) represent a nascent technology that could be used for clean and efficient energy production. A single SOFC cell consists of porous anode, cathode and of a solid metal oxide electrolyte between them. The fuel, which can be pure hydrogen or hydrocarbon based, is fed to the anode and air is fed to the cathode. Oxygen molecules enter the cathode/electrolyte interface and extract electrons from the cathode. The resulting oxygen ions react with the fuel at the anode-electrolyte boundary and this produces electric current and depending on the fuel also reaction by-products such as pure water, carbon dioxide and heat. The ideal standard potential, or H2 oxidation potential, is 1.229 V. This ideal single cell voltage is reached when pure hydrogen and oxygen reacts at normal temperature and pressure. The total fuel cell stack voltage depends on how many single fuel cells are connected together and what is the final reaction voltage for each cell [1], [2].

The achievable electrical efficiency of SOFC can range from 50% to 75% depending on the fuel and operating conditions [3]-[5]. With combined heat and power production the total efficiency can be over 80% [6], [7]. The output voltages of individual fuel cell stacks are usually below 100 V_{dc} while the three phase grid interconnection with line-to-line voltage of 400 V_{ac} requires inverter input voltages in the range of 410-1000 V_{dc} [7], [8]. The adequate inverter input voltage can be obtained either by connecting the fuel cell stacks in series or by using a boosting DC-DC converter, which also can provide galvanic isolation from the grid. The DC/DC conversion stage is also used to accurately control the current drawn from the cell, as the available stack current is a function of the process

control parameters and as the fuel cell ramp-up is a slow process, sudden load variations could lead to stack overloading, fuel starvation and eventually stack failure.

The DC-DC converters suitable for fuel cell applications can be divided into two main categories: voltage-fed converters and current-fed converters. Compared with voltage-fed converters, the current-fed converters have inherently a lower input current ripple because of the input inductor providing voltage boosting and filtering, a lower rectifier diode voltage stress because of reduced voltage ringing at the secondary, and a smaller transformer turns ratio because of the operating principle of boosting. The current-fed converter is also more tolerant of switching-asymmetry-induced DC offsets in the transformer magnetizing current; a quality that reduces the risk of transformer saturation and current overshoots [9].

The DC-DC converter presented in this paper is based on the resonant push-pull boost topology presented by Kwon et al. [10]. The converter is part of a 10 kW power SOFC power conditioning unit designed for a fuel cell stack with operating area of 40-60 V and 200 A. In the second section the prototype system is introduced in brief. In the third section the most relevant design equations for each circuit component is given. The measurement results and discussion about the factors affecting the resonant push-pull efficiency are given in the fourth section and in the final section, the advantages and disadvantages of the resonant push-pull topology are summarized and conclusions are made.

The SOFC power conditioning unit

Overview of the power conditioning unit

The power conditioning unit including the DC-DC converter and a commercial grid-tie inverter were successfully integrated to a SOFC demonstration unit designed and operated by VTT Technical Research Centre of Finland [11]. The components used in the resonant push-pull converter prototype are listed in Table I.

Table I: Prototype component values

Component	**Description**
Input inductor L_1	AMCC168s, 11 turns of 35 mm^2 stranded wire in one layer, air gap 2.8 mm, nominal inductance 25 μH. Maximum peak-to-peak current ripple @ 200 A < 2%.
S_1 & S_2	2 x 2 x IXFN180N20, 200 V, $R_{DS(on)}$ = 0.010 Ω @ 25 °C
S_3 & S_4	2 x IXFN180N20
Transformer	2 parallel PM114/93 N87 cores, 2 + 2 turns of 48 mm^2 Litz primary, 12 turns of 6.3 mm^2 Litz secondary
Snubber capacitors C_{c1} & C_{c2}	2 x 3 x 20 uF polypropylene, 37.5 mm
Resonant capacitors C_{r1} & C_{r2}	2 x 2 x 680 nF polypropylene, 27.5 mm
Rectifier diodes D_1-D_2	2 x DSEI2x101-12A, 1200 V

Resonant push-pull DC-DC converter

The schematic of the resonant push-pull converter can be seen in Fig. 1.

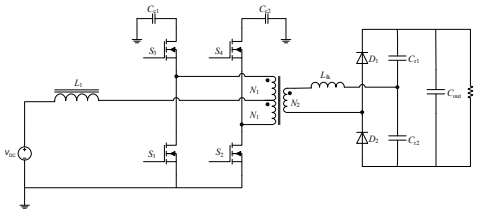

Fig. 1: Schematic of the resonant push-pull converter.

The theoretical converter waveforms and operating modes for D > 0.5 can be seen in Fig. 2. The analysis for D < 0.5 is omitted due to space restrictions.

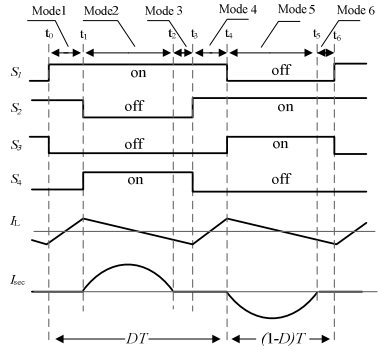

Fig. 2: Theoretical operation modes for resonant push-pull converter with D > 0.5.

Mode 1

At t_0 transistor S_1 is turned on while S_2 still conducting. The input inductor current begins to rise with rate determined by V_{DC}/L_1 and the current is divided equally between S_1 and S_2. The voltage across all the windings is zero, the rectifier diodes are reverse biased and no current is transferred into secondary.

Mode 2

At t_1 transistor S_2 is turned off while S_1 still conducting. The input inductor current begins to decrease with rate determined by

$$\frac{0.5V_{\text{pri(max)}} - V_{\text{DC}}}{L_1}, \tag{1}$$

where $V_{\text{pri(max)}}$ is the maximum voltage seen by all the primary components and it can be calculated from

$$V_{\text{pri(max)}} = \frac{V_{\text{DC}}}{1-D}. \tag{2}$$

Current starts to flow in the transformer secondary as diode D_1 forward biases. The transformer secondary current can then be expressed as

$$i_{\text{sec}}(t) = \frac{nV_{\text{pri(max)}} - V_{\text{Cr}}}{Z_{\text{r}}} \sin \omega_{\text{r}}(t - t_1) \tag{3}$$

The damping caused by the circuit resistances which reduces the resonance amplitude is not accounted in (3). The transformer turns ratio n is $(2N_1)/N_2$. The characteristic resonant frequency and impedance is obtained from

$$\omega_r = \frac{1}{\sqrt{L_{lk} C_r}} \quad Z_r = \sqrt{\frac{L_{lk}}{C_r}} \quad C_r = C_{r1} + C_{r2} \tag{4}$$

The initial resonant capacitor voltage V_{Cr1} can be derived using the maximum resonant capacitor voltage ripple assuming that the converter is symmetrically operated and the output voltage is equally divided between the resonant capacitors.

$$V_{Cr} = \frac{V_{out}}{2} - \Delta V_{Cr}, \tag{5}$$

where the maximum capacitor voltage deviation from the average voltage is

$$\Delta V_{Cr} = \frac{I_{load}}{\frac{2}{T}(C_{r1} + C_{r2})}. \tag{6}$$

The transistor S_4 is turned on shortly after instant t_1 with zero voltage switching, as the transistor body diode is conducting. The sum of magnetomotive forces in the transformer is zero

$$N_1 i_{pri1}(t) - N_1 i_{pri2}(t) - N_2 i_{sec2}(t) = 0 \tag{7}$$

and the input current is sum of the primary currents, so the transistor currents at mode 2 are

$$i_{S1}(t) = \frac{i_{L1}(t)}{2} + n i_{sec}(t) \quad i_{S4}(t) = -\frac{i_{L1}(t)}{2} + n i_{sec}(t). \tag{8}$$

Mode 3

In this mode the secondary diodes are switched off with zero current, which practically eliminates the reverse recovery effects. The input inductor current is divided equally between switches S1 and S4 so that

$$i_{S1}(t) = \frac{i_{L1}}{2} \quad i_{S2}(t) = -\frac{i_{L1}}{2} \tag{9}$$

Mode 3 does not occur if the secondary current does not become zero before t_3. In that case the secondary current is cut off in mode 2 at t_3 and the current is decreasing at rate

$$\frac{di_{sec}(t)}{dt} = \frac{0.5V_{out} + \Delta V_{Cr}}{L_{lk}} \cdot 10^{-6} s \tag{10}$$

This rate of change in current determines the maximum diode reverse recovery current and recovery time, if operating the converter without mode 3. Operation in modes 4-6 is similar as in modes 1-3.

Component dimensioning

In this section the equations and principles needed for dimensioning and scaling of the magnetic components, semiconductors and capacitors is presented.

Input inductor

Inductor design is an important part of the converter design process, especially in fuel cell applications where input current ripple should be low. Desired current ripple rate can be achieved and inductor core losses can be lowered by using large input inductance. However, large inductor will increase the size and price of the converter. Therefore, the inductor design is a tradeoff between the current ripple rate, converter size, losses and price of the components. A suitable capacitor at the converter input will reduce the input current ripple even further depending on the current source output impedance. Based on the desired input ripple current percent $r \in [0,1]$, the required inductance can be determined from

$$L \geq \frac{V_{\mathrm{DC}}|0.5-D|}{I_{\mathrm{L}} f_{\mathrm{sw}} r} \tag{11}$$

The main limiting factor for input inductor scaling is current. If using thick copper foil windings as required by the large current the number of turns and thus stacked layers must be kept low in order to avoid excess ac winding losses [12], [13]. The problem is that the low turns count increases the ac ripple current and thus increases both winding and core losses. This problem has been addressed in [14] by using a separate thick dc winding and a thin ac winding on the same core. Both dc and ac current components are divided between the windings according to the winding impedances.

Another design approach is to limit the ac current component by increasing the inductance. This requires a gapped core in order to store all the energy and a wide winding window in order to compensate the increase in dc resistance due to larger number of turns. This approach practically eliminates the need for input capacitors. If considering an inductor using AMCC168C gapped core with operating conditions of 30 V and 345 A like in [14] in a resonant push-pull converter, the core and gap losses dominate at smaller inductance values and high ripple currents and at larger inductance values the dc losses are dominant. The dc and ac winding losses can be pushed very low by using a gapped amorphous C-core with a wide winding window, but there can be relatively high additional gap losses, which degrade the efficiency [15]. On the other hand, there are no input capacitor losses.

Transistors S1 and S2

The maximum voltage which the transistors and all other primary components have to withstand is acquired from (2). In case that the resonant half period length $\sqrt{(L_{\mathrm{lk}}C_{\mathrm{r}})}\pi$ is smaller than $(1\text{-}D)T$, which allows mode 3 to occur, the RMS current of the main transistors can be calculated from

$$I_{\mathrm{S1\&S2(RMS)}} = \sqrt{\frac{1}{T}\int_0^{\sqrt{L_{\mathrm{lk}}C_{\mathrm{r}}}\pi}\left(n\frac{nV_{\mathrm{pri(max)}}-V_{\mathrm{Cr}}}{Z_r}\sin\omega_{\mathrm{r}}t+\frac{I_{\mathrm{L}}}{2}\right)^2 dt+\frac{1}{T}\int_0^{DT-\sqrt{L_{\mathrm{lk}}C_{\mathrm{r}}}\pi}\left(\frac{I_{\mathrm{L}}}{2}\right)^2 dt} \tag{12}$$

In case that $\sqrt{(L_{\mathrm{lk}}C_{\mathrm{r}})}\pi$ is larger than $(1\text{-}D)T$, the RMS current of the main transistors can be calculated from

$$I_{\mathrm{S1\&S2(RMS)}} = \sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(n\cdot\frac{nV_{\mathrm{pri(max)}}-V_{\mathrm{Cr}}}{Z_r}\sin\omega_{\mathrm{r}}t+\frac{I_{\mathrm{L}}}{2}\right)^2 dt+\frac{1}{T}\int_0^{(D-0.5)T}\left(\frac{I_{\mathrm{L}}}{2}\right)^2 dt} \tag{13}$$

Maximum transistor losses are strongly depedent on the conduction losses as the input voltage is low and current is high. At transistor turn-on the stray inductances delay the current rise allowing the voltage across the transistor to fall before significant overlap between voltage and current occur and thus the only significant switching losses result from transistor turn-off [16], [17]. The conduction losses in the resonant push-pull converter are inherently higher than in the full bridge boost topology [18], [19] as the maximum primary voltage (2) is twice as high and transistors with higher voltage rating must be used. The MOSFET on-state resistance increases together with the transistor voltage rating, so the higher primary voltage comes with a penalty.

The knowledge of MOSFET avalanche characteristics is very important in the converter scaling. The maximum avalanche energy in the resonant push-pull converter depends on the primary stray inductances and current and the maximum avalanche current can occur with $D < 0.50$ being the peak reflected resonance current. With $D \geq 0.50$ the maximum avalanche current equals to half the input current at mode 1. There are two recognized avalanche failure mechanisms in MOSFETs. First is the activation of the parasitic bipolar transistor, which causes a localized thermal runaway amplified by the negative temperature coefficient in the BJT. This phenomenon is related to high current densities and fast turn-off transitions, where there may be voltage build-up across the very small resistance

between the body and the source, where the BJT base-emitter junction is formed. Another mechanism is the overall increase in junction temperature caused by the avalanche energy dissipation and other loss mechanisms in the MOSFET [20]. The temperature distribution is not necessarily uniform across the semiconductor area, but there may be hotspots especially close to the bond wires due to higher current density and the imperfections in the semiconductor structure can also cause variations in the thermal resistance [21]. The intrinsic carrier concentration increases with temperature due to reduced energy bandgap and when the intrinsic carrier concentration is equal to the background doping concentration, the device is not able to support the applied voltage anymore. As the critical temperature in reached, a local mesoplasma with peak temperature in excess of 1000 °C can form and cause permanent damage [22].

MOSFET conduction losses, which dominate in the low voltage converters, increase with temperature due to rise in the drain-source resistance. As the current rating of an individual converter module increases, the cooling requirements in order to keep the junction temperatures and losses at desired level also increase and thus larger heatsinks and more airflow is needed.

Transistors S3 and S4

Fig. 3 together with (14) and (18) illustrate the effect of resonant half period length in snubber transistor current and losses.

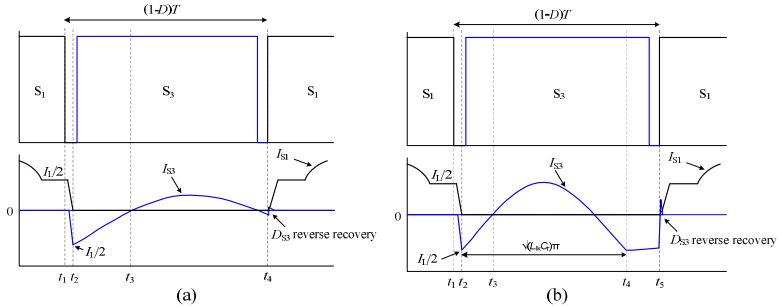

Fig. 3: Snubber transistor currents while operating without mode 3 (a) and in mode 3 (b).

The snubber transistor rms current is acquired from

$$I_{\text{snubber(RMS)}} = \sqrt{\frac{1}{T}\int_{t_1}^{t_4}\left(n\frac{nV_{\text{pri(max)}} - V_{\text{Cr}}}{Z_{\text{r}}}\sin\omega_{\text{r}}t - \frac{I_{\text{L}}}{2}\right)^2 dt + \frac{1}{T}\int_{0}^{(1-D)T-\sqrt{L_{\text{lk}}C_{\text{r}}}\pi}\left(\frac{I_{\text{L}}}{2}\right)^2 dt} \tag{14}$$

The last integral term in the current equation is neglected, if the resonance half period is longer than time interval (1-*D*)*T*. If the half period is shorter, the snubber current is limited to half the input current during t_4-t_5, Fig. 3(b). When operating the converter with short resonance period the snubber rms current is significantly increased and the high intrinsic diode forward current combined to large di/dt during diode switch off at instant t_5 lead to increased recovery current peak and switching losses, as seen from the diode section below. Large dv/dt rates at diode recovery combined with high junction temperature can subject the transistor to latchup and/or thermal failure. The current stress and losses on the snubber capacitors are also increased in mode 3.

Transformer

The maximum voltage of one primary winding is half the maximum voltage across both transformer primary windings (2). The secondary voltage is the maximum primary voltage times turns ratio. The maximum RMS currents flowing in the transformer windings can be evaluated from

$$I_{\text{pri(RMS)}} \approx I_{\text{S1\&S2(RMS)}} \tag{15}$$

$$\begin{cases} I_{\text{sec(RMS)}} = \sqrt{\dfrac{2}{T}\int_0^{\sqrt{L_{\text{lk}}C_{\text{r}}}\pi}\left(\dfrac{nV_{\text{pri(max)}}-V_{\text{Cr}}}{Z_{\text{r}}}\sin\omega_{\text{r}}t\right)^2 dt}\ , \sqrt{L_{\text{lk}}C_{\text{r}}}\pi < (1-D)T \\ I_{\text{sec(RMS)}} = \sqrt{\dfrac{2}{T}\int_0^{(1-D)T}\left(\dfrac{nV_{\text{pri(max)}}-V_{\text{Cr}}}{Z_{\text{r}}}\sin\omega_{\text{r}}t\right)^2 dt}\ , \sqrt{L_{\text{lk}}C_{\text{r}}}\pi > (1-D)T \end{cases} \tag{16}$$

The effective leakage inductance taking part in the resonance can be determined for example by referring the leakage of both shorted primary windings to secondary. The transformer design in the resonant push-pull converter is more complicated than in topologies utilizing two winding transformer. Due to center-tapped primary there will be twice as much primary-secondary intersections if interleaving the windings for same MMF distribution than in two winding transformers. The primary and secondary dc resistances are also at least doubled compared to a two winding transformer operated in similar conditions, as illustrated in Fig. 4, where the ac to dc resistance ratios are calculated based on the principles introduced in [13].

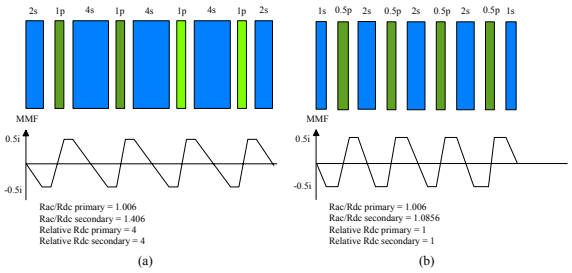

Fig. 4: Calculated resistance ratios in transformers for resonant push-pull (a) and full bridge boost with a voltage doubler (b) interleaved with eight intersections. Both transformers operate with winding thickness of one skin depth and a turns ratio of 1:3.

For the same number of primary-secondary intersections the primary winding in the two winding transformer can be split into parallel turns while maintaining smaller a number of secondary turns. This results in lower dc resistances and ac to dc resistance ratios than in the resonant push-pull transformer and this allows more power to be transferred through a single core in the two winding transformer. The difference in transformer ac resistances between a center-tapped and a two winding transformer increases, if less extensive interleaving or non-interleaved structure is used.

Rectifier diodes

The maximum reverse voltage which the secondary rectifier diodes have to support equals the output voltage while assuming symmetrical operation. The diode RMS current can be calculated from

$$\begin{cases} I_{\text{diode(RMS)}} = \sqrt{\dfrac{1}{T}\int_0^{\sqrt{L_{\text{lk}}C_{\text{r}}}\pi}\left(\dfrac{nV_{\text{pri(max)}}-V_{\text{Cr}}}{Z_{\text{r}}}\sin\omega_{\text{r}}t\right)^2 dt}\ , \sqrt{L_{\text{lk}}C_{\text{r}}}\pi < (1-D)T \\ I_{\text{diode(RMS)}} = \sqrt{\dfrac{1}{T}\int_0^{(1-D)T}\left(\dfrac{nV_{\text{pri(max)}}-V_{\text{Cr}}}{Z_{\text{r}}}\sin\omega_{\text{r}}t\right)^2 dt}\ , \sqrt{L_{\text{lk}}C_{\text{r}}}\pi > (1-D)T \end{cases} \tag{17}$$

The total RMS current can be divided by the total number of parallel diodes in order to get the current for a single diode assuming that the current splits equally between the diodes. With SiC diodes having positive temperature coefficient this is more likely than with SI diodes. The average diode current is

obtained by neglecting the square root and exponent from (17). The diode related switching losses can be estimated from [16], [23], [24].

$$P_{sw} = Q_{\mathrm{rr}} V_{\mathrm{r}} f + E_{\mathrm{C}} = \frac{I_{\mathrm{rm(rec)}} t_{\mathrm{rr}}}{2} V_{\mathrm{r}} f + \frac{1}{2} C_{\mathrm{j}} V_{\mathrm{r}}^2 , \tag{18}$$

where $I_{\mathrm{rm(rec)}}$ is the peak reverse recovery current dependent on the di/dt value at diode turn off (10), t_{rr} is the reverse recovery time, f is the switching frequency, C_{j} is the reverse voltage dependent junction capacitance and V_r is the reverse voltage which the diode need to support [23].The reverse current value is often given in the datasheets as a test circuit limited value I_{rm}, which is not a diode limited value. The $I_{\mathrm{rm(rec)}}$ and t_{rr} values also increase with temperature, so switching losses can get higher than anticipated [24]. The nonlinear diode capacitance C_{j} is charged and discharged at every switching cycle, but this energy is not dissipated in the diode itself, but in the external circuit [16]. The recovery charge before the reverse current peak is also dissipated mainly in the external circuitry, not in the diode itself.

Voltage doubler capacitors

The peak voltage which the individual voltage doubler (or resonant) capacitor has to withstand equals half the output voltage, if assuming symmetrical operation. The voltage ripple for an individual capacitor can be calculated from (6) and the total RMS capacitor current for both upper and lower capacitors is then

$$I_{\mathrm{C_r(RMS)}} = \frac{C_{\mathrm{r1}} \cdot 2\Delta V_{\mathrm{Cr}}}{(1-D)T} \tag{19}$$

The maximum permissible power loss in a capacitor can be evaluated from

$$P_{C(\max)} = \alpha \cdot A \cdot \Delta T , \tag{20}$$

where α is the heat transfer coefficient (3.5 x 10^{-3} W/cm^2 C° for polypropylene), A is the cooling area of the capacitor, which usually is about 85 % of the total outer area, and ΔT is the allowed internal heating of the capacitor. The limits for allowable RMS voltage ripple and current can now be determined from [25]

$$V_{\mathrm{AC_r(max)}} = \sqrt{\frac{P_{\mathrm{C(max)}}}{2\pi f C_{\mathrm{r1}} \tan\delta}} \quad I_{\mathrm{C_r(max)}} = \sqrt{\frac{2\pi f C_{\mathrm{r1}} P_{\mathrm{C(max)}}}{\tan\delta}} , \tag{21}$$

where $\tan\delta$ is the capacitor loss tangent.

The larger the transformer leakage inductance, the smaller the resonant capacitors have to be in order to maintain the desired resonant period length at higher frequencies as seen from (4). The decrease in capacitance results in higher capacitor voltage ripple (6), which in turn requires more capacitor area in order to handle the increased power loss in the capacitor (20), (21).

Converter efficiency

Operating the converter with mode 3 in order to achieve ZCS for the output rectifier diodes may not result in better overall efficiency, if using fast or ultrafast rectifiers. The primary conduction and switching losses increase as the resonant period gets shorter and the reduction in diode switching losses can be overshadowed by the increased primary losses. The decrease in overall converter efficiency while operating the converter in mode 3 is demonstrated in Table II.

Table II: Effect of resonant period length in resonant push-pull efficiency

Input 50.8 V, 3800 W, $D = 0.52$, $R_L = 107\ \Omega$	A	B	C
Leakage inductance	3.2 µH	3.2 µH	3.2 µH
Resonant capacitor C_r	1.36 µF	2.72 µF	4 µF
S_1 & S_2 losses	101	100	100
S_3 & S_4 losses	42	32	23
S_3 & S_4 I_{rms}	25	16	14
Diode conduction losses	14	15	16
Diode switching losses	0.8	0.8	6
Transformer losses	30	30	30
Calculated efficiency	94.78 %	95.03 %	95.14 %
Measured efficiency	94.7 %	95.4 %	95.7 %

In case A the converter is operating with a short resonance period and the decrease in efficiency is mainly caused by increased rms current and intrinsic diode switching losses in the snubber transistors. In case B the converter is operated at the edge of ZCS with very short mode 3. The snubber losses are significantly smaller than in case A. In case C the converter is operated without mode 3. The snubber losses are further reduced and despite of increased rectifier diode switching losses, the overall efficiency is improved. The rectifier diode switching losses are quite low despite the lack of ZCS, as the diode current is not cut-off at its peak value and because the leakage inductance is limiting the di/dt at turn-off. If operating the converter in mode 3, it is advantageous to keep it short in duration.

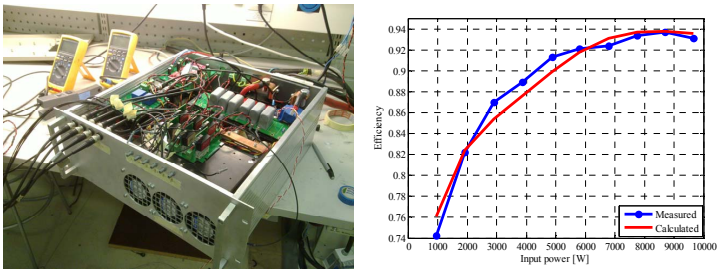

Fig.5: Prototype converter with measured and calculated efficiency sweep over the input power range with input voltage $V_{in} = 50$ V, load resistor $R_L = 45.6\ \Omega$ and resonant capacitor $C_r = 4$ µF.

The dominant losses in the lower power range are switching losses, as the duty cycle range is 0.11-0.56. In the range of 2900-7000 W the snubber transistor S_3 and S_4 switching losses depend mainly on the nonlinear intrinsic diode characteristics as the transistor turn-on and turn-off occur at zero voltage, while the diode experiences large forward current and reverse recovery effects. The transistor S_1 and S_2 switching losses are strongly dependent on the reflected load current value at turn-off and on the gate drive turn-off speed. The peak efficiency of 93.7% occurs at 8700 W. The efficiency was degraded by the non-interleaved Litz-transformer and the intentionally overdimensioned transistors with relatively high $R_{ds(on)}$. Losses from auxiliary devices such as cooling fans were not included in the measurement.

Conclusion

A 10 kW DC-DC converter utilizing a resonant push-pull topology was designed and built. The achieved peak efficiency with the nominal input voltage and load was 93.7% at 8700 W. In the resonant push-pull topology the winding losses are increased due to center-tapped primary and the availability of low $R_{ds(on)}$ MOSFETs is limited due to high primary voltage. Attention needs to be paid to the specifications of the intrinsic diodes in the snubber transistors, as they can experience large forward currents together with large di/dt and transient voltages at turn-off and are thus prone to latch-up and/or thermal failure at high power levels.

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Publication II

Hiltunen J. Väisänen V. Silventoinen P.
A bidirectional current-fed resonant push-pull converter for low voltage, high current applications

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A Bidirectional Current-Fed Resonant Push-pull Converter for Low Voltage, High Current Applications

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***Abstract*— In this paper, a bidirectional current-fed resonant push-pull converter is proposed for energy storage applications where high voltage conversion ratio, high power and low current ripple are needed. In this study, theoretical waveforms of bidirectional RPP are shown, analytical analysis is provided and a modulation method for reverse power flow operation is proposed. Finally, theoretical results are verified with a 5kW prototype. The main contribution of this paper is modifying previously presented resonant push-pull topology and its modulation principle to provide bidirectional power flow.**

I. INTRODUCTION

A current-fed resonant push-pull (RPP) converter [1] has many favorable properties, such as low current ripple, high voltage conversion ratio, wide input-voltage range and galvanic isolation. It is known that the flux imbalance, present in voltage-fed push-pull, is not a serious problem with RPP converter due its high-impedance input inductor [2] and the balancing effect of voltage doubler capacitors [3]. In addition to the balancing effect of voltage doubler will increase the voltage conversion ratio of RPP. This makes it very attractive for applications where high voltage conversion ratio is needed. Another important characteristic of the RPP converter is soft switching, which is achieved in a similar manner as in the quasi-resonant converters [4]. Because of the resonance, zero current switching of the secondary diodes are achieved and the reverse recovery problems of secondary diodes are eliminated [5].

Voltage spikes of the boost switches are a well-known problem in boost derived topologies. In RPP converter this problem is solved by using an active snubber [6] which will limit the energy content of voltage spikes and thereby increase the reliability of the converter. Another favorable property of RPP is that it can utilize the whole duty cycle range with no minimum duty cycle requirement. This allows a wide operating range and therefore even zero output voltage can be achieved. This wide output voltage capability provides soft-starting without any additional start-up circuits [7].

The RPP topology has been studied in several publications and it has shown robust and uninterrupted performance in fuel cell applications [1] [8]. Despite all the favorable properties, the RPP converter is not capable of bidirectional power flow and therefore it cannot be directly adopted for low voltage hybrid power conditioning systems [9] where it would be well suited. Fortunately, the RPP topology can be easily modified for bidirectional applications (Fig. 1). However, previous publications have not shown how to use the RPP converter in bidirectional power flow applications.

This paper studies the operation of RPP converter in the reverse power flow mode. In this study, the theoretical waveforms of bidirectional RPP are shown, analytical analysis is provided and a modulation method is proposed. Finally, the feasibility of the proposed converter is demonstrated with a 5kW laboratory prototype. The main contribution of this paper is to modify previously presented resonant push-pull topology and its modulation principle to provide bidirectional power flow.

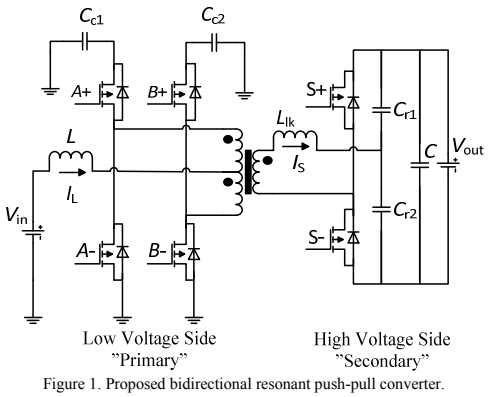

Figure 1. Proposed bidirectional resonant push-pull converter.

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II. ANALYSIS OF THE PROPOSED CONVERTER

The basic principle for the forward power flow operation of resonant push-pull converter is well covered in previous publications [1] [10]. Therefore, the analysis of forward power flow operation is omitted in this context and the main focus is on the reverse power flow operation.

In the reverse power flow operation, where the power is flowing from high voltage side to low voltage side, the operation can be divided into three different modes (Fig. 2). The theoretical waveforms for reverse power flow region are presented in Figure 3. Based on these theoretical waveforms the volt-second balance law for the input inductor can be derived as

$$V_{in}D-\frac{V_{out}D}{n}+\frac{V_{in}}{2}-\frac{V_{out}}{4n}-V_{in}D+\frac{V_{out}D}{2n}=0\,. \quad (1)$$

From (1) the voltage conversion ratio of RPP can be derived as

$$\frac{V_{in}}{V_{out}}=\frac{1-D}{2n}. \quad (2)$$

It can be seen that, the resulting equation is the same as for the forward power flow case.

For the RPP, the soft switching of the secondary side switches is achieved by utilizing the resonance of the transformer leakage inductance L_{lk} and the voltage doubler capacitors C_{r1} and C_{r2}. When either of the secondary side switches is closed, current starts to flow through the transformer secondary winding. This current can be expressed as

$$i_{\sec}(t)=I_{s,peak}\sin\omega_r(t-t_1)\,, \quad (3)$$

where

$$\omega_r=\frac{1}{\sqrt{L_{lk}C_r}},\quad \text{and}\quad C_r=C_{r1}+C_{r2}\,. \quad (4)$$

From (3) and Fig. 3 it can be seen that with a proper selection of L_{lk} and C_r, the secondary switches can be switched at zero-current. Moreover, the lower primary side switches have zero-voltage turn-on and turn-off (Fig. 4), while the upper primary side switches are hard-switched.

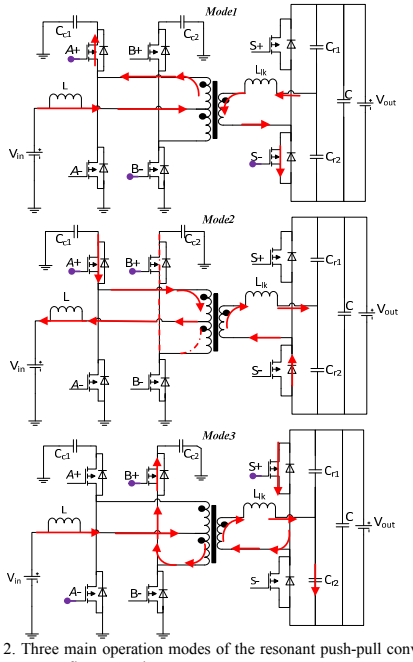

Figure 2. Three main operation modes of the resonant push-pull converter in reverse power flow operation.

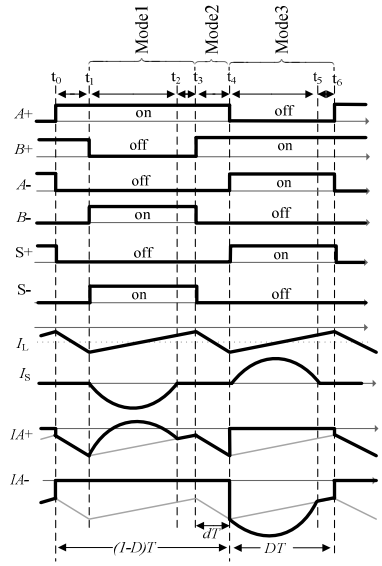

Figure 3. Theoretical waveforms of the resonant push-pull converter in reverse power flow operation.

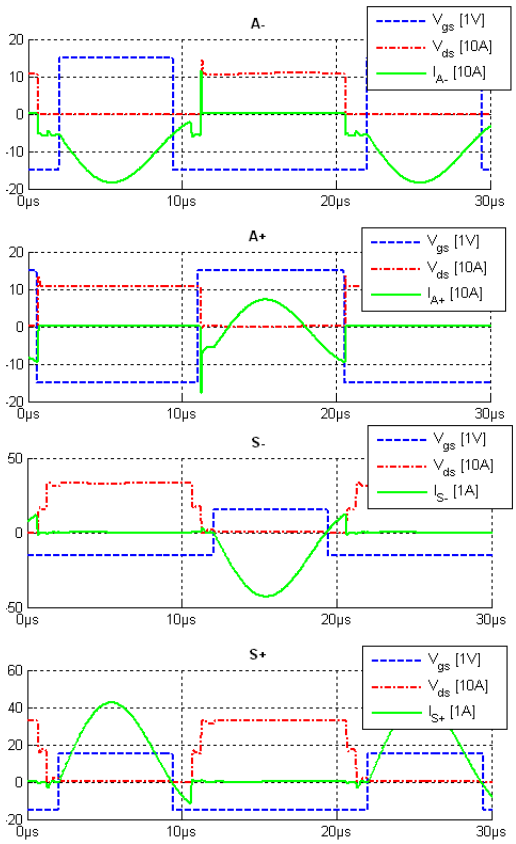

Figure 4. Simulated waveforms of the resonant push-pull converter in reverse power flow operation.

III. MODULATOR CONSIDERATIONS

If the modulator is implemented corresponding to Figure 3, then the voltage conversion ratio will behave as shown in Figure 5a. However, from the control point of view this is not desirable. This is due to the fact that the control variable *D* is not continuous when moving between reverse and forward operation. Therefore the shift between these two modes becomes tricky.

From Figure 3 it can be seen that in order to achieve more reasonable behavior, the duty cycle should be defined as the length of the overlap of the upper primary switches (mode 2) instead of the conduction time of the secondary switches (mode 1). However, by doing so, the implementation of modulator becomes very impractical. A better solution is to modify the modulator input so that

$$D = \begin{cases} d & \text{, when forward power flow} \\ d + 0.5 & \text{, when reverse power flow} \end{cases}, \quad (5)$$

where *d* is the output of controller and *D* is a reference value for the actual modulator. The converter can now be controlled by using only one control signal for both forward and reverse power flow regions. This allows a straightforward control design. However, it should be noted that the controller output has to be limited in the range $d \in [-0.5 \; 1]$ in order to prevent short circuit on the secondary side. The voltage gain of resonant push-pull converter can now be written as

$$G = \begin{cases} \frac{V_{out}}{V_{in}} = \frac{2n}{1-d} & \text{, when } d > 0 \\ \frac{V_{in}}{V_{out}} = \frac{-d+0.5}{2n} & \text{, when } d < 0 \end{cases} \quad (6)$$

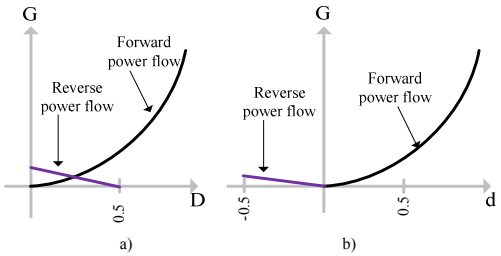

Figure 5. The voltage conversion ratio as a function of duty cycle. a) Duty cycle defined as a conduction time of secondary switches. b) Voltage conversion ratio with the re-defined control variable.

IV. EXPERIMENTAL RESULTS

In order to verify the feasibility of the proposed converter, a 5kW prototype was built (Fig. 6). The prototype is built on a printed circuit board by using TO-247 through-hole semiconductor switches. The modulation and control functions are implemented on a XynergyXS processor card that contains a digital signal processor (DSP) and a field programmable gate array (FPGA). The design parameters and component values used in the prototype are presented in Table 1.

The measured waveforms are shown in Fig. 7. It can be seen that a sinusoidal half-wave current is achieved for the secondary side switches, and therefore zero-current switching is achieved. A peak efficiency of 95.9% was measured for 3kW power at 60V primary side voltage. However, the efficiency is strongly affected by the primary side voltage as can be seen from Fig. 8.

TABLE I. COMPONENT VALUES AND DESIGN PARAMETERS OF BIDIRECTIONAL RESONANT PUSH-PULL PROTOTYPE.

Description	Symbol	Value
Primary side voltage	V_{in}	50-60 V
Primary side current	I_{in}	100 A
Secondary side voltage	V_{out}	660 V
Switching frequency	F_{sw}	50 kHz
Rated power	P	5 kW
Input inductance	L_{in}	20 µH
Snubber capacitor	C_{c1}, C_{c2}	40 µH
Leak inductance	L_{lk}	1.6 µH
Resonant capacitors	C_{r1}, C_{r2}	2.04 µF
DC link capacitor	C_d	60 µF

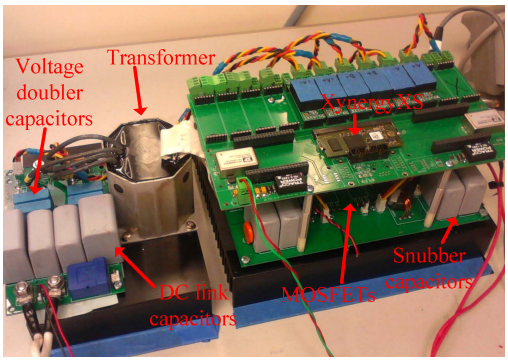

Figure 6. Photograph of the 5 kW bidirectional resonant push-pull converter prototype.

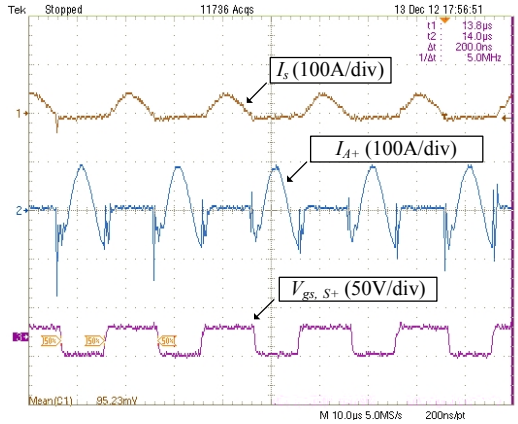

Figure 7. Measured waveforms of the RPP prototype.

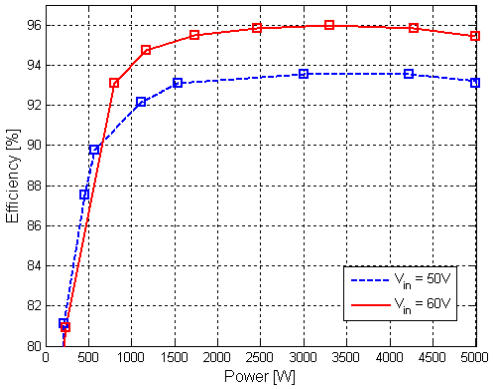

Figure 8. Measured efficiency for 50V and 60V input voltages.

V. CONCLUSIONS AND FUTURE WORK

The resonant push-pull topology has many favorable properties for power conditioning systems where high voltage conversion ratio, isolation and low current ripple are preferred. The RPP topology has been studied in several publications and it has shown robust and uninterrupted performance. However, previous publications are not showing how to use the RPP converter in bidirectional power flow applications.

In this paper, the resonant push-pull converter in reverse power flow mode was studied. Analytical analysis was provided and modulation principles were explained. Moreover, the modulation of both forward and reverse power flow regions were combined under one continuous control variable, and thereby straight forward control design was enabled. Finally, the feasibility of the proposed converter was demonstrated with a 5kW laboratory prototype. The peak efficiency of 95.9% was measured for reverse power flow.

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Publication III

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Variable-Frequency Phase Shift Modulation of a Dual Active Bridge Converter

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Variable-Frequency Phase Shift Modulation of a Dual Active Bridge Converter

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***Abstract*—In this paper, a variable-frequency modulation method for a dual active bridge converter is introduced. The proposed method ensures zero-voltage switching over a wide power range with a minimal circulating current. Unlike previously presented modulation schemes, this modulation method can also be used for half-bridge variants of a traditional dual active bridge converter. The modulation method is given in a closed form, which makes it easy to apply in practice. Further, the phase drift phenomenon is discussed, and a simple phase drift compensation scheme is presented. Finally, a detailed analysis of the proposed modulation method is provided and its feasibility is verified by measurements.**

***Index Terms*—Current control, dc–dc power converters, error correction, modeling, modulation, power system control, switched-mode power supply.**

I. Introduction

OVER the recent years, the dual active bridge (DAB) converter topology has gained popularity because of its favorable zero-voltage switching (ZVS) properties, bidirectional power transfer capabilities, and a low sensitivity to system parasitics. The DAB topology has been widely applied to various energy storage [1] and solid state transformer [2] applications. The DAB is a very attractive topology for applications where bidirectional power flow, galvanic isolation, and a high power density are required.

The DAB topology has been shown to be capable of providing a very high power conversion efficiency [3]. However, the switching and conduction losses of the DAB are heavily dependent on the input-output voltage conversion ratio and the transferred power. When operated outside the nominal voltage conversion ratio, the DAB converter suffers from circulating currents, which significantly increase the conduction losses. Moreover, at light loads, the energy stored in the leakage inductance may not be large enough to discharge the drain-source capacitances of the switching components. This results in a hard-switching that can drastically reduce the power conversion efficiency and increase the electromagnetic interference generated by the converter [4].

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Over the recent years, various modulation strategies have been presented to extend the soft-switching region and reduce the circulating current. The proposed methods have often based on manipulation of the transformer current by introducing a zero-voltage sequence either on the primary or secondary side of the transformer. During this sequence, a zero-voltage is applied to the winding. The zero-voltage sequence is achieved by changing the phase shift between the switching legs of an H-bridge. This gives an additional degree of freedom for the control compared with the traditional phase shift modulation (PSM), where only the phase shift between the primary and secondary H-bridges is controlled. By using a zero-voltage sequence, the soft-switching region of a DAB can be extended and the conduction losses can be reduced. According to the transformer current waveform, this type of a modulation scheme is sometimes called a triangular current mode modulation or a trapezoidal current mode modulation [5]. If a zero-voltage sequence is used in both full-bridges of the DAB, the modulation is sometimes called a dual PSM [6], [7].

All of the aforementioned modulation methods are based on the zero-voltage sequence produced by shorting the primary or secondary winding of a transformer through an H-bridge. By using only one modulation scheme, it is difficult to achieve the best efficiency over the whole operating region. Therefore, different modulation methods are often combined to cover a larger operating region. A hybrid modulation method that combines several different modulation methods has been discussed in publications [8]–[10]. However, the hybrid modulation leads to a complex implementation where the modulation strategy has to be changed according to the operating point.

The use of the zero-voltage sequence can increase the overall efficiency, especially in a low power range, where the hard-switching would normally ruin the efficiency. However, the use of the zero-voltage sequence will increase the transformer RMS current by introducing an additional circulating current inside the H-bridge. This additional current may reduce the efficiency in applications where the transformer conduction losses are dominating. Another limitation of the method is present when a half-bridge variant of the DAB is used. In this case, there is no H-bridge that could be used to generate the zero-voltage sequence. Therefore, modulation methods based on the zero-voltage sequence are not feasible for half-bridge-based converters.

Instead of using a zero-voltage sequence to extend the soft-switching region, a variable switching frequency modulation method can be used. This method is not limited to the full-bridge topologies, but it can also be used for half-bridge topologies. The basic idea of using the variable switching frequency modulation in a DAB converter has been proposed in [11]–[13].

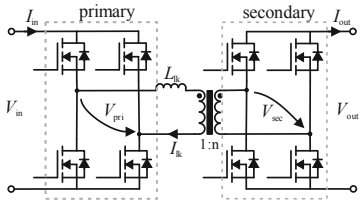

Fig. 1. Circuit diagram of a traditional DAB converter with full-bridges on the primary and secondary side of the transformer.

In [11], a numerical optimization algorithm is used to optimize the switching frequency along with other modulation parameters. This approach gives a freedom to the designer to optimize the modulation method for a specific application and specific hardware. However, it leads to a complicated design process that requires fine-tuning of the parameters. This method also requires the use of a lookup table for implementation. The variable-frequency modulation (VFM) method presented in [12] uses a fixed ratio between the RMS and peak currents to extend the soft-switching range. The method provides a very simple closed-form implementation, but it may result in an unnecessary circulating current and switching at nonoptimal currents.

In this paper, a simple closed-form solution for the VFM is introduced. The presented method is based on switching at a predefined current value. The proposed modulation scheme allows either a ZVS or a zero-current switching (ZCS) depending on how the switching current level is chosen. The modulation method also minimizes the transformer RMS current by limiting the reactive current to some predefined value. The method is most suitable for applications where a half-bridge variant of the DAB converter is preferred over the traditional full-bridge. The feasibility of the proposed modulation method is mainly limited by the transformer ac resistance, turn-off losses, and the gate driving losses.

In this paper, the effect of the phase drift phenomenon [14] is also discussed. The phase drift can distort the phase-shift-to-power relationship in the power flow analysis, which may lead to the failure of the traditional DAB power equation. It can also interfere with the proposed VFM method. The paper introduces a simple phase drift compensation scheme that ensures a proper operation of the variable-frequency modulation. Finally, the effectiveness of the modulation method is demonstrated with a laboratory prototype.

The main contribution of the paper is a closed-form algorithm for the VFM and a generalized power equation for the half-bridge variants of the DAB. The paper demonstrates the effects of the phase drift phenomenon and a method to compensate it. Moreover, a back commutation phenomenon is explained.

II. DAB and PSM

The DAB converter consists of two semiconductor bridges linked together with a high-frequency transformer (see Fig. 1). In the DAB, the leakage inductance of the transformer ($L_{\rm lk}$) is used as an energy transfer element. The power flow through the leakage inductance is controlled by changing the phase shift between the primary and secondary bridges as shown in Fig. 2.

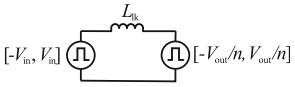

Fig. 2. Simplified operating model of a DAB converter. The model describes the operation of a DAB converter with a sufficient accuracy when the losses are low and the magnetizing inductance is large enough to be neglected.

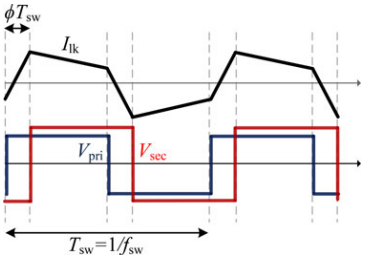

Fig. 3. Idealized operating waveforms of the DAB converter when $V_{\rm in} < V_{\rm out}/n$ and the power flow is from $V_{\rm in}$ to $V_{\rm out}$.

If the losses of the DAB are omitted and the effect of the magnetizing inductance is neglected, the operation of the converter can be simplified into an inductor connected to two equivalent voltage sources (see Fig. 2). By this simplification, idealized operating waveforms can be generated (see Fig. 3). By using the mean-value theorem, the power equation for the converter can be derived as

$$P = \frac{V_{\rm in} V_{\rm out}/n}{f_{\rm sw} L_{\rm lk}} \phi\,(1 - 2\phi) \tag{1}$$

where $f_{\rm sw}$ is the switching frequency and $L_{\rm lk}$ is the leakage inductance of the transformer seen from the primary side. This well-known equation was first presented in [15]. The power equation (1) is sometimes presented in a slightly different form, where the phase shift is presented in radians. However, in this paper, the phase shift ϕ is represented as a percentage of the switching period $T_{\rm sw}$. If radians are preferred, the conversion can be easily made by multiplying the phase shift by 2π.

III. Half-Bridge Variants of the Traditional DAB Topology

In some cases, it is beneficial to use a half-bridge structure instead of a full-bridge (see Fig. 4). The half-bridge converter can be a feasible solution in high-voltage and low-current applications when a low number of active components and a high voltage conversion ratio are needed.

The use of the half-bridge inherently doubles the voltage of the transformer winding. Therefore, the half-bridge can be used to reduce the transformer turns ratio. The voltage doubling effect of the half-bridge allows the use of a smaller leakage inductance in the DAB for the same power. This is very useful for low-power converters, where a high leakage inductance value is required to

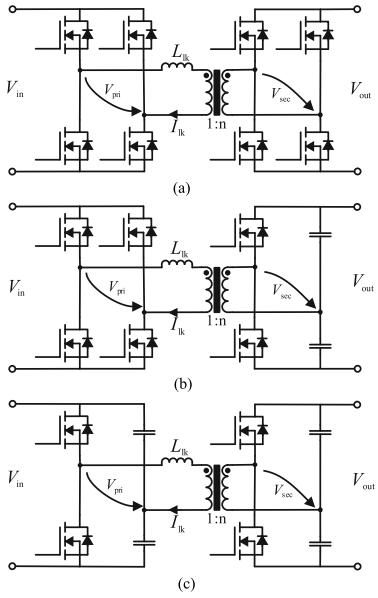

Fig. 4. Three variations of the DAB converter. (a) DAB with a full-bridge primary and a full-bridge secondary. (b) DAB with a full-bridge primary and a half-bridge secondary. (c) DAB with a half-bridge primary and a half-bridge secondary.

limit the power to a desired level. Often, a high inductance value has to be achieved by using an external inductor in series with the transformer. This bulky external inductor may be avoided by using the half-bridge variant of the DAB. The downside of the half-bridge is that it doubles the transformer current compared with an equivalent full-bridge design. Thereby, it increases the conduction losses.

Another benefit gained by the half-bridge is the dc blocking capability. The capacitors used in the half-bridge act as a dc blocking element. This prevents transformer saturation [16] often considered a problem in the DAB converters [17]. The half-bridge can also be used to simplify the converter design; it reduces the number of semiconductor switches and thereby the number of gate drivers and auxiliary components.

The usability of the half-bridge is limited by the increased current stress on the transformer and the power switches. Further, the additional losses in the half-bridge capacitors may restrict the usability. It is often stated that the full-bridge converter can provide a higher power density than the half-bridge converter. However, with the modern ceramic and film capacitors, a very good capacitance to volume ratio and a good high-frequency performance can be achieved. In addition, space and cost savings can be obtained as a result of the reduced number of components. However, the selection between the full-bridge and the half-bridge has to be made on a case-by-case basis, and for many applications, the full-bridge converter is still the more attractive option.

For the design of a half-bridge DAB, a power equation is needed. Unfortunately, the traditional power flow (1) of the DAB has to be modified for the half-bridge converter. This can be done by assuming that the half-bridge capacitors are large enough to be considered constant voltage sources. In addition, the additional voltage conversion ratio caused by the half-bridge has to be taken into account.

The power equation for the half-bridge converter can be derived from (1) by replacing the voltages $V_{\rm in}$ and $V_{\rm out}/n$ with the equivalent voltages V_1 and V_2. These equivalent voltages can be calculated by reducing the transformer winding voltages ($V_{\rm pri}$ and $V_{\rm sec}$) to the same side of the transformer. This yields

$$\begin{cases} V_1 = h_{\rm pri} V_{\rm in} \\ V_2 = h_{\rm sec} V_{\rm out}/n \end{cases} \tag{2}$$

where $h_{\rm pri}$ is a variable describing the structure of the primary-side bridge and $h_{\rm sec}$ represents the structure of the secondary-side bridge. The variables $h_{\rm pri}$ and $h_{\rm sec}$ are valued either 1 or 0.5 depending on the bridge type

$$h_{\rm pri},\ h_{\rm sec} = \begin{cases} 0.5 & |\text{for half bridge} \\ 1 & |\text{for full bridge.} \end{cases} \tag{3}$$

By using the previous definitions, a generalized power equation for the DAB converter and all of its variants can be written as

$$P = \frac{V_1 V_2}{f_{\rm sw} L_{\rm lk}} \phi \left(1 - 2\phi\right) \tag{4}$$

where $L_{\rm lk}$ is the leakage inductance of the transformer seen from the primary side (V_1 side). As mentioned, the phase shift ϕ is represented in percentage of the switching period.

IV. ZVS OF THE DAB

In traditional phase-shift modulation there is always some amount of circulating reactive current between the H-bridge and the dc link capacitors (see Fig. 5). In the zero-voltage-sequence-based modulation [6], [8] there is a circulating current inside the H-bridge in addition to the circulating between the H-bridge and the dc link capacitors. While the circulating current is an inevitable by-product of the ZVS, it will also increase the conduction losses [5]. Therefore, it is desirable to reduce the circulating current to the minimum amount necessary for the zero-voltage switching.

A. Minimum Requirement for the Discharge Energy

When a switching event is taking place in the DAB, the energy stored in the leakage inductance is used to discharge the output capacitances of the semiconductor switches. This stored energy has to be large enough to enable zero-voltage switching. In order to ensure zero-voltage operation, a sufficient amount of inductor current and a dead time has to be applied.

The amount of current needed to discharge the output capacitances can be calculated as shown in several publications [15], [18]. For zero-voltage switching, the following inequality must

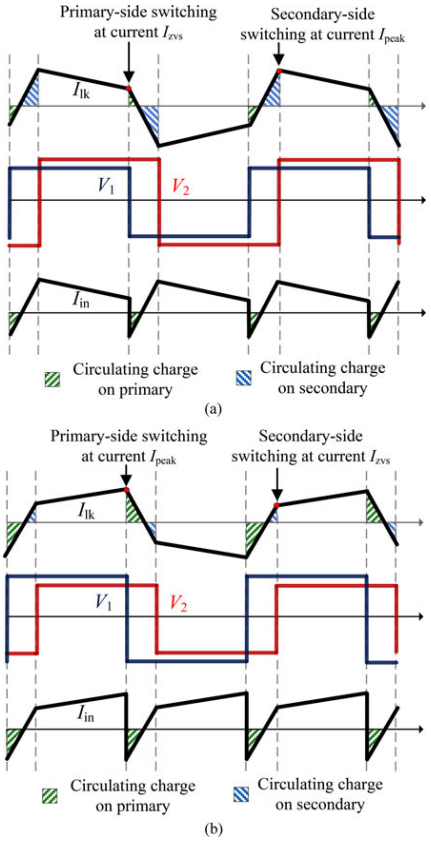

Fig. 5. Idealized operating waveforms of the DAB for two cases. (a) Equivalent secondary voltage (V_2) is higher than the equivalent primary voltage (V_1). The primary-side bridge is zero-voltage switched if the current $I_{\rm zvs}$ is large enough and of the right polarity. The secondary-side bridge is switched at the current $I_{\rm peak}$ and is zero-voltage switched whenever the primary-side bridge is zero-voltage switched (similar switches are assumed for both sides). (b) Equivalent primary voltage (V_1) is higher than the equivalent secondary voltage (V_2). The secondary-side bridge is zero-voltage switched if the current $I_{\rm zvs}$ is large enough and of the right polarity. The primary-side bridge is switched at the $I_{\rm peak}$ current, and it is zero-voltage switched whenever the secondary-side bridge is zero-voltage switched (similar switches are assumed for both sides).

be true:

$$\frac{1}{2}L_{\rm lk}I_{\rm zvs}^2 \geq k\frac{1}{2}C_{\rm o}V_{\rm bridge}^2 \tag{5}$$

where k is the number of switching devices, $I_{\rm zvs}$ is the transformer current at the switching instance, and C_o is the effective output capacitance of the switching device.

B. Back Commutation and the Dead Time

In the case of hard-switching, a dead time between the complementary switching devices is needed to prevent a destructive shoot-through. In a ZVS application, a dead time is needed to complete the zero-voltage transition. If the chosen dead time is too short with respect to the zero-voltage transition time, a hard-switching or a partial ZVS will result. The zero-voltage transition time is the time that is needed for the inductor current to charge or discharge the capacitances of the switching devices. The minimum dead time needed for the zero-voltage transition can be estimated as

$$t_{\rm dead,min} = \frac{Q\left(V_{\rm ds}\right)}{I_{\rm sw}} = \frac{2V_{\rm ds}C_{\rm o,tr}\left(V_{\rm ds}\right)}{I_{\rm sw}} \tag{6}$$

where Q is the charge of the switching leg, $C_{\rm o,tr}$ is the equivalent time-related capacitance of the switching device, and $I_{\rm sw}$ is the current of the switching leg at the switching instance. The current $I_{\rm sw}$ is equal to $I_{\rm zvs}$ or $I_{\rm peak}$ depending on the voltages on the primary and secondary sides (see Fig. 5). The charge Q and the equivalent time-related capacitance $C_{\rm o,tr}$ are functions of drain-source voltage. The capacitance $C_{\rm o,tr}$ is usually given in the datasheet for some fixed value of the drain-source voltage. It must be noted that (6) assumes the current $I_{\rm sw}$ and the voltage $V_{\rm ds}$ to remain constant during the switching transition. In practice, these values change during the transition because of the *LC* oscillation between the leakage inductance and the power switches.

The dead time given by (6) is optimal from the efficiency point of view because it minimizes the conduction time of the body diode. In practice, however, a slightly longer dead time is often required to overcome the inaccuracies in the modulator and the gate driving circuitry. If the dead time is too long, the leakage inductor current can change polarity during the dead time. This will cause the switching leg to back commutate (see Fig. 6), which will lead to increased switching losses. The efficiency in the back commutation case was 92%, while it was 93.7% in the case of Fig. 6(b). The upper limit for the dead time to prevent back commutation can be estimated by assuming linear behavior of the transformer current during the zero-voltage transition. This leads to an inequality

$$t_{\rm dead,max} = \frac{I_{\rm sw}L_{\rm lk}}{V_1 + V_2}. \tag{7}$$

In practice, the transformer current cannot change linearly until the ZVS transition has been completed. Therefore, (7) does not give a fully accurate result and can easily underestimate the maximum dead time. For a better estimation the sum of the zero-voltage transition time (6) and the back commutation time (7) can be used.

In order to achieve an optimal switching transition, a variable length for the dead time is required. Moreover, the dead time should be independently adjusted for both the primary and secondary bridges. In many real-world applications, a fixed dead time is preferred because of the simplicity of the implementation. This may require a tradeoff between the ZVS and the back commutation phenomenon. However, if the current of the switching instance is known and the output capacitance of the switching device is nearly linear within the operating region, a fixed dead time value can be used to achieve sufficient results. Therefore, it would be beneficial if we could force the

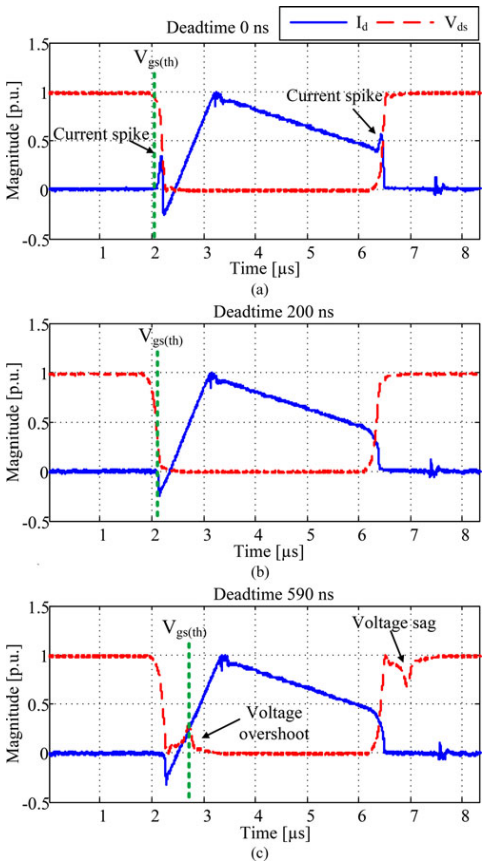

Fig. 6. Three dead time lengths and their effects on the switching waveforms. (a) Dead time is too short to complete full zero-voltage transition. The delivered charge is not enough to fully charge and discharge the capacitances of the switching devices during the dead time. This results in a partial hard-switching that can be seen as current spikes in the figure. (b) Dead time is of the right length, the zero-voltage transition is completed, and the back commutation is prevented. The voltage and current waveforms are smooth without additional overshoots. (c) Dead time is too long. The zero-voltage transition is completed but the inductor current changes polarity and starts to recharge the drain-source capacitances. This results in a back commutation, which can be seen as a voltage sag in the drain-source voltage. The back commutation phenomenon increases the switching losses and the EMI.

switching at a predefined current. The modulation scheme to force switching at a predefined current value is presented in the following.

V. VFM OF THE DAB

In the DAB, the switching frequency together with the leakage inductance defines the maximum power rating of the converter. The selection of the switching frequency is often related to the design process of the magnetic components. Decreasing the switching frequency from its design value would increase the power transfer capability, but is not often possible because of the risk of saturating the magnetic components. Unlike decreasing the switching frequency, increasing the switching frequency limits the power transfer capability of the DAB and reduces the magnetization current of the magnetic cores. While an increase in the switching frequency reduces the power transfer capability, it also extends the soft-switching capability to lower power levels. This makes manipulation of the switching frequency a useful tool for applications where a large soft-switching region is preferred.

A high switching frequency is often undesirable because of the increased switching and gate driving losses. A high switching frequency can also increase the conduction losses as a result of the increased ac resistance. However, a high switching frequency can in some cases provide soft-switching that can compensate for the drawbacks of the increased frequency. Therefore, changing the switching frequency as a function of operating conditions makes sense in cases where the traditional zero-voltage-sequence-based modulation cannot be used to extend the soft-switching region. Altering the switching frequency can be particularly useful in applications where the turn-on losses are dominating over the conduction and turn-off losses. In some cases, the increased switching frequency can also be justified by the side benefits of the soft-switching such as reduced EMI radiation and reduced peak currents.

If we assume that the turn-on losses are dominating over the turn-off losses and all the other losses are considered negligible, it can be argued that the optimal switching frequency would be the lowest switching frequency that provides soft-switching in that specific operating point. This minimum switching frequency can be found by setting the current of the switching instance to the minimum value needed for the zero-voltage switching.

By looking at the power (1) and the idealized operating waveforms in Fig. 3, we can see that the transformer current can be set to a desired value by controlling the switching frequency and the phase shift. By choosing this current value (I_{zvs}) large enough, a ZVS can be achieved. Correspondingly, by setting this current to zero, a ZCS can be achieved.

For the derivation of the VFM algorithm, an equation for the switching current (I_{zvs}) and the phase shift (ϕ) is needed. By using simple algebra and the idealized operational model (see Fig. 2), the equation for the turn-off current can be written as

$$I_{\mathrm{zvs}} = \begin{cases} \dfrac{(4\,|\phi| - 1)\,V_2 + V_1}{4 f_{\mathrm{sw}} L_{\mathrm{lk}}} & |V_1 \le V_2 \\ \dfrac{(4\,|\phi| - 1)\,V_1 + V_2}{4 f_{\mathrm{sw}} L_{\mathrm{lk}}} & |V_1 > V_2\ . \end{cases} \tag{8}$$

By selecting the primary-side input current (I_{in}) as the control variable, the relation between the phase shift and the current reference (I_{ref}) can be derived from (4) as

$$\phi = \mathrm{sign}\,(I_{\mathrm{ref}}) \left(\frac{1}{4} \pm \frac{1}{4} \sqrt{1 - \mathrm{sign}\,(I_{\mathrm{ref}})\, \frac{8 f_{\mathrm{sw}} L_{\mathrm{lk}} I_{\mathrm{ref}} / h_{\mathrm{pri}}}{V_2}} \right). \tag{9}$$

By solving (8) and (9) simultaneously, the algorithm for the VFM can be written as

$$\begin{cases} \phi = \dfrac{1}{4\gamma}\left(\gamma - I_{\mathrm{ref}}\alpha + \mathrm{sign}\left(I_{\mathrm{ref}}\right)\sqrt{\alpha^2 I_{\mathrm{ref}}^2 - 2I_{\mathrm{ref}}\gamma\beta + \gamma^2}\right) \\ f_{\mathrm{sw}} = \dfrac{h_{\mathrm{pri}}V_2}{I_{\mathrm{ref}}L_{\mathrm{lk}}}\phi\left(1 - 2\left|\phi\right|\right) \end{cases} \tag{10}$$

where

$$\alpha = \begin{cases} 1 & |V_1 < V_2 \\ \frac{V_1}{V_2} & |V_1 > V_2 \end{cases} \tag{11}$$

$$\beta = \begin{cases} \frac{V_1}{V_2} & |V_1 < V_2 \\ 1 & |V_1 > V_2 \end{cases} \tag{12}$$

and

$$\gamma = \mathrm{sign}(\mathrm{I}_{\mathrm{ref}})I_{\mathrm{ZVS}}h_{\mathrm{pri}}. \tag{13}$$

This algorithm ensures switching of the low-voltage-side switches at an arbitrary current value (I_{zvs}). In this context, the low-voltage side refers to the side having the lowest value of the equivalent primary and secondary voltages (V_1 and V_2). If we assume similar semiconductor devices for both bridges, the high-voltage side is automatically zero-voltage switched if the low-voltage side is zero-voltage switched.

VI. Limitations of the VFM

The proposed variable frequency modulation ensures switching at a predefined current value and thereby ZVS virtually over the whole region. By selecting the value of the switching current and dead time appropriately, the excess circulating current can be limited. However, when the equivalent primary and secondary voltages deviate considerably from each other, the proposed algorithm gives very high switching frequencies. Correspondingly, a very low switching frequency is obtained when these voltages are close to each other. Because of the hardware limitations, the switching frequency has to be limited to remain within certain predefined limits.

Limiting the switching frequency to a certain minimum value will not affect the zero-voltage switching. This is true because the switching frequency proposed by the algorithm ensures the selected I_{zvs} current. If a frequency below its minimum value is obtained, the minimum frequency will be used. This leads to switching at a higher current value than the selected I_{zvs}. Therefore, the ZVS is achieved but the circulating current is increased.

Limiting the maximum switching frequency will result in the loss of zero-voltage switching. However, the maximum switching frequency limit can often be set so high that it is achieved only in very special occasions (a very low power or a large difference in the equivalent voltages).

The effect of frequency limitation is illustrated in Fig. 7. A schematic diagram of the implementation is presented in Fig. 8. Fig. 7 shows that the region of the minimum switching frequency is large when the reference current is high compared with the required I_{zvs} and small when the reference current is low in comparison. It can also be seen that the switching frequency is related to the transferred power. For a high power, a low switching frequency can be used, but for a low power, a high frequency is needed.

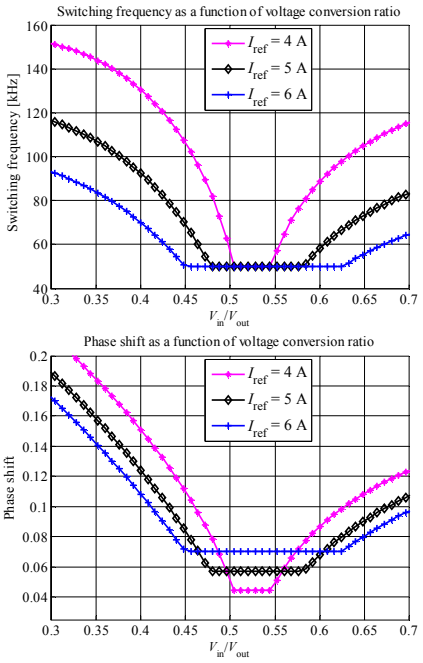

Fig. 7. Switching frequency and phase shift given by the modulation algorithm. In this example, a full-bridge primary, half-bridge secondary converter with a 1:1 transformer is used. The leakage inductance is 26.4 μH and the switching current I_{zvs} is set to 3.5 A.

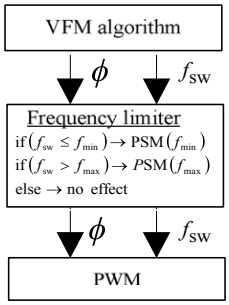

Fig. 8. Switching frequency limitation scheme. When the minimum or maximum frequency level is reached, the traditional PSM is used to continue the operation. The switching frequency limitation is used to prevent extremely high or low frequency values that could damage the hardware.

VII. Feedback Control and Compensation of the Phase Drift

In the derivation of the proposed VFM scheme, an ideal converter was assumed. However, an ideal converter does not exist in reality. Instead, nonidealities in the system will cause an error between the actual system and the power flow (1). The VFM algorithm is derived by taking the same assumption of an ideal converter as in the power flow equation. Therefore, the nonidealities will affect this algorithm also.

In most cases, the voltage and current measurement errors are very small and they do not have a significant effect on the actual algorithm. Further, the leakage inductance ($L_{\rm lk}$), the turns ratio (n), and the switching frequency ($f_{\rm sw}$) are usually well known. Relying on the previous reasoning, it can be stated that the main part of the modeling error of the power flow (1) has to originate from the phase shift (ϕ).

The phase-shift-related error is reported in several publications [14], [19], and it is typically referred to as the phase drift phenomenon. In the previous publications, the phase drift is explained by the effects of the dead time and the power losses of the converter. According to our simulations and measurements, the phase drift is mainly caused by the switching delays of the primary and secondary bridges. Based on our measurements, this is true when the dead time is chosen to match the actual zero-voltage transition time, the converter is zero-voltage switched, and the converter losses are low. In the case of hard-switching and a poorly chosen dead time, the phase drift may behave differently. Owing to the limitations of this paper, the latter case is omitted, and it will be discussed in future publications.

The switching delay of a phase leg is related to the capacitances of the power switches and to the switching current. These capacitances are nonlinear functions of the drain-source voltage [20]. Therefore, the phase drift is severest when the difference between the equivalent primary and the secondary voltage is high, and when the switching currents on the primary and secondary sides deviate considerably from each other. When the equivalent voltages and the switching currents are similar, the phase drift is nearly zero. The magnitude of the phase drift can be estimated by calculating the difference of the switching delays

$$t_{\rm drift} = \frac{Q_{\rm pri}\left(V_{\rm ds}\right)}{I_{\rm sw,pri}} - \frac{Q_{\rm sec}\left(V_{\rm ds}\right)}{I_{\rm sw,sec}}. \tag{14}$$

The effect of the phase drift phenomenon is demonstrated in Fig. 9.

The phase drift problem is severe for converters that are operated outside the nominal operating point with high-capacitance switches, nonsymmetric bridge configurations (full-bridge primary, half-bridge secondary, or *vice versa*) and a high voltage conversion ratio. In modern wide band-gap devices (SiC and GaN), the parasitic capacitance is usually so small that the phase drift may not cause similar problems as with the Si devices. The phase drift phenomenon in the case of hard-switching is not covered in this paper because of its minor effect on the proposed modulation scheme. The phase drift caused by power losses is also omitted in this context as it has only a minor effect on this modulation scheme.

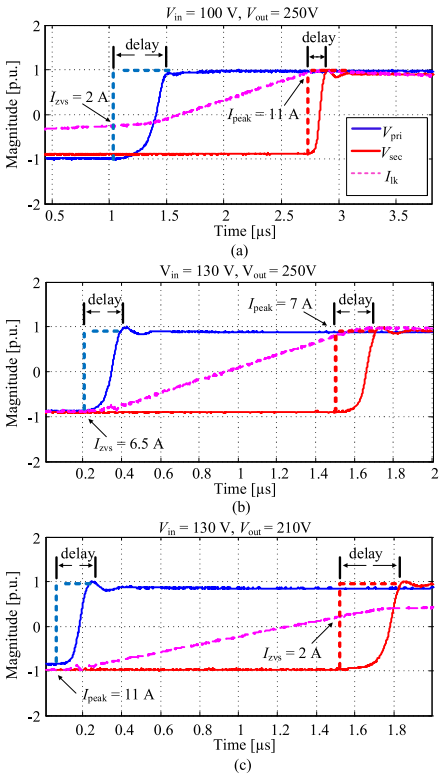

Fig. 9. Measured phase drifts for a DAB converter with a full-bridge primary, half-bridge secondary, and a transformer with a 1:1 turns ratio. For the measurements, STWA88N65M5 MOSFETs were used. (a) Primary-side voltage is smaller than the secondary-side voltage referred to the primary side. The higher voltage and the higher discharging current on the secondary side result in a smaller phase drift on the secondary side. (b) Primary-side voltage is similar to the secondary-side voltage referred to the primary side. The discharging currents are also similar, which results in similar phase drifts on both sides. (c) Secondary-side voltage referred to the primary side is lower than the primary-side voltage. The higher voltage and the higher discharging current on the primary side result in a smaller phase drift on the primary side.

The error caused by the phase drift phenomenon can lead to a failure of the power equation and the VFM algorithm. The phase drift phenomenon can cause severe problems when the modulation algorithm is used in series with the current controller. The current controller will force the error term to zero, which leads to a very different phase shift than is given by the traditional power flow equation. With the VFM algorithm this causes the switching current to drift from its set point ($I_{\rm zvs}$). The phase drift phenomenon can be avoided by using the VFM algorithm as a feedforward term and by compensating the phase drift with a feedback control as shown in Fig. 10.

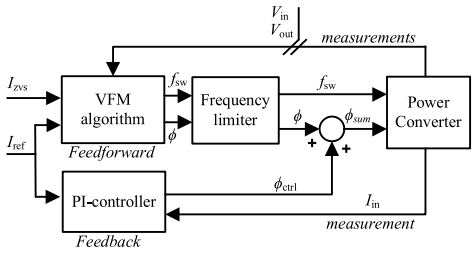

Fig. 10. Phase drift compensation scheme. The VFM algorithm is used as a feedforward, and the phase drift error is compensated by using a feedback controller. The measured voltages ($V_{\rm in}$, $V_{\rm out}$) and current ($I_{\rm in}$) are average values over the switching period. $I_{\rm ref}$ is the desired input current of the converter and $I_{\rm zvs}$ is the desired current value at the switching instant.

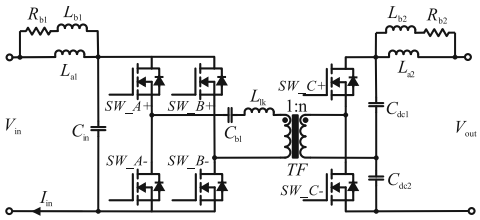

Fig. 11. Schematic diagram of the DAB prototype. Full-bridge on the primary side and half-bridge on the secondary side.

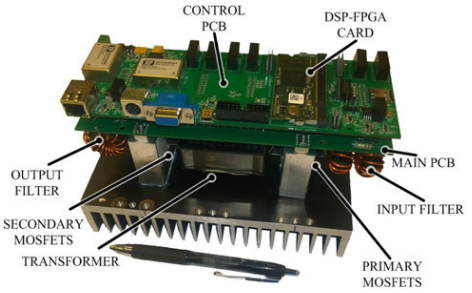

Fig. 12. DAB laboratory prototype. The prototype consists of two printed circuit boards. The bottom one is the main PCB carrying the load current, and the upper one is a control PCB containing the digital signal processor and the measurement electronics. These two PCBs are stacked together by pin headers and mounted on a heat sink.

VIII. Experimental Results

In order to verify the feasibility of the proposed modulation algorithm, a 1-kW prototype was built. The prototype is a variant of the traditional DAB converter with a full-bridge primary and a half-bridge secondary as shown in Fig. 11. The prototype was built on a printed circuit board by using STWA88N65M5 MOSFETs and ADUM3224 gate drivers as shown in Fig. 12. A list of the components and their values is given in Table I.

TABLE I
Component Values for the DAB Prototype

Symbol	Quantity	Value
SW	Power MOSFETs	6 × STWA88N65M5
TF	Transformer	ETD54 N87
n	Turns ratio	1
n1	Primary winding	25 turns 1050 × AWG44 litz
n2	Secondary winding	25 turns 420 × AWG46 litz
$L_{\rm lk}$	Leakage inductance	26.4 μH (internal)
$C_{\rm in}$	Input capacitor	28 × 1 μF/450V ceramic cap.
$C_{\rm dc1}$	Voltage doubler capacitor	14 × 1 μF/450V ceramic cap.
$C_{\rm dc2}$	Voltage doubler capacitor	14 × 1 μF/450V ceramic cap.
$C_{\rm b1}$	Dc-blocking capacitor	10 × 10 μF/25V ceramic cap.
$L_{\rm a1}$	Input choke	63 μH, KoolMu 77930/125μ
$L_{\rm b1}$	Input filter damping choke	31 μH, KoolMu 77930/125μ
$R_{\rm b1}$	Input filter damping resistor	2.2 Ω
$L_{\rm a2}$	Output choke	63 μH, KoolMu 77930/125μ
$L_{\rm b2}$	Output filter damping choke	31 μH, KoolMu 77930/125μ
$R_{\rm b2}$	Output filter damping resistor	2.2 Ω

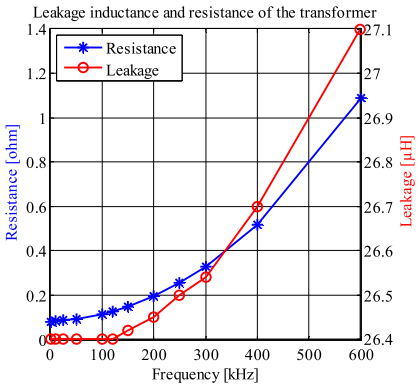

Fig. 13. Leakage inductance and resistance of the transformer as a function of frequency. The measurements are carried out on the primary side with a shorted secondary winding.

The leakage inductance was integrated into the transformer. The transformer was wound on an ETD54 core by using litz wire. The behavior of the leakage inductance and resistance of the transformer is presented in Fig. 13. The winding configuration and the leakage inductance value were not rigorously optimized for the application.

The effectiveness of the proposed modulation method was demonstrated by a set of measurements at various input to output voltage ratios ($V_{\rm in}/V_{\rm out}$ from 0.3 to 0.7) with a fixed dead time of 200 ns. An efficiency comparison of the traditional PSM and the VFM is presented in Figs. 14 and 16. Fig. 14 shows a significant efficiency improvement over the traditional PSM while Fig. 15 shows the efficiency improvement in different load conditions. Fig. 16 illustrates how the VFM scheme forces the switching current to a fixed value by increasing the switching frequency, while the PSM scheme uses a fixed switching frequency that leads to hard switching when operated far outside the nominal voltage conversion ratio.

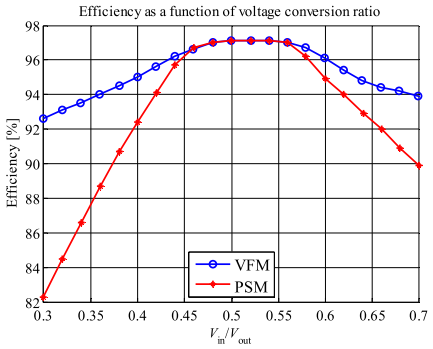

Fig. 14. Measured efficiency for the traditional PSM and for the proposed VFM scheme. During the measurements, the secondary voltage was kept constant at 250 V and the switching current (I_{zvs}) at 3.5 A, and the primary-side current (I_{in}) was controlled to 5 A by using a feedback control to compensate for the phase drift. The VFM algorithm is dynamically seeking the minimum switching frequency that ensures zero-voltage switching. Therefore, it can provide a better efficiency over the operating range than the traditional PSM modulation with a fixed switching frequency.

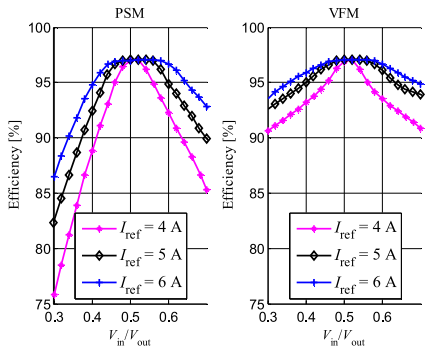

Fig. 15. Measured efficiency curves for the traditional PSM and the VFM at different input current levels (I_{ref}). Efficiencies measured at a 250-V secondary-side voltage and with a fixed 200-ns dead time. For the VFM, a fixed 3.5-A switching current (I_{zvs}) was used.

The loss distributions in various load conditions and voltage conversion ratios are given in Tables II–V. From Tables II–V, it can be seen that the VFM scheme reduces the switching losses as well as the conduction and core losses. However, the auxiliary power consumption is slightly increased due to the increased gate driving power. Despite the significant 50%–65% decrease in the switching losses shown in Tables II–V, the switching losses are higher than would be expected in the case of a complete zero-voltage switching. Thus, we may conclude that the fixed dead time length was not long enough to allow a complete discharge of the output capacitances. Better results could probably be achieved by using a longer dead time or adjusting its value dynamically. The effect of the chosen switching current value

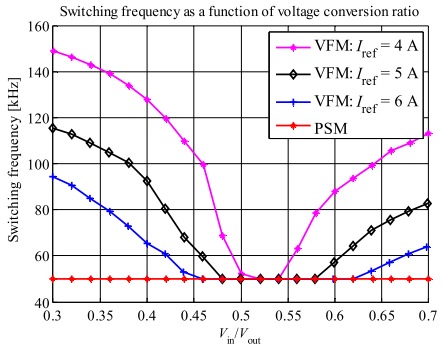

Fig. 16. Switching frequency as a function of voltage conversion ratio for various input current reference values. The switching frequency was measured from the gate transformer primary-side voltage. The effect of the phase drift and slight parameter inaccuracies lead to a slight difference in the frequencies compared with Fig. 7. The measurements were carried out with a fixed switching current of 3.5 A while the secondary voltage was kept constant at 250 V.

TABLE II
LOSS BREAKDOWN AT A VOLTAGE CONVERSION RATIO OF 0.3 AND INPUT CURRENT OF 4 A (VFM $F_{sw} = 141$ kHz, $I_{zvs} = 3.0$ A)

Loss type	Loss with PSM [W]	Loss with VFM [W]
Transformer winding	3.3	2.8
Transformer core	0.4	0.1
Input filter winding	1.3	1.4
Output filter winding	0.1	0.1
Primary conduction	2.4	1.1
Secondary conduction	0.9	0.5
Primary switching	59.4	21.2
Secondary switching	0.3	0.2
Control and gate drive	5.9	7.8

TABLE III
LOSS BREAKDOWN AT A VOLTAGE CONVERSION RATIO OF 0.7 AND INPUT CURRENT OF 4 A (VFM $F_{sw} = 126$ kHz, $I_{zvs} = 4$ A)

Loss type	Loss with PSM [W]	Loss with VFM [W]
Transformer winding	4.6	5.6
Transformer core	2.3	0.6
Input filter winding	1.3	1.4
Output filter winding	0.4	0.6
Primary conduction	2.6	2.1
Secondary conduction	1.6	1.1
Primary switching	0.5	0.1
Secondary switching	77.7	35.2
Control and gate drive	5.9	7.5

(I_{zvs}) on the efficiency is demonstrated in Fig. 17. For optimal efficiency, the switching current value (I_{zvs}) or the dead time should be adjusted dynamically for different voltage conversion ratios. However, this improvement is beyond the scope of this paper and is thus omitted.

The effect of the variable switching frequency modulation on the switching waveforms and the transformer current stress

TABLE IV
LOSS BREAKDOWN AT A VOLTAGE CONVERSION RATIO OF 0.3 AND INPUT CURRENT OF 6 A (VFM $F_{\rm sw} = 101$ kHz, $I_{\rm zvs} = 3.0$ A)

Loss type	Loss with PSM [W]	Loss with VFM [W]
Transformer winding	4.8	4.7
Transformer core	0.4	0.2
Input filter winding	2.9	3.0
Output filter winding	0.2	0.3
Primary conduction	3.0	2.4
Secondary conduction	1.4	1.2
Primary switching	42.5	15.4
Secondary switching	0.6	0.3
Control and gate drive	5.9	7.0

TABLE V
LOSS BREAKDOWN AT A VOLTAGE CONVERSION RATIO OF 0.7 AND INPUT CURRENT OF 6 A (VFM $F_{\rm sw} = 76$ kHz, $I_{\rm zvs} = 5$ A)

Loss type	Loss with PSM [W]	Loss with VFM [W]
Transformer winding	7.8	8.6
Transformer core	2.3	1.3
Input filter winding	3.1	3.1
Output filter winding	1.2	1.3
Primary conduction	4.5	4.4
Secondary conduction	2.4	2.2
Primary switching	0.9	0.8
Secondary switching	42.0	17.1
Control and gate drive	5.9	6.4

is demonstrated in Fig. 18. We can see that in addition to the efficiency improvement, the proposed modulation method can reduce voltage and current spikes and lower the peak and RMS current of the transformer.

IX. CONCLUSION AND FUTURE STUDY

In this paper, the use of half-bridge variants of the traditional DAB converter was discussed. The paper introduced a generalized power flow equation covering all the combinations of half-bridge and full-bridge variants of the traditional DAB converter. By using the generalized power equation, a VFM algorithm was derived. The proposed algorithm can be used to ensure ZVS or ZCS over the whole operating range. The effects of the phase drift phenomenon were discussed, and a simple compensation scheme was provided to reduce the effect of the phase drift. Finally, the feasibility of the proposed modulation scheme was demonstrated by a laboratory prototype.

It is emphasized that the proposed phase drift compensation is an essential part of the modulation algorithm. The use of the algorithm without the compensation may lead to a wrong switching current and to an error between the control variable and the reference. By using this algorithm in series with a PI controller, the control error, and consequently, the switching current will drift from its set point. This can lead to undesired hard-switching. It is still unverified whether the presented modulation method can be used without any phase drift compensation when using low-capacitance power switches such as wide band-gap MOSFETs.

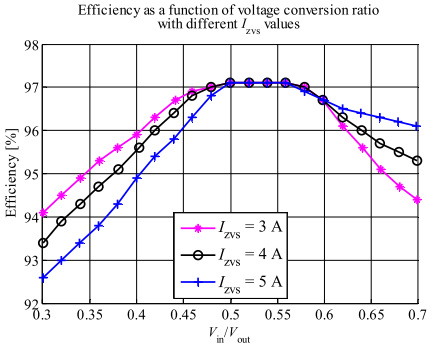

Fig. 17. Measured efficiency for different switching current values. During the measurements, the secondary voltage was kept constant at 250 V, and the primary-side current ($I_{\rm in}$) was controlled to 6 A by using a feedback control to compensate for the phase drift. The current required for a complete $C_{\rm oss}$ discharge is higher on the secondary side than on the primary side. Therefore, the larger $I_{\rm zvs}$ values improve the efficiency at higher $V_{\rm in}/V_{\rm out}$ ratios, while the primary side is already zero voltage switched with smaller $I_{\rm zvs}$ values. If the $I_{\rm zvs}$ reference is larger than the current at which the output capacitances are completely discharged, the increasing switching frequency is only causing additional losses in the converter without bringing any further benefits to the ZVS process.

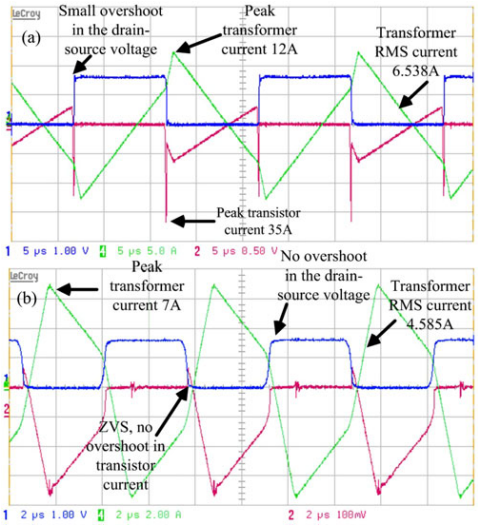

Fig. 18. Measured waveforms for the DAB prototype in the operating point where the primary-side voltage is 80 V and the secondary-side voltage is 250 V. The primary-side current is controlled to match the 4-A reference by using a feedback control to compensate for the phase drift. A fixed dead time of 200 ns is used for both the primary and secondary bridges. (a) Switching waveforms for the fixed-frequency PSM at 50 kHz. (b) Switching waveforms for the VFM at 141 kHz. The measured efficiency for the PSM is 78.5% in this operating point. Correspondingly, the efficiency for the VFM is 91.5%. The VFM also has lower current and voltage peak values and a lower transformer RMS current than the PSM.

Benefits of the proposed modulation scheme:

1) ensures zero-voltage turn-on for all the switches;
2) reduces the EMI by allowing soft-switching in the region where hard-switching would normally be present;
3) removes the excess circulating current from the low-voltage side, which tends to reduce the conduction losses;
4) can reduce the turn-off losses;
5) reduces the current spikes;
6) can reduce the core losses of magnetic components.

Disadvantages of the modulation scheme:

1) increases the switching frequency, which can lead to increased conduction losses as a result of the ac resistance;
2) increases the number of switching events, which can lead to increased losses in some converter designs;
3) increases gate driving losses.

The use of phase drift compensation for zero-sequence-based modulation schemes and the option of combining the VFM with the traditional zero-voltage-sequence-based modulation were not discussed.

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Publication IV

Väisänen V., Hiltunen J. and Juntunen, R.
Phase Drift Phenomenon in Dual Active Bridge Converter – Analysis and Compensation

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Praise Worthy Prize

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Phase Drift Phenomenon in Dual Active Bridge Converter – Analysis and Compensation

Vesa Väisänen, Jani Hiltunen, Raimo Juntunen

Abstract – *In this paper the mechanisms causing phase drift in the dual active bridge topology are presented and two compensation methods are proposed to overcome their effects. The phase drift causes discrepancy between the predicted phase shift and the actual phase shift measured from the transformer primary and secondary voltages. The error in the phase shift causes the input power to be larger or smaller than predicted and it can also interfere with the operation of several modulation methods. By using the phase drift compensation methods presented in this paper the converter input power can be predicted accurately by using the classical power equation. The effects of dead-time on the phase drift are also discussed and a method to calculate a suitable dead-time with respect to the converter operating point is proposed. The value of the phase drift compensation is presented along with a variable frequency modulation method, which enables zero voltage switching at a wide load range with a minimal circulating current.*

Keywords: *DC-DC Power Converters, Dual Active Bridge, Error Correction, Modeling, Modulation, Power MOSFET, Switched-Mode Power Supply*

Nomenclature

$C_{o(tr)}$	Time related output capacitance
C_{oss}	Transistor output capacitance
DAB	Dual Active Bridge
DSP	Digital Signal Processor
FB	Full-bridge
f_{sw}	Switching frequency
HB	Half-bridge
h_{pri}	Switching configuration parameter, primary side
h_{sec}	Switching configuration parameter, secondary side
I_D	Drain current
I_{in}	Input current
I_{peak}	Peak current
I_{sw}	Current at transistor switching instant
I_{zvs}	Minimum current required for zero voltage switching
L_{lk}	Leakage inductance
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
n	Transformer turns ratio
N_{pri}	Transformer primary turns
N_{sec}	Transformer secondary turns
P	Power
P_{ctrl}	Power given by a PI-controller controlling the transferred power
P_{ref}	Power reference
Q_{tot}	Total charge in the switching leg transistor output capacitances
SiC	Silicon Carbide
t	Time
t_{dead}	Dead-time between the switching leg transistors
t_{delay}	Voltage rise time after a switching instant
t_{drift}	Time difference between the primary and secondary switching delays
V_1	Voltage across the leakage inductor, primary side
V_2	Output voltage referred to the transformer primary
V_{DS}	Drain-source voltage
VFM	Variable Frequency Modulation
V_{in}	Input voltage
V_{out}	Output voltage
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ϕ	Phase shift as a percentage of the switching period
ϕ_{ctrl}	Phase shift from the feedback controller
ϕ_{drift}	The difference between the actual and desired phase shift as a percentage of the switching period
ϕ_{rad}	Phase shift in radians
ϕ_{sum}	Sum of the feedback controller and feedforward phase shifts

I. Introduction

Dual Active Bridge converter (DAB) is a galvanically isolated DC/DC converter topology, which has gained a lot of research interest during the last decades due to its

low passive component count, soft-switching capabilities and bidirectional characteristics [1]-[4]. The topology has also been used in fuel cell power conversion, which is also the motivating application in this paper [5], [6].

It was mentioned in [1], [7] and [8] that the ideal power equation may introduce significant calculation errors in practice due to a phenomenon called phase drift.

Because of the phase drift the actual phase shift between the transformer primary and secondary voltages is different than what is requested by the converter control. This can cause power flow also at zero phase shift where, according to (2), the transferred power should be zero. It was also mentioned in and that due to phase drift there is a certain phase shift range where power cannot be transferred and this was mentioned to be related to the dead-time between the phase leg transistors. The phase drift phenomenon will also disturb modulation methods that relay on calculations based on the assumption of an ideal converter. The ideal converter can produce exactly the desired phase shift and therefore also the desired waveforms providing that the other terms of the power equation are accurate [9], [10].

In this paper it is shown that the phase drift does not result solely from the dead-time as stated in [8], but rather from the switching delays and the charge/discharge times of the nonlinear transistor capacitances.

The effect of dead-time is relevant only if the dead-time is too short or too long with respect to the converter operating conditions and these limits will be presented in this paper. The phase drift phenomenon is emphasized when using HB-FB or FB-HB configurations, since the voltages and currents in the primary and secondary bridge transistors can be different and thus also the voltage dependent nonlinear capacitances and the switching delays can differ considerably.

Two different methods to compensate the phase drift are introduced: the first method is based on the calculation of transistor output capacitance charge/discharge times and the second one is based on a feedback controller. It is shown that by compensating the phase drift with these methods the power equation can be used to predict the power flow even with very small phase shift values.

II. Causes for Phase Drift in DAB Converter

In this section the reasons for phase drift are analyzed in both zero-voltage switched and hard switched modes.

II.1. Phase Drift When Operating in Zero-Voltage Switching Mode

Fig. 1 shows a circuit diagram for a DAB converter and Figs. 2 illustrate the idealized voltage and current waveforms for this converter. The power flow of the converter is controlled by adjusting the phase shift between the primary and secondary bridges according to the following equation [11]:

$$P = \frac{V_{in}^2}{2\pi f_{sw} L_{lk}} \frac{V_{out}}{nV_{in}} \phi_{rad} \left(1 - \frac{|\phi_{rad}|}{\pi}\right) \quad (1)$$

The parameter f_{sw} is the switching frequency. The phase shift ϕ_{rad} is expressed in radians. Eq. (1) can be derived into a more general form (2) to simplify its usage with different primary and secondary configurations:

$$P = \frac{V_1 V_2}{L_{lk} f_{sw}} \phi \left(1 - 2|\phi|\right) \quad (2)$$

The phase shift ϕ is now expressed as a percentage of the switching period ($-1 \le \phi \le 1$) and the voltages V_1 and V_2 can be expressed as follows:

$$\begin{cases} V_1 = h_{pri} V_{in} \\ V_2 = h_{sec} \dfrac{V_{out}}{n} \end{cases} \quad (3)$$

where h_{pri} and h_{sec} are 0.5 for a half bridge (HB) and 1 for a full bridge (FB) configuration. The transformer turns ratio n is N_{sec}/N_{pri}, where N_{pri} and N_{sec} are the number of primary and secondary turns, respectively. By using these notations the power equation can be used with all kinds of primary and secondary configurations, not only with FB-FB configuration.

In Figs. 2 the current I_{zvs} denotes the minimum current that is required to achieve zero-voltage switching in primary and secondary bridges. If there is no error in the phase shift ϕ and if the switches are ideal, we can accurately calculate the lengths of the time intervals t_1-t_3 and the magnitudes of currents I_{zvs} and I_{peak} based on the simplified DAB model. In the simplified model the converter is modeled as two voltage sources connected with an inductor.

However, since the transistors can have large nonlinear output capacitances which need to be charged and discharged at each switching instant, the transistor voltages and therefore the transformer primary and secondary voltages cannot change instantly.

As a result, the actual switching instant differs from the intended switching instant and the desired current (such as I_{zvs} or zero crossing) at turn-off may not be achieved.

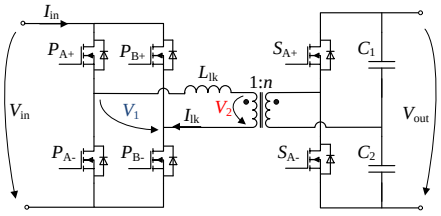
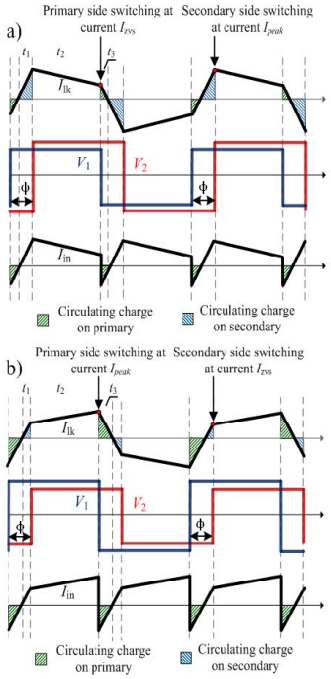


Fig. 1. A circuit diagram of a Dual Active Bridge converter using a FB-FB configuration. The primary transistors are marked with prefix *P* and the secondary transistors with prefix *S*



Figs. 2. Idealized waveforms for the DAB converter in two cases: a) $V_1<V_2$ and b) $V_1>V_2$. The power flow direction is from V_1 to V_2.

If the delays are exactly the same on the primary and secondary side, they will effectively cancel each other and there is no phase drift. However, Fig. 3 illustrates that this may not be the case in practice.

In Fig. 3 (top) the primary switching leg transistor output capacitances are charged and discharged by current I_{zvs} and the secondary transistor capacitances by current I_{peak}. Since I_{peak} is considerably larger than I_{zvs}, the transistor drain-source voltages can change much faster on the secondary side than on the primary side.

This will cause the effective phase shift to be shorter than intended. In Fig. 3 (middle) the converter is operated near a 1:1 point, where $V_1 \approx V_2$. In this case the leakage inductance current is square shaped and both the primary and secondary sides are switched with same current. Therefore, the overall phase drift is ideally zero, since the switching delays between the primary and secondary bridges are identical. The identical switching currents do not ensure identical delays in cases where there are differences between the charges in the primary and secondary transistor output capacitances.

When the input voltage is higher than the reflected output voltage, the primary side transistors are switching at I_{peak} and the secondary side transistors at I_{zvs} as illustrated in Figs. 2 and Fig. 3. The primary side is switching faster than the secondary side and the actual phase shift is now longer than intended.

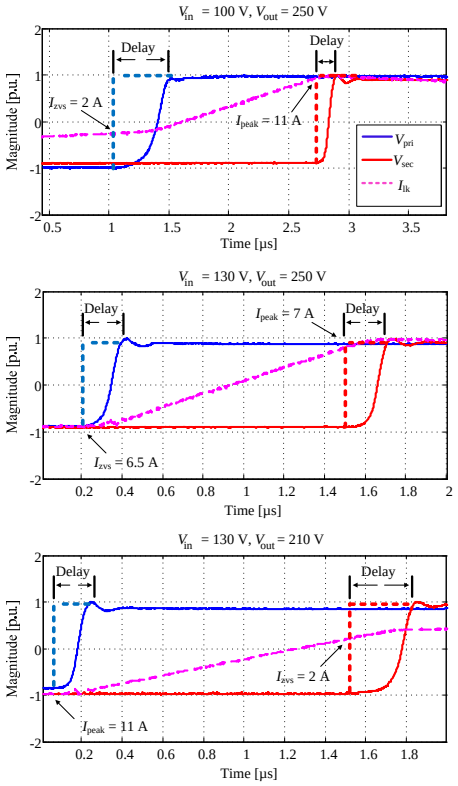


Fig. 3. Measured phase drifts for three cases: $V_1<V_2$ (top), $V_1 \approx V_2$ (middle) and $V_1>V_2$ (bottom). The input current I_{in} = 6 A in all cases. The references for primary and secondary voltages are marked with dashed lines. The converter is using a FB-HB configuration and the converter is in zero-voltage switching in all cases. When the delays are known, the phase drift can be calculated from (7)

The difference between the primary and secondary delays is not as large as in the case where $V_1<V_2$, since the primary side C_{oss} charges are larger than the secondary side charges with the voltages used in the measurement.

According to our measurements the dead-time does not have an appreciable impact to the phase drift providing that the dead-time is not too short or too long. Fig. 4 illustrates the effects of a dead-time selection in a case where V_{in} = 100 V, V_{out} = 250 V and I_{in} = 4 A.

If the dead-time is too short and the transistor is switched on during the drain-source voltage resonance period, the output capacitances are charged and discharged abruptly and this is seen as an overshoot in the drain current. The effect on the phase drift is that the transformer voltage transitions become faster and thus the delays become smaller. The drawback of a too short dead-time is degraded efficiency, since the transistors are partially hard switched.

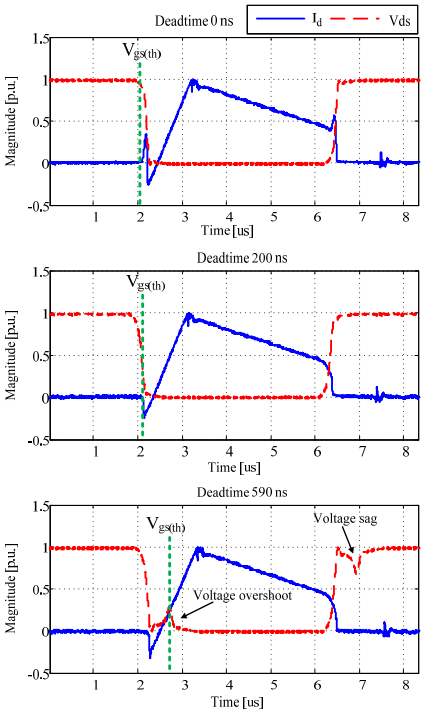


Fig. 4. Measured effects of dead-time on the voltage and current behavior of transistor P_{A-}. The instant where the gate-source voltage has risen to the conduction threshold level is marked with $V_{gs(th)}$

The optimal instant to turn on the transistor is when the transistor output capacitance is discharged and the body diode (or an external freewheeling diode) starts conducting. Since the MOSFET channel is typically a less lossy route for the current than the body diode, the conduction losses can be minimized by allowing the current to commutate to the channel as soon as possible.

If the dead-time is so long that the transistor drain current changes direction from negative to positive before the transistor channel is opened (Fig. 4, bottom) the transistor output capacitance begins to charge and the drain-source voltage increases.

If the dead-time is long enough, the transistor voltage will reach its off state value. This voltage overshoot can be seen as a voltage sag in the complementary transistor drain-source voltage in the same switching leg. The large oscillations in the drain-source voltage are likely to degrade the efficiency more than the partial hard-switching during the short dead-time operation. In Fig. 4 the efficiency was 93.4% in the 0 ns case, 93.7% in the 200 ns case and 92% in the 700 ns case.

The dead-time effects such as voltage sag and overshoot were briefly presented also in [12], but no guidelines have been given on how to select a proper dead-time with respect to the operating conditions.

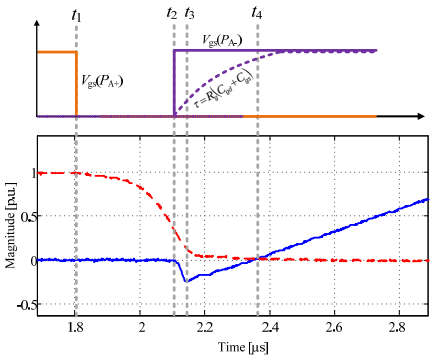


Fig. 5. Zoom of the drain-source voltage (red dashed line) and drain current (blue solid line) behavior of transistor P_{A-} with 200 ns dead-time. Since the drain voltage is not changing during t_3-t_4, there is no distinct Miller plateau in the gate-source voltage

At time instant t_1 transistor P_{A+} is turned off. The energy stored in the leakage inductance begins to charge the output capacitance of transistor P_{A+} and discharge the output capacitance of P_{A-}. The time t_1-t_3 that is required for the discharging can be approximated based on the total charge in the switching leg transistor output capacitances (the determination of this charge will be discussed later) and the leakage inductance current at instant t_1 as:

$$t_1 - t_3 \approx \frac{Q_{tot}}{I_{lk}\left(t = t_1\right)} \tag{4}$$

The current I_{lk} is not constant during t_1-t_3 or during the delay periods in Fig. 3, but is changing nonlinearly.

However, in most cases it is sufficient to calculate (4) with $I_{lk}(t = t_1)$ being I_{zvs} or I_{peak} depending on the operating mode. In cases where the stored energy in the leakage inductance is very close to the minimum energy required for zero-voltage switching, a better approximation can be obtained by using the average leakage inductance current value during time period t_3 in Figs. 2. The length of time period t_3 in Figs. 2 corresponds to the time interval t_3-t_4 in Fig. 5 and the upper limit for its length can be approximated from:

$$t_3 - t_4 \approx \frac{I_{sw} L_{lk}}{V_1 + V_2} \tag{5}$$

In order to ensure zero-voltage switching, the transistor P_{A-} gate-source voltage should not be applied before instant t_2. After the gate-source voltage has been applied, the gate-source voltage begins to rise with a time constant τ, which depends on the gate resistor and on the gate-drain and gate-source capacitances. If the gate-source voltage rises to the threshold voltage between time instants t_3-t_4, the transistor is able to conduct the positive drain current after t_4 and there will be no voltage

overshoots and voltage sags. The dead-time which causes the smallest interference to the current commutation can now be expressed as:

$$\frac{Q_{tot}\left(V_{DS}\right)}{I_{lk}\left(t=t_1\right)} < t_{dead} < \frac{I_{sw}L_{lk}}{V_1+V_2} \tag{6}$$

where I_{sw} is the current at transistor switching instant (either I_{zvs} or I_{peak}).The inequality (6) applies only to ZVS operation. In practice the leakage inductance current behaves nonlinearly during the switching process and cannot change with the rate described by (5) until the resonant process during t_1-t_3 has completed and the voltage across the leakage inductance has reached its maximum value. Therefore, a better approximation for the maximum dead-time length can be calculated as a sum of (4) and (5). If the converter operates under hard switching it is enough to ensure that the dead-time is adequately long to avoid switching leg cross-conduction and short enough to avoid zero-sequences in the transformer current.

II.2. Phase Drift When Operating in Hard Switched Mode

Fig. 6 provides support for the statement that the phase drift is smaller in hard switched mode than in zero-voltage switching mode.

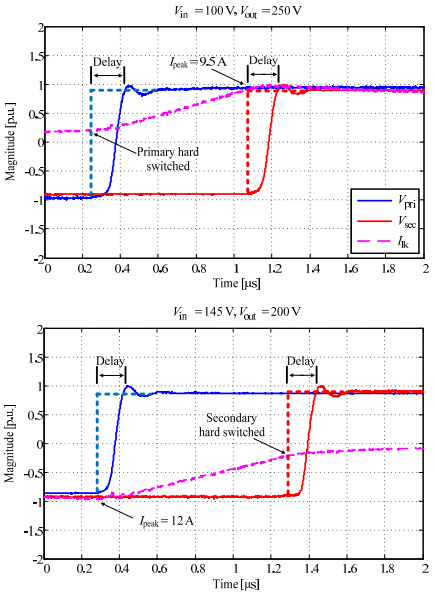


Fig. 6. Measured phase drifts for two cases: V_1<V_2 (top) and V_1>V_2 (bottom). The input current I_{in} = 4 A in all cases. The references for primary and secondary voltages are marked with dashed lines. The converter is using a FB-HB configuration and the converter is in hard-switching in both cases

If operating in case where V_1<V_2 the primary side is hard switched while the secondary side switches at peak current. In case where V_1>V_2 the primary side switches at peak current and the secondary side is hard switched. In both cases the delay differences between the primary and secondary voltages are much smaller than in the soft-switching mode (Fig. 3) and thus the phase drift is also smaller.

When operating in hard-switching the phase drift may not be an issue at all providing that we are not interested in the leakage inductance current waveform, but rather on the power to be transferred. If the converter is current (or power) controlled, the controller will adjust the phase shift so that the current (power) reference is met regardless of the phase drift.

II.3. Phase Drift Differences Between Different Input-Output Configurations

As was mentioned in the introduction, the phase drift phenomenon is emphasized when the primary and secondary sides have a different switching configuration.

Fig. 7 presents a simulated comparison with a FB-HB and FB-FB configuration, when using PSpice and STWA88N65M5 MOSFETs modelled with nonlinear capacitances.

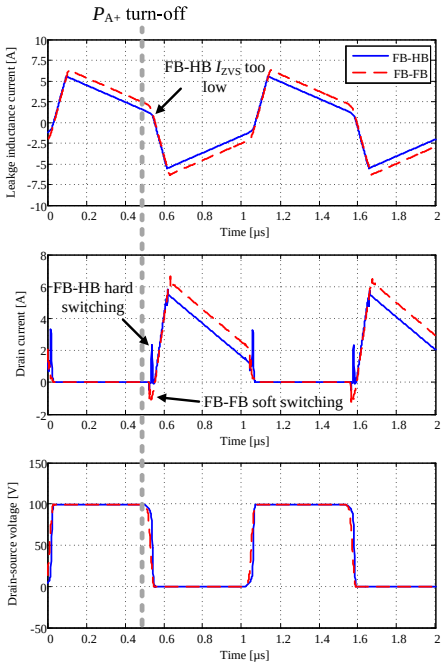


Fig. 7. An example of the phase drift difference between a FB-FB and a FB-HB converter. The turn-off of transistor P_{A+} initiates zero-voltage turn-on process for the transistor P_{A-}. The leakage inductance current should be 2.5 A at P_{A+} turn-off

The operating parameters in the simulation are: V_{in} = 100 V, V_{out} = 250 V, I_{in} = 4 A, I_{zvs} = 2.5 A. The switching frequency that should result in the desired I_{zvs} is 96154 Hz and the corresponding phase shift is 0.1. The transformer turns ratio in the FB-HB is 1:1, while it is 1:2 in the FB-FB.

In the FB-HB configuration the current that is charging and discharging the secondary side transistor output capacitances is twice as large as in the FB-FB configuration. Because of this the FB-HB secondary switches faster and there is a phase drift like in Fig. 3 (top). Due to the phase drift the current I_{zvs} is smaller than the specified 2.5 A at the turn-off instant of P_{A+} and, as a consequence, transistor P_{A-} is hard switched. In the FB-FB configuration the primary and secondary switching times are closer to each other and the phase drift is small. Therefore, the desired turn-off current for P_{A-} is close to the specified value and soft-switching conditions are met. The phase drift affects the input current as well. In the FB-HB configuration the input RMS current was 80% of the reference current, while in the FB-FB configuration it was 95%.

III. Phase Drift Compensation

In this section two different methods that can be used to compensate the phase drift effects are introduced. The phase drift compensation is important when using modulation methods such as the ones described in [9], [13] and [14] where the current values at certain time intervals need to be known.

III.1. Charge Based Compensation

In Fig. 3 it was illustrated that the phase drift depends on the differences between the primary and secondary switching leg voltage transition times. The phase drift can be calculated from:

$$t_{drift} = t_{delay,pri} - t_{delay,sec} = \frac{Q_{pri}(V_{DS})}{I_{sw,pri}} - \frac{Q_{sec}(V_{DS})}{I_{sw,sec}} \quad (7)$$

$$\phi_{drift} = t_{drift} f_{sw}$$

The phase drift can be compensated by adding ϕ_{drift} to the phase shift given by the modulation algorithm such as (2) or (8). As an example in Fig. 3 (top) the primary leg is switching at 2 A and the switching leg charge is 834 nC. The primary delay is thus 417 ns.

The secondary leg switches at 11 A and the charge is 787 nC, which results in a delay of 72 ns. The total phase drift in this case is (417-72) ns•62.4 kHz = 0.0215. If the transition times between the primary and secondary are identical, there is no phase drift. The total capacitive charge in a switching leg can be obtained for example via double pulse test [15].

The charges can also be obtained without assembling actual hardware by using a circuit simulator where the output capacitance can be modeled to be a nonlinear function of the applied voltage. Fig. 8 illustrates the charges obtained for a STWA88N65M5 MOSFET when using a PSpice model and the C_{oss} values from the datasheet. For the sake of comparison the charges are calculated also for a C2M0080120D SiC MOSFET. If a phase drift calculation is performed for the SiC transistor using the parameters of Fig. 3 (top), the total phase drift is only 0.0017, which is 92% smaller than the phase drift with the STWA88N65M5.

Besides having lower absolute C_{oss} charge values the SiC charge behavior as a function of drain-source voltage is much more linear compared to the Si transistor, which also decreases the amount of phase drift in various operating points [16].

It is not necessary to measure the charges by using only one switching leg. By measuring the delays from a complete converter setup, the additional parasitic capacitances such the transformer winding capacitances can be included in the measurement.

The compensation algorithm can be implemented on a DSP by creating a look-up table from the charge and voltage values, calculating the phase drift from (7) and adding the phase drift to the phase shift given by the modulation algorithm.

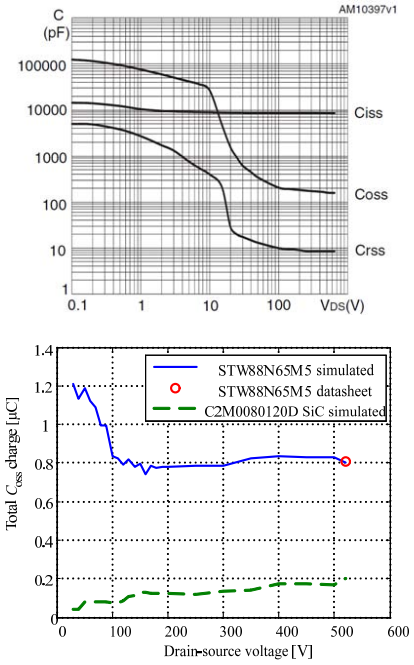


Fig. 8. STWA88N65M5 capacitances from the datasheet and the corresponding C_{oss}charges obtained from a simulation model built with nonlinear capacitances. The datasheet charge value is calculated from ($2 \cdot C_{o(tr)} \cdot V_{DS}$), where $C_{o(tr)}$ is the given equivalent time related capacitance. The total C_{oss} charge for C2M0080120D SiC transistor is provided for comparison

The charge values can also be used when calculating a suitable dead-time from (6). A suitable average charge value could also be used instead of a look-up table depending on the output capacitance nonlinearity and the maximum allowable error in the switching delay estimation.

III.2. Controller Based Compensation

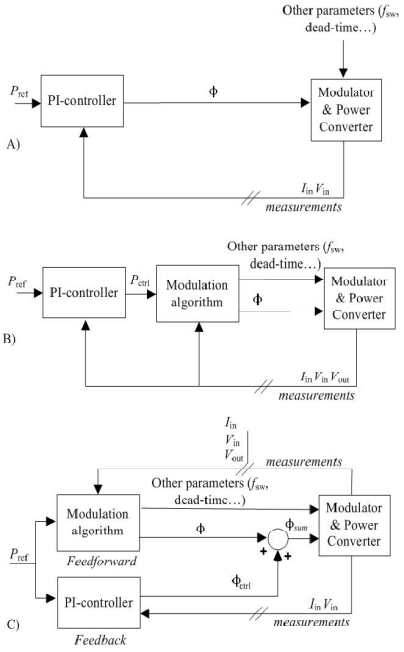
The charge based compensation method has some limitations which undermine its practical value. The number of elements in the look-up table must be quite high especially around the voltage regions where the charge changes steeply in order to avoid sudden changes in the calculated phase drift compensation.

The fluctuation of the compensation value may lead to large oscillation in the input power depending on the operating conditions. Also, since there is a possibility of measurement errors and since there are differences between the individual transistors and gate drivers, there is most likely some error in the calculated compensation value. In order to make the compensation independent on the transistor capacitances, it can be implemented as a feedback PI-controller, Fig. 9(c). The modulation algorithm block calculates the required phase shift and switching frequency based on the measured voltages and the reference current. In this case the other parameters f_{sw}, L_{lk}, n, h_{pri} and h_{sec} have fixed values. The calculated phase shift based on the given power reference P_{ref} is fed to the summation block. The feedback controller observes the actual converter input power and if there is difference between the measured power and the power reference the controller adjusts the phase shift compensation value $_{ctrl}$ so that the phase shift ϕ_{sum} results in the desired input power.

The zero difference between the reference power and the measured power means that if the other terms than ϕ in (2) are known, the phase shift between the transformer primary and secondary voltages has to be correct. Although the phase shift error will be compensated, the converter efficiency is still affecting the accuracy of the power equation. This could be compensated by using efficiency estimates according to the transferred power.

When using a basic phase shift modulation the phase shift could be controlled without the phase shift calculation block by feeding the modulator directly from the power controller, Fig. 9(a). However, in modulation methods where the current values at certain time intervals need to be known, it is important that the desired phase shift can be applied to the converter.

If all the parameters in (2) can be considered accurate, the system can be treated as an ideal system, which produces the desired voltage and current waveforms. In any case, the inclusion of the phase shift calculation block along with the phase shift controller will speed up the system step response, Fig. 9(b). The problem with approach (b) is that if there is error in the system the controller output P_{ctrl} differs from the reference P_{ref} and this causes the modulator output variables to differ from those that would be required to achieve ZVS under the operating conditions. The converter error dynamics are similar to the converter overall dynamics and therefore the stability criteria of the compensation controller can be derived similarly as would be done for the converter power controller.



Figs. 9. Various control approaches for the DAB converter. The approach (c) includes the phase drift compensation, while approaches (a) and (b) are feedback control methods that are prone to phase drift effects

IV. Experimental Results

To provide experimental verification for the results presented in this paper, a 1 kW prototype was built (Fig. 10).

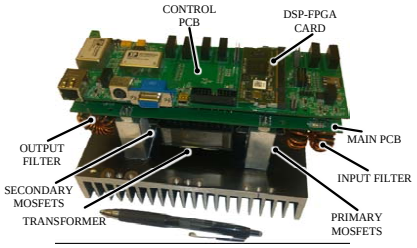


Fig. 10. Dual active bridge prototype having a full bridge primary and a half bridge secondary (FB-HB).

The component values for the converter are given in Table I. Fig. 11 presents the measured phase shifts at various input and reflected output voltage ratios, when no compensation is used.

TABLE I
COMPONENT VALUES FOR THE DAB PROTOTYPE

Symbol	Quantity	Value
Sw	Power MOSFETs	6 × STWA88N65M5
TF	Transformer	ETD54 N87
n	Turns ratio	1
n1	Primary winding	25 turns 1050 × AWG44 litz
n2	Secondary winding	25 turns 420 × AWG46 lits
L_{1k}	Leakage inductance	26.4 µH (internal)
C_{in}	Input capacitor	28 × 1µF/450V ceramic cap.
C_{dc1}	Voltage doubler capacitor	14 × 1µF/450V ceramic cap.
C_{dc2}	Voltage doubler capacitor	14 × 1µF/450V ceramic cap.
C_{b1}	DC-blocking capacitor	10 × 10µF/25V ceramic cap.
L_{a1}	Input choke	63µH, KoolMu 77930/125µ
L_{b1}	Input filter damping choke	31µH, KoolMu 77930/125µ
R_{b1}	Input filter damping resistor	2.2Ω
L_{a2}	Output choke	63µH, KoolMu 77930/125µ
L_{b2}	Output filter damping choke	31µH, KoolMu 77930/125µ
R_{b2}	Output filter damping resistor	2.2Ω

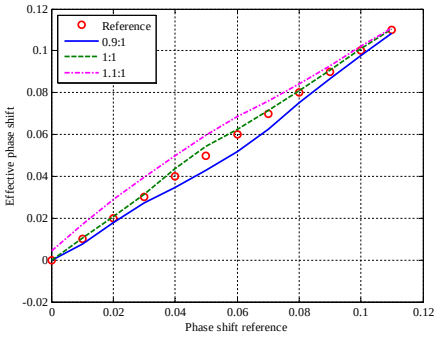


Fig. 11. Measured phase shifts with respect to the reference phase shifts at various V_{in}/nV_{out} ratios. The output voltage V_{out} is 160 V and the input voltages are 74.7 V (0.9:1), 83 V (1:1) and 91.4 V (1.1:1).

The effects described in conjunction with Fig. 3 can also been seen in Fig. 11. With the voltage ratio of 0.9:1 the primary side delays are longer than the secondary delays, which results in smaller phase shifts than intended. The reason for the large phase shift error in the range of 0.03-0.08 is the change in the converter operating mode.

Below the phase shift of 0.03 the converter is operating under hard-switching and therefore the transistor output capacitances are charged and discharged abruptly. After the 0.03 mark the converter shifts into soft-switching, but since the leakage inductance current is small the zero-voltage transition takes time and the delays are long (we are allowing the resonance process to take place by using a long enough dead-time). At larger phase shifts the leakage inductance current is larger and therefore the phase drift calculated from (7) is smaller.

When the voltage ratio is 1.1:1 the secondary delays are larger than the primary delays and therefore the phase shifts are larger than intended. In the 1:1 case the delays are nearly identical on the primary and secondary sides and therefore the measured phase shifts are close to the reference. In order to evaluate the impact of phase drift to the accuracy of the power Eq. (2), the actual phase shift and the input power are measured at various phase shift references and V_{in}/V_{out} values. The efficiency is also measured at each point in order to rule out its effect on the power prediction.

The curve "calculated" corresponds to the power values calculated from (2) using the phase shift reference and the curve "calculated with losses" is obtained from (2) using the measured phase shift and by adding the measured power losses to the result.

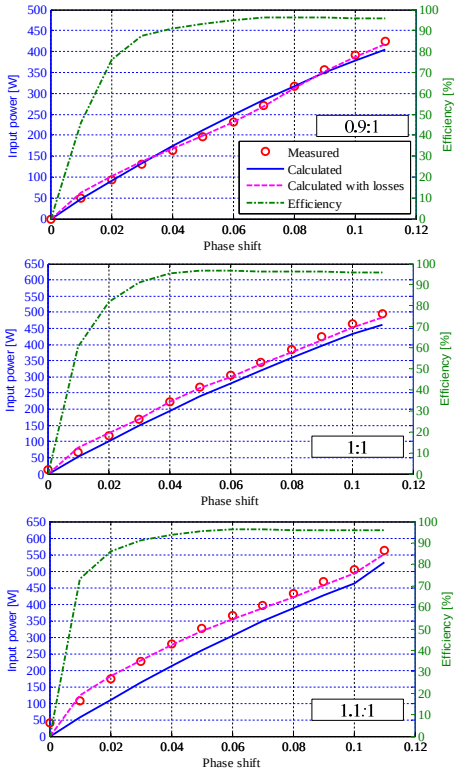


Fig. 12. Measured input powers at various phase shifts with different input voltage to reflected output voltage ratios. Please see Fig. 11 for the voltage levels

It can be seen that by removing the phase drift from the calculation and by taking the power losses in to account the calculated power correlates well with the measured power. There should not be large discrepancies between the predicted power and the measured power like there was in [7], if the converter is operating under the conditions listed below:

- The primary and secondary transistors should be able to produce similar switching times in order to minimize the phase drift. The factors affecting the switching times are the transistor output capacitance (the lower the better), the voltage difference between primary and secondary sides (the output capacitance is voltage dependent) and the switching currents.
- The efficiency should be as high as possible to minimize the effect of power losses.
- The dead-time should be long enough to avoid hard-switching and short enough to avoid the voltage overshoot and voltage sag phenomena (Fig. 4).
- The converter has proper input and output filtering so that we measure the active current instead of the circulating reactive current [17], [18].

The value of the drift compensation is best demonstrated by investigating the leakage inductance current waveforms. If we know that the measured phase drift is equal to the phase shift given by the power equation, we also know the lengths of the time intervals t_1, t_2 and t_3 and the values of I_{zvs} and I_{peak} in Figs. 2. The compensation was used along with a variable frequency modulation method (VFM), which can be derived from the idealized DAB model as follows [19]:

$$\begin{cases} \phi = \dfrac{1}{4\gamma}\left(\gamma - I_{ref}\alpha + sign\left(I_{ref}\right)\sqrt{\alpha^2 {I_{ref}}^2 - 2I_{ref}\gamma\beta + \gamma^2}\right) \\ f_{sw} = \dfrac{h_{pri}V_2}{I_{ref}L_{lk}}\phi\left(1-2|\phi|\right) \end{cases} \quad (8)$$

where:

$$\alpha = \begin{cases} 1 & |V_1 < V_2 \\ \dfrac{V_1}{V_2} & |V_1 > V_2 \end{cases} \quad (9)$$

$$\beta = \begin{cases} \dfrac{V_1}{V_2} & |V_1 < V_2 \\ 1 & |V_1 > V_2 \end{cases} \quad (10)$$

and:

$$\gamma = sign\left(I_{ref}\right)I_{zvs}h_{pri} \quad (11)$$

In (8) I_{ref} is the reference current for the controller. The VFM modulation method is explained in more detail in [19].

The purpose of the modulation method is to produce the desired switching current I_{zvs} by varying the switching frequency and phase shift accordingly. In order to ensure that the algorithm produces the desired I_{zvs} and zero-voltage switching, the actual phase shift measured from the transformer primary and secondary voltages must match the phase shift given by the algorithm.

The algorithm can also be used to obtain zero current switching by setting $I_{zvs} = 0$.

Again, the phase drift compensation is needed to enable switching at zero current. Fig. 13 illustrates the operation of the VFM algorithm with and without the phase drift compensation. The converter operating point is V_{in} = 125 V, V_{out} = 300 V, I_{in} = 4 A and I_{zvs} = 2.5 A.

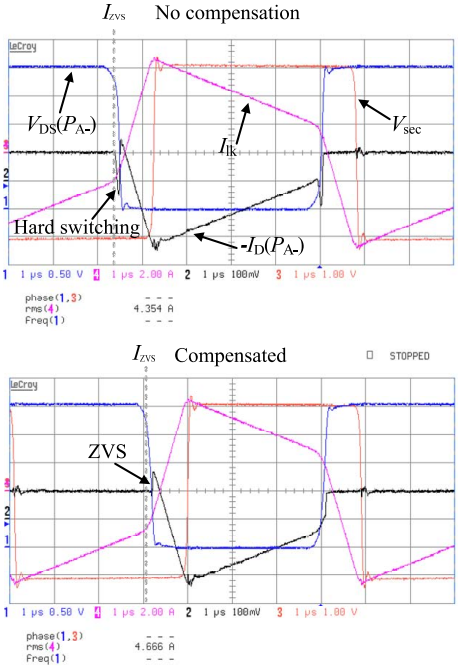


Fig. 13. Measured waveforms of $V_{DS(PA-)}$, inverted $I_{D(PA-)}$, I_{lk} and V_{sec} with the compensation controller disabled (top) and enabled (bottom). Without the phase drift compensation the value of I_{zvs} is approximately 2 A instead of the desired 2.5 A, which causes the transistor P_{A-} to go into hard-switching. The transistor current was measured with a PEM CWT Ultra mini with an output of 50 mV/A

Although the difference in I_{zvs} in Fig. 13 was only 0.5 A, it was enough to make a difference between ZVS (efficiency 93.44%) and partial hard-switching (efficiency 93.09%). The importance of the drift compensation increases together with the amount of phase drift.

V. Conclusion

In this paper it was shown that the phase drift phenomenon results from the different switching delays between the primary and secondary bridges. When using transistors with small output capacitances (such as wide band-gap MOSFETs) and if the differences between the primary and secondary switching currents are small, the phase drift can be negligible. The phase drift is of importance if such modulation methods are used, where the leakage inductance current at a certain time instant

needs to be known. This paper presents two phase drift compensation methods that can be used to correct the discrepancies between the phase shift given by the power equation and the actual phase shift measured from the transistor primary and secondary voltages. The method based on output capacitance charge calculation can also be used for selecting a suitable dead-time under zero voltage switched conditions. To compensate for the possible errors in determining the switching leg charges, a feedback controller based compensation method was proposed. This method is more accurate in the phase drift compensation, although the power losses and voltage drops still slightly reduce the accuracy of the VFM algorithm. The converter voltage drops can be taken into account by calculating them based on the known circuit resistances and currents or by using measurements.

Acknowledgements

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Publication V

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Maximum efficiency point tracking algorithm for dual active bridge converters

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Maximum Efficiency Point Tracking Algorithm for Dual Active Bridge Converters

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Abstract— **This paper presents an algorithm for seeking the most suitable operating point and the maximum efficiency in respect of the operating conditions in a dual active bridge converter. The method is the most suitable for half-bridge variants of the dual active bridge since the previously presented modulation methods are derived only for full-bridge configurations. The maximum efficiency point tracking method is based on a perturb-and-observe type tracker and a variable frequency modulation method where the turn-on currents of the primary and secondary bridges can be adjusted by using closed-form expressions.**

Keywords—algorithms, bridge circuits, DC-DC power converters, energy efficiency, modulation

I. INTRODUCTION

The Dual Active Bridge converter (DAB) is a galvanically isolated DC/DC converter topology, which has gained a great deal of research interest during the past decades due to its low passive component count, soft-switching capabilities and bidirectional characteristics [1]-[5]. The topology has also been used in fuel cell power conversion, which is also the motivating application in this paper [6], [7].

The simplest way to control the power flow of the DAB converter is to adjust the phase shift between the primary and secondary bridges. This modulation method is often referred to as conventional phase shift modulation [8], rectangular modulation [9] or single phase shift control [5]. The converter can operate under zero voltage switching (ZVS) if the magnitude of the resonant inductor current at the switching instant is large enough to charge and discharge the output capacitors of the bridge transistors. The drawback of the rectangular modulation is that the zero voltage switching is limited only to a narrow operating range where the V_{in}/V_{out} ratio is close to the nominal voltage conversion ratio [9].

In fuel cell applications, the stack output voltage changes as a function of the current and in the long run the stack degradation can decrease the available voltage even with a constant current [10]. To enable soft switching at a wider load range or at voltage conversion ratios much different from the nominal ratio, various modifications to the rectangular modulation have been proposed.

A triangular modulation method allows zero current switching (ZCS) at the low voltage side and zero voltage switching at the high voltage side and is typically employed at light loads [11]-[13]. Triangular modulation has an upper power limit after which it is preferable to switch to other modulation methods to improve the efficiency. A modulation method often referred to as trapezoidal modulation allows smaller transformer RMS currents compared to triangular modulation at and beyond the power level where the transition between triangular and trapezoidal modulation is feasible [11], [14]. The terminology used for describing the possible variations in the resonant inductor current waveform include also extended-phase-shift control [14], dual-phase-shift control [15], [16] and triple-phase-shift control [17]-[19].

The modulation methods used for extending the DAB soft-switching range have been limited to full-bridge configurations because both ends of the transformer primary or secondary windings need to be simultaneously connected either to the positive or the negative rail in order to generate the zero-voltage sequences. This is achieved by adjusting the phase shift between the switching legs of an H-bridge. The modulation of the half-bridge variants of the DAB has not been discussed due to the limited number of degrees of freedom in shaping the resonant inductor current. To provide a simple and effective way for extending the soft switching range in both full-bridge and half-bridge variants of the DAB, a closed form modulation method based on a variable switching frequency modulation (VFM) was presented in [20].

The contribution of this paper is to provide an algorithm for the online efficiency maximization of the converter when using variable switching frequency modulation. The efficiency is maximized by varying the currents in which the primary and secondary bridges are switching. The method can produce both zero-voltage switching and zero-current switching depending on which approach is more suitable for the operating conditions. Unlike many previously proposed modulation schemes, the proposed method does not require a large amount of data stored offline since the computational effort is low and can be performed online. The method is best suited for DAB configurations having a half-bridge on both sides, but it can also be used to improve the conversion efficiency with all kinds on primary and secondary configurations.

The research leading to these results has received funding from the European Union's Seventh Framework Programme (FP7/2007-2013) for the Fuel Cells and Hydrogen Joint Technology Initiative under grant agreement n° 621213.

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II. Dual Active Bridge and Soft Switching

Fig. 1 illustrates a dual active bridge converter having a full-bridge primary and a half-bridge secondary.

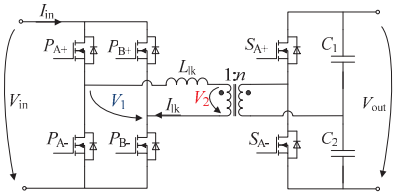

Fig. 1. Schematic of a dual active bridge converter having a full-bridge on the primary side and half-bridge on the secondary side.

The classical power equation presented in [2] can be derived into a more general form to simplify its usage with different primary and secondary configurations [20].

$$P = \frac{V_1 V_2}{L_{lk} f_{sw}} \phi\left(1 - 2\left|\phi\right|\right). \tag{1}$$

The phase shift ϕ is now expressed as a percentage of the switching period ($-1 \le \phi \le 1$), and the voltages V_1 and V_2 can be expressed as

$$\begin{cases} V_1 = h_{pri} V_{in} \\ V_2 = h_{sec} \dfrac{V_{out}}{n} \end{cases}, \tag{2}$$

where h_{pri} and h_{sec} are 0.5 for a half-bridge (HB) and 1 for a full-bridge (FB) configuration. The converter switching frequency is denoted with f_{sw}. The transformer turns ratio n is N_{sec}/N_{pri}, where N_{pri} and N_{sec} are the number of primary and secondary turns, respectively. By using these notations, the power equation can be used with all primary and secondary configurations, not only with a FB-FB configuration.

The VFM modulation is explained in detail in [20], but the basic idea is to change the converter phase shift and switching frequency to produce a desired switching current I_{zvs} either on the primary or the secondary side. If one side is switching at current I_{zvs}, the other side is switching at current I_{peak}, as shown in Fig. 2.

Fig. 2a and Fig. 2b present the typical resonant inductor waveforms that are achieved by using the triangular and trapezoidal modulation methods in a DAB converter using a FB-FB configuration. The illustration is not comprehensive, as the two full-bridge circuits can generate 12 different voltage patterns [8]. However, the given voltage waveforms serve as a comparison for the waveforms produced by VFM. As shown in Fig. 2, the VFM modulation method can produce similar current waveforms as triangular modulation when the parameter I_{zvs} is set to 0 (in practice not exactly zero to avoid calculation anomalies). There is no zero sequence in the current produced by VFM, but the comparison is justified since in triangular modulation the zero sequence length diminishes along with increasing power [8].

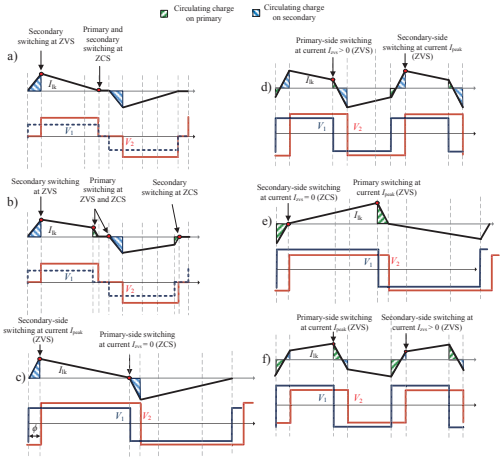

Fig. 2. Current I_{lk} when using triangular modulation and when $V_1 < V_2$. b) Current I_{lk} when using trapezoidal modulation and when $V_1 < V_2$. c) Current I_{lk} when using VFM, setting $I_{zvs} = 0$ and when $V_1 < V_2$. d) Current I_{lk} when using VFM, setting $I_{zvs} > 0$ and when $V_1 < V_2$. e) Current I_{lk} when using VFM, setting $I_{zvs} = 0$ and when $V_1 > V_2$. f) Current I_{lk} when using VFM, setting $I_{zvs} > 0$ and when $V_1 > V_2$.

III. Maximum Efficiency Point Tracking

A. Algorithm Implementation

The maximum efficiency point tracking algorithm (MEPT) is based on the perturb-and-observe method, which is well-known from solar applications [21]. However, instead of calculating the converter power and adjusting the converter voltage reference to maximize the power, we are calculating the efficiency and adjusting the parameter I_{zvs}. The starting point for I_{zvs} can be negative, zero (ZCS) or some arbitrary value greater than zero, which enables the possibility for ZVS depending on the charges in transistor output capacitances (time related C_{oss}) [20].

The MEPT function is called with the filtered efficiency value and the desired I_{zvs} step. The efficiency values are summed until the desired number of cycles is reached, after which the efficiency values are averaged. If the efficiency increases compared to the previous value, the next I_{zvs} perturbation is made in the same direction as the previous perturbation. If the efficiency decreases, the next perturbation is made in the opposite direction than the previous perturbation. Finally, the function checks the I_{zvs} against the defined minimum and maximum limits and returns the value of I_{zvs}.

B. Software and Control Structure

Fig. 3 presents the converter control structure, which is based on a state machine clocked with a constant frequency of 100 kHz. The MEPT algorithm updates its output value only after a defined number of cycles in order to make the I_{zvs}

perturbation period longer than the settling time of the efficiency measurement [22]. The input current controller is based on the control scheme presented in [20] and the controller is discretized based on the current switching frequency in each cycle to maintain stability and the desired response.

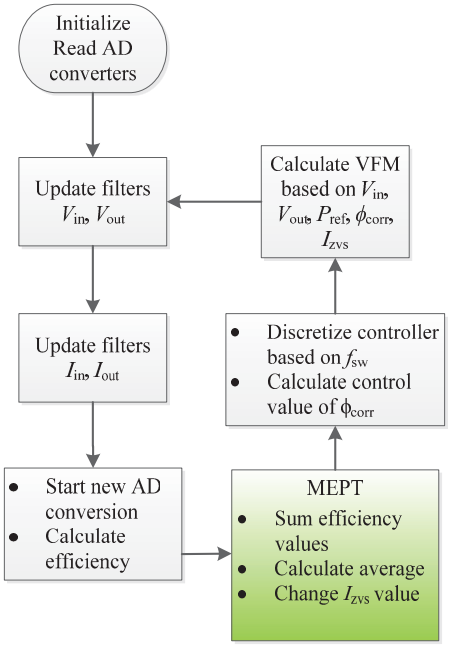

Fig. 3. Structure of the converter control software. The loop is a state machine driven by a synchronization flag, which changes its value at a constant time cycle of 10 µs. The microcontroller is running with a clock of 168 MHz. The gate drive signals are formed from VFM output by a FPGA modulator running at 200 MHz.

C. Possible Problems With Maximum Efficiency Point Tracking

The maximum efficiency point tracking algorithm may fail to find the global efficiency optimum if the converter current and voltage measurements introduce an error which changes as a function of the I_{zvs} and therefore of the switching frequency. In this case, the measured efficiency might not correlate with the actual efficiency and the converter controller may see one global efficiency maximum or more in operating points which in reality do not produce the maximum efficiency. Under these conditions, it may be impossible to find the real maximum efficiency with any tracking algorithm.

When using perturbation steps too small with a noisy efficiency measurement, the algorithm may become stuck in a local maximum. This could be resolved for example by making a larger perturbation at certain time intervals allowing a larger change in the converter efficiency. To make a feasible initialization for the I_{zvs} starting point and the tracking direction, certain assumptions can be used. The optimal efficiency point will likely be found among the following operating points:

- point where the converter is at the edge of zero voltage switching ($C_{oss(tr)}$ charge based approach [23]);
- point where the transformer and transistor RMS currents are minimized;
- point where the I_{zvs} is set close to zero (zero current switching).

The maximum efficiency point can also be found by making a sweep with different I_{zvs} values and observing the resulting efficiencies. The sweep can be made at constant intervals or when the ratio of V_1 and V_2 or the value of the input current exceeds the defined hysteresis levels. However, this method can also fail if there are false maxima in the measured efficiency curve.

IV. Experimental Results

A. Prototype Description

The MEPT is tested with a 1 kW DAB prototype having a full-bridge on the primary side and a half-bridge on the secondary side (Fig. 4). The control algorithms of the converter are implemented on a STM32F417 32-bit ARM microcontroller. The other component values are listed in Table I. The internal current measurements are conducted using ACS714 series current measurement ICs and the voltages are measured using ACPL-C87 sensors. The external reference measurements are conducted with LabVIEW controlled Keysight 34461A multimeters.

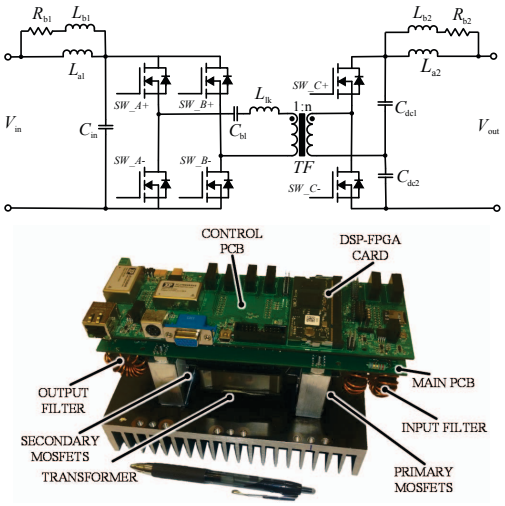

Fig. 4. DAB prototype for testing the MEPT algorithm.

TABLE I
COMPONENT VALUES FOR THE DAB PROTOTYPE

Symbol	Quantity	Value
SW	Power MOSFETs	6 x STWA88N65M5
TF	Transformer	ETD54 N87
n	Turns ratio	1
n1	Primary winding	25 turns 1050 x AWG44 litz
n2	Secondary winding	25 turns 420 x AWG46 litz
L_{lk}	Leakage inductance	26.4 µH (internal)
C_{in}	Input capacitor	28 x 1µF/450V ceramic cap.
C_{dc1}	Voltage doubler capacitor	14 x 1µF/450V ceramic cap.
C_{dc2}	Voltage doubler capacitor	14 x 1µF/450V ceramic cap.
C_{bl}	DC-blocking capacitor	10 x 10µF/25V ceramic cap.
L_{a1}	Input choke	63µH, KoolMu 77930/125µ
L_{b1}	Input filter damping choke	31µH, KoolMu 77930/125µ
R_{b1}	Input filter damping resistor	2.2Ω
L_{a2}	Output choke	63µH, KoolMu 77930/125µ
L_{b2}	Output filter damping choke	31µH, KoolMu 77930/125µ
R_{b2}	Output filter damping resistor	2.2Ω

B. Maximum Efficiency Point Tracking and Efficiency

The measured impact of MEPT on the converter efficiency and a picture of the prototype are given in Fig. 5. The perturbation step ΔI_{zvs} was 0.1 A.

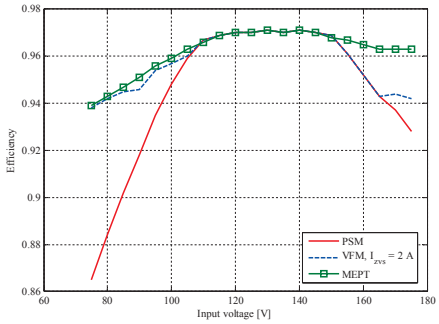

Fig. 5. Efficiency comparison between conventional phase shift modulation (PSM), variable frequency modulation with a fixed I_{zvs} and maximum efficiency point tracking. The output voltage V_{out} is fixed at 250 V and the input current I_{in} is controlled to be 6 A. The preselected value of I_{zvs} in VFM is rather close to optimum with lower input voltages (operating mode as in Fig. 2e), but as the input voltage increases beyond 140 V the selected I_{zvs} begins to denote the secondary high voltage side switching current (Fig. 2f). Due to higher C_{oss} energies in the secondary transistors, the given I_{zvs} of 2 A is too small for soft switching. The MEPT algorithm seeks the best efficiency for the operating conditions by changing the value of I_{zvs} dynamically, thus mitigating the effect of non-linearities in the transistor capacitances.

The values of I_{zvs} given by the MEPT algorithm for obtaining the efficiencies of Fig. 5 are presented in Fig. 6. In the shaded area, the switching currents are not affected by the MEPT since the V_1/V_2 ratio is close to the ideal value of 1, where the leakage inductance current waveform is a square wave and $I_{zvs} = I_{peak}$. On the left side of the shaded area, the operating mode is as in Fig. 2e, and on the right side, it is as in Fig. 2f. The maximum efficiencies are obtained with I_{zvs} values that are close to the minimum current required for complete C_{oss} discharge in the switching legs.

Although the preferred operating mode in this case was ZVS, this might not be the case when the conduction losses are dominating over the switching losses. It might be preferable to switch the transistors around zero current or discharge the output capacitances only partially to avoid excess increase in the switching frequency and thus the AC resistances in the converter. The novelty of the presented method is that the best operating point is searched automatically without prior knowledge of the actual circuit parasitics.

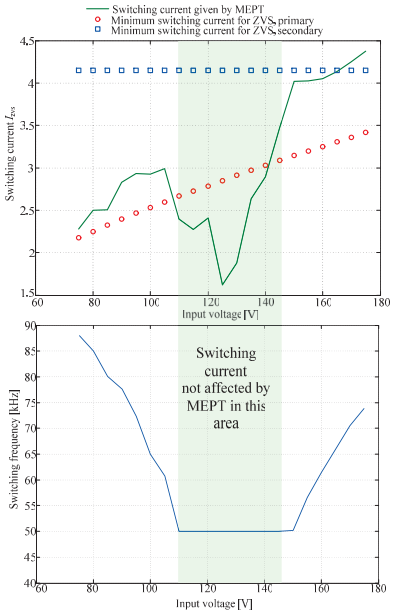

Fig. 6. The switching currents given by MEPT and the calculated minimum switching currents for discharging the output capacitances of the STW88N65M5 transistors when the input voltage V_{in} is changing and the output voltage V_{out} is fixed at 250 V. The switching frequency increases in the non-shaded area to keep the I_{zvs} at the desired level.

C. Converter Loss Distributions and Efficiency Behavior

Fig. 7 illustrates the impact of a varying I_{zvs} on the converter efficiency. The overall converter losses and the individual loss contributions are plotted as a function of I_{zvs} in the case of Fig. 5 and an input voltage of 75 V. The other losses exclude only conduction losses (caused by filters, transistors and transformers). It is seen that there is a global loss minimum at the point where the converter is fully soft switched. When the I_{zvs} is increased beyond this point, the frequency dependent losses are increasing along with the increased switching frequency.

The I_{zvs} values below zero indicate that the switching current is negative on either the primary or secondary side in Fig. 2 and there is no circulating charge available to charge and discharge the transistor output capacitances. The larger the negative switching current is, the higher the switching losses are caused by current and voltage overlap.

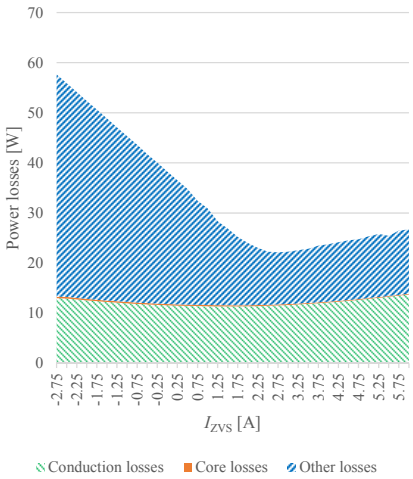

Fig. 7. Measured loss distributions when V_{in} = 75 V, V_{out} = 250 V and I_{in} = 6 A.

The switching frequency with I_{zvs} = -2.7 A was 50 kHz and the corresponding primary referred AC resistance of the transformer was 93 mΩ. With I_{zvs} = -2.7 A, the values were 99 kHz and 114 mΩ, respectively. The reason why the conduction losses are not increasing along with the increasing switching frequency and AC resistances is illustrated in Fig. 8. The VFM algorithm produces a minimum transformer and transistor RMS current at a certain value of I_{zvs}, which depends on the operating conditions and the converter parameters.

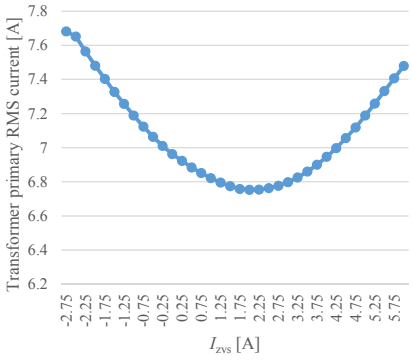

Fig. 8. Variation of transformer primary RMS current as a function of I_{zvs} in the operation conditions of Fig. 7.

Another example of the loss distributions is given in Fig. 9. In this case, $V_1 > V_2$ and it is beneficial to ensure soft switching on the high voltage secondary side. The minimum switching losses and the lowest overall losses occur at higher I_{zvs} currents because the energy required for ZVS is higher.

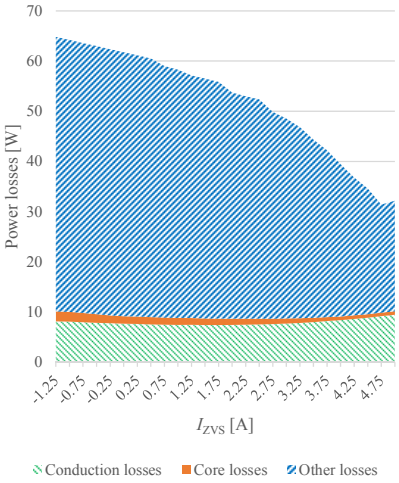

Fig. 9. Measured loss distributions when V_{in} = 160 V, V_{out} = 250 V and I_{in} = 4 A.

The switching frequency with I_{zvs} = -1.25 A was 50 kHz and the corresponding primary referred AC resistance was 93 mΩ. With I_{zvs} = 4.75 A, the values were 131 kHz and 135 mΩ, respectively.

D. Conduction Loss Comparison With Previously Presented Methods

The methods for minimizing the conduction losses over a wide operating range in a low voltage, high current application were discussed in [8] and [24]. The method presented in this paper and in [20] can produce even smaller RMS currents and also smaller overall losses if the operating conditions allow the I_{zvs} variations without excess increase in the switching frequency and AC resistances. Fig. 10 presents a comparison of the RMS currents achievable with MEPT (or VFM) and the modulation methods presented in [8] and [24].

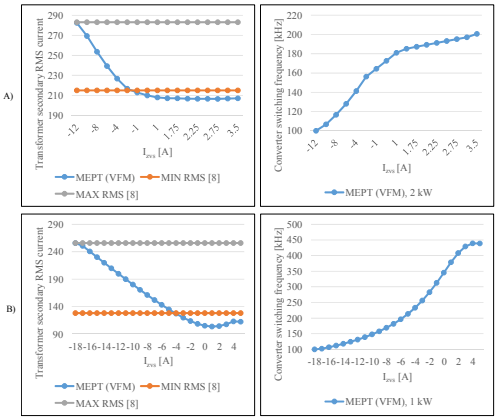

Fig. 10. Transformer secondary RMS currents and corresponding VFM switching frequencies when V_1 = 450 V, V_2 = 11 V, L_{lk} = 26.7 µH and N_{sec}/N_{pri} = 1/19. The output power is a) 2 kW and b) 1 kW. The minimum values of I_{zvs} produce identical results with the conventional phase shift modulation, which results in the maximum RMS currents.

In order to evaluate the impact of reduced RMS currents and increased switching frequencies on the overall losses when using VFM, the DAB prototype described in [8] and [24] is modeled in PSpice and simulated in the cases of Fig. 10. The frequency dependent losses are included by using nonlinear MOSFET models, a hysteretic transformer core model and frequency dependent winding resistances. The efficiency improvements between the conventional phase shift modulation (PSM) and VFM are illustrated in Fig. 11.

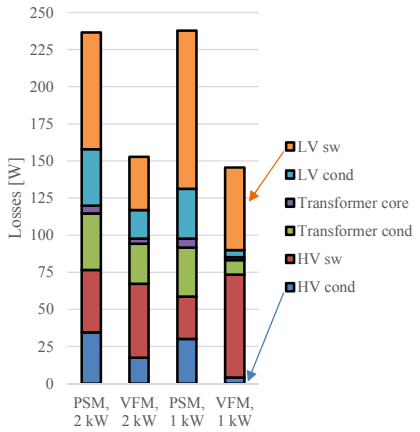

Fig. 11. Simulated power losses when using PSM and VFM modulation in a HV-LV application. The VFM cases are simulated with I_{zvs} = 1 mA. Gate drive losses are not included in the switching losses.

The VFM and therefore also the MEPT algorithm are best suited for cases where the switching frequency remains within reasonable limits compared to the nominal minimum switching frequency as the I_{zvs} value is varied. In the simulated 1 kW example, the HV side switching losses (mainly turn-off losses) increased significantly due to the high switching frequency, but the large reduction in RMS currents and conduction losses compensated for this despite the increased AC resistances. The primary referred transformer AC resistance was 153 mΩ at 100 kHz and 336 mΩ at 345 kHz. The LV side switching losses were reduced in both 1 kW and 2 kW cases since the switching current was close to zero instead of a large negative value.

V. Conclusion

This paper presents a maximum efficiency point tracking algorithm which can find the most suitable operating point for a Dual Active Bridge converter within the constraints of the underlying variable frequency modulation. The maximum efficiency point can be found by varying the minimum current value at which the primary or secondary bridge is switched. It is shown that both the conduction and switching losses can be reduced significantly by selecting a suitable switching current, and the purpose of the maximum efficiency point tracking algorithm is to automatize this process without prior knowledge of the circuit parasitics and operating conditions.

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