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CONTROL DESIGN ISSUES IN GRID-CONNECTED SINGLE-PHASE CONVERTERS, WITH THE FOCUS ON POWER FACTOR CORRECTION

ACTA UNIVERSITATIS LAPPEENRANTAENSIS 920

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Dissertation for the degree of Doctor of Science (Technology) to be presented with due permission for public examination and criticism in the Auditorium of the Student Union House at Lappeenranta–Lahti University of Technology LUT, Lappeenranta, Finland, on the 25th of September, 2020, at noon.

Acta Universitatis
Lappeenrantaensis 920

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ISBN 978-952-335-547-7
ISBN 978-952-335-548-4 (PDF)
ISSN-L 1456-4491
ISSN 1456-4491

Lappeenranta–Lahti University of Technology LUT
LUT University Press 2020

Abstract

Jari Honkanen
Control design issues in grid-connected single -phase converters, with the focus on power factor correction
Lappeenranta 2020
92 pages
Acta Universitatis Lappeenrantaensis 920
Dissertation, Lappeenranta–Lahti University of Technology LUT
ISBN 978-952-335-547-7, ISBN 978-952-335-548-4 (PDF)
ISSN-L 1456-4491, ISSN 1456-4491

Electrical equipment is most commonly powered from a mains connection. The mains alternating voltage is rectified, isolated, and regulated in a power supply. The power supply acts as an interface between the mains voltage and the powered equipment. In addition to protecting the equipment from the mains voltage, the power supply isolates the mains connection from the distortions of the powered equipment. The protection against distortion is accomplished by controlling the voltages inside the power supply and the shape of the current drawn from the mains.

In many cases, the simplest control loop design will suffice, but a more elaborate control loop design is usually needed to meet all the design requirements. The current loop performance of the digitally controlled power factor correction is improved with a simple feedforward term. The idea for the proposed solution stems from the Lyapunov control theory.

The voltage loop performance of the power factor correction is improved by using a fuzzy nonlinear controller. The controller is simple to implement, as the underlying solution is to schedule the gains of two different PI controllers with the error between the measurement and the reference. Application of the presented controller simplifies the control design as the control designs for the steady-state and transient performance are decoupled, allowing the control to yield a fast transient with a low distortion, which are typically mutually exclusive. With a linear control, the dynamics of the DC link is a choice between a low distortion and a fast transient performance.

Further, this doctoral dissertation discusses the benefit of a digital control

platform with the option to optimize the feedback measurement. The idea of proper timing of the current measurement, thereby minimizing the effects of anti-alias filtering, is investigated in the case of current measurement in a grid-forming inverter. The benefit of the proper timing of the measurement and filter design is a reduction in noise by $-20\,\mathrm{dB}$ in the current measurement with a minimal phase delay.

All of the results obtained in the study were verified by extensive experimental measurements to validate the achieved performance and show that the algorithms and methods provide benefits in an actual setting.

Keywords: digital control, power electronics, power factor correction

Acknowledgments

I want to express my gratitude to Mr. Samuli Räisänen as the head of the Powernet project as well as his role to introducing me to the world of power electronics and the fantastic people in it. I also want to thank my former colleagues Mikael Tötterman and Pasi Lauronen and rest of the wonderful people of Efore Oyj. I truly enjoyed my brief time in Espoo working with some of the best engineers in the field of power electronics.

I want to thank the reviewers Professor Teuvo Suntio and Professor Mikko Routimo. Your efforts have greatly improved this dissertation.

Special thanks to Professor Pertti Silventoinen. It was a pleasure to work under you guidance.

I want to thank my supervisor and good friend Dr Juhamatti Korhonen for your endless support with the research, writing and your boundless patience. Special thanks also belong to the original project group Dr Juha Ström and Dr Janne Hannonen. There could not have been a better research group than you two. Some of the best times I have ever had were spent working with the rest of the original gang of 6405, Dr Juho Tyster, Dr Arto Sankala, Dr Mikko Qvintus, Dr Tommi Kärkkäinen and mr Saku Levikari.

I want to thank all my current colleagues and friends. You all have made work something to look forward to. I wish to especially thank Jussi Karttunen for the many interesting conversations. And of course for your part in getting me into the many ways extra special place that is Danfoss Editron. I also tip my hat to the new class of 6405, it is a pleasure to see that the people and locations may change but the spirit remains the same. As spoken by Zarathustra "I say unto you: one must still have chaos in oneself to be able to give birth to a dancing star."

I will always be grateful to Dr. Hanna Niemelä for her efforts to improve the language of this dissertation.

I want to express my deepest gratitude to the best parents anyone could hope for, Aila and Keijo and my sister Emppu. More overly protective parents would have thought of a mains connected tube amplifier to be too dangerous and difficult first project for a child with no prior knowledge of anything

related to electronics.

Finally I want to thank my family Aino and Essi. You two are my bringers of joy and mscd.x

Jari Honkanen
September, 2020
Lappeenranta, Finland

Two things I know that are true:
1. Nothing in this world has ever been done as well as it could have been
and
2. Nothing in this world needs to be done \textfb{that} well done!

Yours, Jari

Contents

List of Symbols and Abbreviations

Latin alphabet

$d(t)$	controlled duty ratio
$e(t)$	control error
i_1	switch 1 current measurement
$\mathrm{K_1}$	set of control gains for the first membership function
$\mathrm{K_i}$	integrator gain
$\mathrm{K_p}$	proportional gain
L	inductance
$S(s)$	sensitivity function of a closed-loop system
$T(s)$	tracking function of a closed-loop system
u	voltage
$V(t)$	Lyapunov function

Greek alphabet

$\Delta(t)$	Additive disturbance signal
ω	angular frequency
$\omega(t)$	integrator state in a controlled system
φ	voltage phase
ϕ	current phase

Subscripts

f_{AA}	anti-aliasing cutoff frequency
f_{ctrl}	control frequency

f_{out} output frequency

f_{s} current sampling frequency

f_{sw} switching frequency

I_n n:th current harmonic

V_{RMS} root-mean squared voltage

M_1 first membership function

m_1 lower limit for the membership function

m_2 upper limit for the membership function

P_{average} Average power

ref reference

T mains cycle period

t_{ADC} AD conversion time

t_{DT} dead time

u_{AC} output voltage

u_{ref} reference voltage

V_n n:th voltage harmonic

I_{RMS} root-mean squared current

Abbreviations

AA anti-aliasing (filter)

AC alternating current

ADC analog-to-digital converter

CCM continuous current mode

DC direct current

DCM discontinuous current mode

DPF displacement power factor

DSP digital signal processor

EMI electromagnetic interference

FPGA field programmable gate array

GaN gallium nitride

IGBT insulated gate bipolar transistor

MHz megahertz

MOSFET metal oxide field effect transistor

PF power factor

PF_D distortion power factor

PFC power factor correction

SiC silicon carbide

THD total harmonic distortion

T-S Takagi–Sugeno

ZOH zero-order hold

List of publications

The results of the study are documented in a scientific journal and peer-reviewed conference publications. This doctoral dissertation consists of the following publications.

Publication I

Honkanen, J., Hannonen, J., Silventoinen, P., and Räisänen, S. (2015), "Single phase PFC control with Lyapunov method," in *17th European Conference on Power Electronics and Applications EPE'15 ECCE-Europe*, Geneva, Switzerland, pp. 1–5.

Publication II

Honkanen, J., Hannonen, J., Korhonen, J., Nevaranta, N., and Silventoinen, P. (2018), "Nonlinear PI-control approach for improving the DC link voltage control performance of a power factor corrected system," *IEEE Transactions on Industrial Electronics*, Vol. 66, Iss. 7, July 2019, pp. 5456–5465.

Publication III

Korhonen, J., Honkanen, J., Rautio, J., and Silventoinen, P. (2019), "Effect of Current Measurement Timing and Antialiasing Filter in a Single-Phase Inverter," in *Proceedings of IEEE Applied Power Electronics Conference and Exposition*, Anaheim, CA, USA, pp. 938–943.

Publication IV

Hannonen, J., Ström, J. P., Honkanen, J., S. Silventoinen, P., Räisänen, S. and Pokkinen, O. (2013), "Design of digitally controlled isolating 1-phase AC/DC converter by using centralized processing unit," in *15th European Conference on Power Electronics and Applications (EPE)*, Lille, France, pp. 1–10.

Author's contribution

In Publication I, Mr. Honkanen was the principal author of the paper and the main contributor to its scientific content. Mr. Honkanen developed the algorithm, constructed the experimental setup for the measurements, and executed the empirical experiments and simulations. The software for the experimental device was written mostly by Dr. Hannonen. Dr. Korhonen and Dr. Nevaranta helped with writing and commented on the paper.

In Publication II, Mr. Honkanen was the principal author of the paper and the main contributor to its scientific content. Dr. Hannonen took part in conducting the experiments with the author. Mr. Räisänen and Prof. Silventoinen provided comments on the paper.

In Publication III, Mr. Honkanen was responsible for the design and construction of the experimental device. These tasks covered dimensioning of the magnetic components, winding of the transformers and the inductors, design of the PCBs for the inverter and the FPGA platform, design of the embedded system, and development of the embedded hardware and software. Mr. Honkanen was also responsible for the design of the measurements and the sampling algorithm.

In Publication IV, Mr. Honkanen was the coauthor responsible for the design of the control and the signal processing used for conditioning of the measurements. Mr. Honkanen was also responsible for all of the modeling work and took part in the debugging of the experimental device. The schematic of the experimental device was designed by Dr. Hannonen, who together with Dr. Ström was also responsible for the software design of the embedded platform. All of the authors were responsible for the design of the experimental setup and measurements.

1 Introduction

Power electronics is a field of engineering that focuses on the control and conversion of electrical energy. The control of power supplies is implemented with semiconductors that are switched on and off at a rate from thousands to millions of times per second to produce high-frequency voltage pulses to control the energy flow. The use of high switching frequencies allows compact conversion systems still reaching efficiencies of 98–99% (Badstuebner et al., 2010; Rothmund et al., 2019; Radimov et al., 2020).

Most electronic devices are powered from the mains. In a typical power supply, the AC mains voltage is first rectified before further processing by switch mode converters is possible. This applies to all kinds of systems, such as battery chargers (Yilmaz and Krein, 2013), communication towers (Badstuebner et al., 2010), and computers (Singh et al., 2016), all of which run on DC power processed by switch-mode power supplies. The main problem with power supplies is the electromagnetic interference (EMI) that they cause and the nonlinear loading that they present to the mains (Mainali and Oruganti, 2010).

Nonlinear loads disrupt and interfere with the mains voltage, and thus, also with other equipment that shares the same mains connection (Mainali and Oruganti, 2010). The disruption is the result of nonlinear loads drawing non-sinusoidal current from the mains. The distorted, harmonic-rich currents interact with the impedance of the mains connection, introducing harmonics to the mains voltage waveform and thus distorting the mains voltage (Faiz et al., 2015). The harmonic currents also cause extra heating in the distribution transformer windings and cores, thereby increasing the losses in the distribution network (Faiz et al., 2015). Compared with a pure sine shape, the distorted current also increases the peak current drawn from the mains connection for a given power level.

1.1 Power factor

In an effort to limit the ill effects of nonlinear loads in the mains-connected equipment, standards have been established for the quality of power drawn from the mains (IEC61000-3-2, 2009). The standard limits the allowed harmonic currents to acceptable levels, and most mains-powered devices have to adhere to these limits. In order to properly interface a nonlinear power electronic load to the mains, the quality of the current drawn from the mains has to be corrected. This quality of the mains current is called the power factor.

Power factor is defined as

$$\mathrm{PF} = \frac{P_{\mathrm{average}}}{I_{\mathrm{RMS}} \cdot V_{\mathrm{RMS}}}. \tag{1.1}$$

The mean value of the product of voltage and current over an interval of one mains cycle T is obtained by the ratio of average power P_{average} to RMS power

$$P_{\mathrm{average}} = \frac{1}{T}\int_0^T v(t)i(t)dt. \tag{1.2}$$

As the mains voltages and currents are periodic, the waveforms can be decomposed into the mains frequency fundamental signal and its integer multiples using a Fourier series

$$v(t) = V_0 + \sum_{n=1}^{\infty} V_n cos\left(n\omega t - \varphi_n\right) \tag{1.3}$$

$$i(t) = I_0 + \sum_{n=1}^{\infty} I_n cos\left(n\omega t - \phi_n\right), \tag{1.4}$$

where φ and ϕ are the phases of specific harmonic components of voltage and current waveforms. The average power can be obtained by substituting (1.3) and (1.4) into (1.2)

$$P_{\text{average}} = \frac{1}{T}\int_0^T \left(V_0 + \sum_{n=1}^{\infty} V_n \cos(n\omega t - \varphi_n)\right)\left(I_0 + \sum_{n=1}^{\infty} I_n \cos(n\omega t - \phi_n)\right) dt. \tag{1.5}$$

As mentioned in (Erickson and Maksimovic, 2001), calculating the integral (1.5) yields

$$P_{\text{average}} = V_0 I_0 + \sum_{n=1}^{\infty} \frac{V_n I_n}{2} \cos(\varphi_n - \phi_n). \tag{1.6}$$

On the other hand, taking the root mean square value of (1.3) and (1.4) yields

$$V_{\text{RMS}} = \sqrt{V_0^2 + \sum_{n=1}^{\infty} \frac{V_n^2}{2}} \tag{1.7}$$

$$I_{\text{RMS}} = \sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}. \tag{1.8}$$

As noted in (Erickson and Maksimovic, 2001), the significance of the phase present in (1.6) is that only the harmonic components that have a correct phase relationship add to the average power delivered to the load. This is in contrast to RMS values (1.7) and (1.8), as all the harmonics increase the RMS value regardless of the phase.

A power factor of 1 thus requires that the RMS and average values of the current and voltage signals are equal. This is achieved when the current and voltage waveforms have the same harmonic content with a matching phase relationship (Erickson and Maksimovic, 2001). In the case that the mains voltage is not carrying harmonics, a high power factor requires that the mains current is free from both reactive currents and current harmonics.

When nonlinear loads are used, a high power factor can be achieved by filtering the mains current with either passive filters, by using capacitive and

inductive components, or actively with power electronics. The main issue with passive harmonic filtering is that the filters are expensive and large because of the low-frequency mains harmonics that need to be filtered (Singh et al., 2003). When power electronics are used to filter the harmonics, only the high switching frequencies have to be filtered passively (Rossetto et al., 2000). This allows the use of small electromagnetic interference (EMI) filter components designed to filter out the high switching frequencies (Liu et al., 2013) in the range of tens to hundreds of kiloherz. The EMI filter has capacitance that draws reactive current; however, as the EMI filter components are dimensioned to be effective for the kHz to MHz range, they have a limited effect on the 50–60 Hz mains frequencies. Thus, in a power electronics system, the harmonic currents typically have the most adverse effect on the system and are of the highest concern (Levron et al., 2014).

In a mains-powered device, such as a charger or a computer power supply, the harmonic currents are controlled with a dedicated power electronics circuit called the power factor correction, or in short, PFC.

1.2 Power electronics circuits for an AC interface

An active power factor correction can be accomplished with various power electronics circuits. A commonly used circuit is a boost converter, but also Cúk, flyback, and single-ended primary-inductor (SEPIC) converters are used to provide the PFC function (Fardoun et al., 2012), (Bist and Singh, 2015), (Jovanovic and Jang, 2005). With wide band gap devices, a totem-pole converter can also be effectively used for the PFC. It is, however, not practical with silicon devices because of the hard switching losses in a half bridge (Huang and Huang, 2017).

In single-phase systems, power factor correction is most commonly achieved with a boost converter. The choice of the boost converter is obvious as it has a low component count, it is simple to control, and the switch is easy to drive (Brown, 2001).

1.2.1 Boost PFC

The boost converter is depicted in Figure 1.1. The mains voltage is rectified by using a diode rectifier, and the full-wave-rectified voltage is then interfaced to the DC link voltage with a boost converter. The boost converter is controlled to produce the current that tracks the mains voltage waveform. This operation minimizes the effect of the nonlinear current on the mains voltage (Orabi and Ninomiya, 2003).

Typical variations of the boost PFC configurations are single and parallel boost converters and a bridgeless boost converter. Bridgeless and parallel boost converters, in particular, are used for higher power levels because of the distribution of the losses between several devices (Singh et al., 2003).

Bridge configurations with four switches are used when the direction of the power has to be reversed, for example in active filters and uninterruptible power supplies (Erickson and Maksimovic, 2001). In these kinds of applications, the PFC is also referred to as an active front end.

1.2.2 Single-phase inverter

The main components of the inverter are shown in Figure 1.2. The four transistors are used to provide a pulse-width-modulated voltage, which is then filtered with an appropriate passive filter. If the inverter is connected to the grid, it can draw or supply the grid with sinusoidal current, thereby acting as a PFC to the current being fed or drawn from the grid.

In grid-forming operation, the inverter is required to support any load that is typically powered from mains voltage, and it should thus provide steady sine voltage under linear and nonlinear load voltages at the u_{DC} node. There are standards that define the dynamical performance requirements for single-phase inverters used to supply AC voltage as well as limits for allowed electromagnetic emissions (IEC-62040-3, 2014).

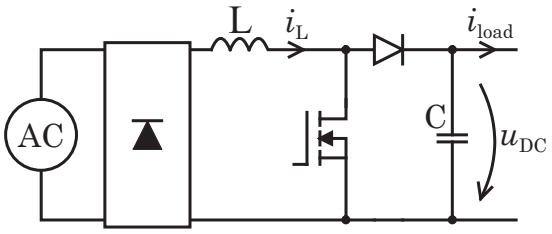


Figure 1.1. Single switch boost converter; the most common power factor correction topology in single-phase systems.

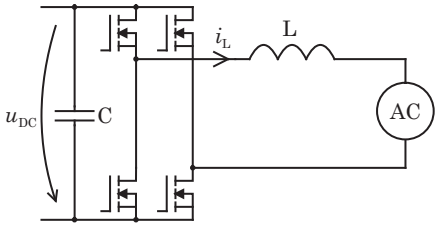


Figure 1.2. Single-phase inverter.

1.2.3 Power-factor-corrected power supply

As most devices are required to have a PFC, a basic power supply has three main parts: an EMI filter, a rectifier, and a DC/DC converter. An example of a power-factor-corrected power supply is shown in Figure 1.3. The load is fed from the rectified voltage by a DC/DC converter, which provides voltage level conversion and galvanic isolation, and the PFC stage ensures a proper mains connection without excessive interference to the grid. Therefore, the PFC acts as an interface between the DC/DC stage and the mains voltage by eliminating the adverse effects of the nonlinearities and the resulting harmonics from the mains. As described for example in (Wu, 2006), the boost in the PFC cannot have an appropriate power factor without changing the switch duty cycle. For this reason, the mains current has to be actively controlled with a feedback.

1.2.4 PFC control

The PFC control has two main objectives: It controls the input current waveform and the level of the rectified DC voltage. Because the DC link voltage

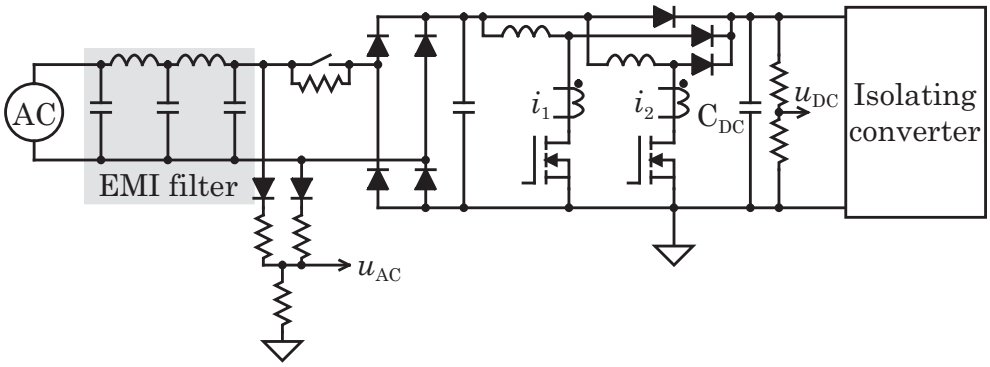


Figure 1.3. Structure of the parallel boost PFC. The main components are the EMI filter, two identical boost converters in parallel, and an isolating converter that translates the DC link voltage into the required voltage level. The figure also shows the placements of the measurements used for the feedback control. The switch currents i_1 and i_2 are measured with current transformers, u_{AC} is the rectified grid voltage measurement, and u_{DC} is the DC link voltage measurement.

level, which is the output of the PFC, is regulated, the power supplies that draw power from it work at relatively constant input voltages. This enables a higher efficiency as the controlled DC link voltage ensures more consistent operating conditions for the rest of the power circuits. Because the boost PFC provides a regulated DC link, it can be designed to work with different mains voltages and frequencies (Jang and Jovanovic, 2009), with possibly a derated power level.

As the PFC controls the level of the rectified DC voltage along with the input current waveform, an appropriate PFC control has to provide fast regulation of the DC link voltage. The performance of the DC link regulation is usually evaluated by the time it takes for the DC link to stabilize from a load step. A PFC should ensure a minimal voltage sag when the load is stepped up with a fast return to the nominal voltage level.

As the THD is a measure of the quality of current drawn from the mains, the THD is also a measure of the performance of a PFC. The THD of the drawn mains current in a power supply with a PFC is affected both by the input current control (Louganski and Lai, 2007) and the voltage control, thereby making the design of a PFC control a trade-off between the mains current quality and the DC link voltage regulation (Sebastian et al., 2010).

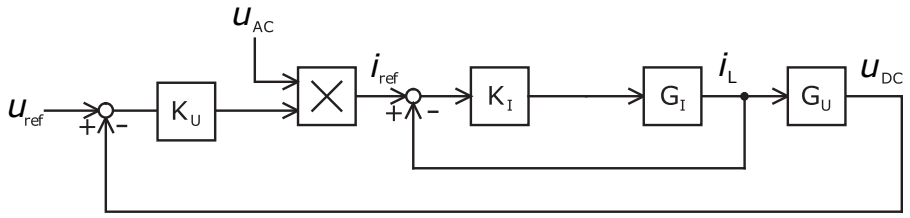


Figure 1.4. Basic cascade control structure of the PFC (Erickson and Maksimovic, 2001).

The basic control structure of the PFC is shown in Figure 1.4. The PFC controller has two main control loops; an outer voltage loop and an inner current loop (Erickson and Maksimovic, 2001). The voltage loop regulates the DC link voltage to set the reference value by setting the reference current level. The current loop then controls the current to match the current reference level set by the voltage control.

When the PFC is operating normally in the continuous current mode, the switch conduction time is varied across the mains cycle in order to force the current waveform to follow the mains voltage waveform. The most common control method is to use a PI control with current measurement for the feedback (Xie et al., 2004). Several analog and digital control integrated circuits (ICs) are available for this purpose, covering most single-phase applications. The PI controller works as long as the gain can be set high enough to ensure enough attenuation to the input voltage dynamics of the PFC, and in most cases, the current control provides sufficiently low harmonics with a high gain control only. Problems arise, however, when the gain of the feedback loop is insufficient to counter the effects of the mains voltage. Common problems caused by the mains voltage interaction are crossover distortion and a phase shift between the mains voltage and the input current (Hui Qu and Ruan, 2006). In cases where the gain cannot be sufficiently increased to provide appropriate PFC operation, feedforward and nonlinear control methods are used (Louganski and Lai, 2007).

Despite the current control, the PFC has several sources for an increase in the THD. Significant zero cross distortion arises from the oscillatory current loop response, limitations on the duty ratio, and the amount of capacitance on the DC link side of the input diode bridge (Sun, 2004). The PFC is also operating in the discontinuous current mode (DCM) when the current is less than half of

the ripple amplitude, which typically happens when the converter is operating at a less than 10–20% load (Lim and Khambadkone, 2011).

1.2.5 DCM operation of the PFC

The DCM operation occurs if the average inductor current is less than the amplitude of the switching ripple during a switching cycle. In this case, for a portion of the switching cycle there is no energy stored in the inductor and the current is clamped to zero. This results in distortions caused by a change in the control dynamics (Lim and Khambadkone, 2011), oscillations of the measured current (De Gusseme et al., 2007), and the phase lead of the current with respect to the line voltage (Sun, 2004). Numerous studies have been conducted to address distortion in the DCM operation. When a digital controller is used, the waveform can be corrected when the system goes into the DCM by calculating the average current from the sample, and a feedforward can be used to further improve the current waveform (De Gusseme et al., 2005). (Kim et al., 2017) propose a modulated carrier control to improve the current shape when the system goes into the DCM, allowing an improved power factor in low-power operation.

Even with a proper mains current shape, the DCM operation has a very limited power range owing to the high peak currents involved. A PFC is typically designed to operate in the DCM only for low power ranges of a few hundred watts. As the industrial power supply under consideration is operated with a 20–100% load corresponding to 600 W to 3 kW for most of the time, the low-power mode where the DCM operation takes place is not considered in the control design presented in this doctoral dissertation.

1.2.6 Current measurement

The quality of measurements is paramount to a high-performance control. In this doctoral dissertation, the timing of the measurement delay and the achievable reduction in the noise level with a proper timing of the feedback measurement signals are studied. The quality of the measurement directly affects the performance of the control design.

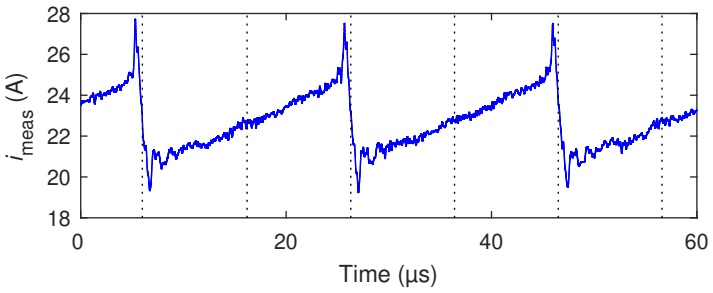


Figure 1.5. Current ripple measured from the output of the LTSR-15NP current transducer output. The dashed lines illustrate the sample instants at the middle of the ripple waveform.

A well-known method for primary inductor current sampling is to time the sample at the middle of the switched current ripple waveform (Persson, 2001). A properly timed measurement offers a minimized delay, immunity against switching noise, and direct measurement of the average current value from the switched current waveform. The problem with this method is that the accuracy of the measurement is tied to the accurate timing of the sampling instant. When fast current slopes are sampled, even small errors in the timing will significantly impair the measurement. The problem is illustrated with a measured current shown in Figure 1.5, which depicts the current waveform at the peak of full load current.

The current ripple is typically designed to be 10–20% of the maximum peak load current (Brown, 2001). The current ripple is a compromise between the size of the inductor and the ripple amplitude with the given switching frequency and DC link voltage. The presence of the current ripple means that small deviations from the middle of the current waveform will significantly impair the measurement accuracy. For example, the highest applied pulse width produces a voltage pulse of 500 ns, during which the full 5 A ripple occurs. Thus, even a deviation of 100 ns from the center of the voltage pulse will produce an error of an ampere. In the experimental inverter, the gate driver has a 60 ns delay and the switch delays are 35 ns, both of which vary depending on temperature. Switching delays can thus significantly degrade the accuracy of the average current measurement as the ripple can be higher in amplitude than the average of the current when the load current is less than nominal.

The problem with the accuracy required for the timing is further exacerbated by the fact that different switches have widely varying delays that depend on the switched current, temperature, DC link voltage, and gate driver (Brown et al., 2012). Therefore, the delay is not constant in different operating environments. Lastly, the sample and hold amplifier of the AD converter has a finite acquisition time. For example, the 12 bit AD converter MAX11115 used in this study has an acquisition time of 52 ns (Maxim Integrated, 2013), which represents 10% of the minimum pulse duration.

One option for counteracting the effect of high current slopes is to sample only a part of the current waveform with a lower slew rate (Van de Sype et al., 2004). However, this method sacrifices the improvement in the control performance achieved by the dual sampling of the current. The switched current measurement could also be filtered, but because of the large current ripple, significant filtering will add a high phase shift to the measurement, which again limits the attainable control performance (Ma et al., 2018).

All of the problems related to sample timing are the more pronounced, the more the switching frequencies are increased. With the adoption of wide band gap devices, the designer has a strong motive for increasing the switching frequencies as the output filter components are likely the heaviest and costliest part of the inverter (Gurpinar and Castellazzi, 2016; She et al., 2017) and with higher switching frequencies, the passive filter components can be sized smaller (Roy et al., 2018; Ghosh et al., 2018).

In **Publication III**, the problem with synchronous sampling is solved by using an AA filter with a bandwidth higher than the switching frequency, and the sample is timed to the low-pass-filtered version of the current.

1.3 Digital hardware in power electronics

In most industrial power supplies, digital hardware is required for communications, sending out the system state and alerts, and receiving commands from higher-level controls (Tötterman and Grigore, 2012). It is possible to increase the system integration by incorporating the low-level power electronics feedback control into the same digital hardware. This also provides an opportunity to use control signals and measurements for condition mon-

itoring (Hannonen et al., 2016b), hardware-level aging detection (Hannonen et al., 2014), and component value detection (Hannonen et al., 2016a). The options available for the digital control of power electronics include the use of a microcontroller, a microcontroller along with a programmable logic, and fully customized hardware (Bielewicz et al., 1996).

A dedicated controller with sufficient peripherals for the digital power control application can also be used. This means that for a centralized power supply control, the controller is chosen so that it has sufficient hardware resources, such as pulse width modulation, and AD channels available. Although this method may be the most cost-effective one, it is also the most susceptible to single sourcing problems and the least portable among the different digital control hardware.

A common method to apply customized hardware is to use a processor for the signal processing and control functions and an FPGA for the peripheral drivers. This allows complex timing functions to be precisely executed with the FPGA hardware and general software to be used for the application. The processor can then be chosen based on the processing needs, and the required IO functionalities can be built on the FPGA. Depending on the amount of custom hardware used, this method allows hardware abstraction, and the application software can thus be written at a more general level, making the software more portable between different processors.

The benefit of custom hardware is the absence of any extra processing headroom associated with context switches, branching code execution, or instruction and pipeline delays typically present with microprocessors. With custom hardware, all of the components built inside the logic fabric run in parallel and have a minimal effect on other parts of the system. The significance of this is that the speed of the control loop is not limited by the overhead caused by other functions that would use processor time. The downside of custom hardware is the cost of development compared with software.

In **Publication IV**, the digital control platform and the benefits of custom hardware and a dedicated microcontroller are discussed. An example design with an FPGA and a microcontroller is presented, and it is used to control an AC/DC single-phase power supply.

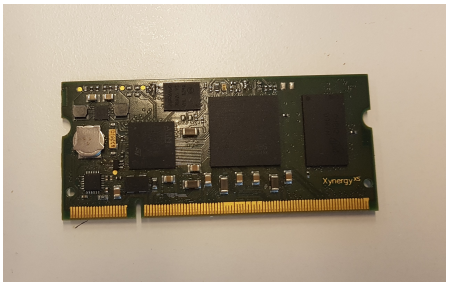


Figure 1.6. XynergyXS board used to control the AC/DC power supply.

1.3.1 Digital control platforms used in the study

In **Publications I**, **II** and **IV**, the experimental device is a 3 kW AC/DC power supply, which is controlled by using a microcontroller for the signal processing and an FPGA for the timing of the sampling for measurements and modulation.

The power-factor-controlled power supply has a control platform that has a Cortex-M4f407 floating point microcontroller and a Xilinx Spartan 6 FPGA shown in Figure 1.6. The combination of an FPGA and a microcontroller has the benefits of easy software implementation of the control and flexibility for the peripherals that the FPGA allows.

The AC/DC power supply has a centralized digital control platform, which controls the PFC and the isolating DC/DC converter, placed on the isolated secondary side of the DC/DC converter. This is done as the PFC and DC/DC converter currents are measured using current transformers, which intrinsically provide the required galvanic isolation. Thus, the required signal crossings across the isolation barrier are limited to the AC voltage and DC link voltage measurements, neither of which requires a high bandwidth. The low bandwidth requirement for the PFC voltage measurements greatly simplifies the measurements as they can be sampled with a lower frequency, and median filtering and averaging can then be used to minimize the noise present in the measurements.

The inverter used in **Publication III** is controlled with a custom hardware implemented in an FPGA. The digital control platforms are shown in Figure 1.7. The developed FPGA control hardware platform includes analog multiplex-

Figure 1.7. Cyclone 10 LP FPGA card used for the inverter control. The designed control card includes two 2 MHz sampling analog-to-digital converters and analog multiplexers for a total of 14 AD channels in a 2x7 configuration.

ers and analog-to-digital (AD) converters. In order to minimize the latency of the calculation, the inverter control is implemented directly in the FPGA logic and written by using a hardware description language. The main benefit of the control design with custom hardware is the control calculation latency. For example, the PFC control of the AC/DC power supply takes up to 16% of the clock cycles of the interrupt routine, which is about 3 µs with the 50 kHz control frequency and the 168 MHz DSP clock. Conversely, the total latency between a completed AD sample and a PWM register update in the FPGA controlled inverter is less than 100 ns, even though the complexities of the control algorithms are about the same.

1.4 Scope and motivation of the work

The research of this doctoral dissertation started in collaboration with Powernet Oy. The study aimed at making use of the benefits of a centralized digital control platform in an off-line industrial power supply. The objective of the study was to develop the health monitoring and aging detection of a power supply by utilizing the benefits of digital control design. The health monitoring algorithms were developed together with the control design as both used the same measurements and partially shared the required signal processing. A PFC converter is part of most mains-connected systems, and therefore, significant improvements in the PFC performance are beneficial to most systems.

The motivation for improving the performance of the power factor correction

(PFC) and measurements came from the need to improve the performance of an AC/DC power supply. With standard cascaded PI control loops, neither the current nor the voltage loop performs satisfactorily. There are multiple reasons why the performance was not sufficient without special control methods. In the case of the current control, the digital control of the individual boost circuits of the parallel boost converter was not deemed to be reasonable. The power supply was controlled with a 50 kHz control frequency and with both boost converters having the same duty cycle command. This limited the attainable gain of the current loop, and therefore, the control loop control had to be designed with a line voltage feedforward. The Lyapunov method was used as the resulting control is directly derived from the structure and dynamics of the power supply.

The performance limitation of the voltage control is a fundamental property of a single-phase PFC. Because the input current is sinusoidal, the resulting sinusoidal ripple in the DC link is unavoidable. The performance of the DC link voltage during a load step cannot be achieved with a linear controller without sacrificing the input current THD.

In order to achieve satisfactory dynamics for the single-phase inverter, a high control bandwidth is required, which is obtainable with dual sampling of the measurements. The dual sampling is used to get average current and voltage measurements from the switched current waveform. Without the slew rate limitation obtainable by the anti-alias (AA) filtering, switching noise cannot be avoided. Furthermore, the narrowest switched pulse is only 500 ns, and with all of the uncertainties present in the generated voltage pulses, sampling at the middle point of the voltage pulse is not consistent enough to be practical. The inverter sampling was implemented by dual sampling of the filtered current. The filter was designed to have a cutoff frequency that is higher than the modulation frequency, and the sampling instant was then timed to provide over 20 dB of improvement of the measurement noise.

1.4.1 Digital control platform

In **Publication IV**, the choice between an off-the-shelf microcontroller, a half customizable embedded system with a microcontroller and an FPGA, and a fully customizable embedded system implemented in the FPGA is discussed

in the context of a digital control platform. The publication addresses the use of a centralized digital control platform for the control of the PFC and the DC/DC converter. The digital platform is also used for condition monitoring purposes, which is the topic of several publications and the doctoral dissertation of Dr. Janne Hannonen.

1.4.2 Improvements in the current control

A common way to improve the linear current loop performance is to include feedforward terms in the control. For example, an input voltage feedforward has been used either directly (Xie et al., 2004) or by modeling the admittance and then using the inverse of the admittance model to filter the mains voltage in order to produce the feedforward (Louganski and Lai, 2007).

A nonlinear control can be designed either with a sliding mode control or with Lyapunov-based methods in both the continuous and discrete time domains. The nonlinear control law has been designed by using Sontag's optimal control with a continuous (Pahlevaninezhad et al., 2012) and a discrete control design (Das et al., 2013). A digital version of the sliding mode control was proposed in (Marcos-Pastor et al., 2016). In all the current loop control designs, the objective is to make the measured current closely follow the reference current waveform, which can then act as a control variable of the voltage loop. The nonlinear control methods commonly require division and square root operations, which tend to be much more computationally intensive than linear control methods.

In **Publication I**, the line voltage feedforward term is formed by using the Lyapunov function. The Lyapunov-function-based control design comprises a stabilizing control law along with the Lyapunov function, which can be used to prove the stability. The control law is a PI controller with a mains voltage feedforward term, which arises from the dynamic equation of the boost converter. The control is applied by using a digital controller and calculated by using only sum and multiplication functions.

With the standard cascade PI control, the crossover has an oscillatory response, which stems from an inadequate current loop gain (Louganski and Lai, 2007). The system is controlled by using an integrating control design,

and the result is a common PI controller with an input voltage feedforward term. The online implementation is simplified by omitting a division operation without affecting the current reference tracking performance. With the designed control, the crossover spike is completely removed from the input current waveform.

1.4.3 Improvements in the voltage control

The DC link performance is significantly affected by the requirements for the mains current distortion. The key issue is the rectified current adding a twice the mains frequency component to the DC link voltage. The ripple voltage is introduced to the current reference through the current control. Thus, the higher the gain of the voltage control is at the second harmonic of the mains frequency, the higher is the current distortion (Sebastian et al., 2010). The options to reduce the current-distorting effect of the DC link ripple are either to filter the ripple or design a nonlinear control and a controlled parameter to control the DC link indirectly, thereby reducing the effect of the ripple.

A ripple cancellation method where the ripple is estimated and the estimate is then subtracted from the measurement was introduced in (Leung et al., 2016b) and (Leung et al., 2016a). The estimation and cancellation were accomplished with a dedicated analog circuitry, and it was shown that the bandwidth of the DC link control can be increased. A similar estimation with digital signal processing was presented in (Chiang et al., 2016), where the authors used a phase-locked loop to accurately estimate the ripple. In both of these cases, the achieved performance is regulation of the DC link in about two mains cycles.

Nonlinear control solutions based on Lyapunov functions have also been proposed. In (Li and Zhong, 2014), the voltage control was designed with a measurement from peak load power, which was used to define a feedforward term to improve the voltage control loop regulation. The control loop was designed by using a discrete form of the Lyapunov equation. Another design with also a discrete nonlinear control was proposed in (Das et al., 2013). The controller is a nonlinear state-space controller, which controls both the current and the voltage. The performance of both controllers defined with a discrete form of the Lyapunov function is very similar and stabilizes the DC link in two to three mains cycles.

A fuzzy logic controller in the regulation of the DC link was studied in (Faucher et al., 2009). The use of fuzzy logic is a way to model human thinking by following a thought process like "if the error is large, and the rate of change for the error is negative and small, then a slight adjustment is needed." This thought process is modeled by fuzzy rules, which are then defuzzified to produce a control signal. The fuzzy logic controller uses measurements from the DC link and the derivative of the error between the set value and the measurement. The controller uses the Takagi–Sugeno (T-S) fuzzy logic for simple defuzzification. The reported performance of the fuzzy logic controller is comparable with Lyapunov-based controllers, with the system achieving regulation within three mains cycles.

In **Publication II**, the DC link control is designed by using a Takagi–Sugeno-style fuzzy control called a parallel distributed control (PDC). The controller is a nonlinear PI controller with the gain scheduled with the DC link voltage. The difference between the PDC control and the fuzzy logic control is that the PDC is based on a mathematical model of the system and can be analyzed using nonlinear control methods. When the traditional PI voltage loop offers a compromise between transient speed and steady-state harmonics, the developed fuzzy controller effectively decouples the transient and steady-state control performances making it possible to extend the transient speed without excessively distorting the input current. The PDC is cheap in terms of the required calculation effort and offers excellent static performance for both the DC link and input current when compared with a similarly tuned linear controller. The designed controller also stabilizes after a load step within three mains cycles, which matches or surpasses the performance attained with more complex nonlinear designs.

1.4.4 Dual sampling inverter control measurements

The performance of a control loop is significantly affected by the speed and accuracy of the measurements. In **Publication III**, custom hardware is designed to offer high-accuracy current measurement in a dual sampled single-phase inverter. The custom hardware is designed to provide minimal latency between the sampled measurement and the control update. The benefit of the optimized measurement is that the current measurement band can be significantly increased compared with a situation where the same ripple attenua-

tion is achieved with anti-aliasing filtering only. The current measurement bandwidth is maximized by using an AA filter with a bandwidth wider than the switching frequency, which does not significantly attenuate the switching ripple, yet decreases the slew rate of the sampled signal. The lower rate of change makes it possible to take accurate samples at a double switching frequency rate even at very high duty cycles.

1.5 Research methods and scientific contributions of the doctoral dissertation

All of the studies and the reported improvements in performance were verified in the laboratory by using experimental devices. The study applies system modeling and signal processing for the online measurements and the off-line data analysis and processing.

The key scientific contributions of this doctoral dissertation are

- Design of the PFC current control feedforward with Lyapunov's stability theorem
- Development of a nonlinear algorithm to reduce the harmonics and improve the speed of convergence in a single-phase PFC converter
- Design of improved current measurement in a high di/dt current waveform

1.6 Structure of the doctoral dissertation

The rest of the doctoral dissertation concentrates on utilizing the benefits of the digital control system, with the focus of the control design on the power factor correction. Chapter 2 introduces the power factor control hardware used in the study. Further, the chapter outlines the operation of the boost power factor control and the issues in the control of the DC link. The chapter addresses the choice that has to be made between the low steady-state current

harmonics and the fast transient performance of the control design. Moreover, the chapter discusses the use of fuzzy control for the DC link control and how it can be effectively used to improve the steady-state current waveforms when high gains are used in the DC link control.

The current control design is also analyzed by using the Lyapunov function. The use of a very simple feedforward to improve the performance of the current control is discussed, and it is shown to be derived from the direct use of the Lyapunov theory.

Chapter 3 focuses on the effect of the measurement timing and the method to mitigate the effects of high current slew rates and component delays. The accuracy of the measurement is important as the attainable performance is limited by the quality of the measurements used for the feedback.

Chapter 4 concludes the doctoral dissertation and discusses future research.

2 PFC control design

The performance of a PI-controlled PFC depends on achieving a high enough gain to provide distortion-free current reference tracking. Because the PFC can only feed power in one direction, the power supply is not controllable at the mains voltage zero cross instant, and the recovery from the mains zero crossing will add to the distortion if the response is too oscillatory. The achieved control gain might be too low because of a low switching frequency to mains frequency ratio or excessive noise present in the measurements.

In this case, the control frequency is limited and both of the boost switches are controlled with the same duty cycle. As reported in (Hannonen et al., 2016b), the control of the AC/DC power supply takes up to 69% of the processing resources when the control is run at 50 kHz, and therefore, only one controller is used to save resources. Furthermore, a design without an individual PFC control saves significant calculation resources as all of the power supply controls can be run on the same interrupt. This reduces the overhead when compared with a system with several interrupt service routines. The control is also run at a frequency lower than the switching frequency as opposed to a control with at every switching cycle, which would imply the control being run at 200 kHz.

The control is calculated at a rate of 50 kHz, and only the largest of the two measured currents are used for the feedback. Because the two boost converters are controlled with the same duty cycle, there is invariably a difference between the two measured currents, as the hardware is not exactly identical. The use of only the higher of the two currents was deemed the simplest option as the one calculated current controller then limits both currents without extra logic. On the downside, this also adds disturbance to the measurement, which is then amplified by the control.

2.1 Power factor control hardware used in the study

The objective of the entire PFC system is to shape the grid current to follow the grid voltage waveform and to keep the DC link voltage at 405 V. The PFC operation is accomplished by measuring the DC link voltage, the mains current, and the mains voltage, after which a feedback is used for forcing the PFC current to track the mains voltage. The DC link voltage is thus controlled by changing the level of the peak of the mains current to such a value that the charging and discharging currents are balanced.

The PFC hardware used to study condition monitoring and power factor correction has two interleaved boost converters for the PFC operation and an isolating DC/DC power supply for voltage level translation and galvanic isolation. The use of two boost converters in parallel helps in distributing losses and allows the use of smaller individual inductors. The parallel operation makes it possible to drive the boost converters in opposite phases, which significantly reduces the grid current ripple and thus simplifies further power line filtering. The power supply is presented in Figure 2.1 with the main components highlighted.

The control system measures the mains voltage u_{AC}, the DC link voltage u_{DC}, and the switch currents i_1 and i_2. The switch currents are measured using current transformers. In order to guarantee that the transformers are not saturated, the maximum duty cycle for the switch is limited to 0.8. This ensures that the designed circuit does not go into saturation, but duty cycle limitation also introduces a distortion at the voltage zero crossing instant as a result of insufficient volt seconds across the input inductor.

In order to save on the calculation resources available in the microcontroller, only one PI controller is used and the resulting duty cycle is used for modulation of both of the boost converters. In order to make the maximum current reference level work properly, only the larger of the measured currents is used for feedback.

The controller uses the mains voltage for current reference generation and the feedforward control of the current loop. The mains current is obtained by multiplying the output of the DC link voltage control with the measured mains

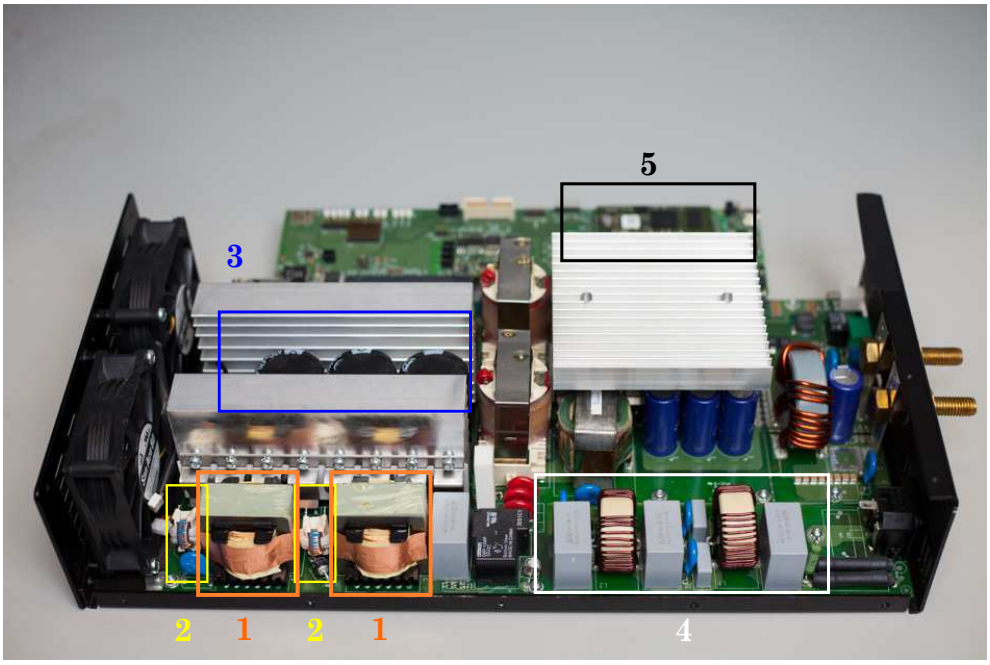


Figure 2.1. Power supply used for the experimental measurements. PFC inductors 1 and 2 are the current transformers used to measure the PFC current, 3 indicates the 1.5 mF DC link capacitors, 4 is the EMI filter, and 5 is the Xynergy embedded control platform.

voltage. The DC link voltage is used as a feedback for the voltage control.

2.2 Construction of the input current controller

The current control is designed first, using a Lyapunov function for construction of the current controller (**Publication I**).

The control model for the inductor current of a boost converter is

$$L\dot{i}(t) = u_{in}(t) - u_{dc}(t) \cdot d(t). \tag{2.1}$$

In order to increase the low-frequency performance, the system is augmented with an integral of the controlled state multiplied by an integral constant. As the integration is done by the controller, the integral gain can be freely chosen and is here denoted by K_I

$$L\dot{i}(t) = u_{in}(t) - u_{dc}(t) \cdot d(t) \tag{2.2}$$
$$\dot{\omega}(t) = K_I i(t). \tag{2.3}$$

The system (2.2)–(2.3) depends on the input voltage, the DC link voltage, and the controlled duty cycle $d(t)$. In order to design a stabilizing control law, a Lyapunov function ($V(x(t))$) is constructed. The control and the stability proof are thus built in parallel. The Lyapunov function is defined as a positive definite function, i.e., a function that only gets positive values, along which the dynamical system gets only negative values (Haddad and Chellaboina, 2008). Formally

$$V(0) = 0, \tag{2.4}$$
$$V(x(t)) > 0, \tag{2.5}$$
$$V'f(x(t)) \leq 0. \tag{2.6}$$

In order to use the Lyapunov function to construct a control law, a simple quadratic Lyapunov function is used

$$V = \frac{1}{2} i(t)^2 + \frac{1}{2} \omega(t)^2. \tag{2.7}$$

Substituting (2.2) and (2.3) into (2.6) yields

$$V'f(x(t)) = i(t) \cdot \dot{i} + \omega(t) \cdot \dot{\omega}(t) \tag{2.8}$$
$$= i(t) \left[u_{in}(t) - u_{dc}(t) \cdot d(t) \right] + K_I \omega(t) i(t). \tag{2.9}$$

The control law $d(t)$ then has to be designed such that (2.9) is negative definite. One option is

$$d(t) = \frac{1}{u_{dc}(t)} \left(u_{in}(t) + K_I \omega(t) + K_p i(t) \right). \tag{2.10}$$

Substituting (2.10) into (2.9) gives

$$
\begin{aligned}
V'f(x(t)) = & \\
& i(t)\cdot\Big[u_{in}(t) - u_{dc}(t)\cdot\frac{1}{u_{dc}(t)}\big(u_{in}(t) + K_I\omega(t) + K_p i(t)\big)\Big] && (2.11)\\
& \quad + K_I\omega(t)i(t) \\
& = -K_p i(t)^2. && (2.12)
\end{aligned}
$$

Because the Lyapunov function derivative is negative definite, the stability is guaranteed. The effect of the designed control can be seen by substituting (2.10) into the controlled system (2.2)–(2.3)

$$
\begin{aligned}
L\dot{i} &= u_{in}(t) - u_{dc}(t)\cdot\frac{1}{u_{dc}(t)}\big(u_{in}(t) + K_I\omega(t) + K_p i(t)\big) && (2.13)\\
&= -K_p i(t) - K_I\omega(t) && (2.14)\\
\dot{\omega}(t) &= K_I i(t). && (2.15)
\end{aligned}
$$

As can be seen, the system dynamics is only dependent on the positive constants set by the user. The effect of the mains voltage is thus practically eliminated from the system dynamics.

2.2.1 Simplifying the feedback controller

Because the direct application of the Lyapunov function requires a division operation, a simpler version of the controller is designed. It is pointed out that during operation, the DC link voltage varies within 10–20% of the reference value. The dynamics of the DC link is also significantly slower than the bandwidth of the current control loop, even at large load changes. Therefore, the DC link term given in (2.10) can be considered constant without a significant error, and the control can be calculated from the mains voltage measurement with multiplication by a constant of $\frac{1}{u_{\mathrm{ref}}}$, thus avoiding a division in the calcu-

lation of the control law. This simplifies the control law to

$$d(t) = \frac{1}{u_{\text{ref}}}\left(u_{\text{in}}(t) + K_I\omega + K_p i(t)\right) \tag{2.16}$$

$$= u_{\text{in}}(t)\cdot\frac{1}{u_{\text{ref}}} + \frac{K_p}{u_{\text{ref}}}i(t) + \frac{K_I}{u_{\text{ref}}}\omega(t). \tag{2.17}$$

Combining this with the integrating state in Figure 2.3 and noting that the gains K_p and K_i are freely chosen constants, the current controller is

$$d(t) = K_p i(t) + K_I\omega(t) + \frac{1}{u_{\text{ref}}}\cdot u_{\text{in}}(t) \tag{2.18}$$

$$\dot{\omega}(t) = K_I i(t). \tag{2.19}$$

As the gains K_P and K_I can be chosen freely, the factor multiplying them by a constant of $\frac{1}{u_{\text{ref}}}$ can be omitted. The resulting controller can be considered a standard PI controller with an extra feedforward term $\frac{1}{u_{\text{ref}}}\cdot u_{\text{in}}(t)$ added for decoupling the mains voltage dynamics.

2.2.2 Control tuning

The control design of a PI control is designed by traditional methods using a Bode plot. Because only the largest of the sampled inductor currents is used for the control, the current loop dynamics is calculated applying a 500 µH inductance. With the feedforward term canceling the effect of the mains voltage, the modeled system is the current equation of the input inductor with the inductor voltage as the controlled parameter

$$\dot{i}(t) = \frac{u(t)}{L}. \tag{2.20}$$

The current loop is designed to have a minimum gain of 40 dB at the mains voltage frequency and a crossover frequency of approximately 1 kHz, which provides a phase shift of less than 0.05° for the reference tracking response. The final current loop is then tuned experimentally to yield a satisfactory response. The final tuned controller loop gain is shown in Figure 2.3 with the gain given in Table 2.1. The bandwidth of the controller can be read from the 0 dB point of the loop gain function, and it can be seen to be 1.3 kHz with the phase margin of 68°. The effect of the feedforward term is presented with experimental results in Section 2.4.

2.2.3 Effect of the DC link voltage on the inductor current control

Because the actual DC link voltage influences the actual current in the inductor, but its effect is not mitigated entirely by the simplified control (2.18), the effect of the DC link voltage variation is estimated. Because the effect enters the control loop through the duty cycle, the effect is investigated by calculating the inductor current with an additive perturbation term $\Delta(t)$, which represents the ripple signal of the DC link. The response is modeled by adding the perturbation to the dc link voltage in the control model (2.1) which yields

$$L\dot{i}(t) = u_{\text{in}}(t) - (u_{\text{dc}}(t) + \Delta(t)) \cdot d(t) \tag{2.21}$$

$$\Leftrightarrow u_{\text{in}}(t) - u_{\text{dc}}(t) \cdot d(t) - \Delta(t) \cdot d(t) \tag{2.22}$$

As the disturbance is modeled as an additional input, the disturbance response can be calculated from the closed loop equation by adding the disturbance to the closed loop equation (2.13) - (2.15). The duty cycle $d(t)$ gets values between 0 and 1, the worst-case effect of the disturbance is obtained when $d(t) = 1$. Using the worst case amplitude for the disturbance yields

$$L\dot{i}(t) = -K_p i(t) - K_I \omega(t) - \Delta(t) \tag{2.23}$$

$$\dot{\omega}(t) = \quad K_I i(t). \tag{2.24}$$

The effect of the DC link voltage disturbance on the inductor current can be evaluated by calculating the response from $\Delta(t)$ to inductor current $i(t)$ which is seen in Figure 2.2. It should be noted that with the simplification of omitting the division in the control algorithm, the effect of the DC link is not mitigated. However, with the nominal 400V DC link voltage and during normal operation, the voltage varies between 390 and 410 V at double the mains frequency, and thus the disturbance has an amplitude of less than 10 % of the modulation range. This effect is further attenuated by more than -20 dB by the control as seen in the disturbance sensitivity function response shown in Figure 2.2, and therefore, the DC link voltage ripple has a limited effect on the control performance.

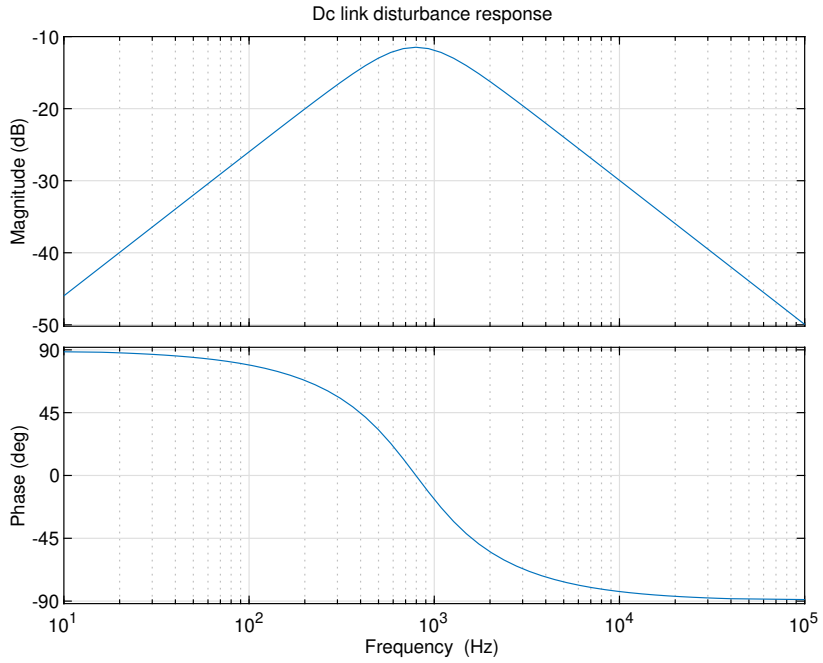


Figure 2.2. Effect of the DC link disturbance on the inductor current.

Table 2.1. Converter current control parameters

Symbol	Quantity	Value
L	boost inductor	500 µH
C	DC link capacitance	1500 µF
$K_{\mathrm{P_I}}$	proportional gain	3.7500
$K_{\mathrm{I_I}}$	integrator gain	12500
f_{ctrl}	control calculation frequency	50 kHz

2.3 Nonlinear DC link voltage control

The voltage control is designed next, using a Takagi–Sugeno controller for construction of the voltage controller (**Publication II**). The DC link control

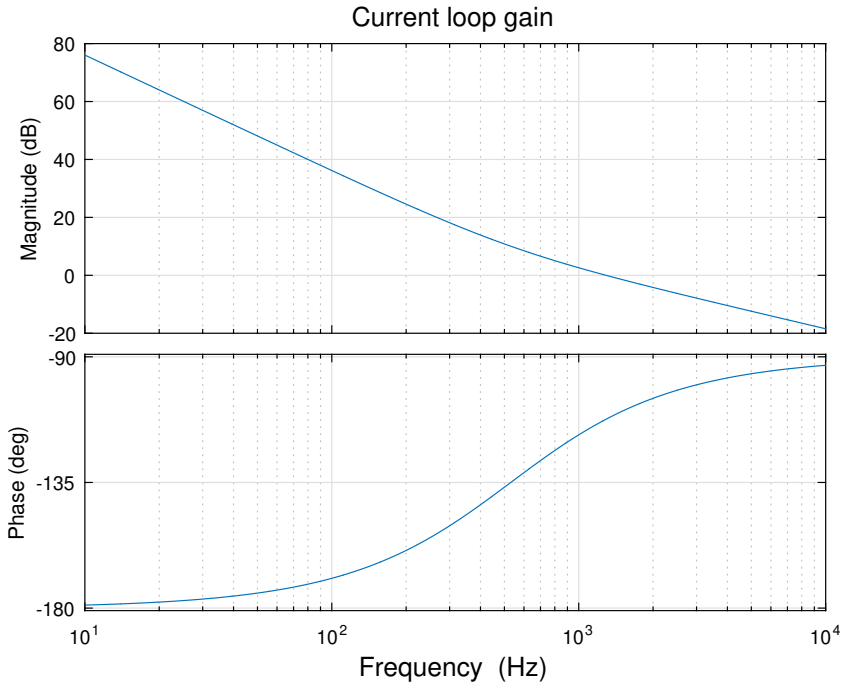


Figure 2.3. Loop gain of the PFC current loop.

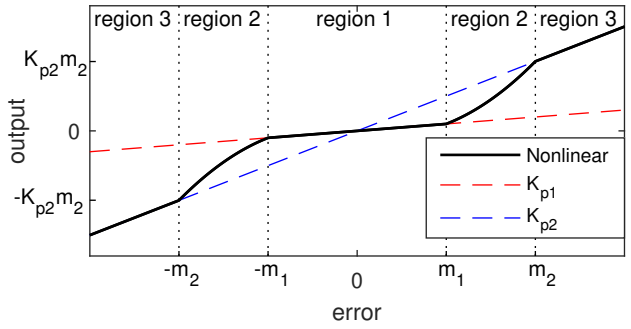


Figure 2.4. Nonlinear voltage control gain is a weighted sum of the two PI controllers. The widths of the regions are chosen so that the maximum load ripple amplitude is within the linear region.

balances the input and output currents so that the average value of the DC link is kept constant. The bandwidth of the control has to be high enough to ensure that at the moment of the full load step, the DC link voltage will not drop so

low that either the DC/DC converter or the PFC current control will lose its ability to control the voltage. The speed of the load step is determined by the bandwidth, or correspondingly, the gain of the DC link control. As discussed in (Sebastian et al., 2009), the higher gain also results in higher harmonics of the input current.

In order to increase the convergence speed, the influence of the DC link ripple has to be mitigated. This increases the distortion caused by the voltage loop, and therefore, an improved control is designed in such a way that low gains are used for the DC link ripple, but the gain is increased as the error increases when a higher control effort is needed. This type of control can be designed by using a fuzzy control.

Fuzzy models of Takagi–Sugeno (T-S) style can be used to define nonlinear models by using several linear models and weighting functions called fuzzy membership functions. A T-S model-based control has thus several state-space control gains, which are combined together with a fuzzy logic. A T-S-type nonlinear control allows mathematical analysis with matrix inequalities, and it can be used with the robust and optimal control theory (Tanaka and Wang, 2004).

The basic idea behind the fuzzy control is illustrated in Figure 2.4, which shows the composite gain function. The gain function is designed to have three regions. In region 1, the gain is constant and the gain function is linear in terms of error. The constant, linear gains limit the amount of additional distortion from the nonlinearity of the controller. In region 3, the gain is also linear with a high gain, and region 2 has gains that are an average of the low and high gains. In this way, the high gain control is used when the error is large, but low gains are used to provide a low distortion, and there is a transition region where the gain changes with the size of the error. The membership functions with which the gains are weighted are shown in Figure 2.5. Mathematically, these functions are

$$M_1 = \frac{m_2 - e(t)}{m_2 - m_1}, \quad M_2 = \frac{e(t) - m_1}{m_2 - m_1} \tag{2.25}$$

$$K_1 = [K_{\mathrm{P}_1}, K_{\mathrm{I}_1}], \quad K_2 = [K_{\mathrm{P}_2}, K_{\mathrm{I}_2}], \tag{2.26}$$

where K_1 and K_2 are the gain vectors for the high- and low-gain PI controllers. The controller then uses the two PI controllers and weighs their gains with the

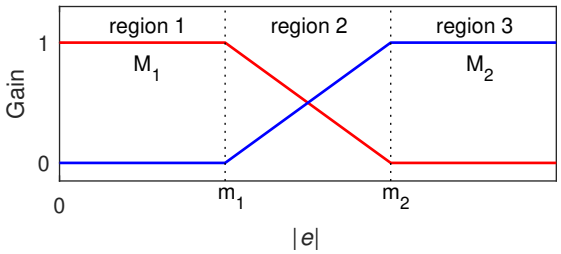


Figure 2.5. Membership functions for fuzzy systems.

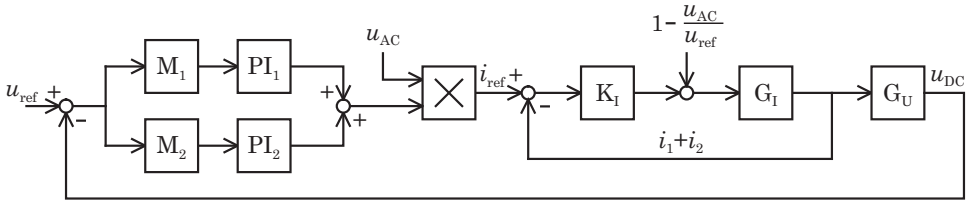


Figure 2.6. Final PFC control with the designed current and voltage control.

membership functions (2.25) to provide the appropriate control action. The block diagram of the fuzzy controller is shown in Figure 2.6. A control of this type is called a parallel distributed compensator (PDC) (Wang et al., 1995), and it is written as

$$u = \sum_{i=1}^{r} M_i K_i x(t), \quad i = 1,2,3...r. \tag{2.27}$$

The PDC allows a systematic state feedback control design to be made directly from the T-S fuzzy model and also offers a framework for analyzing the stability of the control design.

2.3.1 DC link control design

The control model for the DC link capacitor voltage is designed with the input current $i(t)$ as a controlled variable. The modeled plant is thus

$$C \cdot \dot{u}_{\mathrm{DC}}(t) = i(t) - \frac{u_{\mathrm{DC}}(t)}{R}, \tag{2.28}$$

where $u_{\mathrm{DC}}(t)$ is the controlled DC link voltage, C is the DC link capacitance, $i(t)$ is the controlled current, and R models the load as a resistance. As the

control objective is to regulate the error between the measured DC link voltage and the reference to zero, the system is represented with the controlled state being the error between the DC link voltage $u_{\mathrm{DC}}(t)$ and the reference u_{ref}

$$e(t) = u_{\mathrm{DC}}(t) - u_{\mathrm{ref}}. \tag{2.29}$$

With the change of coordinates, the controlled plant is

$$\dot{e}(t) = \frac{1}{C} \cdot \left(i(t) - \frac{e(t)}{R} \right). \tag{2.30}$$

As with the current control, the plant is augmented with an integrating state to guarantee a zero steady-state error. Adding an integrator state $\dot{\omega}(t)$ gives

$$u(t) = -K_P e(t) + \omega(t) \tag{2.31}$$
$$\dot{\omega}(t) = -K_I e(t). \tag{2.32}$$

Combining (2.30) and (2.31)–(2.32) gives the state-space model of the capacitor voltage controlled with an integrating controller

$$\dot{e}(t) = e(t) \cdot \left(-\frac{K_P}{C} - \frac{1}{RC} \right) + \frac{1}{C}\omega(t) \tag{2.33}$$
$$\dot{\omega}(t) = -K_I e(t). \tag{2.34}$$

To control the system (2.33)–(2.34) with the PDC controller (2.27), the PI controller (2.31)–(2.32) is replaced by

$$u(t) = e(t) \cdot (M_1 K_{\mathrm{P}_1} + M_2 K_{\mathrm{P}_2}) + \omega(t) \tag{2.35}$$
$$\dot{\omega}(t) = e(t) \cdot (M_1 K_{\mathrm{I}_1} + M_2 K_{\mathrm{I}_2}). \tag{2.36}$$

The membership functions M_1 and M_2 determine the control behavior so that when the error is less than m_1 or more than m_2, only a single PI controller is used. Therefore, the controller implementation differs from the traditional PI control only in region 2, where the gains are interpolated.

For implementation, the controller (2.35)–(2.36) is converted into a simpler form. As stated above, in the case of the PI-controlled DC link voltage, the measured signal $z(t)$ is the absolute value of the error $|e(t)|$ between the measured DC link voltage and the reference, and m_i are the voltage levels used to schedule the gains of the controllers. Substituting (2.25) into (2.35)–(2.36) yields

$$u(t) = e(t) \cdot \left((m_2 - |e(t)|) \frac{K_{\mathrm{P}_1}}{m_2 - m_1} + (|e(t)| - m_1) \frac{K_{\mathrm{P}_2}}{m_2 - m_1} \right) + \omega(t) \tag{2.37}$$

$$\dot{\omega}(t) = e(t) \cdot \left((m_2 - |e(t)|) \frac{K_{\mathrm{I}_1}}{m_2 - m_1} + (|e(t)| - m_1) \frac{K_{\mathrm{I}_2}}{m_2 - m_1} \right). \tag{2.38}$$

By rearranging the terms (2.37)–(2.38), the following form is obtained for the controller

$$u(t) = \frac{K_{\mathrm{P}_1} m_2}{m_2 - m_1} e(t) - \frac{K_{\mathrm{P}_2} m_1}{m_2 - m_1} e(t) + \left(\frac{K_{\mathrm{P}_2}}{m_2 - m_1} - \frac{K_{\mathrm{P}_1}}{m_2 - m_1} \right) e(t) \, |e(t)| + \omega(t) \tag{2.39}$$

$$\dot{\omega}(t) = \frac{K_{\mathrm{I}_1} m_2 e(t)}{m_2 - m_1} - \frac{K_{\mathrm{I}_2} m_1 e(t)}{m_2 - m_1} + \left(\frac{K_{\mathrm{I}_2}}{m_2 - m_1} - \frac{K_{\mathrm{I}_1}}{m_2 - m_1} \right) e(t) \, |e(t)| . \tag{2.40}$$

Defining the constants in (2.39)–(2.40) as

$$p = \frac{1}{m_2 - m_1} \tag{2.41}$$
$$K_p = (pK_{\mathrm{P}_1} m_2 - pK_{\mathrm{P}_2} m_1) \tag{2.42}$$
$$K_i = (pK_{\mathrm{I}_1} m_2 - pK_{\mathrm{I}_2} m_1) \tag{2.43}$$
$$K_{\mathrm{p}^2} = (pK_{\mathrm{P}_2} - pK_{\mathrm{P}_1}) \tag{2.44}$$
$$K_{\mathrm{i}^2} = (pK_{\mathrm{I}_2} - pK_{\mathrm{I}_1}), \tag{2.45}$$

the controller (2.39)–(2.40) can be simplified to

$$u(t) = e(t) \cdot K_p + e(t) \cdot |e(t)| \cdot K_{\mathrm{p}^2} + \omega(t) \tag{2.46}$$
$$\dot{\omega}(t) = e(t) \cdot K_i + e(t) \cdot |e(t)| \cdot K_{\mathrm{i}^2}. \tag{2.47}$$

The full nonlinear PI controller is achieved by combining the PI controllers and the regions of the membership functions

$$\begin{aligned}
&\text{if } |e(t)| < m_1 \\
&\qquad u(t) = e(t) \cdot K_{\mathrm{P}_1} + \omega(t) \\
&\qquad \dot{\omega}(t) = e(t) \cdot K_{\mathrm{I}_1} \\
&\text{else if } |e(t)| > m_2 \\
&\qquad u(t) = e(t) \cdot K_{\mathrm{P}_2} + \omega(t) \\
&\qquad \dot{\omega}(t) = e(t) \cdot K_{\mathrm{I}_2} \\
&\text{else} \\
&\qquad u(t) = e(t) \cdot \left(K_p + |e(t)| \cdot K_{\mathrm{p}^2} \right) + \omega(t) \\
&\qquad \dot{\omega}(t) = e(t) \cdot (K_i + |e(t)| \cdot K_{\mathrm{i}^2}).
\end{aligned} \tag{2.48}$$

Formulated in this way, the fuzzy PI controller increases the complexity of the standard PI control only by two comparison operations, two multiplications, two sums, and an absolute value calculation.

2.3.2 Voltage control tuning

As discussed in (Sebastian et al., 2009), the maximum bandwidth for the PFC voltage control is less than 44 Hz in order to be in compliance with the Class

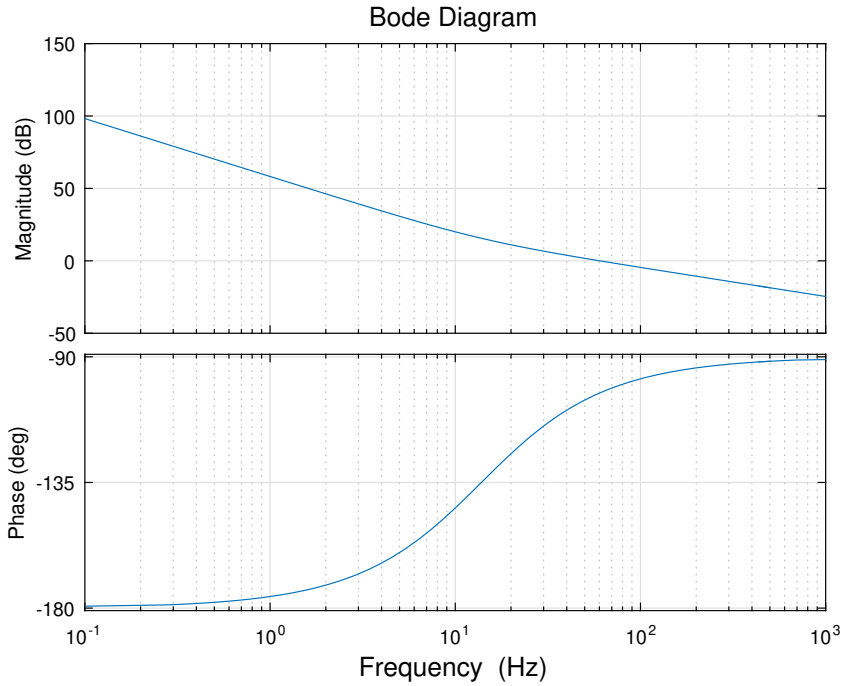


Figure 2.7. Bode plot for the fast voltage gain.

D limits of the IEC standard 61000-3-2 (IEC61000-3-2, n.d.). The control was tuned experimentally, and the final loop is shown in Figure 2.7. The corresponding gains are given in Table 2.2. The gain crossover is 34 Hz with the 65 degree phase margin. The chosen bandwidth is lower than the theoretical maximum, but it gives some margin for the extra distortion caused mainly by the crossover distortion resulting from the duty ratio limit, which is imposed by the current transformers used for measurement.

The simulated load step with a PFC simulation and the load step calculated directly with the dynamic model are shown in Figure 2.8 and compared with the measured step response. Both the simulated and calculated responses match very well the measured response, which validates the modeling of the PFC circuit. The PFC is operating in the DCM with a 150 W load, for which the current controller is not designed, and therefore, the DC link contains extra harmonics not present in the simulation or during 2.4 kW loading.

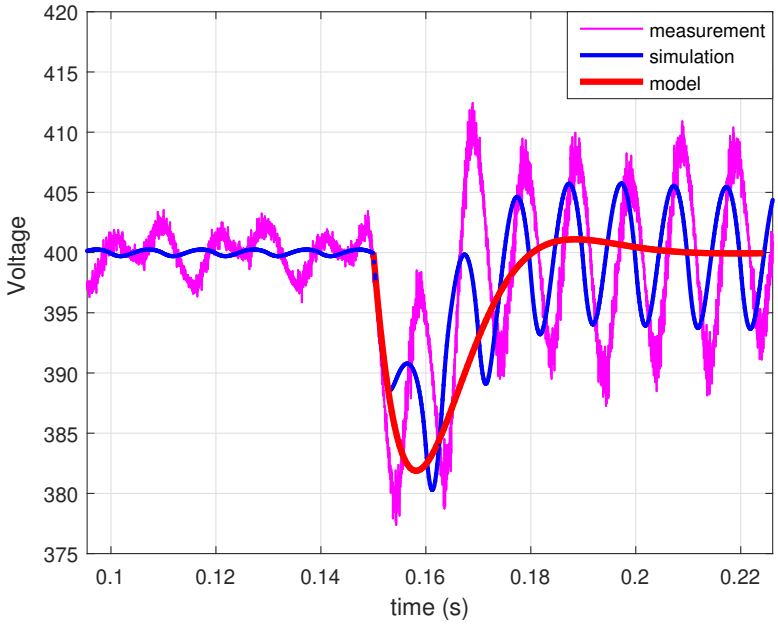


Figure 2.8. Load step response from 150 W to 2.5 kW measurement compared with a simulation with a PFC circuit and a response calculated from a state-space model.

2.3.3 Controller stability

With the nonlinear control, the fuzzy DC link controller belongs to the class of nonlinear systems with sector-bounded, memoryless nonlinearity, which is a function of measured output. The sector that bounds the nonlinearity is seen in Figure 2.4. The stability problem of a feedback system with sector-bounded nonlinearity has been shown to be effectively solvable by the use of linear matrix inequalities (Tingshu Hu et al., 2004) (Yung-Shan Chou et al., 1999).

The system is stable if it satisfies the circle criterion for the Nyquist plot; in other words, the Nyquist curve of the system does not enter a circle defined by the sector that bounds the nonlinearity (Haddad and Chellaboina, 2008). The gain of the fast PI control is designed to be twice as high as the low gains, and thus, the circle is defined as the crossings by the inverse of the slopes, being with the proposed control -1 and $-\frac{1}{2}$. The Nyquist curve of the loop gain is shown in Figure 2.9; as can be seen, the curve does not pass through the circle. Thus, the linear system with the sector-bounded nonlinearity is stable.

The stability of a system comprised of several subsystems can be verified if a common positive definite matrix P, which is a solution to the Lyapunov inequality (2.49), can be found (Tanaka and Wang, 2004). When the system is described with more than one linear model, the Lyapunov inequality can be written in the form

$$A_i^T P + PA_i < 0, \quad i = 1,2...r, \tag{2.49}$$

where A_i are the state matrices for all the subsystems. Then, the matrix P forms a quadratic Lyapunov function with the system states

$$V(x(t)) = x(t)^T Px(t). \tag{2.50}$$

With the PDC controller, the proof of stability for the closed-loop DC link control is obtained by finding a common P for the closed-loop system matrices A_i such that the Lyapunov inequality given in (2.49) holds. Because the PFC is loaded using a constant power load, the load does not provide any damping to the system, and thus, the load resistance $R = \infty$. The system

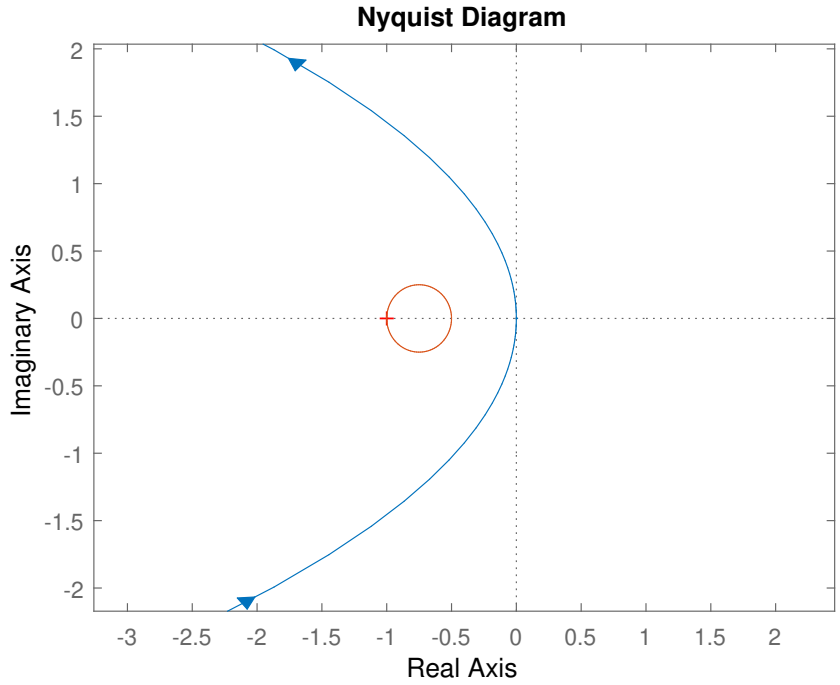


Figure 2.9. Nyquist plot of the loop gain of the DC link voltage control, with the forbidden region indicated by a red circle. The two points that define the circle are the slopes of the sector that bounds the nonlinearity of the composite gain function, which in this case are -1 and $-\frac{1}{2}$ as the high gains obtained by multiplying the slow gains by two.

(2.33)–(2.34) can be written in a matrix form as

$$A_1 = \begin{bmatrix} -\frac{K_{P1}}{C} & \frac{1}{C} \\ -K_{I1} & 0 \end{bmatrix} = \begin{bmatrix} -261.267 & 666.667 \\ -34.074 & 0 \end{bmatrix}, \tag{2.51}$$

$$A_2 = \begin{bmatrix} -\frac{K_{P2}}{C} & \frac{1}{C} \\ -K_{I2} & 0 \end{bmatrix} = \begin{bmatrix} -522.467 & 666.667 \\ -68.148 & 0 \end{bmatrix}. \tag{2.52}$$

The positive definite matrix

$$P = \begin{bmatrix} 16.3972 & -6.6741 \\ -6.6741 & 285.5394 \end{bmatrix} \tag{2.53}$$

can be verified to prove the stability by substituting A_1 and A_2 and the common P (2.53) into the Lyapunov inequality (2.49). Upon substitution, the matrices can be verified to be negative definite.

$$A_1^T P + P A_1 = \begin{bmatrix} -8113 & 2942 \\ 2942 & -8899 \end{bmatrix} < 0 \tag{2.54}$$

$$A_2^T P + P A_2 = \begin{bmatrix} -14251 & -5040 \\ -5040 & -8899 \end{bmatrix} < 0 \tag{2.55}$$

2.4 Experimental results

The Lyapunov-based control is compared with a standard PI controller. The PI control gains are the same, and the only difference comes from the feedforward term. First, the performance of the PFC is tested in the steady state with a standard PI controller without the feedforward and with the full load. With the standard PI control there is a large current spike at the zero cross instant as can be seen in Figure 2.10. The current peaking is exacerbated by the limitation of the duty cycle. As analyzed in (Hui Qu and Ruan, 2006), large spikes are present at the zero cross instant as a result of the phase lead of the mains voltage to the current.

The effect of the Lyapunov-based control is shown in Figure 2.11. When the designed controller applying the Lyapunov-based control with the line

voltage feedforward is used, the current peak at the zero crossing instant is completely eliminated. The distortion at the zero crossing comes from the limitation of the duty cycle. The grid voltage tracking of the Lyapunov controller along with the corresponding duty cycle obtained from the embedded system is shown in Figure 2.12. This also clearly shows the maximum duty ratio limitation to 0.8. The limitation is added to prevent saturation of the current transformers.

The current reference tracking response during a load step is shown in Figure 2.13. The load is stepped from 150 W to 2.4 kW, and the waveforms are captured from the embedded controller. During the 150 W load, the current reference tracking is not perfect as the PFC is operating in the DCM, and once the system enters the normal CCM operating mode, the current can be seen to track the reference. Because the PFC has a diode input bridge, the mains voltage measurement is also rectified.

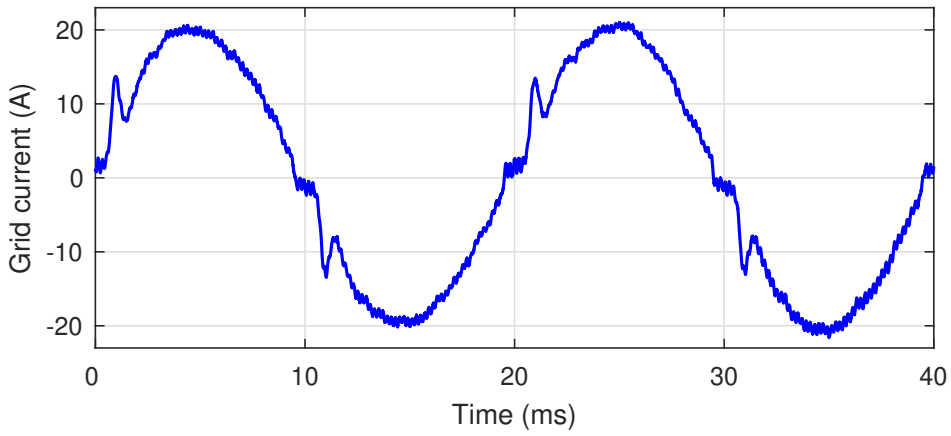


Figure 2.10. Full nominal load with a PI control without the feedforward term.

2.4.1 Nonlinear DC link voltage control measurements

The dynamic performance of the fuzzy control was tested with load steps from 150 W to 2.4 kW and from 2.4 kW to 150 W. The PFC current loop was controlled by using the Lyapunov-based controller. The mains current and DC link dynamics are shown in Figure 2.15a and Figure 2.15b along with the underlying fast linear controller. At the 150 W load, the PFC is operating in

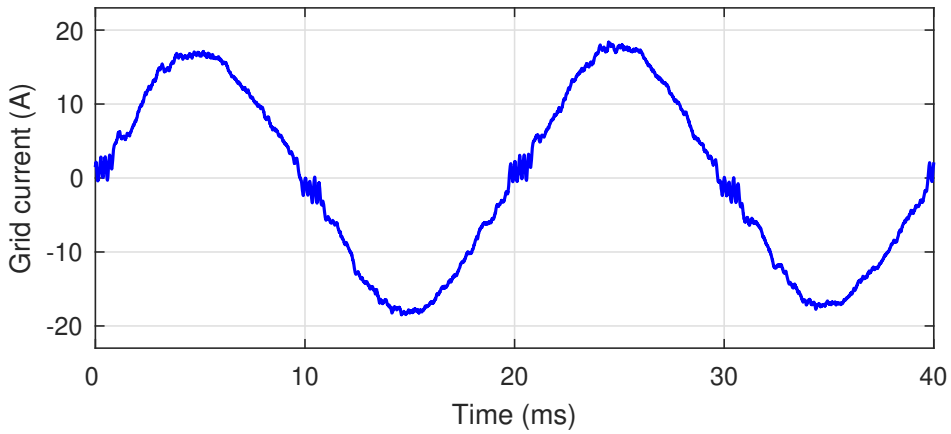


Figure 2.11. System at the nominal 3 kW load with the control derived by using the Lyapunov function.

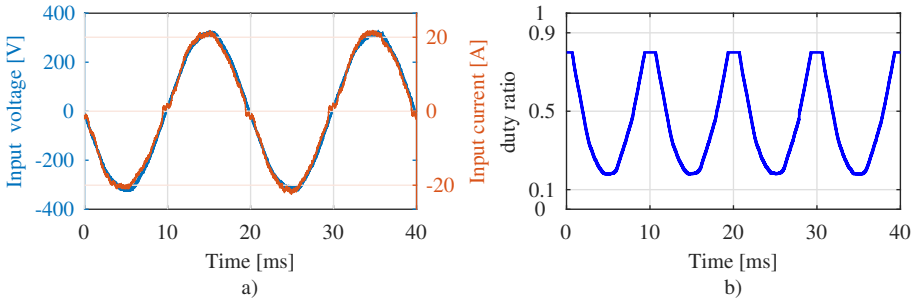


Figure 2.12. PFC current and mains voltage with the corresponding duty command. The measurements are taken with the embedded system.

the DCM, which causes heavy distortion of the current as the controller is designed to operate in the CCM.

The load steps are applied to the full bridge converter that loads the PFC converter, which is effectively a constant power load to the DC link. The PFC converter parameters are given in Table 2.2.

The converter operates in the DCM when the power level is 150 W, and therefore, the current is significantly distorted. The distortion at a low power is not significant in terms of the system design, because most industrial power supplies are operated at moderate power levels for most of the time. Nevertheless, it is interesting to note that the fuzzy DC link control has much less

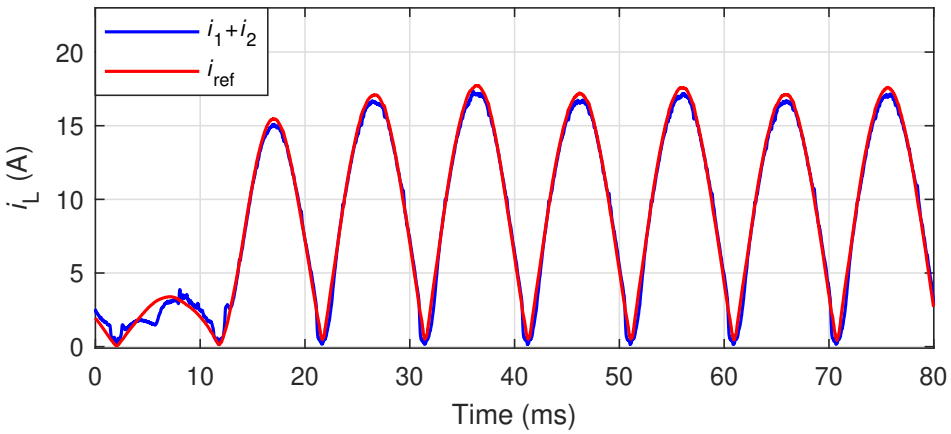
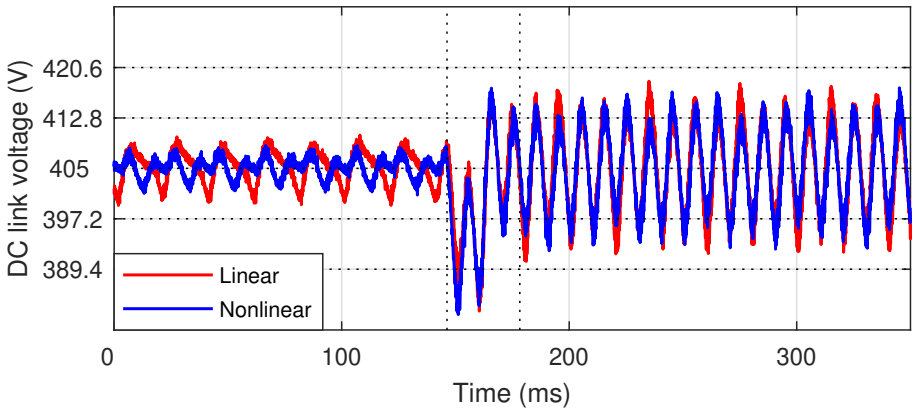


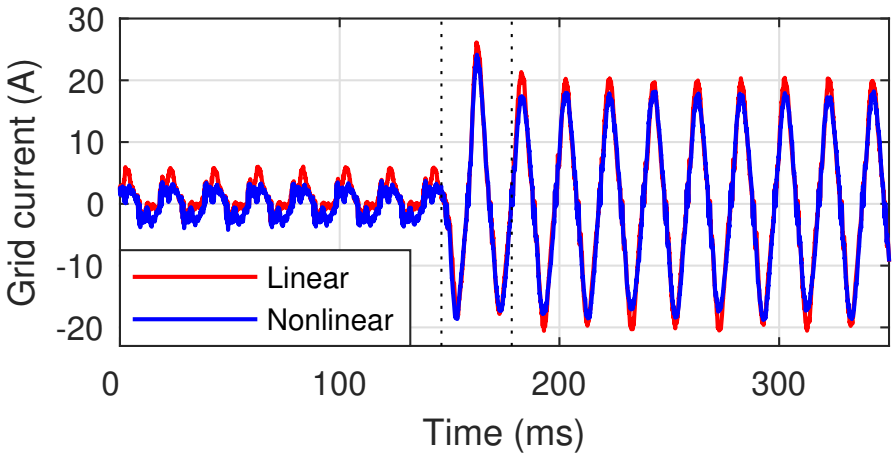
Figure 2.13. Current reference tracking response taken from the internal measurements of the embedded system during a load step. The current is distorted before the step because of the DCM current. The reference is the nonlinear PI controller output multiplied by the mains voltage measurement.

distortion than the linear control even at low power levels. The dynamics of the DC link is practically equivalent between linear and nonlinear controls, which is expected as the same fast control is used. The linear control operates with a higher peak current and distortion. The reduction in the mains current distortion with the fuzzy controller is visible when the harmonics are compared in Figure 2.16. As the gain is halved, the fuzzy controller has only half of the THD of the linear control.

When the load is stepped down, the controllers have practically equivalent dynamics as seen in Figure 2.15a and Figure 2.15b. As the PFC is not bidirectional, it cannot feed the power back to the mains, and thus, the PFC operation is simply halted when the DC link crosses 420 V. The dynamics is thus independent of the control during a large load step-down.

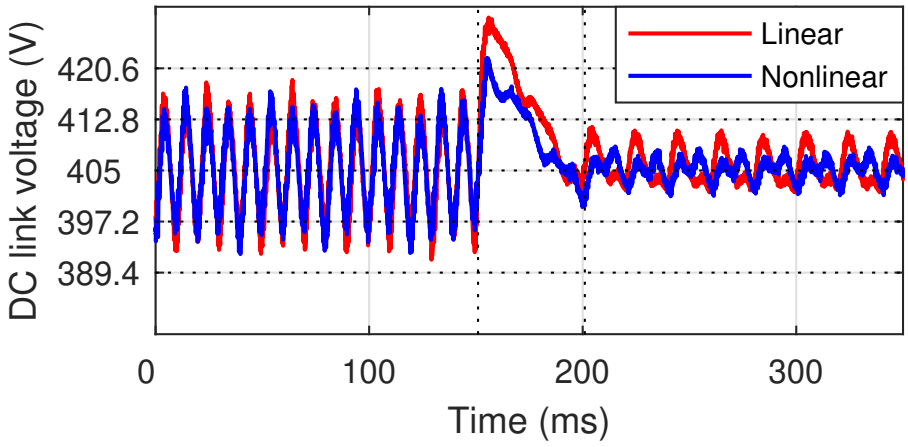


(a)

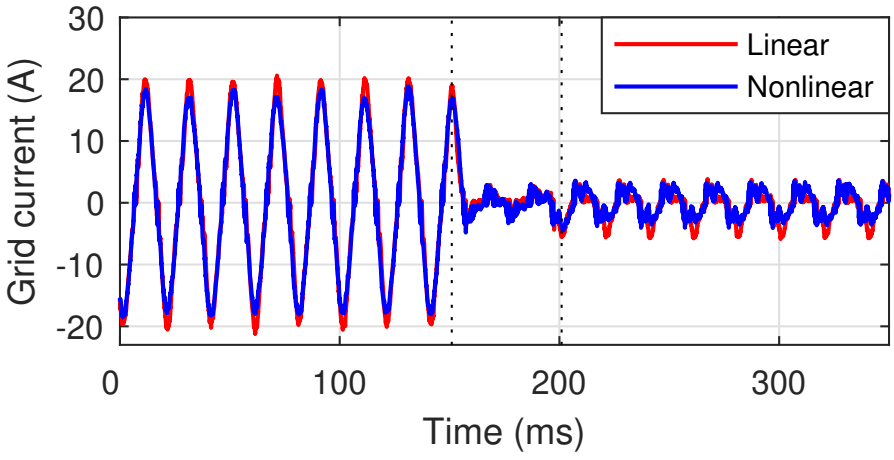


(b)

Figure 2.14. a) Voltage of the DC link and b) input current waveform during a load step from 150 W to 2.4 kW. The load step is applied to the system at t = 150 ms. The voltages on the y-axis represent the gain regions of the nonlinear controller. The settling time of the load step for both control methods is 50 ms.



(a)



(b)

Figure 2.15. a) Voltage of the DC link and b) input current waveform during a load step from 2.4 kW to 150 W. The load step is applied to the system at t = 150 ms. The voltages on the y-axis represent the gain regions of the nonlinear controller. The settling time of the load step for both control methods is 50 ms.

Table 2.2. Converter parameters

Symbol	Quantity	Value
K_{P_1}	proportional gain (slow)	0.3919
K_{I_1}	integrator gain (slow)	34.0741
K_{P_2}	proportional gain (fast)	0.7837
K_{I_2}	integrator gain (fast)	68.1481
f_{ctrl}	control calculation frequency	5 kHz

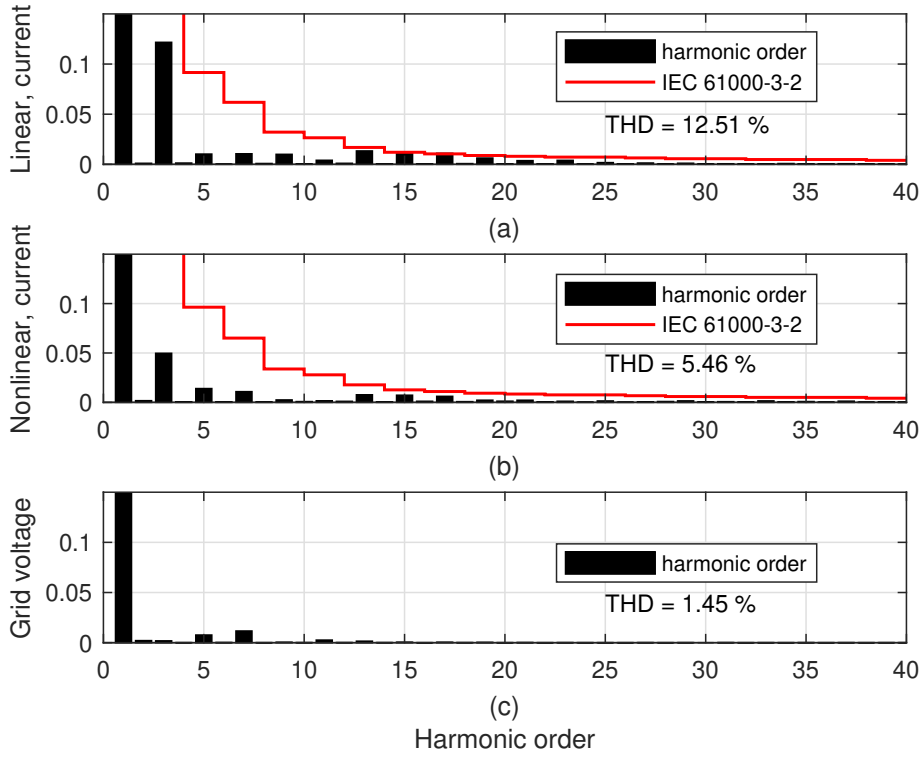


Figure 2.16. Comparison of the input current harmonic content with a) linear and b) nonlinear controllers. The figure c) shows the harmonic content of the mains voltage when the converter is turned off. Harmonics are calculated from a 30 second averaged measurement.

2.5 Discussion on the PFC voltage and current controls

Both of the designed controllers share a similar philosophy. They start with a linear control, but extend the performance by adding features from the non-

linear control theory. The current control is designed directly by using a Lyapunov function, which draws on the dynamics of the system to derive the controller. The resulting control is reminiscent of a PI control, but with an additional feedforward term to decouple the input voltage dynamics. Typically, the PFC current control is designed assuming that the system is linear, and a simple additive feedforward term can be added to improve the performance.

The presented control loop design has the same principal idea of mitigating the effect of the line voltage as was studied for example in (Xie et al., 2004) and (Louganski and Lai, 2007). In both of these papers, the authors use transfer functions to model the input admittance of the boost PFC circuit, and they arrive at a line voltage feedforward, which is a pure gain or a phase lead type compensator for the input admittance. In the approach presented in the present study, the additional feedforward is aimed to mitigate the line voltage signal entering the state equation instead of the effect of the input admittance on the input current.

The DC link controller is similarly derived from the dynamics of the system. The widths of the regions can be calculated from the DC link ripple, which is a design factor in the PFC control. The resulting controller also uses the fast PI control gains, and therefore, it can probably simply replace the control code present in the PFC to reduce the steady-state current harmonics. Even though the fuzzy control theory is used to derive the controller, the underlying idea is simple to understand even without any knowledge of fuzzy systems. The benefit of adopting the T-S control approach is that the resulting controlled system can be analyzed with the Lyapunov theory, and the stability can be numerically proved.

With the proposed control, the obtained load transient dynamics is at least as good as can be achieved by the best linear control (Sebastian et al., 2010). The T-S nonlinear control allows the DC link voltage loop to be designed to recover from a load step in approximately two mains cycles while still performing within the harmonic current standards, which is at least as good as reported in (Pahlevaninezhad et al., 2012), (Leung et al., 2016b), (Li and Zhong, 2014), (Das et al., 2013), all of which involve significantly more complex control calculations.

3 Control design of a single-phase inverter considering improved timing of the measurement

The control performance of an inverter is limited by the inverter output filter, the switching frequency f_{sw}, and control delays. Primary delay sources have been reported to be the anti-aliasing filter, analog-to-digital conversion, computation delay, gate driver, and switching delays (Kim et al., 2014; Vukosavic et al., 2016). Half of the switching frequency determines the Nyquist frequency of the control as the current measurement and the computed PWM voltage reference values are zero-order hold (ZOH) by nature for PWM inverters (Ma et al., 2018). The time taken by sampling and control calculation determines the control delay, which poses a limit on the control bandwidth. In order to maximize the control performance, the inverter can be sampled and controlled twice per switching cycle (Blasko and Kaura, 1997).

Optimizing the current sampling bandwidth and accuracy has been a topic of studies in the literature. For instance in single-phase inverters, scaling of the current measurement and offset errors have been compensated with a proportional resonant controller (Kim et al., 2013). For three-phase inverters, scaling and offset error compensation methods, such as a periodic disturbance observer and a proportional integral plus two resonant controllers have been proposed (Yamaguchi et al., 2014; Kim et al., 2014; Vukosavic et al., 2016; Nam et al., 2017). These compensation methods are primarily executed in the dq frame.

The problem with synchronous sampling can be solved by using an AA filter with a bandwidth higher than the switching frequency, and the sample is timed to the low-pass-filtered version of the current (**Publication III**). The basic idea is illustrated with the unfiltered and filtered versions of the inductor current, which can be seen in Figure 3.1. The purpose of the AA filter is

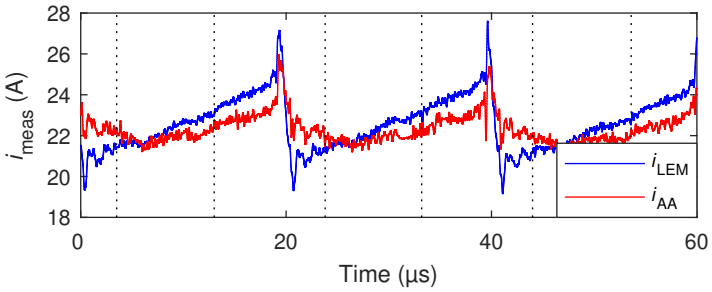


Figure 3.1. Current measurements from the current sensor output (i_{LEM}) and the anti-aliasing filter output (i_{AA}). The measured current measurement sampling trigger signal is indicated by a dashed line.

not to provide significant filtering per se, but to limit the measurement signal slew rate to a more manageable value. Because the fast di/dt slopes are filtered instead of the switching ripple, accurate placement to the middle of the current waveform is less significant, and the phase delay of the AA filter can be kept to a minimum.

The effect of the proper delay tuning and noise in measurement is illustrated in unloaded and resistive load conditions with the dual sampled current shown in Figure 3.2. The inverter has a 50 Hz and 220 Vrms output reference. Unloaded, the inverter voltage is imposed on the EMI filter capacitors, which also load the inverter with a roughly 300 VA capacitive load. This sets the no-load current reference at around 1.4 Arms. The effect of the AA filter is clearly seen in Figure 3.2, where the difference between two sampling instants is illustrated. The AA filter itself does very little to mitigate the effects of the switching ripple, but with proper timing, the switching ripple is almost completely removed from the measurement. The mean switching noise is reduced by over 90% in both the loaded and unloaded cases. The sample time instant was tuned experimentally. The AA filter caused a slightly over 2 µs delay for the switching frequency component, and the final timing value used for the experimental results was 3.5 µs.

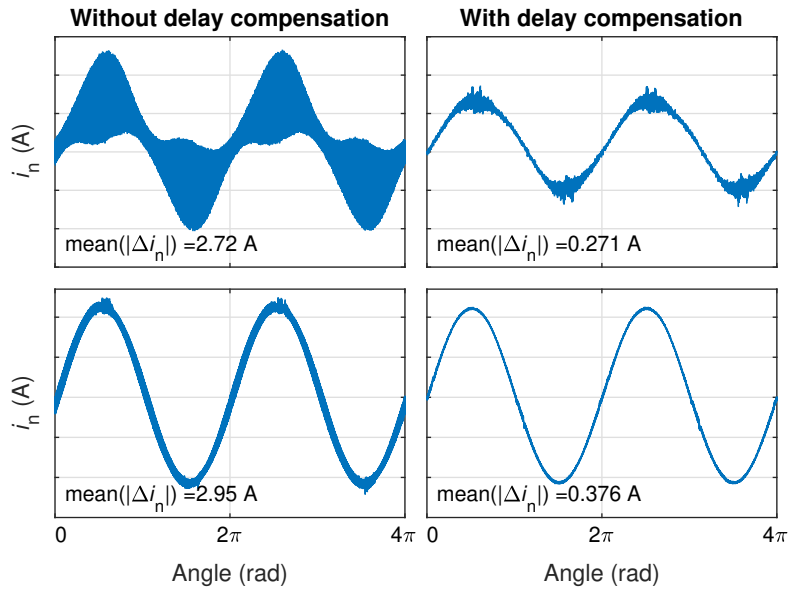


Figure 3.2. Current measurements taken from the converter control. No-load conditions are depicted in the top graphs, and the resistive load of 15.4 A in the bottom graphs. Δi_n is the difference between the two consecutive current samples.

3.1 Single-phase inverter control

A single-phase inverter in stand-alone operation has to be able to supply basic loads and off-line equipment with minimal electromagnetic interference. In order to minimize emissions, the output must be filtered with an EMI filter, which attenuates the switching frequencies from the output. Problems commonly arise when an EMI filter is added to the system, as the EMI filter adds dynamics to the high frequency range, which will degrade the performance and robustness and may even outright destabilize the inverter.

In the case of additional resonance in the system dynamics, the control design requires more attention. Next, a model of a stand-alone inverter including an EMI filter is derived and used for the design analysis of a cascaded PI control. The specific target is to highlight the importance of acknowledging the full dynamics of the controlled dynamics with an EMI filter included. This is an important issue as an EMI filter is almost always required in power electronic applications to meet the regulations.

Table 3.1. Experimental setup.

f_{out}	output frequency	50 Hz
f_{sw}	switching frequency	50 kHz
f_{ctrl}	control frequency	100 kHz
f_{s}	current sampling frequency	100 kHz
f_{AA}	AA cutoff frequency	70 kHz
t_{DT}	dead time	250 ns
t_{ADC}	AD conversion time	438 ns
u_{AC}	output voltage	230 V
u_{DC}	DC link voltage	365 V
L_1	primary inductance	410 µH
L_2	1st EMI filter inductance	2.4 µH
L_3	2nd EMI filter inductance	2.4 µH
C_{X1}	1st X-capacitance	9.1 µF
C_{X2}	2nd X-capacitance	2.2 µF
C_{X3}	3rd X-capacitance	9.3 µF
	current sensor	LTSR 15-NP LEM
	gate driver	Si8271DB-IS
	ADC	MAX11115
	FPGA	10CL010YU256I7G
	SiC Mosfet	C3M0065090D

3.1.1 Modeling of a single-phase inverter with an EMI filter

The differential-mode electrical circuit of the single-phase inverter including an EMI filter considered here is depicted in Figure 3.3. The modeled device is shown in Figure 3.4. The primary inductor L_1 is composed of two inductors with half of the inductance, and the additional inductors are the stray inductors of the common-mode filters. The converter state-space equations are formed using the circuit in Figure 3.3. The state vector is ordered to mirror the physical structure of the inverter and the EMI filter. The state vector is

$$\mathbf{x}(t) = \left[i_1(t), u_1(t), i_2(t), u_2(t), i_3(t), u_3(t) \right]^T, \tag{3.1}$$

where the state variables are the primary inductor L_1 current $i_1(t)$, the first x-capacitor C_1 voltage $u_1(t)$, the first stray inductor L_2 current $i_2(t)$, the second

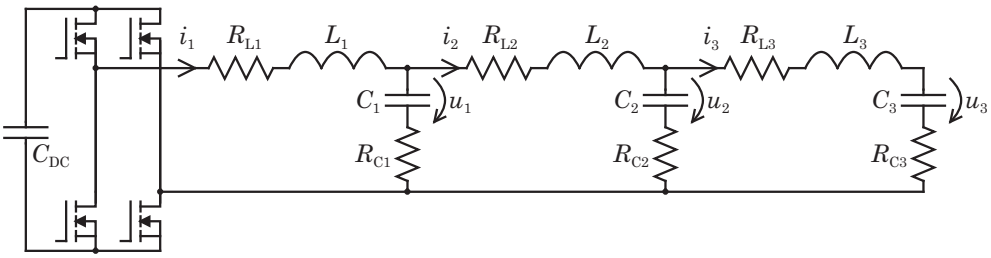


Figure 3.3. Simplified electrical model of a single-phase inverter with the EMI filter components included.

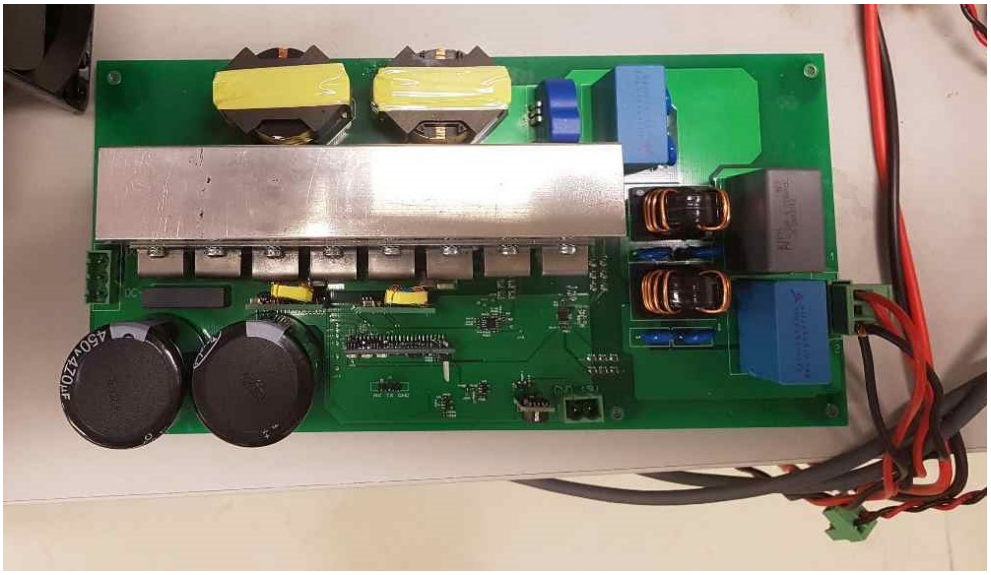


Figure 3.4. Single-phase inverter with the EMI filter and the FPGA control used for the experimental measurements.

x-capacitor C_2 voltage $u_2(t)$, the second stray inductor L_3 current $i_3(t)$, and the output capacitor C_3 voltage $u_3(t)$. The system is modeled using state-

space equations, and the matrices are

$$\mathbf{A} = \begin{bmatrix} -\frac{R_1}{L_1} & -\frac{1}{L_1} & \frac{R_{C_1}}{L_1} & 0 & 0 & 0 \\ -\frac{1}{C_1} & 0 & \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{R_{C_1}}{L_2} & \frac{1}{L_2} & -\frac{R_2}{L_2} & -\frac{1}{L_2} & \frac{R_{C_2}}{L_2} & 0 \\ 0 & 0 & -\frac{1}{C_2} & 0 & \frac{1}{C_2} & 0 \\ 0 & 0 & \frac{R_{C_3}}{L_3} & \frac{1}{L_3} & -\frac{R_3}{L_3} & -\frac{1}{L_3} \\ 0 & 0 & 0 & 0 & \frac{1}{C_3} & 0 \end{bmatrix}, \mathbf{B} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.2}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix}$$

where $R_1 = R_{L_1} + R_{C_1}$, $R_2 = R_{C_1} + R_{C_2} + R_{L_2}$, $R_3 = R_{C_2} + R_{C_3} + R_{L_3}$ are obtained from the resistances of the primary inductor R_{L_1}, the first and second stray inductor resistances R_{L_2} and R_{L_3}, the primary x-capacitor resistance R_{C_1}, and the first and second x-capacitor resistances R_{C_2} and R_{C_3}, respectively. The output matrix represents the measurements of the state model.

In order to obtain a mathematical model for control analysis, the impedance was measured from the system under study. The impedance measurement and the fitted model are shown in Figure 3.5. The estimated model parameters are shown in Table 3.1, and they were obtained by using the nominal values for the components and then tuning the parameters to match the model to the measured impedance.

When the output impedance of the system is measured, the input is the current injected to the output capacitor and the output is the voltage of the output capacitance. The corresponding input and output matrices are

$$\mathbf{B_Z} = \begin{bmatrix} 0 \\ \vdots \\ \frac{1}{C_3} \end{bmatrix}, \mathbf{C_Z} = [0 \dots 1], \tag{3.3}$$

where $\mathbf{B_Z}$ and $\mathbf{C_Z}$ are the input and output matrices for the modeled impedance.

The eigenvalues of the state matrix $\mathbf{A}$ correspond to the resonance frequencies of the system illustrated in Figure 3.5. The model is of the 6th order and has

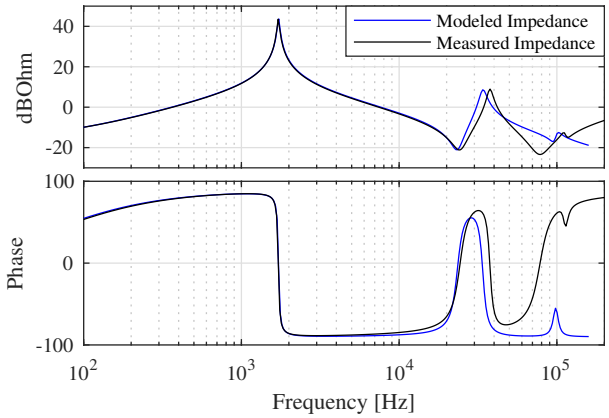


Figure 3.5. Fitted impedance model and impedance measurement.

two main resonances. The main peak, which is at the 1.8 kHz frequency, is caused by the LC resonance of the entire capacitor bank and the primary inductor L_1. The EMI filter resonant peaks are at 32 kHz and 100 kHz. In terms of control design, the low-frequency EMI filter peak is the one that causes instability, especially in a case where the inverter is loaded with a capacitive load as the resonance peak shifts to the control band.

3.1.2 Inverter feedback control

The inverter has a practical requirement of having an integrator in the voltage loop to guarantee zero mean voltage regardless of the loading condition. An integrator in the inner current loop is also a practical requirement, as the inverter has to be able to accurately limit the current to a set value in overload and short-circuit conditions. Because of these requirements, a cascaded PI controller with a PI control in both the voltage and current loops is chosen. Owing to the requirements of the short-circuit and overcurrent protection as given in the IEC standard 62040-3:2011, the current measurement is placed in series with the primary inductor L_1. The resulting closed-loop control is depicted in Figure 3.6 with only the feedback measurements of the system (3.1) shown. The delay block represents the total conversion delay of the measurement. The control is calculated on an FPGA, which is running at the 128 MHz clock frequency, and the total latency between measurements being

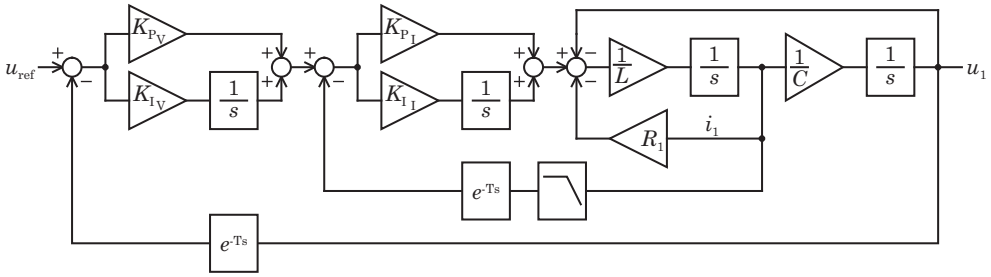


Figure 3.6. Control block diagram with the additional EMI filter states omitted. The control measurements are the first capacitor voltage u_1 and the primary inductor current i_1. The current loop includes an anti-aliasing filter. The delay block represents the sampling delay of the digital control system.

ready and the control completed in less than 100 ns.

When the inverter is loaded with a resistive load, the resistance adds damping to the dynamics, which tends to move the system towards more stable operation. Therefore, the resistive load is the least restrictive load to the inverter in terms of the stability of the control loop. However, a resistive load is usually considered for validation of any proposed control law (Komurcugil et al., 2015). In contrast, a capacitive load shifts the EMI filter resonance peaks to a lower frequency. When the resonances are shifted to lower frequencies, the overall control system tends to shift towards more unstable and oscillatory behavior. In terms of system stability, the capacitive load is the most critical, and therefore used for control analysis.

3.2 Control design

A cascade PI controller structure is considered. A traditional approach to tune a cascaded control structure is one loop at a time with the assumption that the current control decouples the voltage and current loops (Tzou and Jung, 1998). First, the inner current loop is designed to have as high crossover frequency as possible taking into account the switching frequency. Next, the outer voltage control loop is designed to also have as high bandwidth as possible limited by the desired gain and phase margins. Using these basic tuning guidelines for the cascade control design, the control loop is typically well

behaved and has a good load transient response (de Bosio et al., 2017).

The closed-loop control is analyzed with the tracking and sensitivity responses. The reference to the output tracking function $T(s)$ and the sensitivity function $S(s)$ can be expressed as

$$T(s) = \frac{U_1(s)}{U_{\text{ref}}(s)} \tag{3.4}$$

$$S(s) = 1 - T(s). \tag{3.5}$$

The peak value of the sensitivity function is used to analyze the robustness of the controlled inverter. The significance of the sensitivity function is that it guarantees robustness against any model uncertainty with a gain less than the robustness margin. The sensitivity peak value also guarantees the minimum gain G_m and phase P_m margins (Skogestad and Postlethwaite, 2005) given by

$$G_m \geq -20\log_{10}\left(1 - |S(j\omega)|_\infty^{-1}\right) \tag{3.6}$$

$$P_m \geq \quad 2\arcsin\left(\frac{|S(j\omega)|_\infty}{2}\right). \tag{3.7}$$

For instance, a sensitivity peak of 3 dB guarantees at least 10.6 dB of gain margin and 41° of phase margin. This sensitivity value is used as a limit for the control design.

Table 3.2. Parameters used for the analysis

Symbol	Quantity	Value
C_{load}	load capacitor	86µF
K_{P_v}	proportional gain (voltage)	0.3354
K_{I_v}	integrator gain (voltage)	1280
K_{P_i}	proportional gain (current)	12.65
K_{I_i}	integrator gain (current)	75000
f_{sw}	switching frequency	50 kHz
ω_c	anti-aliasing filter cutoff frequency	70 kHz
f_{ctrl}	control frequency	100 kHz

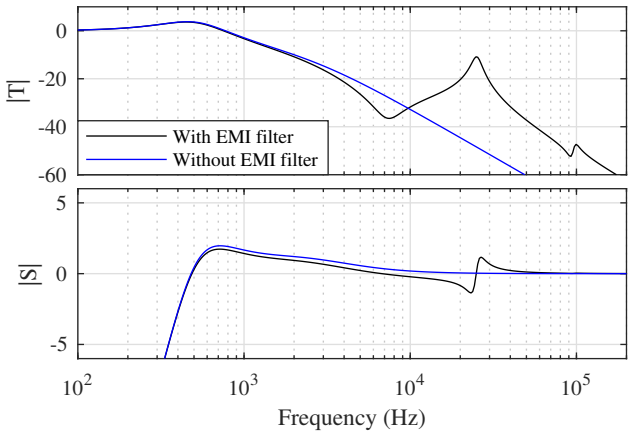


Figure 3.7. EMI filter effect on the tracking and sensitivity functions.

In order to address the influence of the EMI filter on the closed-loop dynamics, the system model shown in Figure 3.3 is studied with and without an EMI filter and considering the maximum capacitive load. The parameters of the EMI filter given in Table 3.1 and the control parameters given in Table 3.2 are considered in the example. The influence of the EMI filter is clearly noticeable in Figure 3.7 as an introduction of a resonance–antiresonance pair in the voltage frequency response. In the example case, the gain of the reference to the output loop can be seen to increase by 37 dB at the resonance, which significantly affects the system stability especially at high capacitive loads. As the maximum value of the sensitivity function gives the robustness margin for the entire system, the maximum value of the sensitivity function is limited by the control design.

It should be noted that the controller parameters used in the analysis presented in Figure 3.7 have been designed so that the control loop is well behaved under additional resonating dynamics.

3.2.1 Sensitivity of the cascaded PI control

To further analyze the influence of the EMI filter on the system dynamics, the influence of the controller parameter on the closed-loop performance is investigated. In the analysis, the anti-alias filter of the current control loop and

an additional delay of 5 µs associated with the analog-to-digital conversion (ADC) and the PWM update shown in Figure 3.6 are taken into account. In Figures 3.8–3.9, the sensitivity functions are shown when the voltage and current control parameters are varied. It can be seen that the effects of the different control gains are distributed over the controllable band.

The voltage control introduces the most significant effect on the system sensitivity at low frequencies. The system sensitivity with respect to variations in the proportional gain K_{P_v} of the voltage control loop is shown in Figure 3.8a and the integrator gain K_{I_v} in Figure 3.8b. For a high performance, the bandwidth should be as high as possible. The integrator can be seen to reduce the low-frequency sensitivity by increasing the sensitivity just above the bandwidth. The sensitivity peaking can be mitigated by increasing the proportional gain, which also increases the EMI filter resonance-induced peak. Therefore, it can be concluded that the EMI filter imposes a limit on how high a voltage control bandwidth can be achieved for a given maximum sensitivity peak. It should be noted that this is the case even if the EMI filter resonance is in the range of tens of kHz, and the bandwidth of the voltage control is in the range of hundreds of Hz.

The current control gains can be seen to have the strongest influence on the high-frequency band at the antiresonance frequency, which is seen in Figure 3.9a and b. Both the proportional gain K_{P_I} and the integral gain K_{I_I} increase the EMI filter resonance peak. The current control gains have an influence on the frequency band above the voltage loop bandwidth. Therefore, the current loop gains can be used to tune the high-frequency peak caused by the EMI filter. There is also a lower bound on the current gains imposed by the voltage loop. The current loop bandwidth has to be higher than the voltage loop for the system to remain stable.

3.2.2 Tuning of the cascaded control

The current loop bandwidth is practically limited by the PWM frequency and sampling (Ma et al., 2018). After the initial current loop design, the voltage loop is tuned so that the peak sensitivities between the voltage loop control and the EMI filter are balanced. The obtained voltage loop tracking and sensitivity functions are shown in Figure 3.10. With the initial cascade control

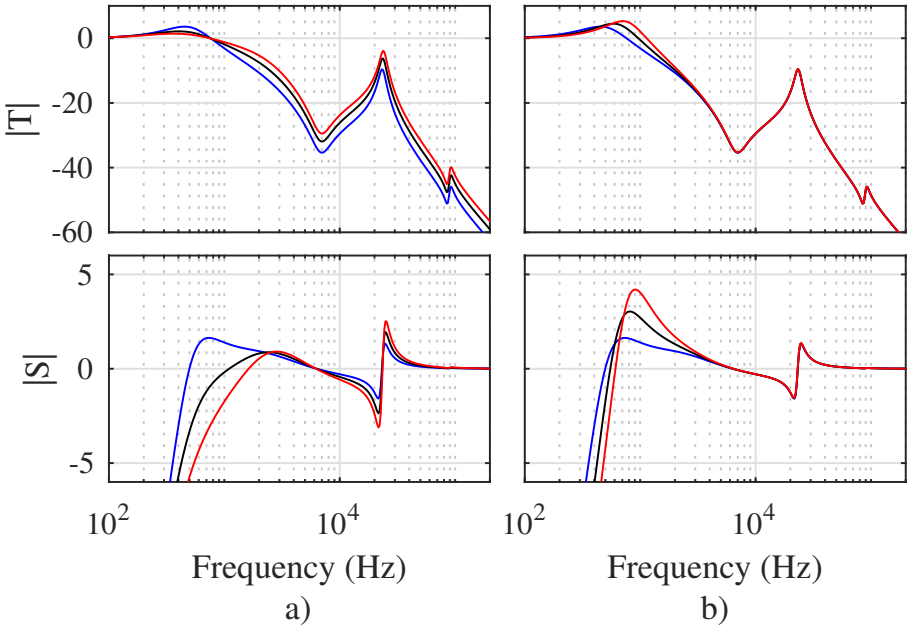


Figure 3.8. Voltage controller effects on the reference tracking and sensitivity of the inverter loaded with a capacitive load; the effects of increasing a) the proportional gain K_{P_v} and b) the integral gain K_{I_v}. The figures are plotted with initial gains shown in blue and with the 1.5x gain in black and the 2x gain in red.

design with one loop tuned at a time, the achieved sensitivity at the fundamental frequency of 50 Hz is -34 dB. The initial current loop design has a bandwidth of 8 kHz, while the voltage loop bandwidth is 270 Hz. The voltage loop bandwidth means that the control reduces the voltage distortion up to the 5th harmonic of the fundamental.

To further improve the voltage loop performance, as a final step, the full system with both control loops is tuned for the maximum voltage loop bandwidth. As the high-frequency sensitivity peak is influenced by the current controller, the voltage control bandwidth can be increased while reducing the current control gains. The control gains are tuned until the two sensitivity peaks are of equal magnitude, effectively trading the current controller gains for the voltage loop gain.

The final, fine-tuned voltage loop is shown in Figure 3.11 along with the measured tracking function. Because the sensitivity function response is not eas-

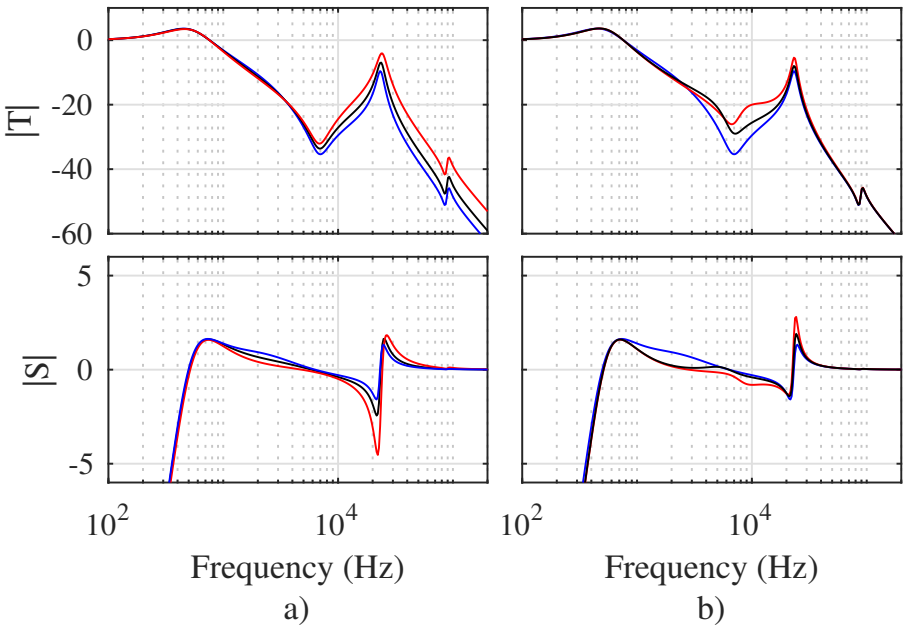


Figure 3.9. Effect of the current controller on the reference tracking and sensitivity of the inverter loaded with a capacitive load; the effects of increasing a) the proportional gain $K_{\mathrm{P_i}}$ and b) the integral gain $K_{\mathrm{I_i}}$. The figures are plotted with initial gains shown in blue and with the 1.5x gain in black and the 2x gain in red.

ily measurable from the hardware used in the study, the tracking function was measured and the sensitivity function was calculated by using (3.5) from the model after fitting the model response with the measurement. It can be noticed that the modeled response agrees very well with the measured one.

The initial and tuned responses are shown in Figure 3.10. The current loop bandwidth is lowered from the initial 8 kHz to 3.3 kHz, the bandwidth of the voltage loop gain is increased to 400 Hz, and the sensitivity at the fundamental 50 Hz frequency is lowered from -34 dB to -40 dB. Compared with the first step cascade control, the voltage loop bandwidth is thus increased by approximately 50%, and the sensitivity up to the 7 th harmonic is decreased by a factor of 2, or 6 dB.

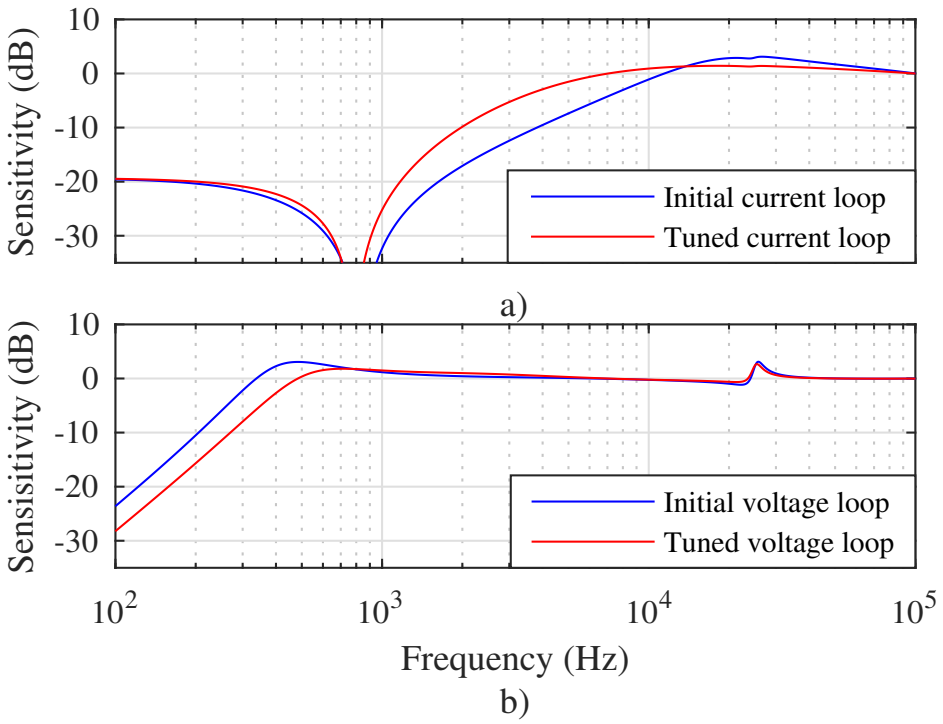


Figure 3.10. Tracking and sensitivity loop shapes with the initial and final-tuned PI controllers; a) for current control and b) voltage control.

3.3 Experimental measurements

To further verify the performance of the inverter by the AA-filtered measurements applying the designed sampling, the system was tested with dynamical loads. The first one is the resistive load step shown in Figure 3.12. The inverter is loaded with a 15.4 Ω resistor, which is connected to the output at the peak of the voltage waveform. With the dual sampling and optimized control, the transient recovers in around 500 µs.

A short-circuit and recovery are shown in Figure 3.13. The short-circuit is applied by using a 2 A C-type circuit breaker. The voltage control is designed to provide a maximum current reference of 25 A. The C-type breaker opens after a 2 ms short-circuit current, at which point the output voltage can be seen to rise as a result of arcing inside the circuit breaker. The arc is extinguished

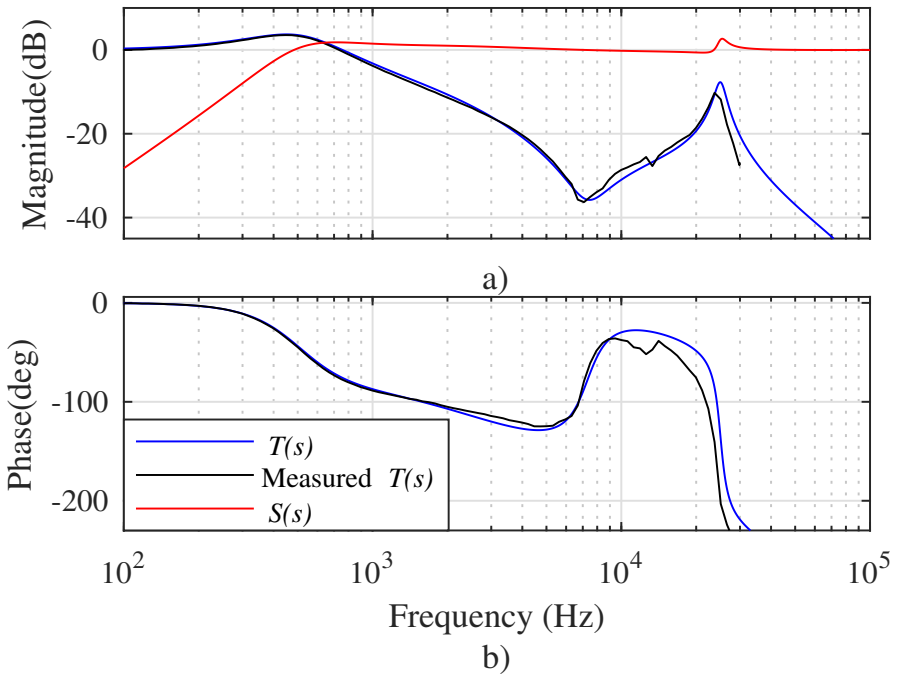


Figure 3.11. Tracking performance and sensitivity of the closed-loop system. The measurement is taken up to the Nyquist frequency of the 50 kHz PWM.

as the reference changes polarity, and the system resumes normal operation.

The inverter was also tested with a capacitive 86 µF load, which is shown in Figure 3.14. As a manually operated mechanical switch was used, the disconnect shows a transient at 100 ms caused by a bounce of the mechanical switch aperture. The system has a fast response, and the transient decays without significant oscillations. Because the load has a much lower impedance than the EMI filter output capacitor, the switching ripple is seen at the load capacitor current. The output current has a very high current spike at the moment of load connection, as the inrush current between the load capacitance and the EMI filter capacitance is only limited by the impedance of the connecting wires.

Figure 3.15 shows the system performance with a 1.6 kVA nonlinear load with a crest factor of 3.2. The load is a 3 kW DC/DC converter with the PFC turned off. The DC link capacitance of the load is 1.5 mF, and the load power is

chosen so that the 22 A saturation current of the main inductors of the inverter is not exceeded. The output voltage THD is 3.0% calculated from the 50 first harmonics when loaded with a nonlinear load.

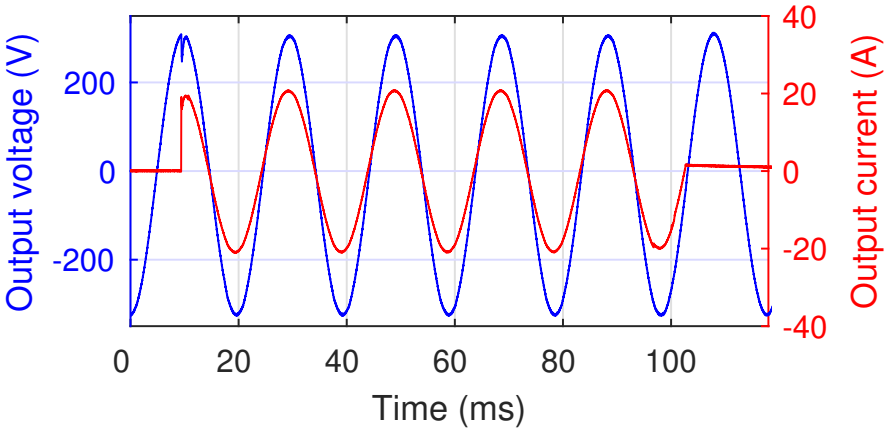


Figure 3.12. Test with a 3.5 kW resistive load step.

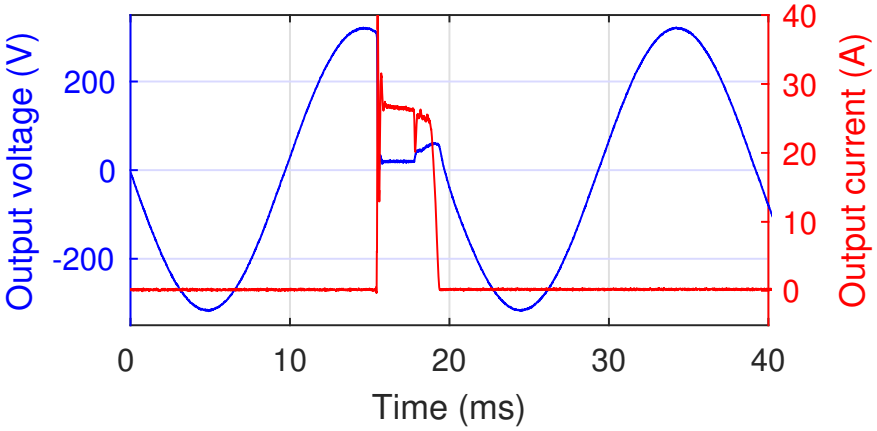


Figure 3.13. Short-circuit test. The short-circuit is applied using a 2 A C type circuit breaker. The rise in the voltage during the short-circuit is caused by arcing inside the circuit breaker.

3.3.1 Discussion on dual sampling and control

The main issues with the dual sampling and control are the calculation frequency and accurate timing of the sample to the center of the current wave-

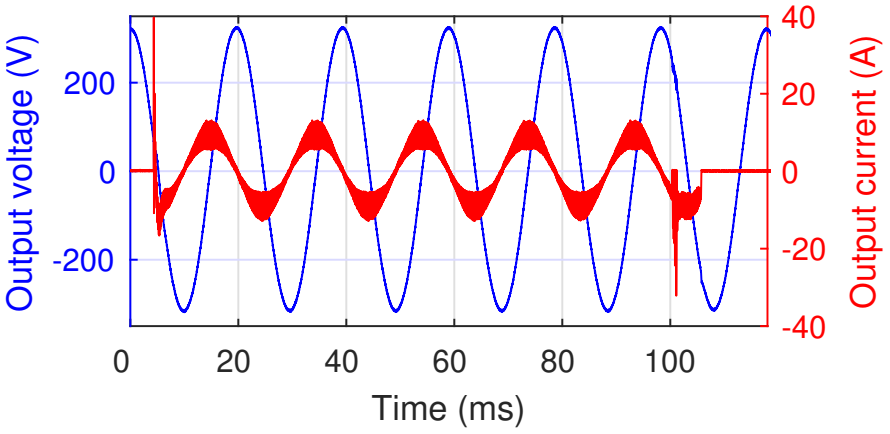


Figure 3.14. 1.5 kVA capacitive load step.

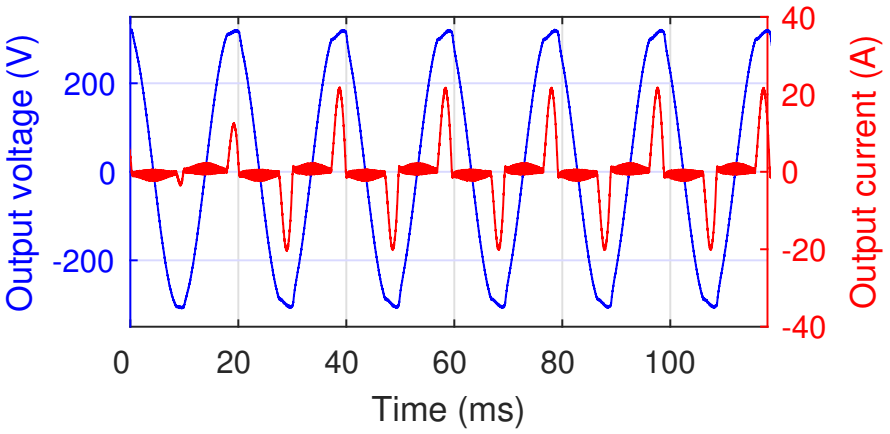


Figure 3.15. Inverter loaded with a 1.6 kVA nonlinear load. The nonlinear load is a 3 kW off-line power supply with the PFC turned off. The load power was chosen to yield a maximum peak current of 22 A.

form. The sampling issue can be solved with an anti-aliasing filter that is tuned higher than the switching frequency to minimize the phase delay of the filter. The filtering and measurement timing reduces the noise from the maximum of 2.72 A to 270 mA peak-to-peak noise with the inverter running without a load. When dual sampling and tuned measurement are used in the control design, noise is minimized in the measurement and control delay.

An EMI filter is included in the control design. Even though the effect of the

EMI filter is in the 20 KHz frequency range, the high-frequency EMI peaking has a profound effect on the control design. It is common knowledge that a well-behaved converter can be oscillatory or completely unstable when an EMI filter is added (Erickson and Maksimovic, 2001). Thus, the EMI filter is taken into account in the control design by completing the robust control design with the full system by balancing the sensitivity function peaks of the EMI-filtered system. This is shown to be achievable by tuning both control loops as a final step after the initial loop tuning is completed.

4 Conclusions and future research

Digital control is known to offer numerous opportunities for control design. The scientific publications discussed in this doctoral dissertation provide examples of simple extensions to basic power supply control systems that aim to significantly improve the performance, control stability, and robustness, and to simplify the control system design.

The use of a digital platform also allows the integration of multiple power supply controls into a single device. This can reduce the required hardware and also enables the use of multiple measurements from different parts of the power supply for control purposes. The DC link voltage feedforward can be used in subsequent power supplies to mitigate the effect of DC link voltage fluctuation.

The input voltage feedforward term in a current control loop of a boost power factor controller was shown to arise naturally from the use of the Lyapunov stability-based control. The added feedforward term can be simplified to a simple addition and multiplication term, and the difference between the accurate feedforward with division and the simplified version can be considered insignificant in terms of the attained performance boost. The resulting controller has a traditional PI control structure, but offers a significantly lowered sensitivity towards mains voltage variation by providing the input voltage waveform as a feedforward term directly to the PWM signal.

The benefits of the digital control were also extended to the PFC control by applying the fuzzy control theory. The performance of the DC link control was extended with a very simple gain scheduling, which was shown by experiments to allow great improvements in both the transient and steady-state performance. As of writing, the author has not seen any publication with a better performance, and even the most sophisticated controllers studied in the literature have as good performance at most, but with a significantly increased complexity. The fuzzy DC link control is very simple to understand,

and it is obvious why it performs so well. The controller further decouples, and thereby simplifies, the DC link control as the transient and steady-state performances can be tuned separately.

The programmability of the digital control also allows optimization of the measurement sampling. As the measurement bandwidth poses a limit on the controllable band, the optimization of the measurement and control delays provide more tools for the control designer to design the control loop. Even though the crossover frequency of the controlled loop gives the bandwidth, the robustness requires that the controllable range extends beyond the bandwidth of the closed loop. The robustness therefore benefits from a measurement bandwidth substantially larger than the closed-loop bandwidth. The optimization of the measurement band was tested and the minimization of the minimization of the effects of anti-alias filtering was discovered. The tests were performed using a single-phase inverter with dual-sampled and controlled current and voltage measurements. The control design was implemented in two parts where the inner current loop and the outer voltage loops were first tuned separately, and as a final step, the complete control design was fine tuned to provide maximum performance for the chosen robustness margins with the worst-case capacitive load. The measurement delay has an effect on the control design as a result of the interaction between the control loop delay and the main resonance frequency of the EMI filter.

4.1 Suggestions for future work

Because the measurement timing was adjusted manually to provide a minimum difference between the samples taken on the different sides of the current waveform, an obvious extension of this would be to use a feedback to minimize the difference. A topic of future study will also be to investigate how far the bandwidth can be extended with feedback-adjusted sampling and AA filter effect minimization. As the optimized sample timing and the minimized control delay extend the controllable band, the effect of the extended band on the robustness and performance of a single-phase inverter would be an interesting topic of study.

Wide band gap devices are available, and they have already been shown to

allow a significant increase in switching frequencies when compared with silicon devices. The full benefit of the GaN and SiC devices is also a subject of future research, for instance with the focus on the effects of the increased switching frequencies and the increased controllable bandwidth allowed by the emerging technologies. The effects of EMI filtering on the achievable control bandwidth are also under investigation. When the digital delays of the sampling and calculation are minimized, the effects of the EMI filter resonances are limiting the control performance; however, with the increased controllable band enabled by the wide band gap devices, the EMI filter resonances can be actively damped.

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Publication I

Honkanen, J., Hannonen, J., Silventoinen, P., and Räisänen, S.
Single phase PFC control with Lyapunov method

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17th European
Conference on Power Electronics and Applications EPE'15 ECCE-Europe
Geneva, Switzerland, pp. 1–5

Single phase PFC control with Lyapunov method

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Keywords

<<Control methods for electrical systems>>, <<Digital control>>, <<Power factor correction>>

Abstract

In this paper a current control method based on Lyapunov function for single phase active power factor correction (PFC) is presented. Lyapunov functions can be used for defining control law for either linear or nonlinear systems. The control is designed with cascade structure, where a voltage controller feeds the current amplitude reference to the current controller. The operation and performance are demonstrated with measurements from 3 kW power supply which uses power factor correction. The designed controller is shown to track the mains voltage with close to unity power factor.

Introduction

Mains fed power converters are used to transfer power between the mains and load. Power factor is a measure for quality of power drawn by the converter. Power factor takes into account the distortion and the reactive component of the grid current. Peak current and possibly the RMS current drawn from the mains increase as the power factor decreases. In order to limit reactive and harmonic current drawn from of the mains, regulations exist for lowest allowed power factor.

Power factor correction allows reactive and nonlinear loads to be sourced from mains voltage with minimal distortion to the mains. Typical arrangements for single phase active PFC are single switch boost, dual boost circuits in either parallel or bridgeless topology and a full bridge converter.

With PFC the power is controlled with feedback from mains current and voltage therefore a dedicated control circuitry is needed to drive the transistors. Linear methods for controlling PFC converter include PI control with mains voltage feedforward, admittance feedforward [1] and current feedforward [5].

Nonlinear control for the use of switch mode power supplies and PFC control has been studied [2] where the authors used Sontag's formula for designing an optimal nonlinear controller for PFC converter. The authors of [3] used the semisystematic method of backstepping, which produces the control along with a proper Lyapunov function. Designing a controller with Lyapunov functions allows significant flexibility to the designer as the system's and controller's dynamics can be either linear or nonlinear. This allows more accurate description of a nonlinear plant to be used in the control design. Also, any function that is a viable Lyapunov function can be used to prove stability which also provides a degree of freedom during the design. In this paper the control is designed for the current loop of the PFC using Lyapunov stability criterion to define the current controller. The controller is appended with a dynamic equation that allows for integral action for the error between reference and measurement in the current control loop.

PFC dynamics and control design

The boost converter dynamics can be represented with state-space as

$$L * \dot{i}_L = V_i + (d-1) * V_o, \tag{1}$$

$$C * \dot{V}_o = (1-d) i_L - \frac{V_o}{R} \tag{2}$$

where V_i is the input voltage, V_o is the output voltage, d is the duty ratio and i is the inductor current. It can be seen from (1) that the control signal d appears directly in equation of the controlled state.

From (1) it can be seen that the controlled variable is only dependent on the output and input voltages. The current dynamic is nonlinear as the applied input signal is dependent on the duty ratio as well as the output voltage which is influenced by the current. The DC link voltage also has fluctuation at twice of the mains voltage frequency because of the sinusoidal current shape. The output capacitance is designed to provide enough energy storage to limit voltage ripple to less than 10 % of the nominal value at full load.

Controller synthesis

Stability of a dynamical system can be proved with a Lyapunov method. Lyapunov method uses a function of the states, which is always positive and has a derivative that is always negative. Control design can be accomplished with Lyapunov function by choosing a control law that guarantees that the derivative of the chosen Lyapunov function is negative definite.

In order to provide a high gain for low frequencies, the system is augmented with an integral of the current. The system is to be controlled with state-feedback of the form $d = u(x, \omega)$ and ω is the dynamic part of the controller. The closed loop current dynamic equation with the controller is

$$\dot{x} = (u(x,\omega) - 1)\frac{V_o}{L} + \frac{V_i}{L} \tag{3}$$

$$\dot{\omega} = \beta(x,\omega), \tag{4}$$

where u is the new input. The control design is accomplished by choosing functions $u(x,\omega)$ and $\beta(x,\omega)$ such that system (3)-(4) is stable and provides integral action to the error between reference and measurement. To stabilize the system to a reference value, the Lyapunov function is defined with the error between state and set-point $z = x - x_{ref}$. The positive definite Lyapunov function is chosen as

$$V = \frac{1}{2}z^2 + \frac{1}{2}\omega^2 \tag{5}$$

and the corresponding Lyapunov function derivative is

$$\dot{V} = z(u(z,\omega) - 1)\frac{V_o}{L} + \frac{V_i}{L}z + \omega\beta(z,\omega). \tag{6}$$

The control signal $u(z,\omega)$ is augmented to compensate the effects of input and output voltages. The control signal is redefined as

$$u = 1 - \frac{V_i}{V_o} + \widetilde{u}(z,\omega), \tag{7}$$

where $\widetilde{u}(z,\omega)$ is the new control signal. Substituting (7) to (6) yields

$$\dot{V} = z\widetilde{u}(z,\omega)\frac{V_o}{L} + \omega\beta(z,\omega). \tag{8}$$

The control law guarantees stability whenever (8) is negative definite and any choise of the functions

$\widetilde{u}(z,\omega)$ and $\beta(z,\omega)$ that renders the equation (8) negative definite is a stabilizing control law. Since integral action is desired, the $\beta(z,\omega)$ is chosen as $-Kz$ where K is gain for the dynamic term. The control signal $\widetilde{u}(z,\omega)$ is used to compensate the dynamic part of the controller and is chosen as

$$\widetilde{u}(z,\omega) = -\frac{L}{V_o}K_1 z + \frac{L}{V_o}K\omega \tag{9}$$

$$\beta(z,\omega) = -Kz. \tag{10}$$

Substituting (9) and (10) to (8) yields

$$\dot{V} = -K_1 z^2 + Kz\omega - Kz\omega = -K_1 z^2, \tag{11}$$

which guarantees stability. The current controller for the original system (3)-(4) is obtained by combining (7), (9) and (10)

$$\begin{aligned} u(z,\omega) &= -\frac{L}{V_o}K_1 z + \frac{L}{V_o}K\omega + 1 - \frac{V_i}{V_o} \\ \dot{\omega} &= -Kz, \end{aligned} \tag{12}$$

where K and K_1 are the design values which are used to tune the systems dynamic behavior. Since they can be chosen arbitrarily and the constants L, V_o are known positive values, (12) can be reformulated so that $K_P = \frac{L}{V_o}K_1$ without loss of generality. This yields

$$\begin{aligned} u(z,\omega) &= -K_P z + \frac{L}{V_o}K\omega + 1 - \frac{V_i}{V_o} \\ \dot{\omega} &= -Kz. \end{aligned} \tag{13}$$

The gains of the dynamic part of the controller can be combined in the controller (13) to bring it to more compact form. This is achieved by defining

$$\widetilde{\omega} = \frac{L}{V_o}K\omega \tag{14}$$

$$\Rightarrow \dot{\widetilde{\omega}} = \frac{L}{V_o}K\dot{\omega} = \frac{L}{V_o}K(-Kz) = -\frac{L}{V_o}K^2 z. \tag{15}$$

The gain for the dynamic part is defined as $K_I = \frac{L}{V_o}K^2$ which brings the final controller to the form

$$\begin{aligned} u(z,\widetilde{\omega}) &= -K_P z + \widetilde{\omega} + 1 - \frac{V_i}{V_o} \\ \dot{\widetilde{\omega}} &= -K_I z, \end{aligned} \tag{16}$$

where K_P and K_I are arbitrary positive design values, z is the error between set point and measurement and $\widetilde{\omega}$ is the integral of the error. This forms a PI controller with added feedforward term.

Experimental results

The controlled system was presented in [4]. The PFC control algorithm is implemented with STM32F4 micro controller and a FPGA is used for PWM generation and AD-conversion timing. The control law defined in (16) has a division of output and input voltages. The use of division in the control algorithm was averted by using the reciprocal of the DC link voltage reference instead of the measurement. This also prevents measurement noise from corrupting the duty cycle generation. The use of the reference adds a low frequency error to the feedforward term, as the actual DC link voltage has load dependent steps and fluctuations. The used constant reference value works regardless because the DC link voltage dynamics are slow relative to the current loop dynamics. The integrator in the closed loop provides high

gain at low frequencies which decreases the effects of the DC link voltage dynamics.

The PFC is loaded with phase shifted full bridge buck converter that regulates the 400 V DC link to 24 V DC and up to 125 A current. The load steps are applied by changing the loading of the full bridge converter. The PFC has two parallel single switch boost converters that are 180 degrees out of phase and the individual boost converters are operated at 100 kHz switching frequency. Both of the boost converters have the same duty cycle command and therefore they are controlled as if there were only one boost.

The DC link voltage is controlled with PI control. The voltage controller was tuned to achieve stable operation during full load step. The gain of the voltage loop is a compromise between fast dynamics and input current quality. Increasing the gain of the 100 Hz component directly appears in the current loop reference and therefore increases the second harmonic in the mains current.

The current loop is executed at 50 kHz frequency. PFC currents are measured with current transformers and sampled synchronously. The sample is taken at the middle of the duty cycle, which allows average value to be measured directly [7]. The maximum duty cycle is limited to 0.8 to allow time for the current transformers to reset. The duty cycle limitation causes a cross over distortion in the current which is visible in Figure 2a). The voltage loop is executed at 5 kHz frequency.

The current controllers operation system is measured during load steps from 100 W to 3 kW and from full 3 kW load to 100 W load and constant operation at full load. Figure 1 shows the system's operation during load steps. Current waveform shows peaking during the first line cycle after load change as the DC link voltage drops lower than the peak mains voltage. This is because the dc link capacitor current is charged through the boost diodes. After the first line cycle the DC link voltage is high enough for the power factor correction to resume normal operation. Figure 2 shows the current waveform during full load operation and the corresponding control signal waveform. The control signal is saturated at 0.8 and the effect of the limited duty ratio can be seen in the zero crossing of the current waveform. The PFC current is designed to follow the mains voltage waveform, which is seen from the Figure 2a as the current follows the distorted mains voltage waveform.

Table I: System parameters for 3 kW single phase PFC converter

L	inductor	500 μH
C	DC link capacitor	1.5 mF
V_o	DC link reference	400 V
V_i	nominal input voltage	230 VAC

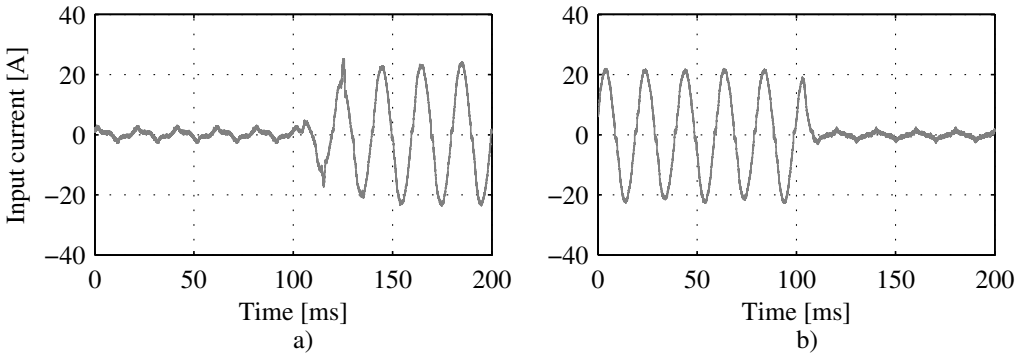

Figure 1: Figures (a) and (b) show the mains current during dynamic load change. In Figure (a) the load is changed from 100 W to 3 kW and in Figure (b) the load is changed from 3 kW to 100 W. The current spikes in Figure a) are caused by the capacitive charge spike that occurs when DC link voltage drops below the peak value of mains voltage

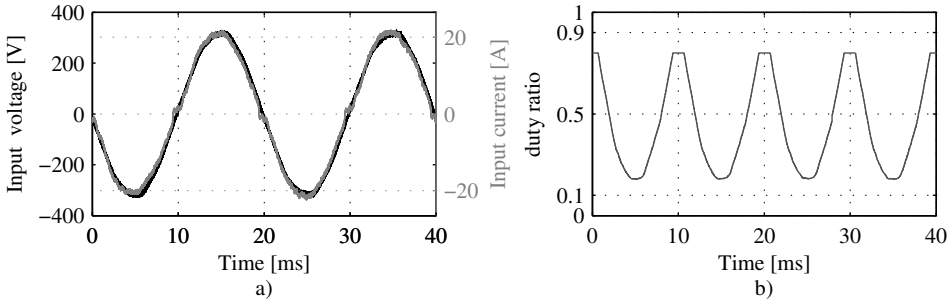

Figure 2: Figure a) shows mains current and voltage and Figure b) shows the duty ratio. The duty ratio and current measurements are taken with system operating at full load. Duty ratio is limited to 0.8 to ensure adequate time for the current transformers to reset and this causes the crossover distortion at the zero crossing which is seen in Figure a).

Conclusion

The Lyapunov theory can be effectively used to construct a controller for switch mode power supplies. Example case was presented where the control design was used to define an integrating controller for a single phase boost PFC converter. The controller was designed using Lyapunov stability criterion. The benefit of using the Lyapunov method is that the designer is left with a lot of freedom for the choice of control law. This is apparent from the equation (8) as any choice of functions $\widetilde{u}(z,\omega)$ and β that render the function negative definite can be used. In the presented PFC current control design the desired functionality was integral action for the error term and in addition to this the Lyapunov method brings about a feedforward term that improves the systems behavior.

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Publication II

Honkanen, J., Hannonen, J., Korhonen, J., Nevaranta, N., and Silventoinen, P.
Nonlinear PI-control approach for improving the DC link voltage control performance of a power factor corrected system

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IEEE Transactions on Industrial Electronics
Vol. 66, Iss. 7, July 2019, pp. 5456–5465.

Nonlinear PI-Control Approach for Improving the DC-Link Voltage Control Performance of a Power-Factor-Corrected System

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***Abstract*—When fast voltage control is used in a power factor control, the ripple of the dc link causes current harmonics. This paper proposes a method to reduce the harmonic content of a fast voltage loop in a power factor correction, which can both produce low distortion during steady-state operation and fast recovery from a load transient. The performance is achieved by using a Takagi–Sugeno-type nonlinear controller for dc-link voltage control. The proposed nonlinear control is compared with linear proportional–integral (PI) control, which is tuned to meet the standardized regulations for the harmonic content in a 3-kW single phase power supply. The results show that the presented nonlinear voltage controller can maintain the dynamic performance of the linear control with reduced current harmonics. It is also shown that the used nonlinear control method requires only marginally more complex control algorithm compared to commonly used linear PI control.**

***Index Terms*—AC–DC power converters, digital control, fuzzy control, voltage control.**

NOMENCLATURE

A_i	State transition matrix in the T–S model.
C	DC-link capacitance.
$e\,(t)$	Error between dc-link voltage and reference.
i_1, i_2	Inductor 1 and 2 current measurement.
$i\,(t)$	DC-link input current.
K_i	ith state-feedback gain vector.
K_I	Integral gain in the PDC.
K_{I_1}	Integral gain in slow PI control.
K_{I_2}	Integral gain in fast PI control.
K_P	Proportional gain in the PDC.
K_{P_1}	Proportional gain in slow PI control.
K_{P_2}	Proportional gain in fast PI control.
$L_{1,2}$	Primary inductances of the boost converter.
LMI	Linear matrix inequality.
m_1	Error level for low-gain PI control.
m_2	Error level for high-gain PI control.
M_i	Membership function i of nonlinear controller.
P	Common positive-definite matrix.
PDC	Parallel distributed compensator.
PFC	Power factor correction.
PI	Proportional integrating (control).
r	Number of weighting functions.
R	Load resistance.
T–S	Takagi–Sugeno (model).
u_{DC}	DC-link voltage measurement.
u_{AC}	Rectified ac input voltage measurement.
u_{ref}	DC-link voltage reference.
$V\,(x\,(t))$	Lyapunov function.
$x\,(t)$	State vector of a state-space model.
$z\,(t)$	Weighting variable in a weighting function.
$\omega\,(t)$	Integrator state in the PI controller.

Manuscript received January 19, 2018; revised April 29, 2018 and June 29, 2018; accepted August 14, 2018. Date of publication September 10, 2018; date of current version February 28, 2019. *(Corresponding author: Jari Honkanen.)*

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Digital Object Identifier 10.1109/TIE.2018.2868282

I. INTRODUCTION

THE power factor is essentially a measure related to the quality of currents in ac power lines. Having a low power factor indicates inefficient utilization of electrical power as a result of the increased current stress with the given power level. In particular, the power factor is reduced when the load is either reactive or nonlinear, as is common when diode rectifiers are used. In general, the inherent drawback related to the nonlinear loads is the increased peak load current, as well as the increased harmonic distortion of currents in the mains. The harmonic currents can degrade the mains voltage quality and, therefore, interfere with other equipment connected to the same main power supply. In order to limit the interference in the mains voltage, there are standards such as IEC-61000-3-2 [1], where limits for the maximum allowed harmonic content of grid currents are defined. As a result, the effects of the low power factor have to be corrected in most of the applications.

In single-phase systems, PFC is most commonly achieved with a boost converter. In some cases, Cúk, flyback, and single-ended primary-inductor converters are also used to provide the PFC function [2]–[4]. With wide-bandgap devices, a totem-pole converter can also be effectively used for PFC [5]. When the

power is significantly higher, for instance, in industrial three-phase systems, a bridge configuration is common, and in these applications, the PFC is commonly referred to as an active front end or active rectifier. Bridge configurations are also used when the direction of the power has to be reversed, for example, in motor inverter applications.

The PFC converter is operated in either a discontinuous current mode (DCM) or a continuous current mode (CCM). The current mode operation of the converter describes whether the switching current decreases to zero during the switch cycle. The DCM operation is typically applied in low-power and low-cost systems, as it can be used without current measurement, thereby resulting in a significantly simpler control circuitry. However, the DCM operation has a limited power range because of the high peak currents, and therefore, the maximum power range within which power supplies are typically designed to operate in the DCM is about 150–300 W. Systems designed to operate in the CCM may operate in the DCM at low power, and this increases the total harmonic distortion (THD) of the current. In order to circumvent the increase of current distortion, Kim *et al.* [6] propose a modulated carrier control to improve the current shape when systems goes into the DCM allowing for an improved power factor in low-power operation.

The standard method for controlling the current and dc-link voltage is to use PI controllers for both the voltage and current control loops. When the PFC is working as intended, the current waveform follows the grid voltage feeding full-wave-rectified sine current to the dc link. This is common to all single-phase PFC converters regardless of the actual topology. The PFC can be used for reducing the effects of harmonic currents of nonlinear loads from the mains, as was done in [7].

The input current control has been actively studied, and several methods have been proposed in the literature. In [8], Louganski and Lai used an input voltage feedforward with a tuned phase lead circuit to improve the current waveform of the PI-controlled current loop. Nonlinear optimal control of the PFC current has been studied, for example, in [9], where the authors designed an optimal control based on Sontag's method. In [10], Rao *et al.* compared PI, notch filter, and nonlinear current control methods. In [11], Marcos-Pastor *et al.* used digital sliding-mode control for the current loop. In all current loop control designs, the goal is to have the measured current closely follow the reference current waveform, which then can act as a control variable to the voltage loop.

Since the voltage control loop directly controls the peak current drawn from the mains, the dc-link ripple is also introduced to the mains current waveform. This causes distortion in the reference of the current control and thereby ripple in the grid current. In order to limit the distortion, the voltage controller has to have limited gain in the frequency range of the dc-link ripple. The maximum achievable gain of the dc-link voltage under PI control with the given harmonic current levels has been studied in [12]. With the interaction of the dc-link ripple and the grid current, the main tradeoff in the voltage loop control design is balancing the allowable current distortion and the voltage loop dynamics.

Broadly speaking, the methods to increase the voltage dynamics can be categorized into two main groups. The dc-link voltage ripple is filtered out or canceled by the estimation of the ripple, or the control parameter is chosen in a way not to include the dc-link ripple. The dc-link ripple estimation filtering is studied in [13] and [14]. The authors used an additional analog circuitry to accurately estimate and cancel the dc-link ripple from the voltage control loop, thus allowing higher gains for the control. The method provides fast recovery in about three mains cycles from load transient, but requires significant signal processing to obtain an accurate estimate of the ripple. In [15], Chiang *et al.* estimated the ripple, but the required signal processing was done with using a phase-locked loop and a digital controller. With the ripple estimation, the converter was able to stabilize in about two mains cycles.

In [16], the voltage loop was studied under a control based on a discrete energy function. The idea of the energy function method is to measure the peak power of the load and then use this information to determine a feedforward term to improve the response of the voltage control loop to load changes. The discrete energy function approach was shown to recover approximately within two mains cycles. A nonlinear controller based on a discrete energy Lyapunov function was designed in [17]. The controller in question is a nonlinear state-space controller and regulates both the voltage and the sinusoidal current. The control system manages to stabilize the control loop in two to three main cycles. In addition, in [18] and [19], a fuzzy logic has been studied for the voltage loop control. Lu *et al.* [20] used an extended state observer to estimate the load current of a three-phase rectifier. The load current estimate is used in place of load current measurement feedforward to improve the regulation of the dc link during load transient.

This paper presents a nonlinear PI-control method for voltage control in a PFC system, which can provide a fast step response and low current loop distortion. Compared with foregoing papers [9], [12], [13], [16], [17], the proposed approach has several advantages; the approach is simple to tune as the tuning procedure is similar as in a standard linear PI controller, while the overall controller complexity is kept to a minimum. With the proposed control, the obtained load transient dynamics are at least as good as can be obtained by the "best" linear control [12] or nonlinear control with more complex structure, such as used in [17]. Finally, a major improvement in the harmonic performance is obtained by control gain scheduling. The nonlinear control allows the dc-link voltage loop to be designed to recover from a load step in approximately two mains cycles, while still performing within the harmonic current standards. The nonlinear control system is implemented using a PI controller with variable control gains, which depend on the error between the measured dc-link voltage and the dc-link reference. This allows us to speed up the dc-link dynamics when the system voltage error is higher than the dc-link voltage ripple, but the gain for the dc-link ripple is low at a constant load. The presented controller performance is shown experimentally, and a simple tuning method is provided. The controller is implemented with digital hardware and shown to be only marginally more complicated when compared with a PI control.

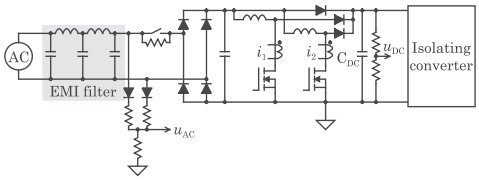

Fig. 1. Structure of the parallel boost PFC. The PFC has two identical boost converters in parallel, and the boost switches are controlled with switchings 180° out of phase. This effectively doubles the apparent switching frequency and reduces the switching ripple from the input current.

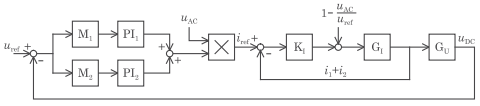

Fig. 2. Controller structure of the nonlinear controller. The scaling functions M_1 and M_2 are used to weigh the output of slow and fast controllers. G_I and G_U describe the current loop and voltage loop dynamics, respectively.

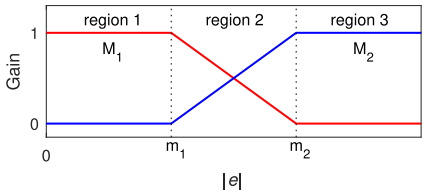

Fig. 3. Interpolating functions M_1 and M_2. The absolute value of the error is used, as the interpolating functions are symmetric about the origin.

The experimental setup used for this study has an interleaved boost circuit providing the PFC operation. The main circuit of the applied PFC is presented in Fig. 1. The control system measures the mains voltage u_{AC}, the dc-link voltage u_{DC}, and the switch currents i_1 and i_2. The controller uses the mains voltage for current reference generation and feedforward control of the current loop. The dc-link voltage is used as a feedback for the voltage control. The objective of the entire PFC system is to shape the grid current to follow the grid voltage waveform and to keep the dc-link voltage at 405 V.

The rest of this paper is organized as follows. Section II discusses the problem statement and introduces the nonlinear controller. Then, Section III discusses the calculation burden and effective implementation of the proposed controller. Finally, in Section IV, the performance of the nonlinear control is experimentally evaluated and compared with a linear PI controller.

II. Problem Statement

The voltage control loop in a PFC system provides the current reference for the current control. The inner current controller is needed for the current to track the mains voltage waveform. In practice, the inner loop has a significantly higher bandwidth than the mains frequency, and therefore, the cascaded current and voltage control loops can be designed separately. In this paper, only the outer voltage loop is considered. This paper addresses issues in the voltage control loop design of a PFC system, and particular attention is paid to reduce the harmonic content and improve the dynamic performance. It is emphasized that, owing to specific design aspects of the voltage loop performance and the fact that the control loop can be designed separately, this paper focuses exclusively on the voltage control loop design. In practice, for the current control loop, any conventional current controller that can be used with a PI-controlled voltage loop works with the nonlinear voltage controller. The chosen design method for the nonlinear PI voltage controller is studied in state-feedback representation, and the method is based on a T–S-type nonlinear model. The control structure is depicted in Fig. 2. The T–S-type nonlinear model consists of linear submodels, and the output is a weighted sum of the linear models. A controller that has a parallel structure and weighting functions is referred to as a PDC. The PDC is commonly given in a state-feedback form

$$u = \sum_{i=1}^{r} M_i K_i x(t), \quad i = 1, 2, 3 \ldots r \tag{1}$$

where r is the number of weighting functions, M_i are the weighting functions used to calculate the output, and K_i are the corresponding control gains. In the fuzzy control literature, the weighting functions are traditionally called membership functions.

Fig. 3 shows the interpolating functions, where m_1 and m_2 are the boundaries of the different operating regions of the controller. When the error is in region 1, the system uses the low-bandwidth controller to ensure low distortion, and correspondingly, when the error is in region 3, high gains are used to provide fast convergence from the load disturbance. When the error is in region 2, the control signal is a weighted sum of the high and low gains.

The most important behavior of the gains is observed when the error is in region 2. In this case, the control signal is a weighted sum of the high- and low-gain PI outputs with the weight depending on the error size. The weighting in region 2 allows smooth transition from low to high gains, which eliminates discontinuity in the control signal that would otherwise occur in the boundary if gains were abruptly increased. The basic idea of the nonlinear PDC with the resulting gain of the controller is shown in Fig. 4, where the dashed lines represent the linear gains and the solid line the nonlinear gain. Note that the proportional and integral gain functions of the controller have the same overall shape as both the proportional and integral parts are scheduled with the same scaling functions M_1 and M_2.

In this paper, the width of the regions of the different gains is designed so that with the full load, the dc-link voltage ripple can fit in region 1, which means that the ripple amplitude is less than the chosen voltage level m_1. This ensures that in the steady state, the system has linear gains, and thus, the controller

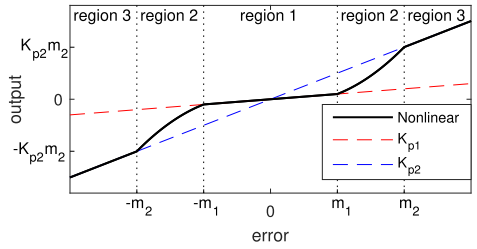

Fig. 4. Linear and nonlinear gains of the controller. The nonlinear gain is indicated by the solid line, and the linear gains are presented with the dashed lines, where red represents low gain and blue high gain.

nonlinearity does not produce extra harmonics to the current. The size of region 2 was experimentally chosen to be the same as the ripple voltage amplitude.

A. Controller Stability

Stability of a system comprised of several subsystems can be proved if a common positive-definite matrix P, which is a solution to the Lyapunov inequality (2), can be found. When the system is described with more than one linear model, i.e., $r > 1$ in (1), the Lyapunov inequality can be written in the form

$$A_i^T P + P A_i < 0, \quad i = 1, 2 \ldots r \tag{2}$$

where A_i are the state matrices for all subsystems. Then, the matrix P forms a quadratic Lyapunov function

$$V(x(t)) = x(t)^T P x(t). \tag{3}$$

Stability can be guaranteed if a common P can be found that fulfills (2) for all i. The benefit of the T–S-type control over direct Lyapunov-function-based designs is that the common positive matrix P can be found straightforwardly using numerical solvers [21]. The numerical solution of (2) is accomplished with LMIs. Since many control optimization problems in control design can be represented in the LMI framework, the PDC controller can be used as optimization and automation of the nonlinear control design. For example, robustness or performance limits can be designed as additional restrictions. These can be designed into the system with robust control methods based on the H_∞ theory [22]. In this paper, the following weighting functions and control gains are considered:

$$M_1 = \frac{m_2 - z(t)}{m_2 - m_1}, \quad M_2 = \frac{z(t) - m_1}{m_2 - m_1} \tag{4}$$

$$K_1 = [K_{P_1}, K_{I_1}], \quad K_2 = [K_{P_2}, K_{I_2}] \tag{5}$$

where $z(t)$ is chosen as the absolute value of the error between the measurement and the reference, and m_1 and m_2 are the voltage limits for error values that are used to weight the controllers. The closed-loop state matrices and common P, which proves stability, are given in the Appendix. Note that the continuous-time versions of the equations are used for the stability analysis of the voltage loop, due to the fact that the control frequency (see Table I) is several decades faster than the bandwidth of the voltage controller. Thus, the effects of the sampling and calculation become insignificant.

TABLE I
CONVERTER PARAMETERS

Symbol	Quantity	Value
$L_{1\&2}$	boost inductors	500 µH
C	DC link capacitance	1500 µF
K_{P_1}	Proportional gain (slow)	0.3919
K_{I_1}	Integrator gain (slow)	34.0741
K_{P_2}	Proportional gain (fast)	0.7837
K_{I_2}	Integrator gain (fast)	68.1481
f_{ctrl}	control calculation frequency	5 kHz

III. NONLINEAR VOLTAGE CONTROL IMPLEMENTATION

The voltage loop bandwidth of the PFC is limited to be less than the mains frequency, and the current is controlled with a high-bandwidth controller relative to the voltage. Since the current is controlled with the inner loop as seen in Fig. 2, the controlled parameter is the input current. The control model for the dc-link voltage is then made with the current as input and the dc-link voltage as output. The model is

$$C \cdot \dot{u}_{\mathrm{DC}}(t) = i(t) - \frac{u_{\mathrm{DC}}(t)}{R} \tag{6}$$

where u_{DC} is the controlled dc-link voltage, C is the dc-link capacitance, $i(t)$ is the controlled current, and R models the load as a resistance. As the control object is to regulate the error between the measured dc-link voltage and reference to zero, the system is represented with controlled state being the error between the dc-link voltage $u_{\mathrm{DC}}(t)$ and reference u_{ref}

$$e(t) = u_{\mathrm{DC}}(t) - u_{\mathrm{ref}}. \tag{7}$$

The dc link is modeled with error as the state and controlled current as the input. The control model can then be written as

$$\dot{e}(t) = \frac{1}{C} \cdot \left(i(t) - \frac{e(t)}{R} \right). \tag{8}$$

Since the system is to be controlled with integrating controller, the model is augmented with the integrator state, which is represented by ω. Using a standard PI controller

$$i(t) = -K_P e(t) + \omega(t) \tag{9}$$

$$\dot{\omega}(t) = -K_I e(t) \tag{10}$$

and combining (8)–(10), PI-controlled dc-link dynamic in a state-space form is obtained as

$$\dot{e}(t) = e(t) \cdot \left(-\frac{K_P}{C} - \frac{1}{RC} \right) + \frac{1}{C}\omega(t) \tag{11}$$

$$\dot{\omega}(t) = -K_I e(t). \tag{12}$$

With the defined form (11), (12), the voltage loop control can be, in practice, tuned using any well-established control design methods like pole placement possibly with optimization and analyzed with bode diagrams.

When the PDC controller (1) is used, the PI controller (9), (10) is replaced with

$$u(t) = e(t) \cdot (M_1 K_{P_1} + M_2 K_{P_2}) + \omega(t) \tag{13}$$

$$\dot{\omega}(t) = e(t) \cdot (M_1 K_{I_1} + M_2 K_{I_2}) . \tag{14}$$

The interpolating functions M_1 and M_2 determines the control behavior so that when the error is less than m_1 or more than m_2, only a single PI controller is used. Therefore, the controller implementation differs from the traditional PI control only in the region where the gains are interpolated.

In order to make the implementation to more convenient form, the controller (13), (14) is brought to simpler form. As stated above, in the case of the PI-controlled dc-link voltage, the measured signal $z(t)$ is the absolute value of error $|e(t)|$ between the measured dc-link voltage and reference, and m_i are the voltage levels, which are used to schedule the gains of the controllers. Substituting (4) into (13) and (14) yields

$$u(t) = e(t) \cdot \left((m_2 - |e(t)|) \frac{K_{P_1}}{m_2 - m_1} + (|e(t)| - m_1) \frac{K_{P_2}}{m_2 - m_1} \right) + \omega \tag{15}$$

$$\dot{\omega} = e(t) \cdot \left((m_2 - |e(t)|) \frac{K_{I_1}}{m_2 - m_1} + (|e(t)| - m_1) \frac{K_{I_2}}{m_2 - m_1} \right) . \tag{16}$$

By rearranging the terms (15), (16), the following form for the controller is obtained:

$$u(t) = \frac{K_{P_1} m_2}{m_2 - m_1} e(t) - \frac{K_{P_2} m_1}{m_2 - m_1} e(t) + \left(\frac{K_{P_2}}{m_2 - m_1} - \frac{K_{P_1}}{m_2 - m_1} \right) e(t) \, |e(t)| + \omega \tag{17}$$

$$\dot{\omega} = \frac{K_{I_1} m_2 e(t)}{m_2 - m_1} - \frac{K_{I_2} m_1 e(t)}{m_2 - m_1} + \left(\frac{K_{I_2}}{m_2 - m_1} - \frac{K_{I_1}}{m_2 - m_1} \right) e(t) \, |e(t)| . \tag{18}$$

Defining the constants in (17) and (18) as

$$K_p = (pK_{P_1} m_2 - pK_{P_2} m_1) \tag{19}$$

$$K_i = (pK_{I_1} m_2 - pK_{I_2} m_1) \tag{20}$$

$$K_{p^2} = (pK_{P_2} - pK_{P_1}) \tag{21}$$

$$K_{i^2} = (pK_{I_2} - pK_{I_1}) \tag{22}$$

$$p = \frac{1}{m_2 - m_1} \tag{23}$$

the controller (17), (18) can then be simplified to

$$u(t) = e(t) \cdot K_p + e(t) \cdot |e(t)| \cdot K_{p^2} + \omega(t) \tag{24}$$

$$\dot{\omega}(t) = e(t) \cdot K_i + e(t) \cdot |e(t)| \cdot K_{i^2} . \tag{25}$$

Note that the small subscript terms now denote gain terms of the nonlinear controller.

The full nonlinear PI controller is achieved by scheduling the gains with the error term

$$\begin{aligned} &\text{if } |e(t)| < m_1 \\ &\qquad u(t) = e(t) \cdot K_{P_1} + \omega \\ &\qquad \dot{\omega} = e(t) \cdot K_{I_1} \\ &\text{else if } |e(t)| > m_2 \\ &\qquad u(t) = e(t) \cdot K_{P_2} + \omega \\ &\qquad \dot{\omega} = e(t) \cdot K_{I_2} \\ &\qquad \text{else} \\ &\qquad u(t) = e(t) \cdot \left(K_p + |e(t)| \cdot K_{p^2} \right) + \omega(t) \\ &\qquad \dot{\omega}(t) = e(t) \cdot (K_i + |e(t)| \cdot K_{i^2}) . \end{aligned} \tag{26}$$

It is important to note that the implementation of the full controller increases the complexity of the standard PI controller only by a maximum of two comparison operations, two multiplications, two sums, and an absolute value calculation.

A. Controller Tuning

Since the nonlinear controller is composed of two PI controllers and the voltage regions, the authors suggest the following control design method with the following design steps for the presented high-performance PFC voltage control.

1) Tune a standard PI controller for desired dc-link voltage dynamics. The tuned gains are the fast gains K_{P_2} and K_{I_2}.
2) The steady-state gains K_{P_1} and K_{I_1} are then scaled down with a factor of 2 from the first set of gains.
3) The voltage range for the low gains m_1 is set to match half of the peak-to-peak ripple amplitude of the dc-link voltage at full load.
4) High-gain voltage level m_2 is set to $2 \cdot m_1$.
5) The full controller from (26) is used with the gains calculated from (19)–(23).

Using these definitions, the proposed nonlinear controller has the exact same tuning method that is used with standard PI control of the dc-link voltage with an improved steady-state performance. Therefore, the presented controller can directly replacing the existing PI controller and improve the steady-state performance, while maintaining the dynamic performance.

The dc-link ripple, which is used for the voltage levels where gains are scheduled, can be either measured with the tuned fast PI controller or calculated from a simple relation between the input power and the dc-link capacitor size [23].

IV. Experimental Results

The system performance is validated by experimental tests using a digitally controlled ac–dc converter prototype shown in Fig. 5. The main components of the system are inductor coils, current transformers, a dc-link capacitor, an electromagnetic interference (EMI) filter, and a digital control board. The converter input stage consists of a diode rectifier and a parallel

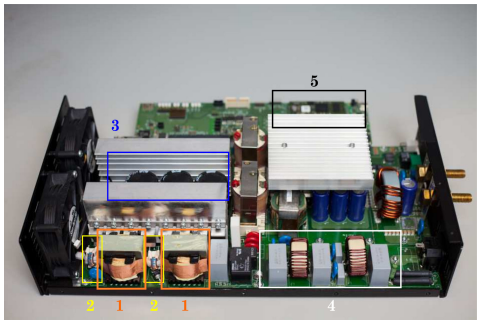

Fig. 5. Power supply used for the experimental measurements. The inductors (1) in the lower left corner are the boost inductors, and the toroidal coils (2) in the lower right corner are the common-mode EMI filter inductors. The current transformers that are used for the switch current measurement are also visible between the PFC inductors.

TABLE II
CONTROLLER COMPARISON

Input current THD with PI control	12.36 %
Input current THD with proposed Nonlinear control	6.13 %
PI settling time of load step from 150 W to 2.4 kW	32 ms
Nonlinear settling time of load step from 150 W to 2.4 kW	32 ms
PI settling time of load step from 2.4 kW to 150 W	50 ms
Nonlinear settling time of load step from 2.4 kW to 150 W	50 ms

boost stage for the PFC operation. The PFC is loaded with a 3-kW 24-V/125-A phase-shifted full-bridge converter. The converter is controlled using the XynergyXS digital control board. The board has an STM32F407 floating point microcontroller and Xilinx Spartan-6 FPGA, which is used for system timing and modulation. The load steps are applied to the full-bridge converter that loads the PFC converter. Since the full-bridge converter has a significantly faster settling time than the dc-link voltage, the converter is effectively a constant power load to the dc link. The PFC converter parameters are given in Table II.

In the experimental tests, the input current and the dc-link voltage are measured using an Agilent DSO 6104A oscilloscope. A Tektronix PS5210 differential voltage probe is used for voltage measurements, and Agilent Technologies N2781A 150-A/10-MHz current probes are used for current measurements.

The system dynamic operation is tested by applying a 150-W-to-2.4-kW and 2.4-kW-to-150-W load steps. Fig. 6(a) and (b) shows the dc-link voltage and input current dynamics using linear and nonlinear controllers during the load transient from 150 W to 2.4 kW. It is noted that the nonlinear gain is used when the error is more than 7.8 V from the set value of 405 V, and the voltages on the Y-axis represent the gain regions of the nonlinear controller. The transient is applied at $t =$ 150 ms, and the system can be seen to stabilize after the load step in roughly two mains cycles. It can also be noticed that the dynamics are practically equivalent in both controllers despite the nonlinear gains being used during the load transient. It is

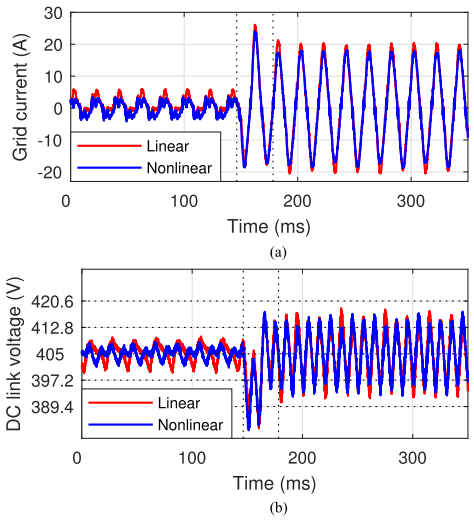

Fig. 6. (a) Input current waveform during a load step from 150 W to 2.4 kW. The load step is applied to the system at $t = 150$ ms. (b) Voltage of the dc link. The settling time of the load step for both control methods is 32 ms.

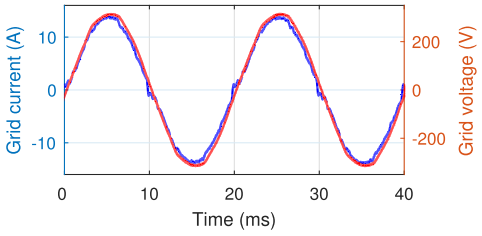

Fig. 7. Steady-state waveforms at 9.6-A RMS current with the proposed nonlinear voltage controller regulating the dc-link voltage.

worth mentioning that the current waveform has a significant zero cross distortion, which can be seen in Fig. 7. This distortion is caused by limitation of the duty cycle, which is limited by the software to the maximum value of 0.8. The hard limit is imposed in order to ensure that the current transformers that are used to measure the feedback current from the switches have enough time to reset in all possible operating conditions.

In Fig. 8(a) and (b), the results from the other load step test are shown. Again, similar performance between the controllers can be seen, and the control behaves as intended. Since the PFC hardware cannot feed power back to the grid, the PFC operation is simply halted when the dc-link voltage goes above 420 VDC. The nonlinear controller has lower overshoot, but this is not caused by the dynamics of the controller, and instead depends on the phase of the grid voltage at which the load is stepped down.

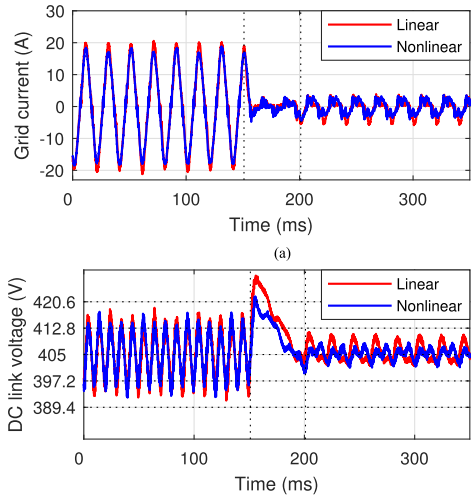

Fig. 8. (a) Input current waveform and (b) the voltage of the dc link during a load step from 2.4 kW to 150 W. The load step is applied to the system at $t = 150$ ms. The voltages on the Y-axis represent the gain regions of the nonlinear controller. The settling time of the load step for both control methods is 50 ms.

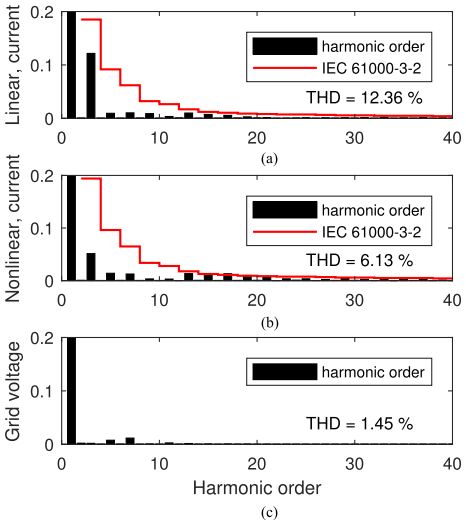

Fig. 9. Comparison of the input current harmonic content with the (a) linear and (b) nonlinear controllers. (c) shows the harmonic content of the mains voltage when the converter is turned OFF.

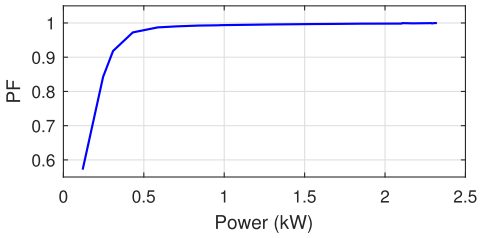

Fig. 10. Power factor with respect to load power using the nonlinear voltage control.

The effect of the nonlinear controller on the grid current quality is evaluated by applying a harmonic current analysis, that is, the THD is studied. The current harmonics are used to calculate the THD at a 2.4-kW load. The THD calculation is done by taking into account the root-mean-square (rms) values of the first 40 current harmonics. In Fig. 9, the input current rms harmonics are illustrated for both control configurations: the linear PI control and the nonlinear PI control. In addition, the applicable limits for odd harmonics specified in the IEC 61000-3-2 standard for Class A devices are shown with a red curve for both control configurations with the calculated harmonics. Note that the harmonic limits are slightly different between linear and nonlinear controllers, as the fundamental rms currents are different. Evidently, both controllers have a dominating third harmonic and low amounts of higher order harmonics. More importantly, it can be observed that the third harmonic is significantly reduced when the nonlinear controller is applied. It can be noticed from the steady-state currents in Figs. 6(a) and 8(a) that the linear voltage controller produces a higher current peak with a higher distortion when compared with the nonlinear control.

Moreover, Fig. 9 shows that in the case of the linear controller, the calculated THD of the input current is 12.36%, which is mostly due to the elevated third harmonic. Correspondingly, the THD decreases significantly, to 6.13%, when the nonlinear controller is employed. Thus, the nonlinear controller can achieve an over 50% improvement in the current THD. The measurement was taken with the system input current following the actual mains voltage waveform, and therefore, some of the distortion is caused by the distortion in the mains voltage itself. The mains voltage harmonics with the converter turned OFF are presented in the bottom of Fig. 9. Note that the mains voltage has noticeable fifth and seventh harmonics, which can be seen in both current harmonics as the PFC current waveform is set to follow the mains voltage.

To further validate the performance of the nonlinear voltage control, in Fig. 10, the measured curve of the power factor with respect to the load power is shown. It can be noticed that with load power above 0.75 kW, the PFC system power factor is close to unity. The power factor was measured using the Yokogawa PZ4000 power analyzer, and a HITEC B2000 current transformer was used for current sensing. Moreover, the steady-state waveforms of grid current and voltage at 9.6-A rms current are shown in Fig. 7, which shows that they are closely to same phase

with each other; thus, the current follows the mains voltage. The comparison of the linear and nonlinear controllers is given in Table II, where the settling times of load steps and input current THDs are given.

V. Conclusion

This paper presented a nonlinear controller for the dc-link voltage control of a PFC converter. The controller was shown to effectively improve the quality of the mains current when compared with a linear PI controller. It was shown that the proposed nonlinear controller has a simple structure, viz., the complexity is only marginally more complex than a traditionally used linear PI controller. Thus, the simple structure provides benefits for the practical implementation of the algorithm. More importantly, the control can also be tuned straightforwardly with the same method as would be used with the traditional PI controller. The effectiveness of the nonlinear controller was verified by experimental tests using harmonic current analysis and by comparing the time-domain performance of the nonlinear controller with the linear counterpart. The time-domain requirement was fulfilled, as the proposed nonlinear controller can stabilize the system within two to three mains cycle against load transient. Note that this result is comparable to the results obtained with more complex control structures, like in [17]. Moreover, the nonlinear controller was shown to effectively improve the THD of the input current from 12.36% to 6.13% without affecting the dynamics of the dc link. The limits for odd harmonic content according to IEC 61000-3-2 were used to show that the proposed controller meets the harmonic requirement for Class A devices.

Appendix

Since the controller is known, the proof of stability for the closed loop is the problem of finding common P for the closed-loop systems A_i such that that the Lyapunov inequality given in (2) holds. Assuming a no-load condition, i.e., $R = \infty$, the system (11), (12) can be written in matrix form as

$$A_1 = \begin{bmatrix} -\frac{K_{P1}}{C} & \frac{1}{C} \\ -K_{I1} & 0 \end{bmatrix} = \begin{bmatrix} -261.267 & 666.667 \\ -34.074 & 0 \end{bmatrix} \tag{27}$$

$$A_2 = \begin{bmatrix} -\frac{K_{P2}}{C} & \frac{1}{C} \\ -K_{I2} & 0 \end{bmatrix} = \begin{bmatrix} -522.467 & 666.667 \\ -68.148 & 0 \end{bmatrix}. \tag{28}$$

The positive-definite matrix

$$P = \begin{bmatrix} 16.3972 & -6.6741 \\ -6.6741 & 285.5394 \end{bmatrix} \tag{29}$$

can be verified to prove the stability by substituting A_1 and A_2 and the common P (29) to the Lyapunov inequality (2).

Acknowledgment

The authors would like to thank Powernet Oy for cooperation in the study and providing the converter prototype. The authors would also like to thank Dr. H. Niemelä for her help in improving the language in this paper.

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Publication III

Korhonen, J., Honkanen, J., Rautio, J., and Silventoinen, P.
Effect of Current Measurement Timing and Antialiasing Filter in a Single-Phase Inverter

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Proceedings of IEEE Applied Power Electronics Conference and Exposition,
Anaheim, CA, USA, pp. 938–943

Effect of Current Measurement Timing and Antialiasing Filter in a Single-Phase Inverter

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***Abstract*—Synchronous current measurement is a standard method for digital inverter control. Conventionally the measurement is sampled at pulse-width modulation carrier peaks to provide an average value of the current over the modulation cycle. With increased switching frequencies of inverters, the accuracy of the current measurement may suffer, especially during short output voltage pulses at high duty cycles. This paper focuses on the effect of sampling instant timing of the current measurement of a single-phase H-bridge inverter. Experimental tests show that proper analog to digital conversion timing and antialiasing filter design will significantly improve the current measurement accuracy.**

***Index Terms*—Single-phase inverter, Current measurement, Antialiasing filter**

I. Introduction

Synchronous current measurement has been a standard method for digital inverter control for decades [1]. The inverter current control performance is limited by several delays from the measurement to eventually pulse-width modulated (PWM) output voltage waveform. In the literature, the primary delay sources have been reported to be the antialiasing filter, analog to digital conversion (ADC), computation delay, gate driver, and switching delays [2], [3].

In general, the current control is limited by the output filter, the switching frequency f_{sw} of the inverter, and system delays. Half of the switching frequency determines the Nyquist frequency of the control system. The current measurement and the computed PWM voltage reference value are zero-order hold (ZOH) by nature for digital PWM [4].

Current measurement errors impair the converter control. For example, in single-phase inverters the current measurement scaling and offset errors have been compensated with a proportional resonant controller [5]. For three-phase inverters scaling and offset error compensation methods, such as periodic disturbance observer and proportional integral plus two resonant controllers have been proposed [2], [3], [6], [7]. These compensation methods are primarily executed in the dq-frame.

The switching frequencies of modern inverters have been consistently increasing, especially as a result of advances in switch semiconductor technologies [8], [9]. For grid-connected inverters, the increased switching frequencies allow the grid filter inductive components to be dimensioned smaller [10], [11]. Even with relatively high switching frequencies (above tens of kilohertz), the current measurement accuracy is very dependent on the correct timing of the measurement.

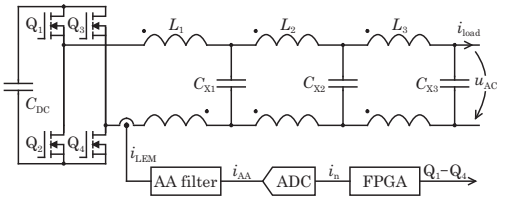

Fig. 1. Single-phase grid-forming inverter with an EMI filter. The current measurement i_{LEM} is filtered with an antialiasing filter, then converted from analog to digital format, and finally fed to the controller. i_{n} is the sampled current measurement.

In this paper, the effects of the antialiasing filter and current sample timing on the current measurement accuracy are studied. The sample timing compensation procedure is described with and without an antialiasing filter. A fixed delay compensation was used in this study, and one of the primary research questions of this paper is to find out whether a fixed delay is sufficient for current control at relatively high switching frequencies (tens of kilohertz). The study is performed with an experimental test set-up for a single-phase grid forming inverter, shown in Fig. 1. The inverter control unit is able to communicate the measured samples to a PC for post processing and analysis.

II. Current measurement of a single-phase inverter

The current measurement sample should give the average value of the load current over the PWM cycle. Conventionally the inverter output current is measured at the mid-point of the PWM cycle, or at the beginning and the mid-point of the PWM cycle. These two points are the PWM carrier triangle waveform peaks. In an ideal system, these two points give the average current over the PWM cycle, and are free of switching noise. In an actual system, during high reference duty cycles, the PWM produces very short pulses. Sampling the current during a short pulse will potentially lead to a sample with induced high frequency noise, or sampling an erroneous value

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during a current slope with very high di/dt. This problem was addressed with a single sampling current measurement method, which alternates the sampling peak of the carrier based on the duty cycle [12]. However, this method does not address the measurement error produced by the measurement loop delays.

A. Measurement error sources

The current measurement is subject to delays and phase-shift caused by the antialiasing filter, ADC, and digital signal processing. In addition, the actual voltage pulse generated by the inverter is not precisely in phase with the carrier, due to gate driver and switching delays, and an offset generated by dead time [3]. The delays also drift during operation. For example, the switching delays are a function of switched current. Also, dead time originated shift may have a discontinuity when the load current changes polarity. Other sources for measurement drift are temperature and component aging [13]. Also, the output of the antialiasing filter will not be a pure sinusoidal signal, as the duty cycle will have an effect on the waveform.

In a single-phase converter, the current measurement error must be minimized, because it may be the only measurement alongside the DC link voltage measurement. When considering the case that there is no antialiasing filter and the measurement is only limited by the sensor and the ADC, current measurement is problematic at high switching frequency with short PWM pulses. The problem arises when modulation duty cycle is high, which results in output voltage pulses in the range of hundreds of nanoseconds. During the short pulse, the current will change with an amplitude of the current peak-to-peak ripple. This will result in high di/dt. This presents an issue on the timing of the current measurement, as multiple delays in the system can cause the triggering instant to differ significantly from the center of the sampled waveform.

The measurement error that is originated by the delays has a different effect depending if the current is sampled once or twice per PWM period. Obviously, if the delays are not properly compensated, the value of each sample will be erroneous in both cases. For the single sampling method, the error will produce a DC offset on the current measurement signal. Compensation of such an error in a single-phase inverter may be hazardous, since the error may be originated by the measurement loop, or it may actually be a DC offset in the current. In the case of two samples per period, the measurement signal will have a ripple at sampling frequency. This is because the samples will be from a triangular ripple current produced by the inverter. Therefore, one of the samples will have a value that is smaller than the average current value over the PWM cycle, and the other sample value will be larger than the average current value. With this approach, the mean value of the last two samples can be used to calculate the load current average over the PWM cycle. The drawback of the additional mean value calculation is the additional delay in the current control, which limits the bandwidth [4].

The antialiasing filter dimensioning, namely the RC cutoff frequency, affects the phase-shift between the switching current ripple and the filter output signal that is sampled by the ADC. If the RC circuit is dimensioned for a lower cutoff frequency than f_{sw}, the current ripple will be attenuated, but the phase-shift of the filter will cause significant delay to the measurement. On the other hand, if the RC circuit is dimensioned for a higher cutoff frequency than f_{sw}, the phase-shift will be less than 45°, and the bandwidth limitation of the current loop will not as be significant, because the effective control bandwidth is limited by the Nyquist frequency of PWM ($f_{\mathrm{Ny}} = f_{\mathrm{sw}}/2$). In this case, the timing of the measurement will play a much bigger role in order to limit the measurement error.

B. Delay compensation tuning

The objective of the current measurement is to provide an accurate sample of the average current and to have high bandwidth for control loop. Therefore, two current samples are measured per PWM cycle. In order to minimize the phase lag, and consequently maximizing the measurement bandwidth, the antialiasing filter cutoff frequency is tuned above the switching frequency.

In [14] an antialiasing filter was used, but the triggering of the current measurement was still done at PWM carrier peaks. If the phase-shift caused by the antialiasing filter is not compensated, it will cause a measurement error. In this paper, the compensation is referred to as the required delay on the ADC trigger signal that will provide an accurate sample of the average current.

The approach used in this paper is to use an antialiasing filter with a higher cutoff frequency than f_{sw}, and compensate the delay generated by the filter in the timing of the current measurement. In order to minimize the delays of the current control loop, the voltage reference for PWM is updated as soon as the computation is executed [15].

When the sampling instant is delayed from the carrier peaks, it will cause for the sampling to be during a switching operation of the inverter. Here the trade-off will be done between the high di/dt originated error and using an antialiasing filter and introducing a delay, which has to be compensated. The antialiasing filter will reduce the switching noise seen by ADC, which is shown in Section III.

The following delays in the measurement can be considered almost constant during operation: analog to digital conversion, computation, and gate driver delays. The switching delays vary as a function of current, and antialiasing filter output as a function of duty cycle. A few approaches can be taken in the compensation of the switching delays and loading condition. A fixed delay compensation value is the simplest solution, and it was selected for this study. The effectiveness of this approach is demonstrated in Section III.

The delay compensation value was first calculated as the sum of the described delays and the final value was fine tuned experimentally to achieve the best result. The primary delay was introduced by the antialiasing filter. When the cutoff

TABLE I
EXPERIMENTAL SETUP.

f_{out}	output frequency	50 Hz
f_{sw}	switching frequency	50 kHz
f_{ctrl}	control frequency	100 kHz
f_{s}	current sampling frequency	100 kHz
f_{AA}	AA cutoff frequency	70 kHz
t_{DT}	dead time	250 ns
t_{ADC}	AD conversion time	438 ns
u_{AC}	output voltage	230 V
u_{DC}	DC link voltage	365 V
L_1	Primary inductance	410 µH
L_2	1st EMI filter inductance	2.4 µH
L_3	2nd EMI filter inductance	2.4 µH
C_{X1}	1st X-capacitance	9.1 µF
C_{X2}	2nd X-capacitance	2.2 µF
C_{X3}	3rd X-capacitance	9.3 µF
	current sensor	LTSR 15-NP LEM
	gate driver	Si8271DB-IS
	ADC	MAX11115
	FPGA	10CL010YU256I7G

frequency of the antialiasing filter was 70 kHz, the phase lag at the switching frequency of $f_{\mathrm{sw}} = 50$ kHz is 37°, which represents a delay of 2.1 µs for the switching frequency component. Rest of the delay sources are presented in Table I and the final compensation value was found at 3.5 µs.

Another approach for the delay compensation would take into account the varying delays caused by the switching delays and the effect of varying duty cycle on the phase lag of the antialiasing filter. A grid forming inverter must be able to feed various loads, including non-linear and capacitive loads. As a result, this compensation method would require an extensive look-up table for each condition. Therefore, this method is left for future research.

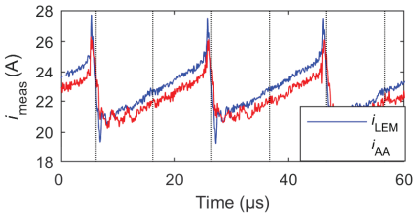
III. EXPERIMENTAL RESULTS

The effect of current measurement timing and antialiasing filter were experimentally tested with a single-phase H-bridge converter. Bipolar modulation was used and the switching frequency was $f_{\mathrm{sw}} = 50$ kHz. The measurement setup information is given in Table I. The system was tested with several loading conditions:

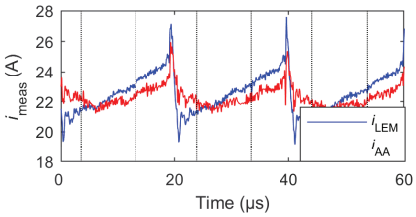
- no-load
- 26.6 Ω
- 15.3 Ω
- 86 µF
- 86 µF and 186 Ω in parallel

During the no-load condition, the inverter feeds the grid filter. The total capacitive loading imposed by the EMI filter is 20.6 µF.

The first set of measurements were performed by measuring the current sensor output signal (i_{LEM}) and the antialiasing filter output (i_{AA}) from the converter. The measured waveforms without and with the antialiasing filter capacitor are shown in Fig. 2. The sampling time of the current measurement was manually tuned to minimize the difference between the two consecutive measurement ADC samples (Δi_{n}). Without



(a) No AA filter capacitance



(b) With AA filter

Fig. 2. Current measurements from the current sensor output (i_{LEM}) and antialiasing filter output (i_{AA}). Measured current measurement sampling trigger signal is indicated with a dashed line. Both measurements are with compensated sample timing to minimize the measurement error.

the antialiasing filter the timing error was compensated by delaying the trigger signal by 500 ns from the carrier peaks and with the antialiasing filter by 3.5 µs. It can be seen from Fig. 2(a) that due to high di/dt even a small change in timing of the current sample at the falling current edge will significantly affect the sampled value.

Next, the sampled measurements from the FPGA control were logged with four different current measurement cases:

- without antialiasing filter capacitor and sampled at carrier peaks
- without antialiasing filter capacitor and sampled at compensated instants (500 ns delay)
- with antialiasing filter and sampled at carrier peaks
- antialiasing filter and sampled at compensated instants (3.5 µs delay)

These measurements were logged at no-load condition and with a 15.3 Ω resistive load. The results can be seen in Fig. 3. The effect of compensating the timing without the antialiasing filter capacitor has a very small impact on the sampled current measurement. The same applies to adding the antialiasing filter and sampling the current at carrier peaks. Once the antialiasing filter is used and proper compensation is applied, the difference between the consecutive current measurements is significantly reduced. The mean value of the absolute value of the difference between the two consecutive current samples (mean$|\Delta i_{\mathrm{n}}|$) is shown for each measurement in Fig. 3. It can be seen that the loading condition does not have a very big impact on the difference between the two consecutive samples, regardless of

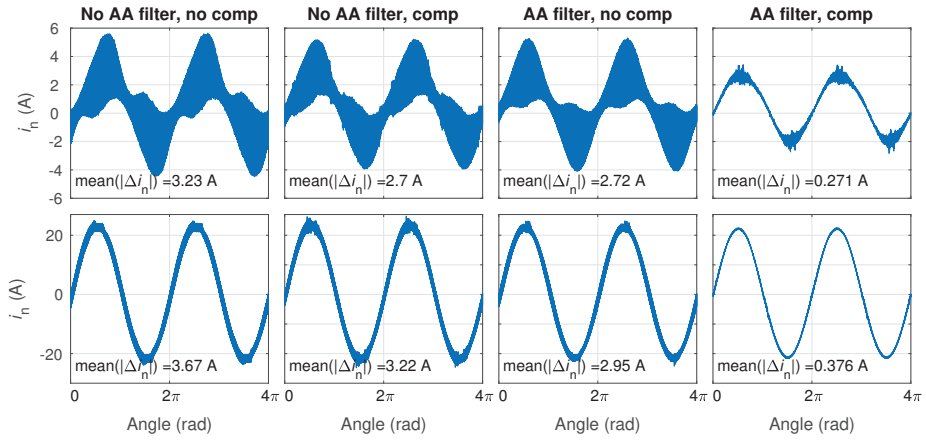


Fig. 3. Current measurements from the converter control. No load conditions on top graphs and resistive load of 15.4 A on bottom graphs. Δi_n is the difference between the two consecutive current samples.

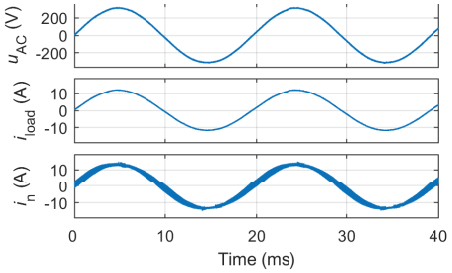


Fig. 4. Grid voltage (top), load current (middle), sampled current (bottom), when the load was $R = 26.6\,\Omega$, and the current was sampled at carrier peaks.

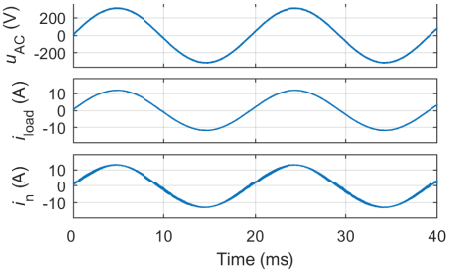


Fig. 5. Grid voltage (top), load current (middle), sampled current (bottom), when the load was $R = 26.6\,\Omega$, and the current sample was compensated with a 3.5 µs delay.

the timing of the samples within the PWM cycle.

Next, the effect of loading condition and the delay compensation on the control are studied. For the following measurements, the antialiasing filter was used ($f_\mathrm{AA} = 70\,\mathrm{kHz}$). Now the loading conditions under study are $R = 26.6\,\Omega$, $C = 86\,\mu\mathrm{F}$, and parallel connected $C = 86\,\mu\mathrm{F}$ and $R = 186\,\Omega$. With the parallel connected RC load case, only current controller was used. The oscilloscope for the measurements was Agilent DSO 6104A, the output voltage u_AC was measured with Tektronix PS5210 differential voltage probe, and the load current i_load with Rohde & Schwarz RT-ZC20 30A current probe. The current samples from the FPGA (i_n) are illustrated with the measurements. It should be noted, that the samples from the FPGA and the measured values from the oscilloscope are manually aligned. The total harmonic distortion for the 50 first harmonics for the measured grid voltages and currents are shown in Table II.

The measurements for resistive loading condition and when the current was sampled at carrier peaks is shown in Fig. 4, and when the current sample was delay compensated in Fig. 5. The grid voltage and current show very little change, regardless of the sampling instant. Only the sampled current and the THD values in Table II have a noticeable difference.

The measurements for capacitive load of $C = 86\,\mu\mathrm{F}$ are shown in Figs. 6–7. In this loading condition, the load current has some disturbance at low current amplitudes when the measurement instant is not compensated. Also, the sampled current has a more distorted waveform compared to the compensated measurement. The current THD is improved by 0.89 % when the sampling is compensated.

The last loading condition was parallel connection of $C = 86\,\mu\mathrm{F}$ and $R = 186\,\Omega$. The measurements are shown in

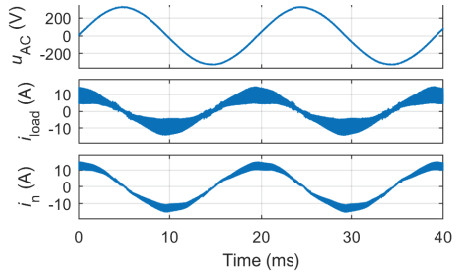


Fig. 6. Grid voltage (top), load current (middle), sampled current (bottom), when the load was $C = 86\,\mu\text{F}$, and the current was sampled at carrier peaks.

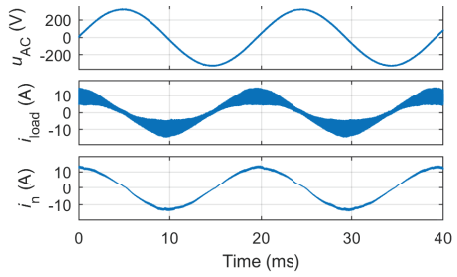


Fig. 7. Grid voltage (top), load current (middle), sampled current (bottom), when the load was $C = 86\,\mu\text{F}$, and the current sample was compensated with a $3.5\,\mu\text{s}$ delay.

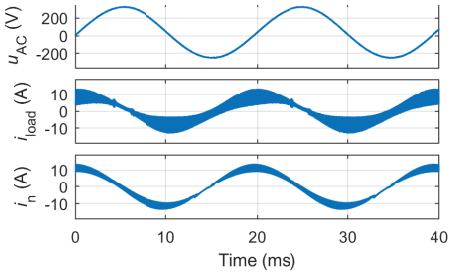


Fig. 8. Grid voltage (top), load current (middle), sampled current (bottom), when the load was parallel connected $C = 86\,\mu\text{F}$ and $R = 186\,\Omega$, and the current was sampled at carrier peaks.

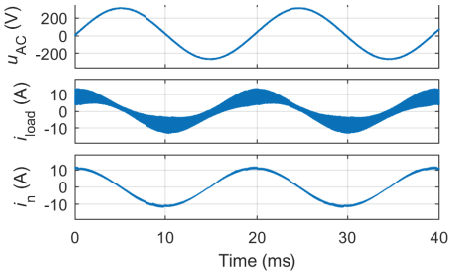


Fig. 9. Grid voltage (top), load current (middle), sampled current (bottom), when the load was parallel connected $C = 86\,\mu\text{F}$ and $R = 186\,\Omega$, and the current sample was compensated with a $3.5\,\mu\text{s}$ delay.

Figs. 8–9. Again, a slight disturbance can be seen in the load current when the current is sampled at the carrier peaks. Now the load current THD is improved 0.82 % when the sampling is compensated.

When the Figs. 4–9 are studied, the effect of duty cycle and loading condition on Δi_n can be determined. The difference between the two consecutive current samples is more dependent on the duty cycle than the loading condition. This can be seen as Δi_n has the smallest value at load voltage peaks, during which the duty cycle is high. Similarly Δi_n is proportionally higher when the load voltage and the duty cycle are near zero. This trend applies to all measured cases. Even though Δi_n varies primarily as a function of the duty cycle, the absolute values change depending on loading condition. Therefore, in order to fix the residual measurement error, an extensive manual tuning would have to be performed.

Overall, when Table II is considered, it can be seen that the proper measurement timing compensation improves the THD in every loading condition. However, it can also be noticed that the THD of the formed grid voltage is below 1 % even when the current sampling is at the carrier peaks. So, it can be concluded that performance-wise the improvements were proportionally significant, when the sampling was compensated,

TABLE II
TOTAL HARMONIC DISTORTION OF THE LINE VOLTAGE AND CURRENT.

Loading condition	Sample instant	THD u_AC	THD i_load
$26.6\,\Omega$	Carrier peaks	0.59 %	0.60 %
$26.6\,\Omega$	$3.5\,\mu\text{s}$ delay	0.39 %	0.42 %
$86\,\mu\text{F}$	Carrier peaks	0.53 %	2.76 %
$86\,\mu\text{F}$	$3.5\,\mu\text{s}$ delay	0.46 %	1.87 %
$86\,\mu\text{F} \parallel 186\,\Omega$	Carrier peaks	0.90 %	1.98 %
$86\,\mu\text{F} \parallel 186\,\Omega$	$3.5\,\mu\text{s}$ delay	0.37 %	1.16 %

even though the absolute values of the improvements were relatively smaller.

To illustrate the effect of the sampling in the frequency spectrum, the FFT of the sampled current in the capacitive loading condition (i_n from Figs. 6–7) is shown in Fig. 10. The 5th and 7th harmonics have clearly lower magnitude with the compensation and proper sample timing. Above 6 kHz the non-compensated sampled current has a noticeably larger magnitude which is most significant around the 25 kHz Nyquist frequency of the PWM. The proper timing of the sampling instant significantly lowers the switching noise from the measured current. Obviously, the lower noise allows higher

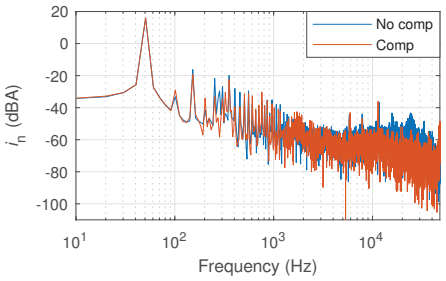


Fig. 10. Sampled current FFT, when the load was $C = 86\,\mu$F. With 'No comp' the current is sampled at carrier peaks, and with 'Comp' with a 3.5 µs delay.

gains to be used for the current control.

IV. Conclusions

In this paper, the effect of proper current measurement sample timing for a single-phase inverter was demonstrated. The conventional current measurement method of sampling at PWM carrier peaks was found to produce a significant measurement deviation for the consecutive samples. The same applied, even when the sampling and switching delays were compensated. With the use of antialiasing filter that has a cut-off frequency that is higher than the PWM Nyquist frequency, the current measurement samples showed reduced deviation. The experimental results showed that a fixed sampling compensation can provide sufficient current sampling regardless of the duty cycle and loading condition. The downside of the method was that even though the compensation delay can be estimated, manual tuning is required to achieve the best result.

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Publication IV

Hannonen, J., Ström, J. P., Honkanen, J. Räisänen, S. Silventoinen, P.,
and Pokkinen, O.
Design of digitally controlled isolating 1-phase
AC/DC converter by using centralized processing unit

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Design of Digitally Controlled Isolating 1-phase AC/DC Converter by Using Centralized Processing Unit

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Keywords

<<DC power supply>>, <<Power factor correction>>, <<Switched-mode power supply>>, <<Systems engineering >>, <<Single phase system>>

Abstract — This paper presents a fully digital control design for 1-phase 3 kW AC/DC converter. The centralized control system is designed and implemented on microcontroller-FPGA combination. This paper emphasizes the control design flexibility for switching mode power supplies when the programmable controller approach is used.

I Introduction

The control of switching mode power supplies (SMPS) have been the interest of many researchers and system engineers for decades. Numerous publications and books have been published on the modeling and implementation of the control aspects of an SMPS [1–4]. A traditional way to implement the SMPS control circuit is to use analog circuits as they are known well and are easy to implement, and they provide control signals for the SMPS accurately without major delays and timing issues. Despite the fact that digital control in SMPS has been studied since 90's [5], and that the digital control have been a common approach for example in motor drive applications for decades, it has been in background when the SMPS control platforms are discussed. Among the rapid development and increased computational power in the programmable controllers the digital control approach in SMPS devices has become an interesting topic.

As the traditional analog control design is well known and widely used in SMPS applications, a great variety of control ICs which provide the core control functions for the SMPS are commercially available. These ICs provide a good selection of solutions for different power supplies and they also decrease the design effort of the SMPS control. However, this solution presents limitation to the flexibility, since the control method to be used with the selected IC is in most of the cases fixed [6].

A more flexible way to implement the system control is to use a programmable controller or multiple controllers that are configured with software. The control unit can be a processor- (e.g. microcontroller, MCU or digital signal processor, DSP), a programmable logic- (e.g. field programmable gate array, FPGA or Complex Programmable Logic Device, CPLD) or a combination of these. The programmable controller presents functionalities that are not available or difficult to implement with analog control. The functionalities that the digital control approach enables are for example data logging, self-diagnostics with digital data analysis, remote system control, system health monitoring utilities, parameter estimation and system adaptation to different operating conditions [5, 7]. The digital control also allows the use of more advanced linear or non-linear control algorithms [2, 7]. These kind of control methods are for example sliding mode and fuzzy control.

The use of centralized digital control approach is not entirely free of challenges. Obviously the design effort for the controller platform and the control itself increases when a digital control approach is used. When using digital control it should be noted that limitations on the control execution rate are introduced when the speed is compared to

analog control. The centralized control approach also introduces signal partitioning issues especially, when a galvanic isolation between the input and output of the power supply must be provided [8].

This paper presents a centralized controller and platform design on a switching mode power supply. The design from the centralized controller and digital control point of view is presented and factors that need to be considered when choosing the centralized digital controller are reviewed. In experimental section a design of centralized digital controller platform by applying a combination of MCU and FPGA is presented. The implemented digital controller system is used to control a 3 kW AC/DC power supply.

II Digital controller platform design

When designing a digital control system, the requirements for control performance must be defined before any considerations of the controller or platform to be used should be made. The most distinct difference between the digital and analog control is the maximum applicable operating frequency. The control loop frequency and the delay time in digital control system cause limitation for maximum control frequency. The most crucial and time critical task for a the centralized controller is to execute power stage control functions of the SMPS. Control task execution rate determines minimum requirement for computational performance.

As the control tasks execution and peripherals define the computational performance for the system, the rest of the controller processing capacity is available on the additional functionalities outside the power stage control. These kind of tasks are for example system health monitoring, user interface, system remote control, and communication related procedures. It should be noted that all additional functionalities increase the need for context switches which increase the non-application specific work load (overhead) on the MCU, especially when interrupt based execution is applied. The context switch overhead should be minimized in order to meet the requirements for time critical control and allow the MCU processing capability to be used economically. The context switch overhead can be reduced by decreasing the number of those processes that need active software interventions. For example in most of the 32-bit MCUs many communication, AD conversions and timing procedures can be done in the background of the active processing.

Review on controllers for centralized control of power electronics applications

The controller choice for centralized digital control is mostly defined by the needed computational performance. The performance needed is highly dependent on the application, therefore an universal solution for a controller is difficult to determine. In several publications various solutions for digital system controller are proposed. For example in [9, 10] a controller system with a DSP and FPGA combination is presented. The system control can also be implemented by a dedicated microcontroller for power supply control [7], or completely by programmable logic device [11, 12]. In the following, few widely used control platform solutions are reviewed:

- A single chip MCU specially designed for power electronics control systems
- A single chip multi core MCU or DSP with two or more processing cores.
- A combination of a not power electronics control orientated MCU or DSP combined with a programmable logic device, such as an FPGA or a CPLD
- An FPGA with external peripheral devices such as AD converters

An MCU specifically designed for power electronics control applications consists of a controller that includes high resolution pulse width modulators (PWM) even up to megahertzes of switching frequencies, versatile AD and DA converters, analog trip section, and peripherals for communication[13]. The power electronics control dedicated microcontrollers may consist of co-processors dedicated for the time critical control execution. The issue that this controller type may present is the code portability between different MCUs due to highly individual system configuration and controller family related co-processors and peripherals. Therefore the single sourcing risk for a specific controller type should be noted. Also the calculation intensive functions might introduce computational performance issues when done on MCUs [14]. The power electronics control application dedicated MCU is well suitable for production line systems due to cost efficiency of the devices [13].

A microcontroller with multiple processing cores is applicable solution for a SMPS centralized controller when the MCU computational load caused by additional functionalities such as data logging and multiple communication

peripherals (CAN, Ethernet, SPI, USART) are increased. By using two MCU cores, the controller unit does not have to share the computational performance between the control and additional functionalities [15]. In multicore system the time critical and complex computational algorithms can be processed parallel. The SMPS design benefits from the multi core system in design costs and decreased need for printed circuit board (PCB) real estate. As the system is highly integrated on one chip the single sourcing problem with multi core systems is emphasized. The code portability to other controller family becomes easily an issue, as the data sharing and core related configurations are usually MCU family specific. The multicore system is applicable in those systems where multiple co-functionalities, which need intensive computational performance and DSP features, are added to time critical control function execution [15].

A flexible and adaptable system controller platform can be achieved by using FPGA or other programmable logic system. This approach allows the designer to fully develop all the needed functionalities for the SMPS control. The FPGA based system controls are executed parallel. This allows multiple independent control system executions simultaneously, hence the response time reduces and digital control system execution rate can be increased significantly [16]. The parallel logic based operation also removes the context switching overhead issues in the control system outlined in the beginning of Section II. Some of the FPGAs support a configurable embedded processors such as MicroBlaze by Xilinx [17] and Nios II by Altera [18] that can be implemented in the logic design. The embedded processors can be used similarly compared to MCUs, hence the sequential execution is made easy. This is versatile feature to be used for example in power stage control functions implementation. The most versatile advantage by using the programmable logic is the full reusability of the programmed code. Aside from few exceptions such as core blocks and embedded processors designed for certain FPGA family, the logic design dependency on chip manufacturer is low. This is due to the standardized hardware description languages such as VHDL and Verilog, which are presented in standards IEEE Std 1076-2008[19] and IEEE Std 1364-200 [20]. Due to standardized logic description, the platform changes do not cause major revision demand for the system control design. Although the FPGA is very flexible, the system control development might be sufficiently slower compared to microcontroller based approach due to extensive development of all peripherals. Also the programmable logic approach needs external devices for system control such as AD converters and bus drivers which increase the costs and PCB real estate demand for the design.

An MCU or DSP combined with an FPGA enables flexibility for system control design [9]. The MCU can be applied for example signal conversions, digital filtering, control loop processing, and other signal processing tasks. The FPGA feasibility comes in applications where a the peripherals integrated in MCU are not versatile enough or the MCU high control loop execution rate is aimed [12, 16]. The FPGA provides full configurability and therefore the components and behavioral that are not included on MCU can be implemented on FPGA. Although MCU combined with a programmable logic device allows flexibility in design, the solution may end up costly. This controller approach is applicable in systems where strict timing requirements with up to tens of megahertz rate of execution is required or the MCU peripherals are not versatile enough for the system control. The solution can also be preferred in large systems, where parallel operation or multiple simultaneous controlled PWM channels are required. The flexibility of FPGA and the eased control functions design of the MCU make this approach attractive also in research and development purposes.

The control platform should always be chosen according to the application. The one controller approach is a preferable solution if the system costs or PCB area are needed to be minimized. If any of the available microcontrollers do not have the needed peripherals for the system control or they can not provide the performance needed to fulfill the required timeframe the FPGA based approach should be preferred. When the controlled platform must provide high flexibility and computational performance or the platform is used for multiple different purposes with only slight changes in control design, the MCU with FPGA approach is versatile option for system controller.

III Experimental system design

An experimental digital controller system is designed for a 3 kW AC / DC power supply with 230 V AC input voltage and 24 V DC output voltage. In this prototype design, an MCU combined with FPGA solution, XynergyXS [21], is applied as the system controller. The controller includes an ARM Cortex-M4 based STM32F4 series microcontroller and a Xilinx Spartan 6 series FPGA. The microcontroller is operated with 168 MHz clock frequency and it is equipped with a floating point unit. The FPGA is operated with clock frequency of 250 MHz.

System hardware and signaling

The SMPS is designed to produce a galvanically isolated output voltage with maximum output current of 125 A. The AC/DC power stage consists of a primary side passive rectifier and an interleaved continuous conduction mode boost

stage for providing 400 V primary DC link voltage and active power factor correction (PFC). The parallel boost stage operation reduces current stress for switches due to load being shared between two boost stages. The interleaved operation of the boost stages double the apparent switching frequency seen from the grid side of the converter, hence the current ripple is reduced. The isolating DC/DC stage is implemented using a phase shifted full bridge for driving step down transformers. The phase shifted modulation allows for zero voltage switching operation and hence reduces the switching losses in the primary side full bridge switches. Secondary power stage consists of current doubler circuit with synchronous rectifier, of which operation is presented in [3]. Synchronous rectifier power stage can be used to minimize losses by replacing the rectifying diodes with MOSFETs [22]. The current doubler topology reduces the transformer current rating and reduces the current ripple at the output compared to conventional rectifier [4]. A main circuit diagram with control system and measurement signal conditioning is presented in Figure 1.

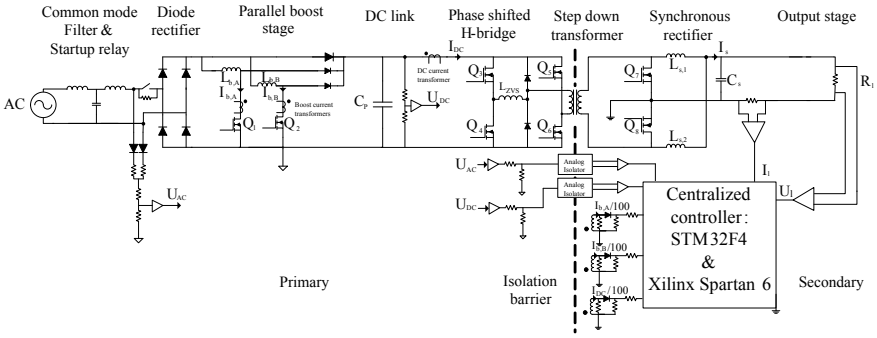

Figure 1. Main circuit diagram of the AC/DC power supply with centralized controller and measurement signal conditioning. The centralized control unit is placed on the secondary side of the converter. The unit includes STM32F4 Cortex M4 ARM-architecture based microcontroller and Xilinx Spartan 6 based FPGA. Control signals of the switches Q_1 - Q_8 are left out of the presentation.

As shown in Figure 1 there are three power stages where controllable semiconductor switches exist. The parallel boost stages at the primary side are operated with 180 ° interleaved carrier frequencies, as presented in Figure 2 each with 100 kHz switching frequency. The full bridge and the synchronous rectifier stages are both run with 60 kHz frequency. The synchronous rectifier switches Q_7 - Q_8 control are synchronized to gate pulse instructions of Q_4 and Q_3 respectively.

In centralized control system approach all the measurement signals are provided to the system controller. The measured signals are applied for both control and system state monitoring. In this system design the signals used for SMPS control are DC link voltage (U_{DC}), rectified input AC voltage (U_{AC}), boost A and B switch currents ($I_{b,A\&B}$), DC current (I_{DC}), load voltage (U_l) and secondary load current (I_l).

As presented in Figure 1, the system controller unit is placed on secondary side of the power supply. Therefore the measurement signals $I_{b,A\&B}$, I_{DC}, U_{AC}, and U_{DC} must be isolated from the primary ground. As presented in [8] the signal partitioning can be done by multiple different methods. In this design, isolative current transformers are preferred solution for measuring $I_{b,A\&B}$ and I_{DC}. The transformers secondaries are referenced to same ground as the centralized controller. Similarly the gate pulses for full bridge control are implemented by using pulse transformers, which provide galvanic isolation between the gate and the controller ground plane. The drawback when using the current transformers is the limitation in duty cycle reference due to transformer core saturation phenomenon. The saturation can be avoided by limiting the duty cycle of the H-bridge in order to give the transformer core time to reset between two sequential pulses. In this design, both the full bridge and PFC duty cycle reference is limited to 0.8.

The primary side switching signals (PFC gate pulse instruction and startup relay control) are isolated by using optocouplers. The measurement signals U_{AC}, and U_{DC} are provided to the centralized control unit by using analog isolating differential amplifiers. The differential analog isolation is considered to provide minimum phase delay in the measurement signal and increase the tolerance towards common mode interferences.

Centralized control system design

Centralized control is divided into MCU and FPGA sections. The MCU deals with control tasks, measurement signal AD conversions and signal processing, power stage control, communications, and system state monitoring. The FPGA is applied for pulse width modulators for PFC and phase shifted PWM for full bridge. The FPGA also includes hardware trip functionality and it provides measurement timing for undersampled $I_{b,A\&B}$ and I_{DC} signals,

presented in Figure 2.

The MCU execution is divided into several tasks with unique priorities. Although no real time operating system is applied, MCU processing time is shared for different tasks by running them from prioritized interrupts. Priority levels of different interrupts are defined by demand of time critical operation. In this design, power stage control processes are run on timer interrupts which have the highest priority. By this, the consistency of power stage controls can be ensured.

The second interrupt priority is reserved for externally triggered, time critical AD converted data processing. The $I_{b,A\&B}$ and I_{DC} measurement is based on undersampling, so that each current pulse is sampled only once. The pulse width modulators implemented on the FPGA trigger timing critical AD conversions on the MCU using external interrupts at determined instants during the switching periods. In these occurrences the possible ongoing other AD conversion is put on wait state by the MCU AD converter, to be continued after the time critical conversion is done. The AD conversions of $I_{b,A\&B}$ and I_{DC} are presented in Figure 2.

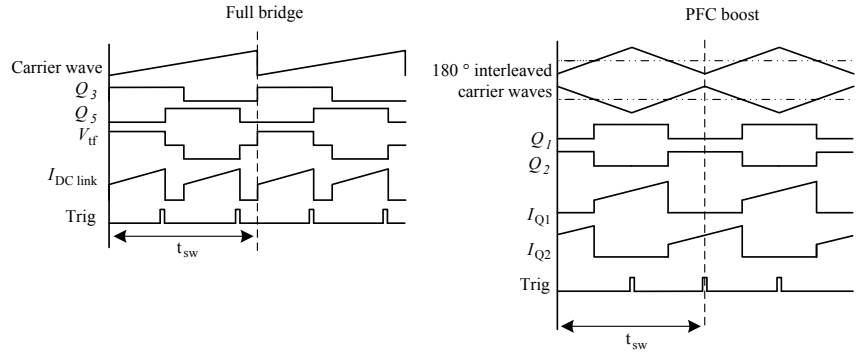

Figure 2. Current measurement timing in PFC and full bridge. The figure shows the gate pulse instructions and their corresponding signals. In full bridge carrier wave, gate pulses of Q_3 and Q_5, corresponding transformer voltage and DC link current are presented. The PFC boost shows 50 % interleaved carrier frequencies, gate pulses of Q_1 and Q_2 and their corresponding current pulses. The trig signal in both of the figures show the timing of AD conversion of the current signal. The horizontal dashed line in PFC figure represents the reference value for PWM.

In the designed phase shift modulation scheme for the full bridge, I_{DC} peak value is at the rising and falling edge of Q_5. The I_{DC} is measured two times in one switching period in order to detect unbalance in the transformer current. The unbalance in the current cause transformer core saturation and it can be detected if the derivative between two sequental samples exceeds the preset over limit value. The measurement rate of the I_{DC} can be halved so that the current is measured only on either rising or falling edge of Q_5 if the transformer core saturation is not considered to be an issue. If the I_{DC} value is measured twice on the switching period, the mean value of the conversion results should be used for power stage control.

A switch current measurement method by using current transformers is applied for $I_{b,A\&B}$ measurement. This is considered to be viable solution when the undersampling of the current signal is used. By measuring the switch current at $t_{sw}/2$, the boost continuous / discontinuous current state does not become an issue from the control point of view when the current pulse is placed symmetrically on $t_{sw}/2$. With all duty cycle references in range of $0<d<1$ the current is flowing through the switch at $t_{sw}/2$.

All the other tasks aside power stage control and AD conversions are considered to be non time critical. Most of the system peripherals such as communication from MCU to FPGA run in background of the MCU. The non time critical processes such as USART for user interface communication is run with lowest priority, outside of the interrupt system.

PFC control

Power factor correction is used to prevent reactive and nonlinear loads from disturbing the electrical grid. Nonlinear loading increases the harmonic content of the grid current and even though the reactive power increases loading in the grid, it does not do actual work. There are standards such as IEC61000-3-2 [23] that define minimum current harmonic content for mains connected devices.

The PFC control is implemented in a way that the input AC current follows the waveform of the input AC voltage. The

complete control scheme is implemented as cascaded PI (proportional-integral) controllers for voltage and current. The basic control structure of the PFC controller is presented in Figure 3.

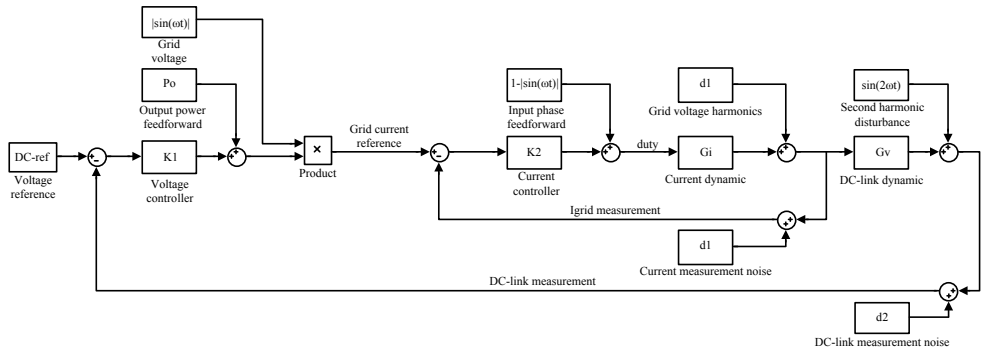

Figure 3. PFC control structure with feed forward paths and major disturbances shown.

The input current of a boost stage can be represented as

$$L_{b,x}\dot{I} = V_o d - V_o + V_i, \tag{1}$$

where V_o is the output voltage, V_i input voltage, I input current and d controlled duty ratio. Since the input of the system is dependent on the output voltage, the system exhibits nonlinear behavior with the changing duty ratio and output voltage. Since the actual volt seconds applied to the boost converter are proportional to the ratio of input and output voltages, a feedback from the input and output voltages can be used to mitigate the effect on dynamics of the varying set-point. If d is replaced by u+1-V_i/V_o equation 1 reduces to

$$\dot{I} = \frac{uV_o}{L}, \tag{2}$$

where u is the newly defined input. This new input is effectively decoupled from the output voltage dynamics. In actual implementation, this is done by adding the defined duty ratio from preliminary feedback to the output of the current controller. The actual controller for PFC current is designed to system modeled by equation 2. Current controller parameters are presented in Table I.

The DC link voltage contains a disturbance of two times the mains frequency, which is caused by sinusoidal power transferred to the DC link. The bandwidth of the voltage controller needs to be limited in order to prevent the controller to follow the DC link disturbance. The voltage loop bandwidth reduction is detrimental to the controlled system time domain performance. The dynamic performance of the controller can be improved by adding a feed forward from the output power to the voltage controller output so that current control reacts to the changes in the loading directly. However, the output power measurement may also contain noise due to measurement hardware unidealities and hence the feed forward signal needs to be filtered. In this system, the feed forward is filtered with a low pass filter with cutoff frequency of 1 kHz, which is higher than the voltage control loop bandwidth. The PFC voltage controller parameters are presented in Table I.

The models used for PFC control implementation provide an estimate on the parameters as the actual circuit has dynamics and delays, such as EMI filtering, which are not taken into account in the modeling. The model is also made for one boost stage only, but in this design the interleaved boost is used as it was presented above. However the controller parameters are not very sensitive as the preliminary input voltage feedback does the bulk of the current control and the transient performance of the voltage controller is mainly accomplished with the output power feed forward.

Phase shifted full bridge

The phase shifted full bridge is used to control the system output. The basic operation of the phase shifted full bridge with current doubler secondary is presented in [1, 4] and similar system with synchronous rectifier in [3]. In this

design the I_{DC} is used for full bridge control as it has the same dynamics as the I_s, only scaled with the step down transformer transform ratio and the gain of current doubler circuit. The control system is constructed in cascade form, where the inner loop consists of current controller that is fed by a voltage controller. The full bridge controller implementation is presented in Figure 4.

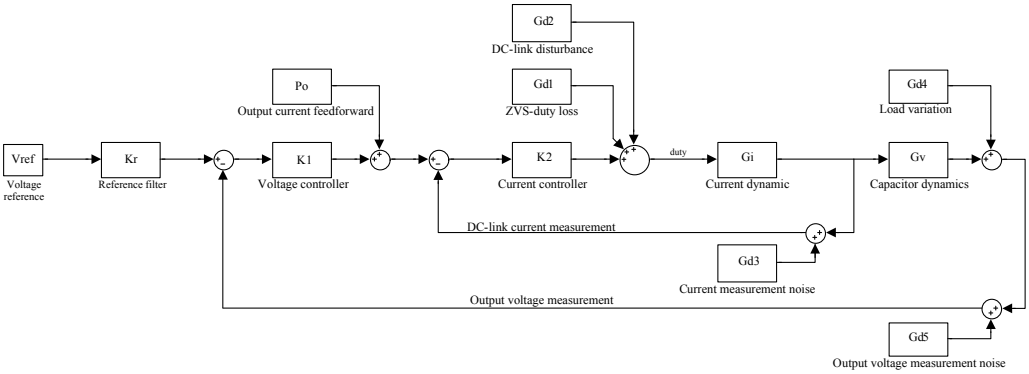

Figure 4. Full bridge control structure with feed forward paths and major disturbances shown.

The full bridge is fed with DC link voltage with the sinusoidal disturbance, as presented above. The level of disturbance in DC link voltage is dependent of the load of the converter, which also affects to the fluctuations in the output voltage. The full bridge control is required to cancel the DC link voltage disturbance as effectively as possible from the converter output voltage. Regardless of the used control method, the DC link voltage fluctuation effect can not be completely removed from the output without the inclusion of feed forward from the disturbance. The full bridge voltage controller is implemented by using PI control structure form. The controller parameters are presented in Table I.

The full bridge current control is designed by using robust control approach. The robust control is used as the system has uncertainties due to reactive component tolerances and basic operation of phase shifted full bridge. Uncertain dynamics include the duty cycle loss which is relative to I_s [1], which also affects on the inductance decrease of the output inductors.

The full bridge current control is designed with Glover-McFarlane loop shaping method, [24]. The method is a two-stage process. First, the open loop system singular values are shaped with a weighing function in order to have desirable frequency domain characteristics and then the weighted system is robustified in the face of plant perturbations. This process often yields a controller of very high order and for the ease of implementation model reduction techniques can be employed. The calculated controller was initially of 8th order for which a 4th order hankel norm approximation yielded a satisfactory response. Bode diagrams of the closed loop system with both 8th and 4th order controller are shown in Figure 5 along with discretized 4th order system. The discretized controller achieves same gain and phase margins as the 8th order system and their closed loop frequency characteristics are similar enough that the reduced order controller was used. The 4th order controller is implemented by using two second order transposed direct form II controller in cascade. Controller zeros and poles are presented in Table I.

Table I. Parameters in used controllers in continuous time domain. The controller with presented zeros and poles are discretized with the method presented.

Controller	Zero(s)	Pole(s)	Discretization method	Execution frequency
PFC voltage	14	0	Backward Euler	50 kHz
PFC current	20000	0	Backward Euler	50 kHz
Full bridge voltage	4600	0	Backward Euler	50 kHz
Full bridge current	-7914	0	Tustin	50 kHz
	-2770	-60002		
	-993	-3355		
	-356	-274		

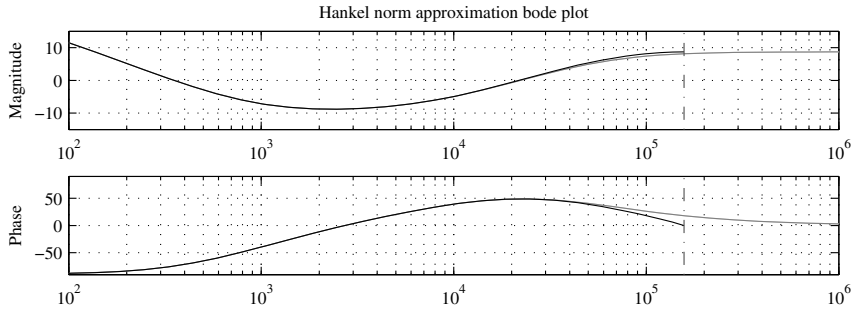

Figure 5. Comparison of closed loop bode diagrams with 8th and 4th order continuous controller (grey) and discretized 4th order control (black). The 8th and 4th order continuous controllers are in practice similar. The differences are visible only when the 4th order controller is discretized.

Experimental results

The designed SMPS centralized control system operation is verified with a practical system. The designed centralized control method viability is analyzed by evaluating the input power factor correction and full bridge control performances. The measurements are done by using Yokogawa PZ4000 power analyzer, Agilent Technologies N2781A 150A/10MHz current probes, Agilent DSO 6104A oscilloscope and Tektronix PS5210 differential voltage probes.

The PFC control performance is analyzed by using the power analyzer. The power factor is measured with loads from 5 % to 100 % of the converter nominal 3 kW power. The measured power factors are presented in Figure 6.

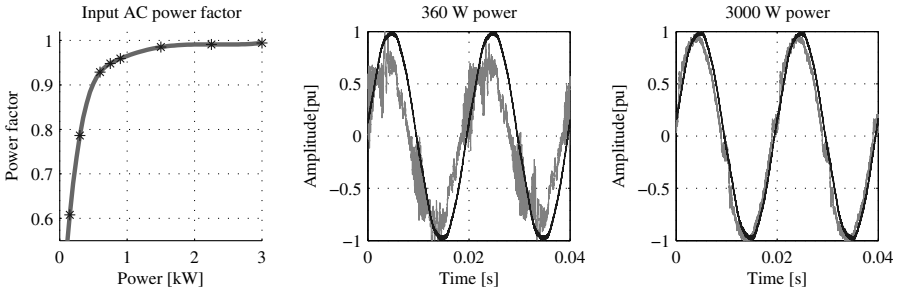

Figure 6. The performance of PFC with varied power levels. The figure in the left presents the input power factor in function of output power. The figures in the middle and right show the normalized input AC voltage (black) and current waveforms (gray) with 360 W and 3000 W output power respectively. The voltage is normalized with the measured peak value of input AC voltage 335.6 V. The currents are normalized with peak values of AC currents, 4.0 A and 22.0 A respectively. Current distortion and phase shift decreases when the output power is increased.

The Figure 6 shows that lower than 0.9 power factor exists in power levels of $< 20\%$ of 3 kW. The power factor behavior is affected by heavy EMI filtering on the SMPS input stage, which introduces phase lead in the current and distorts the current waveform. The effect of the EMI filter on current distortion and phase is constant, since by increasing the output power over 50% of the nominal, the system power factor increases up to 0.99.

The power supply full bridge control steady state performance can be analyzed with output voltage ripples. The voltage ripple is caused by sinusoidal disturbance in DC link of which effect can be minimized with properly designed control. The output voltage ripples and DC link voltages are presented in Figure 7.

The voltage ripple at the output is dependent on the DC link disturbance since the current controller can not follow the reference accurately. The phase lag between the current and the reference is caused by slow dynamics of the designed controller, hence ripple in the output voltage is introduced. The phase shift between the actual current and the reference increases in function of output power as can be seen in the reference waveforms in Figure 7.

The control dynamic performance of the full bridge controller is analyzed with voltage step at the output from 0 to 24 V and by stepping load up and down at the system output. In the Figure 8 the output voltage and load steps are presented.

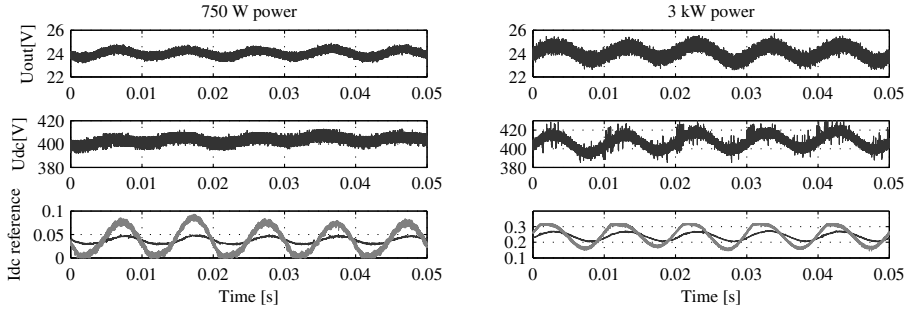

Figure 7. DC link voltage and output voltage behavior of the SMPS with 750 W and 3 kW output power. Also the current controller reference with gray and DC current with black is represented in the lowest two figures. The output voltage behavior is dependent on the current controller performance.

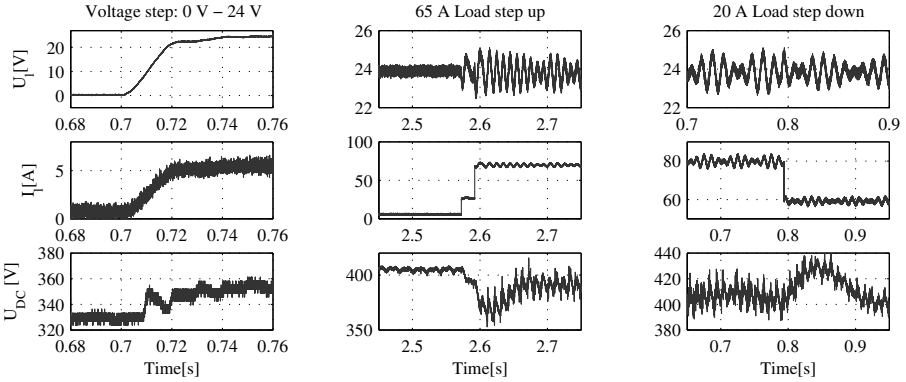

Figure 8. Output voltage with load current and DC link voltage behavior in various dynamical situations. The first figure represents voltage control dynamics when the output voltage is stepped at startup from 0 to 24 V. The figures in the middle and right represent the control dynamical performance in load step situations.

The output voltage step response rise time is limited to achieve 90% of the maximum in 20 ms as can be seen from Figure 8. This is done in order to prevent the charge current at the system input exceed the nominal input current of the system. The limitation is implemented by low pass filtering the voltage reference given to the full bridge voltage controller. The full bridge controller dynamic performance in load changes can be analyzed with the waveforms in the middle and right of the Figure 8. The maximum load step up and down is limited due to DC link voltage measurement limitations of the hardware. The system maximum load step down is 20 A and 65 A up with nominal output voltage.

The load step performance is mostly determined by the system measurement signal conditioning performance. In this experimental setup the PFC voltage control dynamical performance was reduced so that DC link measurement signal noise does not have an effect on the controller. The reduced dynamics have an effect on system control performance on both, load steps up and down. An increasing load step causes voltage drop in the DC link as presented in the middle waveforms in Figure 8. With load step up >65 A the DC link voltage drops low enough to saturate PFC controller, hence the controller loses the ability to control the DC link voltage. This peaks the input current over the allowed range. When the load is stepped down, the input power does not follow the output power fast enough. The excess energy taken from the AC input during the voltage controller settling time is stored to DC link and hence the DC link voltage increases. With load step of 20 A down, the DC link voltage increases over the allowed range with the used controller.

IV Conclusions

In this paper a digital system control for SMPS by using centralized controller is presented. The hardware of the system consists of a parallel boost PFC stage feeding power to the DC link. A phase shifted full bridge converter with synchronous rectification is used for regulating the output voltage to 24 V. All the system controls are implemented

on a combination of MCU and FPGA. A cascaded control structure method was used for both, PFC and full bridge control. Robust output characteristics are achieved by using Glover-McFarlane loop shaping method in the current control of full bridge. The centralized controller design is verified with experimental tests.

A review on controller suitable for centralized control approach was presented. The choice for the controller is dependent on multiple variables: the system overall costs, design flexibility, needed peripherals, software code portability, PCB area available or the estimated life span and sourcing of the controller.

The experimental tests show that digital control is an option for the SMPS control, especially when more complex control algorithms are applied. Although the digital control system can be used to estimate parameters, the control is dependent on the measurement signal quality. Therefore the signal conditioning should be put effort as much as the choice for suitable controller when designing a centralized digital control system.

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ISBN 978-952-335-547-7
ISBN 978-952-335-548-4 (PDF)
ISSN-L 1456-4491
ISSN 1456-4491
Lappeenranta 2020