Lappeenranta-Lahti University of Technology LUT
School of Engineering Science
Computational Engineering and Technical Physics
Technical Physics

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SILICON PIN-DIODES WITH GATE INDUCED PASSIVATION - FABRICATION AND CHARACTERISATION

Master's Thesis

Examiners: Prof. Panja Luukka
M. Sc. (Tech.) Markku Kainlauri

Supervisors: M. Sc. (Tech.) Markku Kainlauri

ABSTRACT

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72 pages, 45 figures, 11 tables.

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Keywords: silicon PIN diode detector, induced junction, Al_2O_3 passivation

Silicon PIN diode has been common and efficient configuration for detector purposes for long time. In order to reduce the dead layer on top of the detector, PIN diodes with induced passivation were fabricated and characterised. The induced junction was created on n-type high resistivity silicon by taking advantage of field effect passivation achieved with charged oxide, Al_2O_3 in this case. Gates were fabricated on top of the diodes to control the charge on the silicon surface. Two transparent gate materials were tested: graphene and indium tin oxide (ITO). The gated diodes were compared to other types of diodes fabricated on the same wafers. The diodes were characterised with four measurement techniques: current-voltage (IV), capacitance-voltage (CV), transient current technique (TCT) and radiation measurements. In IV measurement it was demonstrated that it is possible to change the state in the diode with gate biasing. The leakage current level was few $\mathrm{nA\,cm^{-2}}$ and the detectors showed response to visible light and gamma radiation.

TIIVISTELMÄ

Lappeenrannan-Lahden teknillinen yliopisto LUT
School of Engineering Science
Laskennallinen tekniikka ja teknillinen fysiikka
Teknillinen fysiikka

Tarusisko Hirvenoja

PII PIN-DIODIT HILAINDUSOIDULLA PASSIVOINNILLA - VALMISTUS JA KARAKTERISOINTI

Diplomityö

2021

72 sivua, 45 kuvaa, 11 taulukkoa.

Tarkastajat: Prof. Panja Luukka
DI Markku Kainlauri

Hakusanat: pii PIN diodi ilmaisin, indusoitu liitos, Al_2O_3 passivointi

Pii PIN diodi on ollut yleinen ja tehokas rakenne ilmaisinsovelluksissa jo pitkän aikaa. Ilmaisimen pinnalla olevan kuolleen kerroksen ohentamiseksi valmistettiin ja karakterisoituun PIN diodeja indusoidulla passivoinnilla. Indusoitu liitos valmistettiin n-tyypin korkean resistiivisyyden piille hyödyntäen varautuneen oksidin, tässä tapauksessa Al_2O_3:n, aiheuttamaa kenttäpassivointia. Diodien päälle valmistettiin hilat, joilla oksidin varausta voidaan säädellä. Kahta läpinäkyvää hilamateriaalia testattiin: grafeenia ja indiumtinaoksidia (ITO). Hilallisia diodeja verrattiin muihin diodityyppeihin samoilla kiekoilla. Diodeja karakterisoitiin neljällä eri mittaustekniikalla: virta-jännite (IV), kapasitanssi-jännite (CV), muutostilan virtaa mittaavalla menetelmällä (TCT) ja säteilymittauksilla. IV mittauksilla osoitettiin, että diodin tilaa on mahdollista muuttaa syöttämällä jännitettä hilaan. Vuotovirran taso oli muutamia $\mathrm{nA\,cm^{-2}}$ ja ilmaisimet osoittivat vastetta näkyvälle valolle ja gammasäteilylle.

PREFACE

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Espoo, October 4, 2021

Tarusisko Hirvenoja

CONTENTS

LIST OF ABBREVIATIONS 6

LIST OF SYMBOLS 7

1 INTRODUCTION 9
- 1.1 Background . . . 9
- 1.2 Objectives and delimitations . . . 9
- 1.3 Structure of the thesis . . . 11

2 BASICS OF SEMICONDUCTOR DETECTORS 12
- 2.1 Semiconductor materials . . . 12
- 2.2 PN-junction . . . 14
- 2.3 PIN diode as radiation detector . . . 16
- 2.4 Induced junction . . . 17
- 2.5 Gated diode . . . 19
  - 2.5.1 Graphene . . . 20
  - 2.5.2 Indium tin oxide (ITO) . . . 21

3 DIODE FABRICATION 22
- 3.1 Methods . . . 22
  - 3.1.1 Lithography . . . 22
  - 3.1.2 Image reversal . . . 23
  - 3.1.3 Graphene transfer . . . 25
- 3.2 Devices . . . 26
- 3.3 Processing . . . 28
  - 3.3.1 Graphene gate . . . 31
  - 3.3.2 ITO gate . . . 35

4 DIODE CHARACTERISATION 37
- 4.1 Current - voltage (IV) . . . 37
  - 4.1.1 Measurement . . . 37
  - 4.1.2 Results and discussion . . . 43
- 4.2 Capacitance - voltage (CV) . . . 54
  - 4.2.1 Measurement . . . 54
  - 4.2.2 Results and discussion . . . 57
- 4.3 Transient current technique (TCT) . . . 58
  - 4.3.1 Measurement . . . 58
  - 4.3.2 Results and discussion . . . 61

4.4 Radiation . . . 62
4.4.1 Measurement . . . 62
4.4.2 Results and discussion . . . 64

5 CONCLUSIONS 67

REFERENCES 68

LIST OF ABBREVIATIONS

Al_2O_3	aluminum oxide
ALD	atomic layer deposition
BOE	buffered oxide etch
CSA	charge sensitive amplifier
CV	capacitance-voltage characteristics
CVD	chemical vapor deposition
DIW	deionized water
EQE	external quantum efficiency
FWHM	full width at half maximum
Gr	graphene
HIP	Helsinki Institute of Physics
IPA	isopropanol/2-propanol
ITO	indium tin oxide
IV	current-voltage characteristics
LCD	liquid crystal display
LED	light emitting diode
MCA	multichannel analyzer
MIC	metal ion containing
MIF	metal ion free
MOS	metal-oxide-semiconductor
NaOH	sodium hydroxide
OLED	organic light emitting diode
PCB	printed circuit board
PIN	structure of p-type layer, intrisic layer and n-type layer
PMMA	polymethyl methacrylate
SiN_x	silicon nitride
SiO_2	silicon dioxide
SMU	source measurement unit
TCT	transient current technique
UV	ultraviolet
VMU	voltage measurement unit

LIST OF SYMBOLS

A	area
C	capacitance
E_g	energy
E_F	Fermi energy
E_g	energy of band gap
E_i	ionization energy
ε	total permittivity
ER	energy resolution
I	current
J_{bulk}	current density in the bulk
$J_{surface}$	surface current density
λ	wavelength
N	charge density
P	perimeter
q	charge of an electron
R_C	contact resistance
R_S	sheet resistance
R_T	total resistance
V_{bias}	bias voltage
V_{FB}	flat band voltage
V_{fd}	full depletion voltage
V_G	gate voltage
V_T	threshold voltage
W	width
w	capacitor thickness

1 INTRODUCTION

1.1 Background

Semiconductor industry is nowadays very large and silicon has been the main enabler for that. Silicon detectors have been developed for decades, the goal being to fabricate detectors with smaller leakage current and thinner dead layers to maximise the radiation response. The main problems with silicon detectors are radiation damage and performance degradation, but the small size, good energy resolution and fast detection have been the driving forces to develop detectors to overcome the problems [1].

In this thesis the process of fabricating and characterization of gated induced junction silicon diode detectors is described. Induced junction works like pn-junction but instead of doping it is based on field effect passivation. The inversion layer is created with charged oxide which attracts minority charge carriers in semiconductor bulk to the surface. Induced junction photodiode and the working principle of induced junction was first time reported in 1978 [2]. The gate is a conductive material deposited on top of the diode active area which is biased to control the inversion layer in the semiconductor.

The motivation for the fabrication of these diodes was testing out passivation techniques with induced junctions and gates. For gates, graphene and indium tin oxide (ITO) were chosen. The advantage of using induced junction is minimizing the dead layer on top of the active area of the detector. Dead layer consists of everything that is on top of the active area (in this case silicon bulk). Problem with dead layer is that it absorbs some of the radiation entering the detector but does not act as a detecting medium. Thick dead layer can cause significant energy loss [1]. The passivation layer is only tens of nanometers thick and there is no dead layer in form of doped area. To minimize the thickness of dead layer, the gate materials were chosen to be as thin as possible. Graphene is only one atom layer thick which means it should not suppress the radiation entering the detector like thicker metal layer would.

1.2 Objectives and delimitations

The main goal of this thesis is to find out if the gate gives an advantage on the operation of the induced diode detector. A set of four wafers is fabricated, each of them having slightly different back-end processing steps (or no back-end processing at all). The wafer

design includes five different types of diodes that can be compared to each other. Gates are fabricated on two wafers to test two different gate materials. For gate materials, testing graphene (Gr) was the main interest and the wafer with indium tin oxide (ITO) gates was fabricated to be a reference for that. Both gate materials are transparent which allows testing the detectors with visible light.

The induced junction is based on the oxide having a strong charge that induces an inversion layer into the silicon surface. The inversion layer is comparable to pn-junction made with traditional doping of silicon. Usually the induced junction is created by having lightly doped wafer with majority charge carriers having the same charge than in the oxide. Most common combinations are p-type silicon and SiO_2, and n-type silicon and Al_2O_3. In this thesis the focus is on the latter one.

When a gate electrode is deposited on top of the charged oxide, the electrode can be biased to cancel or to boost the charge in the oxide and that way change the state of the induced layer. The focus in the measurements was to observe the effect of gate biasing for detector operation.

In this thesis the whole process of fabricating the diodes is described, starting from the silicon wafers and continuing into characterisation of the final devices. The design and structure of diodes is already defined because front-end processing is already done. Front-end processing steps include the fabrication of the diodes with metal contacts and back-end processing includes the gate fabrication. The fabrication is done in VTT Micronova cleanroom in Espoo.

The characterisation includes four types of measurements: current-voltage (IV), capacitance-voltage (CV), transient current technique (TCT) and radiation. The first two, IV and CV, focus on measuring the detector properties in the dark to get an idea about the leakage current of the detector. The latter two (TCT and radiation) focus on the detector operation with different radiation sources: visible light (red laser) in TCT and gamma rays in radiation measurements.

The main focus for characterisation is on IV measurements. Large number of different types of diodes are measured from several wafers to be able to compare and find out the differences. Having several wafers that have same design will show the differences caused by differences in fabrication steps. Being able to measure different types of diodes from same wafer will be good for comparing different diode types. Majority of IV measurements is done at VTT Micronova in Espoo.

CV, TCT and radiation measurements are done at Helsinki Institute of Physics (HIP) Detector Laboratory at Kumpula campus of University of Helsinki. For these measurements only limited amount of diodes are measured, the focus being in the induced junction diodes with gate. In TCT and radiation measurements the focus is to check that the diodes actually work as detectors, and possibly get an idea about how good detectors they are or how the design could be improved.

1.3 Structure of the thesis

The thesis starts with description of most important properties of semiconductors and description of semiconductor detectors in chapter 2. In the chapter 3 most important techniques and the fabrication process are described. The chapter also includes fabrication results. Chapter 4 focuses on electrical characterisation of components fabricated in previous section. Four different types of measurements are described: current-voltage (IV), capacitance-voltage (CV), transient current technique (TCT) and radiation. Each measurement type is presented as its own section, starting with description of the measurement technique and setup and then moving into the results and discussion. In chapter 5 the conclusions from the results are given.

2 BASICS OF SEMICONDUCTOR DETECTORS

Semiconductor materials are the basis of the microelectronics industry and also very important materials for solid state detectors. In detector applications, semiconductor detectors have several advantages: their energy resolution is remarkably better when compared to other types of detectors (gas filled or scintillation detectors), they are small, size can be varied and the detection is fast. These properties make semiconductor detectors good for radiation detection. Of course, like all detectors, also semiconductor detectors have properties that make them non-ideal, like performance degradation and radiation damage after long term use. [1]

In this section the basic properties of semiconductors and semiconductor detectors are discussed, starting from properties of semiconductor materials and from there moving to pn-junctions and semiconductor detector structures.

2.1 Semiconductor materials

The electrical properties of solid state materials are based on the material energy band structures. Energy bands are based on quantized electron energies: electron energy must be on allowed energy level. When considering semiconductors, three bands are important: valence band, conduction band and forbidden gap between previous two. Electrons can only be in valence band or in conduction band. Solid state materials can be divided into three categories based on their energy band structures: metals, insulators and semiconductors.

Metals conduct electricity well because there is no band gap between valence band and conduction band, and electrons are free to move. In insulators and semiconductors the outer shell electrons are in the valence band and their movement is restricted by forbidden gap. Insulators are very poor conductors, because the energy gap is wide (at least 5 eV). That means that electrons need to gain high energy to be able to move from valence band into conduction band. Semiconductors also have a band gap, but it is considerably lower than for insulators, around 1 eV, depending on the material. Semiconductor energy band structure is shown in figure 1, taking also the core energy band into account. Low band gap means that it is easier for electrons to move to higher energy states than it is in insulators. The conductivity of semiconductor materials is limited when compared to metals as the movement of electrons is restricted because of the band gap. [1]

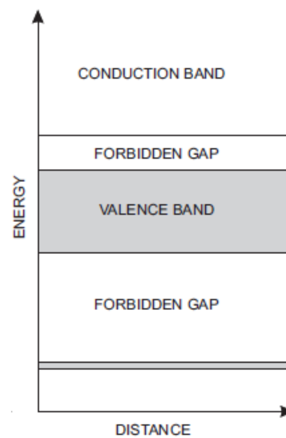


Figure 1. Energy band structure in semiconductors. From [3].

Most commonly used semiconductor materials in detector applications (and overall in any semiconductor applications) are silicon (Si), germanium (Ge) and gallium-arsenide (GaAs). Many other materials are also researched but none of them have reached the same popularity as those three. Silicon and germanium both have diamond lattice structure and have four valence electrons, which means that they belong to group IV in the periodic table. The valence electrons forming covalent bonds with neighboring atoms are the basis for doping. [3]

Valence electrons in covalent bonds can be excited from valence band into the conduction band. This excitation can happen thermally or by radiation, such as visible light or charged particles. When a valence electron moves up to a conduction band, it leaves behind a vacancy in the valence band. That vacancy is called hole. Electrons and holes are the charge carriers in semiconductor materials, electron having a net negative charge and hole having a net positive charge. When electron moves from valence band up to conduction band, it forms an electron-hole pair. Formation of electron hole pairs is the basis for semiconductor detector operation. Electron-hole pairs can form at any non-zero temperature but they are more likely to happen if an electric field is present. Without electric field the thermally excited electron-hole pairs recombine leading to equilibrium. [1]

The previous descriptions are about intrinsic semiconductors, pure semiconductor materials without any impurities or dopants. In intrinsic semiconductors the density of charge carriers is relatively low (about $10^{10}\,\mathrm{cm}^{-3}$ in silicon in room temperature [1]). To improve the conductivity of the material, dopant materials can be added into the semiconductor material. Depending on what type of charge carriers are wanted, dopant materials for silicon are from either group III or group V elements from the periodic table. After doping the majority charge carrier concentration can be several magnitudes higher compared to

intrinsic semiconductor ($10^{12}\,\mathrm{cm}^{-3}$ to $10^{18}\,\mathrm{cm}^{-3}$ [3]) and the minority charge carrier concentration is several magnitudes lower compared to intrinsic charge carrier concentration.

Elements from group III have three valence electrons, one less than silicon. Semiconductor doped with group III element is called p-type as the majority charge carriers are holes with a positive charge. Group V elements have five valence electrons which means that after forming a bond with silicon there is one extra valence electron. Material doped with group V atoms is called n-type because majority charge carriers are electrons with a negative charge. The most common material used for p-type doping is boron (B) and for n-type doping it is phosphorus (P). The free charge carriers form their own level inside the forbidden band. In the case of p-type material this acceptor level is close to valence band and in the case of n-type material the donor level is close to conduction band. The electrons in these levels are more loosely bound to atoms and can move more freely in the material.

Another parameter related to band gap structure is Fermi energy, E_F. Fermi energy tells about the chemical potential in the material. In intrinsic semiconductor the Fermi level is in the middle of the forbidden gap in between valence and conduction bands. With doping the Fermi level moves closer to the formed acceptor or donor level. [3]

The energy needed to excite electron from valence band into conduction band depends on the band gap energy of the material. That energy can be approximated from

$$E_i \approx 2.6E_g + 0.6\text{ eV}, \tag{1}$$

where E_i is the ionization energy and E_g is the size of band gap. Silicon band gap is $1.12\,\mathrm{eV}$ and the energy needed to excite an electron from valence band into conduction band is $3.6\,\mathrm{eV}$. For detector applications low ionization energy is an advantage because it allows detecting particles with lower energies. For many other types of detectors, like scintillators or gas detectors, excitation energies are tens of eV. [1], [3]

2.2 PN-junction

Joining together n- and p-type semiconductor materials forms a pn-junction which is the basis for semiconductor detector operation. When parts with different types of charge carriers are joined together, automatically the free charge carriers are attracted to the opposite side where they recombine. That creates an area with fixed charges to both sides

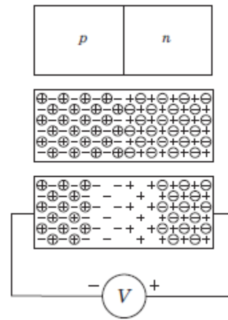


Figure 2. Pn-junction and formation of the depletion region in reverse biased pn-junction. From [3].

of the junction called depletion region. Depletion region is always formed when the pn-junction is present, but it can be controlled by applying voltage to the junction. When positive voltage is applied to p-type material and negative to n-type the current flows freely through the junction. This is called forward biasing. In detector applications the junction is biased to have negative potential to p-type side and positive potential to n-type side of the junction. This is called reverse biasing and is shown in figure 2.

The energy band structure in different biasing schemes is shown in figure 3. Without applied voltage between differently doped regions the potential difference is equal to the built in potential and the energy bands have bent to create constant Fermi level. When forward bias is applied, the band bending is decreases. That means that the potential difference between valence and conduction bands is smaller than the built in potential. In the case of reverse bias the energy bands bend even further, compared to thermal equilibrium. That leads to depletion region extending further as the potential difference on different sides of the junction increases. [3]

In reverse biasing the width of the depletion region is increased as the free charge carriers are attracted to opposite side of the junction. In reverse biased mode the depletion region acts like a capacitor because the resistance of the depletion region is high. When radiation entering the detector creates electron-hole pair, the charge carriers are quickly collected to opposite sides of depletion region. Detector operated in reverse biased mode, without any radiation present, has very low current flow. The current getting through the reverse biased detector is called leakage current. Minimizing the leakage current is important part of the detector design and fabrication, as it should be remarkably lower compared to measured signal. [1], [3]

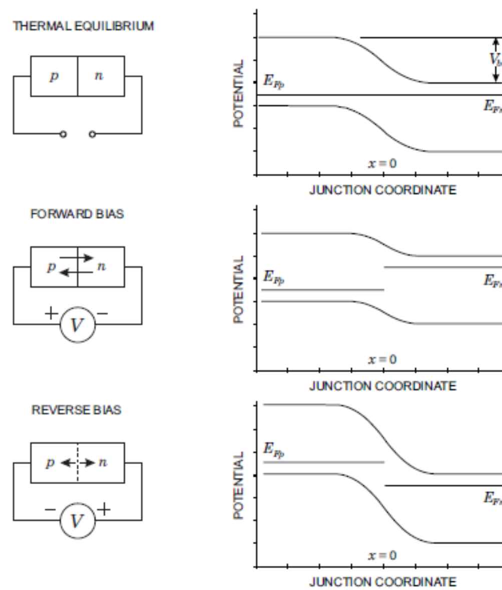


Figure 3. Energy bands inside the pn-junction in different biasing schemes. From [3].

2.3 PIN diode as radiation detector

PIN diode is a common structure for semiconductor detector applications. Basically PIN diode is heavily p- and n-doped layers with an intrinsic bulk layer between them. Technically it is not possible to have completely intrinsic silicon and because of that the bulk is lightly n- or p-doped. In figure 4 is shown the basic PIN diode structure with n-type silicon bulk. The detector entrance is in the middle of the topside (junction contact in fig. 4) and on both sides of that junction are shown smaller junctions, called guard ring. The role of guard ring is to prevent unwanted current from substrate edges from entering the detector. The guard ring and the contact to the front side of the junction (anode in case of p+ doping) are biased to the same potential. The active area of the detector is the bulk between doped layers. The active area extends to about halfway through the space between junction contact and guard ring.

The entire backside of the detector is coated with metal to create ohmic contact. For measurements or detector operation, the bias is supplied to the detector from the backside. Depending on the type of used material, the junction contact and guard ring are set to either higher or lower potential than the backside.

As was already mentioned in previous section, semiconductor detectors are operated in reverse biased mode, often biased to have the depletion region to reach through entire bulk (fully depleted). The full depletion voltage V_{fd} is important parameter for detectors as it defines in what voltage range the detector can be operated. The full depletion voltage of

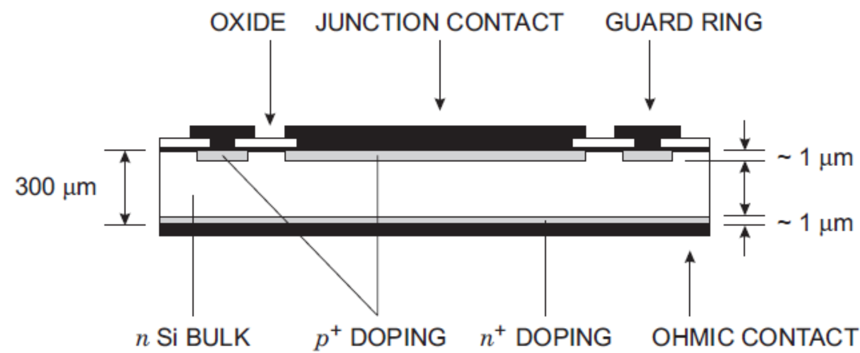


Figure 4. Structure of basic PIN diode detector. From [3].

the detector depends on the quality of the substrate. For high resistivity wafers with only small amounts of impurities and low doping concentration the full depletion voltage is lower than for wafers with lower resistivities. Common resistivities for detector applications are 1-10 $\mathrm{k\Omega\,cm}$. [4] In figure 4 the detector thickness is shown to be $300\,\mu\mathrm{m}$, which is common thickness for silicon detectors because the V_{fd} does not become too high with resistivities $<5\,\mathrm{k\Omega\,cm}$.

PIN diode can be used to detect different kinds of radiation, like charged particles or visible light. The energy needed to create one electron-hole pair in silicon is approximately $3.6\,\mathrm{eV}$, as was mentioned earlier. Charged particle passing through the detector will create several electron-hole pairs which are swept by applied electric field to edges of the detector where the charge carriers induce a current into the metallic contacts. The detection is most efficient when detector is operated in fully depleted mode as then the entire silicon bulk will act as detecting media and the electric field extends through the entire wafer, making collection of the charge carriers more efficient. When the purpose is to detect visible light, the materials and the thickness of dead layer become more important because of the short wavelength and low energy of photons. Photon energy is enough to create only one electron hole pair after entering the detector. [1], [3]

2.4 Induced junction

Silicon surface passivation has been important part of any semiconductor device processing for several decades. In induced junction the passivation is utilized to create inversion layer to reduce the dead layer on top of the detector active area. The most common way to achieve surface passivation is by depositing thermal SiO_2 layer on the wafer to prevent the surface recombination losses. The SiO_2 surface passivation is based on reducing

the density of states at the Si-SiO_2 interface. With materials with higher fixed charge the passivation is based on field effect passivation. Materials with high fixed charge are Al_2O_3 (large negative fixed charge, $10^{12}\,\mathrm{cm}^{-2}$ to $10^{13}\,\mathrm{cm}^{-2}$ after annealing [5], [6]) and silicon nitrides (SiN_x, large positive charge). [7] The charge in SiO_2 is lower, $10^{10}\,\mathrm{cm}^{-2}$ to $10^{12}\,\mathrm{cm}^{-2}$ after annealing [8], [9].

Induced junction is like traditional pn-junction but instead of doping the junction is formed by having charged oxide induce an inversion layer to the surface of the substrate. The first induced junction photodiode was introduced by Hansen in 1978 [2]. They presented a way to create n-type inversion layer to p-type silicon wafer using SiO_2. The positive charge in SiO_2 attracts electrons to the surface and when the electron concentration at the surface is equal or larger than the hole concentration in the bulk, inversion layer can be formed. Ohmic contact to the inversion layer is created by having a doped ring around the active area (n+ doping in the case of p-type silicon). [2]

The early publications about induced junction diodes focused on p-type substrates and SiO_2 passivation. As the induced junction needs the charged oxide have same charge as majority charge carriers in semiconductor bulk, forming inversion layer with SiO_2 does not work in a same way for n-type silicon substrates. Induced junction photodiodes using n-type silicon wafer as a substrate were reported by Juntunen *et al.* [10]. They used Al_2O_3, which has large negative charge, to create the induced junction. To increase light collection efficiency the surface of their photodiode was nanostructured to have black silicon underneath the Al_2O_3. Alpha particle detector utilizing Al_2O_3 induced junction was presented in recent master's thesis with promising results [11].

The advantage of induced junction is thinner dead layer (compared to traditional pn-junction) which means that less radiation is absorbed in it. The thickness of dead layer is critical for detecting UV-light due to short wavelength. External quantum efficiency (EQE) is parameter for presenting the quality of a photodiode, it is defined as a ratio between collected charge carriers and the photons incident to he device. Induced junction photodiodes are reported to have good response on wide range of visible light wavelengths (200-1000 nm) and especially in UV range ($<400\,\mathrm{nm}$) [2], [10]. The induced junction photodiodes with black silicon were reported to have EQE over $96\,\%$ over entire visible light spectrum without applying bias [10]. Another issue with UV photodiodes has been the degradation of the detector after long exposures to UV radiation. Induced junction detectors have been shown to handle well the exposure to UV radiation [12], [13].

2.5 Gated diode

In gated diode additional metal (or other conductive material) layer is added to the diode. By biasing the gate the surface states of the diode can be changed. The operation of gate is based on having surface passivation and controlling the field effect passivation with the voltage applied to the gate. Diodes with gates has been utilized for studying the leakage current and extracting different components of the leakage current since 1960s [14]. The gate on diodes used for leakage current analysis has been on the edges of the traditional pn-junction and the gate is used to create inversion layer that continues further in the silicon surface than the original junction. For that kind of gated diode operation the diode is in accumulation state until the gate bias is large enough to create inversion layer. This kind of gated structure with gate on the sides of the junction is tested with PIN structure for radiation detection [15], [16].

With induced junction the basic of operation is same as described above, and the gate is placed on top of passivating oxide, in the case of this thesis Al_2O_3 layer. The structure is similar to MOS-capacitor (metal-oxide-semiconductor). But because the junction in the active area is now induced junction instead of doped, the gate is used to control the state of the induced junction. When voltage is applied to the gate, depending on the polarity and magnitude of the bias there are three possible states for the MOS capacitor; accumulation, depletion and inversion. These states are basically same also for the gated diode.

As the three layers of MOS structure are joined together, all materials have different potentials or charges. That causes bending of the band gaps which leads to different states. At certain voltage the Fermi level is uniform through all three layers. The voltage used to achieve this condition is called flat band voltage (V_{FB}) and it can be used to determine the three other states. [17] The states are

1. accumulation ($V > V_{FB}$)
2. depletion ($V_{FB} < V < V_T$) and
3. inversion ($V << V_{FB}, V < V_T$).

V_T in threshold voltage between depletion and inversion. In accumulation the gate voltage is higher than the flat band voltage which means that the majority charge carriers are attracted to the surface of the semiconductor. The depletion happens when the gate voltage has the same polarity as the majority charge carriers attracting the minority charge carriers

into the semiconductor surface. When the gate voltage is large enough to attract minority charge carriers to the surface in such large population that an inversion layer is formed, the diode is in inversion. [4], [17]

The oxide considered for MOS capacitors is often SiO_2, which has relatively low charge, especially when compared to doping concentrations or to charge in the Al_2O_3. In the case of Al_2O_3 with n-type silicon the inversion layer is strong even without applying voltage. The oxide charge and the thickness of the oxide have an effect to the threshold voltage V_T.

Two materials were tested for gates for induced junction diodes: graphene and indium tin oxide (ITO). The main criteria for choosing these materials were their transparency and the minimal thickness to reduce the dead layer. Both properties are important for detecting visible light.

2.5.1 Graphene

Since single layer graphene was first time demonstrated in 2004 [18], it has gained huge amounts of attention because of its unique properties. Graphene is only one atom layer thick with honeycomb lattice and it has semimetal properties with slight overlap of valence and conduction bands in its natural state [18]. That means that graphene has high conductivity and it can be used as an electrode in some applications but it can also be used as a semiconductor. Graphene does not have a natural band gap. Zero band gap, monolayer structure and the high mobility, $10\,000\,\mathrm{cm^2/Vs}$ [18], compared to electron mobility of Silicon ($1350\,\mathrm{cm^2/Vs}$ [1]), makes graphene attractive material to be used in semiconductor applications. Graphene has been used as an electrode and as semiconductor in many forms in different applications, like solar cells, field effect transistors (FETs), light emitting diodes (LEDs) and modulators [19], [20].

Again, the monolayer structure of the graphene makes it interesting material for diode gate material. For detector purposes minimizing dead layer on top of active area is important to keep energy absorption in dead layer in minimum [1]. Graphene is only one atom layer thick, the thickness being few Ångströms, metal gate (like Al) would add at least tens of nanometers or even more on top of the detector active area. For photosensitive devices another criteria for good gate material is optical transparency. Graphene absorbs 2.3% of white light and the absorption does not vary noticeably between different wavelengths [21]. Graphene has been successfully used as an transparent electrode in perovskite solar

cells [22], which is promising result while considering graphene for gate material.

2.5.2 Indium tin oxide (ITO)

ITO, indium tin oxide, is commonly used transparent conductive oxide. It is n-type semiconductor material that has wide band gap, about $4\,\mathrm{eV}$ (can be tuned to be higher), and low resistivity, $<10^{-4}\,\Omega\,\mathrm{cm}$ [23]. The transmittance of ITO films is $>80\,\%$ and values up to $95\,\%$ have been reported. ITO can be deposited by many different methods like magnetron sputtering, molecular beam epitaxy, thermal evaporation and pulse laser deposition. [24] It has been demonstrated that by altering sputtering parameters it is possible to change the properties of ITO film, like the optical transmittance and the conductivity [25]–[27]. The applications of ITO include flat panel liquid crystal displays (LCD), organic light-emitting diodes (OLED), solar cells and many more.

3 DIODE FABRICATION

3.1 Methods

In this section few of the most critical processing methods, photolithography and graphene transfer, are introduced. Only these two methods were chosen to be introduced in more detail, because those were the most important ones for the processing that was done for this thesis. The more technical details are given later, the purpose of this section is to give a bit more background information to those methods.

3.1.1 Lithography

Photolithography is a method that is used for creating patterns to the wafer and to protect areas that are not processed during that step. The lithography process includes spin coating, exposing and developing photoresist on the wafer. After the processing step is finished, the resist is removed. The basic lithography process is shown in figure 5.

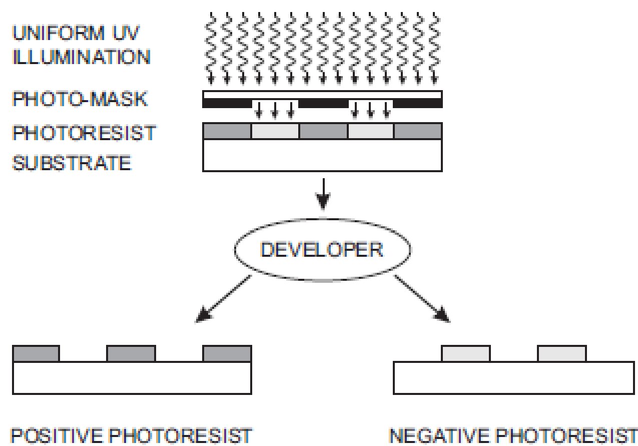


Figure 5. The basic process of lithography for positive and negative photoresists. Picture from [3].

Photoresist is photosensitive material and when it is exposed to ultraviolet (UV) light, the structures of the material change. There are two types of photoresists, positive and negative. When positive resist is exposed, it becomes easily soluble to developer. With negative resist the exact opposite happens, as the exposed resist becomes harder and non-soluble. [3]

For exposure there are several options. The most common one, and also the one used in this thesis, is using a mask aligner with mercury lamp and a mask, that has the pattern of entire wafer. Other options are using a stepper or a laser writer. Stepper also uses mask, but it is smaller and the wafer is exposed a part at the time. With laser writer the pattern is exposed pixel by pixel using laser. [28]

There are two types of photomasks: light field and dark field masks. Light field masks have the pattern made from opaque material and rest of the mask is clear. Dark field masks have the negative of the pattern, the mask is opaque and the structures are open. The polarity is chosen to fit the purpose of the mask.

After the exposure the resist is developed. Development is final step before the pattern is finished. If the resist is positive tone, the exposed parts are dissolved into developer, and with negative tone resist unexposed parts are dissolved. Development solutions are generally divided into metal ion containing (MIC) or metal ion free (MIF). MIC developers are often based on NaOH or KOH. Sodium (Na) and potassium (K) are harmful for semiconductors which means that using developers containing them should be avoided in semiconductor detector processing. Many developers attack aluminum or other alkaline sensitive materials. Because of these reasons for wafers processed as a part of this thesis the used developer was MIF type which does not attack aluminum. The development can be done by immersing wafer into a tank or a beaker filled with developer or on a track. On track based processing options are puddles or spray. The development rate ($\mu\mathrm{m/min}$) is given in developer data sheet. [29]

Two most common ways to use lithography are shown in figure 6. Etching process is shown in figure 6a. In etching process the metal deposition is done first and the resist is applied on top of it. Then the metal is etched from the resist openings, using wet or dry etching, and resist is removed. The lift-off process is shown in figure 6b. In lift-off process the patterning is done first and then the metal is deposited everywhere. After resist removal, metal that was deposited on top of the resist comes off leaving patterned metal to the wafer.

3.1.2 Image reversal

For lift-off it is possible to use image reversal technique to get undercuts to ensure best possible results after removing the resist. Image reversal resists behave like positive resists if few special steps are not taken during the lithography process. After the reversal process

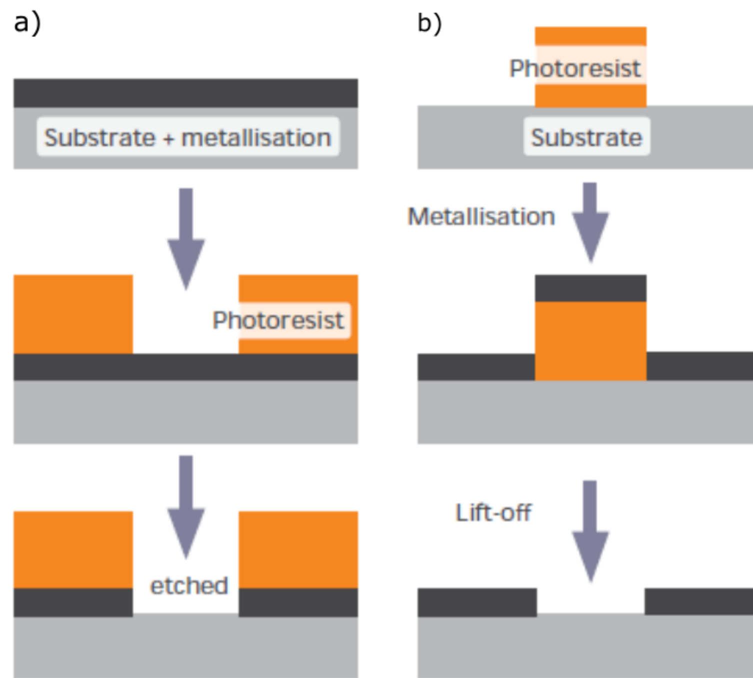


Figure 6. Two basic process flows for lithography a) wet etching and b) lift-off. Picture from [30].

the result is negative pattern. It is also possible to use normal positive or negative resist for lift-off, but the properties of image reversal resist are better for the purposes of the lift-off. The undercuts, which make the resist removal process easier, are possible only with negative or image reversal resists. Ideally, positive resists have straight sides but in practice the sides are sometimes over-developed. The purpose of undercuts is to make sure that there is some open resist after metal deposition. If all of the resist is fully covered in metal, the lift-off does not work. Negative resists form harder bonds, which means that they can handle higher temperatures, but that also means that the resist is harder to remove [30].

Image reversal has few additional steps compared to basic lithography process. In the work done for this thesis, same positive AZ 5241E resist is used for image reversal process.

Image reversal starts with resist spinning and exposure with mask. The exposure is followed with reversal bake at stable temperature. The reversal-bake is the most critical step in the process and to ensure consistent results, it is best to use hotplate. With hotplate it is easier to set temperature to right value and keep it within needed limit of ± 1°C [31] from the set temperature. The recommended reversal-bake temperature is 120 °C for 2 minutes [31], but for the work done for this thesis 110 °C for 2 minutes was found to be the most suitable. During reversal bake the exposed parts of the resist crosslink and

become unsoluable in the developer.

Another additional step in image reversal process is flood exposure. In the flood exposure the wafer is exposed to high dose of UV light. The dose can vary within range of 150-500 mJ/cm^2. The recommended dose for AZ 5214E resist is 200 mJ/cm^2. [31] After the flood exposure the wafer is developed the same way it would be without image reversal steps.

3.1.3 Graphene transfer

Chemical vapor deposition (CVD) is the most common way of growing graphene sheets on top of metal substrates, often on copper substrates. During past fifteen years many different methods have been used to transfer graphene from the growth substrate to the target substrate. Generally the methods can be divided into two categories: etching and etching-free transfer.

In etching transfer the metal substrate is etched away. Etching is done either before or after the actual transfer, depending on the method. In intact transfer graphene is protected with supporting layer. Commonly used supporting layer material is polymethyl methacrylate (PMMA) resist, which creates a flexible but mechanically strong protection layer that is easily removed with solvents. Other etching transfer method is clean transfer, in which the graphene is transferred directly from the growth substrate to the target substrate and then the growth substrate is etched away. Clean transfer methods were developed to get rid on polymer residues in graphene after transfer. [32]

In etching-free transfer the graphene sheet is peeled away from the growth substrate either mechanically or with electrochemical bubbling. Mechanical delamination is a dry method for transferring graphene. It is based on forming a bond between graphene and the target substrate. The bond can be formed either with an adhesive that stays between graphene and target substrate or with stamping method. In stamping method the graphene is first removed from the growth substrate with help of other substrate and from there it is released to target substrate. [32] In electrochemical bubbling the graphene sheet (protected with layer of PMMA) is released from the growth substrate in aqueous solution using the growth substrate as cathode. Bubbling transfer is fast method, delaminating the graphene in only seconds when etching the substrate can take hours [33]. The bubbling transfer is also reported to have graphene films free of metal contamination from the growth substrate [32].

Bubbling transfer is based on electrochemical reaction of water reduction creating hydrogen bubbles at the interface between graphene and the metal film. The graphene (usually covered with PMMA) peels off from the growth substrate and floats on top of the electrolyte. The bubbling transfer was first introduced by Wang *et al.* in 2011 [34]. They used aqueous solution of $K_2S_2O_8$ as electrolyte, CVD grown graphene on copper foil, protected with PMMA layer, as their cathode and glassy carbon as an anode. The entire process took about 60 minutes. The process was not fully etching-free as some chemical etching was observed during the bubbling process.

The first fully etching-free method was reported in 2012 by Gao *et al.* [33]. It was remarkably fast compared to bubbling process presented in [34] and to traditional etching methods, because the delamination of graphene-PMMA stack happened in tens of seconds. In the initial work, platinum (Pt) was used as the growth substrate, but the method works also with other substrate types. Aqueous solution of NaOH (sodium hydroxide) was used as electrolyte, the Pt substrate with graphene and PMMA was used as cathode and a piece of Pt foil was used as anode. The Gr-PMMA stack was cleaned with deionized water (DIW) and then transferred to Si/SiO_2 substrate. This method was the one used for graphene transfer in the work done for this thesis. The use of NaOH in bubbling might leave some traces into the graphene film which could cause some problems in the semiconductor.

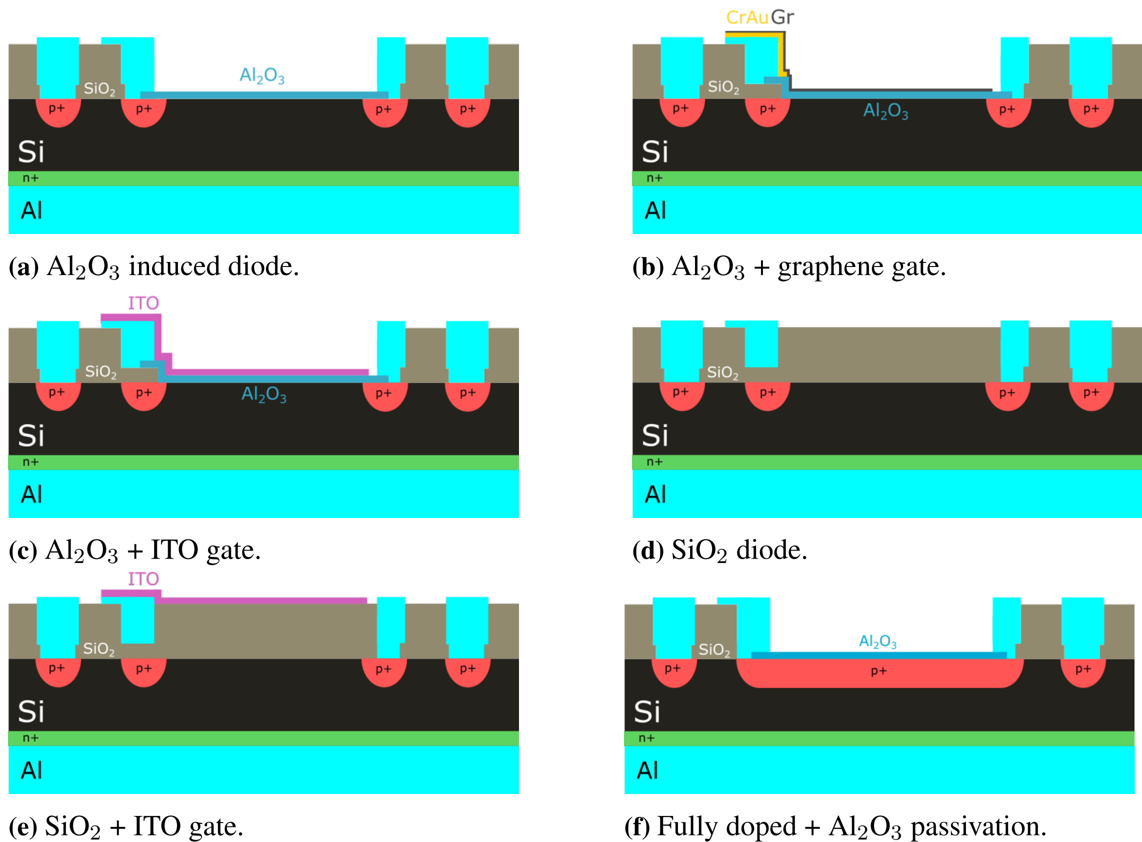
3.2 Devices

The focus of the thesis is centered around Al_2O_3 passivation, induced junctions and gated diode structure. Especially induced junctions and gated diodes are not yet very common structures for detectors, as was discussed in section 1.1. In order to have something to compare results from these more unconventional structures there needed to be also more traditional structures. For that reason there were quite many different variations included into the design.

The ”basic diode” was round diode with active area $1650\,\mu m$ active area diameter and in the design there are several variations to that diode. The variations are

- Al_2O_3 induced junction diode (fig. 7a),
- Al_2O_3 induced junction diode with gate (graphene/ITO) (figs. 7b-7c),
- field oxide (SiO_2) diode (fig. 7d),

- field oxide (SiO_2) diode with gate (ITO) (fig. 7e),
- fully Boron implanted with Al_2O_3 passivation (fig. 7f).



(a) Al_2O_3 induced diode.

(b) Al_2O_3 + graphene gate.

(c) Al_2O_3 + ITO gate.

(d) SiO_2 diode.

(e) SiO_2 + ITO gate.

(f) Fully doped + Al_2O_3 passivation.

Figure 7. Diode types that were studied in this thesis.

In order to study the source of the leakage current, a further variation to the basic diodes were diodes with different active area diameters. The basic diameter is 1650 µm and the variations were scaled up or down from that. This kind of diodes come with five different active area diameters: 850 µm, 1150 µm, 1485 µm, 2475 µm and 3300 µm. After measuring all five different sizes, it was possible to calculate the major source of leakage current (bulk or surface). The wafer design also includes different shapes of diode designs, but those diodes are not characterized in this work.

In addition to the diodes, that were the main interest in this work, the design included different types of FETs as test structures. To study the effect of gate and the contact between different layers, two types of FETs (figure 8) were measured: Al_2O_3 under the gate (fig. 8a) and SiO_2 under the gate (fig. 8b.

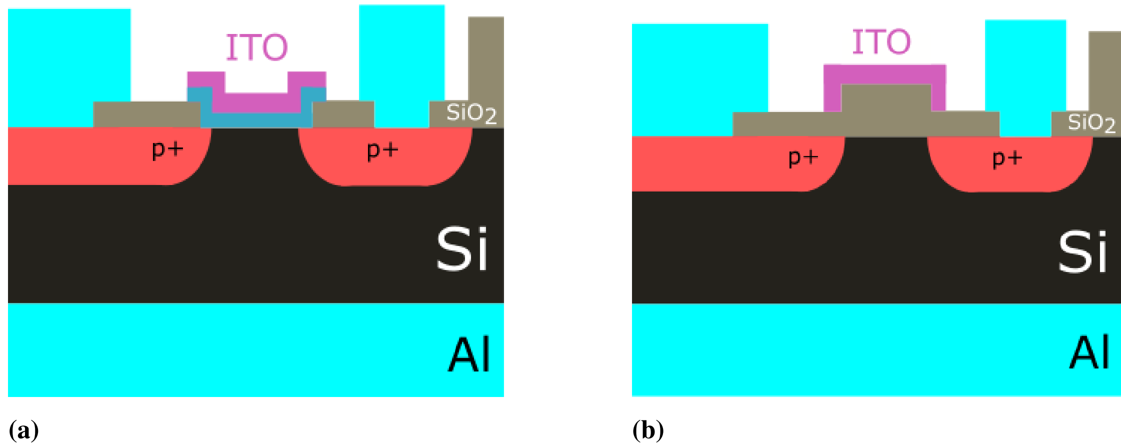


Figure 8. Cross sections of FET test structures a) Al_2O_3 passivation, b) with SiO_2.

3.3 Processing

Detectors were fabricated on high resistivity silicon wafers, information about wafers is shown in table 3. The gate processing was done for wafers that had already all front-end processing steps done (steps 1-5 in table 3). Wafers presented in variation table 3 were part of a lot of 8 wafers, but only those four included in the table are relevant for the work done in this thesis. Front-end processing steps are shown in figure 9. The process started with wafer oxidation. For oxidation, the lot was divided and some of the wafers were sent out to external service provider, and some were oxidized in Micronova cleanroom. $400\,\mathrm{nm}$ thick oxide was grown to all wafers, dry oxide to the wafer oxidated at Micronova and wet oxide to those oxidated externally. Oxidation in Micronova was done in diffusion furnace Centrotherm E1200 HT 260-4. Oxidized wafer is the starting point for processing, shown in figure 9a.

The fabrication of diodes was started with first lithography (fig. 9b). Lithography tools

Table 2. Information about wafers that were used, provided by the manufacturer.

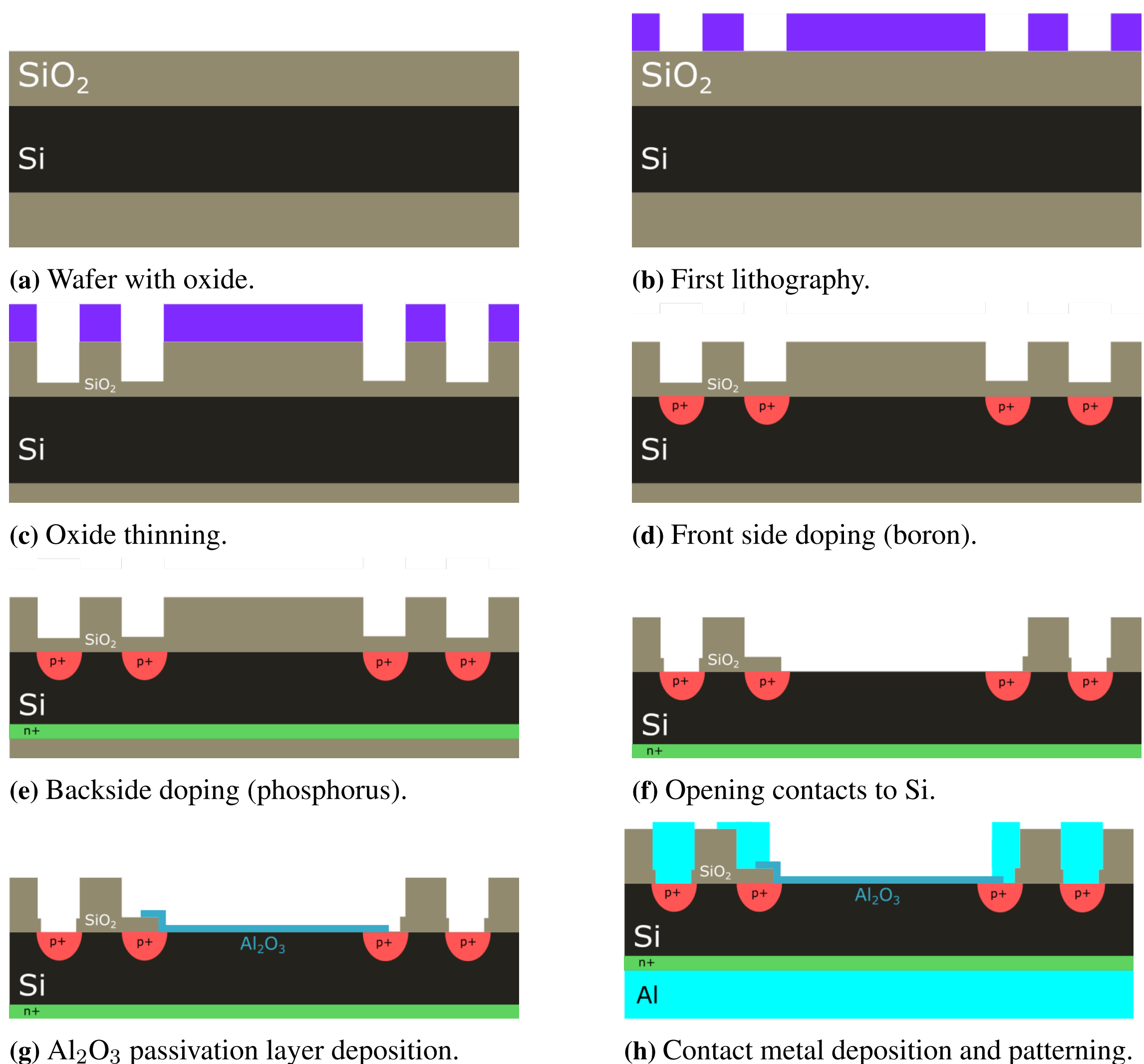
Manufacturer	Topsil GlobalWafers A/S
Material	High resistivity float zone (FZ) Silicon
Diameter	$150\,\mathrm{mm}$
Thickness	$675\,\mu\mathrm{m}$
Type	n (Phosphorus)
Crystal orientation	(1-0-0)
Resistivity	$>10\,\mathrm{k\Omega\,cm}$
Finish	double side polished

Table 3. Wafer variation table. Only wafers relevant for this thesis are included.

Process step	O2	S1	S3	S4
1. Oxidation				
1.1 Micronova (dry oxide)	x			
1.2 External (wet oxide)		x	x	x
2. Implantations				
2.1 Front	x	x	x	x
2.2 Back	x	x	x	x
3. Oxide etch	x	x	x	x
4. Al_2O_3	x	x	x	x
5. Contact metal				
5.1 Front	x	x	x	x
5.2 Back	x	x	x	x
Graphene gate				
6. Gate pads (Cr/Au)				
6.1 Lithography				x
6.2 Evaporation				x
6.3 Lift-off				x
7. Graphene transfer				x
8. Graphene patterning				x
9.ITO gate				
9.1 Lithography			x	
9.2 Sputtering			x	
9.3 Lift-off			x	

were same in all front-end processing steps. The resist coating was done on coater developer track EVG 120, exposures were done with Mask AlignerSuss MicroTec MA150 and development was done on developer track Convac M6000. All photomasks (for front-end and back-end processes) are quartz contact masks designed at VTT and ordered from Compugraphics Photomasks.

Lithography was followed with thinning the oxide to 70 nm (fig. 9c). The etch was done in buffered oxide etch (BOE) tank, O-wafers were etched for 4 minutes 15 seconds and S-wafers for 4 minutes and 25 seconds. The front side implantation of boron was done through thinned oxide (fig. 9d). In figure 9 is shown the process flow for Al_2O_3 induced junction diode. Because of that the front side doping is only on guard rings. The entire backside was implanted with phosphorus (fig. 9e). Both implantations were done with Eaton NV8200 ion implanter.



(a) Wafer with oxide.

(b) First lithography.

(c) Oxide thinning.

(d) Front side doping (boron).

(e) Backside doping (phosphorus).

(f) Opening contacts to Si.

(g) Al_2O_3 passivation layer deposition.

(h) Contact metal deposition and patterning.

Figure 9. Front end processing steps.

The second mask layer was for opening contacts to Si and the result after lithography process and wet etching in BOE (4 minutes, 30 seconds) is the structure in figure 9f. The third mask layer is passivation of the diode active area with $30\,\mathrm{nm}$ ALD (Picosun SUNALE R-150B) deposited Al_2O_3. The patterning was done after the deposition by wet etching in aluminum etch (main component phosphoric acid) at $40\,°\mathrm{C}$ for 18 minutes (fig. 9g). The final mask layer in front-end processing were depositing and patterning aluminum (Al) contact layers (fig. 9h). $300\,\mathrm{nm}$ of Al was deposited first on the front side of the wafer with OEM Mark Eclipse IV and after lithography it was patterned by wet etching in aluminum etch at $40\,°\mathrm{C}$ for 1 minute 50 seconds. The last step was to deposit Al layer also to backside of the wafer with the same sputtering tool.

3.3.1 Graphene gate

Graphene gates were continued on top of the steps shown in figure 9. Steps for fabricating the graphene gates are shown in figure 11. First step was to do lithography with image reversal (fig. 11a) for fabricating gate contact pads by evaporating chromium (Cr) and gold (Au) layers (fig. 11b). The processes described in this thesis are done in Micronova cleanroom using Suss MicroTec Gamma 4 -resist track for spin coating, baking and developing. The used resist is AZ 5214E [31]. For exposures, mask aligner MA6 fron Suss MicroTec has been used, Evaporation was done with Instrument Mattila IM-9912 evaporator. The thickness of Cr layer was $15\,\mathrm{nm}$ and the thickness of Au layer was $30\,\mathrm{nm}$. Finished pad is shown in figure 10. Additional metal layer on top of previously deposited aluminum pads was needed to make the step between the gate pad and graphene less steep. The height of aluminum pad is $300\,\mathrm{nm}$ and the thickness of graphene is only one atom layer, which causes it to break easily if the height differences are large.

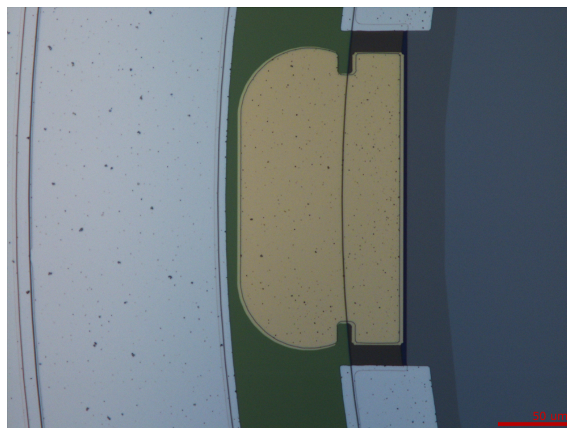


Figure 10. Evaporated CrAu layer on gate contact pad after lift-off.

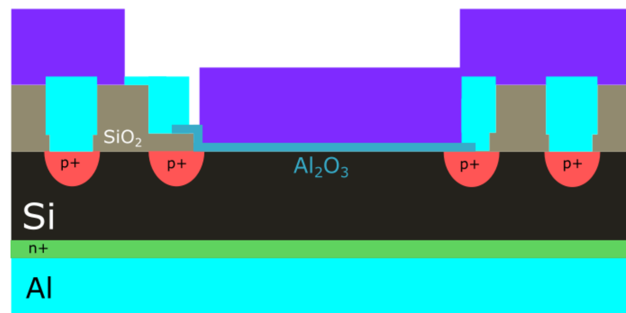
After doing the lift-off to finish gate pads 11c, the graphene transfer is done with bubbling transfer, the bubbling process is described in section 3.1.3. The graphene is CVD grown on copper substrate from Graphenea and it had a diameter of $100\,\mathrm{mm}$. The graphene sheet was released from the copper substrate in aqueous NaOH solution and transferred to bowl of DIW. The graphene sheet was floating on top of water with PMMA layer being the topmost layer. To get the graphene sheet to wafer, the wafer needed to be slid underneath the graphene in DIW. Then the wafer was lifted up with the graphene, guiding the graphene to wanted area with help of tweezers. Then the wafer was left to dry. The placement of graphene on the wafer is shown in figure 12. The method used for transferring the graphene caused there to be a thick layer of water between the wafer and graphene. It took over 24 hours to get the wafer dry enough to continue processing. This long exposure to water caused some damage to Al_2O_3 structures on the wafer.

The next step in the graphene transfer process was baking the wafer in resist oven (Memmert UFE 400). The wafer was in the oven for total of 45 minutes, temperature of the oven was increased every 15 minutes. The starting temperature was $120\,°\mathrm{C}$, then it was increased first to $150\,°\mathrm{C}$ and finally to $180\,°\mathrm{C}$. Because the temperature was increased while keeping the wafer in the oven, the set temperature was reached only at the end of 15 minute interval (except $120\,°\mathrm{C}$, that was the oven temperature when the wafer was put in). During this first bake remaining moisture was removed underneath the graphene-PMMA stack.

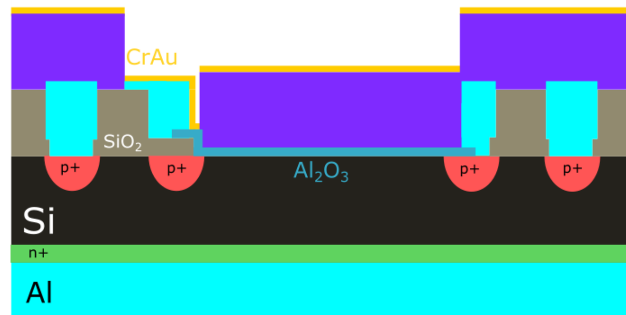
After the first bake, the PMMA layer was removed. The wafer was kept for 4 minutes in acetone and 1 minute in IPA. The wafer was dried by blowing after taking it out of IPA, without dipping it into water first. Then the wafer was put to vacuum oven to $300\,°\mathrm{C}$ overnight. Purpose of keeping the wafer in the vacuum oven for a long time was to remove remaining PMMA particles and to increase the adhesion of the graphene to the wafer.

The final phase of graphene gate processing was patterning the graphene. Lithography was done with same AZ5214E resist as the other lithography layers. This time the resist was used in normal positive mode. Lithography results are shown in figure 13. Lithography parameters were not optimized for this process which lead to graphene ripping away from some of the gates during development (figures 13b and 13c). The graphene was etched in O_2 plasma (Oxford Instruments plasma stripper PRS900) for 5 minutes with $100\,\mathrm{W}$ power and $100\,\mathrm{sccm}$ oxygen flow. After etching the final step was removing the resist. It was done by keeping the wafer 15 minutes in acetone and then few minutes in IPA, again drying it right after it came out from IPA. Finished graphene gates are shown in figure 14. The figure 14b shows that even with microscope it can be difficult to see

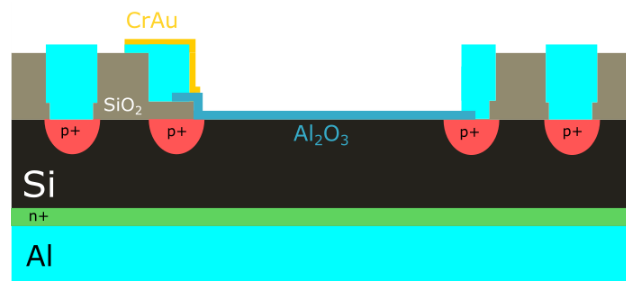
which components have broken graphene.



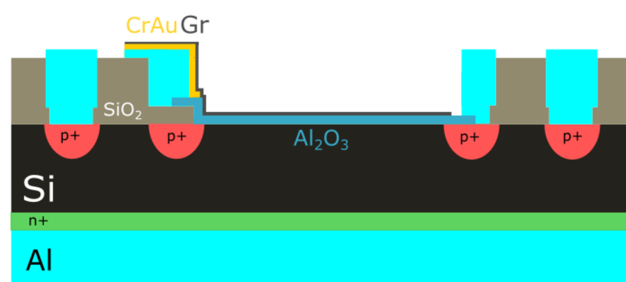
(a) Lithography for lift-off.



(b) Evaporated contact metal.



(c) Contact pads after lift-off.



(d) Finished device with graphene gate.

Figure 11. Process steps for fabricating graphene gates.

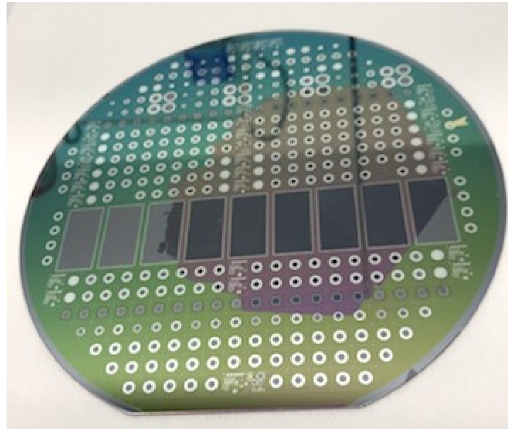
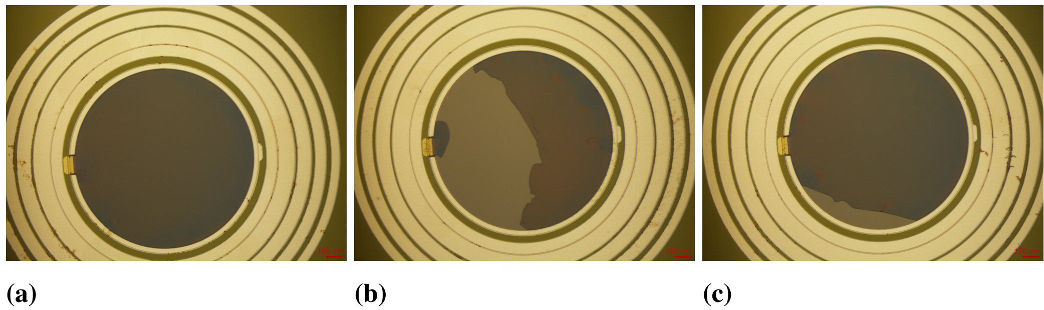


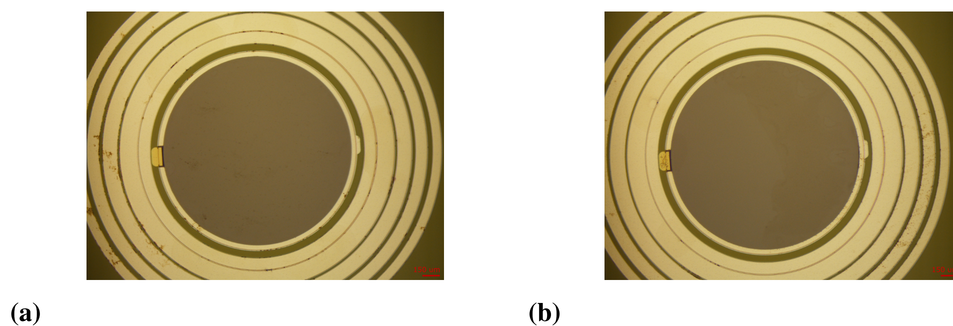
Figure 12. The dark area is graphene after drying after the transfer.



(a) **(b)** **(c)**

Figure 13. Graphene gates after O_2 etching, before removing resist. Darker areas have graphene and resist, from lighter areas the resist was ripped away during development.

Before starting chacterization the wafer was annealed (ATV PEO-603) in N_2 at $425\,°C$ for 30 minutes. Annealing step was important to create contact between Al_2O_3 layer and Silicon and activate the Al_2O_3 layer passivation. Annealing in temperatures above $400\,°C$ have been shown to increase the charge in Al_2O_3 (same goes also for SiO_2) and increase the passivation [5], [6], [35].



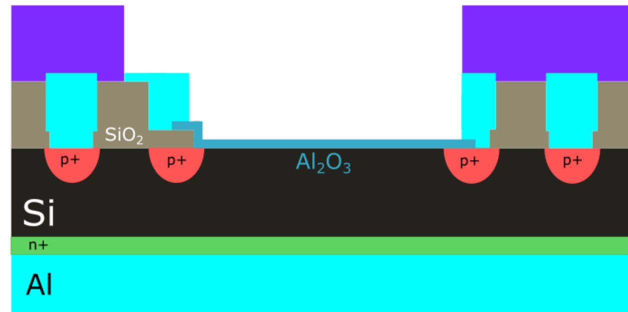
(a) **(b)**

Figure 14. Finished graphene gates: a) full graphene, b) broken graphene.

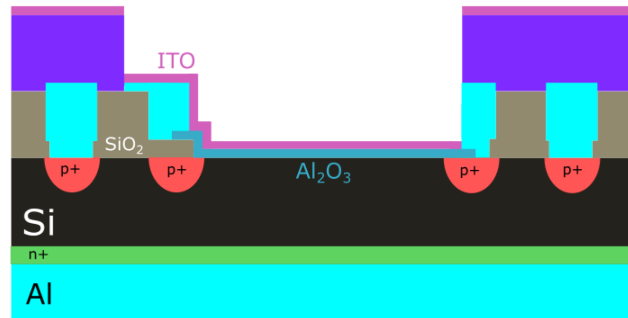
3.3.2 ITO gate

The wafer with ITO gates was processed to act as a reference for the graphene gated diodes. The processing was continued after steps shown in figure 9. The steps for fabricating ITO gates is shown in figure 15. ITO was fabricated with lift-off process and the first step was to do image reversal lithography (figure 15a), described in section 3.1.2. The ITO deposition was done with sputtering (VonArdenne CS 730 S Cluster System). The target thickness was $50\,\mathrm{nm}$, sputtering power $400\,\mathrm{W}$ and sputtering time $100\,\mathrm{s}$. The parameters were chosen based on previous experiments of sputtering ITO to achieve conducting film. The film thickness was checked after sputtering with spectroscopic ellipsometer Semilab SE-2000 and it was found to be about $(38 \pm 5)\,\mathrm{nm}$ on a monitor wafer.

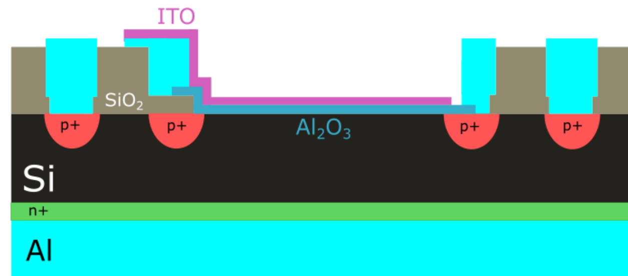
ITO gates were finished with lift-off (figure 15c). The wafer was 27 minutes in acetone, then it was transferred in IPA to posistrip, in which it was kept for 20 minutes. After rinsing with water the wafer was spindried. At the end the wafer was annealed at the same time with the other wafer, $425\,^{\circ}\mathrm{C}$ for 30 minutes. Finished ITO gate is shown in figure 16.



(a) Lithography for lift-off.

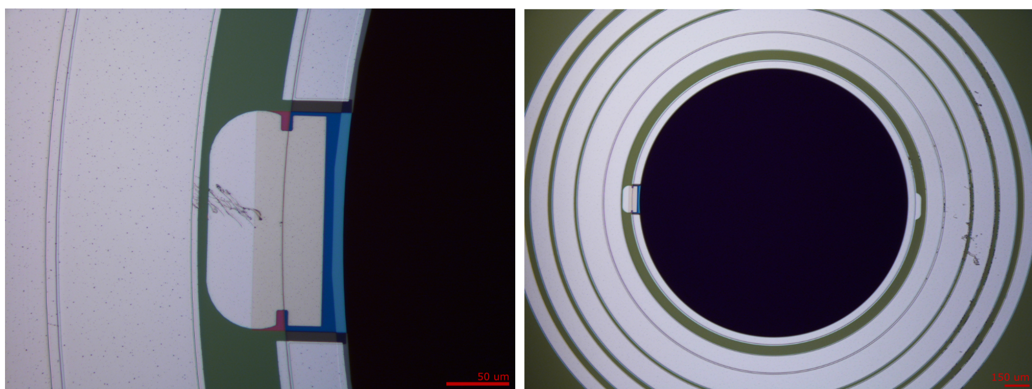


(b) Sputtered ITO.



(c) Finished ITO gate.

Figure 15. Process steps for fabricating graphene gates.



(a) **(b)**

Figure 16. ITO after lift-off: a) close up to the gate contact pad, b) finished gated diode.

4 DIODE CHARACTERISATION

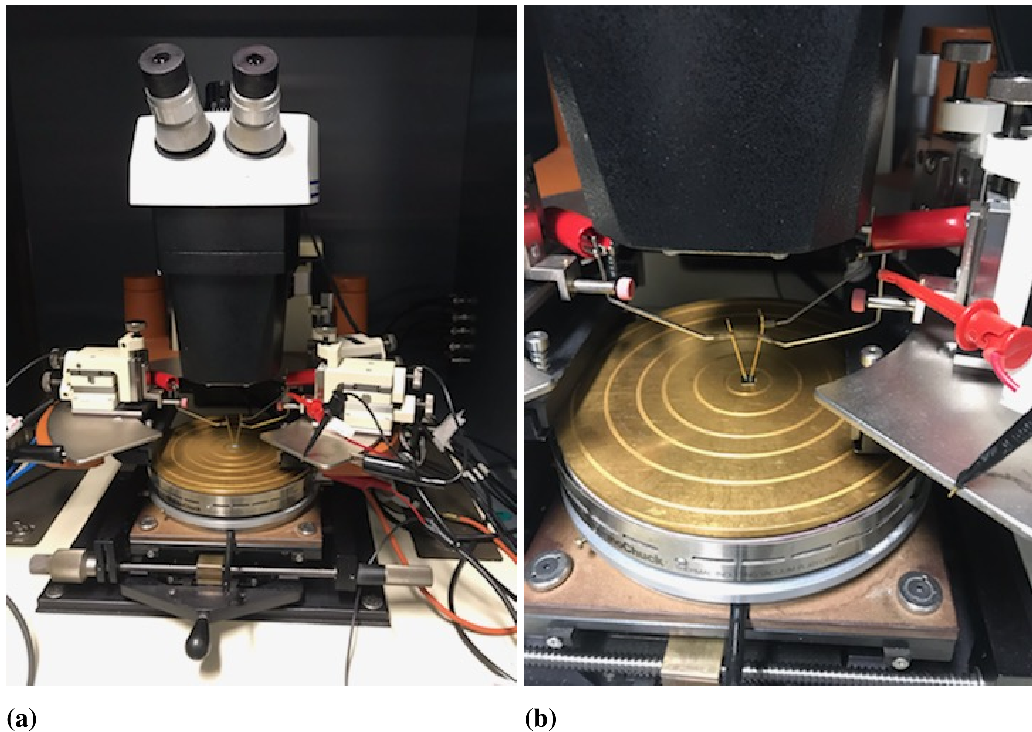
After fabrication, the quality and the functionality of the detectors is tested with different types of measurement techniques. This sections is organized to subsections for different measurement types, in which the measurement setup and connections are described first, then followed by results and discussion.

4.1 Current - voltage (IV)

4.1.1 Measurement

Current-voltage (IV) characteristics are important part of characterisation of semiconductor detectors. Reverse IV measurement done in dark (in case of light sensitive detectors) tells the level of leakage current in the detector. Semiconductor detectors are operated in reverse biased mode, as was explained in more detail in section 2. For diodes with n-type bulk studied in this thesis it means applying positive voltage to the backside (cathode) of the detector and negative voltage to the front (anode) of the detector and measuring the current from the anode. The reverse biasing increases the depletion region further into the silicon bulk. As there are no free charge carriers in depletion region (only charge carriers generated by heat or incoming radiation or caused by non-idealities of the material), the detector leakage current without light or radiation is very small. For good commercial PIN diode detectors the leakage current is order of 2-10 $\mathrm{nA/cm^2}$ [36], [37]. The level of leakage current tells about the quality of the detector: the smaller, the better.

Major part of IV measurements was done at Micronova. The setup consists from manual probestation and Agilent 4155C/4156C parameter analyzer, which is connected to a computer through GPIB. The measurement is controlled with computer, using software programmed with MATLAB. The parameter analyzer has four source measurement units (SMUs) and two voltage measurement units (VMUs). For the most part, only SMUs are used for diode measurements. VMUs were used only in TLM measurements. The probestation, shown in figure 17a, is inside a cabinet, which has doors and additional cloth covering to ensure maximum darkness. It consists from a chuck on the moving stage, a level for the manipulators and a movable microscope. The bias is supplied to the chuck on which the wafer (or a chip, like in figure 17b) is laying. The front side contacts are made with needles. Test structures, FETs and TLMs were measured using a probecard with four probes with $200\,\mathrm{\mu m}$ pitch.



(a) **(b)**

Figure 17. Probestation that was used in IV measurements, a) entire probestation inside the cabinet, b) closeup of a gated diode sample contacted with needles.

The diode connections to the parameter analyzer are shown in figure 18. In the picture the connections for gated diodes are shown. If the diode did not have a gate, SMU4 was not used and the measurement was done with two probes instead of three. The high voltage was supplied to cathode through SMU1. Depending on the measurement type (cathode sweep or gate sweep) the voltage was either sweeped from $0\,\mathrm{V}$ to $50/100\,\mathrm{V}$ and back to $0\,\mathrm{V}$. The maximum voltage was usually $50\,\mathrm{V}$ for the gated diodes and for diodes without gate it was $100\,\mathrm{V}$. The voltage was set to $0\,\mathrm{V}$ to anode and to guard ring through SMU2 and SMU3. The gate voltage was varied through SMU4, both positive and negative voltages were used. Current was measured from all four contacts.

CV, TCT and radiation measurements were done at Helsinki Institute of Physics (HIP) Detector Laboratory at Kumpula campus, and the IV results of chips used in those measurements were tested with their setup. Setup consisted from probe station with needles attached to micromanipulators. The largest difference was that current was only measured from the cathode (backside of the wafer) and anode. The guard ring was connected to the ground. The voltage was supplied to the cathode by Keithley 2410 source meter and it was also used to measure the total current. The anode current was measured with Keithley 2410 picoAmpere-meter. [38] For the gated diodes the gate voltage was supplied with PS613 DC power supply (positive voltages only). Measurements done with HIP setup

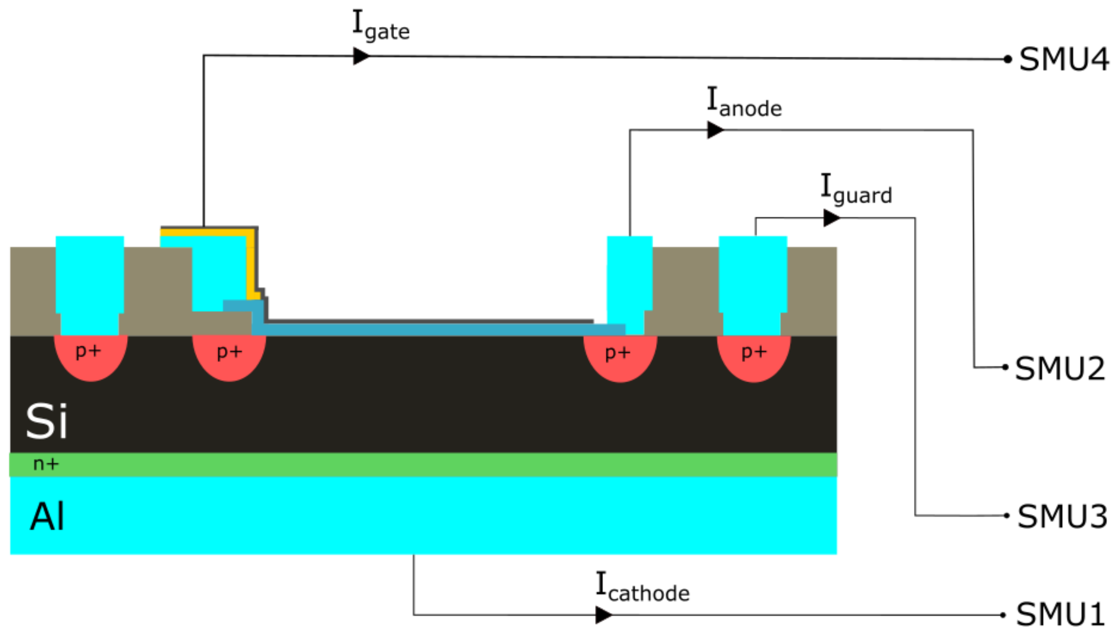


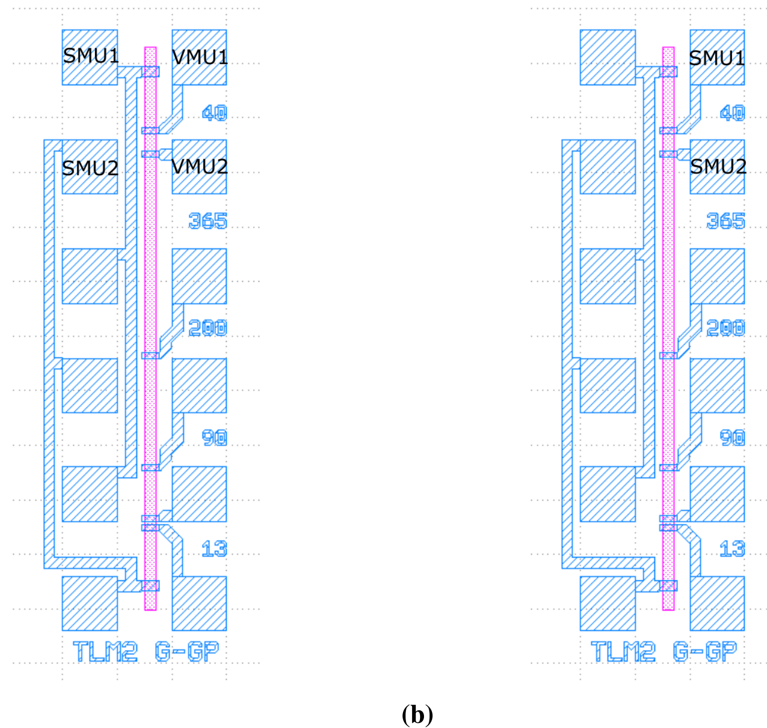
Figure 18. Connections to parameter analyzer in diode IV measurements.

will be mentioned in results, otherwise they are measured with VTT Micronova setup.

Transfer length method (TLM) measurements

In order to find out the contact resistance between gate material (ITO/graphene) and the contact pad material (Al/CrAu), transfer length method was used for measuring the structure in figure 19. The measurement was done with the same setup as described above, using a four needle probecard with 200 µm pitch. In figure 19a is shown the connections to parameter analyzer in case of four point measurement. During measurement, current was supplied to the pads on the left side of the structure through SMU1 and SMU2 and induced voltage was measured from the right side of the structure (VMU1 and VMU2). After each measurement the probes were moved over next length and the measurement was repeated. In the structure there were five different lengths to measure.

It was not possible to get results with four point measurement from graphene gated TLM structure, and instead the measurement was done as two point measurement. In two point measurement the current was supplied through the same pads from which the voltage was measured, this is shown in figure 19b. The most probable reason for four point measurement not working with graphene as gate material is breaking of graphene at some point of the structure. The width of the gate bar is 20 µm and it goes on top of the gate pads, as the metal deposition was done before gate material deposition.



(a) **(b)**

Figure 19. TLM measurement structures with measurement contacts for a) four point measurement and b) two point measurement. The blue parts are contact pads and the pink bar is gate material.

During measurement the voltage was swept through SMU1 from $0\,\mathrm{V}$ to $250\,\mathrm{mV}$, then to $-250\,\mathrm{mV}$ and back to $0\,\mathrm{V}$ with $50\,\mathrm{mV}$ steps. The voltage of SMU2 was set to $0\,\mathrm{V}$. Same applies to both four point and two point measurements.

When the measured voltage values are plotted as a function of the supplied current, the line fitted into the data gives the value of resistance during the measurement. That is the total resistance of the system. In the four point measurement the value of the measured voltage is plotted as difference between two measured voltages (VMU2-VMU1). In two point measurement the resistance is calculated from measured voltages from SMUs. An example from measurement data from four point measurement is shown in figure 20. When all different lengths are measured, the resistance values from all of them are used to calculate the contact resistance.

By plotting the total resistances R_T as function of the length (fig. 21), a line can be fitted into the data. Equation of that line is

$$R_T = \frac{R_S}{W} L + 2R_C, \tag{2}$$

where R_S is the sheet resistance, W is the width of the TLM bar and R_C is the contact

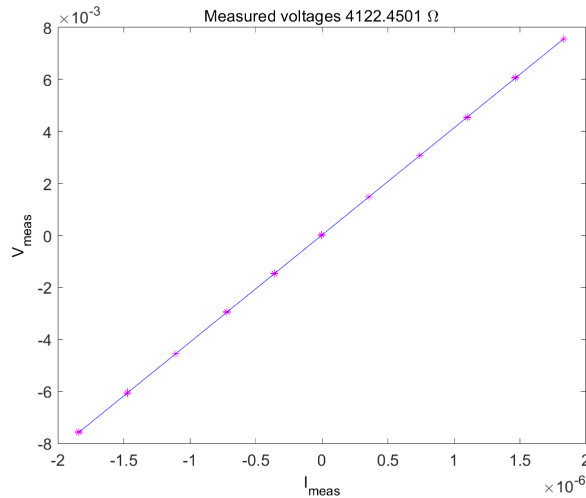


Figure 20. Measurement data from TLM four point measurement.

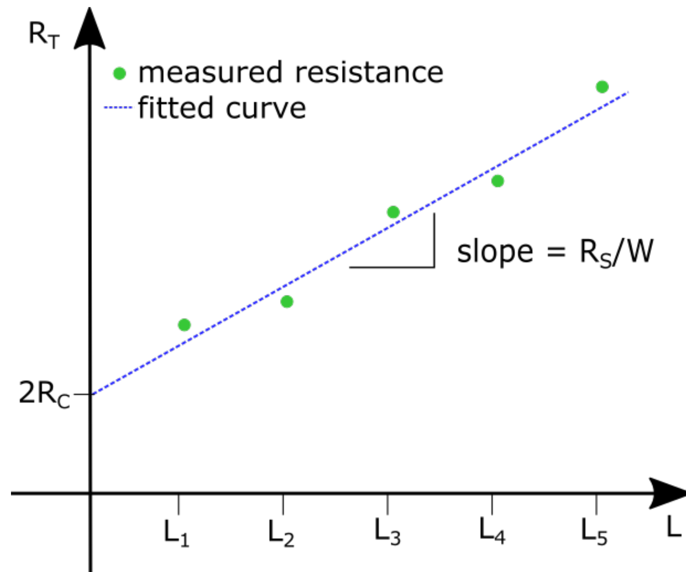


Figure 21. Determining R_C from measurement data. Based on picture in [39].

resistance [39]. From that equation contact and sheet resistances can be solved.

FET measurements

In order to figure out suitable gate voltages for diode measurements, couple of FETs were measured. The connections for FET measurements are shown in figure 22. During measurement, the source voltage was set to 0 V through SMU1. For gate sweeps the drain voltage was set to fixed negative values through SMU3 while the gate was sweeped from minimum value to maximum value (SMU2) and back to minimum value. The used values of drain and gate voltages varied between components. Current was measured through all three SMUs. Figure 22b shows the contact points for probes. At the right bottom corner

there is pad that is not connected to anywhere and there is no SMU marked to it. That pad was just a place for fourth probe of the probe card which was not needed during the measurement.

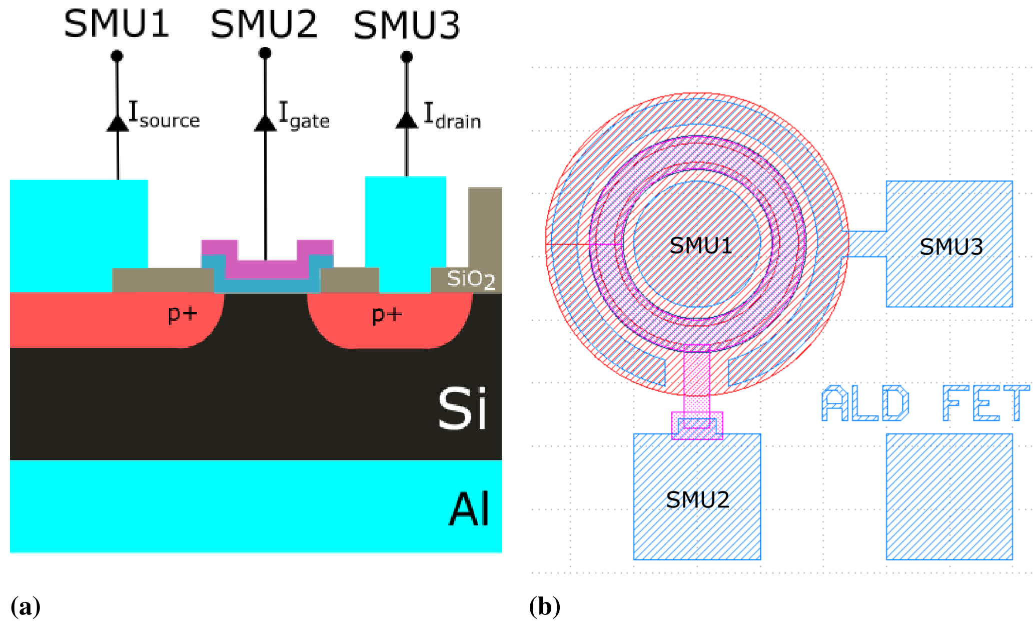


Figure 22. Connections used in FET measurements a) connections to SMUs from the cross sections b) mask design showing the SMU connections.

Analyzing components of leakage current

To study the origins of leakage current, set of five different sizes of the diode were measured. The diode was structurally same as the diodes with $1650\,\mu\text{m}$ diameter, but it was scaled up or down.

Generally, the sources of leakage current can be divided into bulk and surface leakages. The relation between them can be written

$$I = PJ_{surface} + AJ_{bulk}, \tag{3}$$

where I is the measured leakage current, P is the perimeter of diode, $J_{surface}$ is the current density of surface component of leakage current, A is the surface area (active area) of the diode and J_{bulk} is the current density of bulk component of the leakage current [40]. When the equation is divided by area, it takes form

$$\frac{I}{A} = \frac{P}{A} J_{surface} + J_{bulk}. \tag{4}$$

After all different sized diodes were measured, a curve can be fitted into data of current from chosen cathode voltage plotted as a function of P/A. The constants of the fit gives an idea where the major part of leakage current in the diode comes from.

4.1.2 Results and discussion

TLM measurement results are presented in tables 4 (total resistances from graphene) and 5 (total resistances from ITO). Curves fitted into the data are shown in figure 23 and the parameters calculated from those fits are presented in table 6. With ITO the same structure is measured from four different chips but from graphene only from one chip. That is because the transferred graphene was smaller than the wafer and it covered only part of the wafer. And because there were some problems after the transfer, only one of the measured chips gave reliable results.

As can be seen from tables 5 and 4, the measured lengths on different wafers are a bit different. That is because the contact pads on S04 are $2\,\mu\mathrm{m}$ larger in every direction compared to S03. Larger contact pads are also the reason why there are only three datapoints included in the fit in figure 23b. The shortest measured distance was only $1\,\mu\mathrm{m}$ on the mask design and the measurement result over that distance seemed like an outlier when the data was plotted. It is possible that due to small distance, measurement was short circuited or that there was not a real gap. Over $74\,\mu\mathrm{m}$ distance it was not possible to get proper measurement signal which could mean that the graphene is somehow damaged somewhere in that area. Having damaged graphene in that area could also explain why the four point measurement did not work.

Table 4. Measured total resistances from graphene. There was no contact with $74\,\mu\mathrm{m}$ long part so there is no measurement result.

	S03-K10 [Ω]
$L = 1\,\mu\mathrm{m}$	62.11
$L = 28\,\mu\mathrm{m}$	6355
$L = 74\,\mu\mathrm{m}$	-
$L = 188\,\mu\mathrm{m}$	14300
$L = 354\,\mu\mathrm{m}$	24500

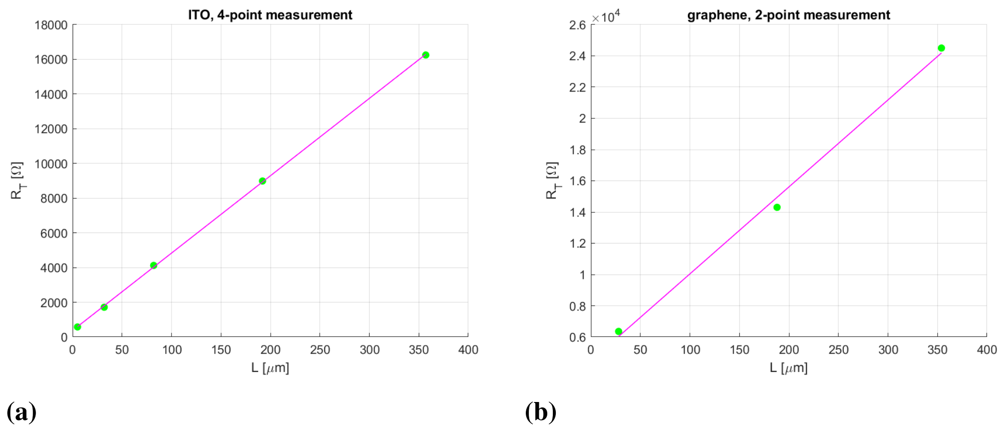


Figure 23. Fitted curves to TLM measurement data a) four point measurement from ITO (S03-A10) and b) two point measurement from graphene (S04-K10).

Table 5. Measured total resistances from ITO.

	S03-V08 [Ω]	S03-V10 [Ω]	S03-K10 [Ω]	S03-A10 [Ω]
$L = 5\,\mu m$	671	624	556	578
$L = 32\,\mu m$	2021	1805	1455	1713
$L = 82\,\mu m$	4122	4154	2950	4123
$L = 192\,\mu m$	9448	8988	6481	8987
$L = 357\,\mu m$	17231	16940	12504	16248

Results shown in table 6 show that there is quite large variation in ITO contact resistances. That might mean that the contact between metal and ITO is not very good. Detectors were fabricated in non-convential order so that the contact metal (Al) was deposited before gate material (ITO/graphene). That might lead to worse contacts than having gate material under the contact metal. In the case of graphene, doing the transfer on top of already finished metal structures can cause issues as graphene is very thin and breaks easily because of the height differences.

The values of contact and sheet resistances for graphene are remarkably higher than the resistances from ITO. Especially contact resistance is over ten times larger for graphene than it is for ITO. The sheet resistance is closer to values measured from ITO. The results from graphene are from two point measurement and results from ITO are from four point measurement which makes the results difficult to compare. In two point measurement the

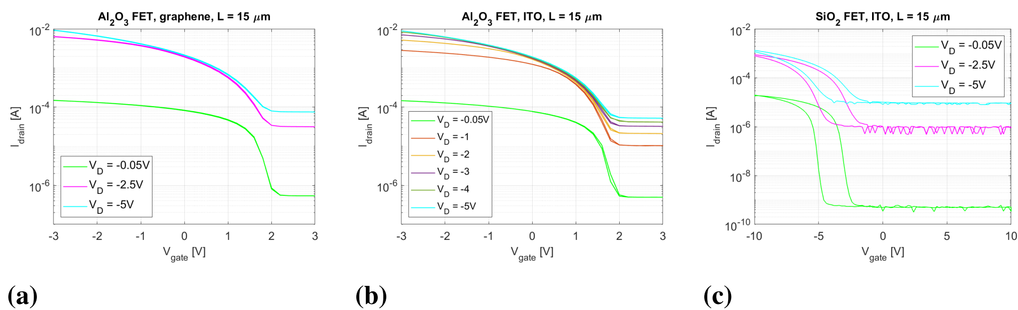
Table 6. Calculated results from all TLM measurements. Results from components starting S03 have as ITO gate material and S04 has graphene.

	S03-V08	S03-V10	S03-K10	S03-A10	S04-K10
R_C [Ω]	207	162	137	187	2235
R_S [Ω/□]	941	925	676	892	1114

voltage is measured with same probes as the current is supplied. That means that some components affecting to sheet resistance that are excluded in four point measurement can be included in two point measurement.

Another type of test structures that were used to verify that the structures should be working as expected were FETs. The measurement was described in section 4.1.1. The results are from gate sweeps from from three types of FETs: Al_2O_3 as dielect under graphene (fig. 24a) and ITO (fig. 24b) gates and SiO_2 (field oxide) as dielect with ITO gate (fig. 24c). The results show transition from inversion to accumulation in the transistors. With Al_2O_3 the threshold voltage is $2\,\mathrm{V}$ and with SiO_2 it is around $-4.5\,\mathrm{V}$. With SiO_2 in transition state there is hysteresis which makes estimating the transition voltage harder. With Al_2O_3 there is no hysteresis. The results of the FET measurements were used to select suitable gate voltages for measuring the gated diodes.

Threshold voltages with different signs are explained by different types of charges in the oxides: Al_2O_3 has a large negative charge and SiO_2 has a smaller positive charge. Fixed negative charge density in Al_2O_3 is reported to be $10^{12}\,\mathrm{cm}^{-2}$ to $10^{13}\,\mathrm{cm}^{-2}$ [5], [6] and the fixed positive charge in SiO_2 has been reported to be $10^{10}\,\mathrm{cm}^{-2}$ to $10^{12}\,\mathrm{cm}^{-2}$ [8], [9]. Thickness of the oxide layer and size and sign of the charge have an effect in the threshold voltage. Al_2O_3 layer is a lot thinner (30-40 nm) compared to the field oxide thickness (300-400 nm).

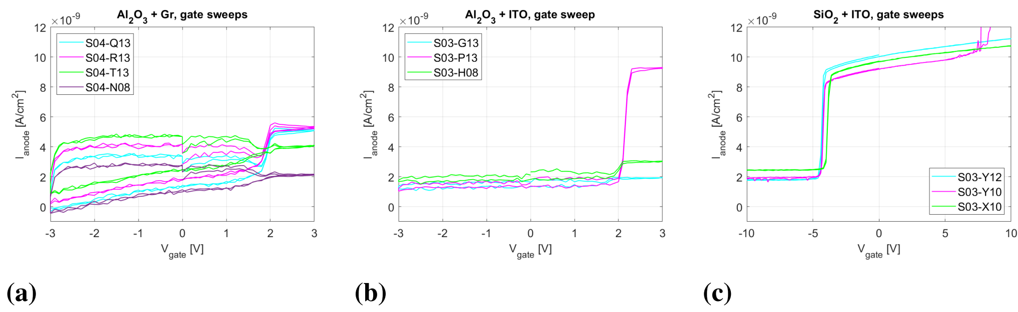


(a) **(b)** **(c)**

Figure 24. FET gate sweeps: a) Al_2O_3 + graphene gate, b) Al_2O_3 + ITO gate and c) SiO_2 + ITO gate.

Figure 25 shows that in gated diodes the transition from inversion to accumulation happens at the same gate voltage in diodes as it did on FETs: with Al_2O_3 passivation at $2\,\mathrm{V}$ and with SiO_2 passivation at $-4.5\,\mathrm{V}$.

It seems that the current difference between inversion and accumulation state is not as clear in Al_2O_3 induced junction diodes compared to the diodes having SiO_2 passivation.



(a) (b) (c)

Figure 25. Diode gate sweeps, cathode current 50 V: a) Al_2O_3 + graphene gate, b) Al_2O_3 + ITO gate and c) SiO_2 + ITO gate.

In figures 25a and 25b the transition is barely noticeable on some devices. With the graphene gated diodes there is also a hysteresis, but with ITO gate there is no hysteresis with either dielectric. As was shown in section 3.3.1, due to non-optimized lithography phase the graphene was etched away from some diodes. One reason for not having as clear transition from inversion to accumulation state with graphene gated diodes could be that the graphene is broken in the measured component. S04-N08 (purple curve in fig. 25a) seems to have smallest transition from inversion to accumulation. On the wafer, it was on different row than the other three diodes that are presented in the same figure. It is possible, that the area, where S04-N08 was located was under water (during graphene transfer) for longer time than other areas as the water dried unevenly from different places. But as the transition from inversion to accumulation with ITO gated Al_2O_3 diodes has same type of behaviour than the graphene gated ones, there is probably also some other reasons behind the behaviour. ITO had a distinct purple color which was clearly visible in the probestation microscope and based on that it is unlikely that ITO would have been broken.

SiO_2 passivated diodes show a really clear transition from inversion to accumulation at approximately -5 V and the differences between diodes are less noticeable than in Al_2O_3 passivated ones, but there still is some differences. In the mask design, SiO_2 passivated diodes are placed to the edges of the wafer. Also, S03-X10 is on the opposite side of the wafer than S03-Y12 and S03-Y10. As the wafers are handled with tweezers from the edges, it is possible that there is more contamination in the SiO_2 passivated diodes. The contamination might cause differences in the leakage current levels or behaviour of the diode. Contamination might explain why the transition from inversion to accumulation in S03-X10 (green curve) starts at slightly different gate voltage compared to other two. With high positive gate voltages S03-Y10 (pink curve in fig. 25c) shows behaviour that is different to other two measured components that are shown in the same figure. There probably was something wrong with that component even though the results otherwise

look the same as the other components.

Based on data shown on figures 24 and 25, the gate voltages for cathode sweeps were chosen to be $3\,\mathrm{V}$, $1\,\mathrm{V}$, $0\,\mathrm{V}$, $-1\,\mathrm{V}$ and $-3\,\mathrm{V}$ for Al_2O_3 passivated diodes. The results for graphene gated version is shown in figure 26a and for the ITO gated version in figure 26b. The data is shown as a mean value from multiple measurements. Data from each device is measured once, but the sweep was run from $0\,\mathrm{V}$ to $50\,\mathrm{V}$ and then back to $0\,\mathrm{V}$ with $1\,\mathrm{V}$ steps. For calculating the mean values both sweeps were taken into account. The leakage currents from diodes are presented in unit $\mathrm{nA/cm^2}$ to make it easier to compare the results to other results. The active are of diode that has been used to normalize the results is $0.0214\,\mathrm{cm^2}$.

Results in figure 26 show the same behaviour as the gate sweeps in figure 25: with gate voltages smaller than $2\,\mathrm{V}$ the diode is in inversion and with gate voltage $3\,\mathrm{V}$ the diode is in accumulation. This shows that it is possible to control the charges in the oxide layer with the gate to change the state of the device. But because the inversion is very strong, the gate voltage does not seem to have an effect with smaller gate voltages in either case (graphene or ITO). The level of anode leakage current is less than $4\,\mathrm{nA/cm^2}$ in both Al_2O_3 passivated gated diodes, but with ITO gate it is a bit lower. With $50\,\mathrm{V}$ cathode voltage and gate voltages smaller than $3\,\mathrm{V}$ the anode current in ITO gated diode is about $1.4\,\mathrm{nA/cm^2}$ and in graphene gated diode the current is about $2.4\,\mathrm{nA/cm^2}$. In accumulation state (V_G $\geq$3 V) the difference between these two gate materials is smaller, about $0.5\,\mathrm{nA/cm^2}$.

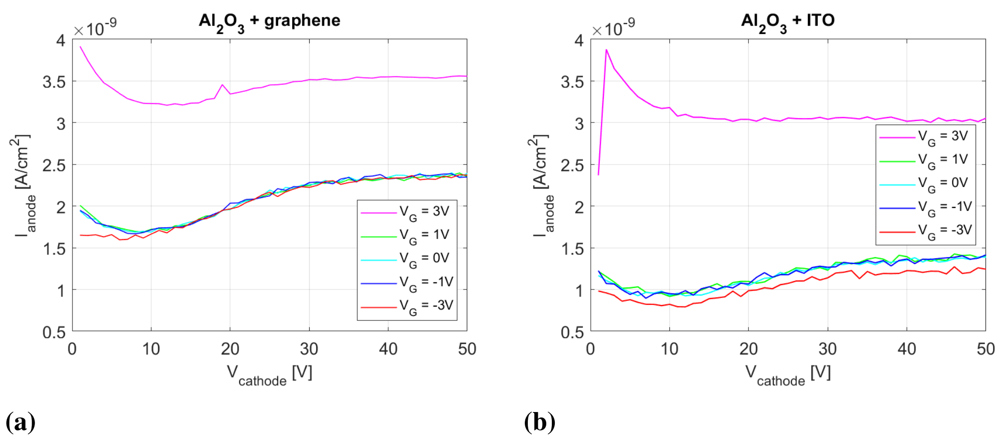
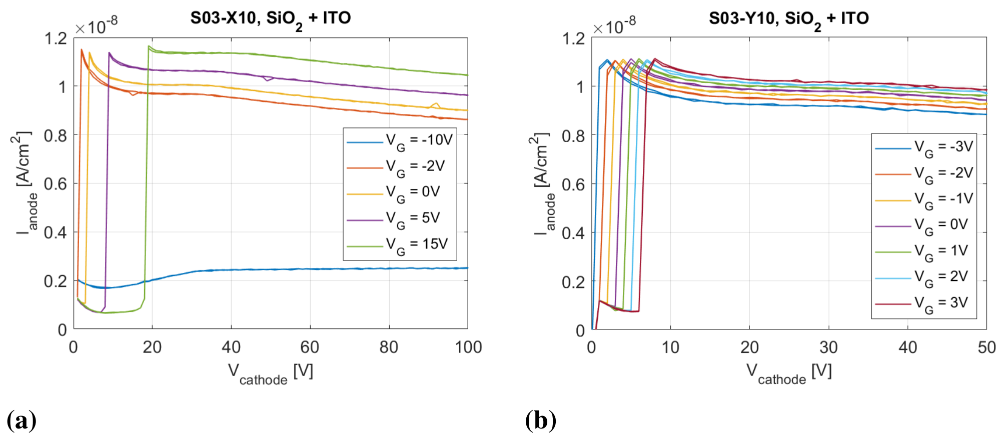


Figure 26. Effect of gate voltage to the anode current in Al_2O_3 induced junction gated diodes a) graphene gates, b) ITO gates. Data is presented as mean values from several components.

Differences between results from ITO and graphene gated diodes are probably at least partially explained by the long exposure of S04-wafer to DI-water during the graphene

transfer. It has been shown, that without thermal treatment (annealing), Al_2O_3 is slowly etched in DIW [41]. Also swelling of Al_2O_3 film when exposed to water has been reported [42]. The conditions in this case are different than what was described in the references as the wafer was not fully immersed in DI-water. Instead there was a layer of DIW on top of the wafer that was left to evaporate. But it is possible that there has been some etching or other reactions because the water covering stayed on for a long time. The next step for graphene gated diodes would be doing the graphene transfer with dry transfer.

The first test of SiO_2 passivated gated diode was done with same gate voltages as for Al_2O_3 passivated ones (results shown in figure 27b). Because SiO_2 is ten times thicker than Al_2O_3, it can handle higher voltages, as shown in figure 25c. For the next measurement the used gate voltages were chosen based on figure 25c and the measurement result is shown in figure 27a. Few measurement points are removed from the data, because they were determined to be caused by external sources outside the probestation.



(a) **(b)**

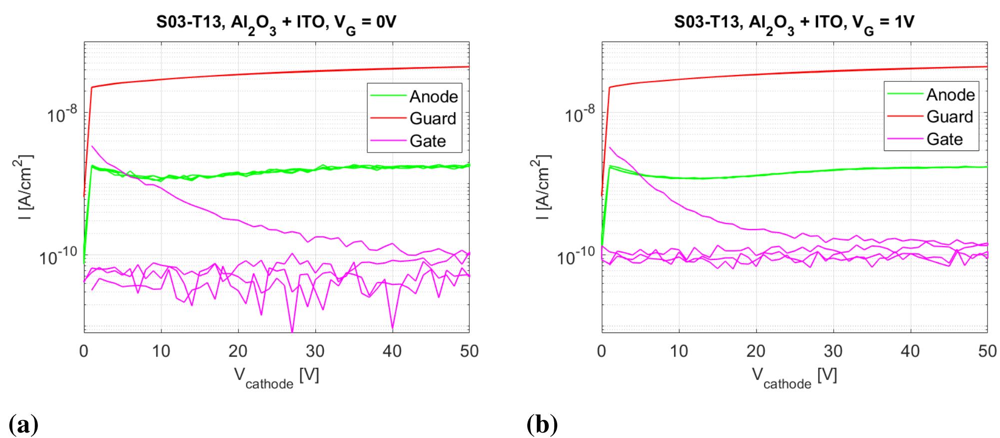
Figure 27. Effect of gate voltage to the anode current in SiO_2 induced junction gated diodes.

Results in figure 27 show the differences between diode states better than results from Al_2O_3 passivated diodes. That could be because of the smaller positive charge in SiO_2 compared to Al_2O_3 negative charge. With $V_G = -10\,\mathrm{V}$ the diode is in inversion and the behaviour is similar to the behaviour of Al_2O_3 passivated diodes with gate voltages $<3\,\mathrm{V}$. According to results in 25c, IV curves should look the same with all gate voltages smaller than $-5\,\mathrm{V}$. At $50\,\mathrm{V}$ cathode voltage the anode current in SiO_2 diode in inversion is about $2.5\,\mathrm{nA/cm^2}$.

In accumulation state the anode currents in gated SiO_2 diodes range from $8.5\,\mathrm{nA/cm^2}$ to $10.05\,\mathrm{nA/cm^2}$, depending on the gate voltage. These values are almost/over three times higher compared to ITO gated Al_2O_3 diodes ($3\,\mathrm{nA/cm^2}$). In accumulation state the

beginning of the curve behaves in an interesting way. The curve starts with low current which increases sharply at a point that seems to vary based on gate voltage. It shows clearly in both pictures in figure 27 that with gate voltages closer to the transition voltage the sharp increase happens with smaller cathode voltages. This kind of behaviour would be expected to be observed also from Al_2O_3 passivated diodes if they were measured with voltages higher than the threshold voltage.

Two versions of gated diode leakage currents (anode, gate and guard ring) are shown in figure 28. The cathode voltage is supplied to the wafer through the chuck on the probe station and because of the large area of the chuck which causes a lot of leakages the cathode current behaves differently compared to the anode, gate or guard ring currents and it is not included into the figures. The interesting part in figure 28 is the capacitive behaviour of the gate current. At the beginning, the leakage current from gate is larger than the anode leakage current. After a while the gate leakage current decreases. Measuring same range two times shows that after the initial charging the gate current stays on the same level for the rest of the measurement. Another interesting thing is that this charging/capacitive phenomenon is not depended on gate voltage: the figure 28a is measured with $V_G = 0\,\mathrm{V}$. The level of final gate currents is different between figures 28a and 28b ($V_G = 1\,\mathrm{V}$) which is expected because of applied gate voltage on the latter case. The level of gate leakage current seems to have no effect on anode leakage current as the anode leakage current stayed same during the repeated measurement.



(a) **(b)**

Figure 28. Leakage currents measured from the front side of the wafer: anode, guard ring and gate. Backside voltage is sweeped from $0\,\mathrm{V}$ to $50\,\mathrm{V}$ and back to $0\,\mathrm{V}$ two times in a row, gate voltages are a) $0\,\mathrm{V}$ and b) $1\,\mathrm{V}$.

To test where the breakdown voltage might be, a diode was biased to $400\,\mathrm{V}$. This measurement was done with HIP setup. The curve is shown in figure 29, it shows that the diode was able to handle the voltage without any indications about breaking down. The

breakdown voltage was estimated to be around $600\,\mathrm{V}$ but it was not tested experimentally. The high breakdown voltage allows operating diodes on high voltages without need to worry about it breaking down.

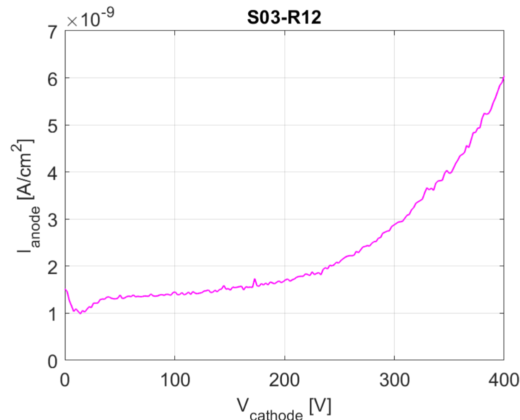


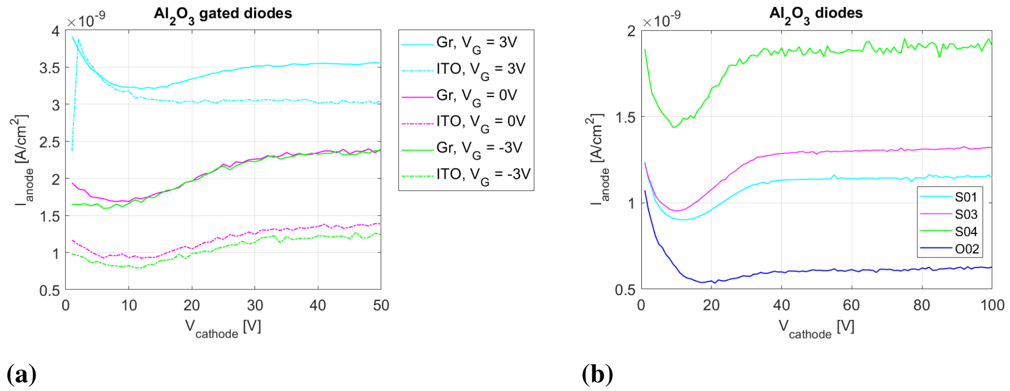
Figure 29. Al_2O_3 passivated diode without gate was biased to $400\,\mathrm{V}$.

The results comparing Al_2O_3 passivated diodes between wafers are shown in figure 30: diodes with gates in figure 30a and diodes without gates in figure 30b. The data is again shown as averages of several components. As it was already discussed earlier, when ITO and graphene gated diodes are compared in inversion mode (V_G <$3\,\mathrm{V}$) at $50\,\mathrm{V}$ cathode voltage, the anode current of ITO diode is approximately $1\,\mathrm{nA/cm^2}$ smaller than with graphene gate. In accumulation mode the difference is about $0.5\,\mathrm{nA/cm^2}$, ITO again having lower anode current.

The averages of anode currents from Al_2O_3 induced junction diodes from all four different wafers is shown in figure 30b. Differences in wafer processing were shown in table 3. Wafer S01 can be thought as a reference for changes during further processing that has been done for S03 (ITO gates) and S04 (graphene gates). O02 has been processed exactly same as S01 but the oxidation has been done at Micronova (S-wafers were oxidated by external service provider).

The easily noticeable differences are that O02 has about $1\,\mathrm{nA/cm^2}$ lower anode current and S04 has about $1\,\mathrm{nA/cm^2}$ higher anode current at $50\,\mathrm{V}$ cathode voltage compared to S01 and S03. The lower current of O02 can be explained by to Boron traces in the oxidation furnace which happens to improve the junction in our case. Similarly as in figures 30a and 26b, the anode current on S04 is higher than in S03. During the graphene transfer process S04 was covered in water for long time (about 24 hours) and that has reduced the passivation properties of Al_2O_3, as was discussed earlier. The difference at

$100\,\mathrm{V}$ cathode voltage between S01 and S03 is about $0.2\,\mathrm{nA/cm^2}$. That difference could be at least partially explained by deposition of ITO by sputtering. Sputtering can be quite rough process as there is different types of radiation in the chamber during the process. It is possible that the radiation has caused some damage to diodes even with being coated with resist (ITO gate was fabricated with a lift-off process).



(a) **(b)**

Figure 30. Comparison of Al_2O_3 passivated diodes between wafers; a) graphene and ITO gated diodes and b) diodes without gates.

Comparison between different types of diodes on the same wafer is shown in figure 31: diodes on O02 in figure 31a and diodes on S03 in figure 31b. The data in both figures is shown as a mean value from several measurements. Some data points are removed because they were quite obviously caused by some external sources and were not related to the measurement. The diode without oxide is only shown in figure 31a because the design did not work with gate in reverse biased mode. The anode leakage current from it (diode without passivation) is the worst, over $5.5\,\mathrm{nA/cm^2}$ at $100\,\mathrm{V}$ cathode voltage. The lowest leakage current is Al_2O_3 induced junction diode at O02, the leakage current at $100\,\mathrm{V}$ cathode voltage is approximately $0.6\,\mathrm{nA/cm^2}$. Also on S03 Al_2O_3 induced junction diodes have the lowest leakage current at $100\,\mathrm{V}$ cathode voltage, approximately $1.4\,\mathrm{nA/cm^2}$.

The results from different sized diodes were plotted in two states: partially depleted at $10\,\mathrm{V}$ cathode voltage in figure 32a and after full depletion in figure 32b. The data in latter one is taken as a mean value from measurement of cathode voltages from $40\,\mathrm{V}$ to $50\,\mathrm{V}$ to reduce noise in the data. The estimation of full depletion is done based on the CV results from basic diodes (d = $1650\,\mathrm{\mu m}$) and by comparing the IV results of all different diode sizes. From all five different sizes ($850\,\mathrm{\mu m}$, $1150\,\mathrm{\mu m}$, $1485\,\mathrm{\mu m}$, $2475\,\mathrm{\mu m}$ and $3300\,\mathrm{\mu m}$), two diodes were measured with three gate voltages: $0\,\mathrm{V}$, $2\,\mathrm{V}$ and $3\,\mathrm{V}$. The measurement points in figure 32 are presented as a mean value from those two measurements in the cases there where two successful measurements. The smallest ones were damaged during

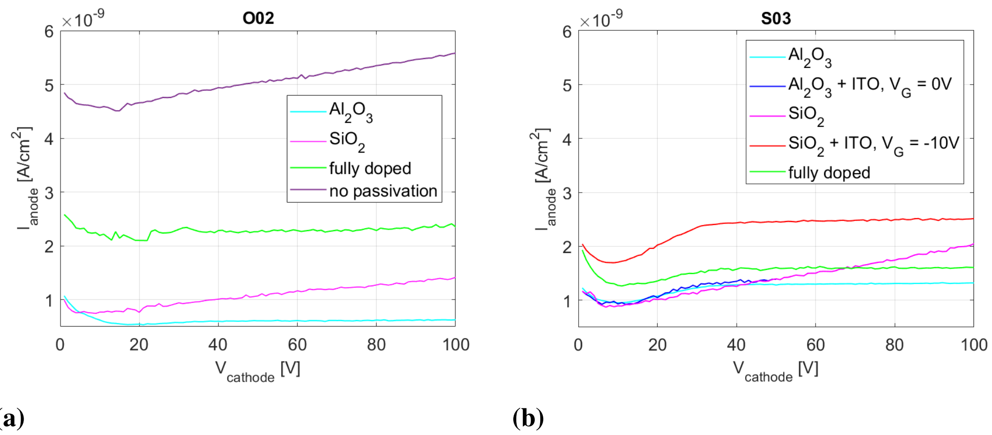


Figure 31. Measurement results from different types of devices from two wafers a) O02, oxidation done at Micronova, b) S03, ITO gates and oxidation done externally.

previous measurements and the data from them was not reliable. Because of that the data from smallest diodes is not included in the plots at all.

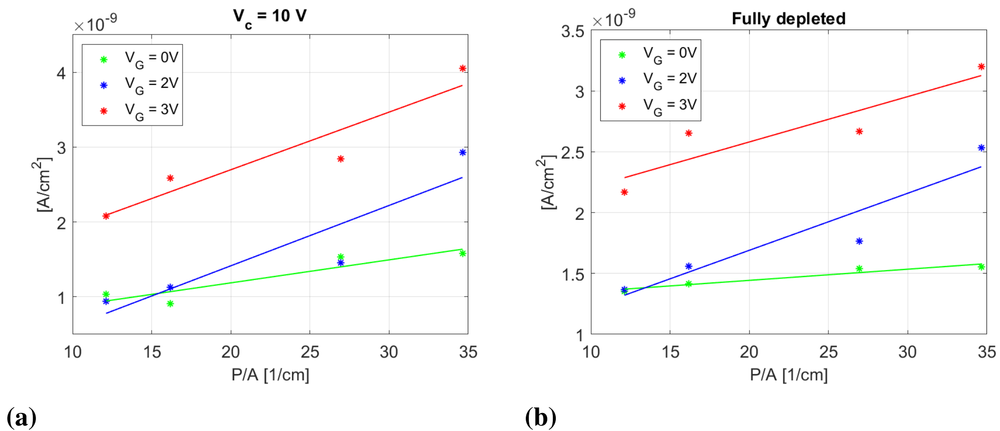


Figure 32. Measured leakage currents from different diode sizes with curve fits to analyze the source of leakage currents. Data from cathode voltage a) 10 V (partially depleted) and b) average from 40 V to 50 V (fully depleted).

Curves in figure 32 were fitted according to equation 4. The equations for those fits are presented in table 7 for partially depleted diodes and in table 8 for the fully depleted data. It is clear in figure 32 that with gate voltages 2 V and 3 V measurement points deviate from the line. The fit was still considered to be good enough as the meaning of it was to get an idea about the major source of leakage current, not analyze it deeply. With $V_G = 0\,\mathrm{V}$ the fit is better. The equations in tables 7 and 8 show that the majority of the leakage current in all cases is from silicon bulk. Small surface leakage current tells that the passivation is successful.

Table 7. Equations for curves fitted in to measurement data from different sizes of diodes with 10 V cathode voltage in figure 32a.

Gate voltage	$I/A = P/A \cdot J_{surface} + J_{bulk}$ [A cm^{-2}]
$V_G = 0$ V	$I/A = (P/A \cdot 0.031 + 0.572) \cdot 10^{-9}$
$V_G = 2$ V	$I/A = (P/A \cdot 0.081 - 0.198) \cdot 10^{-9}$
$V_G = 3$ V	$I/A = (P/A \cdot 0.077 + 1.158) \cdot 10^{-9}$

Table 8. Equations for curves fitted in to measurement data from different sizes of diodes with full depletion cathode voltages in figure 32b.

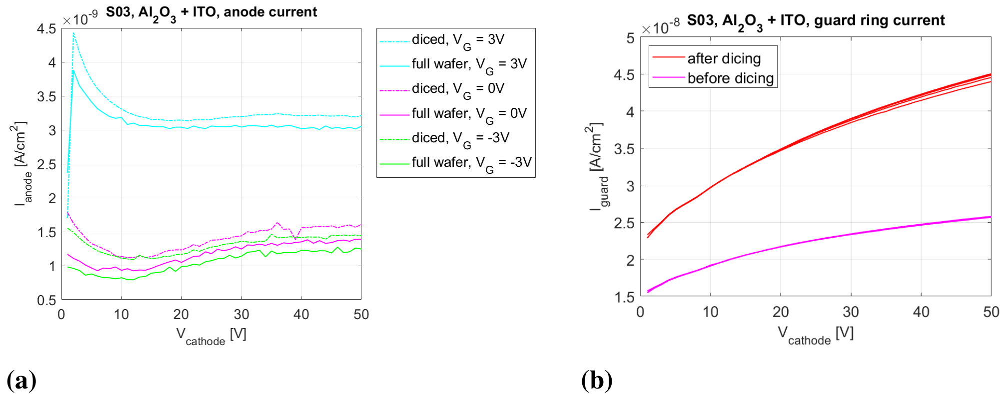
Gate voltage	$I/A = P/A \cdot J_{surface} + J_{bulk}$ [A cm^{-2}]
$V_G = 0$ V	$I/A = (P/A \cdot 0.009 + 1.260) \cdot 10^{-9}$
$V_G = 2$ V	$I/A = (P/A \cdot 0.047 + 0.753) \cdot 10^{-9}$
$V_G = 3$ V	$I/A = (P/A \cdot 0.037 + 1.835) \cdot 10^{-9}$

The slopes from partially depleted detector are steeper in all three cases. That point was chosen from the beginning of measurement and as for example figure 30b shows, around that cathode voltage the leakage current is the lowest in basic diode. The depletion region extends over the full wafer when cathode voltage is 35 V which means that in partially depleted state the diode is more unstable. Also the surface leakage current is higher with lower cathode voltage compared to the fully depleted diodes. The fit to $V_G = 2$ V has negative value for bulk current density. Reason for that is probably that the diode is in very unstable state, as $V_G = 2$ V is the transition voltage from inversion to accumulation and also partial depletion is unstable state.

When diodes are fully depleted, the surface component of the fit decreases with all gate voltages. It is good that the leakage current is smaller when the diode is in the state in which it would usually be operated at.

After most of the IV measurements were done, S03 and S04 wafers were diced into chips to be used in other types of measurements. The diodes were diced into individual 5.5 mm x 5.5 mm chips. Chips were measured after dicing to ensure that it had not damaged the diodes. The results from measurements before and after dicing are shown in figure 33. In figure 33a is shown the change in anode current. At 50 V cathode voltage, the increase in anode current seems to be about $0.2\,\mathrm{nA/cm^2}$ with each presented gate voltage. Figure 33b shows that the guard ring current increased more: about $0.8\,\mathrm{nA/cm^2}$ with low cathode voltages and with 50 V cathode voltage the increase was almost $2\,\mathrm{nA/cm^2}$. The data was chosen to be presented only highlighting the difference caused by dicing because the guard ring current does not depend on the gate voltage. Together these results show what was expected: the anode current did not increase because guard rings stop the leakage

current caused by the the diced edges. Results from graphene gated diodes showed the same results.



(a) **(b)**

Figure 33. Effect of dicing on S03 wafer a) anode currents and b) guard ring current. Results are mean values from Al_2O_3 passivated ITO gated diodes.

4.2 Capacitance - voltage (CV)

4.2.1 Measurement

The capacitance in the detector was measured in capacitance-voltage (CV) measurements and from these measurement results full depletion voltage was derived. At full depletion voltage the depletion region extends through the entire detector bulk. Detectors are often operated on voltages above the full depletion voltage.

CV measurements were all done at HIP Detector Laboratory in Kumpula. The measurement setup is shown in figure 34. The setup consists from LCR meter E4980A, that can be used in frequency range from 20 Hz to 1 MHz. The LCR meter measures impedance of the component using AC signal. The high voltage to the cathode is supplied with Keithley 2410 source meter. The ISOBOX (yellow box in figure 34) is for keeping the high voltage for biasing the detector separated from measured capacitance, essentially protecting the capacitance meter. [38] The setup in figure 34 shows the connections for measuring diodes without gates. For gated diodes, the gate was contacted with another needle which was connected to PS613 DC power supply.

Two different frequencies were tested in measurements, 1 kHz and 1 MHz. It seemed that there was not a big difference in results and most of the measurements were chosen to

do with $1\,\mathrm{MHz}$ frequency. The cathode voltage was sweeped from $0\,\mathrm{V}$ to $100\,\mathrm{V}$ and used gate voltages were $0\,\mathrm{V}$, $1\,\mathrm{V}$, $2\,\mathrm{V}$ and $3\,\mathrm{V}$. Some components were only measured with gate voltages $0\,\mathrm{V}$ and $3\,\mathrm{V}$.

The detector can be thought as a plate capacitor. Biased anode and cathode act as plates of the capacitor and the depletion region is the medium with high resistance. Generally, the capacitance C of a plate capacitor is defined as

$$C = \frac{\varepsilon A}{w}, \tag{5}$$

where ε is total permittivity of the material, A is the area of the capacitor (active area of the detector) and w is the thickness of the capacitor (width of the depletion region). Taking into account relation of the width of the depletion region to bias voltage

$$w = \sqrt{\frac{2\varepsilon V_{bias}}{qN}}, \tag{6}$$

in which where V_{bias} is the bias voltage, q is a charge of an electron and N is charge carrier density in the bulk. Then the capacitance can be written

$$C = A\sqrt{\frac{\varepsilon qN}{2V_{bias}}}, \tag{7}$$

in which all the terms, except for capacitance and bias voltage, are constants. [3] The relation between V_{bias} and C can now be seen as $V_{bias} = 1/C^2$. This is common way for presenting CV measurement data, as it clearly highlights the full depletion of the device.

Determining of the full depletion voltage is shown in practise in figure 35. The beginning (where the red curve is fitted) shows the depletion of the device and the flat part (where pink curve is fitted) shows when the device is fully depleted. The Curve fitting was done by using curve fitting tool in MATLAB and the V_{fd} was determined from crossing point of the two fits.

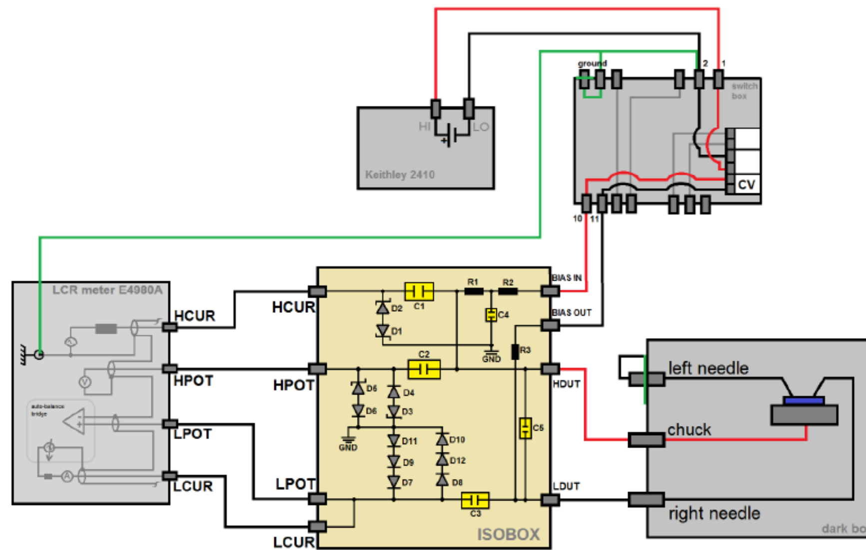


Figure 34. CV measurement setup at Kumpula. The picture shows connections for diodes without gates. From [38].

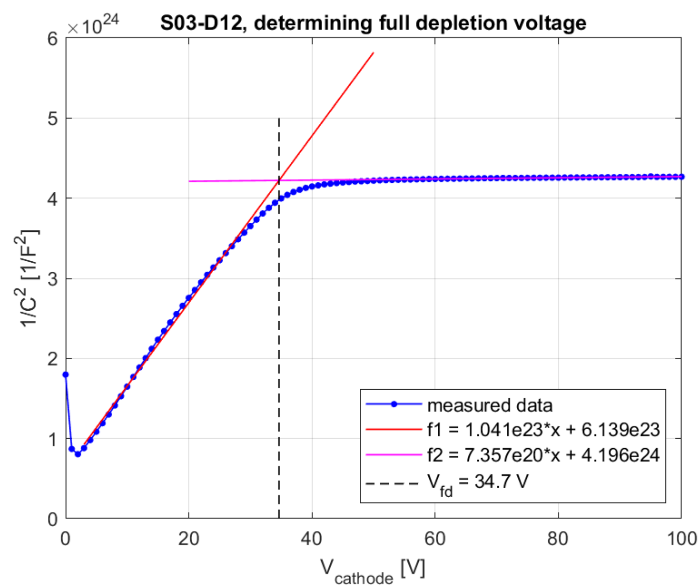


Figure 35. Schematic for determining the full depletion voltage.

4.2.2 Results and discussion

CV measurement data from ITO gated diode is shown in figure 36. The figure shows that the capacitance decreases as the gate voltage increases. This can probably be explained by reduction of negative charge in the Al_2O_3 layer. When positive voltage is applied to the gate, it starts to cancel negative fixed charge in Al_2O_3 until at $V_G = 2\,V$ it is fully cancelled and the diode shifts to accumulation state.

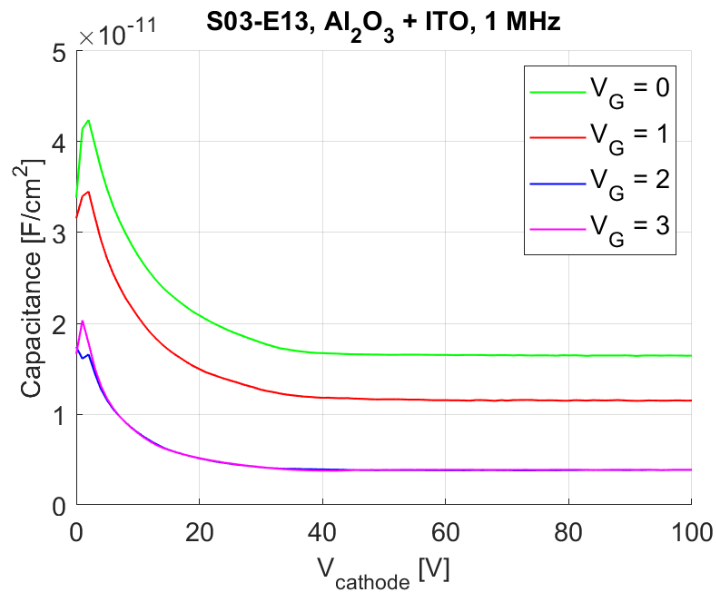
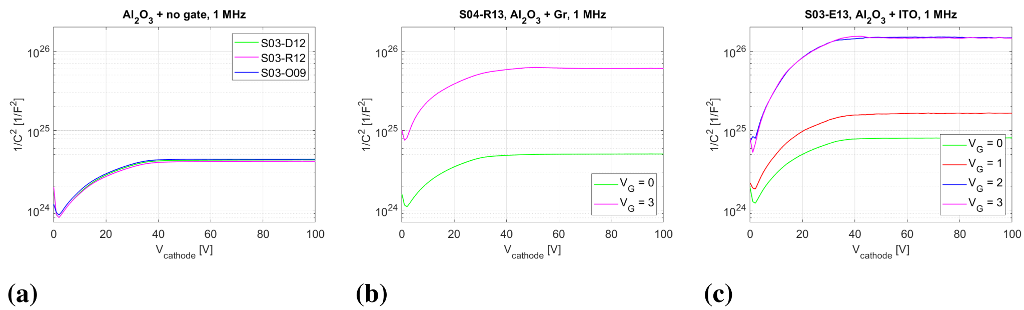


Figure 36. CV curves from a gated diode.

In figure 37 is shown the measured CV data in V - 1/C^2 form and the full depletion voltages determined from those curves are shown in table 9. All measured detectors have Al_2O_3 induced junction, and S03-E13 has ITO gate and S04-R13 has graphene gate. The V_{fd} can be rounded to 35 V in almost all cases. The results are only from limited group of detectors because only small batch was chosen for these further tests.

Table 9. Calculated full depletion voltages.

Device	no gate V_{fd} [V]	$V_G = 0V$ V_{fd} [V]	$V_G = 1V$ V_{fd} [V]	$V_G = 2V$ V_{fd} [V]	$V_G = 3V$ V_{fd} [V]
S03-D12	34.7				
S03-R12	35.4				
S03-O09	34.8				
S03-E13		35.1	35.9	35.3	34.5
S04-R13		32.8			35.2



(a) **(b)** **(c)**

Figure 37. Measurement data plotted in 1/C^2 form. Full depletion voltages were detemined from these curves.

Having a low full depletion voltage even with thick silicon ($675\,\mu\mathrm{m}$) tells that the doping level of the silicon wafer is really low. The full depletion voltage tells mainly about quality of the silicon that was used as a base for the detectors. Low full depletion voltage allows operating the detector in fully depleted state with relatively low reverse bias voltages. The charge carrier density in the bulk was solved using equation 6 to be about $1 \times 10^{11}\,\mathrm{cm}^{-3}$. That corresponds to wafer resistivity about $44\,\mathrm{k}\Omega\,\mathrm{cm}$ [43]. The purity of silicon is really good as the resistivites commonly used in particle detection are $1\,\mathrm{k}\Omega\,\mathrm{cm}$ to $10\,\mathrm{k}\Omega\,\mathrm{cm}$. For a commercial production it would be too expensive to use wafers with over $40\,\mathrm{k}\Omega\,\mathrm{cm}$ resistivity.

4.3 Transient current technique (TCT)

4.3.1 Measurement

Detector reactivity to light was tested with transient current technique (TCT) measurements using red laser (λ = $660\,\mathrm{nm}$). In TCT measurement the detector active area is illuminated with laser and current generated by charge carriers is measured.

The red laser does not penetrate far into the silicon bulk which means that the measured charge carriers are formed near the surface. The shape of the measured curve depends on the type of majority charge carriers. [4] In the case of detectors studied in this thesis, the bulk is n-type, the induced junction at the front side of the wafer is p-type and the backside of the wafer is fully implanted into n-type. That means that the charge carriers read from the front side of the wafer are holes and the electrons are collected to the back. The measured signal consists from the fast collection of holes and the drift of electrons through the wafer [4]. The mobility of holes is almost three times less than the mobility of electrons (at room temperature electrons $1350\,\mathrm{cm}^2/\mathrm{Vs}$ and holes $480\,\mathrm{cm}^2/\mathrm{Vs}$ [1]) but

in the case of red laser the charge carriers are generated near the illuminated top surface. This leads to holes reaching the electrode faster than the electrons drifting through the thick silicon bulk.

When TCT measurement is repeated with different bias voltages, the expected outcome is that with higher bias voltages the peak current increases and the drift of minority charge carriers becomes shorter. When the detector is not yet fully depleted, the drift continues with the same slope until end of the measurement. When the detector is fully depleted, there is sharp shift in the curve indicating that the minority charge carriers have reached the electrode.

TCT measurements were done at HIP Detector Laboratory at Kumpula. Five detectors were measured in total. All of them had Al_2O_3 induced junction: two without gates, two with ITO gate and one with graphene gate. For measurements, detectors diced into individual $5.5\,\mathrm{mm}$ x $5.5\,\mathrm{mm}$ chips were wire bonded into printed circuit board (PCB). Wire bonds were made to anode, guard ring and gate (in the case of gated diodes). For biasing, the cathode was contacted through metal underneath it. The schematic of measurement is shown in figure 38. The connections are shown directly into the detector for clarity. Bonded detector attached to the sample holder in TCT measurement setup is shown in figure 39.

The measurement was done with fixed cathode voltages, the amount of used voltages varied between measurements. For gated diodes the measurement was done with gate voltages $0\,\mathrm{V}$, $1\,\mathrm{V}$, $2\,\mathrm{V}$ and $3\,\mathrm{V}$. The gate bias was supplied through the same PS613 DC power supply as in CV and IV measurements. The laser was triggered at $50\,\mathrm{Hz}$ to $60\,\mathrm{Hz}$ rate and same trigger rate was used also for the oscilloscope. The laser power was $500\,\mathrm{mW}$.

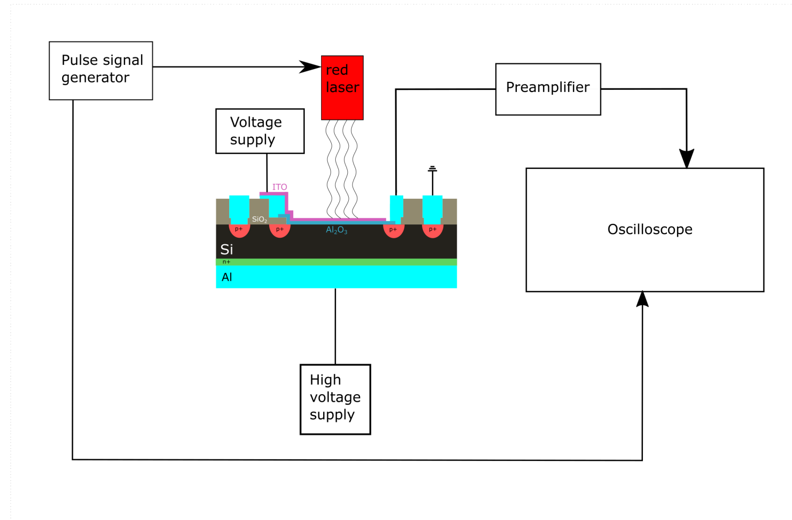


Figure 38. Measurement setup schematic for TCT measurements. Based on [44].

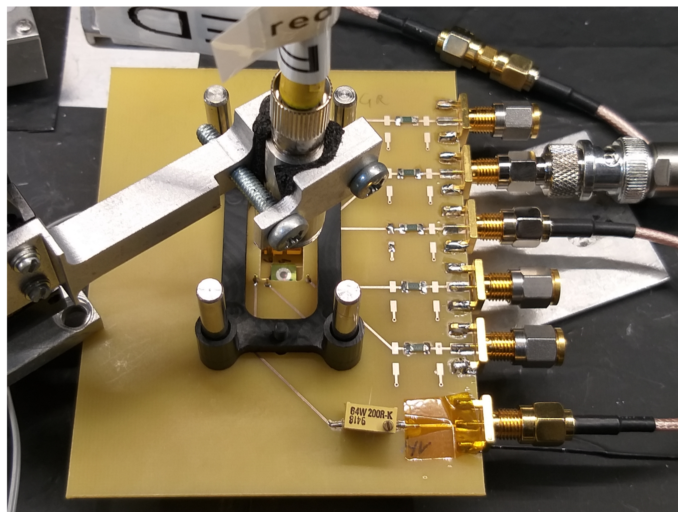


Figure 39. Diode in sample holder for TCT measurements. On right side there are three connections (from top of the picture to bottom): guard ring to ground, voltage supply to gate, reading the signal from anode and bias to the backside (cathode).

4.3.2 Results and discussion

Results for induced junction diode is shown in figure 40. The curves show, that the detector is not fully depleted with bias voltages under $40\,\mathrm{V}$. Bias voltages higher than that show the distinct sharp increase in the slope. Otherwise the result shows what was expected: by increasing bias voltage, the peak of transient current increases and the full collection on electrons happens faster.

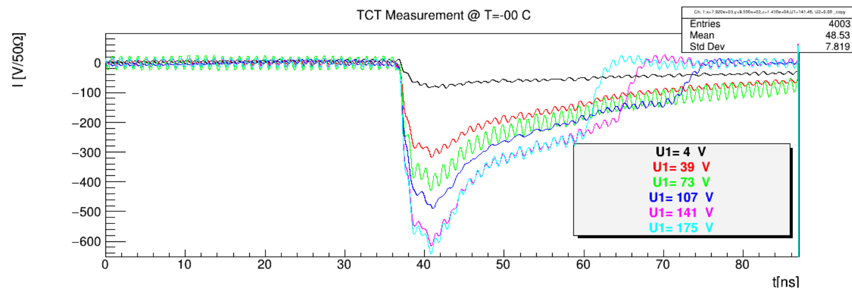


Figure 40. TCT measurement from Al_2O_3 diode without gate (S03-O09).

Results with two different gate voltages are shown in figure 41: at $V_G = 0\,\mathrm{V}$ (fig. 41a) and at $V_G = 3\,\mathrm{V}$ (fig. 41b). Overall, it seems that gate does not have large impact in operation of the diode while illuminated with red laser. The sharp increases indicating full depletion with $0\,\mathrm{V}$ gate voltage look quite similar to the one without gate. The increase starts quite suddenly in the middle of the curve. When the gate voltage is $3\,\mathrm{V}$ the current is a bit lower than with $0\,\mathrm{V}$. That could mean that the charge carrier lifetime is shorter when the diode is in accumulation. It is also possible that in accumulation some holes are not collected at the anode contact. In accumulation there is positive charge in the silicon surface which causes holes getting pushed into the bulk and making it more difficult to get to the surface to be collected. With both gate voltages the gate also seems to have an effect to shift the curves into positive currents after all the holes are collected. In diodes without gate this was not observed. Reason for that could be that in addition to bias applied to the backside of the diode there is also the voltage applied to the gate. That might lead to higher electric field and maybe to some capacitive phenomenon.

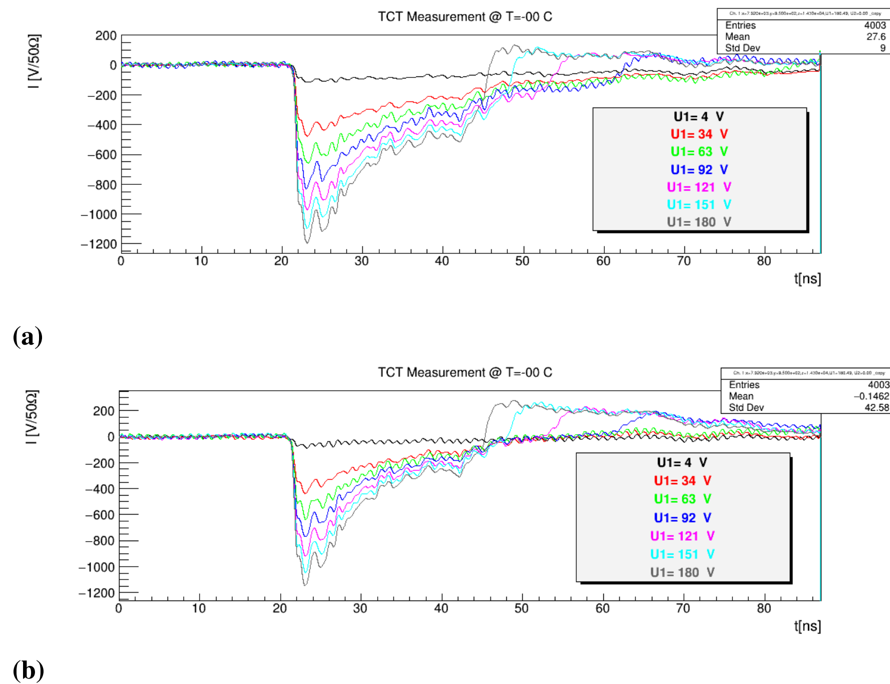


Figure 41. TCT measurement from Al_2O_3 + ITO gated diode (S03-T13) at a) $V_G = 0\,\mathrm{V}$ and b) $V_G = 3\,\mathrm{V}$.

4.4 Radiation

4.4.1 Measurement

The operation of the detectors was tested with radioactive isotope samples. Used isotopes were Am-241, Ba-133, Cs-137 and Co-57 and the measurements focused in gamma ray energy range. The characteristic peaks of these isotopes are well known which makes them good for testing detectors. This measurement was done in HIP Detector Laboratory.

For the measurement the wire bonded detector was placed in metallic sample holder. The anode was contacted with a pin for biasing and readout. Guard ring was left floating as there was no contact. Having fully enclosed sample holder was important to prevent any additional signal from light in the laboratory. During the measurement disk shaped radiation sources were placed on top of the sample holder containing the detector. Detector was biased to be fully depleted, with voltages ranging from $-50\,\mathrm{V}$ to $-100\,\mathrm{V}$. Negative voltages were needed for reverse biasing the detector from anode. Due to time constraints and challenges in making gate contact, only two devices without gate were characterized.

The detector in the sample holder was connected to a charge sensitive amplifier (CSA), Amptek CoolFET. The output from preamlifier goes to Cremat CR-160 shaping amplifier,

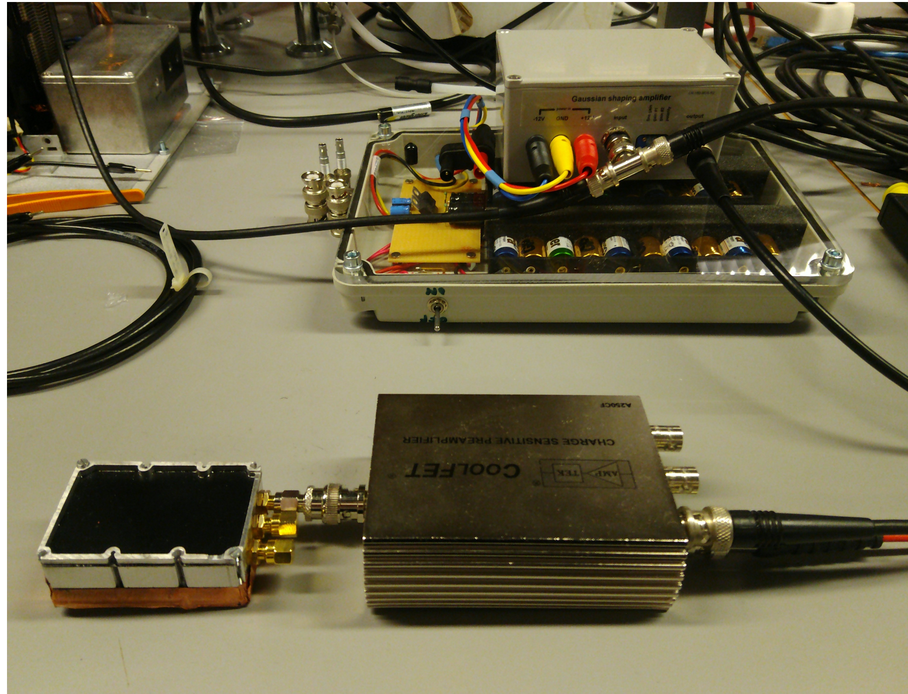


Figure 42. The basis of radiation measurement setup: at the front is the sample holder attached to preamplifier and at the back is shown the shaping amplifier.

Table 10. Gamma ray energies for four radiation sources with probabilities for their emission. Only the energies that were observed or were in the range that could have been observed are included.

Am-241 [45]		Ba-133 [46]		Co-57 [47]		Cs-137 [48]	
E_g [keV]	%	E [keV]	%	E [keV]	%	E [keV]	%
60	36	31	99	122	86	32	6
		81	34	136	11	662	85

which has CR-200-250ns shaper module. In shaping amplifier the noise is removed and the signal is shaped into gaussian pulses. Then the height of the pulse is measured and organized into a histogram with multichannel analyzer (MCA), Amptek MCA-8000D. In the histogram x-axis is the channel number (corresponding to the energy deposited into the detector) and y-axis is the number of particles detected on each channel. The sample holder with amplifiers is shown in figure 42. Energies of gamma rays of the four radiation sources are well known in the literature and those are shown in table 10. The x-axis was scaled to energy (keV) using the strongest peaks, $60\,\mathrm{keV}$ peak from Am-241 and $31\,\mathrm{keV}$ peak from Ba-133.

For further analysis of detector performance, energy resolution ER was calculated for some of the strongest peaks. The energy resolution tells about the detection accuracy of the detector. The smaller the energy resolution is, the better. The best silicon detectors

have energy resolution under $1\,\%$. The energy resolution is determined

$$ER = \frac{\text{FWHM}}{E(peak)}, \tag{8}$$

where FWHM is the full width at half maximum of the peak and $E(peak)$ is the energy of the peak center. [1] A gaussian distribution was fitted into the data to determine the FWHM. The fitting and calculations were done using MATLAB's fitting tools. The fitted curve as a function of energy E is

$$f(E) = a \cdot \exp\left(-\left(\frac{E-b}{c}\right)^2\right), \tag{9}$$

where a, b and c are parameters that are determined in the fit. Then with those parameters

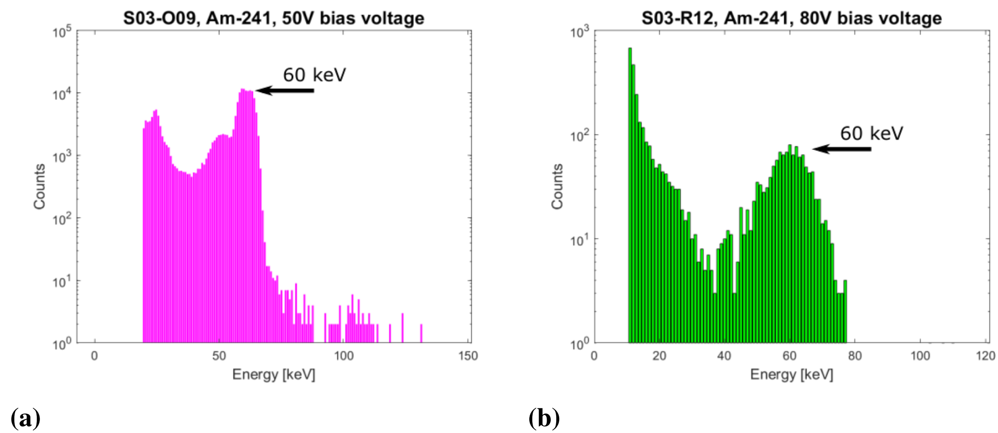
$$\text{FWHM} = 2c\sqrt{\log(2)}. \tag{10}$$

4.4.2 Results and discussion

Measured radiation spectrums from Am-241 are shown in figure 43 and spectrums from Ba-133 are shown in figure 44. The measurement setup was not optimized for measuring these particular detectors and possibly because of that there was something wrong with the rest of the measurements. Because of having unreliable data from Cs-137 and Co-57 the results from those is not shown. All of the measurements were quite noisy at the measurement threshold (smallest measured values). Some of the noise might be caused by backscattering or decays from other isotopes that have been formed in the sources within time.

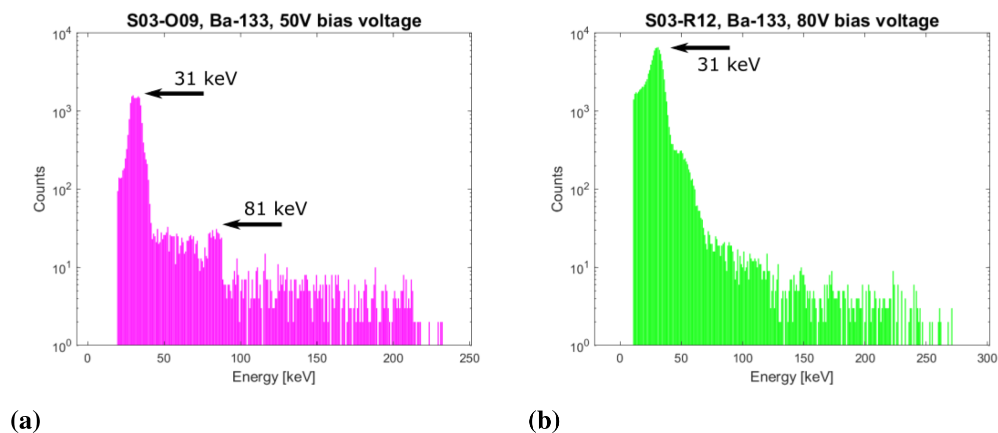
With Am-241 source the amount of recorded hits in S03-O09 is almost double of the hits in S03-R12. The most probable reason for that is that S03-O09 was measured for $300\,\mathrm{s}$ and S03-R13 only for $85\,\mathrm{s}$. For all other measurements the length of the measurements was about $300\,\mathrm{s}$. The bias voltages were different with each detector but the effect of that should not be very large.

It seems that lower energies ($30\,\mathrm{keV}$ to $100\,\mathrm{keV}$) are detected better than other energies. Cs-137 should have its strongest peak at $662\,\mathrm{keV}$ but it was not detected with neither of two tested detectors. The two strongest peaks of Co-57 are $122\,\mathrm{keV}$ and $136\,\mathrm{keV}$. Only



(a) **(b)**

Figure 43. Am-241 measurement results from a) S03-O09 and b) S03-R12.



(a) **(b)**

Figure 44. Ba-133 measurement results from a) S03-O09 and b) S03-R12.

$122\,\mathrm{keV}$ peak was faintly detected (less than 10 particles during $300\,\mathrm{s}$) with S03-O09. With S03-R12 neither of those peaks was detected. But there were many inconsistencies in the measurements that making any conclusions would require further measurements with more optimized setup and measurement conditions. The measurement conditions, like bias voltage, should be same in each measurement.

The energy resolution was calculated for Am-241 $60\,\mathrm{keV}$ peak from both detectors and for Ba-133 $31\,\mathrm{keV}$ peak measured from S03-O09. The fitted gaussian distribution for S03-O09 Am-241 is shown in figure 45 and the calculated values for FWHM and energy resolutions are presented in table 11.

The variation between energy resolutions from different measurements is large and the values of energy resolution are high. As there were many inconsistencies between the measurements it is difficult to say what caused this variation. With more optimized measurement conditions the results could be better. Already in 1990s the best commercial

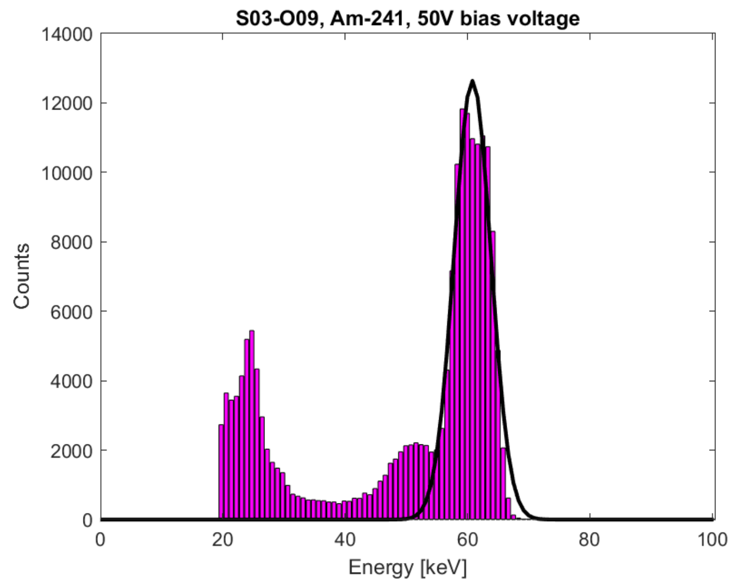


Figure 45. Gaussian fitted to S03-O09 $60\,\mathrm{keV}$ peak from Am-241 measurement.

Table 11. Energy resolutions calculated for three measurements.

	FWHM [keV]	Energy resolution [%]
S03-O09		
Am-241	7.1	12
Ba-133	8.2	26
S03-R12		
Am-241	12	21

silicon PIN diode detectors were reported to have FWHM less than $3\,\mathrm{keV}$ from Am-241 $60\,\mathrm{keV}$ peak in room temperature [49]. In study where same four isotopes were used to test silicon PIN diode detectors, the energy resolutions for $650\,\mu\mathrm{m}$ thick detectors were reported to be in range $1.3\,\mathrm{keV}$ to $10.2\,\mathrm{keV}$ [50].

5 CONCLUSIONS

Silicon PIN diode detectors were fabricated on four wafers. The focus was on diodes with gate induced passivation but design included also other types of diodes for comparison. Two thin, transparent gate materials were tested: graphene and indium tin oxide (ITO). Diode types were Al_2O_3 induced junction diode, Al_2O_3 with graphene and ITO gates, fully boron doped, SiO_2 passivated and SiO_2 passivated with ITO gate. The graphene transfer process was not optimized which caused some degradation in diodes with graphene gates.

Diodes were characterised with four types of measurements: reverse IV and CV, TCT with red laser and radiation with radioactive isotopes. IV measurements were the main characterisation method, different types of diodes from all four wafers were measured. In CV and TCT measurements the focus was on Al_2O_3 induced junction diodes with and without gate. Due to limited time for measurements the radiation measurements were done only for diodes without gates.

The transition from inversion to accumulation happened at $-2\,\mathrm{V}$ with Al_2O_3 induced junction gated diodes and with SiO_2 passivated ones at $4.5\,\mathrm{V}$. The gate material did not affect on the transition current in the case of Al_2O_3. SiO_2 passivated diodes were fabricated only with ITO gate. The level of leakage current in fully depleted diode in inversion was about $1.4\,\mathrm{nA\,cm^{-2}}$ for Al_2O_3 with ITO gate and about $2.4\,\mathrm{nA\,cm^{-2}}$ for both Al_2O_3 with graphene gate and SiO_2 with ITO gate. The full depletion voltage was determined from $1/C^2 - V$ graphs to be $35\,\mathrm{V}$.

The differences between wafers after different back-end processing steps were noticeable. In Al_2O_3 induced junction diodes the variation of leakage current in fully depleted diode was almost $1.5\,\mathrm{nA\,cm^{-2}}$ between the lowest and highest.

The TCT measurement showed that the Al_2O_3 gated diodes have a good response to red laser. When the diode was in accumulation, the charge carrier lifetime seemed to be shorter and the detector photoresponse was lower than when the diode was in inversion. The data from radiation measurements was unreliable for the most part, but the strongest peaks were detected.

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