Lappeenranta
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ACTIVE INVERTER OUTPUT FILTERING METHODS

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Abstract

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Frequency converters are widely used in the industry to enable better controllability and efficiency of variable speed AC motor drives. Despite these advantages, certain challenges concerning the inverter and motor interfacing have been present for decades. As insulated gate bipolar transistors entered the market, the inverter output voltage transition rate significantly increased compared with their predecessors. Inverters operate based on pulse width modulation of the output voltage, and the steep voltage edge fed by the inverter produces a motor terminal overvoltage. The overvoltage causes extra stress to the motor insulation, which may lead to a premature motor failure. The overvoltage is not generated by the inverter alone, but also by the sum effect of the motor cable length and the impedance mismatch between the cable and the motor. Many solutions have been shown to limit the overvoltage, and the mainstream products focus on passive filters.

This doctoral thesis studies an alternative methodology for motor overvoltage reduction. The focus is on minimization of the passive filter dimensions, physical and electrical, or better yet, on operation without any filter. This is achieved by additional inverter control and modulation. The studied methods are implemented on different inverter topologies, varying in nominal voltage and current.

For two-level inverters, the studied method is termed active du/dt. It consists of a small output LC filter, which is controlled by an independent modulator. The overvoltage is limited by a reduced voltage transition rate. For multilevel inverters, an overvoltage mitigation method operating without a passive filter, called edge modulation, is implemented. The method uses the capability of the inverter to produce two switching operations in the same direction to cancel the oscillating voltages of opposite phases. For parallel inverters, two methods are studied. They are both intended for two-level inverters, but the first uses individual motor cables from each inverter while the other topology applies output inductors. The overvoltage is reduced by interleaving the switching operations to produce a similar oscillation accumulation as with the edge modulation.

The implementation of these methods is discussed in detail, and the necessary modifications to the control system of the inverter are presented. Each method is experimentally verified by operating industrial frequency converters with the modified control. All the methods are found feasible, and they provide sufficient overvoltage protection. The limitations and challenges brought about by the methods are discussed.

Keywords: AC motor drives, active filter, AC motor protection, industrial power system transients, overvoltage protection
UDC 621.313.3:621.316.94

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It is very likely that the person who has read this thesis most thoroughly is Dr. Hanna Niemelä. She helped this thesis become readable, at least languagewise. Thank you for your diligent effort.

Luckily, I did not have to carry the full weight of the research on my own. Instead, I had a chance to work with a bunch of bright minds. I would like to thank Dr. Juha-Pekka Ström for being a mentor, sharing your insight into the field of research, and contribution to the development of the methods. For Mr. Juho Tyster, thank you for challenging my ideas, giving valuable input on how to improve them, and all the help in the lab. The work ethic of Dr. Ville Naumanen rubbed off on me. Thank you for the guidance and the hectic research burst that we shared in your sauna of an office. For Dr. Toni Itkonen, thank you for sharing your expertise in the field of parallel inverters. In addition, I would like to thank the people at the office for the more or less fruitful discussions over coffee. It has been an absolute pleasure working with all of you.

The financial support for this work by the Finnish Foundation for Technology Promotion, Emil Aaltonen Foundation, and Lauri and Lahja Hotinen Fund is most sincerely appreciated.

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Lappeenranta, September 14th, 2012

Juhamatti Korhonen

Contents

List of Symbols and Abbreviations

Roman letters

c	Speed of light
C_{DC}	DC link capacitance
C_f	Filter capacitance
f_{osc}	Voltage oscillation frequency
i	Current
i_{cap}	Filter capacitor current
i_{circ}	Circulating current among parallel inverters
i_{load}	Load current
i_{output}	Inverter output current
$i_{output1}$	Inverter output current of parallel inverter 1
$i_{output2}$	Inverter output current of parallel inverter 2
l_c	Motor cable length
L_f	Filter inductance
L_{load}	Load inductance
L_{p1}	Transmission line model parallel inductance 1
L_{p2}	Transmission line model parallel inductance 2
L_s	Transmission line model series inductance
n	Number of parallel inverters
R_f	Filter resistance
R_{load}	Load resistance

R_{p1}	Transmission line model parallel resistance 1
R_{p2}	Transmission line model parallel resistance 2
R_{s}	Transmission line model series resistance
t	Time
t_{cp}	Active $\mathrm{d}u/\mathrm{d}t$ charge period duration
t_{cpulse}	Active $\mathrm{d}u/\mathrm{d}t$ charge pulse duration
t_{d}	Propagation delay
t_{icpulse}	Active $\mathrm{d}u/\mathrm{d}t$ current correction pulse duration
t_{r}	Voltage rise time
t_{t}	Voltage transition time
u	Voltage
u_{cap}	Filter capacitor voltage
u_{DC}	DC link voltage
u_{motor}	Motor voltage
$\hat{u}_{\mathrm{motor}}$	Motor peak voltage
u_{output}	Inverter output voltage
u_{output1}	Inverter output voltage of parallel inverter 1
u_{output2}	Inverter output voltage of parallel inverter 2
u_{output3}	Inverter output voltage of parallel inverter 3
u_{pulse}	Voltage pulse amplitude
u_{ref}	Modulator voltage reference signal
Z_{c}	Motor cable impedance
Z_{L}	Motor terminal impedance for a single voltage edge with parallel cables connected to the motor
Z_{m}	Motor transient impedance

Greek letters

Δt_{sw}	Time interval between switching operations used to accumulate consecutive voltage oscillations
Γ_{M}	Motor reflection coefficient

Γ_S	Inverter reflection coefficient

Acronyms

AC	Alternating current
CHB	Cascaded H-bridge inverter
DC	Direct current
DTC	Direct torque control
EMI	Electromagnetic interference
FC	Flying capacitor inverter
IGBT	Insulated gate bipolar transistor
IM	Induction motor
LC	Electrical circuit consisting of an inductor and a capacitor
LCR	Electrical circuit consisting of an inductor, a capacitor, and a resistor
LR	Electrical circuit consisting of an inductor and a resistor
M^2C	Modular multilevel converter
NPC	Neutral point clamped inverter
PEBB	Power electronic building block
PVC	Polyvinyl chloride
PWM	Pulse width modulation
RC	Electrical circuit consisting of a resistor and a capacitor
VSI	Voltage source inverter

List of publications

Publication **I**:

Korhonen, J., Ström, J.-P., Tyster, J., Sarén, H., Rauma, K. & Silventoinen, P. (2009), "Control of an Inverter Output Active du/dt Filtering Method," in *Proceedings of the 35th Annual Conference of the IEEE Industrial Electronics Society, IECON 2009.*

Publication **II**:

Ström, J.-P., Korhonen, J., Tyster, J. & Silventoinen, P. (2011), "Active du/dt — New Output Filtering Approach for Inverter-Fed Electric Drives," *IEEE Transactions on Industrial Electronics*, vol. 58, pp. 3840–3847.

Publication **III**:

Naumanen, V., Korhonen, J., Silventoinen, P. & Pyrhönen, J. (2010), "Mitigation of High du/dt-originated Motor Overvoltages in Multilevel Inverter Drives," *IET Power Electronics*, vol. 3, pp. 681–689.

Publication **IV**:

Naumanen, V., Korhonen, J., Silventoinen, P. & Pyrhönen, J. (2011), "Multilevel Modulation Method for Mitigation of High du/dt-Originated Oscillating Overvoltages at Motor Terminals," *IET Power Electronics*, vol. 4, pp. 29–38.

Publication **V**:

Korhonen, J., Itkonen, T., J., Ström, J.-P., Tyster, J. & Silventoinen, P. (2012), "Active Motor Terminal Overvoltage Mitigation Method for Parallel Voltage Source Inverters," *IET Power Electronics*, accepted for publication.

Publication **VI**:

Korhonen, J., Itkonen, T., J., Ström, J.-P., Tyster, J. & Silventoinen, P. (2012), "Active Motor Terminal Overvoltage Suppression Method for Parallel Inverters with Output Inductors," *International Review of Electrical Engineering*, accepted for publication.

Chapter 1

Introduction

Electromechanical conversion is a key contributor in today's energy systems. Processes involving electric motors account for a vast majority of electrical energy consumption. The industry employs fans, pumps, and compressors, and most of these drives still operate at a fixed speed. This means that they consume a constant amount of electrical power, even though the load varies. This leads to the loss of energy when operating below nominal load, as the flow is adjusted mechanically, for example by valves. The use of variable speed AC motor drives has been found to be a much more energy-efficient method for these applications. Here, power electronics represents an advancement in energy savings and enables control of the torque and speed of the motor, enhancing the performance of the drive (Bose, 2000, 2009).

A traditional voltage source inverter (VSI) topology is illustrated in Figure 1.1. The grid AC voltage is converted to the DC voltage by a diode rectifier. The DC link capacitance C_{DC} functions as a filter by reducing the intermediate circuit voltage ripple. The inverter is used to control the output current frequency and amplitude by modulating the output voltage. By pulse width modulation (PWM), a desired voltage mean value can be produced for a switching frequency period. A PWM-modulated inverter output voltage and a reference signal used to generate the voltage waveform are presented in Fig. 1.2. The PWM method and the switching frequency of the inverter and the load impedance define the load current ripple. If the load impedance is assumed constant, the load current ripple can be reduced by increasing the inverter switching frequency.

Even though other power switches are used in power electronic applications, an insulated gate bipolar transistor (IGBT) is the current mainstream device for low-voltage inverters. The low-voltage range is defined up to 1.5 kV DC voltage and 1 kV AC voltage. The improvements in the IGBT technology have enabled the increase in the inverter efficiency.

The power rating of an inverter can be increased by varying the inverter topology either by paralleling the devices or by connecting them in series. The parallel connection increases the current rating of the device, and it can be done within a power switch at the semiconductor

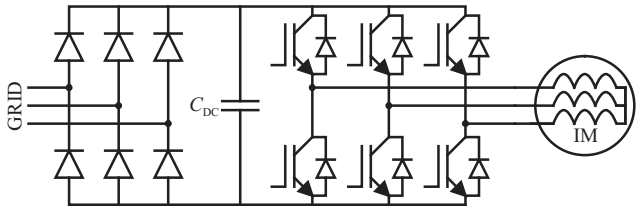


Figure 1.1. Three-phase frequency converter feeding an induction motor.

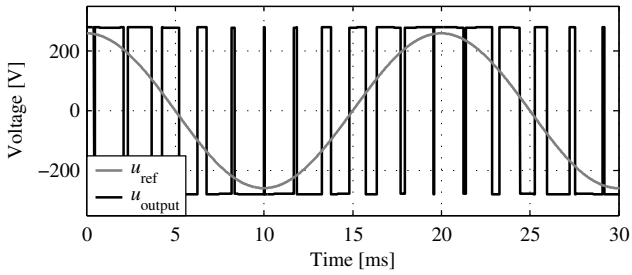


Figure 1.2. Two-level VSI output voltage and the corresponding modulator reference signal.

level (Azar et al., 2008). If paralleling of chips inside a single casing becomes inconvenient, for example for manufacturing reasons, IGBTs can be connected in parallel in a single inverter (Bortis et al., 2008). Even larger units can be constructed and connected in parallel. These elements can be referred to as power electronic building blocks (PEBBs). This way, entire frequency converters can be assembled modularly to feed a single load (Kawabata and Higashino, 1988).

The other method to increase the power rating of an inverter is to raise the voltage by series connection. Rather than connecting power switches in series to produce a two-level inverter, the emphasis is now on multilevel inverters. By definition, a multilevel inverter is capable of producing an output phase voltage with at least three voltage levels. The most acknowledged multilevel inverter topologies are the neutral point clamped inverter (NPC), the flying capacitor (FC), the cascaded H-bridges (CHB), and the modular multilevel converter (M^2C) (Nabae et al., 1981; Franquelo et al., 2008; Malinowski et al., 2010; Glinka and Marquardt, 2005). These multilevel inverters are able to handle medium voltages even when the basic switch component is a low-voltage IGBT. The multilevel inverter topologies vary in modularity. For NPC and FC inverters, the structure is nonmodular, but in the CHB and M^2C cases the inverter stage can use a series connection to increase the voltage rating and the number of output voltage levels modularly. For example, a cascaded H-bridge inverter with three series-connected PEBBs is able to produce seven output voltage levels. Such a topology is shown in Figure 1.3. Even though multilevel inverters are generally considered to be medium-voltage converters, three-level inverters are also very applicable to low-voltage drives (Teichmann and Bernet, 2005; Lee and Yao, 2011).

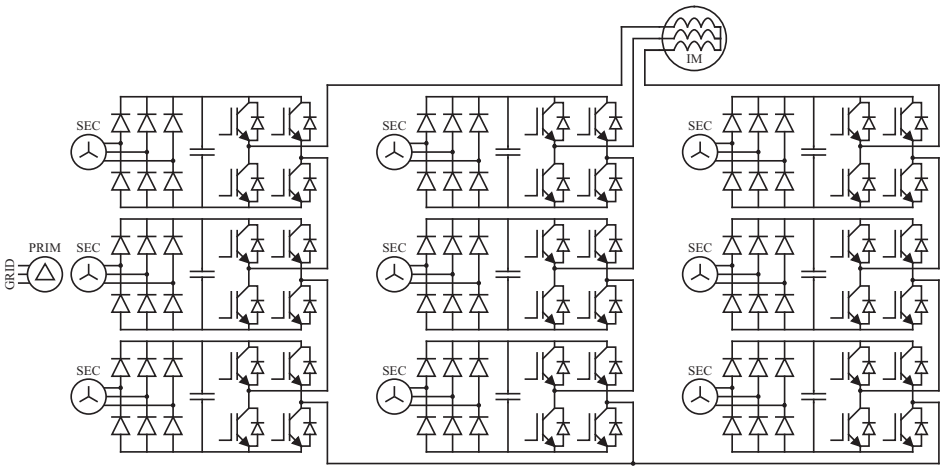


Figure 1.3. Cascaded H-bridge topology.

The reason why multilevel inverters are so appealing for AC drives, especially for high-power applications, is their more sinusoidal output voltage waveform compared with traditional two-level inverters. A seven-level inverter output voltage is illustrated in Figure 1.4. The switched voltage is lower compared with the nominal voltage. The switching frequency seen at the output of the inverter, or the apparent switching frequency, is a sum of the switching frequencies of each PEBB. For the same apparent switching frequency, each IGBT has to be switched less frequently in a multilevel inverter than in a two-level inverter. For these reasons, the load current ripple is proportionally lower for a multilevel inverter.

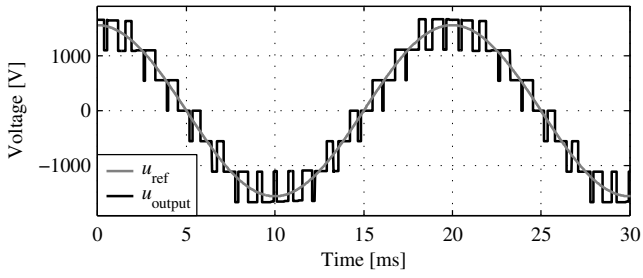


Figure 1.4. Inverter output voltage for a seven-level cascaded H-bridge topology and the modulator reference signal used to generate the voltage.

1.1 Motivation of the work

Despite the obvious advantages in controllability and efficiency, the frequency converters pose challenges with the input and output interfacing. The grid interface is regulated so that the converter may only generate a certain amount of harmonics to the grid (IEEE, 1993; IEC, 2008, 2011). This is usually handled with various types of grid filters (Mohan et al., 2003) or with a combination of an active rectifier and a passive filter (Liserre et al., 2005).

On the output inverter side, two major fault contributors have been reported. Both of these result from advancements in the IGBT technology, and occur in the form of the increased $\mathrm{d}u/\mathrm{d}t$ of the output voltage. The first problem is the motor terminal overvoltage caused by an impedance mismatch between the motor cable and the motor stator inductance. The overvoltage may result in a premature stator insulation failure (Persson, 1992). The impedance mismatch would not be a problem if the voltage fed to the motor were sinusoidal. The problem arises when the voltage fed from the inverter is pulse width modulated. The overvoltage occurs when the transition time of the voltage edge is proportionally short compared with the propagation delay. These criteria are met when the frequency converter and the load are placed at least several meters apart. Several filtering applications have been proposed to reduce the overvoltage.

The second potential fault source is bearing faults caused by the current flowing through the bearings. The bearing currents may result from a magnetic asymmetry in the motor; however, today the more likely fault mechanism is the common-mode voltage and the high $\mathrm{d}u/\mathrm{d}t$ transitions of the voltage fed by the inverter (Link, 1999). A standard two-level inverter always produces a common-mode voltage to the load. The common-mode voltage can be significantly reduced by a sinusoidal filter placed at the output of the inverter (Steinke, 1999; Rodriguez et al., 2006). The common-mode voltage peak value can be reduced for a two-level VSI by modulation (Tallam et al., 2010). With multilevel inverters, the common-mode voltage can be reduced proportionally compared with two-level inverters. However, for medium-voltage inverters, the absolute value of the common-mode voltage may remain at concerning levels (Naumanen, 2010; Naumanen et al., 2010).

1.2 Objective of the work

The viable motor terminal overvoltage filtering solutions of today are limited to passive approaches that either reduce the output voltage transition rate or match the impedances of the cable and the motor (Finlayson, 1998; Steinke, 1999; Habetler et al., 2002; Moreira et al., 2002, 2005; Akagi and Matsumura, 2011). A common component for the inverter output filters is an inductor. It is commonly the physically largest component in the filter, and it causes a voltage drop according to the inductance. The drop has to be compensated by the inverter, but this can be done only to a certain extent. One of the objectives is to reduce the electrical and physical size of the inductor, which may also lead to a more efficient filtering solution.

The main objective is to study filtering solutions that minimize the passive filter component size and provide sufficient overvoltage reduction. These targets are met with four different solutions that apply additional and revised inverter modulation. The additional modulation is used either to control the passive filter element, or to use the inherent voltage waveform capability of different inverter topologies to suppress the overvoltage. The study was conducted on one of the analyzed filtering approaches as a continuation of the prior work presented in (Ström, 2009).

1.3 Scientific contributions and description of publications

The scientific contributions of this doctoral thesis are:

- Development of a control algorithm of an LC circuit that is implemented to reduce the $\mathrm{d}u/\mathrm{d}t$ of the PWM voltage edges.
- Development of an overvoltage suppression method for a multilevel inverter drive with a long motor cable that operates without any passive filters.
- Analysis of an overvoltage mitigation method for parallel inverters with individual motor cables.
- Development of an overvoltage mitigation method for parallel inverters with output inductors.
- Development of a current balancing control to enable symmetrical loading of the parallel inverters when using active overvoltage mitigation.

A brief description of the publications comprising this doctoral thesis is given below:

Publication I discusses a new $\mathrm{d}u/\mathrm{d}t$ filtering method. The active $\mathrm{d}u/\mathrm{d}t$ topology and the filtering concept are described. The control sequences for the varying output $\mathrm{d}u/\mathrm{d}t$ with the same passive filter element are presented. The dimensioning principle of the filter passive components and the output voltage transition time compared with the cable length are reported. Implementation of the control system is described to produce the additional modulation necessary for the active $\mathrm{d}u/\mathrm{d}t$ filtering on top of the traditional motor control.

Publication II deepens and extends the theory of the active $\mathrm{d}u/\mathrm{d}t$ filtering method. The operation of the filtering approach at different load current amplitudes is discussed. The filtering performance of the method is prone to load current variation, and therefore, an approach to compensate the effects of a varying current is proposed.

Publication III describes the phenomenon of motor terminal oscillating overvoltage for multilevel inverters. A new modeling method for the motor terminal voltage is presented. It uses measurement data extracted from an experimental setup to simulate the motor voltage for

each simulated voltage edge. With this modeling approach, a theory is derived for an ideal motor terminal overvoltage mitigation that does not need any passive filter components. The method uses the accumulation of oscillating motor terminal voltages to minimize the overvoltage, and is referred to as edge modulation.

Publication IV extends the mitigation method presented in Publication **III** to a multilevel modulation presentation. The minimum pulse times requirements of the modulator are given compared with the cable length. The effect of the modulation method on the frequency content of the output voltage is discussed.

Publication V studies an overvoltage suppression method for parallel inverters. The overvoltage suppression method is originally presented in (Miettinen, 2011). The method uses individual motor cables for each inverter and interleaved modulation to produce a voltage superposition at the motor terminals to reduce the peak motor overvoltage. A current balancing method for the inverters is proposed.

Publication VI introduces a method of motor terminal overvoltage reduction for parallel inverters with output inductors. The inductors are dimensioned smaller than in the passive filtering approach. They are used to produce a third voltage potential at the output of the inverter. The neutral voltage potential is used for the accumulation of oscillations caused by the consecutive switching operations of the inverters. The current balancing method introduced in Publication **V** is also applied to this method under study.

1.3.1 Author's contributions

The author has been the primary author in Publications **I**, **V**, and **VI**. The theory and implementation of the method in Publications **I** and **II** were carried out in co-operation with Dr. Juha-Pekka Ström and Juho Tyster, M.Sc. The implementation of the active $\mathrm{d}u/\mathrm{d}t$ control was the main task of the author. The development of the mitigation method, the new method for motor terminal voltage modeling, and Publications **III** and **IV** were made in close cooperation with Dr. Ville Naumanen. The study of the method discussed in Publication **V** was conducted by the author, and the method introduced in Publication **VI** was developed by the author. Dr. Toni Itkonen implemented the crucial parts of the control presented in Publications **V** and **VI**.

The following list includes other publications contributed by the author, but excluded from the thesis. The topics of these publications are in the field of active inverter output filtering.

1. Ström, J.-P., Tyster, J., Korhonen, J., Rauma, K., Sarén, H. & P. Silventoinen (2009), "Active $\mathrm{d}u/\mathrm{d}t$ Filtering for Variable Speed AC Drives," In *Proceedings of the 13th European Conference on Power Electronics and Applications, EPE '09*.

2. Tyster, J., Iskanius, M.; Ström, J.-P., Korhonen, J., Rauma, K., Sarén, H. & P. Silventoinen (2009), "High Switching Speed Three Phase Inverter With Twenty

Nanosecond Minimum Gate Drive Pulse," In *Proceedings of the 13th European Conference on Power Electronics and Applications, EPE '09*.

3. Korhonen, J., Itkonen, T., Ström, J.-P., Tyster, J. & P. Silventoinen (2010), "Active motor terminal overvoltage mitigation method for parallel two-level voltage source inverters," In *Proceedings of the IEEE Energy Conversion Congress and Exposition, ECCE 2010*.

4. Naumanen, V., Korhonen, J., Luukko, J. & Silventoinen, P. (2010), "Multilevel inverter modulation method to reduce common-mode voltage and overvoltage at the motor terminals," In *Proceedings of the 26th IEEE Convention of Electrical and Electronics Engineers in Israel, IEEEI 2010*.

5. Korhonen, J., Laakkonen, T., Itkonen, T., Tyster, J., Ström, J.-P. & Silventoinen, P. (2011), "Motor terminal overvoltage suppression method for parallel inverters," In *Proceedings of the 14th European Conference on Power Electronics and Applications, EPE 2011*.

6. Ström, J.-P., Tyster, J., Korhonen, J., Purhonen, M. & Silventoinen, P. (2011), "Active $\mathrm{d}u/\mathrm{d}t$ filter dimensioning in variable speed AC drives," In *Proceedings of the 14th European Conference on Power Electronics and Applications, EPE 2011*.

7. Tyster, J., Ström, J.-P., Korhonen, J. & Silventoinen, P. (2011), "Efficiency Measurements on active $\mathrm{d}u/\mathrm{d}t$ output filtering," In *Proceedings of the 14th European Conference on Power Electronics and Applications, EPE 2011*.

Chapter 2

Cable-reflection-induced motor terminal overvoltage

As the power switch technology has progressed, the inverter efficiency has improved. Power is consumed during each switching operation transition in proportion to the switched current and voltage. The inverter output voltage is produced by modulating the DC link voltage, and therefore, energy is dissipated during switching operations. Hence, from the perspective of efficiency, it is only beneficial to limit the switch transition times as short as possible. The current switch technology provides low-voltage IGBTs that have transition times in the range from tens to hundreds of nanoseconds (IEC, 2007).

As briefly described in the previous chapter, some adverse effects have arisen with the improvements in the device efficiency. The fast voltage transitions produce high-frequency components, which may generate noise that is conducted or radiated for example to the nearby devices or the supply grid. This noise may cause unwanted behavior and is referred to as electromagnetic interference (EMI) (Skibinski et al., 1999).

The common-mode voltage of an inverter is the average of the output phase voltages. The peak value of the common-mode voltage for a standard two-level VSI is half of the DC link voltage. It must be noted that the two-level inverter may not produce a switch state that will produce zero common-mode voltage. The common-mode voltage can cause bearing currents (Link, 1999) and generate EMI (Skibinski et al., 1999).

The fast switching operations of the inverter and the impedance mismatches along the connections from the inverter to the motor can cause a motor terminal overvoltage (Persson, 1992). In an industrial environment, the inverter and the motor can be from tens to hundreds meters apart. Even longer distances can be found for example in mine installations (Rodriguez et al., 2006). In this chapter, the phenomenon causing the overvoltage, the negative effects of the transient, and the present means of limiting the overvoltage are discussed.

2.1 Transient motor terminal overvoltage

The motor terminal overvoltage caused by a combination of impedance mismatches, long motor cables, and inverter switching transients can be explained by the transmission line theory (Heaviside, 1893, 1899). The application-specific presentation of the motor terminal overvoltage with a PWM switching inverter with IGBTs was originally presented in (Persson, 1992).

In the following, the cable reflection phenomenon is described assuming that the voltage fed by the inverter into the cable is a step function. As the inverter phase switches polarity, a voltage edge is introduced to the motor cable. The voltage edge travels at a speed that depends on the insulation material of the cable. Often, the velocity is approximated to be half the speed of light, which applies for example to a typical polyvinyl chloride (PVC) insulated three-phase motor cable. The velocity may vary between 0.32c and 0.7c with different insulation materials (Kerkman et al., 1997).

The voltage edge first interacts with the motor after a propagation delay

$$t_\mathrm{d} = \frac{l_\mathrm{c}}{v}. \tag{2.1}$$

The transient impedance of the motor Z_m differs from the cable impedance Z_c, and thus, a reflection takes place at the terminals. The peak terminal voltage may rise to

$$\hat{u}_\mathrm{motor} = u_\mathrm{pulse}(1+\Gamma_\mathrm{M}) = u_\mathrm{pulse}\left(1+\frac{Z_\mathrm{m}-Z_\mathrm{c}}{Z_\mathrm{m}+Z_\mathrm{c}}\right), \tag{2.2}$$

where u_pulse is the amplitude of the incident voltage. The motor impedance is dependent on the frequency, and the impedance differs by decades from the output frequency to the transient voltage frequency range (Mirafzal et al., 2007). The impedance of a motor has also been reported to decrease with the motor power. This applies also to the transient impedance, and therefore, the reflection coefficient may vary between $\Gamma_\mathrm{M} = 0.6 - 0.95$ (Saunders et al., 1996).

The reflected voltage travels back to the inverter. The inverter impedance for the reflecting voltage edge depends on the inverter switching commands. The impedance seen at the inverter terminals may be a combination of free-wheeling diodes, conducting switches, and the DC link capacitor (Kosonen, 2008). Regardless of the switching states, the impedance is considerably lower than that of the motor cable, and therefore, the reflection coefficient at the inverter has most commonly been assigned to be $\Gamma_\mathrm{S} \approx -1$ (Persson, 1992).

The voltage travels between the inverter and the motor, and it is always reflected at the terminals, where it changes its polarity and amplitude. The oscillation frequency is defined by the cable length and signal propagation speed

$$f_\mathrm{osc} = \frac{1}{4t_\mathrm{d}} = \frac{v}{4l_\mathrm{c}}. \tag{2.3}$$

The oscillation attenuates over several cycles. Every time the voltage reflects at the motor, the returning pulse has a smaller amplitude, since $\Gamma_M < 1$. The cable also contributes to the attenuation. Skin and proximity distort the traveling voltage edge, since they function as frequency-dependent resistances along the cable (Skibinski et al., 1997). The voltage waveform distortion caused by transmission lines has been known since the time of the telegraph (Nyquist, 1928). The transmission medium can distort a traveling wave that contains many frequency components. The medium may cause phase distortion and attenuation as a function of frequency.

2.1.1 Effect of voltage transition rate on the overvoltage

Instead of being a step function, the inverter output voltage transition has a finite $\mathrm{d}u/\mathrm{d}t$. As the impedance mismatch points and the reflection coefficients remain the same at the cable ends, the overvoltage depends on the relation between the transition time t_t of the voltage and the propagation delay. If the transition time of the voltage is shorter than two times the propagation delay, the peak motor overvoltage is equivalent to the value given by (2.2). The point when the transition time equals $2t_d$ is called the critical cable length (Kerkman et al., 1997). For example, if $v = 0.5$c and the transition time is 100 ns, the critical cable length is 7.5 m.

When the cable is shorter than the critical length, the reflecting voltage front has traveled to the motor and back to the inverter before the voltage at the output of the inverter has changed to u_{pulse}. The reflected voltage changes polarity, which decreases the peak motor overvoltage. The first local minimum in the overvoltage is found when the transition time of the voltage is $4t_d$ (Persson, 1992). It is emphasized that this applies only to symmetric ramp-shaped voltage transition waveforms. The voltage waveform during the transition affects the overvoltage reduction, and it should be taken into account in some filtering approaches.

2.1.2 Overvoltages above $2u_{DC}$

In the literature, several cases have been reported where the overvoltage at the motor terminals exceeds the value of $2u_{DC}$. These cases are caused by the accumulation of oscillating overvoltages from consecutive switching operations or by additional discontinuities in the transmission line.

Two-level inverters

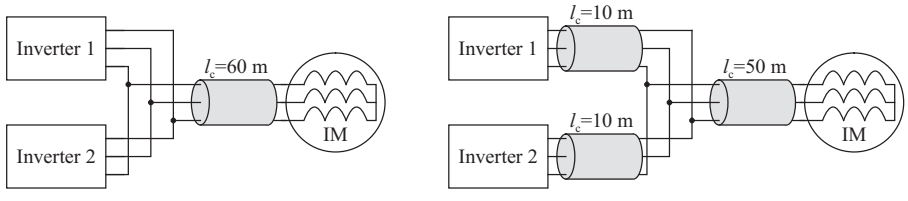
The previously described overvoltage phenomenon was associated with the case of a single inverter switching operation. An overvoltage may exceed the value given in (2.2) if two or more voltage oscillations accumulate at the motor terminals (Kerkman et al., 1997; Skibinski et al., 1997). For this to happen, the second switching operation must take place before the

oscillation caused by the previous voltage edge has decayed. The motor terminal overvoltage that has a peak value above $2u_{DC}$ may be a result of two consecutive switching operations of a single phase or, as the motor terminal voltage is usually measured line-to-line, the consecutive switching operations may be from different phases. The double pulsing from single-phase switching operations occurs for short pulses, which are produced at very low and high modulation indices. The most drastic case for two switching operations takes place if two phases change polarity simultaneously. This produces a peak line-to-line voltage of $2u_{DC}(1+\Gamma_M)$.

The case that was described last is unacceptable for any PWM driving an electric motor. It can be avoided by restricting the modulator to switch two phases within a certain time period. This approach can be used to reduce the accumulation of voltages from two phases, if the time period is set to the approximated decay time of the oscillation. For the single-phase accumulation, the prevention may be carried out by setting the minimum pulse requirement according to the decay time. If these periods are determined too long, this will degrade the controllability. This problem also becomes more serious if the switching frequency of the PWM is increased, because the restricted period between the switching operations will become proportionally longer compared with the PWM switching period.

Parallel two-level inverters

When parallel inverters are feeding a single load, different cable configurations may be used. The traditional two-inverter parallel topology with a single motor cable is shown in Figure 2.1a. However, a configuration may consist of individual motor cables leading from each inverter to a certain distance, for example 10 meters, after which the cables are connected to a common motor cable. Such a wye-connected cable configuration is illustrated in Figure 2.1b. The additional cable setup may be used to replace output inductors to prevent short circuits and to reduce circulating currents.



(a) Two inverters, single 60 m cable

(b) Two inverters, wye-connected cables, 10 m and 50 m

Figure 2.1. Two possible parallel inverter cable configurations.

Table 2.1. Lumped motor cable parameters for a one-meter section (Moreira et al., 2002).

R_s [mΩ]	L_s [μH]	R_{p1} [MΩ]	R_{p2} [kΩ]	C_{p1} [pF]	C_{p2} [pF]
1.5	0.24	173	13.9	137.1	22.5

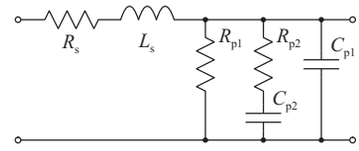
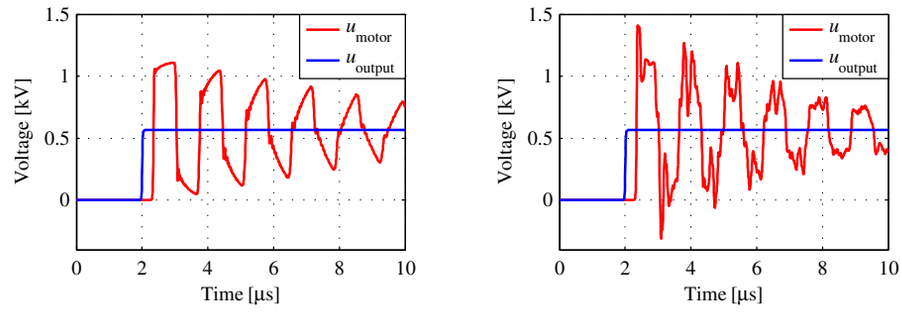


Figure 2.2. Single section of a lumped single-phase cable model (Moreira et al., 2002).

First, the reference of two inverters feeding a motor through a single 60 m cable was simulated. The motor cable was simulated in one-meter sections, and a lumped cable model section is shown in Figure 2.2. The lumped cable model is a widely studied and applied method to simulate motor cables (Moreira et al., 2002; Wang et al., 2010; Akagi and Matsumura, 2011). However, higher precision can be achieved by using simulation tools that are based on the Maxwell equations. The modeling of the motor cable was out of the



(a) Two inverters, single cable, 60 m, $\hat{u}_{motor} = 1110\,V = 1.97\,u_{DC}$

(b) Two inverters, wye-connected cables, 10 m and 50 m, $\hat{u}_{motor} = 1409\,V = 2.49\,u_{DC}$

Figure 2.3. Simulated motor terminal and inverter output voltages. A single cable is used for (a), and 10 m cables leading to a 50 m common motor cable in (b).

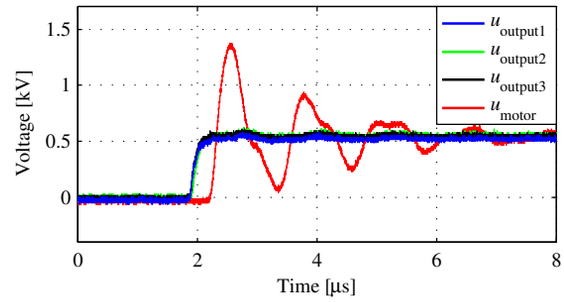


Figure 2.4. Measured inverter output and motor terminal voltages. Three parallel inverters with individual 20 m cables leading to a 20 m common cable. The motor peak voltage is $\hat{u}_{motor} = 1375\,V = 2.39\,u_{DC}$ (Korhonen et al., 2011).

scope of the thesis, and a lumped section model was found adequate for simulations. The cable parameters are given in Table 2.1 (Moreira et al., 2002), and the load parameters are $L_{\text{load}} = 625\,\text{mH}$ and $R_{\text{load}} = 231\,\text{m}\Omega$. The simulations were performed by MATLAB® SIMULINK™. An overvoltage according to (2.2) is depicted in Figure 2.3a, with a peak motor voltage of $\hat{u}_{\text{motor}} = 1110\,\text{V} = 1.97\,u_{\text{DC}}$. Thus, the cable reflection phenomenon is the same as with a single inverter, with the exception that the source impedance is that of the parallel connection.

The simulation results for the configuration where two parallel inverters with 10 m cables lead to a 50 m motor cable are illustrated in Figure 2.3b. The individual cable sections may have a different impedance than the common cable, but the same lumped cable model was used for the simulations. As the voltage edges are fed simultaneously from the inverters, they will first interact in the point of common connection. This produces a voltage surge above the DC link voltage to be transmitted to the motor cable. The resulting motor peak voltage is $\hat{u}_{\text{motor}} = 1409\,\text{V} = 2.49\,u_{\text{DC}}$.

Motor terminal overvoltages above $2u_{\text{DC}}$ have also been measured with three parallel inverters. There was a 20 m cable from each inverter leading to a 20 m common cable. The load was a 22 kW induction motor and the DC link voltage was 575 V. The peak motor terminal voltage was found to be $\hat{u}_{\text{motor}} = 1375\,\text{V} = 2.39\,u_{\text{DC}}$. This measurement was originally presented in (Korhonen et al., 2011).

Multilevel inverters

Resonating overvoltages have also been reported in multilevel inverter applications (Endrejat and Pillay, 2009). Here the overvoltage does not reach even two times the nominal voltage value, but compared with the output voltage of a single H-bridge, the amplitude of the oscillation is approximately 4.8 times as high. The resonance is a result of placing an output reactor further than the critical cable length away from the inverter and the accumulation of overvoltages caused by an inverter switching frequency that interacts with the cable resonance frequency.

2.1.3 Effects of motor terminal overvoltage

It has been widely reported that the longevity of the motor insulation is compromised because of repetitive transient overvoltages with high voltage transition rates (Persson, 1992; Bonnett, 1996; Melfi et al., 1998; Bidan et al., 2001; Moreira et al., 2005; Melfi, 2006; Cavallini et al., 2010). The overvoltage occurs at the motor terminals multiple times within the switching period of the inverter, as each voltage transition results in an oscillating overvoltage waveform. The first edge has the highest $\mathrm{d}u/\mathrm{d}t$ and amplitude, as the reflecting surge is attenuated by the cable losses.

The overvoltage at the motor terminals may lead to a phase-to-phase or phase-to-ground in-

sulation failure. If the transient overvoltage exceeds the insulation partial discharge inception voltage level, the voltage stress over a certain point in the insulation will become too high and an electrical spark will occur. For instance in random-wound motors, small air gaps may be present in the insulation. These air gaps are susceptible to partial discharges. However, some motor insulation types are expected to face partial discharges, and the insulation is designed to withstand them without a premature failure (Stranges et al., 2007).

The high $\mathrm{d}u/\mathrm{d}t$ produces an uneven distribution of voltage across the stator windings. At transition times below 50 ns, the voltage over the first turns of the winding can be, depending on the source, from 45 % (IEC, 2007) to 90 % (Cavallini et al., 2010) of the voltage fed to the motor. The uneven voltage distribution produces a high voltage stress between the winding turns, especially in random-wound motors. The voltage stress may arise above the interturn insulation level, leading to partial discharges, and eventually, to an insulation failure. As the transition time increases, the stress over the first turns is reduced and the voltage is more evenly distributed over the windings.

Industrial standards have been assigned to the voltage level that a motor insulation should withstand. The peak voltage level is a function of transition time. For instance, according to (IEC, 2007), a 690 V motor should withstand a 1.6 kV peak line-to-line voltage for a rise time t_r of 10 ns, 1.9 kV for $t_\mathrm{r} = 100$ ns, and 2.15 kV for $t_\mathrm{r} > 500$ ns. The voltage rise time is defined as the period when the voltage rises from 10 % to 90 % of the transient voltage peak value (IEC, 2007). A standard DC link voltage of a 690 V drive is approximately 976 V. Hence, if the motor terminal overvoltage is not above $2u_\mathrm{DC}$, the overvoltage may be at a dangerous level if the rise time is below 100 ns.

The motor insulation can also fail because of 'the antiresonance phenomenon' (Mirafzal et al., 2009). The motor impedance changes as a function of frequency, and at higher frequencies the impedance starts to drop. In the megahertz range the motor impedance is very low, and if this frequency is excited by the motor cable resonance, an internal series resonance may occur. The resonance amplifies the voltage, and it may lead to a turn-to-turn insulation failure. This failure mechanism cannot be observed externally from a motor, as the resonances occur between the stator winding turns.

As the common-mode voltage is the average of the phase voltages, the overvoltages at the motor terminals contribute to the common-mode voltage. The oscillating overvoltage increases the common mode voltage peak value and its $\mathrm{d}u/\mathrm{d}t$.

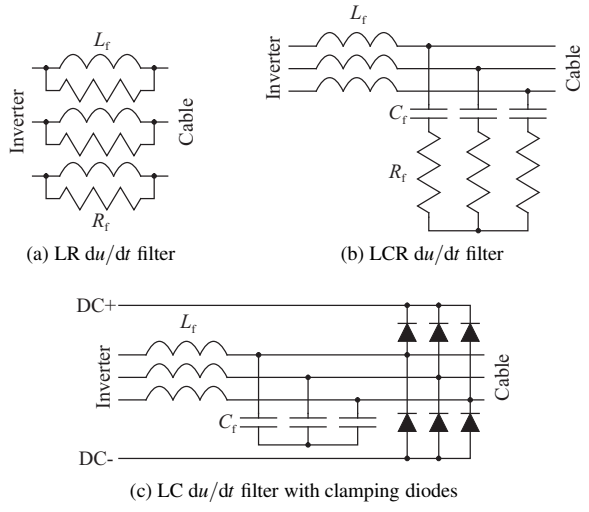
2.2 Passive filtering

The motor terminal overvoltage has traditionally been limited by passive filtering. The filtering methods reported in the literature are a $\mathrm{d}u/\mathrm{d}t$ filter, a sinusoidal filter, and a cable termination circuit (Skibinski, 1996; Finlayson, 1998; Steinke, 1999; Habetler et al., 2002; Moreira et al., 2002, 2005; Akagi and Matsumura, 2011).

The $\mathrm{d}u/\mathrm{d}t$ filter is placed at the output of the inverter, and it reduces the output voltage transition rate. For the filtering to be sufficient, the ratio of the transition time and the propagation delay must be above two, which is the limit for the critical cable length. If the output voltage is considered to be a ramp waveform, the ideal overvoltage suppression will take place when the ratio is $t_\mathrm{t}/t_\mathrm{d} = 4$ (Persson, 1992). However, this will apply only if the source reflection coefficient is -1. Some filter topologies aim to match the source impedance to the cable impedance, and the sufficient rise time has to be defined independently according to the filter topology.

The simplest solution is to place a line reactor at the output of the inverter (Finlayson, 1998). To reach a minimum overvoltage for each inductance value, a resistor matching the cable impedance can be connected in parallel with the inductor (Akagi and Matsumura, 2011). Such a filter topology is illustrated in Figure 2.5a.

A second-order LC filter is a common basis for $\mathrm{d}u/\mathrm{d}t$ filtering. If a steep voltage edge is fed to an LC circuit, the output voltage will start to oscillate at a frequency of $1/(2\pi\sqrt{L_\mathrm{f}C_\mathrm{f}})$ with a peak amplitude of $2u_\mathrm{DC}$. The LCR filter, shown in Figure 2.5b, has a resistor connected in series with the capacitor to damp the overshoot of the LC circuit. The overshoot cannot be entirely mitigated, even when the LCR circuit itself is critically damped (von Jouanne and Enjeti, 1997). Another way to limit the LC circuit overshoot is to add clamping diodes to the circuit (Habetler et al., 2002). This configuration is shown in Figure 2.5c. Here, the rise time of the filter output voltage is $t_\mathrm{t} = \frac{\pi}{2}\sqrt{L_\mathrm{f}C_\mathrm{f}}$, if the circuit is loss-free.



(a) LR $\mathrm{d}u/\mathrm{d}t$ filter

(b) LCR $\mathrm{d}u/\mathrm{d}t$ filter

(c) LC $\mathrm{d}u/\mathrm{d}t$ filter with clamping diodes

Figure 2.5. Filtering topologies for reduction of the voltage transition rate.

A common-mode reduction path can be added to the LCR $\mathrm{d}u/\mathrm{d}t$ filter. The path is placed from the filter capacitor wye connection back to either one of the inverter DC rails or to the neutral point at the DC link, if it is available and accessible (Rendusara and Enjeti, 1997). For

the topology shown in Figure 2.5c, the common-mode reduction path is inherent. An output inductor design that has an integrated differential-mode and common-mode inductance for a LR filter is presented in (Tallam et al., 2011).

The sinusoidal filtering method aims to produce a near sinusoidal filter output voltage waveform (Steinke, 1999; Rodriguez et al., 2006). An LC filter shown in Figure 2.6 is a common topology for a sinusoidal filter. The LC circuit resonance must be set between the switching frequency of the inverter and the fundamental frequency. The more sinusoidal voltage waveform reduces the common-mode voltage fed to the motor. An alternative diode clamp is accompanied by a sinusoidal filter with a resonance frequency below the switching frequency (Hanigovszki et al., 2004).

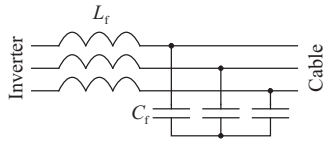
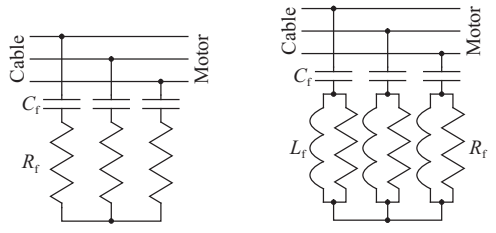


Figure 2.6. Sinusoidal filter topology.

A straightforward method to eliminate the motor terminal overvoltage is to use an impedance matching circuit at the motor terminals (Skibinski, 1996; von Jouanne et al., 1996). The terminator may be an RC or LCR circuit, which are shown in Figure 2.7. The impedance of the parallel connection of the termination circuit and the motor impedance match that of the cable. As previously mentioned, the motor transient impedance is significantly higher than the cable impedance, which allows the motor impedance to be neglected in the circuit design. The terminator does not limit the $\mathrm{d}u/\mathrm{d}t$, but a correctly dimensioned terminator eliminates the overvoltage. The $\mathrm{d}u/\mathrm{d}t$ may be reduced with a more complex terminator, but a drawback of the topology is an oscillating motor terminal voltage (Yuen and Chung, 2010).



(a) RC termination circuit (b) RLC termination circuit

Figure 2.7. Cable termination topologies.

A diode clamp can be used in the termination circuit, and the energy can be fed back to the DC link instead of being dissipated in the RC circuit. The clamping diode bridge can be placed either at the motor terminals (Chen and Xu, 1998), or next to the inverter (Shimizu et al., 2012). As the diode bridge is at the motor terminals, the auxiliary cable has two leads. The diode bridge and the auxiliary cable may become a path for the reactive power fed back from the motor, and thus, they have to be dimensioned to be able to carry reactive power back to the DC link. When the diode bridge is placed at the inverter, an auxiliary three-phase cable

is connected in parallel with the actual motor cable at the motor terminals. The impedances of the actual and auxiliary cables should be the same. The parallel connection of the cables produces a voltage division at the motor terminals for the propagating voltage edge. The reflection coefficient that the edge sees is

$$\Gamma_{\mathrm{M}} = \frac{\frac{Z_{\mathrm{m}} Z_{\mathrm{c}}}{Z_{\mathrm{m}}+Z_{\mathrm{c}}} - Z_{\mathrm{c}}}{\frac{Z_{\mathrm{m}} Z_{\mathrm{c}}}{Z_{\mathrm{m}}+Z_{\mathrm{c}}} + Z_{\mathrm{c}}}, \tag{2.4}$$

where the impedance of the cables is Z_{c} and the motor impedance is Z_{m} (Shimizu et al., 2012). Since the motor impedance is significantly larger than the cable impedance, the edge is transmitted to the auxiliary cable and travels back to the DC link. The reflection coefficient of the DC link is estimated to be $\Gamma_{\mathrm{S}} \approx -1$. The voltage edge travels between the inverter and the motor, reflecting at the terminals. The reflections from the parallel cables accumulate so that the overvoltage is reduced. The methods would cancel out the overvoltage in the case of ideal transmission lines, but for actual motor cables, a residual overvoltage remains (Shimizu et al., 2012).

2.3 Active filtering

In the field of power electronics, the term active filtering is most commonly associated with power conditioning when nonlinear loads are connected to the grid (Akagi, 1996). Over the years, several active filtering approaches have been adopted also on the load inverter side. For example, some of these methods have concentrated on common-mode reduction (Di Piazza et al., 2009). In addition, active variation of the gate resistor has been used to restrict di/dt and du/dt of the inverter switches and to reduce the conducted EMI (Idir et al., 2006; Kagerbauer and Jahns, 2007).

Active filtering methods have been presented to limit the motor terminal overvoltage. The filtering is for a two-level inverter, and the inverter uses additional switching operations for each PWM voltage edge (Deisenroth and Trabert, 1993). It is suggested in the paper that the motor terminal overvoltage can be filtered by charging the motor cable by timing a short voltage pulse, which depends on the cable parameters. The overvoltage cannot be filtered this way, because the first voltage edge still results in an overvoltage. The paper also proposes adding an output inductor and using a charge pulse at PWM pulse edges to limit the overvoltage.

The inverter output voltage transition rate can also be reduced by modifying the inverter to a resonant or quasi-resonant topology (Kedarisetti and Mutschler, 2012). This requires additional passive components, power switches, and diodes added to the traditional two-level VSI topology.

Active filtering has also been carried out with a three-level inverter by actively damping the oscillating overvoltage (Lee and Nam, 2002). The damping is achieved by timing two consecutive switching operations so that the oscillations are in an opposite phase. This results

in an inverter output voltage that resembles that of a typical two-level inverter. A similar approach has been studied in Publications **III** and **IV**, and the method will be discussed in Section 3.2.

An overvoltage suppression method for parallel inverters has been presented in (Miettinen, 2011). The method is based on individual motor cables from each inverter leading to the motor terminal. The parallel inverters are not switched simultaneously, but the switching operations are interleaved according to the propagation delay of the cable. Now, the transient voltage reflects at the motor terminals according to the impedance of the parallel cables, and the overvoltage can be reduced. This method is under further study in Section 3.3.1.

Chapter 3

Active inverter output filtering methods

In this chapter, the focus is on the studied active inverter output filtering approaches to limit the motor terminal overvoltage. The methods aim to reduce the passive component dimensions of the output filter, or even make it obsolete by means of additional inverter modulation. The methods are topology specific, and they each use the inherent characteristics of the topology to reduce the overvoltage.

3.1 Active du/dt filtering for a two-level voltage source inverter

This section is an introduction to Publications **I** and **II**. The active du/dt filtering concept uses additional modulation at the PWM voltage transitions, which allows the output voltage of a passive filter element to be controlled individually. The filter is a second-order LC filter. The aim of the active du/dt is to increase the voltage transition times in order to reduce the motor terminal overvoltage.

3.1.1 Active du/dt filtering principle

When a voltage edge with an amplitude of u_{pulse} is introduced to an undamped LC circuit, the output of the circuit starts to oscillate at a frequency of $f = \frac{1}{2\pi\sqrt{L_{\text{f}}C_{\text{f}}}}$ and an amplitude of $2u_{\text{pulse}}$. An overvoltage of this magnitude is not acceptable, and an approach to eliminate the overshoot is taken by means of an additional inverter control.

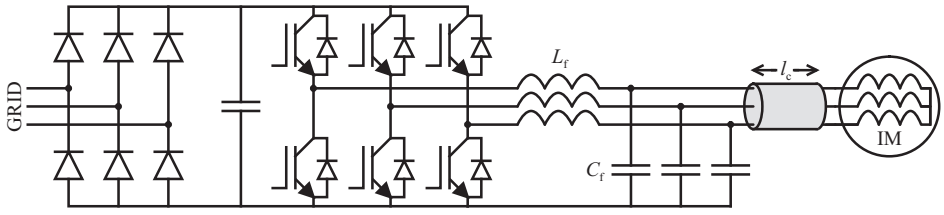


Figure 3.1. Two-level inverter with an LC output filter.

The LC filter may be constructed in several ways. The simplest topology is shown in Figure 3.1. The feedback from the capacitor wye connection to the DC link negative bus is optional, since it is a path for the common-mode voltage, and it does not affect the control of the LC circuit. The feedback may also be placed at the positive bus of the DC link. The filter capacitors may also be distributed and connected to both of the DC buses. If the DC link has an even number of capacitors, the feedback from the capacitor wye connection may also be placed in the midpoint of the capacitor bank, if such a path is available.

The control principle of the active $\mathrm{d}u/\mathrm{d}t$ method is to modulate the filter input voltage so that the output voltage will change polarity. The voltage transition time at the filter output is the same as the period when the additional modulation is performed. From the standpoint of the inverter control, the interval is referred to as a charge period. In theory, the modulation may be carried out with several voltage pulses, which may be of different pulse widths. This will allow the time variation of the voltage transition with a single passive element. However, the study is restricted to a single-pulse filter control.

As presented in (Ström et al., 2009), the capacitor charge modulation sequence of a single-pulse filter has a duration defined by the LC circuit

$$t_{\mathrm{cp}} = \frac{2\pi}{3}\sqrt{L_{\mathrm{f}}C_{\mathrm{f}}}. \tag{3.1}$$

The time required to produce an average voltage of $u_{\mathrm{DC}}/2$ during the modulation sequence is equivalent to a 50 % duty cycle. The switching times of the modulation sequence are then $0 \rightarrow \frac{t_{\mathrm{cp}}}{2} \rightarrow t_{\mathrm{cp}}$. With this sequence, the filter output voltage is half of the DC link voltage at $t = \frac{t_{\mathrm{cp}}}{2} = t_{\mathrm{cp}/2}$. The charging sequence is depicted in Figure 3.2. The $\mathrm{d}u/\mathrm{d}t$ of the filter output is highest in the middle of the charge period

$$\frac{\mathrm{d}u}{\mathrm{d}t}(t = t_{\mathrm{cp}/2}) = \frac{u_{\mathrm{DC}}}{\sqrt{L_{\mathrm{f}}C_{\mathrm{f}}}}\sin\frac{\pi}{3}. \tag{3.2}$$

The capacitor current also reaches its peak value at $t = \frac{t_{\mathrm{cp}}}{2}$

$$i_{\mathrm{cap}}(t = t_{\mathrm{cp}/2}) = \frac{u_{\mathrm{DC}}}{\sqrt{\frac{L_{\mathrm{f}}}{C_{\mathrm{f}}}}}\sin\frac{\pi}{3}. \tag{3.3}$$

The capacitor current returns to zero at the end of t_{cp}. This study assumes that the load current does not change during the charging period. Equations (3.1) – (3.3) apply when there are no discontinuities in the charge current waveform during t_{cp}.

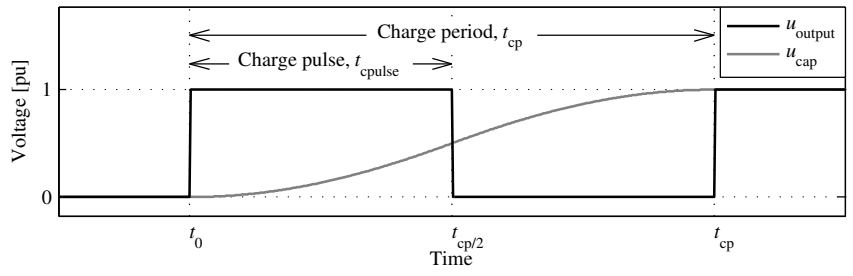


Figure 3.2. Active du/dt modulation sequence for a rising voltage edge.

An example of a PWM period with the active du/dt method is illustrated in Figure 3.3. The component value setting process of the passive filter is carried out with a target transition time of 4 µs and $L_f = 10\,\mu H$. The capacitor value is calculated to be $C_f = 364.8\,nF$. A dead time of 1 µs is used for the simulation. The charging pulse duration is 2 µs and the charge period is 4 µs. The capacitor peak current is $\hat{i}_{cap} = 93.5\,A$ and the highest du/dt is 256.2 V/µs. The original PWM pulse duration is $t = 6 - 20\,\mu s$.

3.1.2 Current correction during voltage transition

The effect of the phase-leg current variation on the filter charging is not presented in Figure 3.3. The inverter phase-leg current is the sum of the capacitor current and the load current. To put it simply, the operation principle of a two-level VSI leg is that the upper switch controls the output voltage for the positive load current (towards the load) and the lower switch for the negative load current (from the load to the inverter). If the inverter current changes polarity during the charge period, the inverter current may not be restored back to the original amplitude with the control presented in Figure 3.3. Therefore, a new pulse is introduced to the modulation sequence when the current changes polarity during t_{cp}. This pulse will take place after t_{cpulse}, and it is referred to as a current correction pulse $t_{icpulse}$.

For an ideal inverter, which would not need a dead time between the switching operations of the same inverter leg, the current correction pulse would take place right after t_{cpulse}. The duration of the current correction pulse would take the rest of the charging period. This control would maintain the inverter output and filter output voltage waveforms shown in Figure 3.3. The current correction pulse is not necessary if the inverter current does not change polarity during t_{cp}. This applies to a rising voltage edge when the load current is positive, and to a falling voltage edge when the load current is negative.

When the load current reaches an amplitude that is higher than the peak value calculated from (3.3), it is no longer possible for the inverter current to change polarity during t_{cp}. This is why the switching commands must be reassigned from the basic control shown in Figure 3.3. Let us consider a case of a rising voltage edge with a negative load current, which is higher than the value obtained from (3.3). When the lower switch is set to a nonconductive state,

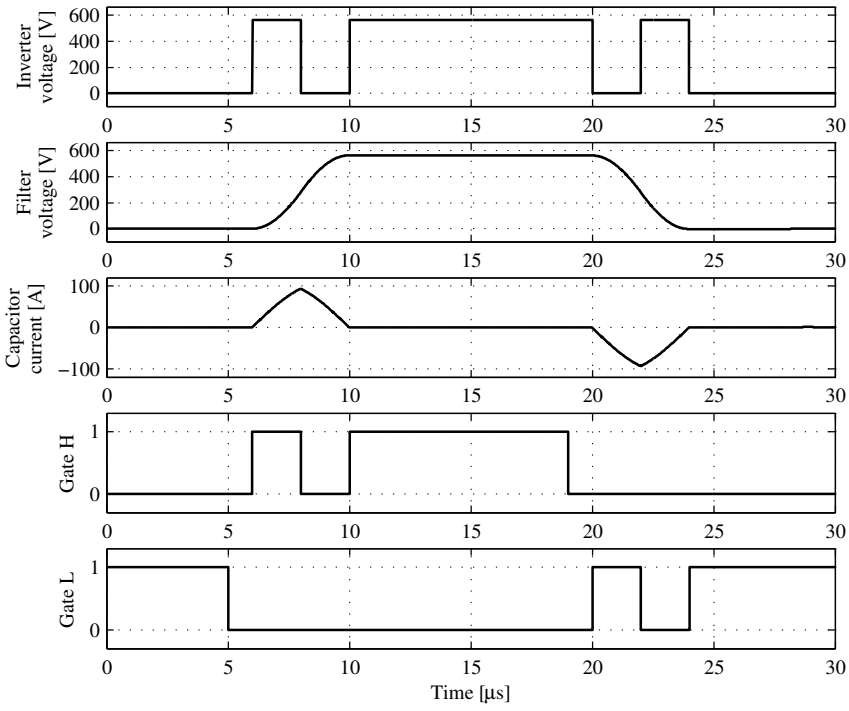


Figure 3.3. Active $\mathrm{d}u/\mathrm{d}t$ simulation with $t_\mathrm{t} = 4\,\mu\mathrm{s}$, $L_\mathrm{f} = 10\,\mu\mathrm{H}$, and $C_\mathrm{f} = 364.8\,\mathrm{nF}$.

the output voltage of the inverter rises to u_DC. As the current is negative, the current flows through the freewheeling diode parallel to the higher switch. Turning the higher switch to a conductive state does not change the voltage waveform. To draw the inverter current back to the initial amplitude, only the current correction pulse is needed.

Introducing a dead time to the control has an effect on the charging of the filter capacitor when the inverter current changes polarity during the charge period. The objective of the modulation sequence is to produce an inverter output voltage waveform illustrated in Figure 3.2. During a dead time, the output voltage depends on the direction of the current. The switching times must be adjusted so that the output voltage of the filter does not resonate, and the inverter current must equal to the load current. Again, the assumption is made that the load current does not change during the charge period. The dead time will not affect the control if the direction of the current does not change during t_cp.

The effect of dead time on the modulation pattern is shown in Figures 3.4 – 3.5. The filter parameters are the previously calculated $L_\mathrm{f} = 10\,\mu\mathrm{H}$ and $C_\mathrm{f} = 364.8\,\mathrm{nF}$ for $t_\mathrm{cp} = 4\,\mu\mathrm{s}$. The dead time used in the simulations is $1\,\mu\mathrm{s}$ and $u_\mathrm{DC} = 565\,\mathrm{V}$.

The initial load current in Figure 3.4 is $-30\,\mathrm{A}$, and the sequence and pulse durations are

presented in Table 3.1. In Figure 3.4a, the switching times are set so that they produce a 2 µs pulse length. However, the current is clamped to zero during the dead time, and the voltage drops to the voltage of the capacitor. Therefore, the voltage will be below u_{DC} at the end of the sequence, and this will cause a residual oscillation to the filter output voltage. In Figure 3.4b, the sequence has an extended charge pulse, which charges the capacitor to u_{DC}. The current will not be correct at the end of the sequence if the current correction pulse duration is maintained at $t_{\mathrm{icpulse}} = 1\,\mu\mathrm{s}$. Figure 3.4c presents a successful modulation sequence. It is emphasized that the charge pulse duration is longer than the time when the filter output voltage is $u_{\mathrm{DC}}/2$, and thus, t_{cp} is longer than calculated with (3.1).

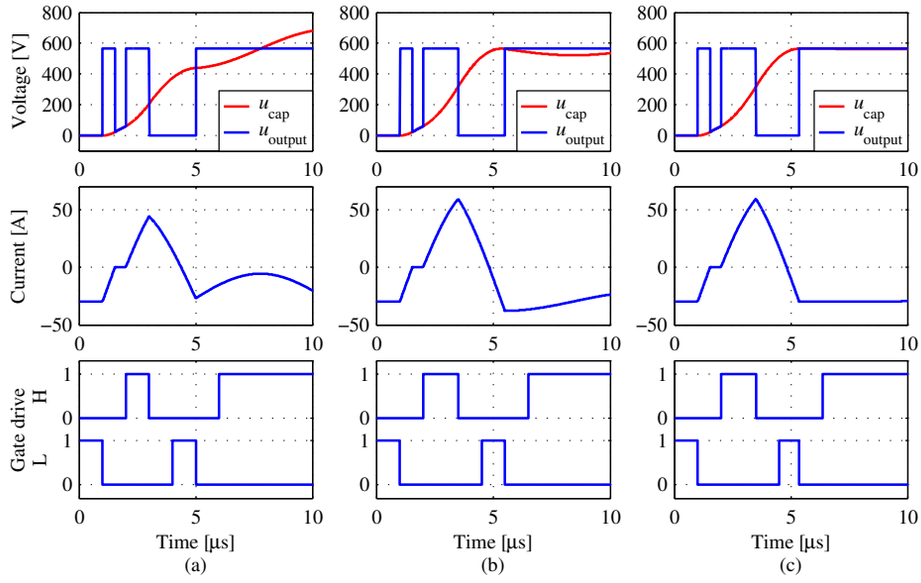


Figure 3.4. Active du/dt simulation with an initial load current of $-30\,\mathrm{A}$ and $L_{\mathrm{f}} = 10\,\mu\mathrm{H}$ and $C_{\mathrm{f}} = 364.8\,\mathrm{nF}$.

Table 3.1. Pulse sequences of Figure 3.4.

	t_{cp} [µs]	t_{cpulse} [µs]	t_{icpulse} [µs]
(a)	4	1	1
(b)	4.5	1.5	1
(c)	4.36	1.5	0.86

The initial load current for Figure 3.4 is changed to $-70\,\mathrm{A}$, which is close to the peak amplitude of the capacitor charge current $\hat{i}_{\mathrm{cap}} = 93.5\,\mathrm{A}$. The sequence and pulse durations used in the simulations are presented in Table 3.2. Figure 3.5a illustrates the behavior of the filter voltage and current if the modulation sequence is the same as in the case where the initial current amplitude is higher than $\hat{i}_{\mathrm{cap}}$. It can be seen that the current is clamped at zero amperes,

which results in an insufficient voltage fed to the capacitor. In Figure 3.5b, a sequence with a short t_{cpulse} is depicted. Usually, IGBTs are assigned minimum pulse lengths, and if t_{cpulse} is shorter than the minimum pulse, an alternative sequence should be sought. The proposed modulation sequence for the simulated variables is shown in Figure 3.5c. Only the current correction pulse was used, and the sequence was 0.24 µs = 6 % longer than the intended t_{cp}.

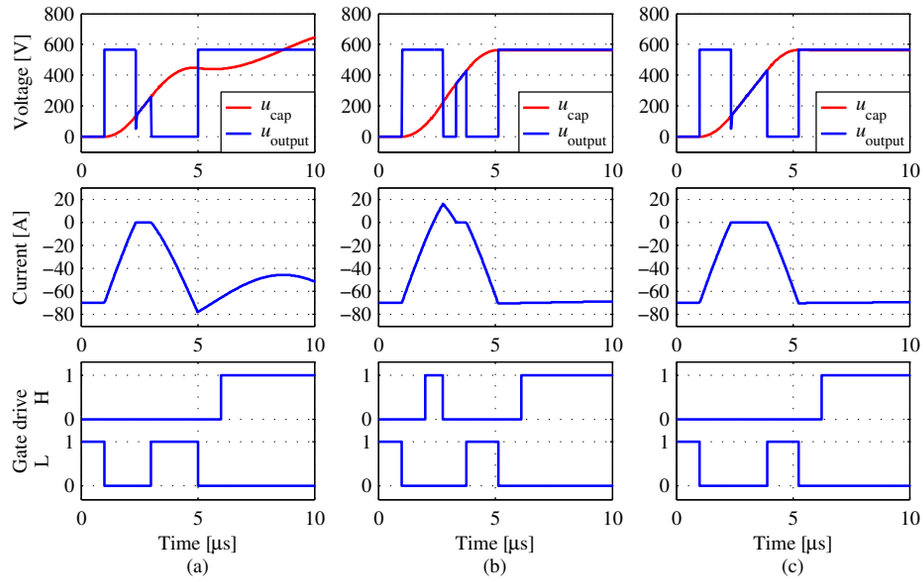


Figure 3.5. Active $\mathrm{d}u/\mathrm{d}t$ simulation with an initial load current of -70 A and $L_{\mathrm{f}} = 10\,\mu\mathrm{H}$ and $C_{\mathrm{f}} = 364.8$ nF.

Table 3.2. Pulse sequences of Figure 3.5.

	t_{cp} [µs]	t_{cpulse} [µs]	t_{icpulse} [µs]
(a)	4	0	2
(b)	4.12	0.76	1.36
(c)	4.24	0	1.35

3.1.3 Discussion

The dimensioning procedure of the active $\mathrm{d}u/\mathrm{d}t$ first takes into account the necessary transition time and the peak $\mathrm{d}u/\mathrm{d}t$ to reduce the motor overvoltage to an acceptable level. A 'minimum' t_{cp} may be restricted by the inverter switching characteristics, for example minimum pulse and dead time requirements. When t_{cp} is chosen, the next limiting factor is the peak capacitor current allowed by the inverter. This determines the ratio between L_{f} and C_{f}.

The inductor losses and possible saturation must be taken into account in the filter design, but these topics are out of the scope of this thesis. The increased switching operations produced by the method must be compensated in the inverter cooling capability.

Several aspects of the control of the inverter must be kept in mind when implementing the active $\mathrm{d}u/\mathrm{d}t$. The active $\mathrm{d}u/\mathrm{d}t$ modulation sequence is triggered by the PWM pulse edges. The PWM functions independently and the switching operations assigned by the motor modulator are the trigger signals for the active $\mathrm{d}u/\mathrm{d}t$ sequences. The PWM includes the motor control and all of its features, such as dead time compensation. The active $\mathrm{d}u/\mathrm{d}t$ modulator generates the charging sequence, including the dead times. The active $\mathrm{d}u/\mathrm{d}t$ modulation sequence must be set according to the load current. When a digital PWM is used, the switching times can be easily acquired at the beginning of the switching period. This data can be used to time the current measurements, if the current measurement is not placed after the filter. The IGBT turn-on and turn-off delays usually differ from each other, and they must be compensated for the inverter to produce the correct voltage waveform. If the rise and fall times of the PWM pulse are different because of the effect of dead time on t_{cp}, this may produce a small error in the volt-seconds fed to the motor. One of the key changes to the modulation is the minimum pulse length for the PWM, which is initially the IGBT minimum pulse, for example 1 µs. The minimum pulse must be increased for the PWM by a charge period, in order for the voltage transition to finish undisrupted, and after the IGBT minimum pulse to take place.

The modulation sequences for the varying load current may be calculated on-line, or they may be precalculated and stored in a look-up table for the control. The calculation of these modulation sequences with dead times for the varying load current is excluded from this thesis, and they will be studied in the future.

3.2 Motor terminal overvoltage mitigation for multilevel inverters

This section discusses an overvoltage reduction method for multilevel inverters, which are presented in Publications **III** and **IV**. A method with the same principle was first studied in (Lee and Nam, 2002), but the timing of the switching operations presented in the paper applies only to an ideal transmission line. The paper presents a low-voltage three-level inverter applying a modulation where the neutral output voltage is used for a period of $2t_{\mathrm{d}}$. This places the second switching operation approximately in the opposite phase of the motor terminal voltage oscillation, and the overvoltage is thereby reduced. The voltage waveform produced by this modulation strategy resembles that of a two-level VSI. To develop the method in (Lee and Nam, 2002) further, the study in this doctoral thesis was extended to general multilevel inverters, and the effect of cable distortion was introduced and discussed in Publications **III** and **IV**.

3.2.1 Edge modulation principle

In this thesis, the method that uses consecutive switching operations of a multilevel inverter to reduce the motor terminal overvoltage is referred to as edge modulation. Each switching operation performed by an inverter results in an oscillating overvoltage at the motor terminals. The principle of the method is to select a time interval Δt_{sw} between two switching operations so that the oscillations will damp each other. Theoretically, the voltage edges are transmitted through an ideal transmission line and they face a load with $\Gamma_{\mathrm{L}} = 1$, and as the inverter reflection coefficient is $\Gamma_{\mathrm{S}} = -1$, the oscillations will completely cancel each other out. Here, $\Delta t_{\mathrm{sw}} = 2t_{\mathrm{d}}$ applies to an ideal overvoltage mitigation.

It has been shown in the literature that a motor cable is not an ideal transmission line (Skibinski et al., 1997). The cable has DC losses and frequency-dependent losses, caused for example by skin and proximity effects (Skibinski et al., 1997). The frequency-dependent factors distort the voltage edge so that the voltage edge is slightly filtered. Every time a propagating voltage travels through the cable, it is filtered again. This impacts on the edge modulation in two ways – the peak residual overvoltage rises and the time interval Δt_{sw} has to be adjusted to achieve the minimum overvoltage. The distortion caused by the cable increases with the length of the cable. Thus, the longer the cable, the larger is the time interval Δt_{sw} compared with t_{d}.

Another factor that has an influence on the residual overvoltage amplitude when using edge modulation is the impedance mismatches at the cable ends. When the reflection coefficient at the motor terminals is decreased from $\Gamma_{\mathrm{L}} = 1$, it increases the residual overvoltage. The residual overvoltage will also increase, if the inverter-side reflection coefficient is increased from $\Gamma_{\mathrm{S}} = -1$ (Lee and Nam, 2002).

A new modeling method for the motor terminal voltage was presented in Publication **III**. The modeling is carried out by measuring the voltage from the motor terminals and extracting an oscillating overvoltage from the measured data. The modeling method does not take into account the DC link fluctuation nor the variation in the voltage edge waveform when the load current changes. Moreover, the actual voltage edges may differ when the transition is performed by an IGBT or by a freewheeling diode. Edge modulation does not usually suffer from the variation in the load current, since the consecutive switching operations are made approximately at the same current.

The edge modulation method is modeled in Figure 3.6 with the method described in the previous paragraph. The voltage waveform was extracted from a measurement where the topology is cascaded H-bridges, feeding a 300 m motor cable with an open end and the DC link voltage of a single PEBB is $u_{\mathrm{DC}} = 975\,\mathrm{V}$. The propagation delay of the cable was $t_{\mathrm{d}} = 2.28\,\mu\mathrm{s}$ and the peak voltage of a oscillating voltage from a single edge was $\hat{u}_{\mathrm{motor}} = 1.92\,u_{\mathrm{DC}}$. The minimum overvoltage was achieved when the time interval was $\Delta t_{\mathrm{sw}} = 2.28 t_{\mathrm{d}}$ and the peak motor voltage was $\hat{u}_{\mathrm{motor}} = 2.39\,u_{\mathrm{DC}}$.

A multilevel inverter is able to switch voltage levels that are proportional to the inverter nominal voltage. For example, if the DC link voltage of a three-level inverter is u_{DC}, the inverter

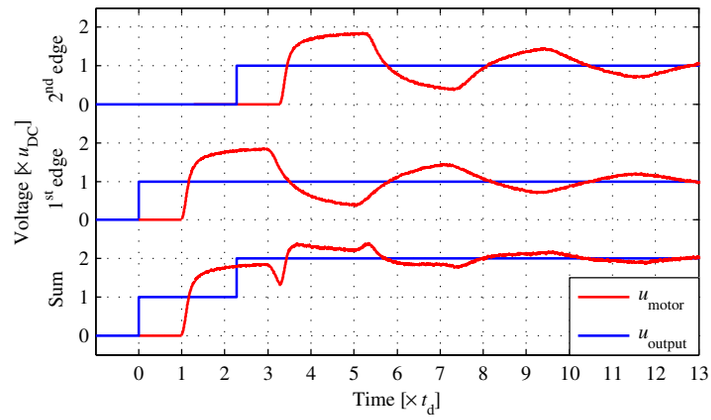


Figure 3.6. Modeled motor terminal voltage with accumulation of the measured motor terminal overvoltages. The time interval between the switching operations is $\Delta t_{sw} = 2.28 t_d$ and the peak motor terminal voltage is $\hat{u}_{motor} = 2.39\, u_{DC}$.

may produce a voltage edge of $u_{DC}/2$. Hence, the peak overvoltage caused by a single voltage transition is $1.5\Gamma_L u_{DC}$. As the number of voltage levels is increased, the proportional overvoltage decreases. Considering for instance the modeled voltages in Figure 3.6, if the inverter were a three-level inverter applying a traditional multilevel PWM, the peak overvoltage at the motor terminals would be 146 % of the full DC link potential. If the edge modulation were applied, the modeled case in Figure 3.6 would result in $\hat{u}_{motor} = 1.20\, u_{DC}$.

Edge modulation was simulated by a three-level topology shown in Figure 3.7. The overvoltage mitigation achieved by the method does not generally suffer from load current variation, because the consecutive switching operations are approximately at the same current. The DC link voltage for the simulation was $u_{DC} = 565$ V and the cable length was 60 m with $t_d = 310$ ns. A dead time of 1 µs was used. The time interval resulting in the minimum residual overvoltage was found to be $\Delta t_{sw} = 710\,\text{ns} = 2.29 t_d$. The motor cable was simulated by a lumped model with one-meter sections. The model is shown in Figure 2.2 and the parameters are given in Table 2.1 (Moreira et al., 2002). The load parameters are $L_{load} = 625$ mH and $R_{load} = 231$ mΩ.

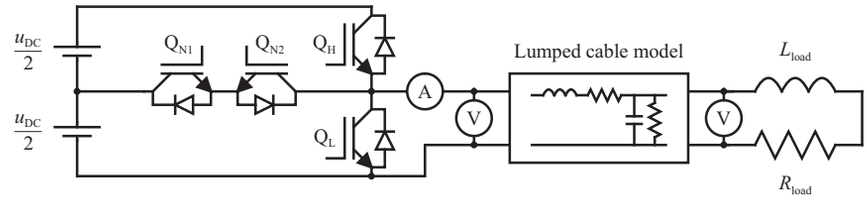


Figure 3.7. Three-level inverter topology.

The initial currents used for the simulation shown in Figure 3.8 were (a) 1 A, (b) −1 A, and

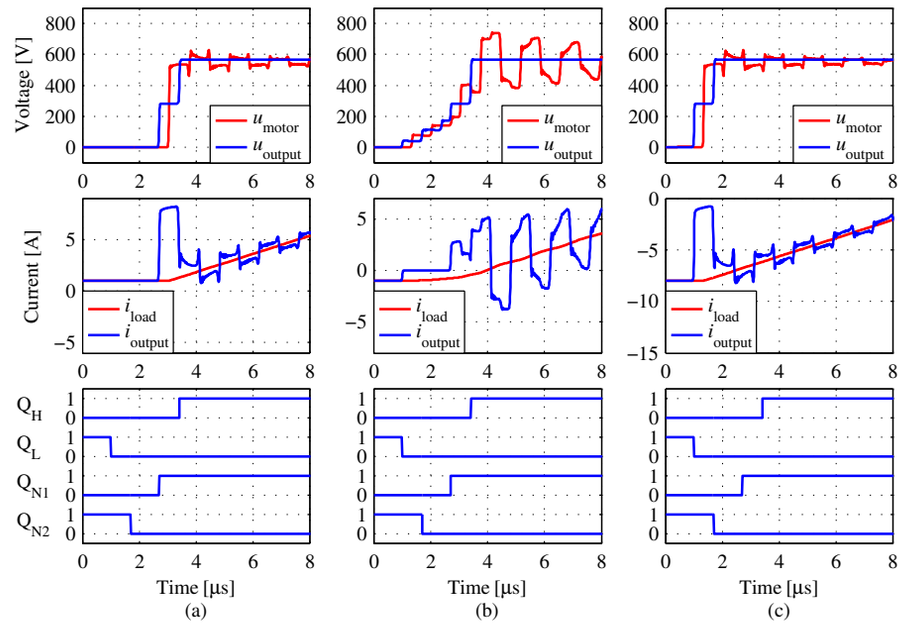


Figure 3.8. Simulated inverter output and motor voltages (top), and inverter output and load currents (middle). The control sequence is shown in the bottom figure. A 60 m cable was used for the simulation, and $\Delta t_{sw} = 710\,\text{ns} = 2.29 t_d$. The initial load currents are (a) 1 A, (b) -1 A, and (c) -8 A.

(c) -8 A. As the DC link voltage was fed to the cable as a step function, a charging current of $i = u_{DC}/Z_c$ is seen at the inverter output. The method functions as expected when the current direction does not change during Δt_{sw}, as can be seen in Figures 3.8a and 3.8c. The peak motor terminal overvoltage was $\hat{u}_{motor} = 628\,\text{V} = 1.11\,u_{DC}$ in Figures 3.8a and 3.8c. The residual overvoltage may increase as a result of unsuccessful oscillation accumulation as the inverter current is clamped to zero amperes during Δt_{sw}, as presented in Figure 3.8b. The peak motor terminal overvoltage is increased to $\hat{u}_{motor} = 740\,\text{V} = 1.31\,u_{DC}$. The current zero clamping takes place because the output voltage from the phase is connected to the neutral point and the current path is blocked until the switch Q_{N1} starts to conduct.

3.2.2 Level-to-level modulation principle

A special case of edge modulation is the minimum pulse that can be achieved by accumulating two oscillating voltages. This modulation pattern is referred to as level-to-level modulation in Publication **IV**. The accumulation is made for consecutive oscillations for the switching operations in opposite directions. The first oscillation has a full period at the motor terminal before the counter oscillation interacts with it. Consequently, Δt_{sw} will be $4t_d$ for an ideal transmission line and over $4t_d$ for an actual motor cable.

Simulations of the level-to-level modulation are presented in Figure 3.9. The topology and the simulation parameters were the same as for Figure 3.8, but now the initial currents were set to (a) 10 A and (b) −10 A. In addition, the time interval was set according to the level-to-level modulation at $\Delta t_{sw} = 1.42\,\mu s = 4.58 t_d$. For both of the simulations the motor peak overvoltage was −132 V, which corresponds to $\hat{u}_{motor} = 1.23\,u_{DC}$. The residual overvoltage is higher than with the edge modulation, because the first voltage edge has traveled through the cable for two additional cable lengths. The oscillation has attenuated during this time, and the accumulation leads to a higher residual overvoltage. The control for the level-to-level modulation depends on the current direction so that the bidirectional switches to the neutral point conducts current during the zero output voltage period.

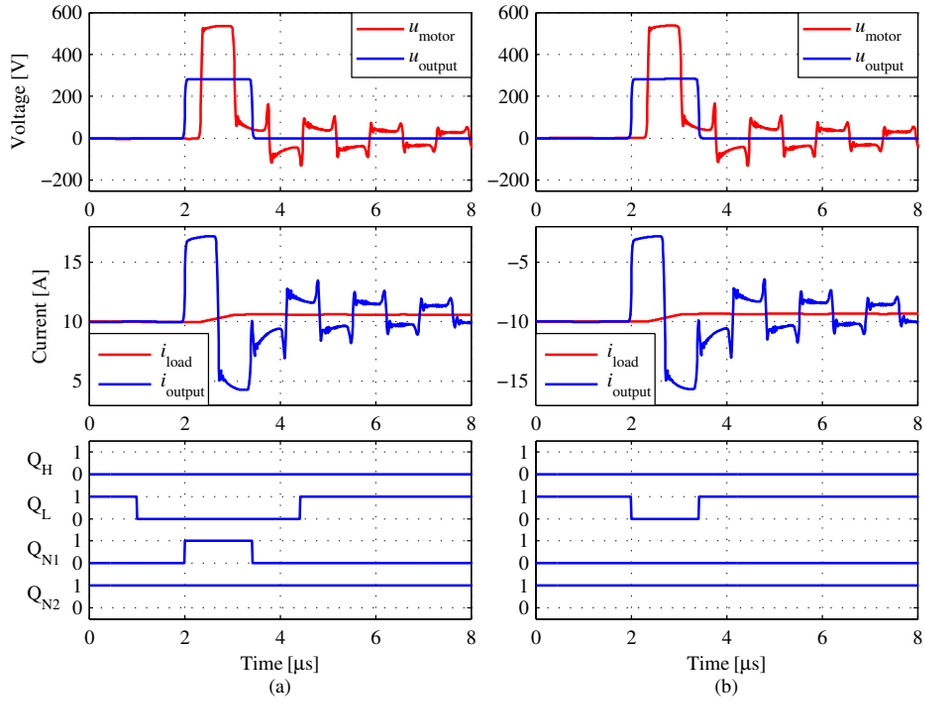


Figure 3.9. Simulated inverter output and motor voltages (top) of the level-to-level modulation. The inverter output and load currents are shown in the middle and the control sequences in the bottom figure. A 60 m cable was used for the simulation and $\Delta t_{sw} = 1.42\,\mu s = 4.58 t_d$. The initial load currents are (a) 10 A and (b) −10 A.

Level-to-level modulation is used only for very low and high duty cycles, and it is seldom used in the PWM pattern. A drawback of this special case is that it depends on the cable length and Δt_{sw}, and the motor modulator has this fixed short pulse between the overmodulation and the regular minimum pulse requirement. In the case of a three-level inverter, the pulse must be longer than the IGBT minimum pulse.

3.2.3 Discussion

The PWM generation will change considerably when applying edge modulation because of the loss of active modulation levels. Besides this change, the motor control remains approximately the same. The minimum pulse requirement has to be modified for edge modulation. In the case of a three-level inverter, the total pulse consists of the rise and fall Δt_{sw} and the initial minimum pulse. If a multilevel inverter with over three voltage levels is used, the switching operations can be cycled between the IGBTs or PEBBs, and narrow voltage pulses can be produced without switching a single IGBT consecutively. In this case, the minimum pulse is $2\Delta t_{\mathrm{sw}}$ and a narrow pulse can, in theory, be of the length of a control clock cycle.

The method reduces the peak overvoltage considerably, but it also damps the oscillation that produces several high $\mathrm{d}u/\mathrm{d}t$ edges to the motor terminals. However, the voltage transition when using the edge modulation has the same $\mathrm{d}u/\mathrm{d}t$ as the first edge of any switching operation without using the method.

Compared with the regular operation of a multilevel inverter, the use of edge modulation increases the common-mode voltage produced by the inverter. This is due to the loss of active voltage levels. In addition, the switching losses are approximately doubled if the same apparent switching frequency is maintained when making the transition from the traditional multilevel PWM to the edge modulation. The apparent switching frequency discussed here considers the two consecutive switching operations as a single voltage transition. This is because during a single PWM period, the edge modulation uses two switching operations for each rising and falling edge. Edge modulation increases the voltage transition amplitude during a single PWM period. Therefore, even if the same apparent switching frequency is used, the current ripple is still increased with the edge modulation compared with the multilevel PWM. To compensate the increased load current ripple, the switching frequency should be higher with the edge modulation.

The propagation delay of the cable changes with the cable temperature. With a fixed Δt_{sw} this will result in an increased residual overvoltage when the temperature deviates from the original temperature at which the Δt_{sw} resulting in the minimum overvoltage was assigned. If the behavior of the propagation velocity as a function of cable temperature is known, Δt_{sw} can be varied with temperature. Yet, measuring the ambient temperature may not be a sufficient approach to compensate the error, since the cable temperature also changes with the current flowing through it. This remains a future research topic. Other factors that may cause variation in the cable characteristics are aging of the materials, changes in the air humidity, and mechanical stress. Another approach to adjust the ideal Δt_{sw} would be on-line tracking with a voltage measurement at the motor terminals, or a current measurement at the inverter output. The measurement resolution should be sufficient to detect the effect of the varying Δt_{sw} on the peak overvoltage.

3.3 Motor terminal overvoltage suppression for parallel inverters

It has been shown in the previous section that oscillating voltages at the motor terminals can be accumulated and the oscillations damped with correctly timed switching operations of a multilevel inverter. Parallel inverters may operate as a multilevel inverter with the use of inductive voltage division (Cougo et al., 2011). The multilevel operation requires the PWM patterns for the inverters to be interleaved, which can be done, for example, by using phase-shifted carrier modulation (McGrath and Holmes, 2002). Output inductors or inter-cell transformers can be used to generate the voltage division, and they are used to limit the circulating current between the inverters.

3.3.1 Method with individual motor cables

A motor terminal overvoltage mitigation method for parallel inverters by using individual motor cables from each inverter and an interleaved modulation was presented in (Miettinen, 2011). The topology for a case of two parallel inverters is shown in Figure 3.10. The patent describes how the $\mathrm{d}u/\mathrm{d}t$ can be reduced by interleaving each switching operation for the parallel inverters, and the increased number of inverters will lead to a smaller $\mathrm{d}u/\mathrm{d}t$. The basis of the method is that the impedance that a transient voltage edge interacts with at the motor terminals is reduced by the parallel cables when the voltage edges are interleaved with proper time intervals.

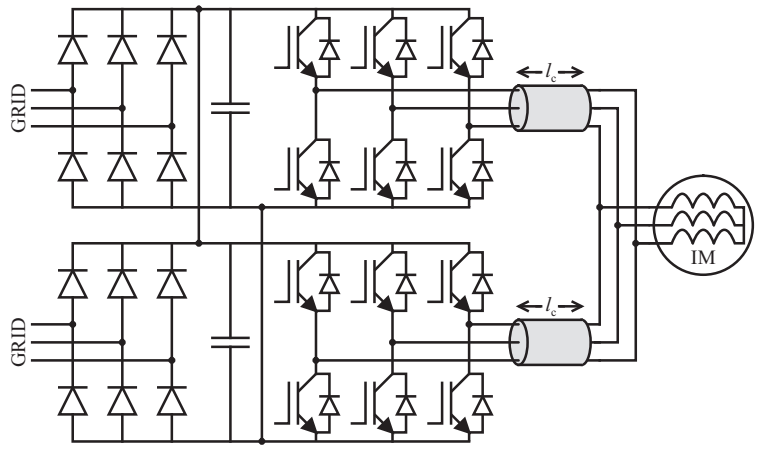


Figure 3.10. Topology of the parallel inverters with individual motor cables from each inverter and a common DC link.

Mitigation principle

An independent study of the method was conducted in Publication **V**, where the method was tested with two and three parallel inverters. The impedance for a single voltage edge at the motor terminals depends on the number of parallel cables in the point of common connection

$$Z_{\mathrm{L}} = \frac{Z_{\mathrm{c}} Z_{\mathrm{m}}}{Z_{\mathrm{c}} + Z_{\mathrm{m}}(n-1)}, \tag{3.4}$$

where n is the number of parallel inverters. The overvoltage can be reduced by interleaving the switching operations and timing them so that the oscillations produced by each switching operation result in the lowest possible overvoltage. The modulation patterns in the case of two inverters are depicted in Figure 3.11. The original PWM pattern is presented above, and the switching operations of the inverters are interleaved with an interval of Δt_{sw}.

The method is simulated with two and three inverters and with an ideal transmission line as a motor cable. The cable impedance was selected to be $Z_{\mathrm{c}} = 100\ \Omega$ and the load impedance $Z_{\mathrm{m}} = 1500\ \Omega$. When two inverters were used, the overvoltage was reduced by $\Delta t_{\mathrm{sw}} = 2t_{\mathrm{d}}$. Such a simulation is shown in Figure 3.12a. For each oscillation, a counter oscillation timed $2t_{\mathrm{d}}$ after the first edge results in a successful accumulation. If an uneven number of inverters are used, one oscillation is left without a counterpart. As seen in Figure 3.12b, with an ideal transmission line this would result in a residual overvoltage.

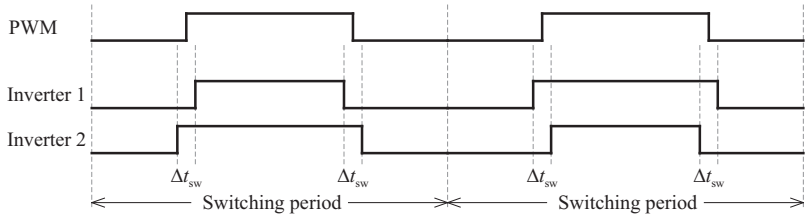
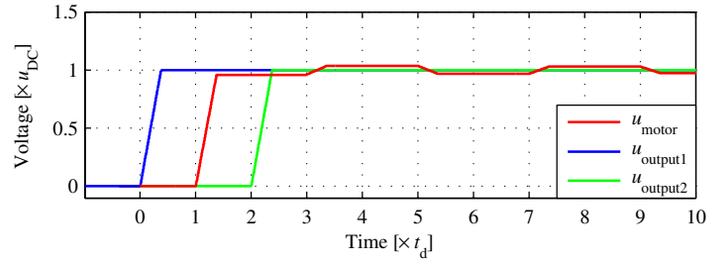


Figure 3.11. Control principle of overvoltage mitigation for parallel inverters. The top graph represents the original PWM signal, and the duty cycles of the parallel inverters are presented below.

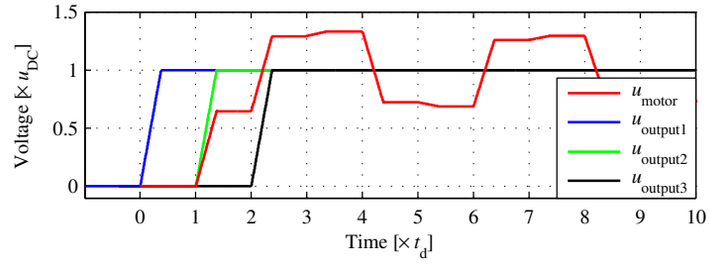
When parallel inverters are not switched simultaneously, the parallel inverters are connected to different DC link potentials, and a circulating current is produced in a phase. When using individual motor cables, the current loop does not close before the voltage edge has traveled to the motor and back to another inverter through its individual cable. When $\Delta t_{\mathrm{sw}} = 2t_{\mathrm{d}}$, the circulating current amplitude for two parallel inverters is

$$i_{\mathrm{circ}} = \frac{u_{\mathrm{DC}}}{Z_{\mathrm{c}}}. \tag{3.5}$$

The circulating current will increase if $\Delta t_{\mathrm{sw}} > 2t_{\mathrm{d}}$.



(a) $n = 2$



(b) $n = 3$

Figure 3.12. Simulated inverter and load terminal voltages with ideal transmission lines. The time interval between the first and last switching operation is $\Delta t_{sw} = 2t_d$. The load peak voltages are (a): $\hat{u}_{motor} = 1.04\,u_{DC}$ and (b): $\hat{u}_{motor} = 1.33\,u_{DC}$.

Varying filtering result as a function of load current

As described in Section 3.2, a motor cable is not an ideal transmission line. The skin and proximity effects distort the voltage edges (Skibinski et al., 1997), and the accumulation is ideal with a Δt_{sw} that is above $2t_d$. The method was simulated with two parallel inverters and with 60 m motor cables, the cable model is shown in Figure 2.2, and the parameters are given in Table 2.1 (Moreira et al., 2002). The dead time was 1 µs and the DC link voltage $u_{DC} =$ 565 V. The LR load parameters were $L_{load} = 625$ mH and $R_{load} = 231$ mΩ. The simulation results are given in Figure 3.13.

As shown in Figure 3.13a, the accumulation is not ideal with an initial load current of 0.4 A. Immediately when the voltage edge from the first inverter has arrived at the second inverter, the circulating current starts to flow. The current changes polarity at the second inverter, and since this change takes place during a dead time, the voltage will change polarity prematurely. This will lead to a higher peak overvoltage than in an ideal mitigation.

When the load current amplitude is higher than twice the circulating current, the output voltage does not suffer from the negative effects of the dead time. In Figure 3.13b, the initial load current is 30 A, and the minimum residual overvoltage is achieved with the simulated configuration.

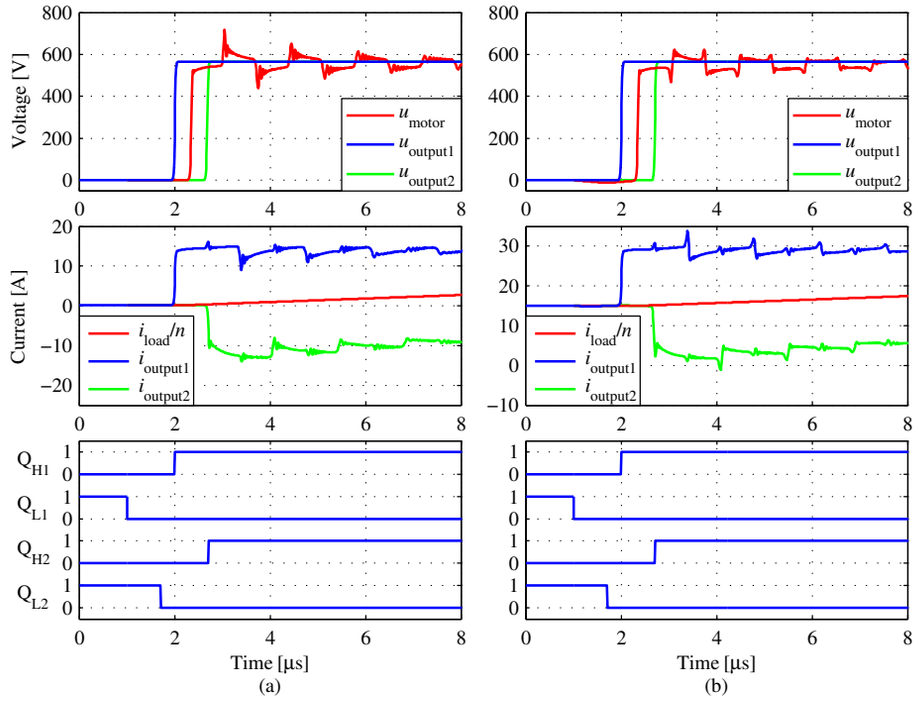


Figure 3.13. Simulated inverter output and load voltages (top) and inverter and load currents (middle) when $n = 2$. The gate drive signals are shown in the bottom figures. The cable length is 60 m with a propagation delay of $t_d = 310$ ns and $\Delta t_{sw} = 710\,\text{ns} = 2.29 t_d$. The initial load currents are (a) 0.4 A and (b) 30 A. The simulated peak motor terminal voltages are (a) $\hat{u}_{motor} = 718\,\text{V} = 1.27\,u_{DC}$ and (b) $\hat{u}_{motor} = 623\,\text{V} = 1.10\,u_{DC}$.

Current balancing among inverters

The current balancing method between the inverters was presented in Publication **V**. To ensure symmetric loading, the order of the switched inverters is cycled. The cycling is carried out by the PWM switching period time level, as shown in Figure 3.11. The symmetric currents increase the inverter lifetime compared with an asymmetric loading, where one of the inverters will carry a considerably larger current. The method does not take into account the asymmetry in the IGBT characteristics, which may cause circulating currents (Cai et al., 2008). To compensate these tolerances, the continuous cycling could be paused for a switching period whenever needed. During this pause, one of the inverters carries a larger proportion of the load current for a longer period.

The interfacing between the motor control and the modulation for the overvoltage reduction are shown in Figure 3.11. The original PWM duty cycle corresponds to the desired volt-seconds that would be fed to the motor if the mitigation method was not used. This

implementation would require the switching times to be known at the beginning of the PWM period, so that Δt_{sw} can be calculated. Another approach is that the PWM switching operation functions as a trigger for the Δt_{sw} generation and the whole PWM period is delayed. The minimum pulse will be defined by the inverter that has the shorter pulse. Therefore, the total requirement is $2\Delta t_{sw}$ and the initial minimum pulse requirement.

Discussion

When the number of parallel inverters is above three, several inverters should be switched synchronously to avoid an increase in the circulating current. Therefore, as presented in (Miettinen, 2011), increasing the total Δt_{sw} in order to reduce the $\mathrm{d}u/\mathrm{d}t$ is not advisable. The reason for limiting the time interval is the increased circulating current. Moreover, the operation below the current amplitude of $2i_{circ}$ will result in an increased overvoltage, because the inverters that are in the freewheeling mode and have not been switched before will change polarity at $\Delta t_{sw} = 2t_d$.

Even though connecting individual motor cables from each inverter is an unorthodox topology, parallel cables may have to be used in high-current applications, where they are used to increase the cable cross-sectional area to withstand the load current (Saunders et al., 1996).

For two parallel inverters, the peak overvoltage was simulated to increase from $1.10\,u_{DC}$ to $1.27\,u_{DC}$ when the time interval was reduced from the ideal $\Delta t_{sw} = 2.29t_d$ to $\Delta t_{sw} = 2t_d$. The measurement results in Publication **V** also show an increase in the peak overvoltage between the ideal time interval and $\Delta t_{sw} = 2t_d$. However, the increase is only from $1.28\,u_{DC}$ to $1.33\,u_{DC}$. As the increase is not dramatic, a new approach for the topology can be used. In the case of partial loading, the load current is reduced. When the load current decreases to a value at which it can be carried by only one of the inverters, it may be more energy efficient to stop switching the other inverter. In this case, the topology will function as presented in (Shimizu et al., 2012).

As mentioned in Section 3.2, the cable transport delay is a function of cable temperature. The method is based on correctly timed switching operations that are dependent on the transport delay, and the previously mentioned measures may have to be taken to guarantee the ideal mitigation.

3.3.2 Method with output inductors

This section introduces the principle further discussed in Publication **VI**. The fundamental principle of inductive voltage division can be applied to produce a third voltage level at zero volts for the purpose of motor terminal overvoltage reduction. The topology used for the overvoltage mitigation method is depicted in Figure 3.14. Now, the emphasis of the inductive component dimensioning is on limiting the circulating current during the time when the parallel inverter legs of the same phase are deliberately connected to opposite DC potentials.

The aim of this procedure is to produce the third voltage output voltage level.

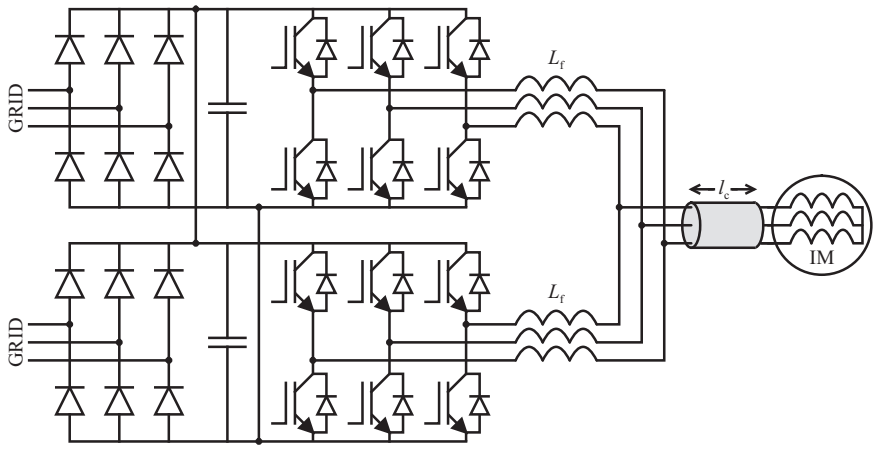


Figure 3.14. Topology of the parallel inverters with output inductors and a common DC link.

The control principle is the same as with the method discussed in Section 3.3.1, and the inverter control is shown in Figure 3.11. The key difference lies in the timing of the Δt_{sw}, where instead of selecting the time interval strictly based on the cable characteristics, the output inductor contributes to the oscillation frequency seen at the motor terminals. The additional inductance increases the oscillation frequency, and Δt_{sw} is assigned so that the oscillations induced by the consecutive switching operations are in the opposite phase.

The key difference with the method shown in Section 3.3.1 in terms of circulating current is that with the point of common connection, the circulating current will start after $2t_d$. With the output inductors and the point of common connection placed right after the inductors, the circulating current does not have such a transport delay. The circulating current amplitude is

$$i_{circ} = \frac{u_{DC}\Delta t_{sw}}{2L_f}, \tag{3.6}$$

if the cabling impedances are neglected.

The reflection coefficient at the inverter end is now defined by the inductor. For an ideal inductor, the reflection coefficient would be $\Gamma_S = 1$, but an actual inductor will have parasitic capacitance, and copper and possible core losses affecting the impedance.

Different operation modes of the method

The operation of the control for the mitigation method is divided into different modes determined by the load current. The reason for modifying the control is to compensate the effects of dead time during the voltage transition. The method was simulated with two parallel inverters with output inductors of $L_f = 20\,\mu H$, with a DC link voltage of 565 V, and a

60 m motor cable model. The cable model is shown in Figure 2.2 and the parameters in Table 2.1 (Moreira et al., 2002). The dead time was 1 µs. The time interval resulting in the minimum overvoltage was found to be $\Delta t_{sw} = 1.15\,\mu s$, and the circulating current amplitude was $i_{circ} = 16.2\,A$. The simulation results are presented in Figures 3.15 – 3.16.

The simulations of a rising voltage edge with a positive load current are shown in Figure 3.15. In Figure 3.15a, the initial load current was 40 A. As the initial inverter current amplitude is greater than the circulating current, the control signals are interleaved by Δt_{sw}. A residual voltage oscillation is seen at the motor, which is at the frequency caused by the cable transport delay. When the initial inverter current amplitude is reduced to be lower than the circulating current in Figure 3.15b, the control is reassigned. Now, Δt_{sw} is between the higher switch control signal of the first inverter and the lower switch control signal of the second inverter.

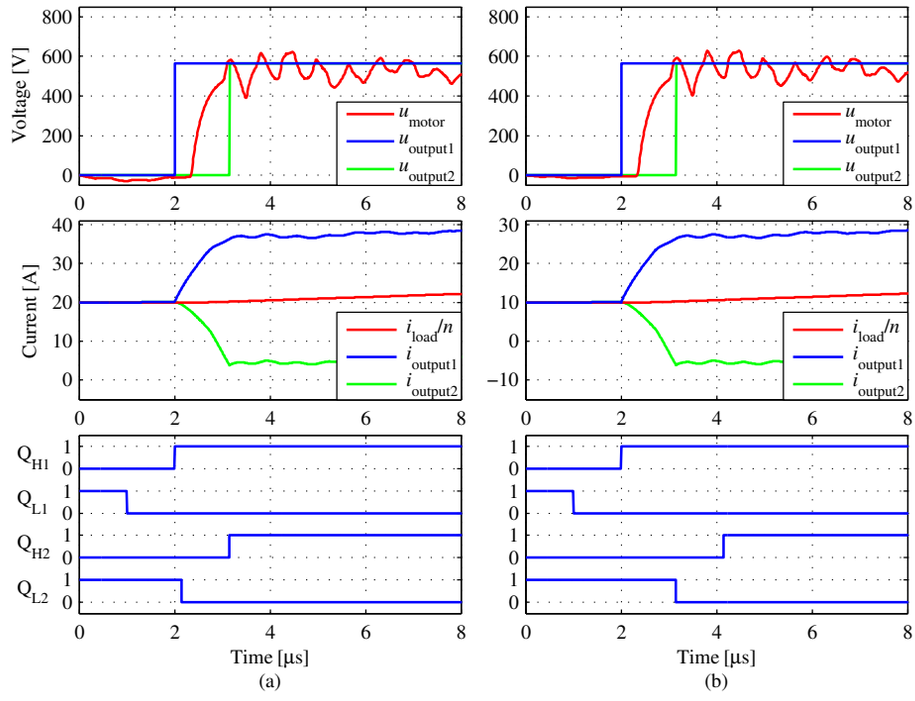


Figure 3.15. Simulated inverter output and load voltages (top) and inverter and load currents (middle) when $n = 2$. The gate drive signals are shown in the bottom figures. The cable length is 60 m with a propagation delay of $t_d = 310$ ns and $\Delta t_{sw} = 1.15\,\mu s = 3.71 t_d$. The initial load currents are (a) 40 A and (b) 20 A. The simulated peak motor terminal voltages are (a) $\hat{u}_{motor} = 623\,V = 1.10\,u_{DC}$ and (b) $\hat{u}_{motor} = 628\,V = 1.11\,u_{DC}$.

Next, a rising edge was simulated with a negative load current, shown in Figure 3.16. With the negative load current, the control signals are interleaved by Δt_{sw}. Figure 3.16a illustrates a case where the inverter current amplitude is larger than the circulating current and the mitigation functions ideally. When the inverter current amplitude is lower than i_{circ}, the sequence

will start when the lower switch of the first inverter is set to a nonconductive state, and the output voltage will rise. This causes the inverter current to rise until the current is clamped at zero amperes. Because of the dead time, the voltage will decrease back to the amplitude of the output inductor. This behavior leads to an unsuccessful accumulation as seen in Figure 3.16b.

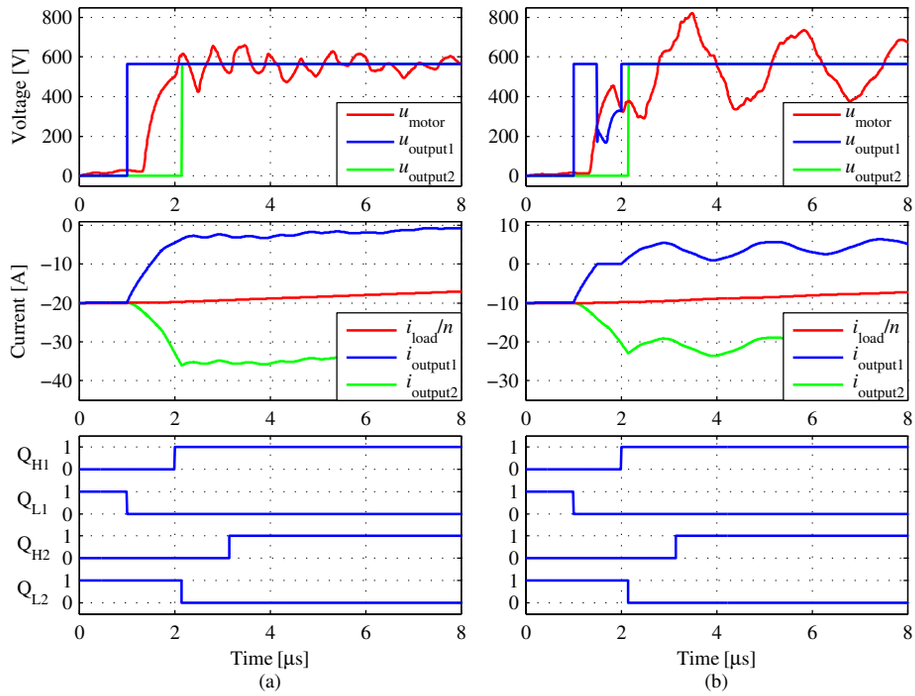


Figure 3.16. Simulated inverter output and load voltages (top) and inverter and load currents (middle) when $n = 2$. The gate drive signals are shown in the bottom figures. The cable length is 60 m with a propagation delay of $t_d = 310$ ns and $\Delta t_{sw} = 1.15\,\mu s = 3.71 t_d$. The initial load currents are (a) -40 A and (b) -20 A. The simulated peak motor terminal voltages are (a) $\hat{u}_{motor} = 659\,V = 1.17\,u_{DC}$ and (b) $\hat{u}_{motor} = 821\,V = 1.45\,u_{DC}$.

Discussion

The motor control approach is identical to the case illustrated in Figure 3.11 and discussed in Section 3.3. The current balancing between the inverters is implemented by the same control principle as presented in Figure 3.11. The circulating current will not always decay to zero, and thus, the inverters will have different initial currents at the beginning of Δt_{sw}. By cycling of the switching turns between the PWM periods, the currents can be balanced. As it was found in Publication **VI**, the continuous cycling of the duty cycles may not guarantee the current balance. The cycling may be controlled and the balance may be achieved over a longer period.

The inductor dimensioning is of key importance to the method. A basic target is that the inductance is as small as possible. However, an opposing factor is that the circulating current should also be as small as possible. The dimensioning procedure can be carried out by assigning a maximum circulating current and inductance. With these parameters, the maximum Δt_{sw} can be acquired by using (3.6). This limits the maximum cable length that can be used with the design parameters. When using a shorter cable, the time interval is reduced and the circulating current along with it.

The method could be implemented with an inter-cell transformer. In that case, the magnetizing inductance would restrict the circulating current and the stray inductance would function similarly as an individual output inductor. The stray inductance therefore determines the $\mathrm{d}u/\mathrm{d}t$ and Δt_{sw} with the motor cable. Compared with individual inductors, the method benefits from the reduced circulating current. However, with an increased magnetizing inductance, the inter-cell transformer cannot be considered a small inductive component, and the benefits sought in smaller passive elements are not reached.

3.4 Comparison of the active filtering methods

In this section, the filtering capabilities of the studied active filtering approaches are discussed. Experimental results for each method are presented in Publications **I** – **VI**, and the filtering results are presented in Table 3.3. The varying peak motor overvoltages presented in the table are caused by the dead-time-related variation. It must be noted that the comparison of the measured values is not absolute, since the measurement setups and the voltage range varied with the different filtering methods.

Table 3.3. Residual motor overvoltages for the studied methods from Publications **I** – **VI**.

Filtering method	l_{c} [m]	$\hat{u}_{\mathrm{motor}}$ [%]
Active $\mathrm{d}u/\mathrm{d}t$	100	102–107
Edge modulation	90	119
	300	120
Level-to-level	300	126
Parallel, individual cables, $n = 2$	20	128–137
Parallel, individual cables, $n = 3$	20	136–143
Parallel, output inductors, $n = 2$	25	114–154

The active $\mathrm{d}u/\mathrm{d}t$ reduces the motor terminal overvoltage by extending the voltage transition time of the PWM voltage edge. The charge period for a single pulse measurement in Publication **II** was 4.8 µs, and for the cable length of 100 m the filtering result was close to ideal. However, the filtering result varies with the cable length when t_{cp} is fixed. The relations between the cable length and the required charge time for different residual overvoltages are presented in (Ström et al., 2011). In the paper, it is approximated by simulations which cable lengths result in a peak motor terminal voltage of 100 % u_{DC}, 130 % u_{DC}, and 150 % u_{DC} with

a certain t_{cp}. With $t_{cp} = 4.8\,\mu s$, a motor cable of 110 m can be driven without any overshoot at the motor terminals, a 155 m cable with a 130 % u_{DC} overvoltage, and a 188 m cable with a 150 % u_{DC} overvoltage. This study expects a successful charging of the filter capacitor with no filter output resonance.

Edge modulation and level-to-level modulation can operate at a fairly constant residual overvoltage. The overvoltage in Table 3.3 has been scaled to represent a three-level inverter with a DC link voltage of 1.95 kV. The tested prototype was a seven-level CHB inverter with a PEBB DC link voltage of 975 V. As discussed in Section 3.2, the residual overvoltage may increase when operating close to a zero load current. When the results from Publications **III** – **IV** are compared with the results presented (Lee and Nam, 2002), the motor terminal voltages are almost similar. Even though the results in (Lee and Nam, 2002) are based on the theory of ideal transmission lines, the results appear to have been measured with $\Delta t_{sw} \neq 2t_d$. Nevertheless, these results do not reach the full potential of the filtering method, unlike in Publications **III** – **IV**.

The filtering method for parallel inverters with individual motor cables was tested with a scaled prototype with $l_c = 20\,m$. The rated current of the inverters was 34 A, which is low compared with traditional parallel drive installations. The premature voltage transition resulting from the dead time close to the zero load current made the motor voltage increase by 9 % u_{DC} when two parallel inverters were used, and by 7 % u_{DC} with three parallel inverters. The studied method for parallel inverters with individual cables was first presented in (Miettinen, 2011). The patent does not provide any measurements, and thus, the comparison is not feasible.

The method for parallel inverters using output inductors was also tested with the scaled prototype. The overvoltage reduction varied significantly with the load current. Similarly as with the other method for parallel inverters, the premature voltage transitions caused by the dead time at the load current below the circulating current increased the overvoltage by 40 % u_{DC}.

3.5 Comparison of the studied methods with the passive solutions

Compared with the existing passive filtering solutions, the studied methods reach similar filtering results. With the du/dt filters, the residual overvoltage at the motor terminals is determined by the ratio of rise time to propagation time. This excludes the parallel LR filter (illustrated in Fig. 2.5a), which, along with the du/dt reduction, uses a voltage division between the resistor and the cable impedance. The longer the voltage rise times are, the longer cables can be used with the allowed residual overvoltage. When comparing the passive solutions of LR, LCR, and LC filters with clamping diodes (von Jouanne and Enjeti, 1997; Habetler et al., 2002; Akagi and Matsumura, 2011), the parallel LR filter has been found to reach the voltage limitation with the smallest output inductance value. The dimensioning of the LC circuits applied to the other filter topologies can be carried out differently, but decreasing

the filter inductance will lead to larger filter currents. The LR filter was found to limit the motor voltage to $\hat{u}_{\text{motor}} = 1.43\,u_{\text{DC}}$ for a 100 m cable with an output inductor of $L_{\text{f}} = 30\,\mu\text{H}$ and $\hat{u}_{\text{motor}} = 1.39\,u_{\text{DC}}$ for a 200 m cable with an output inductor of $L_{\text{f}} = 70\,\mu\text{H}$ (Akagi and Matsumura, 2011). The resistor of the LR circuit was $R_{\text{f}} = 33\,\Omega$. The experimental active $\text{d}u/\text{d}t$ filter with $L_{\text{f}} = 16\,\mu\text{H}$ and $C_{\text{f}} = 0.33\,\mu\text{F}$ results in a charge period of 4.8 µs. With this filter, the residual overvoltage for a 100 m cable was $\hat{u}_{\text{motor}} = 1.02 - 1.07\,u_{\text{DC}}$. Hence, we may conclude that the active $\text{d}u/\text{d}t$ provides a better filtering result even with approximately half of the filter inductance. This will make the active $\text{d}u/\text{d}t$ more appealing especially for high-current applications.

The other studied methods, discussed in Sections 3.2 – 3.3, are comparable with the cable termination circuit in the filtering sense. This is because these active filtering methods reduce the overvoltage by accumulating the oscillating voltages instead of reducing the voltage transition time. When correctly dimensioned, the cable terminator circuit should eliminate the residual overvoltage. As for the studied methods, there will always be a residual overvoltage.

The trade-offs between the passive and active filtering methods are in the passive filter size and the inverter losses. For the active $\text{d}u/\text{d}t$ the filtering result was found superior to the passive methods with a smaller filter, but the inverter losses are larger with the active $\text{d}u/\text{d}t$ because of the additional switching operations (Tyster et al., 2011). For edge modulation, the trade-offs for operating without a filter are the additional switching operations, increased common-mode voltage, and degraded power quality. The active filtering methods for parallel inverters compete well with the passive filters, since the only contributor to additional losses is the circulating current. A drawback is the possible additional noise that may be generated by the circulating current, which is minimal with conventional filtering methods.

3.6 Discussion

The studied filtering methods all are based on controlling an element that has an oscillating step response. For the active $\text{d}u/\text{d}t$, this resonating element is an LC circuit, and for the rest of the studied methods, it is the motor cable oscillation. It was shown that the resonance could be attenuated by a counterpart, and distortion and losses produced to the resonances degrade the overvoltage reduction.

Edge modulation and the parallel inverter mitigation methods apply the inherent characteristics of the inverter to limit the motor terminal overvoltage. The topologies are able to produce an output voltage waveform that interacts with the motor terminal voltage oscillation.

Even though the voltage transitions were presented mainly for rising voltage edges of the PWM cycle, the switching phenomenon is identical to the falling voltage edges. As it is known, the inverter current direction has an effect on the output voltage in terms of the potential during the dead time. Considering the methods that have a need to compensate or change the control with the output current, the presented controls are applicable to falling voltage edges, when the current direction is taken into account. The methods are symmetrical in

terms of current direction.

All the active filtering methods require some overrating to operate at the same switching frequency as without the method. The active du/dt and the edge modulation increase the number of switching operations, which, consequently, has to be compensated by an increased cooling capability. The active du/dt and the methods for parallel inverters increase the inverter current peak value. In the methods for parallel inverters, the switched current is averaged to be approximately the same as without the method. This is achieved by the cycling of the switching order. The circulating currents will, however, result in a higher inverter current ripple.

The studied methods provide protection against double pulsing, which leads to overvoltages above twice the DC link voltage. If the overvoltage is filtered completely at the motor terminal for a single voltage transition, there is no chance of two consecutive voltage edges to somehow accumulate to an overvoltage. However, any residual overvoltage and oscillation are subject to possible accumulation, and the residual overvoltage may be doubled. This is a concern especially for the methods intended for parallel inverters, because a residual overvoltage will remain at an unsuccessful accumulation.

When using the overvoltage mitigation methods for parallel inverters, the application is expected to need parallel inverters to begin with. In other words, the power required by the load exceeds the power rating of a single inverter. The prototype testing presented in Publications **V** and **VI** was performed with scaled power. With a proper power rating of the entire system, the ratio of load and circulating currents can be acceptable. For example, if the load peak current is 600 A and the maximum allowed circulating current 5 % of the peak current, this results in a peak circulating current of 30 A. This peak circulating current restricts the operation range of the method for parallel inverters with output inductors. For each output inductance value, the maximum Δt_{sw} can be calculated by (3.6), when the peak circulating current is selected. With low inductace values, in the range of $10-20\,\mu\mathrm{H}$, the cable length that can be used with the method is relatively low compared with the filtering capability of the other studied methods.

Each of the studied methods requires some modifications to the control system. If the rise and fall times of the voltage are the same, the studied methods will not affect the volt-seconds that are fed to the motor. A slight variation between the rise and fall times may be generated for example with the active du/dt, when the charge times for rising and falling edges are different because of the current and dead time compensation. The residual oscillation caused by an unsuccessful accumulation with the parallel inverter methods can also result in different rise and fall times. These variations are minor, and it can be concluded that compared with oscillating motor overvoltages, these methods provide improved performance to the volt-seconds fed to the motor.

The filtering methods depend on precise inverter output voltage timing. This requires an IGBT switching delay compensation, which is a sum of the control system, the gate driver, and the IGBT switching delays. There are differences between the approaches to the question of which delays need compensation. If the switching operations are performed in the

same direction, as in the edge modulation and the parallel inverter mitigation methods, the differences in the IGBT switching delays are limited to the component tolerances. However, an exception to this is shown in Figure 3.15b, where the current changes polarity during Δt_{sw}. For the first inverter, the voltage transition is at the positive inverter current, and the voltage transition occurs after a turn-on delay of the IGBT. The voltage transition from the second inverter is at the IGBT turn-off, and thus, a corresponding delay takes place. This is a special case for the method, but in order for the method to reach its full potential, the delays must be compensated. In the case of the active $\mathrm{d}u/\mathrm{d}t$, the sequence consists of pulses that require switching operations in both directions. Therefore, the turn-on and turn-off delays of the IGBTs must be compensated at the logic level.

For a two-level VSI applying the active $\mathrm{d}u/\mathrm{d}t$, the delays leading from the controller to the gates of the IGBTs of the same leg are approximately the same, even though some difference may be caused by the component tolerances. In the case of using several PEBBs, more sources of possible timing deviations are present. The clocks and the PWM periods must be synchronized between the PEBBs. A slight jitter can be expected in the clocks of the individual controllers placed at the PEBBs, but an error in the switching operations at such a time scale (order of nanoseconds) will not make the methods nonfeasible.

The current balancing method for parallel inverters, which cycles the switching order for each PWM period, does not guarantee an absolute current balance. This is because the duty cycles vary between the PWM periods, and one the inverters may end up carrying a larger current. Component tolerances of the IGBTs and the output inductors can also be a source of imbalance. In addition, if the methods for parallel inverters are used with a varying switching frequency modulation, such as direct torque control (DTC) (Takahashi and Noguchi, 1986), the balancing of the current will not be sufficient only with the cycling of the switching order. Therefore, the current balancing between the inverters must be carried out with an independent control.

All of the studied methods have some problems caused by dead times, because the phase current is clamped at zero amperes, and the output voltage changes polarity accordingly. For the edge modulation, the effects of dead time are minor, but for the active $\mathrm{d}u/\mathrm{d}t$ and the methods for parallel inverters, the dead time causes some problems. In theory, these problems could be overcome by reducing the dead time to zero. Then, the current will always have a controlled path through one of the IGBTs, and no freewheeling mode where the current could be clamped to zero, will occur. The control-level dead time has to compensate the turn-off and turn-on delays of the IGBTs, and thus, the logic-level dead time is probably not zero. One option to reduce the dead times is to change the traditional DC link to a Z-source inverter (Peng, 2003). The inductors can be dimensioned to limit the possible fast short circuit if the compensation of the turn-off and turn-on delays are off.

A single switching operation from a multilevel inverter does not produce an overvoltage that exceeds the limits set by standards for electrical motors. Unacceptable overvoltages are possible if resonances, such as double pulsing, occur. Edge modulation may be an extension of another modulation strategy, such as multilevel space vector modulation, for special transitions in order to avoid two simultaneous switching operations.

The mitigation methods that are based on pulse accumulation at the motor terminal, that is, the edge modulation and the methods for parallel inverters, must be tuned to have an ideal Δt_{sw} in terms of overvoltage mitigation. The approach taken in this doctoral thesis for all of the studied methods was that the tuning process was carried out by manually tracking the time interval leading to the lowest overvoltage. This approach can be used during the installation process of the inverter in an actual application. Auto-tuning or on-line tracking methods for Δt_{sw} during operation were not studied, but these are topics of future work.

The active filtering methods may pose challenges by the increased EMI compared with the conventional filtering approaches. For example, compared with a single motor cable, the method described in (Miettinen, 2011), (Korhonen et al., 2010), and Publication **V** may generate a larger amount of noise as a result of the loop formed by the parallel cables. In addition, if the active filtering method produces increased common-mode noise, as the edge modulation does, this should be taken into account in the filtering toward the grid and the EMI filtering of the frequency converter.

Chapter 4

Conclusions

Along with the progress in the power switch technology towards faster switching components, IGBTs, an interfacing problem has arisen between voltage source inverters and electrical motors. Premature motor insulation failures have been found to occur when the motor cables are above several meters in length. The fault contributor is an impedance mismatch between the motor cable and the motor, which leads to the motor terminal overvoltage.

In this doctoral thesis, the phenomenon of motor terminal overvoltage induced by the inverter switching transients is discussed. The overvoltage can exceed two times the DC link voltage if another transient is fed to the motor before the first oscillating overvoltage has decayed. Special cases concerning exceptionally high overvoltages were reviewed for parallel and series connections. The effects of terminal overvoltage on the motor were studied in brief, and the current motor insulation standards were presented. The common practice proposes various passive filtering applications to limit the overvoltage, but the literature also suggests that some active filtering methods are feasible.

4.1 Main results

This doctoral thesis focuses on studying the feasibility of implementing overvoltage limitation with decreased passive component dimensions. Active filtering approaches were investigated for three inverter configurations, traditional two-level VSIs, multilevel inverters, and parallel-connected two-level VSIs.

Active $\mathrm{d}u/\mathrm{d}t$ is a filtering method intended for traditional two-level VSIs. It reduces the inverter output voltage transition rate with an LC-type passive filter. Using an LC filter for output filtering is not a new approach, but for the $\mathrm{d}u/\mathrm{d}t$ filtering purpose, an undamped LC circuit causes an oscillating overvoltage by itself. Additional modulation of the inverter

output voltage can control the otherwise oscillating voltage. The method allows the dimensions of the filter inductor to be reduced from the traditional passive filtering methods and topologies. More importantly, the method can provide better overvoltage reduction with a smaller filter. The passive filter efficiency can be improved, because it requires no damping or impedance matching.

The active $\mathrm{d}u/\mathrm{d}t$ method has some challenges concerning the inverter overrating. The inverter has to perform additional switching operations to control the LC circuit. The filter capacitor carries a significant current during the voltage transition, which has to be taken into account in the inverter component and cooling design.

The control has to follow the inverter current and adjust the modulation sequences accordingly for each PWM voltage transition. An offset in any direction causes a residual oscillation at the filter output, and naturally, the oscillation increases with the error. The control system and hardware delays must be well known and compensated so that the inverter produces the output voltage with a high precision.

Edge modulation is an overvoltage mitigation that requires the inverter to be able to produce at least three output voltage levels. The method uses the oscillatory property of the motor terminal transient voltage to always switch two consecutive voltage edges that accumulate at the cable end. When the switching operations are timed so that the oscillations caused by the individual voltage edges are in an opposite phase, the oscillating voltages are damped.

The key advantage of the edge modulation is that the resonating overvoltage can be damped without any filters. However, the use of edge modulation comes at a price of additional switching operations and an increased common-mode voltage fed by the inverter. Multilevel inverter output voltage steps are proportional to the nominal voltage, and therefore, they do not regularly need any output filtering to meet the overvoltage standards set for new motors. The use of edge modulation reduces the number of high $\mathrm{d}u/\mathrm{d}t$ transitions at the motor terminals. However, the voltage transition rate is not reduced by the method.

In this work, two different approaches to limit the overvoltage in the case of parallel inverters were presented. Both of them apply a similar control that uses interleaving of the PWM voltages from the inverters to produce a third voltage level. The overvoltage mitigation principle is then the same as in the edge modulation, that is, the oscillations from the consecutive edges accumulate at the motor terminals. The difference between the parallel methods is topological, and the timing of the consecutive switching operations is set according to the topology.

The first studied parallel topology has individual motor cables leading from each inverter to the motor. In high-current applications, which parallel inverters most commonly are, paralleling of the cables may be required to reach a sufficient cable cross-sectional area. With this topology, the timing of the switching operations is proportional to the transport delay of the cables. The parallel cables change the impedance at the motor terminals, and the overvoltage can be reduced. The overvoltage reduction of the method is altered because of the dead time. The residual overvoltage increases when the inverter that is switched second changes voltage

polarity because of the circulating current.

The second method uses inductive voltage division to produce a zero voltage output level to the cable. The time interval between the switching operations is increased compared with the other parallel topology, since the output inductors reduce the motor terminal oscillation frequency. The method suffers from circulating currents in terms of increased losses and varying overvoltage mitigation. The effects of circulating current are more serious with this method than with the previous one, since the individual cables allow the circulating current to occur after $2t_{\mathrm{d}}$.

Both of the methods use current balancing between the inverters to ensure a longer operation span. For the parallel inverter mitigation methods, no additional switching operations are necessary. The circulating currents increase the inverter current peak and RMS values. At a very low modulation index, the circulating current is high compared with the load current, and this corresponds to the losses.

The inverters have to be developed with the active filtering methods in mind. The thermal management must compensate the possible additional switching operations. The motor control and the specific control for the filtering can be developed separately, but must be implemented together. Compared with the passive $\mathrm{d}u/\mathrm{d}t$ filtering, this is quite a different design routine, where both the inverter and the filter can be designed independently.

The active filtering methods cause some limitations in very low and high modulation index regions. The voltage transition times for these methods have a considerable effect on the minimum pulse requirement of the PWM. This is more of a concern for the active $\mathrm{d}u/\mathrm{d}t$ and the method for parallel inverters with output inductors.

The relevance of the results presented in Publications **I**–**VI** in the field of inverter output filtering is significant. All of the studied methods successfully limit the motor terminal overvoltage. Compared with passive filtering, each studied approach had a matching filtering performance either with a $\mathrm{d}u/\mathrm{d}t$ filter or a cable terminator. The advantages gained by the active filtering methods were in the reduced number or dimensions of the passive components. The trade-offs varied for each method, but typically, they were larger inverter losses and a degraded drive control performance.

The development in the field of power switches will be a great advantage for the active methods that use additional switching operations for the filtering purpose. Compared with the conventional PWM methods, these active filtering methods will benefit more in terms of increased efficiency.

Whereas the study was a success in the filtering sense, the significance of the inverter output filtering is facing a decreasing trend. In the light of the standards for electrical motors, the inverter duty motors should withstand a typical transient overvoltage. This limits the need for inverter output filtering to a case of installing a frequency converter to an older motor or a case of a special installation, where the risk of a motor insulation failure is even smaller. Then again, the studied methods prevent double pulsing, which is harmful to any motor type.

4.2 Suggestions for future work

One the key issues that tip the scales when deciding on filtering methods is efficiency. A review of the efficiencies of different inverter output methods and the overall efficiencies of the inverter, the filter, and the motor is suggested by the author. A survey of this kind will reveal whether the active methods can really compete with the passive filters.

When a motor is fed through a long cable and an overvoltage occurs at the motor terminals, the overvoltage also contributes to the common-mode voltage. The studied methods, except for the edge modulation, thus reduce the common-mode voltage peak amplitude. In addition, if the $\mathrm{d}u/\mathrm{d}t$ of the voltage edge is reduced, the common-mode voltage transitions will also increase in time. For these reasons, the effect of the active filtering methods on bearing currents should be studied.

The filtering methods for parallel inverters require a current balancing control. In Publication **V**, the cycling of the duty cycles was found to work because the time interval was short. When the method with an output inductor required a longer Δt_{sw}, the same current balancing method left some imbalance between the inverters. Therefore, a better current balancing control should be found. It should also compensate the differences between the characteristics of the IGBTs and the output inductors.

All of the studied filtering methods showed some degradation caused by the dead time. Therefore, the methods to minimize the dead time for the filtering purposes are considered to be a relevant future research topic. All of the studied methods may face some uncertainty on timing of the inverter output voltage during the operation. Thus, auto-tuning processes for initialization and control during operation to produce ideal mitigation are suggested to be a topic of further study.

References

Akagi, H. (1996), "New trends in active filters for power conditioning," *IEEE Transactions on Industry Applications*, vol. 32, no. 6, pp. 1312–1322.

Akagi, H. and Matsumura, I. (2011), "Overvoltage mitigation of inverter-driven motors with long cables of different lengths," *IEEE Transactions on Industry Applications*, vol. 47, no. 4, pp. 1741–1748.

Azar, R., Udrea, R., Ng., W.T., Dawson, F., Findlay, W., and Waind, P. (2008), "The current sharing optimization of paralleled IGBTs in a power module tile using a pspice frequency dependent impedance model," *IEEE Transactions on Power Electronics*, vol. 23, pp. 206–217.

Bidan, P., Lebey, T., Montseny, G., and Saint-Michel, J. (2001), "Transient voltage distribution in inverter fed motor windings: experimental study and modeling," *IEEE Transactions on Power Electronics*, vol. 16, no. 1, pp. 92–100.

Bonnett, A. (1996), "Analysis of the impact of pulse-width modulated inverter voltage waveforms on AC induction motors," *IEEE Transactions on Industry Applications*, vol. 32, no. 2, pp. 386–392.

Bortis, D., Biela, J., and Kolar, J. (2008), "Active gate control for current balancing of parallel-connected IGBT modules in solid-state modulators," *IEEE Transactions on Plasma Science*, vol. 36, pp. 2632–2637.

Bose, B. (2000), "Energy, environment, and advances in power electronics," *IEEE Transactions on Power Electronics*, vol. 15, no. 4, pp. 688–701.

Bose, B. (2009), "Power electronics and motor drives recent progress and perspective," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 581–588.

Cai, H., Zhao, R., and Yang, H. (2008), "Study on ideal operation status of parallel inverters," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2964–2969.

Cavallini, A., Fabiani, D., and Montanari, G. (2010), "Power electronics and electrical insulation systems - part 1: Phenomenology overview," *IEEE Electrical Insulation Magazine*, vol. 26, no. 3, pp. 7–15.

Chen, C. and Xu, X. (1998), "Loss-less and cost-effective cable terminator topologies with no voltage overshoot," in *Proceedings of the Thirteenth Annual Applied Power Electronics Conference and Exposition, 1998. APEC '98.*, vol. 2, pp. 1030–1034 vol.2.

Cougo, B., Meynard, T., and Gateau, G. (2011), "Parallel three-phase inverters: Optimal PWM method for flux reduction in intercell transformers," *IEEE Transactions on Power Electronics*, vol. 26, no. 8, pp. 2184–2191.

Deisenroth, H. and Trabert, C. (1993), "Vermeidung von Überspannungen bei Pulsumrichterantrieben," *ETZ*, vol. 114, no. 17, pp. 1060–1067.

Di Piazza, M., Ragusa, A., and Vitale, G. (2009), "Design of grid-side electromagnetic interference filters in AC motor drives with motor-side common mode active compensation," *IEEE Transactions on Electromagnetic Compatibility*, vol. 51, no. 3, pp. 673–682.

Endrejat, F. and Pillay, P. (2009), "Resonance overvoltages in medium-voltage multilevel drive systems," *IEEE Transactions on Industry Applications*, vol. 45, no. 4, pp. 1199–1209.

Finlayson, P. (1998), "Output filters for PWM drives with induction motors," *IEEE Industry Applications Magazine*, vol. 4, pp. 46–52.

Franquelo, L., Rodriguez, J., Leon, J., Kouro, S., Portillo, R., and Prats, M. (2008), "The age of multilevel converters arrives," *IEEE Industrial Electronics Magazine*, vol. 2, Issue 2, pp. 28–39.

Glinka, M. and Marquardt, R. (2005), "A new AC/AC multilevel converter family," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 662–669.

Habetler, T., Naik, R., and Nondahl, T. (2002), "Design and implementation of an inverter output LC filter used for DV/DT reduction," *IEEE Transactions on Power Electronics*, vol. 17, no. 3, pp. 327–331.

Hanigovszki, N., Poulsen, J., and Blaabjerg, F. (2004), "A novel output filter topology to reduce motor overvoltage," *IEEE Transactions on Industry Applications*, vol. 40, no. 3, pp. 845–852.

Heaviside, O. (1893), *Electromagnetic Theory, Volume I*, Cosimo Classics, 2007, New York, USA, ISBN 978-1-60206-271-9.

Heaviside, O. (1899), *Electromagnetic Theory, Volume II*, Cosimo Classics, 2007, New York, USA, ISBN 978-1-60206-276-4.

Idir, N., Bausiere, R., and Franchaud, J. (2006), "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," *IEEE Transactions on Power Electronics*, vol. 21, no. 4, pp. 849–855.

IEC (2007), *IEC 60034-25:2007(E) Rotating electrical machines — Part 25: Guidance for the design and performance of a.c. motors specifically designed for converter supply*, International electrotechnical commission, Geneva, Switzerland, 2.0 edn.

IEC (2008), *IEC 61000-3-6, Electromagnetic compatibility (EMC) - Part 3-6: Limits - Assessment of emission limits for the connection of distorting installations to MV, HV and EHV power systems*, International electrotechnical commission, Geneva, Switzerland, 2.0 edn.

IEC (2011), *IEC 61000-3-12, Electromagnetic compatibility (EMC) - Part 3-12: Limits - Limits for harmonic currents produced by equipment connected to public low-voltage systems with input current >16 A and < 75 A per phase*, International electrotechnical commission, Geneva, Switzerland, 2.0 edn.

IEEE (1993), "IEEE recommended practices and requirements for harmonic control in electrical power systems," *IEEE Std 519-1992*.

von Jouanne, A., Rendusara, D., Enjeti, P., and Gray, J. (1996), "Filtering techniques to minimize the effect of long motor leads on PWM inverter-fed AC motor drive systems," *IEEE Transactions on Industry Applications*, vol. 32, no. 4, pp. 919–926.

von Jouanne, A. and Enjeti, P. (1997), "Design considerations for an inverter output filter to mitigate the effects of long motor leads in ASD applications," *IEEE Transactions on Industry Applications*, vol. 33, no. 5, pp. 1138–1145.

Kagerbauer, J. and Jahns, T. (2007), "Development of an active dv/dt control algorithm for reducing inverter conducted EMI with minimal impact on switching losses," in *Proceedings of the IEEE Power Electronics Specialists Conference, 2007. PESC 2007*, pp. 894–900.

Kawabata, T. and Higashino, S. (1988), "Parallel operation of voltage source inverters," *IEEE Transactions on Industry Applications*, vol. 24, no. 2, pp. 281–287.

Kedarisetti, J. and Mutschler, P. (2012), "A motor-friendly quasi-resonant DC-link inverter with lossless variable zero-voltage duration," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2613–2622.

Kerkman, R.J., Leggate, D., and Skibinski, G.L. (1997), "Interaction of drive modulation and cable parameter on AC motor transients," *IEEE Transactions on Industry Applications*, vol. 33, pp. 722–731.

Korhonen, J., Itkonen, T., Ström, J.P., Tyster, J., and Silventoinen, P. (2010), "Active motor terminal overvoltage mitigation method for parallel two-level voltage source inverters," in *Proceedings of the IEEE Energy Conversion Congress and Exposition, ECCE 2010*, pp. 757–763.

Korhonen, J., Laakkonen, T., Itkonen, T., Tyster, J., Ström, J.P., and Silventoinen, P. (2011), "Motor terminal overvoltage suppression method for parallel inverters," in *Proceedings of the 14th European Conference on Power Electronics and Applications, EPE 2011*, pp. 1–8.

Kosonen, A. (2008), *Power Line Communication in Motor Cables of Variable-Speed Electric Drives*, Doctoral thesis, Acta Universitatis Lappeenrantaensis 320, Lappeenranta University of Technology.

Lee, K. and Yao, W. (2011), "Quantitative system compatibility and characteristics analysis of two-level and three-level low voltage industrial drives," in *Proceedings of the IEEE Energy Conversion Congress and Exposition, ECCE 2011*, pp. 3442–3449.

Lee, S. and Nam, K. (2002), "An overvoltage suppression scheme for AC motor drives using a half DC-link voltage level at each PWM transition," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 549–557.

Link, P. (1999), "Minimizing electric bearing currents in ASD systems," *IEEE Industry Applications Magazine*, vol. 5, pp. 55–66.

Liserre, M., Blaabjerg, F., and Hansen, S. (2005), "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1281–1291.

Malinowski, M., Gopakumar, K., Rodriguez, J., and Perez, M. (2010), "A survey on cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2197–2206.

McGrath, B. and Holmes, D. (2002), "Multicarrier PWM strategies for multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 858–867.

Melfi, M., Sung, A., Bell, S., and Skibinski, G. (1998), "Effect of surge voltage risetime on the insulation of low-voltage machines fed by PWM converters," *IEEE Transactions on Industry Applications*, vol. 34, no. 4, pp. 766–775.

Melfi, M. (2006), "Low-voltage PWM inverter-fed motor insulation issues," *IEEE Transactions on Industry Applications*, vol. 42, no. 1, pp. 128–133.

Miettinen, E. (2011), "Method and arrangement in connection with inverter," U.S. Patent 7,924,583 B2, Apr 12, 2011.

Mirafzal, B., Skibinski, G., Tallam, R., Schlegel, D., and Lukaszewski, R. (2007), "Universal induction motor model with low-to-high frequency-response characteristics," *IEEE Transactions on Industry Applications*, vol. 43, no. 5, pp. 1233–1246.

Mirafzal, B., Skibinski, G., and Tallam, R. (2009), "A failure mode for PWM inverter-fed AC motors due to the antiresonance phenomenon," *IEEE Transactions on Industry Applications*, vol. 45, no. 5, pp. 1697–1705.

Mohan, N., Undeland, T., and Robbins, W. (2003), *Power Electronics, Converters, Application and Design, 3rd edition*, John Wiley & Sons Inc., Hoboken, NJ, USA.

Moreira, A., Lipo, T., Venkataramanan, G., and Bernet, S. (2002), "High-frequency modeling for cable and induction motor overvoltage studies in long cable drives," *IEEE Transactions on Industry Applications*, vol. 38, no. 5, pp. 1297–1306.

Moreira, A., Santos, P., Lipo, T., and Venkataramanan, G. (2005), "Filter networks for long cable drives and their influence on motor voltage distribution and common-mode currents," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 2, pp. 515–522.

Nabae, A., Takahashi, I., and Akagi, H. (1981), "A new neutral-point-clamped PWM inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, pp. 518–523.

Naumanen, V. (2010), *Multilevel converter modulation: implementation and analysis*, Doctoral thesis, Acta Universitatis Lappeenrantaensis 386, Lappeenranta University of Technology.

Naumanen, V., Korhonen, J., Luukko, J., and Silventoinen, P. (2010), "Multilevel inverter modulation method to reduce common-mode voltage and overvoltage at the motor terminals," in *Proceedings of the 26th IEEE Convention of Electrical and Electronics Engineers in Israel, IEEEI 2010*.

Nyquist, H. (1928), "Certain topics in telegraph transmission theory," *Transactions of the American Institute of Electrical Engineers*, vol. 47, no. 2, pp. 617–644.

Peng, F.Z. (2003), "Z-source inverter," *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 504–510.

Persson, E. (1992), "Transient effects in application of PWM inverters to induction motors," *IEEE Transactions on Industry Applications*, vol. 28, pp. 1095–1101.

Rendusara, D. and Enjeti, P. (1997), "New inverter output filter configuration reduces common mode and differential mode dv/dt at the motor terminals in PWM drive systems," in *Proceedings of the 28th Annual IEEE Power Electronics Specialists Conference, 1997. PESC '97*, vol. 2, pp. 1269–1275.

Rodriguez, J., Pontt, J., Silva, C., Musalem, R., Newman, P., Vargas, R., and Fuentes, S. (2006), "Resonances and overvoltages in a medium-voltage fan motor drive with long cables in an underground mine," *IEEE Transactions on Industry Applications*, vol. 42, no. 3, pp. 856–863.

Saunders, L., Skibinski, G., Evon, S., and Kempkes, D. (1996), "Riding the reflected wave-IGBT drive technology demands new motor and cable considerations," in *Proceedings of The Institute of Electrical and Electronics Engineers Incorporated Industry Applications Society 43rd Annual Petroleum and Chemical Industry Conference, 1996*, pp. 75–84.

Shimizu, T., Saito, M., Nakamura, M., and Miyazaki, T. (2012), "A motor surge voltage suppression method with surge energy regeneration," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3434–3443.

Skibinski, G. (1996), "Design methodology of a cable terminator to reduce reflected voltage on AC motors," in *Proceedings of the Thirty-First IEEE IAS Annual Meeting Industry Applications Conference, IAS '96*, vol. 1, pp. 153–161 vol.1.

Skibinski, G., Leggate, D., and Kerkman, R. (1997), "Cable characteristics and their influence on motor over-voltages," in *Proceedings of the Twelfth Annual Applied Power Electronics Conference and Exposition, APEC '97*.

Skibinski, G., Kerkman, R., and Schlegel, D. (1999), "EMI emissions of modern PWM AC drives," *IEEE Industry Applications Magazine*, vol. 5, no. 6, pp. 47–80.

Steinke, J. (1999), "Use of an LC filter to achieve a motor-friendly performance of the PWM voltage source inverter," *IEEE Transactions on Energy Conversion*, vol. 14, no. 3, pp. 649–654.

Stranges, M., Stone, G., and Bogh, D. (2007), "New specs for ASD motors," *IEEE Industry Applications Magazine*, vol. 13, no. 1, pp. 37–42.

Ström, J.P. (2009), *Active du/dt filtering for variable-speed AC drives*, Doctoral thesis, Acta Universitatis Lappeenrantaensis 378, Lappeenranta University of Technology.

Ström, J.P., Tyster, J., Korhonen, J., Rauma, K., Sarén, H., and Silventoinen, P. (2009), "Active d*u*/d*t* filtering for variable speed AC drives," in *Proceedings of the 13th International European Power Electronics Conference and Exhibition, EPE 2009*.

Ström, J.P., Tyster, J., Korhonen, J., Purhonen, M., and Silventoinen, P. (2011), "Active d*u*/d*t* filter dimensioning in variable speed AC drives," in *Proceedings of the 14th European Conference on Power Electronics and Applications, EPE 2011*, pp. 1–7.

Takahashi, I. and Noguchi, T. (1986), "A new quick-response and high-efficiency control strategy of an induction motor," *IEEE Transactions on Industry Applications*, vol. IA-22, no. 5, pp. 820–827.

Tallam, R., Kerkman, R., Leggate, D., and Lukaszewski, R. (2010), "Common-mode voltage reduction PWM algorithm for AC drives," *IEEE Transactions on Industry Applications*, vol. 46, no. 5, pp. 1959–1969.

Tallam, R., Skibinski, G., Shudarek, T., and Lukaszewski, R. (2011), "Integrated differential-mode and common-mode filter to mitigate the effects of long motor leads on AC drives," *IEEE Transactions on Industry Applications*, vol. 47, no. 5, pp. 2075–2083.

Teichmann, R. and Bernet, S. (2005), "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," *IEEE Transactions on Industry Applications*, vol. 41, pp. 855–865.

Tyster, J., Ström, J.P., Korhonen, J., and Silventoinen, P. (2011), "Efficiency measurements on active d*u*/d*t* output filtering," in *Proceedings of the 14th European Conference on Power Electronics and Applications, EPE 2011*, pp. 1–8.

Wang, L., Ho, C.M., Canales, F., and Jatskevich, J. (2010), "High-frequency modeling of the long-cable-fed induction motor drive system using TLM approach for predicting overvoltage transients," *IEEE Transactions on Power Electronics*, vol. 25, no. 10, pp. 2653–2664.

Yuen, K.F. and Chung, H.H. (2010), "A low-loss motor terminal filter for overvoltage suppression," in *Proceedings of the IEEE Energy Conversion Congress and Exposition, ECCE 2010*, pp. 853–861.

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