Lappeenranta
University of Technology

Iiro Hietanen

DESIGN AND CHARACTERIZATION OF LARGE AREA POSITION SENSITIVE RADIATION DETECTORS

Thesis for the degree of Doctor of Science (Technology) to be presented with due permission for public examination and criticism in the Auditorium 1382 at Lappeenranta University of Technology, Lappeenranta, Finland on the 23rd of November, 2012, at noon.

Acta Universitatis
Lappeenrantaensis 491

Supervisor	Professor Tuure Tuuva Department of Mathematics and Physics Lappeenranta University of Technology Finland
Reviewers	Professor Harri Lipsanen Department of Micro- and Nanosciences Aalto University Finland
	Doctor of Science (Technology) Eija Tuominen Helsinki Institute of Physics (HIP) University of Helsinki Finland
Opponent	Professor Harri Lipsanen Department of Micro- and Nanosciences Aalto University Finland

ISBN 978-952-265-318-5
ISBN 978-952-265-319-2 (PDF)
ISSN 1456-4491
Lappeenrannan teknillinen yliopisto
Yliopistopaino 2012

Abstract

Iro Hietanen

Design and characterization of large area position sensitive radiation detectors

Lappeenranta 2012
63 pages
Acta Universitatis Lappeenrantaensis 491
Diss. Lappeenranta University of Technology 2012
ISBN 978-952-265-318-5, ISBN 978-952-265-319-2 (PDF), ISSN 1456-4491

Planar, large area, position sensitive silicon detectors are widely utilized in high energy physics research and in medical, computed tomography (CT). This thesis describes author's research work relating to development of such detector components. The key motivation and objective for the research work has been the development of novel, position sensitive detectors improving the performance of the instruments they are intended for.

Silicon strip detectors are the key components of barrel-shaped tracking instruments which are typically the innermost structures of high energy physics experimental stations. Particle colliders such as the former LEP collider or present LHC produce particle collisions and the silicon strip detector based trackers locate the trajectories of particles emanating from such collisions.

Medical CT has become a regular part of everyday medical care in all developed countries. CT scanning enables x-ray imaging of all parts of the human body with an outstanding structural resolution and contrast. Brain, chest and abdomen slice images with a resolution of 0.5 mm are possible and latest CT machines are able to image whole human heart between heart beats.

The two application areas are presented shortly and the radiation detection properties of planar silicon detectors are discussed. Fabrication methods and preamplifier electronics of the planar detectors are presented.

Designs of the developed, large area silicon detectors are presented and measurement results of the key operating parameters are discussed.

Static and dynamic performance of the developed silicon strip detectors are shown to be very satisfactory for experimental physics applications. Results relating to the developed, novel CT detector chips are found to be very promising for further development and all key performance goals are met.

Keywords: strip detector, computed tomography detector, silicon detector

UDC: 539.1.074 : 53.084 : 577.3

Acknowledgements

The strip detector research work described in this thesis was carried out in the former Research Institute for High Energy Physics (SEFT) at University of Helsinki. A substantial part of the work was carried out during the time I spent at CERN, in Geneva area. Still after many years I want to thank my closest colleagues there, Tuure Tuuva, Jukka Lindgren and Richard Brenner both for the working hours and leisure time we spent together.

In also want to thank again Prof. Tuure Tuuva for another intensive period as my supervisor of this thesis at Lappeenranta University of Technology. Without his simultaneous encouragement and intensive goal setting help I would never have completed this work.

Detection Technology Inc. was my employer for many years and from that period I owe a lot to many great professionals. Here I want to thank especially those persons who worked with me closely in the area of computed tomography (CT) detectors, Wang Yong, Ji Fan, Wu Xiaopeng, Mikko Juntunen, Sami Juottonen and Jyri Tolonen.

Iiro Hietanen
November 2012
Lappeenranta, Finland

Contents

Abstract

Acknowledgements

Contents

List of publications 9

Author's contribution 10

Abbreviations and symbols 11

1 Introduction 13

1.1 Applications of large area position sensitive silicon detectors 13

1.1.1 Large area silicon detectors in high energy physics 15

1.1.2 Large area silicon detectors in computed tomography (CT) 20

1.2 Planar silicon pn-junctions as radiation detectors and photodiodes 29

1.2.1 Principal properties of pn-junctions 29

1.2.2 Radiation detection and photodiode properties of pn-junctions..33

1.3 Fabrication of planar silicon detectors and photodiodes 37

1.4 Planar silicon detector readout 42

2 Silicon strip detectors for high energy physics research 47

2.1 Single sided DC coupled strip detectors..47

2.2 Single sided AC coupled strip detectors..49

2.3 Double sided strip detectors 51

3 Silicon photodiode detectors for CT applications 55

4 Conclusions 59

References 61

Publications

List of publications

This thesis is based on the following publications.

I. Iiro Hietanen, Jukka Lindgren, Risto Orava, Tuure Tuuva, Richard Brenner, Mikael Andersson, Kari Leinonen, Hannu Ronkainen, Ion-implanted silicon detectors processed on a 100 mm wafer. *Nuclear Instruments and Methods in Physics Research,* A301 (1991) 116-120.

II. Iiro Hietanen, Jukka Lindgren, Risto Orava, Tuure Tuuva, Martti Voutilainen, Richard Brenner, Mikael Andersson, Kari Leinonen, Hannu Ronkainen, Ion-implanted capacitively coupled silicon strip detectors with integrated polysilicon bias resistors processed on a 100 mm wafer. *Nuclear Instruments and Methods in Physics Research,* A310 (1991) 671-676.

III. I. Hietanen, J. Lindgren, R. Orava, T. Tuuva, R. Brenner, M. Andersson, K. Leinonen, H. Ronkainen, M. Turala, P. Weilhammer, W. Dulinski, D. Husson, A. Lounis, M. Schaeffer, R. Turchetta, J. Chauveau, Beam test results of an ion-implanted capacitively coupled silicon strip detector processed on a 100 mm silicon wafer. *Nuclear Instruments and Methods in Physics Research,* A310 (1991) 677-680.

IV. R. Brenner, I. Hietanen, J. Lindgren, R. Orava, C. Rönnqvist, T. Schulman, T. Tuuva, M. Voutilainen, M. Andersson, K. Leinonen, H. Ronkainen, Double-sided capacitively coupled silicon strip detectors on a 100mm wafer. *Nuclear Instruments and Methods in Physics Research,* A315 (1992) 502-506.

V. Gy.L. Bencze, C. Seez, M. Aalste, J. Berg, A. Hentinen, I. Hietanen, V. Karimäki, J. Lindgren, M. Pimiä, T. Tuuva, M. Voutilainen, F. Szoncso, G. Walzel, C.-E. Wulz, C. Rönnqvist, K. Österberg, An accurate telescope for beam position monitoring and spatial resolution studies. *Nuclear Instruments and Methods in Physics Research,* A368 (1996) 283-287.

VI. Fan Ji, Seppo Leppävuori, Ismo Luusua, Kimmo Henttinen, Simo Eränen, Iiro Hietanen, Mikko Juntunen, Fabrication of silicon based through-wafer interconnects for advanced chip scale packaging. *Sensors and Actuators A,* 142 (2008) 405-412

VII. Mikko Juntunen, Fan Ji, Kimmo Henttinen, Ismo Luusua, Iiro Hietanen, Simo Eränen, Fully tileable photodiode matrix for medical imaging by using through-wafer interconnects. *Nuclear Instruments and Methods in Physics Research,* A580 (2007) 1000-1003.

Author's contribution

Author is the principal author, chief detector designer and investigator in publication I. Author conducted most of the experiments presented and prepared most of the manuscript including the graphics presented.

Author contributed to the detector design concerning publication II. Author has participated in the presented evaluations and experiments and has strongly contributed to the manuscript.

Beam test experiment presented in publication III was implemented by a research team where author contributed to the preparation of the test samples, and actual running, control and improvement of the experimental setup during the tests.

Author is the corresponding author, chief detector designer and investigator in publication IV. Author conducted most of the experiments presented and prepared the manuscript including the graphics presented.

Publication V describes a telescope instrument similar to the one utilized in the experiment described in publication III. Author contributed to the construction, testing and development of the telescope.

Author co-initiated the research of publications VI and VII relating to through-wafer interconnect (TWI) development for CT applications. Author participated in the early stage design of TWI and detector prototypes utilizing accumulated experience of earlier CT detector designs.

Abbreviations and symbols

3D	Three dimensional
AC	Alternating Current
AD	Analogue-to-Digital
CERN	Conseil européen pour la recherche nucléaire
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical Mechanical Polishing
CMS	Compact Muon Solenoid
CT	Computed Tomography
CVD	Chemical Vapour Deposition
DAS	Data Acquisition System
DC	Direct Current
DCS	Double Correlated Sampling
DELPHI	Detector with Lepton, Photon and Hadron Identification
FOX	Field Oxide
GOS	Gadolinium Oxysulfide
GPS	Global Positioning System
IC	Integrated Circuit
LEP	Large Electron Positron collider
LHC	Large Hadron Collider
LTO	Low Temperature Oxide
MIP	Minimum Ionizing Particle
MOS	Metal-Oxide-Semiconductor
MRI	Magnetic Resonance Imaging
PCB	Printed Circuit Board
SPS	Super Proton Synchrotron
TWI	Through-Wafer Interconnect

C_{int}	Integrating capacitance
Δx	Sample thickness
E	Electric field
E_i	Intrinsic Fermi level
ε_s	Permittivity of silicon
ϕ	Electric potential
ϕ_i	Internal, built-in potential of the pn-junction
ϕ_n	Fermi level deviation from the intrinsic Fermi level E_i in the n region
ϕ_p	Fermi level deviation from the intrinsic Fermi level E_i in the p region
I	Transmitted intensity
I_o	Initial intensity
J_g	Generation current density
k	Boltzmann´s constant
L	Total material thickness
μ	Attenuation coefficient
μ_N	Attenuation coefficient of material N
N_a	Acceptor density
N_d	Donor density
n_i	Charge carrier density in intrinsic, non-doped silicon
q	Absolute value of the electron charge
Q	Signal charge
ρ	Space-charge density
T	Absolute temperature
τ_0	Lifetime of minority charge carrier
V_o	Amplifier output voltage
V_R	Reverse bias voltage
x_n	Width of the n-side depletion region
x_p	Width of the p-side depletion region

1 Introduction

This thesis describes the long term research work carried out by the author in the field of planar, large area, position sensitive, silicon radiation detectors.

The introductory first chapter presents the applications, theory, manufacturing methods and readout systems of such large area detectors. The second chapter of the thesis concentrates on the evolution of large area silicon strip detectors, widely utilized in high energy physics research. Results of the author's research work relating to strip detectors are also presented in chapter two. Another application area of large area silicon radiation detectors, computed tomography (CT) is the subject of chapter three. Results relating to CT detectors complete chapter three and the research work presentation. Conclusions relating to author's thesis research are finally given in chapter four.

1.1 Applications of large area position sensitive silicon detectors

Since the innovative semiconductor research conducted by John Bardeen and Walter Brattain in 1947, and the following invention of the bipolar transistor, silicon transistors have become an important part of our everyday life. Operation of all of our everyday electronics gadgets is based on transistor technology, currently applied in manufacturing of all key components within computers, mobile phones, GPS devices and a wide variety of engineering products.

The manufacturing technology of the present era microchips or silicon chips is still rapidly developing in terms of transistor density, but for the past 30 years nearly all silicon-based electronics have been manufactured utilizing the so-called planar manufacturing technology. In planar manufacturing technology, circular silicon slices known as wafers, are chemically treated to change the semiconducting properties of the silicon material and to add electrical contacts, conductors, capacitors, resistors or other components on the surface of the silicon wafer. Some of such manufacturing steps will be presented in chapter 1.5.

A much less noted application field of planar processed silicon chips is found in light and radiation detection. First planar process developments towards such sensor chips were reported in 1980s [1, 2]. What makes silicon an outstanding material for transistor construction also provides an excellent basis for light or radiation detector manufacturing.

Some of these unique features are

- Stable, solid state material with reasonably good mechanical rigidity
- Ultimate chemical purity and highly controlled impurity doping achievable with present chemical material processing methods

- Material with a stable, high quality oxide (SiO_2) operating as the primary electrical insulator in all planar processed chips
- Mature manufacturing technology developed and maintained by the high volume electronics industry
- Compatibility with all modern electronics due to common technology background
- Low noise performance in many applications

As presented below, the author has had a unique opportunity in working in two quite different application areas of the large area, position sensitive silicon detectors. In spite of the many aspects that are very different in the two application areas presented, it has also been very inspiring to note that they share so many common challenges, performance characteristics and especially manufacturing aspects.

The key characteristics which make the discussed detector chips quite different from the more or less standard size integrated circuits (ICs) utilized in our everyday electronics products, are following:

- Detector chips are very large, often 25 mm x 50 mm or 20 mm x 80 mm or even 100 mm x 100 mm compared to largest ICs of 25 mm x 25 mm
- Detector manufacturing requires ultimate cleanliness and often high or medium resistivity silicon wafer material compared to the lower resistivities applied in IC industry
- Yield requirements are stringent since only a few chips can be placed on one silicon wafer
- Detector structures are inherently much simpler than in IC circuits
- Detector chips cannot be encapsulated like ICs but still need to survive exposure to the conditions and handling encountered in the application environments

The fact that the detector chips are physically very large has by far the largest effect on manufacturing requirements. All standard IC manufacturing equipment is designed for standard IC dimensions and special arrangements are required even for the very basic manufacturing processes. Similarly, all manufacturing steps relating to post processing of the silicon wafers, like wafer dicing (cutting into chips), chip die bonding (chip attachment on a carrier substrate), wire or flip chip bonding (manufacturing of interconnections from detector chips to electronics) must be performed on specialized or even purpose built equipment.

Automated testing of detector chips, while they are still on the wafer, cannot be performed with standard IC testing equipment but typically again require dedicated tester development.

In both of the application areas discussed, the key motivation and goal for the research has been the development of new types of large area, position sensitive detectors improving the performance of the instruments they are intended for.

1.1.1 Large area silicon detectors in high energy physics

In the large scale high energy physics research centres (e.g. CERN, Conseil européen pour la recherche nucléaire [3]), large and massive particle colliders are built to find proof of new elementary particles or in order to increase our physics understanding of all that exists around us. Such heavy-duty experiments, e.g. earlier DELPHI (Detector with Lepton, Photon and Hadron Identification [4]) experiment at the LEP (Large Electron Positron collider [5]) collider or present CMS (Compact Muon Solenoid [6]) detector at the LHC (Large Hadron Collider [7]), both at CERN, are constructed from nested layers of various radiation detectors. Each detector layer is serving a different purpose in the ultimate goal of recording phenomena possibly never seen before.

Typically, the innermost detector layer is placed as close to the particle collision origin as possible. This detector should record as precisely as possible the trajectories of the particles emitted at or near the vertex of the experiment.

The obvious choice of detector medium for these vertex detectors is silicon due to the possibility of placing thin but yet highly sensitive detectors layers close to the origin of the experiment and simultaneously achieving high precision for the tracking capability of the detector. The structures of the DELPHI experiment and its vertex detector Microvertex [8] are presented in figures 1.1 and 1.2.

The operation of the large area silicon detector chips, intended for high energy physics tracking purposes, is based on integrating a large number of radiation sensitive elements on the surface of the silicon detector chip, and then further recording signals in those elements which are traversed by particles. The detector chip active area may be divided into square pixel elements, in which case the physical location of the pixel would identify the coordinate point of particle trajectory. However, due to complexity of readout of signals from a large number of small pixels manufactured on the surface of the silicon chip, the sensitive area is more commonly divided into active element strips, hence the term strip detector.

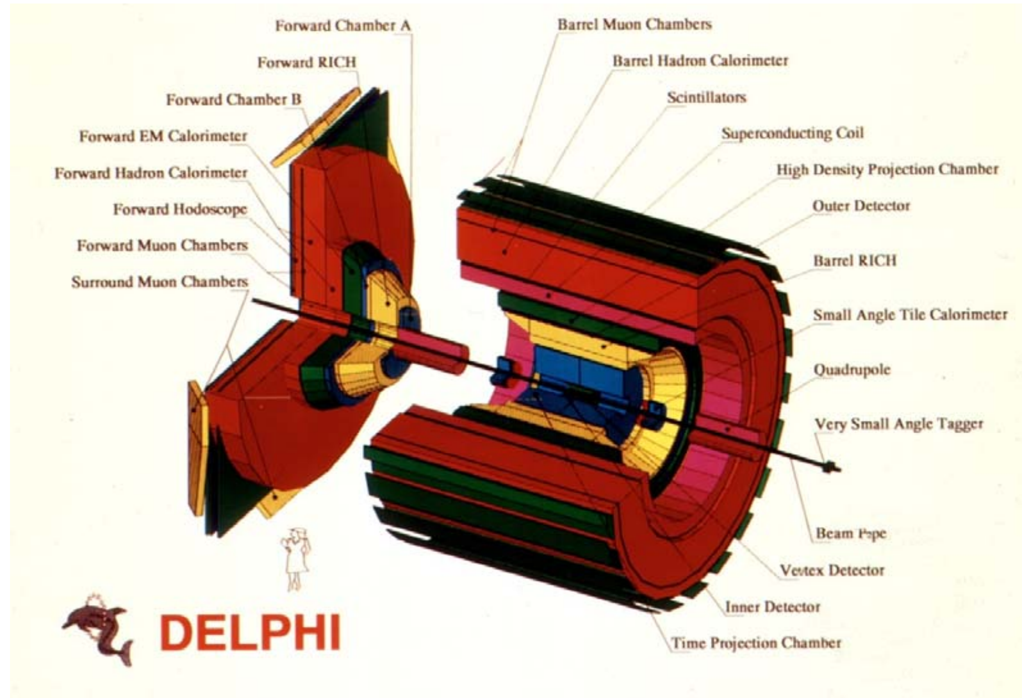

Figure 1.1: DELPHI experiment, note the drafted person for scale. Drawing and copyright by CERN [9].

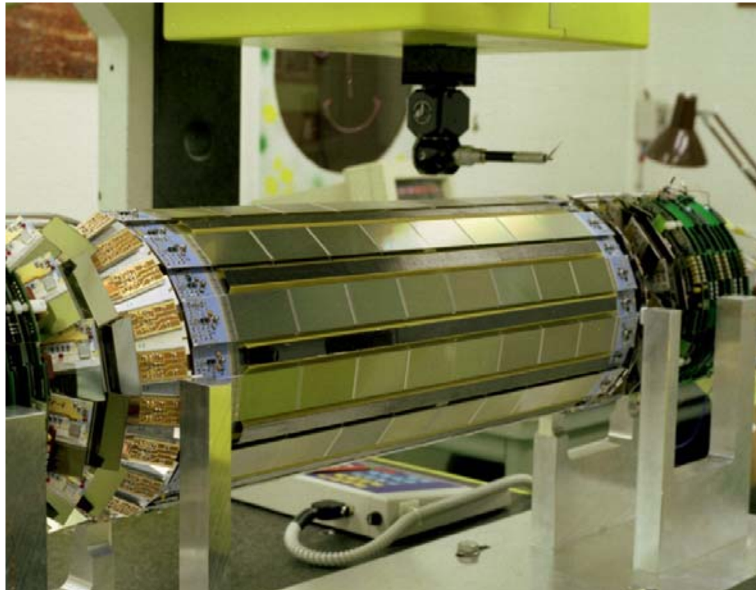

Figure 1.2: Upgraded Microvertex detector of the DELPHI experiment, each outer module carries 8 strip detectors of 30 mm x 60 mm size each. Photo and copyright by CERN [10].

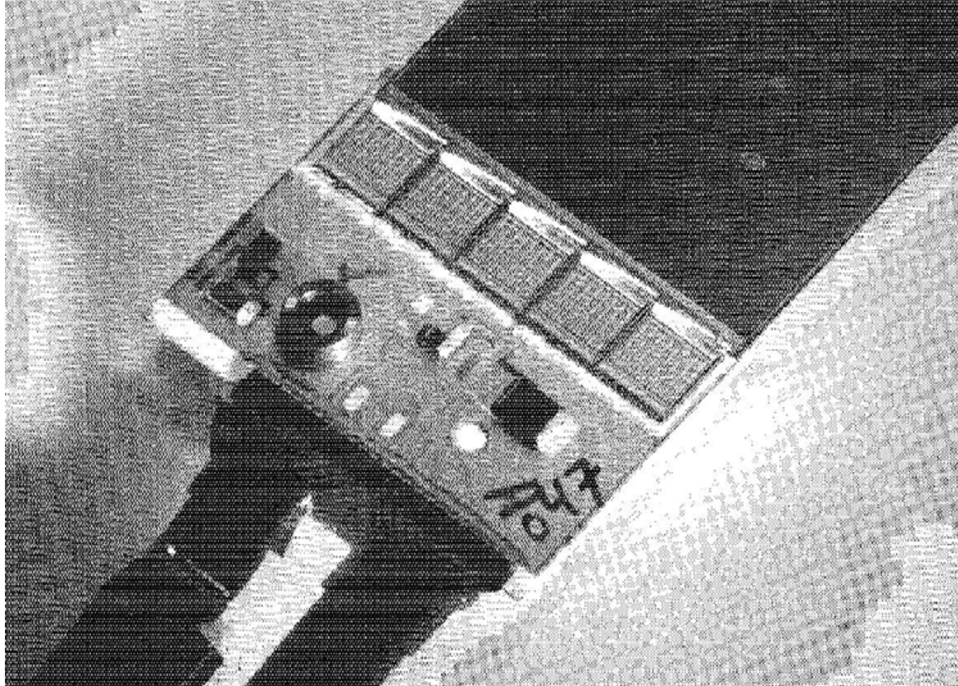

Figure 1.3: A silicon strip detector chip designed for the DELPHI experiment [8].

A strip detector chip (see figure 1.3) consists of a large number of strip shaped electrical electrodes which will record signals whenever a particle traverses the detector chip at any position on or near the strip structure. Since the whole active area of the chip is divided into strips and not into pixels, it is adequate to contact the active elements only at one edge of chip. However, the important and major drawback of such strip electrode structure is that particle position is in most designs recorded only in one dimension.

High energy physics experiments, like DELPHI or CMS, typically have a cylindrical barrel structure and the axis of the coaxial detector coincides with the track of the colliding elementary particles. The vertex detectors also exhibit a cylindrical structure where the strip shaped electrodes of each detector chip are parallel to the axis of the cylinder.

In order to improve the precision of tracking in vertex type silicon detectors, high energy physics experiments typically utilize several layers of silicon detector chips (3 or more) although a minimum of two layers is required to record a particle trajectory. Increasing the number of layers also increases redundancy and noise tolerance of the system. By requiring simultaneous signal in 3 layers on same trajectory, any false signals may be more easily rejected.

The strip shaped electrodes on the surface of the strip detector chip are typically manufactured with a spacing of 25-100 μm. However, the inherent precision of particle

tracking or position resolution of the detector chip is far better than this strip centre-to-centre spacing, also known as strip pitch. This is due to the fact that the signal generated by a traversing particle is shared between several neighbouring strips and by calculating the mathematical centre position of the track, the position resolution may be as low as only one fifth of the strip pitch. In a most simplified method, this could be accomplished by calculating the position of the track by centre-of-mass method meaning that the ratio of signals between two neighbouring strips would be directly used as the indication of track position between such strips. In real life high energy physics experiments the imperfections of the strip detectors may be corrected by measuring and applying more precise functions to the correlation between signal distribution and depicted particle track position.

Full scale utilization of the tracking capabilities of silicon strip detectors sets high demands on the mechanics and readout system of a vertex detector. It is obvious that the very high, typically better than 10 μm tracking precision at the silicon strip detector location, is easily wasted unless the mechanical structure supporting the detector chips is built into an equal level of precision. Construction of a successful vertex detector is as much a mechanical challenge as it is a semiconductor engineering task. A tight spaced particle detector experiment is a demanding assembly location also from many other points of view. Space is at premium, heavy materials cannot be used due to disturbance caused to the particles intended to be detected, large number of detector channels and readout channels requires efficient cooling and radiation levels are reasonably high, to name a few of the challenges to be solved.

In order to understand the scale of signal interfacing required in a high energy physics vertex detector, we can shortly review the two exemplary detector designs already mentioned above. DELPHI Microvertex detector consisted of 288 strip detector chips in total and the number of readout channels was 73728. The present CMS detector has a greatly expanded tracker detector [11] with a massive number of 15 148 strip detector modules installed and these detectors produce data into more than 10 million readout channels.

It is more that obvious that such scales of readout and data handling can only be produced by applying integrated electronics, efficient multiplexing and data reduction as close to the strip detector chips as possible. Even the mere cabling of operating voltages, control signals and actual detector signals is a tremendous challenge when data from such a number of readout channels must be transmitted outside the experiment barrel.

The integrated amplifier electronics utilized in experiments like the ones discussed, must operate at a reasonable total power not to cause problems relating to self-heating of the detector system.

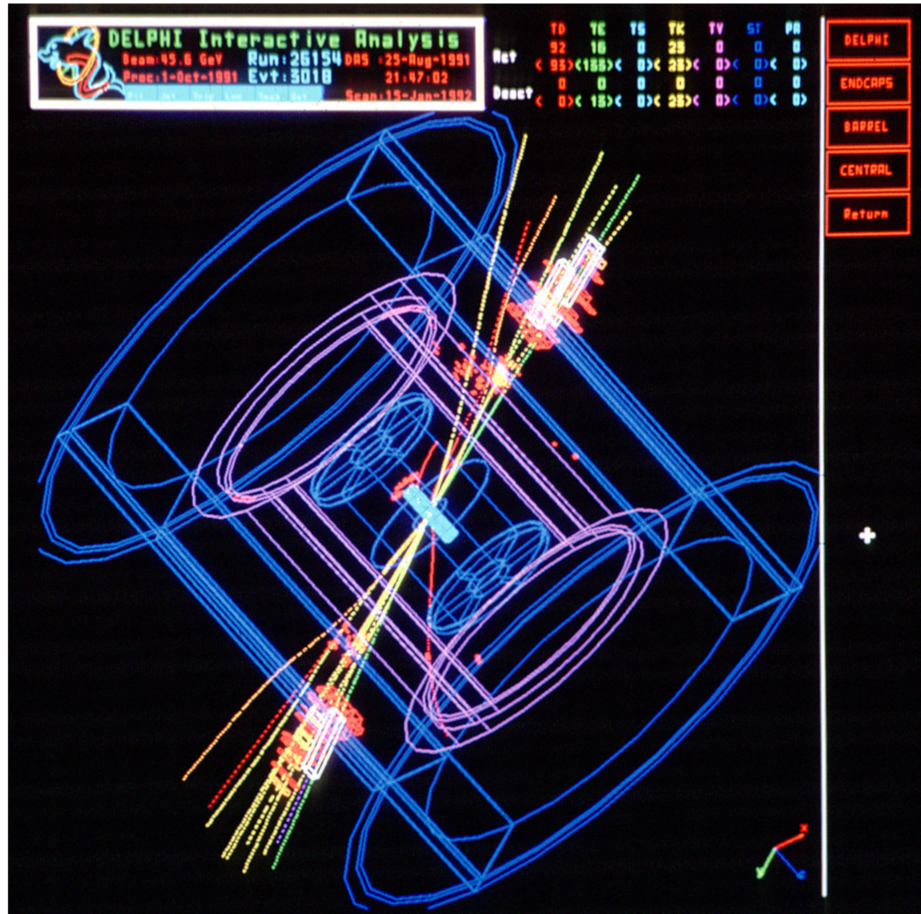

Figure 1.4: DELPHI experiment visualization of a Z0 particle produced in a collision between an electron and positron at the LEP collider. Z0 decays into a quark-antiquark pair which is seen as a pair of hadron jets in the DELPHI detector. Photo and copyright by CERN [12].

Real, visualized data from an electron-positron collision in the DEPLHI experiment is presented in figure 1.4. The experimental station is shown only as a wireframe image of the main, barrel-shaped DELHI structures to clarify the presentation of the actual particle tracks recorded by the various detectors. Figure 1.4 represents a typical situation in high energy physics research where existence or behavior of a short-lived particle is proven by recording the secondary results of the initial particle collision. See text in figure 1.4 for details.

Fundamentals of silicon strip detector physics, manufacturing and readout are presented below in chapters 1.2, 1.3 and 1.4. Chapter 2 is devoted to presentation of design details and results relating to author's research work in the area of these detectors.

1.1.2 Large area silicon detectors in computed tomography (CT)

Computed tomography (CT) scan is a modern, specialized x-ray imaging procedure in which high precision cross-sectional images and further 3D images of the object may be reconstructed by utilizing computer processing of a large number of individual x-ray projection images taken from different angles in respect to the object. Medical x-ray imaging is by far the most common application of CT. Other application areas include non-destructive testing of material samples, typically metal products and various scientific uses.

Ideas and theory of CT scanning were initially developed into a working medical procedure by A.M. Cormack [13, 14] and G.N. Hounsfield and this resulted in them sharing the 1979 Nobel Prize in Medicine. It has been estimated that invention of CT has been the most important step in the development of medical x-ray imaging since the initial discovery of x-rays by Wilhelm Roentgen in 1895. In spite of a lot of research and many advanced innovations in conventional radiography, it was the CT technology which really took the performance of x-ray imaging to the present level where the whole anatomy of a human body can imaged at an amazing precision without the scalpel of a surgeon.

Despite occasional visions that MRI (Magnetic Resonance Imaging) techniques would replace CT imaging as the leading anatomic imaging procedure, number of CT scans and CT scanners has continued a steep growth over the past two decades. CT has become an integral part of routine healthcare and in year 2007, nearly 70 million CT examinations were performed only in United States [15]. Equal tendency has been seen in Europe.

The ingenious operating principle of the CT scanner is based on reconstruction mathematics first introduced by Johann Radon in 1917 [16] and later independently developed by A.M. Cormack in 1960s and 1970s. The basic theory behind the CT reconstruction methods states that a two-dimensional, mathematical function can be reconstructed from its line integrals. In the case of CT image reconstruction, the line integral values are obtained from the individual x-ray attenuation measurements, performed by exposing the object to x-rays in very many different angles and collecting attenuation data utilizing a detector with a large number of measurement channels.

A simplified presentation of the line integral function in the case of an x-ray CT scan is presented in the following.

Let us assume that we have a small sample of a uniform material, with a thickness of Δx, exposed to monocromatic x-rays, see figure 1.5. [17]. Lambert-Beer law states that

$$I = I_0 e^{-\mu \Delta x} \tag{1.1}$$

Where I_o is the x-ray intensity entering the sample, I is the transmitted intensity, μ is the linear attenuation coefficient of the material, and Δx is the sample thickness.

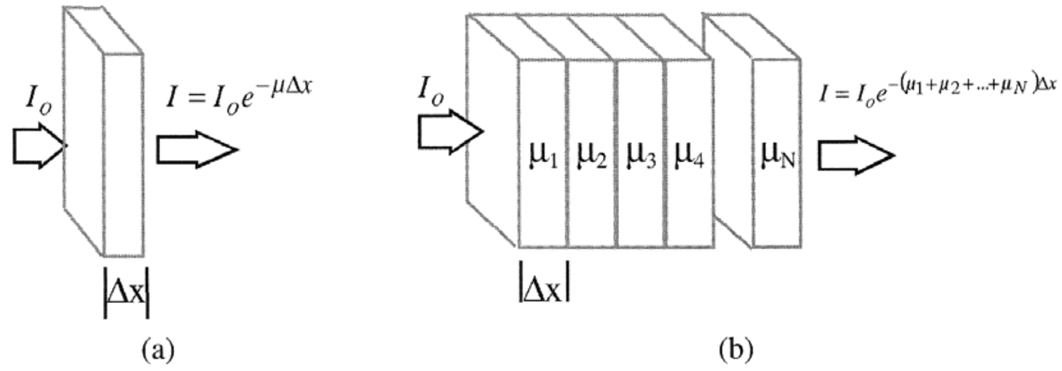

Figure 1.5: Illustration of x-ray attenuation in (a) a uniform material sample, and (b) a series of material samples of varying attenuation coefficients [17].

Let us now consider a multiple set of material samples, where each material exhibits a different attenuation coefficient μ_N and equal thickness Δx. Since the intensity exiting sample N-1 is equal to the intensity entering sample N, we can derive [17]

$$I = I_0 e^{-\mu_1 \Delta x}\ e^{-\mu_2 \Delta x} e^{-\mu_3 \Delta x} .....e^{-\mu_N \Delta x} = I_0 e^{-\sum_{n=1}^{N} \mu_n \Delta x} \tag{1.2}$$

After dividing both sides by I_o and taking a natural logarithm we obtain

$$-\ln\left(\frac{I}{I_0}\right) = \sum_{n=1}^{N} \mu_n \Delta x \tag{1.3}$$

By letting Δx to approach zero we further obtain

$$-\ln\left(\frac{I}{I_0}\right) = \int_L \mu(x) dx \tag{1.4}$$

where L is the total thickness of the object.

Equation 1.4 above states that the natural logarithm of the I/ I_o ratio, measured by one CT detector element in one single view angle, equals to the line integral of attenuation coefficient function along this narrow, collimated x-ray path. Recalling the statement that a two-dimensional mathematical function can be reconstructed from its line integrals, we conclude that the attenuation coefficient function or distribution of μ

within a two-dimensional object may be reconstructed if an adequate number of intensity ratios I/I_0 is measured in different directions. This is a crude oversimplification of the real life reconstruction mathematics but nevertheless describes the very basic principle they are based on.

It should be noted that even before mentioning anything about the actual reconstruction algorithms, we have made simplifying assumptions about the operation of a real CT scanner. The x-ray tube of a CT scanner produces a continuous spectrum of x-ray energies, and x-rays are not monochromatic. Scattering of x-ray photons from the x-ray instrument and object disturbs the attenuation distributions. X-ray detectors and readout electronics are not perfectly linear and their gain may drift and patient may move during the scanning procedure in medical CT. These are the main imperfections effecting real CT imaging quality and reliability.

The treatment of any actual reconstruction algorithms is beyond the scope of this concise CT detector introduction but a few important notes should be made. Following notes concern especially medical CT.

Reconstruction algorithms utilized in CT scanners vary depending on the exact medical imaging procedure and there is no one, exact reconstruction method that all CT scanner manufacturers would use in all CT scans. The mathematics behind the reconstruction algorithms is rather complicated and the details of such algorithms and related computer programs are well kept secrets amongst the CT scanner manufacturers. Due to the errors and artifacts produced by the many different components in a CT scanner, various calibration, correction, error and artifact elimination algorithms may play even a bigger role in the final image quality than the actual, plain reconstruction algorithm.

The principal structure of a medical CT scanner is presented in figure 1.6. [18]. The presented structure, also known as the third-generation construction, consist of an x-ray tube producing a fan shaped beam of x-rays, an arc shaped x-ray detector and a reasonably complex set of precision mechanics allowing the source and detector to rotate at a high speed, presently even more than 2 rotations per second, around the patient. Patient is lying on a light material table motorized to enable axial body movement during the scanning.

A photograph of a state-of-the-art third generation, high definition CT scanner is presented in figure 1.7.

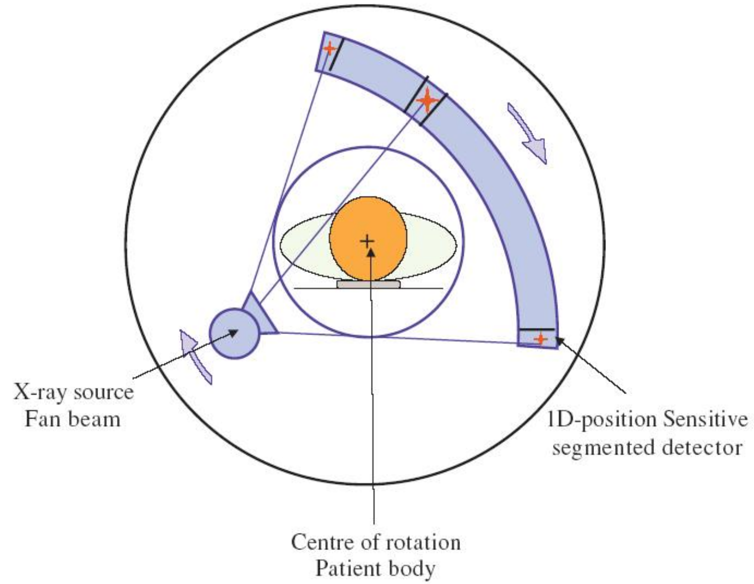

Figure 1.6: Principal structure of a third-generation CT scanner [18].

Figure 1.7: High definition CT scanner in a patient friendly operating environment.

In early third-generation CT scanners the beam is fan shaped (figure 1.8 (a)), meaning that x-rays are emitted from the x-ray tube in a plane perpendicular to the axis of rotation and there is only one row of detector elements to collect one slice of image data at a time. In later, so-called multi-slice CT scanners (figure 1.8 (b)), the x-ray beam is actually cone shaped and several detector element rows are exposed at the same time enabling much larger set of data to be collected in one rotation. It should be noted that with cone shaped x-ray exposure, x-rays are perpendicular to the rotation axis only for the center rows of the detector.

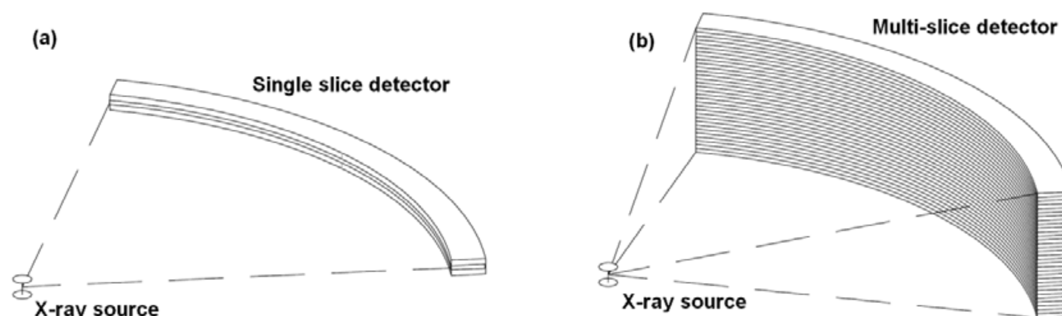

Figure 1.8: X-ray beam and detector configurations in third-generation CT scanners, (a) Single slice CT scanner with a fan-shaped x-ray beam, (b) Multi-slice CT scanner with a cone shaped x-ray beam.

A modern, multi-slice, solid-state CT detector is presented in figure 1.9. Radiation first passes through a precision, post-patient grid collimator enabling x-ray focusing and efficient rejection of scattered radiation. After collimation, radiation enters an inorganic scintillator crystal which is constructed of small individual scintillator sections, all optically separated from each other by nearly opaque but highly reflective intermediate walls. Light emitted by the individual scintillator sections is collected by a photodiode chip consisting of photodiode elements dimensionally matched and aligned to the scintillator sections.

Photodiode chips utilized in state-of-the art CT scanners are very large due to the strong tendency in the CT industry to increase the number of detector rows and simultaneously recorded x-ray image slices. At least one manufacturer is currently routinely selling CT machines which are simultaneously collecting data from 320 detector rows. From radiography point of view the main motivation for this has been the ability to image human heart with only one rotation and therefore within a timeframe where heart muscles are nearly stationary during the scan.

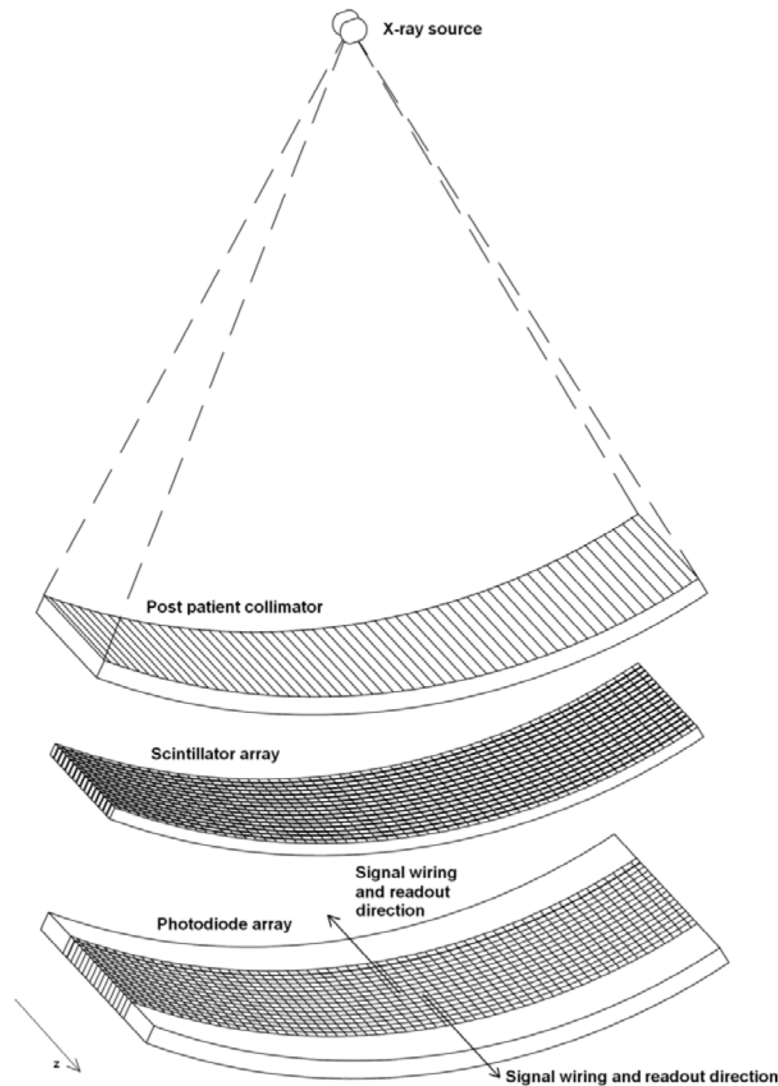

Figure 1.9: Principal structure of a multi-slice CT detector.

Even though there are no real inactive zones within the sensitive photodiode area, the electrical signals generated by the increasing number of photodiode elements must be transmitted to the actual data acquisition system (DAS) of the CT scanner. This is an increasing problem from detector design point of view, and present 64+ slice machines must already use unconventional methods for signal collection, routing and multiplexing. The signal wiring and routing arrangement sketched in figure 1.9 is feasible only in CT detectors with a coverage of 16 or possibly 32 slices but definitively not more than that. The exemplary 16-slice detector presented in figure 1.9 has first 8 rows of detector elements connected into DAS by signal wiring arranged on the silicon

detector and detector substrates in the z direction. The other 8 detector rows are similarly read out in the -z direction.

It should be emphasized again here that the large area silicon detector chips utilized in CT applications operate totally differently in comparison to the high energy physics strip detectors, primarily in the sense that they operate as indirect detectors recording distributed light signals produced by a scintillator matrix attached to them. It has been a historical convention to call such radiation detectors as scintillation detectors, but here a viewpoint emphasizing the key role of the silicon chip has been selected. The scintillator material has a great impact on the overall performance of a modern CT detector, but it is in fact the silicon component beneath the scintillator which distinguishes an advanced, state-of-the-art CT detector from its early predecessors. Therefore, large area CT silicon detector is the term used here to denote a CT detector based on advanced, planar silicon detector chips even though the silicon part actually detects the indirect radiation signal emitted as light from the scintillator.

As mentioned above, conventional type, large area CT detector chips have a limitation due to interconnects that can be routed on the chip itself and then further in the attached electrical interfacing substrates and cables.

Several solutions to the signal routing and multiplexing problem have been proposed and implemented.

One possible method is to use back illuminated photodiodes [19, 20]. In such photodiode components (see figure 1.10) the light photons are absorbed unconventionally not on the chip surface where the diode junction has been constructed, but on the opposite side, the back side. Figure 1.10 also presents the possibility of using a common carrier substrate for the detector chip and related preamplifier electronics.

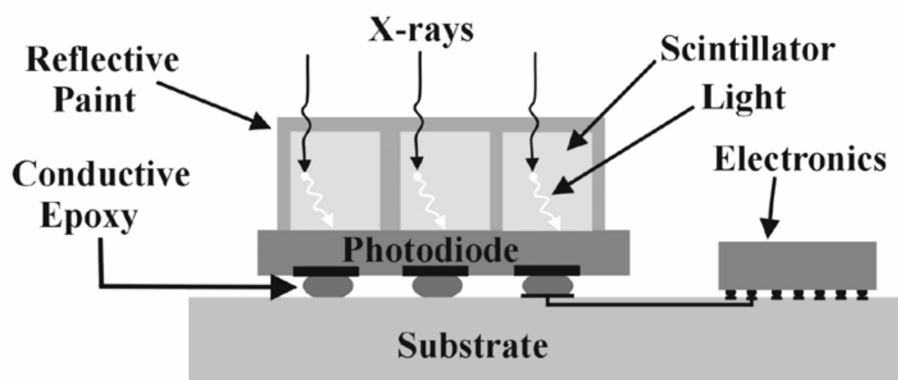

Figure 1.10: Back illuminated photodiode [19].

A second approach is to use a photodiode matrix chip, called passive matrix photodiode [21] where some multiplexing circuitry has been integrated on the photodiode chip

itself. In such a matrix structure, all photodiode elements located within same photodiode row or column share a common signal readout line, figure 1.11. On a passive matrix photodiode chip with m rows and n columns, only m or n readout signal lines are required although a total of m x n photodiode elements can be read out.

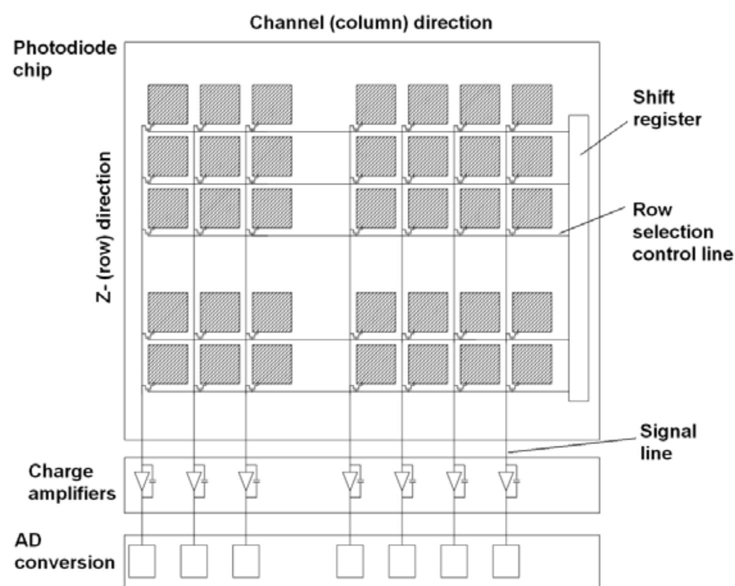

Figure 1.11: Passive matrix photodiode chip [21].

A third solution, which is of special interest in this thesis is a structure where through-wafer interconnects (TWIs), somewhat similar to the smallest vias found on conventional printed circuit boards (PCBs), are manufactured on the photodiode chip (figure 1.12). Such TWIs are then utilized for transmitting the signals of individual photodiode elements from the active surface of the photodiode chip to the inactive side of the chip. This arrangement enables manufacturing of large area photodiode chips without any inactive edge areas. Sometimes terms "edgeless" and "tileable" are used to describe detector chips with such packaging advantage.

Figure 1.13 presents six CT slice images of abdomen area of a patient. The cross-sectional images are from different positions of the abdomen along the spinal column. Intravenous contrast agent has been utilized for improving image contrast. All internal organs are very clearly visible.

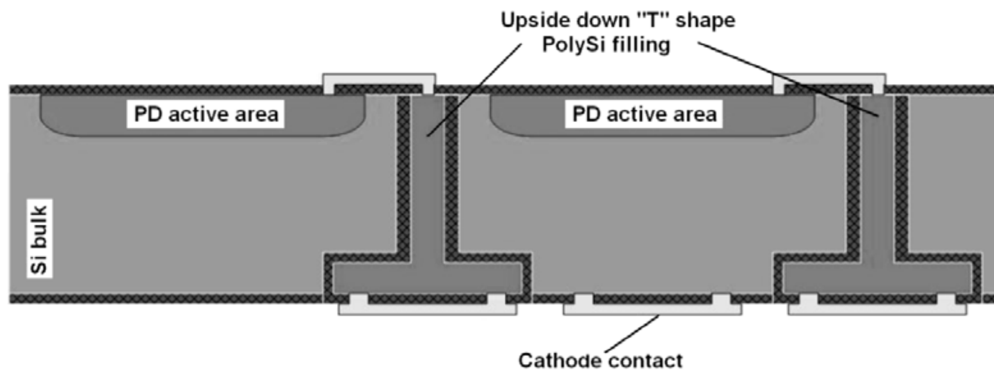

Figure 1.12: TWI photodiode structure enabling edgeless, mechanical integration of neighbouring chips [22].

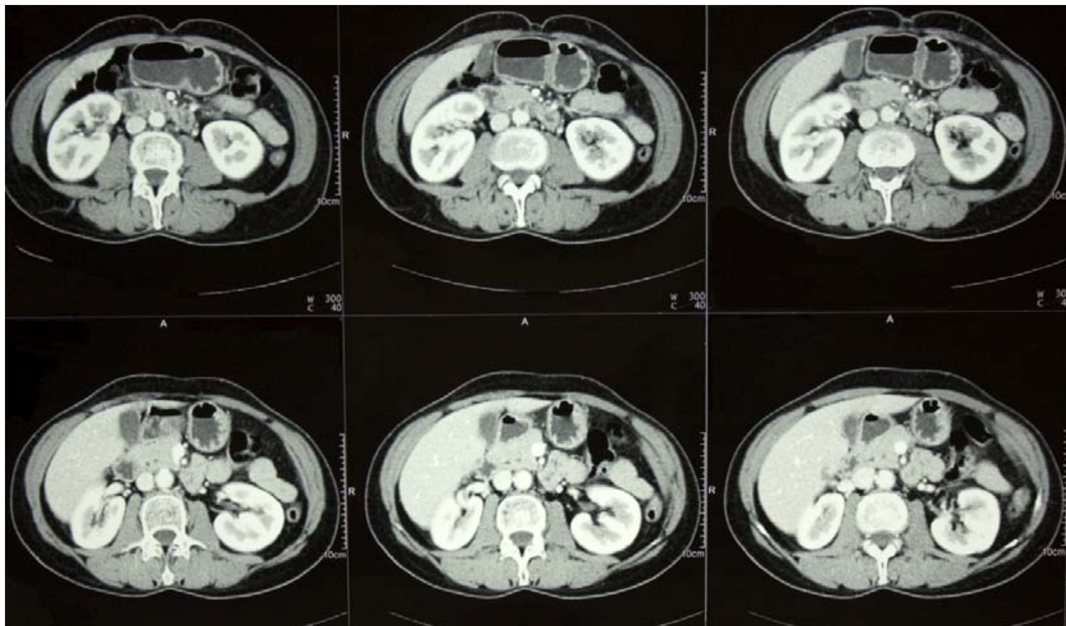

Figure 1.13: Six medical CT slice images of a patient abdomen area.

Fundamentals of CT silicon detector physics, manufacturing and readout are presented below in chapters 1.2, 1.3 and 1.4. Chapter 3 is devoted to presentation of design details and results relating to author's research work in the area of these detectors.

1.2 Planar silicon pn-junctions as radiation detectors and photodiodes

1.2.1 Principal properties of pn-junctions

Silicon strip detectors, large area CT silicon detectors as well as all planar silicon radiation detectors and photodiodes are based on the properties of silicon pn-junctions.

The very basic properties of a pn-junction can be visualized by bringing two initially separated silicon regions of opposite conduction type into intimate contact.

When the regions are integrated to form a single silicon crystal of two conductivity types, excess electrons in the n-type region flow into the p-type region due to the gradient of free carrier density across the junction border. In a similar manner, holes flow into the n-type region. An electric field results from the fixed space charges created by the ionized atoms left behind by the charge carriers flowing across the junction.

An equilibrium state is reached when the drift current component resulting from the electric field equals the diffusion current component resulting from the charge carrier gradients. The principal properties of a pn-junction in such equilibrium state are presented in figure 1.14. Three approximations, typically corresponding well with real silicon detector pn-junctions, have been made here. It has been assumed that the region of the ionized dopant atoms and resulting electric field, is completely depleted of free charge carriers. Therefore this region is called depletion region. On the other hand, it is also assumed that the non-depleted areas on the p and n-sides of the junction have no electric field and that the carrier densities in these regions are equal to dopant atom densities. These regions are called neutral regions. The third well justified assumption is that the junction boundary is abrupt meaning that dopant densities are uniform across the p region and the n region and change stepwise at the junction border.

If we now apply Poisson's equation in the n region in equilibrium conditions, we get

$$-\frac{dE}{dx}=\frac{d^2\phi}{dx^2}=-\frac{\rho}{\varepsilon_s}=-\frac{qN_d}{\varepsilon_s} \tag{1.5}$$

where E is the electric field, ϕ the electric potential, ρ the space-charge density, ε_s the permittivity of silicon, q the absolute value of the electron charge and Nd the donor density in the n region. Integration of equation 1.5 will result in

$$E=-\frac{qN_d}{\varepsilon_s}(x_n-x), \qquad 0<x<x_n \tag{1.6}$$

where x_n is the width of the n-side depletion region.

Further integration will give us

$$\phi = \phi_n - \frac{qN_d}{2\varepsilon_s}(x_n - x)^2 \tag{1.7}$$

where ϕ_n is Fermi level deviation from the intrinsic Fermi level E_i in the n region.

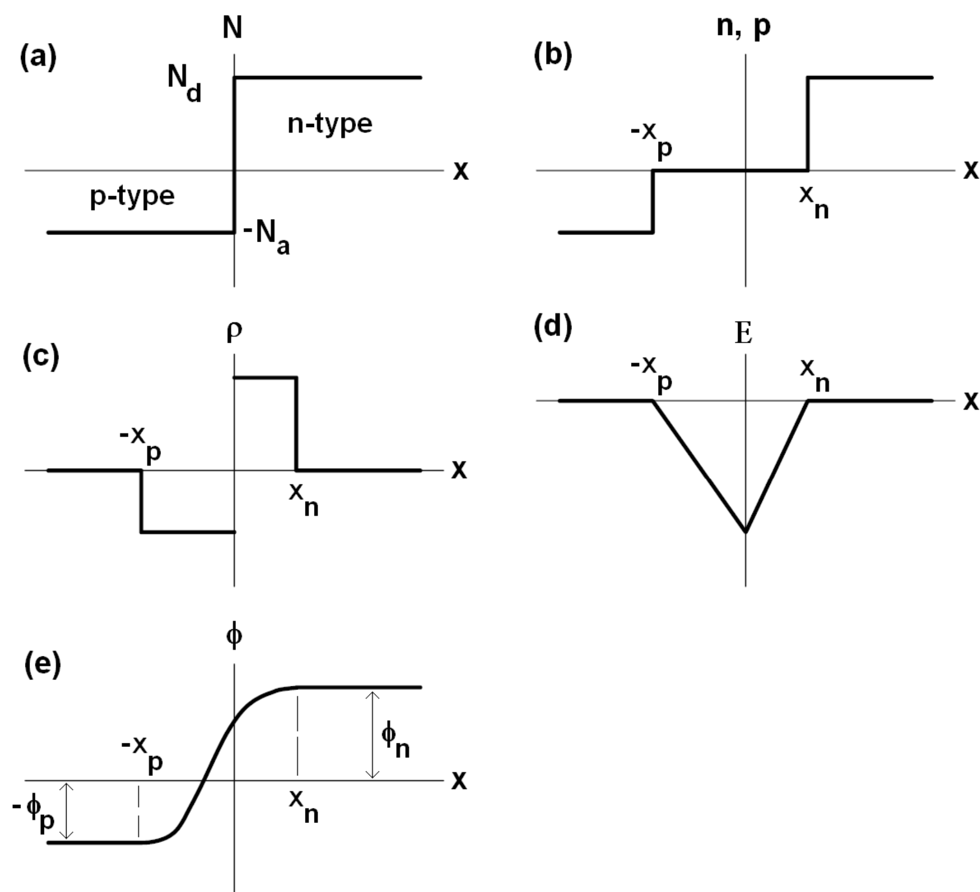

Figure 1.14: Key properties of an abrupt pn-junction: (a) net dopant concentration, (b) carrier densities, (c) space charge density, (d) electric field, and (e) potential.

ϕ_n is further obtained from

$$\phi_n = \frac{kT}{q} \ln \frac{N_d}{n_i} \tag{1.8}$$

where k is Boltzmann´s constant, T is absolute temperature and n_i is the charge carrier density in intrinsic, i.e. ideal, non-doped silicon.

We can now apply same equations on the p-side of the junction, resulting in following corresponding equations

$$E = -\frac{qN_a}{\varepsilon_s}(x + x_p), \qquad -x_p < x < 0 \tag{1.9}$$

$$\phi = \phi_p + \frac{qN_a}{2\varepsilon_s}(x + x_p)^2 \tag{1.10}$$

$$\phi_p = -\frac{kT}{q} \ln \frac{N_a}{n_i} \tag{1.11}$$

where Na is the acceptor density in the p region, x_p is the width of the p-side depletion region, and ϕ_p is the p region Fermi level deviation from E_i.

Internal, built-in potential ϕ_i of the pn-junction is now obtained by subtracting

$$\phi_i = \phi_n - \phi_p = \frac{kT}{q} \ln \frac{N_d N_a}{n_i^2} \tag{1.12}$$

Requiring that the electric field must be continuous at x=o, we further obtain following result, especially meaningful for pn-junctions of high asymmetry in terms of doping densities on n and p-sides of the junction.

$$N_a x_p = N_d x_n \tag{1.13}$$

Planar silicon radiation detectors and photodiodes are typically manufactured on a silicon wafer substrate of low or medium resistivity, whereas the doping density of the planar processed surface electrodes is several orders of magnitude higher.

Equation 1.13 shows that the depletion region will be heavily concentrated on the conductivity region of lower doping density. If a low or medium resistivity, n type wafer material is used, and a high doping concentration p-well is processed on such substrate, the depletion region will extend almost solely to the n bulk region of the pn-junction.

If we combine equations 1.6, 1.9 and 1.13, and assume that we have such an asymmetric pn-junction where N_a>>N_d, we will get

$$x_d \approx \left[\frac{2\varepsilon_s}{q} \phi_i \left(\frac{1}{N_d} \right) \right]^{1/2} \quad (1.14)$$

where x_d is the total width of the depletion region.

Some planar silicon detectors, especially the strip detectors, are operated at a rather large reverse bias voltage in order to increase the detection efficiency and to minimize electrode capacitance. The effect of such reverse bias voltage V_R may be incorporated into equation 1.14 by replacing the built-in potential by the sum of built in potential and the reverse voltage

$$x_d \approx \left[\frac{2\varepsilon_s}{q} (\phi_i - V_R) \left(\frac{1}{N_d} \right) \right]^{1/2} \quad (1.15)$$

The capacitance of the pn-junction is typically of great interest and concern in large area silicon radiation detectors and photodiodes, since its magnitude has a large impact on the noise performance of the whole detector system. In most applications, lowest possible capacitance at the given pn-diode geometry is desirable.

Pn-junction small-signal capacitance per unit area can be obtained assuming a plate capacitor where separation of the electrodes is equal to depletion region width. Utilizing equation 1.15 for an asymmetrical pn-junction, we get

$$C = \frac{\varepsilon_s}{x_d} = \left[\frac{q\varepsilon_s}{2(\phi_i - V_R)\left(\frac{1}{N_d} \right)} \right]^{1/2} \quad (1.16)$$

Another characteristic strongly affecting the quality, detection capability and noise of a planar silicon detector is the dark current of the detector pn-junction.

A detailed analysis of the many geometrical and manufacturing process related factors affecting the dark current of a pn-junction detector is beyond the scope of this introduction. In an ideal pn-junction detector structure, the effect of geometrical design aspects and imperfections caused by the manufacturing process are suppressed at a level, where the total pn-junction dark current is dominated by generation of charge

carriers in the depletion region of the junction. Such current density can be estimated from

$$J_g = \frac{qn_i x_d}{2\tau_0} \tag{1.17}$$

Where J_g is the generation current density and τ_0 is the lifetime of minority charge carriers in the depletion region. Recalling equation 1.15, we can conclude that generation based dark current is proportional to the square root of the reverse bias voltage (assuming $V_R >> \phi_i$) and inversely proportional to the minority carrier lifetime. τ_0 is often used as an indicator of silicon wafer material and manufacturing process quality since a high value of τ_0 results from a low concentration of undesirable energy states in the silicon crystal.

1.2.2 Radiation detection and photodiode properties of pn-junctions

Intuitively, the two radiation types of interest in this thesis, high energy charged particles of high energy physics experiments and visible light photons emitted by scintillator crystals of CT scanners, differ a lot from a detection point of view. This is true in the sense that the optimal operating parameters of the pn-junctions in these detector chips are different mainly due to very dissimilar penetration depths of these radiations.

However, in both of these two applications and detector types the principal detection characteristics are still based on the charge collection properties of depleted pn-junctions. Detectors in both application areas are also manufactured on silicon substrates characterized by high minority carrier lifetimes.

In high energy physics experiments, the charged particle trajectories to be recorded by the strip detector tracker instruments or vertex detectors, are created by very high energy particles, often called relativistic particles or minimum ionizing particles (MIPs). These terms refer to the fact the speed and energy of these charged particles is large enough to require their treatment based on the laws of special relativity, and that the signal charge left by the particle to the detector is a very weak function of the energy carried by the particle. When the speed of the particle approaches that of light, the energy left by the particle to the detector medium reaches a nearly constant, minimum value. At these very high energies, the charged particle loses a very small fraction of its energy when passing through the detector and therefore continues its track virtually unaffected by the detector.

The principle of the detection process of a high energy charged particle hitting the pn-junction of a silicon strip detector is presented in figure 1.15.

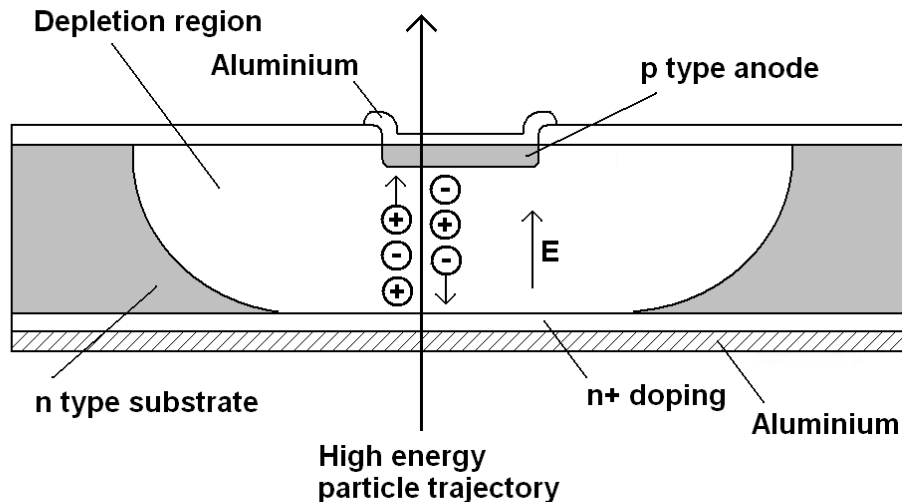

Figure 1.15: Detection process of a high energy charged particle hitting a strip shaped pn-junction of a silicon strip detector.

As described above, the particle traverses the detector chip virtually unaffected. However, based on the Coulomb forces between the particle and the orbital electrons of the silicon crystal, some electrons gain enough energy to cause ionization. Such electrons will move freely in the electric field present in the depletion region of the pn-junction. These free electrons leave behind vacancies, holes, which will equally move in the electric field but into opposite direction. In an ideal situation, all these charge carriers are swept to the top and bottom contacts of the detector component by the electric field.

As presented in figure 1.16, the charge created by a traversing MIP is spread laterally and results in charge signal collection typically in two or three neighbouring pn-diode strips. Strip pitch and dimensions shown here are typical for high density strip structures. Charge sensitive pre-amplifiers connected to each strip will record the signal charges for further signal processing and off-line analysis.

The thickness of the strip detector chips varies typically between 300 μm and 500 μm.

The energy loss of a MIP and hence the signal left in the strip detector chip is roughly constant per unit length of penetration through the detector chip. For a 300 μm thick detector chip the typical signal charge created by a MIP is 4 fC or 25000 electrons.

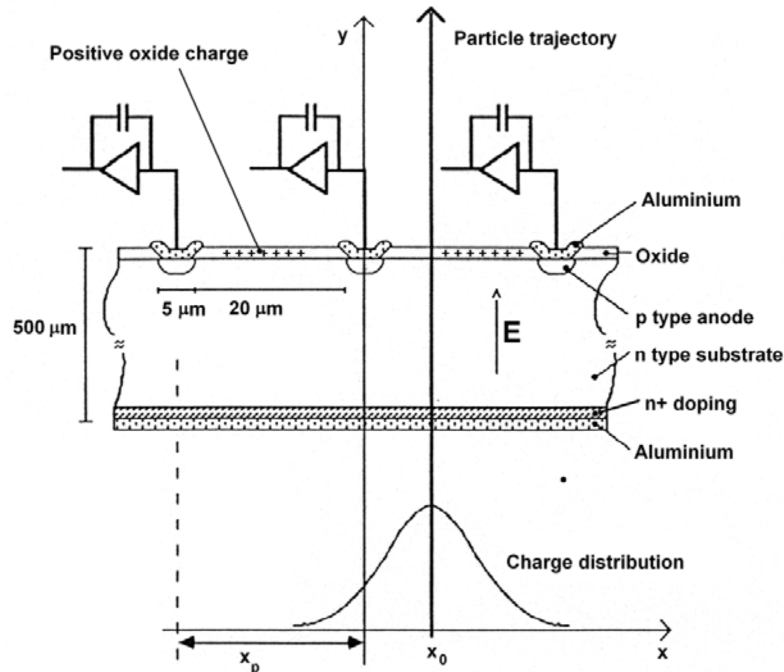

Figure 1.16: Detection process of a high energy charged particle traversing a silicon strip detector between two neighbouring strip electrodes.

In medical, computed tomography (CT) scanner instruments, the radiation penetrating the patient enters the detector construction presented in figure 1.9. Radiation which meets the detector in a perpendicular direction passes through the grid collimator and is absorbed in the scintillating crystal sections aligned with the collimator openings and the underlying photodiode elements. Scintillation crystals utilized in present CT scanners are typically based on gadolinium oxysulfide (GOS, Gd_2O_2S) scintillator material, but different CT instrument and scintillator manufacturers have developed several own recipes to enhance its properties for CT use. GOS, like many other scintillators, produces visible light when x-rays are absorbed into its crystal structure. Intensity of the light emitted is reasonably well proportional to the x-ray intensity absorbed. GOS emits light within a wavelength range of several hundred nm but most typical peak wavelength is 510 nm, which corresponds to a bright green colour.

Although the average penetration depth of the green colour, 510 nm photons is less than 1 µm into the silicon crystal, very large percentage of them will contribute to the signal current and charge. The photon detection process is presented in figure 1.17.

The principal detection process is similar to the strip detectors presented above. In this case, each photon ideally creates one electron-hole pair, and these charges are swept by the internal electric field into the top and bottom electrodes of the photodiode structure.

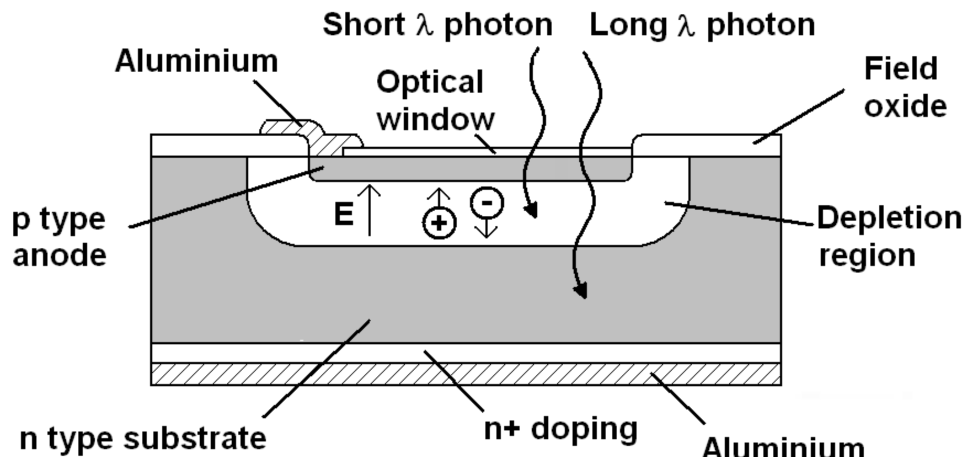

Figure 1.17: Light photon detection process in a large area CT photodiode chip.

Due to the very small penetration depth of the photons, it is not feasible to use a reverse bias voltage across the diode to generate a wide depletion area. A reverse bias voltage will contribute to larger dark current and therefore larger noise in the CT system. CT system photodiodes are typically operated in photovoltaic mode meaning that the DC bias across the photodiode component is minimized and it is often equal to the preamplifier offset voltage, a maximum of a few millivolts.

Low photodiode element capacitance is still desirable and therefore silicon wafer material resistivity for CT detector chips is selected to provide best possible compromise between low capacitance and low dark current.

Due to the small penetration depth and different interaction mechanism of the visible photons, special attention must be placed on the surface structures of the CT photodiode detectors. The entrance window of the photons must be thin and must be optimized in terms of refractive indices of the materials used, otherwise a considerable percentage of the photons will be reflected from photodiode surface. Typically a combination of silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) layers is used. Most CT photodiode components are based on n type substrate materials and p type surface electrodes for the individual detector cells. The impurity doping profile and dose of the p anodes must be carefully designed to minimize loss of photons in the non-depleted surface layer and to maximise the depletion width in the photovoltaic operating mode.

A typical sensitivity curve for a high quality, single element, silicon photodiode, well matched for a CT scintillator, is presented in figure 1.18 [23]. Responsivity, i.e.

photodiode signal current vs. light power entering the photodiode is approximately 0.37 A/W at 510 nm for this particular photodiode product. Figure 1.18 also presents the 100% quantum efficiency (QE) line denoting the maximum achievable signal level in a situation where every light photon entering the photodiode produces an electron-hole pair, and this charge is successfully collected by the electric field of the photodiode.

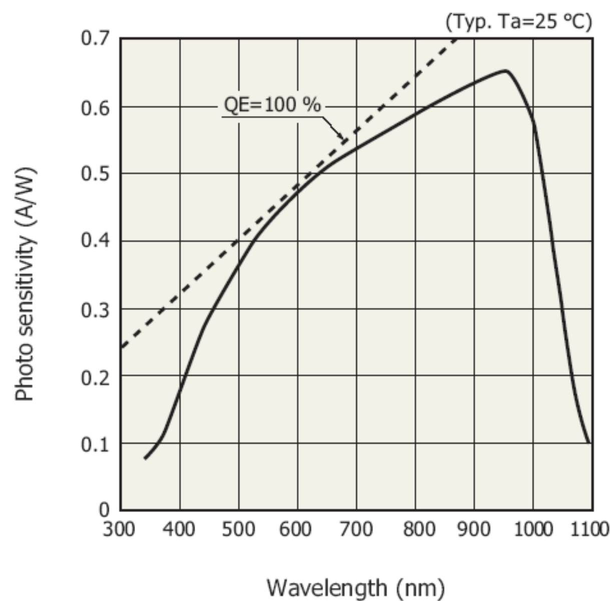

Figure 1.18: Response curve of a high quality photodiode, Hamamatsu S3590-09 [23].

1.3 Fabrication of planar silicon detectors and photodiodes

The planar processing technology of ICs has reached a very advanced level where 12" diameter silicon wafers are processed in state-of-the-art manufacturing lines with linewidths down to 50 nm. Wafer processes are very complicated with a large number of polysilicon and metallization layers.

Planar strip detector and large area CT chip manufacturing processes are far less advanced than IC processes in terms of wafer size, linewidth and process complexity. However these detector chips must operate at very low dark current and capacitance levels and in case of strip detectors, the components must also withstand considerable reverse biasing for optimal performance.

A well-controlled manufacturing process of detector raw material wafers will produce starting material of excellent lifetime and resistivity properties. In order to preserve such critical characteristics throughout the detector chip manufacturing process, an equal level of process control and cleanliness must be implemented.

The number of masking levels required for strip detector manufacturing may be as low as two, compared to a minimum of 11 levels even in the simplest IC circuits. In addition, the smallest strip detector or CT detector chip features required are usually several microns (2-4 µm), and limits of patterning capability are typically of no concern.

From manufacturing point of view, the most challenging characteristic of strip detector and CT silicon detector chips is their very large size. IC circuit dimensions may reach 25 mm x 25 mm in exceptional cases but strip detector and CT detector chips are without exception far larger than this. Strip detector chip dimensions may reach 100 mm x 100 mm while CT detector chips of dimensions 25 mm x 50 mm are more typical. Excluding the challenges relating to post processing of the completed detector wafers (testing, dicing, electrical interfaces, encapsulation), special tooling, equipment and process steps are required in the actual silicon wafer process.

Manufacturing of the optical patterning tooling (masks) for these large area detector chips has traditionally required special attention and methods from the tool producers [24].

Another special requirement results from the need of processing patterned structures on both the front and back surfaces of strip detectors and CT detector chips. Double sided strip detectors presented in chapter 2.3 require almost identical processing on both sides of the wafers. CT detector chips with TWIs, as presented in chapter 1.1.2, equally require several chemical and lithographic patterning steps also on the back side of the wafer.

The main steps and the production flow of a basic type radiation detector chip manufacturing process is presented in figure 1.19. This simplified process description is applicable to charged particle detector chips where p type anode electrodes are manufactured on an n type wafer material.

In the first and very critical manufacturing step, a field oxide (FOX) is grown on the wafer to form the high quality insulation outside the actual pn-junction area. Thermal oxidation produces silicon dioxide (SiO_2) of very high quality and results in a chemically well-controlled interface between the silicon substrate and the FOX.

Thermal oxidation is, however, a very slow process, and FOX thickness is typically increased in another process step where a Chemical Vapour Deposition (CVD) reactor is utilized to deposit a further layer of silicon dioxide on the thermally grown part of FOX. This oxide is called Low Temperature Oxide (LTO) due to the much lower processing temperature compared to thermal oxidation (450 ^{0}C compared to 1050 ^{0}C).

After the oxidation steps follows first patterning step where selected parts of the front side oxidation are removed utilizing the standard lithography steps of planar processing. A photoresist material is deposited, exposed, developed and baked in order to build a

protective layer on those areas where the underlying silicon dioxide should be preserved.

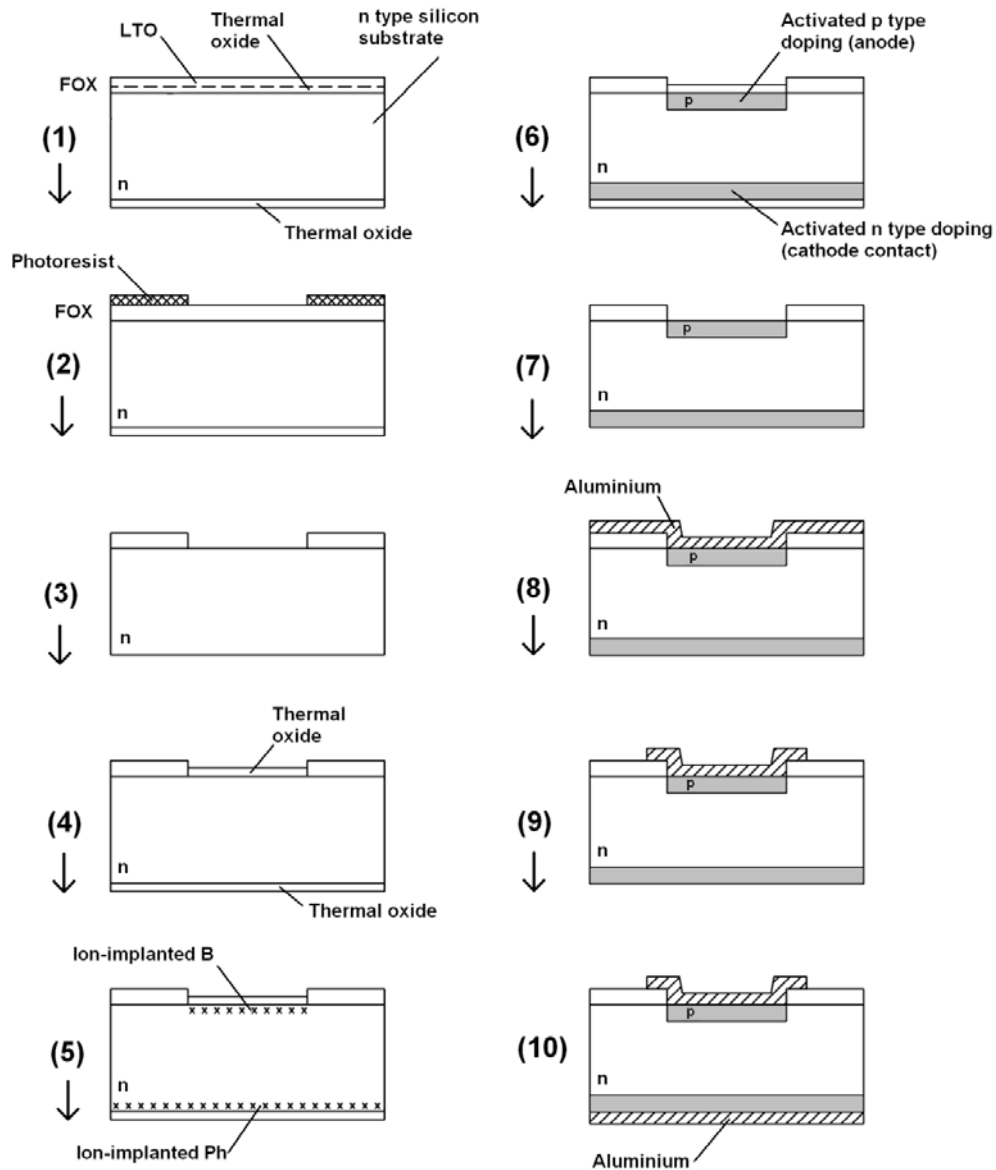

Figure 1.19: Main manufacturing process steps of a typical planar silicon detector chip.

Unprotected silicon dioxide is etched in a chemical bath of buffered hydrofluoric acid. This kind of etching step is referred to as wet etching. Photoresist is removed after the wet etching step.

Front surface p doping is introduced utilizing ion-implantation and a successive annealing step. Ion-implanter introduces boron ions into random lattice locations in the the silicon crystal and the high temperature of the annealing step enables these impurity ions to reach actual lattice sites and become active acceptors. Prior to the ion-implantation step, a thin thermal oxide, also known as screen oxide, is grown to protect the exposed silicon surface.

In our exemplary process, back side of the detector chip is also ion-implanted in order to construct a low resistivity ohmic contact to the n type bulk material. In this case the impurities are phosphorus ions. Otherwise the procedure basics are identical. It should be noted that in this process description, same annealing step is shared by the two ion-implantation steps.

The protective screen oxide is removed next, and sputtering technology is used in order to grow a thin aluminium layer on the front side of the detector chip. Aluminium is then further patterned in a lithographic step similar to the one described above for FOX. A protective layer of photoresist is optically patterned and underlying aluminium is again etched in a wet chemical etching step.

Back side of the detector chip is identically covered by aluminium in a sputtering step.

Both metallizations are annealed in the last actual processing step.

The planar process required for a basic type CT photodiode detector chip is not very different from the charged particle detector process description given in figure 1.19. Figure 1.20 presents again a simplified process flow for a light detecting CT detector chip assuming that steps 1-5 are similar to figure 1.19.

The initial screen oxide grown for ion-implantation serves as the optical window of the photodiode element or a new similar oxide is grown instead. The window material is patterned in a lithographic step similar to the ones described above for FOX and aluminium, see steps (7) and (8) in figure 1.20. Aluminium is deposited on front surface and it is patterned to provide the necessary electrical contact to the p type anodes. Back side is metallized as above.

As explained in chapter 1.2, CT photodiode surface structures must be optimized in terms of light absorption and photon conversion into electron-hole pairs. The active photodiode surface must be covered with an antireflection layer, typically constructed only of silicon dioxide (SiO_2) or consecutive layers of silicon dioxide (SiO_2) and silicon nitride (Si_3N_4). Front side metal should contact the surface p electrode only at a selected location to minimize active area coverage with the opaque aluminium metallization.

Therefore, the planar process for a CT detector chip requires, in principle, only one additional patterning step for the metal contact to the underlying p implant.

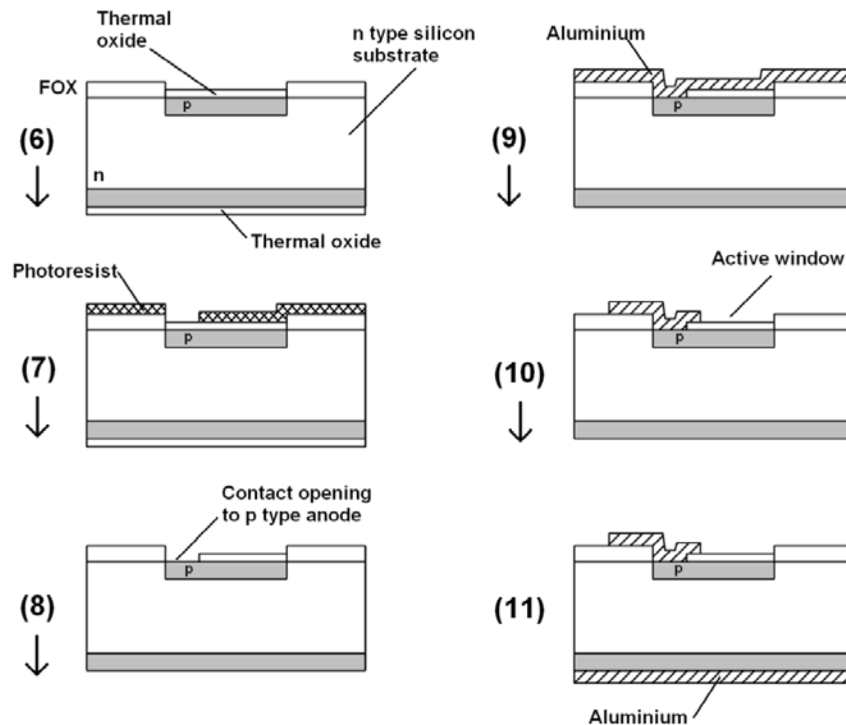

Figure 1.20: Main manufacturing process steps of a typical CT photodiode detector chip.

Despite the compact manufacturing processes described above, and the low number of lithography steps required, special attention is required to ensure that the detectors chips manufactured will exhibit the high performance which is expected for the strip detector or CT detector chips. Some of the key parameters of a well-controlled detector manufacturing process are discussed below.

Extreme cleanliness is required throughout the process line clean room and the equipment utilized for the detector chip processing. Chemical cleaning steps (not shown in figures 1.19 and 1.20) which are applied frequently during the process flow should base on very clean chemicals and use of dedicated wet stations as much as possible. It is often the case that impurity levels of no interest for many IC products will destroy the performance of detector chips. Cleanliness requirements are also highlighted in the high temperature steps where mobilities of any impurity atoms, e.g. metals are very high and they may reach locations and interfaces critical to detector chip operation. In many

cases, high temperature furnaces must be dedicated only for detector chip manufacturing and same furnace tubing may not be shared with IC products.

High and medium resistivity silicon wafers, intended for radiation detector and photodiode manufacturing are typically characterized by very long minority carrier lifetimes. Recalling equation 1.17, it is straightforward to conclude that deterioration in lifetime τ_0 will immediately result in increased dark current of the detector channels. All processing steps should be designed to maintain and improve lifetime within the possible limits. A common technique is to use gettering as a means of improving and maintaining the lifetime properties of silicon crystals [1, 2, 24]. Gettering is a process where unwanted impurities present in the silicon crystal are attracted into an alternative location where they are trapped and do not deteriorate the performance. Heavy phosphorus ion-implantation and a subsequent anneal is a well-known gettering method.

Dark current, inter-element current leakage and isolation, detector element capacitance, and pn-diode breakdown voltage are all known to be sensitive to the oxide charges always present in the FOX between the active pn-diode elements (see figure 1.16). Silicon dioxide typically exhibits some fixed positive charge close to the interface between the SiO_2 layer and the underlying silicon substrate. A reasonable amount of positive charge may even be desirable since positive charge attracts electrons to the interface and may improve isolation of neighbouring diode elements from each other. However, too high or too low oxide charge densities may cause adverse effects to detector chip performance. Mobile charges present in the FOX may cause problems in applications where the biasing of the diode changes during normal detector operation.

1.4 Planar silicon detector readout

The two applications discussed in this thesis, high energy physics experiments and CT scanners, both require simultaneous collection of charge created by ionizing radiation from a large number of readout channels. This compact presentation of the amplifier and readout electronics of these applications concentrates only in the very front-end part of the electronics, i.e. the electronics closest to the detector chips.

The silicon tracker instruments incorporated in high energy physics experiments typically require signal processing and transfer from sensor areas measured in square meters rather than square millimetres. In practise this results in tens of thousands and presently even in millions of readout channels.

Third-generation, cone beam CT scanners also exhibit large imaging areas covered by nearly square detector elements of approximately 1 mm x 1 mm pitch. Such scanner machines typically have a 1 m wide, arc shaped detector, and therefore a state-of-the-art 320 slice scanner will need fast data collection from a total of 1000 x 320 = 320 000 detector elements.

In both these applications, space available for detector chip mechanical supports, electrical interconnections and cabling is at a premium.

CMOS (Complementary Metal-Oxide-Semiconductor) wafer processes currently available from commercial wafer foundries enable very high integration level for all digital signal processing circuits required in the DAS of a physics experiment or a CT scanner. However, device physics of analogue amplifiers and the parameters affecting the electrical noise in this part of the DAS electronics have not changed. A low noise preamplifier still requires adequate power and operating current to produce amplification at low noise levels. In practise this means that power is still consumed more or less in numbers which are directly proportional to the total number of readout channels of the system.

In high energy physics experiments, radiation and signal is produced only in the particle collisions in the interactions point of the experiment. Timing of the collider is delivered to the experimental stations which will align the active windows of the detector instruments to the collision instants.

The operating principle of the integrated readout electronics applied in the Microvertex detector of the DELPHI experiments is presented in figure 1.21 [25]. This presents the principal structure of one amplifier channel.

Each strip detector anode is connected into input of an integrating, charge sensitive preamplifier. The amplifier feedback loop contains a capacitor for signal integration (C_{int}) and a switch for resetting this capacitor. As long as the resetting switch is closed (conducting), amplifier output is shorted to input and no integration occurs. Immediately after opening (not conducting) the switch, any current flowing from the anode of the strip diode towards the input of the preamplifier, will be integrated as a charge Q in C_{int}.

Output voltage of the preamplifier V_o will then be

$$V_0 = \frac{Q}{C_{int}} \tag{1.18}$$

Output of the preamplifier is connected through switches to two sampling capacitors C_{store1} and C_{store2}. The output voltage of the preamplifier may be stored to these capacitors by closing the related sampling switches for a short period. If both switches are closed for a short time after the feedback loop reset switch is opened, both capacitors will follow the preamplifier output. If first sampling switch (Store 1) is opened just before the collision in the experimental station, and the second switch (Store2) will be opened just after the collision, a differential signal consisting of only the charge collected during the collision will be recorded in the capacitors.

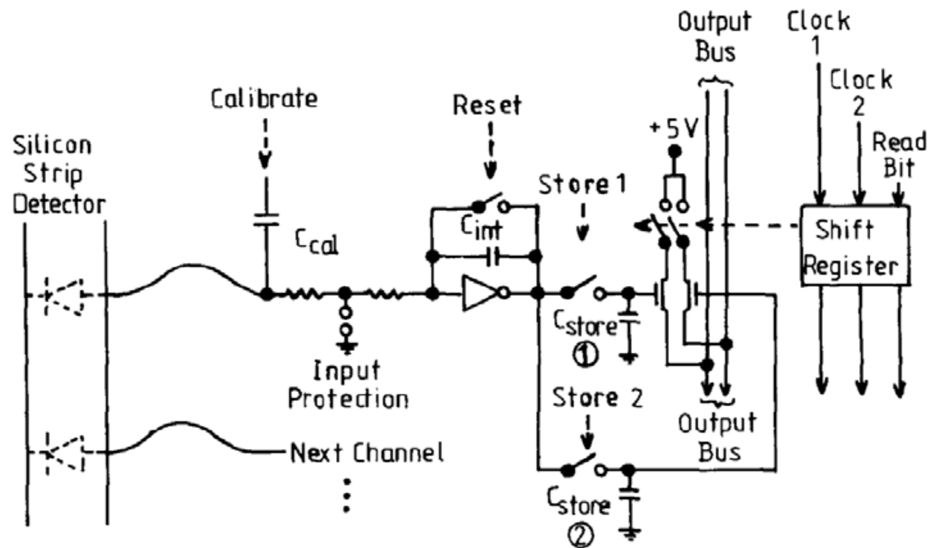

Figure 1.21: Principle schematic of the integrated, preamplifier electronics applied in the Microvertex detector of the DELPHI experiment [25].

This principle of double correlated sampling (DCS) will effectively cancel out some of the non-ideal characteristics of the specific detector chip channel and the preamplifier channel.

The two storage capacitors are connected to two source follower stages connected to a two pin output bus. All channels of an integrated amplifier chip will connect to this common output bus. In addition, output buses of several readout ICs may be daisy-chained and then finally connected to a common receiver amplifier at a higher level DAS amplifier unit.

As has been presented in the earlier chapters, CT scanner systems have evolved from simple one slice, fan beam imaging systems into high speed, wide coverage machines characterized by a cone shaped x-ray beam and a detector of up to 320 000 read out channels. In a modern CT machine, data may by collected from 1 000 different angles during a standard imaging procedure. Assuming that the mechanically rotating part of the machine, the gantry, rotates 360 degrees two times per second, we can simply conclude that data from each of the 320 000 detector channels must be collected at least 2000 times per second.

CT imaging procedure is a continuous process where x-rays are emitted and data collected for several minutes, in a minimum, without interruption. The data acquisition system (DAS) of the CT machine must therefore be capable of processing, transferring and storing very large amounts of data at a high speed to enable both on-line and off-line data reconstruction. Optical links are one method to transfer signals from the rotating gantry to the machine body [26]. Due to the continuous operating mode, current

signals of individual detector and silicon chip channels must be integrated continuously between the data sampling instants.

The fraction of initial x-ray intensity I_0 passing through the patient may be as low as $10^{-4} \times I_0$ at the most dense parts of human body which means that the detector and the DAS must resolve signals within a very wide dynamic range.

Details of the DAS front-end parts utilized in commercial CT scanners are well-kept secrets amongst the machine manufacturers but an inevitable need and trend has been to increase the integration level of the analogue electronics and the placement of such electronics as close as possible to the silicon detector chips. This is a must to be able to handle the multiplexing and signal cabling needs in a state-of-art CT detector.

One commercially available solution to CT system analogue readout is presented in figure 1.22 [27]. This inherently simple readout circuit uses dual-integrator circuitry for each input channel. Each photodiode in the CT detector is therefore connected into two parallel analogue integrators. One integrator is active and the other is in hold state while its output is being digitized by the built-in AD (analogue-to-digital) converter. With such arrangement, each CT detector diode element has a 100% duty cycle and no dead time. Since the circuitry is integrated on one IC chip, good performance match between the two integrator circuits of each channel is achieved. Channel-to-channel variations and noise caused by interconnections are minimized due to same reasons. This circuit provides 20-bit AD conversion at data rates up to 6000 samples per second and therefore meets the readout speed requirement discussed above.

The digital outputs of the individual AD converters are collected by serial interface circuitry and the output of the digital data is handled through a high speed serial interface operating at a 32 MHz data clock frequency.

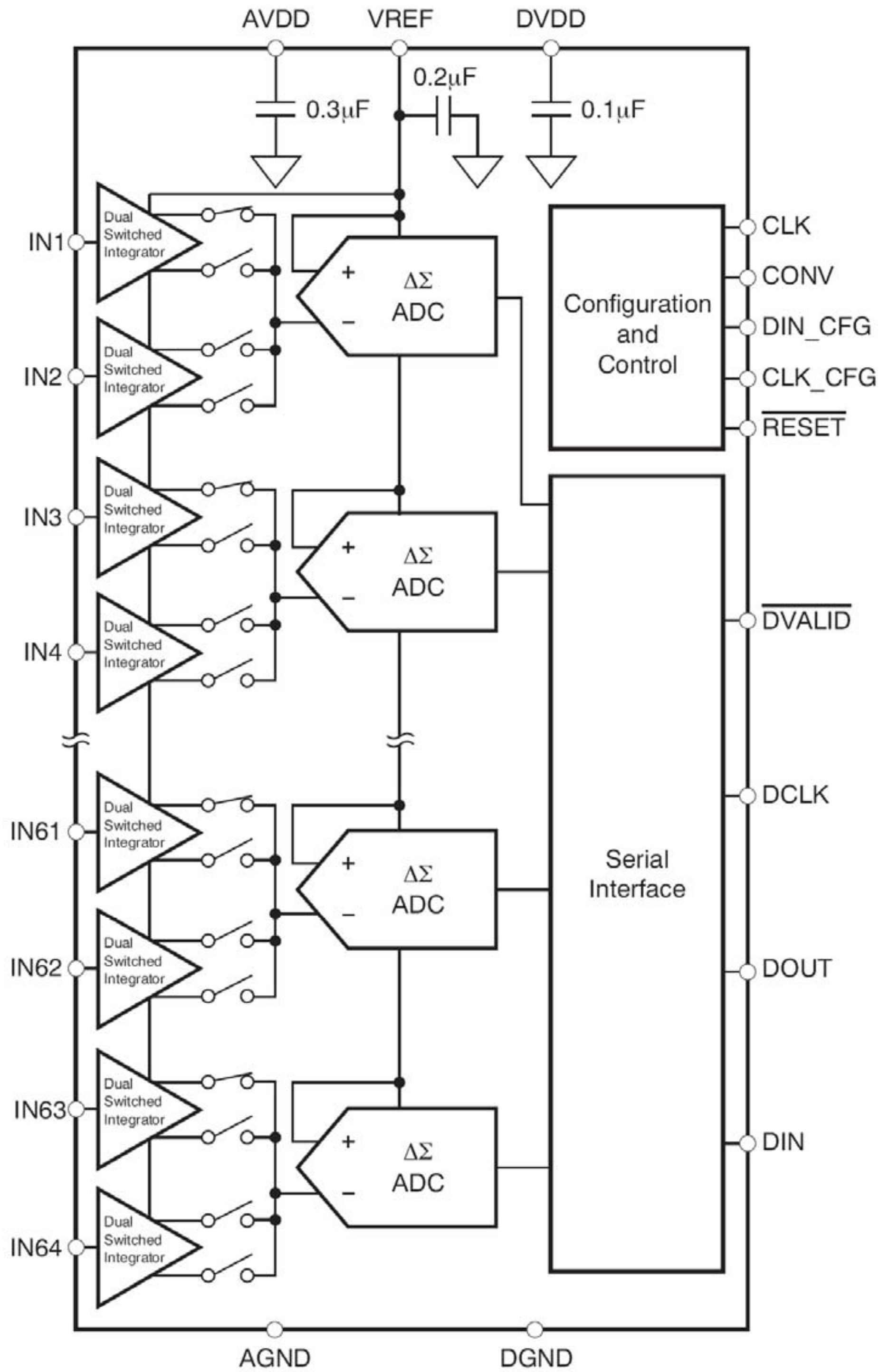

Figure 1.22: Block diagram presentation of DDC264 circuit designed for CT detector readout systems [27].

2 Silicon strip detectors for high energy physics research

2.1 Single sided DC coupled strip detectors

Operating principles of a silicon strip detector were discussed in chapter 1.2.2. As presented in figure 1.16, the charge created by a high energy particle is laterally distributed across an area which typically covers two or three strip electrodes. Figure 1.16 also schematically presents the amplifier interface on early generation silicon strip detectors, also called DC (Direct Current) coupled silicon strip detectors.

On a DC coupled strip detector chip the strip shaped pn-junction anodes are directly connected to the inputs of the preamplifier electronics, hence the term DC coupled. The manufacturing process of a DC strip detector is very compact and basically only includes the manufacturing steps of the exemplary wafer process description given in chapter 1.3.

DC coupling between the strip diode pn-junction and the preamplifier results in that the dark current of the strip diode can only flow into the input circuit of the preamplifier. As presented in chapter 1.4., silicon strip detector preamplifier electronics will in this case integrate in parallel both the signal current and the dark current of the diode during the periods when feedback loop reset switch is open. Such arrangement is not optimal in case the signal charges generated by the traversing high energy particles and the accumulated charge due to the strip diode dark current are in the same order of magnitude.

A photograph of a DC coupled strip detector discussed in publication I is shown in figure 2.1. Interconnections from individual strip electrodes have been manufactured by aluminium wire wedge bonding. A special 12 ring guard-ring structure is implemented here to improve tolerance to high reverse bias voltages.

Typical dark current curve for one complete detector chip is presented in figure 2.2. The total, combined dark current of all strips has been measured from the detector bias voltage line.

Reference [28] presents results from a beam test performed on a this DC coupled strip detector utilizing the CERN SPS (Super Proton Synchrotron) accelerator in CERN North Area experimental facility. A very unique position resolution of 3.9 μm was achieved in this test.

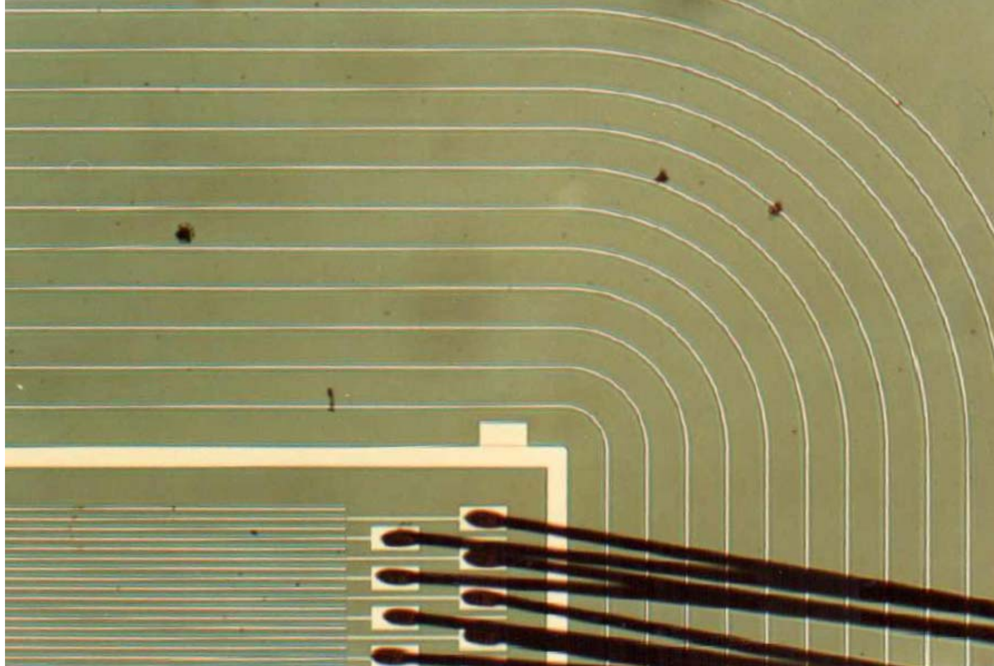

Figure 2.1: Photograph of the corner area of a DC coupled strip detector analysed in publication I. Outermost, thin rings are floating guard-ring structures. Wide metallization line is a biased guard ring structure. Bonding wires (black in photo) connect strip diodes into preamplifier electronics.

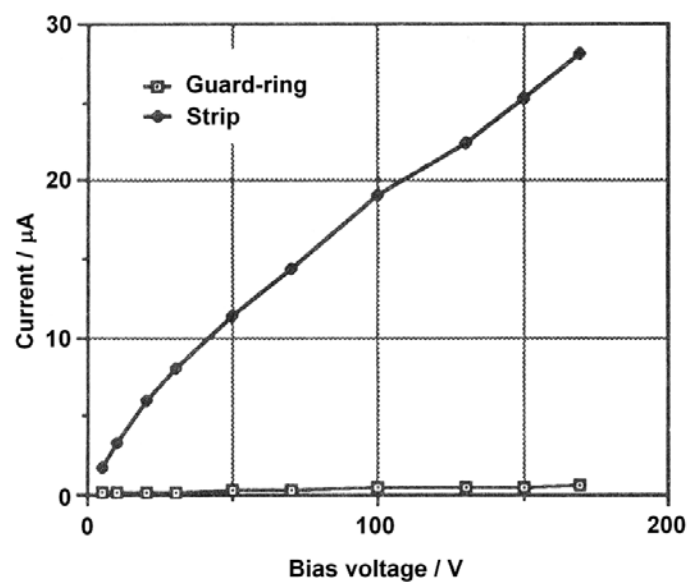

Figure 2.2: Typical dark current curves for strip electrodes and the wide, innermost guard-ring structure. Dark current is shown as a function of reverse bias voltage, from publication I.

2.2 Single sided AC coupled strip detectors

As discussed in chapter 2.1, the DC coupling between the strip detector diode elements and the preamplifier electronics results in integration of the dark current signal and the actual particle signal during the integration period of the preamplifier IC. Dark current will therefore also consume part of the dynamic range of the amplifier since dark current and signal current are summed at the feedback capacitor of the preamplifier circuit.

In order to improve the signal coupling between the strip detector chip and the preamplifiers, the concept of AC (Alternating Current) coupling has been implemented in later generation silicon strip detectors.

One possible implementation of the AC coupling has been presented in figure 2.3. In this strip and readout arrangement, only every second strip diode is connected to readout system. Signals reaching the intermediate strip without readout connection, will capacitively couple to the neighbouring chips which have the readout connection. The strip diode metallizations, which have an ohmic contact to the p type strip anodes in a DC coupled strip detector, are now isolated from them by a thin, thermal silicon dioxide. This results in a relatively large capacitance between the metallization and the p type strip. DC biasing of the p anodes is implemented by polysilicon resistors which are all connected to a common bias bus.

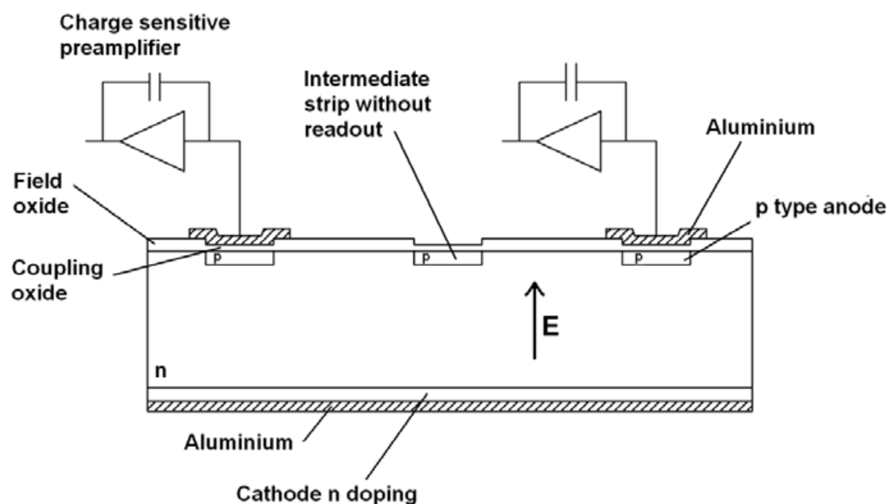

Figure 2.3: AC coupled silicon strip detector implementation with intermediate strips (no readout) and silicon dioxide capacitive coupling to strip metallizations. Polysilicon resistors utilized for p strip DC biasing are not presented.

AC coupling has proven a highly feasible method for improving the dynamic range and noise performance of the strip detector data acquisition system (DAS). Signal charge generated by a high energy particle traversing the strip detector is rapidly swept to the strip detector electrodes meaning that the corresponding high frequency current pulse is coupled effectively into the preamplifier feedback capacitor through the large strip coupling capacitor.

Figure 2.4 presents a photograph of the layout of an AC coupled strip detector which is the subject of publications II and III in this thesis.

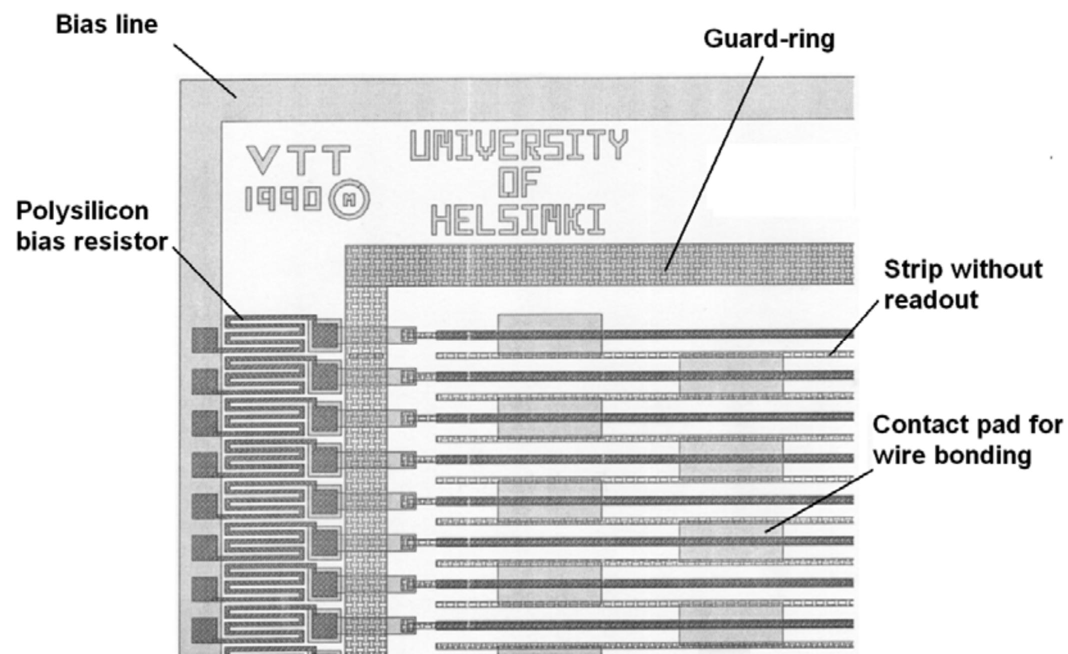

Figure 2.4: AC coupled silicon strip detector layout. Strip electrodes are connected to a common bias bus through zigzag polysilicon resistors. A guard ring structure surrounds the active area [24].

The AC coupled strip detector presented above has been tested utilizing a pion particle beam from the SPS accelerator at CERN. Detailed analysis of the test results is presented in publication III. The signal-to-noise ratio obtained in this test was 31 and MIP position measurement resolution was found to be 4.9 μm.

2.3 Double sided strip detectors

Chapter 1.1.1 shortly touched on the main limitation of strip detectors, the fact that in most implementations they are capable of recording the high energy charged particle trajectories only in one dimensions relative to the x-y plane of the strip detector. Extensive research has been performed on this subject in terms of more advanced designs intending to improve the situation and providing at least partial information also in the second, perpendicular direction.

Probably the most actively studied solution to this problem is the design and manufacturing of double sided strip detectors. In a double sided strip detector both the front and back surface of the detector chip are covered by strip shaped electrodes. Front surface electrodes are identical to those found on the AC coupled, single-sided strip detectors. Back side strips are in this case heavily doped n type strips on the n type wafer substrate.

Principal arrangement of the strip orientations on one double-sided, AC coupled strip detector design is shown in figure 2.5. Strip detectors typically have a rectangular shape where the length of the detector chip (side parallel to strips) is much larger than the width (perpendicular to the strips). A typical detector chip size may be 30 mm x 60 mm. In figure 2.5, p type strips are arranged along the larger dimension of the chip and placed parallel to the elementary particle beam in the collider experiment. P type strips are connected to preamplifier electronics at the ends of the strips, along the shorter dimension of the chip. Back side, n type strips are parallel to the p strips and therefore the ends of the strips are arranged on the longer edge of the chip.

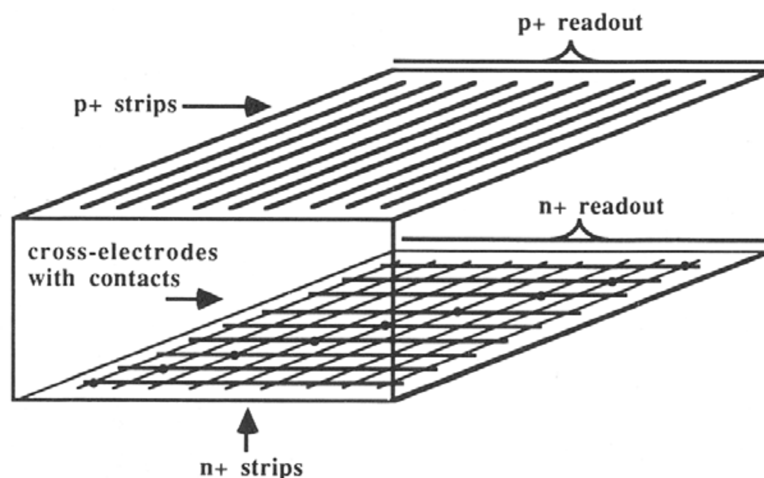

Figure 2.5: Principle design of a double-sided strip detector equipped with cross-electrodes for n type strip readout, from publication IV.

Figure 2.5 immediately reveals the first problem relating to the readout arrangement of double-sided silicon strip detectors. Strip detector chips are utilized in construction of barrel shaped tracker instruments, like the DELPHI Microvertex detector shown in figure 1.2. Strip detector chips are mechanically, and for signal readout, arranged into detector modules, where each strip detector chip should connect to readout electronics, or in the case of detector chip daisy-chaining, into other similar detector chips. Such arrangement is not possible unless all the electrical connections of the strip detector chips are arranged on the shorter edges of the chips. N type strip ends are therefore inherently on the wrong edge of the chip to enable such interconnections.

One possible solution to this problem is already presented in figure 2.5. This is to add on the n-side cross-electrodes which connect to the n type strips. If one cross-electrode connects to one n strip, each n strip may be provided with a preamplifier connection on the same edge of the chip where p type strips are connected. N type interconnections just need to be arranged to the back side of the chip in parallel with the front side p strip connections.

The next design characteristic which must be taken into account is that the chip is often not square, and assuming that the strip pitch is equal on front and back sides of the chip, there are much more n strips than p strips on the chips. With the exemplary chip dimensions of 30 mm x 60 mm there will be roughly a double number of n strips compared to p strips. Making a further justified assumption that the interconnection density and readout electronics must be same on both sides of the detector chip, one must conclude that it is not possible to arrange one cross-electrode and one dedicated preamplifier channel for each n type strip. A straightforward approach is to accept some ambiguity in the signal data from the n-side strips and connect each cross-electrode into two or ever more actual n type strips. Data processing and special algorithms in the tracker experiment level could then be developed to distinguish which n strip is the real origin of the signal seen in the cross-electrode.

From the manufacturing and wafer processing point of view there are also some additional requirements in order to manufacture well separated and properly functional n type strips. As described in chapter 1.3, the basic silicon dioxide SiO_2 passivation (FOX) utilized on both sides of the strip detector chip as the main passivation layer, will typically contain some fixed, positive charge. This charge will attract electrons into a thin silicon layer in the immediate vicinity of the silicon-SiO_2 interface. N type strip electrodes manufactured on the back side of the strip detector chip are of the same conductivity type as the n type wafer substrate. Therefore a special technique is required to isolate the n strips. In some experiments special p type separation strips, corresponding to CMOS channel stops, have been used [29]. Such additional strips decrease the achievable strip pitch on the n-side and increase n strip inter-strip capacitance and therefore noise.

Another solution for the n strip isolation is to use the readout metallizations, which are capacitively coupled from the n strips, also as MOS (Metal-Oxide-Semiconductor) field plates expelling the electrons which otherwise would accumulate in the silicon-SiO_2 interface as mentioned above.

A layout detail of such n-side strip design has been presented in figure 2.6.

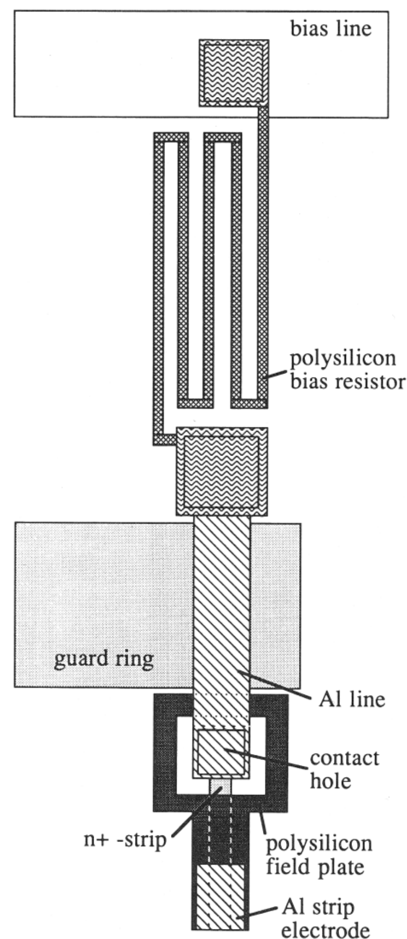

Figure 2.6: Design detail of the n strip end area on a double-sided, AC coupled silicon strip detector, from publication IV.

The metallized, AC coupled readout electrode illustrated in figure 2.6 is clearly wider than the actual n type strip electrode which is under it. The portion of the metal line which is overlapping with the region outside the actual n strip behaves like a MOS capacitor. It is desirable to maintain same reference voltage in all preamplifier

electronics which in practice means that all the n strip readout metallizations are also connected into a virtual DC voltage of a few volts maximum. If a sufficiently large, positive bias potential is now applied to the bias line of the n-side, nearly all of this voltage will appear between the n strip and the AC coupled metal line above it. Since the metallized readout line is in a much more negative potential than the n strip below it, the electron accumulation layer is effectively expelled from silicon-SiO_2 interface.

Another design detail, also clearly presented in figure 2.6 is the conductive polysilicon layer beneath the aluminium readout line. The polysilicon layer serves two purposes. Firstly, processing of polysilicon on the coupling oxide instead of using aluminium directly on it, reduces the probability of pinholes in the coupling oxide. Secondly, the polysilicon layer has been used in the n strip end regions as a lower conductor layer to form a field plate channel stop between the end of the n strip and the nearby, n type guard ring, see figure 2.6.

Some double-sided silicon strip detectors, including the design presented above, have been extensively tested in publication IV. In reference [30] the specific n-side strip isolation issues have been tested with a real high energy particle beam. Once again, the SPS accelerator was utilized on the West Area of the CERN facility. Strip detectors of various designs and two manufacturers were tested. With the strip detector designs including a substantial research contribution by the author, spatial resolutions of 3.8 μm (p-side) and 6.6 μm (n-side) were achieved for a pion particle beam traversing the detector chips in a direction perpendicular to the chip surface.

3 Silicon photodiode detectors for CT applications

The fundamentals of computed tomography (CT) application, principal construction of a CT scanner machine and the CT detector structure were all presented in chapter 1.1.2. In the same chapter, also the requirements of detector and CT detector chip development were presented relating to the need of producing CT instrumentation of wider, single-rotation coverage in human body imaging.

Out of the various solutions provided for the production of large area, edgeless silicon detector chips and detector modules, this chapter will focus on the through-wafer-interconnect (TWI) technology, which is the subject of publications VI and VII.

The basic nature of TWI manufacturing clearly differs from the conventional manufacturing steps applied in planar processing of silicon detector and photodiode chips. Manufacturing of TWIs will require extensive removal of silicon material from the starting wafers when the TWI cavities are etched to the wafer by one method or another. In addition, several more or less mechanical steps are typically required during the manufacturing of TWIs. Various grinding and Chemical Mechanical Polishing (CMP) steps are possible.

All these manufacturing steps are inherently very different from the processing steps of chapter 1.3 requiring ultimate mechanical and chemical purity. Intuitively, it is therefore desirable to completely separate, as much as possible, the TWI process from the pn detector manufacturing process in such a way that either one of the two is completed first and only then the other sub-process is started. With such arrangement, mixed utilization of individual manufacturing steps of very different nature can be avoided. Publications VI and VII discuss TWI research which has been conducted in order to develop a TWI-detector process fulfilling this goal. Due to commercial confidentiality reasons at the time of publication, publication VI does not specifically discuss CT applications although that was the sole driver of the research conducted for the TWIs.

An approach where TWIs are manufactured and completed first was chosen. Etching of the TWI cavities, isolation of the cavity inner surfaces and filling of the cavities were all processed before proceeding to the more-or-less standard manufacturing steps relating to the pn photo-detector electrodes. At the early stages of the research work, as described in publication VI, test chips only containing the critical TWI manufacturing steps and structures were manufactured. Figure 3.1 describes the basic process flow applied for such test chips.

Although many improvement ideas and needs were found during the early prototype manufacturing, the basic design and manufacturing approach was found to be feasible. In addition, further post-processing steps including solder bump bonding between the TWI test chips and an underlying ceramic substrate were successfully demonstrated.

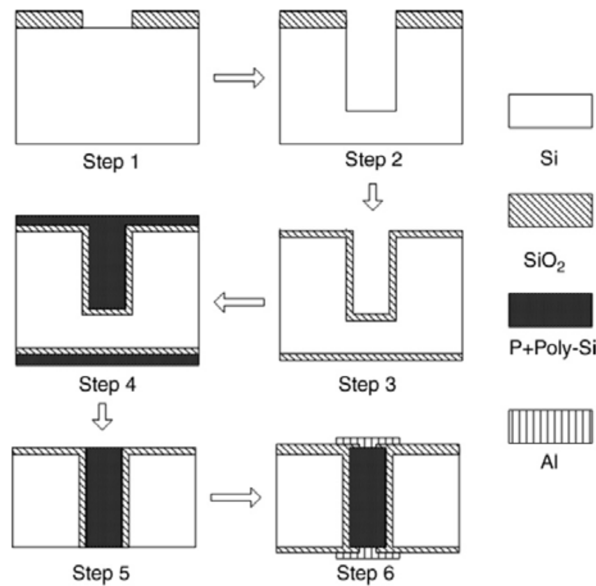

Figure 3.1: Principle process flow of TWI test chips, from publication VI

Encouraged by the promising results from TWI process development the research team continued into manufacturing detector chips with first actual CT oriented detector pn junctions on the same chips. The results of this further development are presented in publication VII.

Completely functional TWI-CT chips were manufactured and the photo-detection characteristics of such chips were little different from conventional CT detector chips. Despite somewhat larger element-to-element variations, the dark current behaviour of the TWI equipped diode elements were at a conventional level of approximately 2 pA at a 10 mV bias voltage. These first tests chips still suffered from TWI yield issues which were later studied and solved. The light response distribution from a 16 x 16 element test chip is presented in figure 3.2. Some of deviating channels may be addressed to imperfect TWIs but it should also be noted that the measurement was performed utilizing instrumentation intended for routine manufacturing control and not for precision measurements.

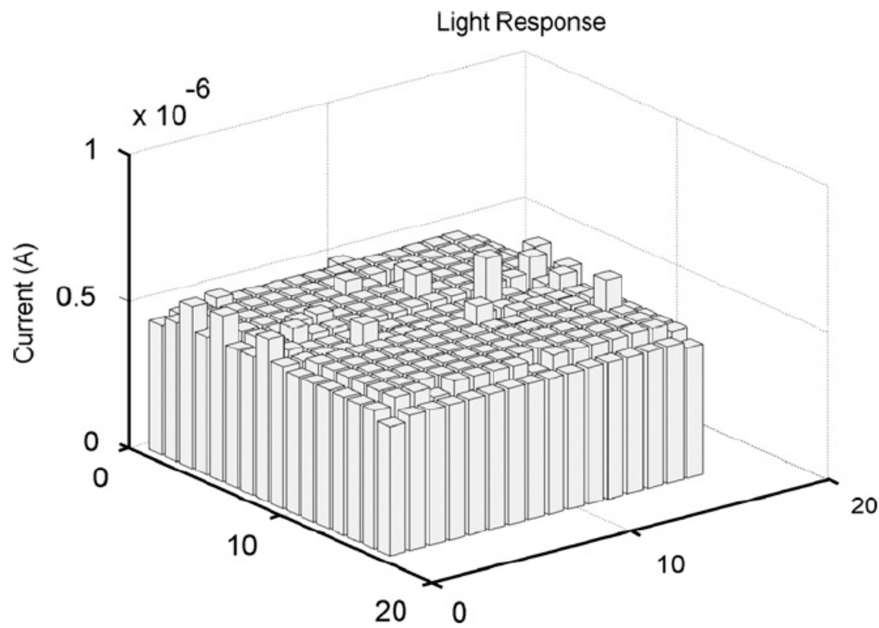

Figure 3.2: Light response distribution of a 16 x 16 element TWI-CT detector chip, from publication VII

Further research of TWIs for CT detector chips performed by the same research group is described in references [31, 32].

4 Conclusions

This thesis presents the research work carried out by the author in two inherently distinct application areas, namely in charged particle tracking relating to high energy physics research at scientific research centres like CERN, and in medical, Computed Tomography (CT) scanning.

The author has contributed to the research and development of novel, large area silicon radiation detector chips is both of these application areas. The thesis first presents these applications, and the theory, manufacturing methods and readout systems of such large area detectors.

In the second chapter results of author's research contribution relating to high energy physics strip detectors is presented. It has been shown that the strip detector chips have been successfully developed starting from early generation, DC coupled detectors all the way to the most sophisticated, double-sided, double-metal AC-coupled devices which still today present the most advanced type of strip detectors utilized. Results of rigorous testing of the developed detectors have been presented and it has been shown that they fulfil the expectations set from the application point of view. The static performance, in terms of dark current, capacitance and inter-strip characteristics, as well as the dynamic performance, i.e. response to actual high energy particles, have been shown to be very satisfactory as presented in the thesis publications I-V.

Third chapter of the thesis presents results of author's research contribution relating to development of through-wafer interconnects (TWIs) for large area CT detector chips.

As shown in publications VI and VII, TWI research relating to large area CT chips has been successfully performed and it been shown to produce prototype devices of satisfying performance from the medical CT application point of view. No unresolved challenges were encountered during this research and it is obvious that with further research and development a commercially viable cone beam CT detector system could be implemented.

References

[1] Kemmer, J. Fabrication of low noise silicon radiation detectors by the planar process. *Nuclear Instruments and Methods*, 169:499-502, 1980

[2] Kemmer, J. Improvement of detector fabrication by the planar process. *Nuclear Instruments and Methods*, 226:89-93, 1984

[3] CERN public website. http://public.web.cern.ch/public/

[4] DELPHI Collaboration. The DELPHI detector at LEP. *Nuclear Instruments and Methods in Physics Research A*, 303:233-276, 1991

[5] S. Myers and E. Picasso. The design, construction and commissioning of the CERN large Electron–Positron collider. *Contemporary Physics*, 31:387-403, 1990

[6] M. de Palma and CMS Collaboration. The CMS experiment at LHC. *Nuclear Physics B - Proceedings Supplements,* 61:32-38, 1998

[7] M. Benedikt, P. Collier, V. Mertens, J. Poole and K. Schindl. LHC Design Report. *CERN report*. CERN-2004-003-V-3, 2004

[8] Bingefors N. et al. The DELPHI Microvertex detector. *CERN Report*, CERN-PPE/92-173, 1992

[9] CERN Document Server. http://cdsweb.cern.ch/record/39141

[10] CERN Document Server. http://cdsweb.cern.ch/record/39186#03

[11] M. Krammer and CMS Collaboration. Operation and Performance of the CMS Silicon Tracker. CERN CMS Report, CMS-CR-2011-256, 2011

[12] CERN Document Server. http://cdsweb.cern.ch/record/39449

[13] A.M. Cormack. Representation of a function by its line integrals, with some radiological applications. *J. Appl. Phys*., 34-2722, 1963

[14] A.M. Cormack. Reconstruction of densities from their projection, with applications in radialogical physics. *Phys. Med. Biol*, 18 No 2, 1973

[15] R. Smith-Bindman at al. Radiation Dose Associated With Common Computed Tomography Examinations and the Associated Lifetime Attributable Risk of Cancer. *Arch. Intern. Med.*, 169(22):2078-2086, 2009

[16] Radon, J. Über die Bestimmung von Funktionen durch ihre Integralwerte längs gewisser Mannigfaltigkeiten. *Berichte über die Verhandlungen der Königlich Sächsischen Gesellschaft der Wissenschaften zu Leipzig*. Mathematisch-Physische Klasse 69, 262 - 277 (1917)

[17] Hsieh J. Computed tomography: principles, design, artifacts, and recent advances. *SPIE - The International Society for Optical Engineering*, 2003

[18] Nikl, M. Scintillation detectors for x-rays. *Meas. Sci. Technol.* 17, R37–R54, 2006

[19] R.P. Luhta et al. Back illuminated photodiodes for multislice CT, *Medical Imaging 2003: Physics of Medical Imaging*, 5030, 235-245, 2003

[20] R.P. Luhta et al. A new 2D-tiled detector for multislice CT, *Medical Imaging 2006: Physics of Medical Imaging*, 6142, 235-245, 2006

[21] Saito Y. et al. Large area 2-dimensional detector for real time 3-dimensional CT (4D-CT). *Medical Imaging 2001: Physics of Medical Imaging, Proceedings of SPIE* ,Vol. 4320:1605-7422, 2011

[22] F. Ji. Fully 2D tileable photodiode detector for medical computed tomography imaging, *Doctoral Dissertation, TKK Dissertations*, 187, 2009

[23] http://sales.hamamatsu.com/assets/pdf/parts_S/s3590-08_etc_kpin1052e08.pdf

[24] Leinonen K. Fabrication and characterization of silicon position sensitive particle detectors, *Acta Universitatis Lappeenrantaensis*, 235, 2006

[25] Anzivino G. First results frm a silicon-strip detector with VLSI readout, *Nuclear Instruments and Methods in Physics Research A*, 243:153-158, 1986

[26] Watanabe N. et al. Optical data transmission apparatus for transmitting a signal between a rotatable portion and fixed portion of an x-ray CT scanner, *United States Patent*, 5,336,897, 1994

[27] Texas Instruments Incorporated. 64-channel, Current-Input Analog-to-Digital Converter, *DDC264 data sheet*, http://www.ti.com/lit/ds/symlink/ddc264.pdf

[28] Hietanen I. et al. Beam test results of an ion-implanted silicon strip detector on a 100 mm wafer, *Nuclear Instruments and Methods in Physics Research A*, 305:173-176, 1991

[29] Batignani G. et al. Development and performance of double sided silicon strip detectors, *Nuclear Instruments and Methods in Physics Research A*, 305:173-176, 1991

ACTA UNIVERSITATIS LAPPEENRANTAENSIS

449. MYÖHÄNEN, KARI. Modelling of combustion and sorbent reactions in three-dimensional flow environment of a circulating fluidized bed furnace. 2011. Diss.

450. LAATIKAINEN, MARKKU. Modeling of electrolyte sorption – from phase equilibria to dynamic separation systems. 2011. Diss.

451. MIELONEN, JARI. Making Sense of Shared Leadership. A case study of leadership processes and practices without formal leadership structure in the team context. 2011. Diss.

452. PHAM, ANH TUAN. Sewage sludge electro-dewatering. 2011. Diss.

453. HENNALA, LEA. Kuulla vai kuunnella – käyttäjää osallistavan palveluinnovoinnin lähestymistavan haasteet julkisella sektorilla. 2011. Diss.

454. HEINIMÖ, JUSSI. Developing markets of energy biomass – local and global perspectives. 2011. Diss.

455. HUJALA, MAIJA. Structural dynamics in global pulp and paper industry. 2011. Diss.

456. KARVONEN, MATTI. Convergence in industry evolution. 2011. Diss.

457. KINNUNEN, TEEMU .Bag-of-features approach to unsupervised visual object categorisation. 2011. Diss.

458. RUUSKANEN, VESA. Design aspects of megawatt-range direct-driven permanent magnet wind generators. 2011. Diss.

459. WINTER, SUSANNA. Network effects: scale development and implications for new product performance. 2011. Diss.

460. JÄÄSKELÄINEN, ANSSI. Integrating user experience into early phases of software development. 2011. Diss.

461. KÄÄRIÄINEN, TOMMI. Polymer surface modification by atomic layer deposition. 2011. Diss.

462. KOCHURA, ALEKSEY. Growth, magnetic and transport properties of InSb and II-IV-As2 semiconductors doped with manganese. 2011. Diss.

463. PUTKIRANTA, ANTERO. Possibilities and challenges of longitudinal studies in operations management. 2011. Diss.

464. HAPPONEN, ARI. Muuttuvaan kysyntään sopeutuva varastonohjausmalli. 2011. Diss.

465. VASAVA, PARITOSH. Application of computational fluid dynamics in modelling blood flow in human thoracic aorta. 2011. Diss.

466. PURO, LIISA. Identification of extractives and polysaccharides as foulants in membrane filtration of pulp and paper mill effluents. 2011. Diss.

467. LAPPALAINEN, PIA. Socially Competent Leadership – predictors, impacts and skilling in engineering. 2012. Diss.

468. PLAMTHOTTATHIL, ANSHY OONNITTAN. Application of electrokinetic Fenton process for the remediation of soil contaminated with HCB. 2012. Diss.

469. EBRAHIMI, FATEMEH. Synthesis of percarboxylic acids in microreactor. 2012. Diss.

470. JANTUNEN, SAMI. Making sense of software product requirements. 2012. Diss.

471. VILKO, JYRI. Approaches to supply chain risk management: identification, analysis and control. 2012. Diss.

472. TANSKANEN, VESA. CFD modelling of direct contact condensation in suppression pools by applying condensation models of separated flow. 2012. Diss.

473. HUHTANEN MIKKO. Software for design of experiments and response modelling of cake filtration applications. 2012. Diss.

474. PARJANEN, SATU. Creating possibilities for collective creativity
Brokerage functions in practice-based innovation. 2012. Diss.

475. KUKKONEN, SAKU. Generalized differential evolution for global multi-objective optimization with constraints. 2012. Diss.

476. LAAKSONEN, JONNA. Tactile-proprioceptive robotic grasping. 2012. Diss.

477. KALLIO, ANNE. Enhancing absorptive capacity in a non-research and development context
An action research approach to converting individual observations into organizational awareness. 2012. Diss.

478. LÄTTILÄ, LAURI. Improving transportation and warehousing efficiency with simulation based decision support systems. 2012. Diss.

479. OYOMNO, WERE. Usable privacy preservation in mobile electronic personality. 2012. Diss.

480. LINNALA, MIKKO. Simulation and optimization tools in paper machine concept design. 2012. Diss.

481. KORPIJÄRVI, JUHA. Aging based maintenance and reinvestment scheduling of electric distribution network. 2012. Diss.

482. KORHONEN, JUHAMATTI. Active inverter output filtering methods. 2012. Diss.

483. KLODOWSKI, ADAM. Flexible multibody approach in bone strain estimation during physical activity: quantifying osteogenic potential. 2012. Diss.

484. VUORENMAA, MARKKU. Osaamisen johtaminen pk-yrityksen kansainvälisen kasvun elinkaarella. 2012. Diss.

485. RAUTIAINEN, MARITA. Dynamic ownership in family business systems – a portfolio business approach. 2012. Diss.

486. LILIUS, REIJO. THE FINNISH IT INDUSTRIES IN TRANSITION Defining and measuring the Finnish software product and IT services industries by applying theoretical frameworks . 2012. Diss.

487. TUOMINEN, PASI. The purpose of consumer co-operation: implications for the management and governance of co-operatives. 2012. Diss.

488. SAARI, ESA. Suurnopeus-turbokoneroottoreiden termodynaaminen ja mekaaninen mallinnus sekä rakenneanalyysi. 2012. Diss.

489. PAANANEN, MIKKO. On innovative search: the use of internal and external sources of innovation among Finnish innovators. 2012. Diss.

490. BELOVA, POLINA. Quasiclassical approach to the vortex state in iron-based superconductors. 2012. Diss.