Lappeenranta University of Technology
Faculty of Technology
Degree Program in Electrical Engineering

MASTER'S THESIS

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Study of Control Methods of a High-Frequency Cycloconverter for Domestic Induction Heating Appliances

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December 3, 2014

ABSTRACT

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Master's Thesis

38 pages, 19 figures, 2 tables, 0 appendices

Examiners: Prof. Pertti Silventoinen
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Keywords: cycloconverter, high-frequency, induction heating

A high-frequency cyclonverter acts as a direct ac-to-ac power converter circuit that does not require a diode bidge rectifier. Bridgeless topology makes it possible to remove forward voltage drop losses that are present in a diode bridge. In addition, the on-state losses can be reduced to 1.5 times the on-state resistance of switches in half-bridge operation of the cycloconverter.

A high-frequency cycloconverter is reviewed and the charging effect of the dc-capacitors in "back-to-back" or synchronous mode operation operation is analyzed. In addition, a control method is introduced for regulating dc-voltage of the ac-side capacitors in synchronous operation mode. The controller regulates the dc-capacitors and prevents switches from reaching overvoltage level. This can be accomplished by variating phase-shift between the upper and the lower gate signals. By adding phase-shift between the gate signal pairs, the charge stored in the energy storage capacitors can be discharged through the resonant load and substantially, the output resonant current amplitude can be improved.

The above goals are analyzed and illustrated with simulation. Theory is supported with practical measurements where the proposed control method is implemented in an FPGA device and tested with a high-frequency cycloconverter using super-junction power MOSFETs as switching devices.

TIIVISTELMÄ

Lappeenrannan teknillinen yliopisto
Teknillinen tiedekunta
Sähkötekniikan koulutusohjelma

Jouni Tynkkynen

Syklokonvertterin ohjausmenetelmien tutkiminen

Diplomityö

38 sivua, 19 kuvaa, 2 taulukkoa, 0 liitettä

Examiners: Prof. Pertti Silventoinen
TkT. Juhamatti Korhonen

Keywords: syklokonvertteri, induktiokuumennus

Korkeataajuus syklokonvertteri toimii ac-ac teholähteenä, joka ei hyödynnä diodisiltaa. Sillaton topologia mahdollistaa kokonaan diodisillan jännitehäviöiden vähentämisen. Syklokonvertterin käyttö mahdollistaa, jopa johtumishäviöiden vähentämisen puolitoistakertaisen kytkinlaitteen muodostamiin häviöihin.

Diplomityössä tutkitaan korkeataajuus syklokonvertterin tasajännitteen muodostumista, kun konvertteria operoidaan back-to-back (synkroonisessa) moodissa. Tämän lisäksi esitetään säätäjä, joka rajoittaa tulopuolen kondensaattoreiden jännitteen nousun estäen ylijännitteen muodostumisen. Säätäjän toiminta perustuu kytkinparien vaihe-eron säätelyyn. Vaihe-eroa säätämällä, voidaan tulopuolen kondensaattoreiden tasajännite purkaa kuormaan ja samalla kasvattaa resonanssivirran amplitudia.

Yllä olevat tavoitteet analysoidaan ja esitetään simuloimalla. Teoriaosiuutta tukee käytännön mittaukset, missä esitetty säätäjän logiikka toteutetaan FPGA laitteelle ja käytännön mittaukset suoritetaan syklokonvertterilla käyttäen teho MOSFETteja kytkiminä.

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List of Symbols and Abbreviations

Abbreviation	Meaning
RMS	root mean square
HF	high-frequency
IH	induction heating
I	current, root mean square (RMS)
U	voltage, root mean square (RMS)
L_r	inductance of resonant load
C_r	capacitance of resonant load
R_r	resistance of resonant load
f_r	resonance frequency
f_sw	switching frequency

1 INTRODUCTION

Induction heating is a commonly used method in many heating applications ranging from domestic to industrial applications. Domestic applications have become increasingly more popular. High-efficiency, safety, precise control, low pollution and quick warming are one of the key factors in domestic induction heating applications. An induction heating setup consists of a workpiece, usually a planar turn winding, that is placed below a metallic a vessel. High-efficiency is guaranteed, since the heat is directly generated in a metallic vessel instead of transferring heat through planar surfaces. The workpiece is supplied by medium to high-frequency power source, frequency typically ranging from 20 kHz to 100 kHz. Since the switching frequency needs to be in high-frequency range, a small conduction loss of power switches is mandatory for achieving high-efficiency power conversion. [1]–[3]

The on-state power loss is mainly caused by on-state resistance of a power switch. Naturally this would be selected as small as possible to reduce on-state losses. One attractive choice is to choose a super-junction MOSFET as a switching device. SJ-MOSFET has a very low on-state resistance at relatively high breakdown voltage, as an example, 18 mΩ at 170 A and 300 V breakdown voltage (IXFB170N30). As the development of semiconductor switches continue, further decrease in on-state resistance is expected. [3]–[5]

In high-frequency inverter operation it is possible to reduce on-state power losses to almost equal or less than on-state power losses in a front-end diode bridge rectifier. As a result, bridge-less circuit topology has been proposed to remove conventional diode rectifiers from a conversion circuit. Secondly, it is also possible to achieve bi-directional switching by connecting two reverse-blocking IGBTs (RB-IGBT) in anti-parallel. On-state power losses can be reduced compared to a series connection of two conventional IGBTs with anti-parallel diode connected against each other. This technique has been utilized for example in matrix converters and ac-to-ac chopper circuits to reduce power losses with the lack of a diode bridge rectifier. Direct ac-to-ac conversion circuits are attractive not only for motor drive systems but also for induction heating applications. [1], [3]

High-frequency cycloconverter as shown in Figure 1(d) is a direct ac-to-ac power conversion circuit. The use of this topology has been discussed on [6] to convert high-frequency input to low-frequency output in PV applications. In the PV application, it is relatively easy to control low-frequency output voltage or power, since the input voltage in this is higher than the output voltage. In induction heating, low-frequency ac is converted to high-frequency ac, which brings challenges in regulating the dc-capacitors and output current amplitude. Cycloconverter excludes the diode-bridge rectifier and thus, provides smaller total device drop compared to conventional bi-directional-switch topologies. In

addition to this, it does not require bulky electrolytic capacitor for smoothing purposes. [6]

1.1 Goals and Scope

A high-frequency cycloconverter is reviewed and the charging effect of the dc-capacitors in "back-to-back" or synchronous mode operation is analyzed. In addition, a control method is introduced for regulating dc-voltage of the ac-side capacitors in synchronous operation mode. The controller regulates the DC-capacitors and prevents switches from reaching overvoltage level. This can be accomplished by variating phase-shift between the upper and the lower gate signals. By adding phase-shift between the gate signal pairs, the charge stored in the energy storage capacitors can be discharged through the resonant load and substantially, the output resonant current amplitude can be improved.

DC-capacitor voltages v_{C1} and v_{C2} are regulated so that their voltage stays positive relative to ac-main voltage to prevent capacitors from discharging through the anti-parallel diodes of the MOSFETs. However, the controller does not remove the existing dc-bias of the dc-capacitors and rather just prevents it from reaching overvoltage levels.

The above goals are analyzed and illustrated with simulation. Theory is supported with practical measurements where the proposed control method is implemented in an FPGA device and tested with a high-frequency cycloconverter using super-junction power MOSFETs as switching devices.

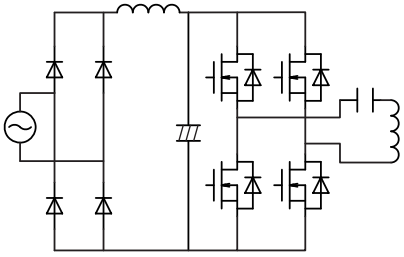
2 Literature Review

2.1 Conventional Induction Heating Topologies

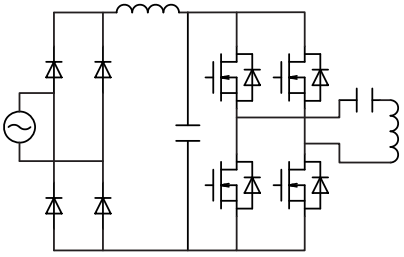
Figure 1 shows three conventional power converter topologies used in induction heating applications. In all of the circuit topologies of Figures (a) to (c) a diode-bridge rectifier is used to convert low-frequency ac to dc-voltage and a full-bridge inverter is used to convert dc-voltage to high-frequency ac-voltage for the resonant load. To operate under zero-voltage switching conditions, the switching frequency is selected higher than the resonant frequency of load. This results in a great reduction of switching power losses, switching stresses and EMI. The electrolytic capacitor is installed to smooth the rectified voltage and to keep resonant current amplitude at constant level. The electrolytic capacitor has to be selected rather big as the signal to be filtered is low-frequency ac. This results in highly distorted current caused by the charging and discharging of the capacitor. Moreover, the electrolytic capacitors offer high energy densities, but suffer from poor long-term failure rates. [2], [3], [7]

The circuit of Figure 1(b) is same as circuit (a) except the bulky electrolytic capacitor is replaced by a small film capacitor. The small capacitor acts as low impedance path for the resonant current and thus, can eliminate distortion from ac-main. However the dc-link voltage and the amplitude of high-frequency output voltage fluctuates at a frequency twice times the ac-main frequency. This might lead to acoustic noise due to electromagnetic force between the working coil and the workpiece to be heated. [2], [3], [7]

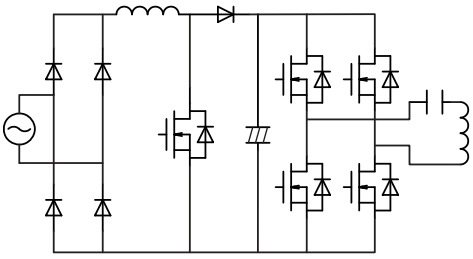
Figure 1(c) shows a popular circuit utilizing a power factor correction (PFC) circuit between the diode bridge rectifier and the inverter. The PFC controller controls the input current by switching the MOSFET on and off. This requires a relatively large electrolytic capacitor to smooth the dc-link voltage distorted by the PFC-circuit. Furthermore, the PFC-circuit requires additional components to meet soft-switching requirements. The PFC circuit also causes additional power losses because high-frequency PWM-signal is applied across the filter inductor. [8]



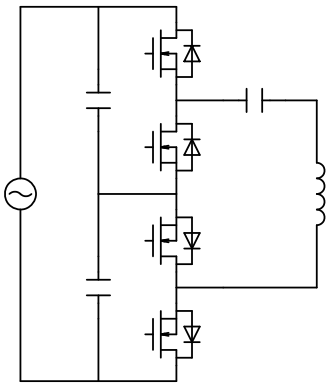
(a) Conventional circuit of an induction heater.



(b) Circuit configuration without a smoothing capacitor.



(c) Circuit configuration of with a PFC circuit.



(d) High-frequency cycloconverter.

Figure 1: Conventional induction heater circuit topologies.

2.2 The Cycloconverter Topology

Figure 1(d) shows the circuit configuration of the high-frequency cycloconverter. The cycloconverter consists of two voltage-source half-bridge inverters. The ac-side consists of two dc-capacitor connected in series. The midpoint of the dc-capacitors is connected between the half-bridge inverters. A series resonant induction heating load is connected to the output terminals of the half-bridge inverters. The ac-main terminals of the inverters are connected to the dc-capacitors. [6]

By eliminating the diode-drops and by operating under zero-voltage switching the cycloconverter expects high-efficiency compared to conventional topologies. Moreover, the performance of this topology continues to improve, as the development of the semiconductor devices allows decrease of the on-state resistance. [6]

The cycloconverter can reduce conduction loss to 1.5 times the on-state resistance of switches as one of the half-bridge inverters is working any given time and the opposite switches are turned on. The back-to-back operated cycloconverter has a slightly higher conduction loss of 2 times the on-state resistance but it still offers great reduction in conduction losses compared to conventional high-frequency power supplies. [6]

2.3 Cross-Signal Operation of The Cycloconverter

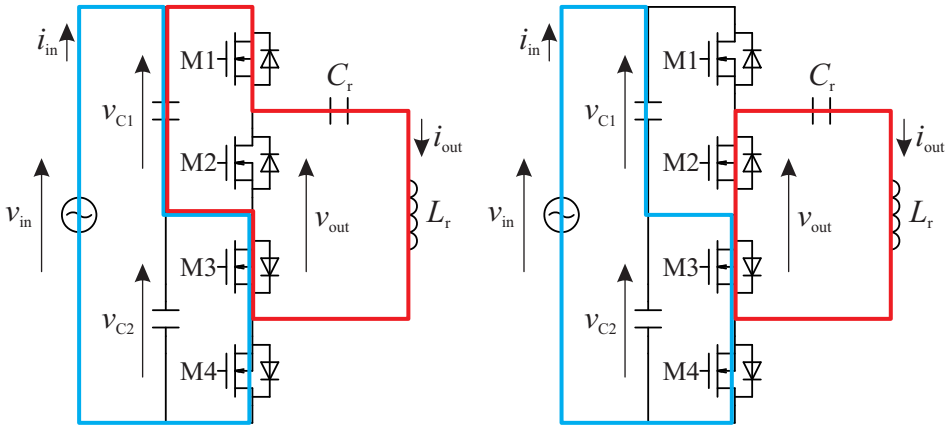
Reference [6] has introduced a control method where only one of the half-bridges is operated at any given time. Figure 2 presents the operating principle of the cycloconverter during cross-gate signal and positive ac-main cycle. As Figure 2(a) illustrates, during switching mode 1, switches M1 and M3 are turned on. The resonant current i_{out} flows through M1, C_1 and M3 during mode 1. The source current i_s continuously circulates through the capacitor C_1 and the body-diodes of M3 and M4. When the resonant current i_{out} is positive, the capacitor C_1 is discharged by i_{out}. The switching mode is changed from mode 1 to mode 2 before the direction of i_{out} changes. This current cannot charge or discharge the capacitor C_2, because the body-diodes are conducting and therefore, the capacitor voltage v_{C2} stays close to zero voltage.

Figure 2(b) shows current paths during switching mode 2 where switches M2 and M4 are in conduction mode. The ac-side current i_s flows through the same path as in mode 1. In mode 2, the positive resonant current charges the dc-capacitor C_2 during a short time period. After that, the direction of the resonant current changes to negative, and substantially discharging the dc-capacitor C_2. Notice that the resonant current flows through the body-diode of M3, since no gate signal is provided for M3. The anti-parallel diode of M3 stays on-state, as the input current flows through the body-diode.

Zero-voltage switching can be achieved in this operating mode. However, at the turn-off of switches M1 and M3 during positive input voltage, the anti-parallel diodes of M3 and M4 may cause reverse recovery current when dc-capacitor C_2 is discharged to zero voltage. The anti-parallel diode in M3 is in conduction mode even when M1 and M3 are turned off, since ac-main current is flowing. As a result, by turning on M4, reverse recovery current may flow through the anti-parallel diodes and cause current ringing by discharging the negative charge stored in C_2. The reverse recovery current does not cause significant switching losses as the capacitor voltage stays almost zero. As no gate signal is provided for M4, the dc-current flowing through the M4's anti-parallel diode causes significant on-state loss. [9]

To further improve the efficiency of the converter, another switching operation by using a state machine has been discussed in [6]. The principle of this operation is to keep lower MOSFETs (M3 and M4) on-state while input voltage is positive and upper MOSFETs M1 and M2 on-state while input voltage is negative. Switching losses will be reduced due to smaller on-state resistance of the MOSFETs compared to resistance of the intrinsic body diodes.

Since C_2 stays close to zero voltage during the operation, a high-frequency voltage pulse with the amplitude of input voltage is applied to resonant load. The output voltage cor-



(a) Current loops of mode 1.

(b) Current loops of mode 2.

Figure 2: Current loops in cross-switching operation.

responds to v_s during mode 1 and zero during mode 2. The dc-link voltage and the amplitude of the high-frequency output voltage are fluctuated at the twice of the ac main frequency. The amplitude fluctuation may cause an acoustic noise due to electromagnetic force between the working coil and the workpiece to be heated. For this reason, the cross-switching operation is limited only to low-power industrial induction heaters. [2]

3 Charging Effect of The DC-Capacitors

3.1 Operation in Synchronous Mode

DC-capacitors are charged up during synchronous mode operation which might result in overvoltage if the dc-bias of the capacitors is allowed to increase without regulating it. Moreover, synchronous mode operation allows the cycloconverter's dc-capacitors to be used as an energy storage for charging energy that can be discharged to load. This gives the possibility to regulate the capacitor voltages as well as grow the resonant current amplitude around ac-main voltage crossovers and hence, improve power flow to load.

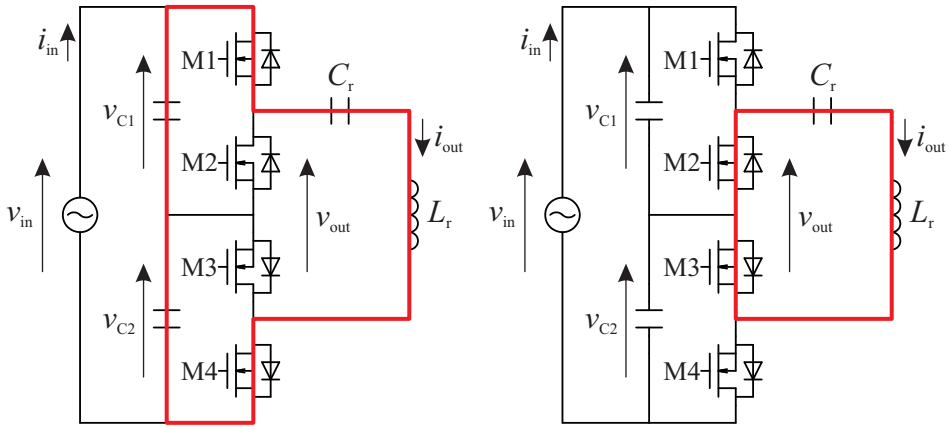
The synchronous operation can be described with the four switching modes shown in Figure 3. The corresponding gate signals and output voltage v_{out} are listed in Table 1. The "on"-state corresponds to a state when gate is turned on or when its intrinsic body-diode is conducting. Synchronous mode operation is based on modes 1 & 2 where as modes 3 & 4 appear as short period between the transition from mode 1 to mode 2 as well as mode 2 to mode 1. The control circuit provides gate signal pulses by alternatively selecting mode 1 and mode 2. The output voltage depends on the active switching mode as shown in the Table 1. The low output voltage corresponds to low voltage level as the resonant load is shorted through switches M2 and M3. Figure 3 is drawn for positive ac-main voltage v_{s} and current i_{s}. In case of negative ac-main voltage, the current loop are same except the direction of currents and the polarity of voltages are reversed.

The input current can be considered not to contain harmonic content as the ac-side capacitors C_1 and C_2 provide a low-impedance path for resonant current and the ac-side inductor L_{s} works as low-pass filter preventing resonant current from flowing through ac-main [10]. The resonant current loops are drawn with red lines.

Figure 3(a) correspond to switching mode 1, where switches M1 and M4 are in conduction mode. This results output voltage $v_{\text{out}} = v_{\text{s}}$. The resonant current has a path through switches M1, M4 and both capacitors C_1 and C_2. The input current i_{s} continuously flows through both capacitors. However, the capacitors are not charged or discharged by resonant or input current during this mode.

Table 1: All possible operating modes of the cycloconverter. The "on"-state corresponds to a state when gate is turned on or when its intrinsic body-diode is conducting.

Switch	**M1**	**M2**	**M3**	**M4**	v_{out}
Mode 1	ON	OFF	OFF	ON	v_{in}
Mode 2	OFF	ON	ON	OFF	≈ 0
Mode 3	ON	OFF	ON	OFF	v_{C1}
Mode 4	OFF	ON	OFF	ON	v_{C2}



(a) Mode 1 **(b)** Mode 2

(c) Mode 3 **(d)** Mode 4

Figure 3: Four possible operating modes of the cycloconverter.

The operation during mode 2 is presented on Figure 3(b). Here switches M2 and M3 are turned on, which corresponds to almost zero output voltage as the switches short-circuit the load and the current flows through the on-state resistances of switches M2 and M3. The input current i_s continuously flows through both capacitors C_1 and C_2, without charging the capacitors.

Figure 3(c) illustrates the operating principle during mode 3 where switch M1 and the body-diode of M3 are in conduction mode. The body-diode of M3 is turned on after completion of mode 1, since the resonant current is flowing positive direction and thus, resulting in synchronous rectification. The output voltage corresponds to v_{C1}, as the capacitor C_1 is connected to load. The resonant current flows through M1, the body-diode of M3 and the upper capacitor C_1. The capacitor C_1 is charged or discharged depending on the direction of resonant current.

The operation of mode 4 is illustrated in Figure 3(d) where switched M2 and M4 are conducting. Here the resonant current flows through M4, the body-diode of M2 and the

capacitor C_2. The mode 4 appears after mode 1, since synchronous rectification turns on the body-diode in M2. The capacitor C_2 is charged or discharged depending on the direction of the resonant current.

3.2 The Effect of Dead-Time

Figure 4 shows the charging curves of energy storage capacitors during synchronous operation simulated with PSCAD software. The blanking time (dead-time) and the size of ac-side capacitors used in the simulation are exaggerated for better illustration. The charging curves remind a rising exponent curve without considering the low-frequency (50 Hz) component. The capacitor voltages can quickly reach destructive levels that can lead to destruction of the power switches.

Figure 4 also shows charging curves of the midpoint voltage for various ac-main voltages. Higher input voltage results in faster charging, i.e. smaller rise-time and higher overvoltage. The dc-voltage of the capacitors reaches its maximum voltage level after a certain time. The steady-state voltage is above breakdown voltage levels even with low input voltages and therefore, the capacitor voltages have to be regulated to low levels.

Figure 5 shows close-up waveforms of the voltage transients during dead-time. The voltage is drawn here as an arithmetic sum of the capacitor voltages as shown in Figure 4 ear-

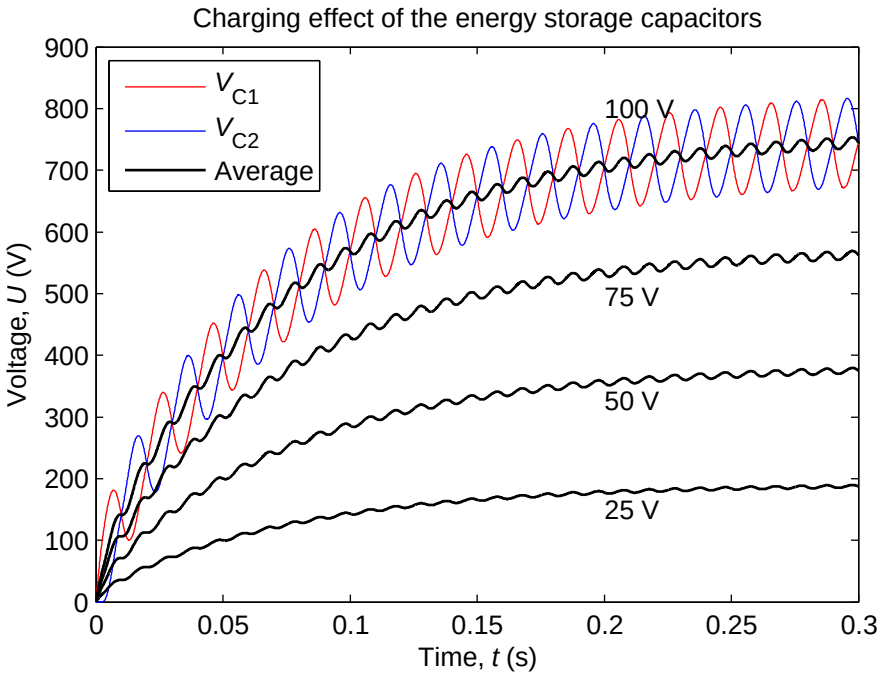


Figure 4: Simulated dc-capacitor voltage waveforms during synchronous mode operation and zero phase-shift angle with various input voltages.

lier and can be denoted as middle point voltage $v_{\text{mid}} = \frac{1}{2}(v_{C1} + v_{C2})$, since it is common to both signals. We can also notice that the duration of the transient is small compared to change in midpoint voltage. Figure 5 also illustrates that the midpoint voltage v_{mid} is preserved during mode 3 when switches M1 and M4 are turned on, as well as, during mode 4 when M2 and M3 are kept on.

By keeping dead-time as small as possible we can increase charging time of the dc-capacitors and gain more margin for voltage regulation. If we increase frequency while keeping dead-time constant we include more voltage transients per ac-main cycle, thus resulting in shorter risetime. Quality factor Q has an effect on how close resonant current is to zero-axis when switching occurs. Higher quality factor results in closer zero-current switching, thus decreasing the voltage transients and increasing risetime.

Figure 3 shows simplified resonant current circuits drawn for each mode. During mode 1 as shown in Figure 6(a), the resonant current flows through both of the ac-side capacitors and switches M1 and M4. Since the current flows through both of the capacitors having opposite charge to each other that the net charge is zero and there is no change in mid-point voltage. The total resonant capacitance of resonant current path is formed by the series capacitance of C_1, C_2 and C_{r}.

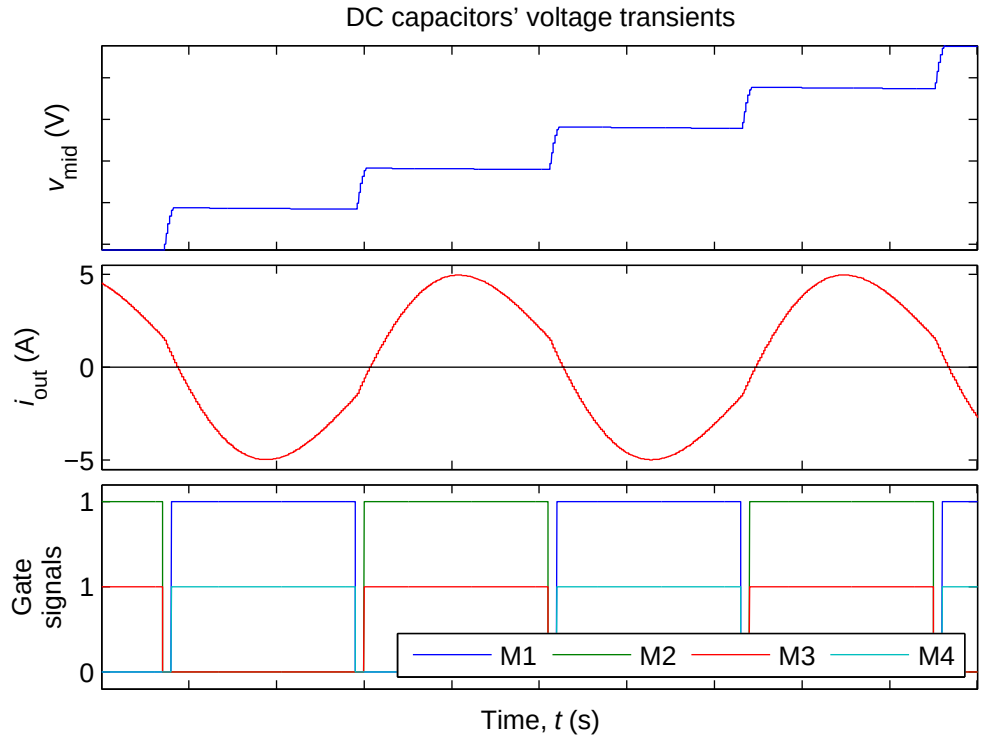
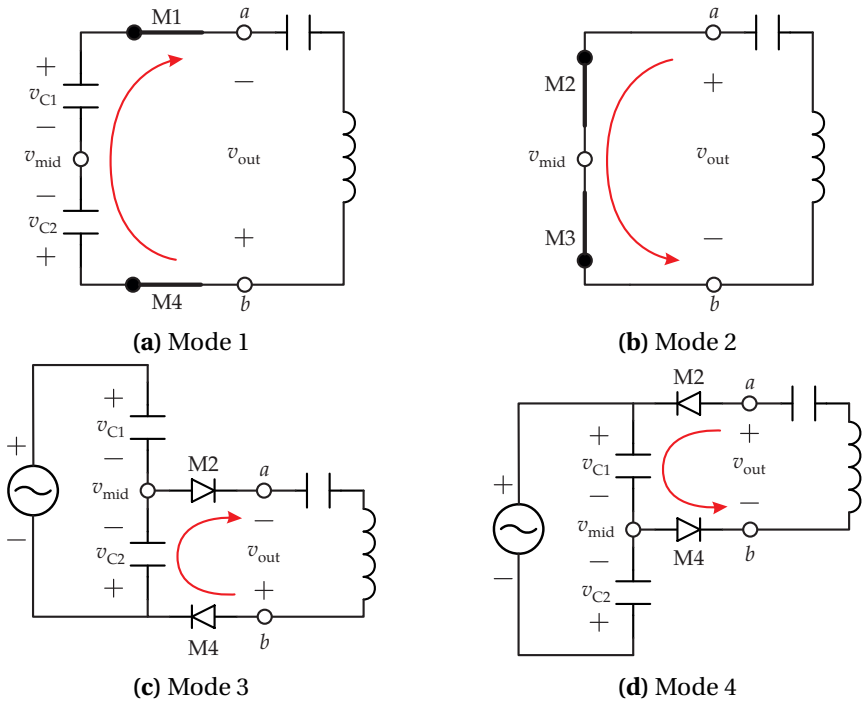


Figure 5: Simulated close-up waveform showing voltage transients of the midpoint voltage during dead-time.



(a) Mode 1 **(b)** Mode 2

(c) Mode 3 **(d)** Mode 4

Figure 6: Simplified resonant circuits of the operating modes.

In mode 2 as illustrated in Figure 6b, the resonant current flows through M2 and M3 and no resonant current flows through the dc-capacitors. As the polarity of v_{C1} and v_{C2} is opposite to each other, the net charge results in zero and there is no change in midpoint voltage. In this mode the resonant capacitance is formed by C_r and results in the highest resonant frequency.

During mode 3 as shown in Figure 6(c), the resonant current flows through C_2 and the body-diodes of M2 and M4 while charging C_2 in polarity shown in the figure. The direction of resonant current makes the midpoint voltage v_{mid} to drop relative to the negative bus of ac-main. A charge can be stored and the midpoint voltage can be preserved, since resonant current flows through C_2 until mode 3 is changed to mode 1 by switching on M2 & M3. We can also notice that characteristic resonant frequency f_r is different because the capacitor C_2 is included in the resonant circuit during this period and the total capacitance is formed by the series capacitance of C_r and C_2.

During mode 4 as illustrated in Figure 6d, the resonant current flows through C_1 and the anti-parallel diodes of M2 & M4. Similarly, charging of C_1 causes a voltage polarity that is opposite to the polarity of C_2. This means that negative net charge is stored in C_2 that causes its voltage to be negative relative to negative bus of ac-main. The total resonant capacitance in mode 4 is the series capacitance of C_r and C_1.

In conclusion we can write the total resonant capacitance of each mode as following:

$$C_{\mathrm{m1}} = \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_{\mathrm{r}}}\right)^{-1} \tag{3.1}$$

$$C_{\mathrm{m2}} = C_{\mathrm{r}} \tag{3.2}$$

$$C_{\mathrm{m3}} = \left(\frac{1}{C_2} + \frac{1}{C_{\mathrm{r}}}\right)^{-1} \tag{3.3}$$

$$C_{\mathrm{m4}} = \left(\frac{1}{C_1} + \frac{1}{C_{\mathrm{r}}}\right)^{-1} . \tag{3.4}$$

We can see that the total capacitance is highest during mode 2 and lowest in mode 1 where all capacitors are in series. The resonant capacitance $C_{\mathrm{m1}} = C_{\mathrm{m2}}$ (assuming $C_1 = C_2$) is between the capacitance of modes 3 and 4. In synchronous operation we are mainly using modes 1–2 and modes 3–4 appear for a short time period (dead-time) in between the modes 1–2. This means that the capacitance C_1 is removed from the resonant circuit after mode 1 is finished and after that, C_2 is removed before mode 2 begins. After mode 2 ends, the capacitance C_1 is included during dead-time and after that C_2 is also included before mode 1 starts again.

Since a pulse signal is applied to the switches, the operating modes are followed by each other in following repetitive order: mode 3, mode 1, mode 4, mode 2, thereby making the capacitor charging effect a continuous process. The polarity of the dc-capacitor voltages has to be opposite to the anti-parallel diodes to prevent short-circuit. This assures that the charge is preserved. Since the dc-capacitors can preserve the charge, the midpoint voltage continues to rise during operation.

The change in the capacitance of the resonant circuit changes the resonant frequency. The angular frequency ω_{r} of a series resonance circuit is given by

$$\omega_{\mathrm{r}} = \frac{1}{\sqrt{LC}} , \tag{3.5}$$

where L and C is the inductance and capacitance of the resonant load. As the equations (3.1)–(3.4) show, C corresponds to C_{r} only in mode 4. The resonant angular frequency for modes 1–3 is different and can be denoted as ω_1, ω_2 and ω_3 respectively.

If there is a change in resonant capacitance, then the change of resonant angular frequency can be conducted as following:

$$\frac{\omega_i - \omega_{\mathrm{r}}}{\omega_{\mathrm{r}}} = \sqrt{1 + \frac{C_{\mathrm{r}}}{C_{\mathrm{m}i}}} - 1, \tag{3.6}$$

where ω_i and C_{mi} are the angular frequency and the total capacitance of the corresponding switching mode.

According to equation (3.6), if the size of C_1 and C_2 is chosen hundred times C_r, then the change in angular frequency during modes 1–2 is 0.5% smaller compared to resonant frequency ω_r. Furthermore, in mode 3 the angular frequency ω_3 would result 1% smaller than resonant frequency ω_r. If the dc-capacitors are selected as high, we can ensure that the resonant frequency fluctuation stays small during operation.

3.3 The Effect of Phase-Shift

Figure 7 shows simulated output waveforms and dc-capacitor voltages of a resonant cycle during positive ac-main voltage and current. Gate signal pairs M1–M2 and M3–M4 are shifted by a phase-shift time. Since phase-shift is adjusted longer than the dead-time of switches, the resonant current amplitude can be improved during ac-main voltage crossover by discharging C_1 for positive resonant current and C_2 for negative resonant current. The resonant current deviates significantly from a sinusoidal waveform since it includes higher frequency components as resonant current is changed rapidly in a short time period.

M1 is turned off before positive resonant current goes to zero and as a result v_{C2} appears as output, since M4 is still conducting and the anti-parallel diode of M2 is turned on as control signal from M1 is removed. As a result, C_2 is charged by resonant current when i_{out} is positive and discharged otherwise. Notice that the lagging dead-time has no effect on the output characteristic. When M4 is turned of, the body-diode starts to conduct until M3 is turned on.

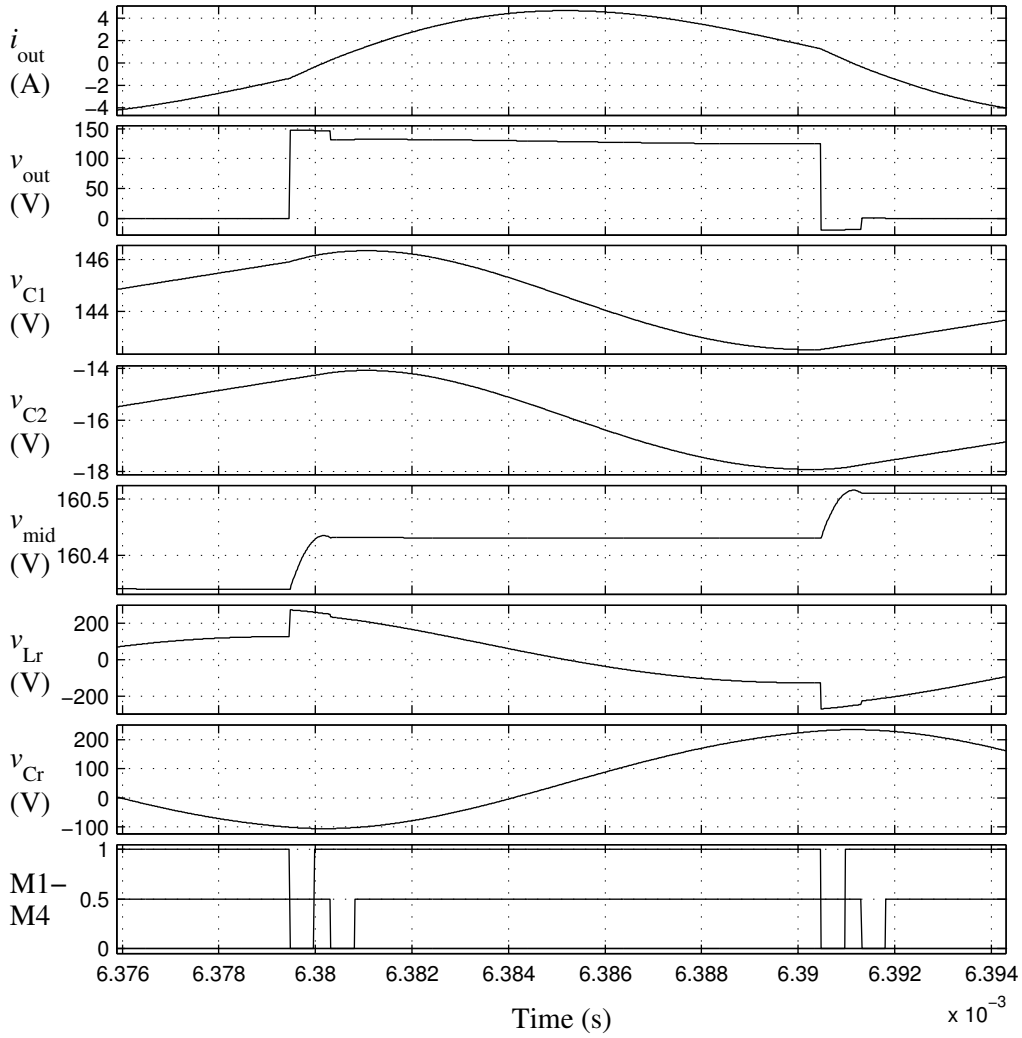


Figure 7: Simulated waveforms of a resonant cycle showing the discharge of dc-capacitors C_1 and C_2 for improving output current amplitude during positive ac main cycle.

3.4 Steady-State DC-Voltage

Figure 8 shows midpoint voltage v_{mid} at steady-steady value. The midpoint voltage has a rising transient and decreasing transient. If the resonant current is centered at its crossover point, the voltage transients are equal and change in the midpoint voltage is almost zero after the completion of phase-shift time.

When M1 is turned off, resonant current flows through the body-diode of M2 and M4. As the resonant current is positive at $t = t_1$, the capacitor C_2 is charged by resonant current when $i_r > i_s$. At time instant $t = t_2$, the current through $i_{C2} = i_s$ because M2 and M3 are turned on and no resonant current flows through C_2, substantially forcing midpoint voltage to decrease.

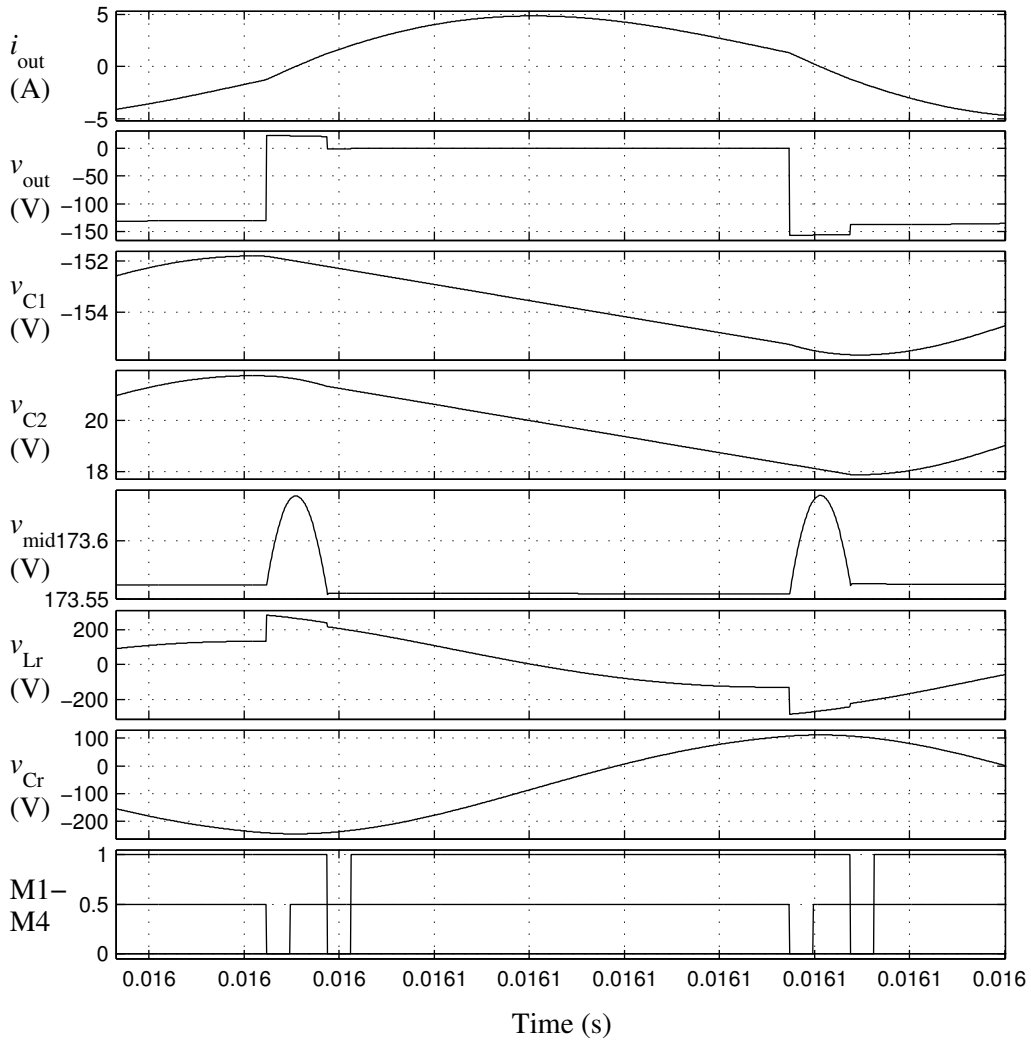


Figure 8: Simulated waveforms of balanced midpoint voltage transients.

4 CONTROLLER DESIGN

4.1 System Idenfication

To control the capacitor voltages at any given time, a proper phase-shift has to be applied between the gate signals in order to discharge the ac-side capacitors and regulate their voltages to desired levels. Figure 9 shows a step response of midpoint voltage when phase-shift time T_{ps} is switched from steady state value to zero and twice the steady-state value. At time interval $t = 0\ldots20$ ms phase-shift is kept at 108 ns which corresponds to steady-state value. If minimum capacitor voltage equals zero, then the midpoint voltage has a value $v_{\mathrm{mid}} = \sqrt{2}/2 v_{\mathrm{in}}$ as can be seen from the figure during $t = 0\ldots5$ ms. At time instant $t = 20$ ms, phase-shift time is decreased in one time step resulting in a slow increase of the dc-bias of midpoint voltage. At time instant $t = 80$ ms phase-shift is increased resulting in a decrease of midpoint voltage until T_{ps} is set back to steady-state value at $t = 95$ ms.The midpoint voltage stays almost steady if a constant phase-shift of twice the dead-time ($T_{\mathrm{ps}} = 108$ ns) is applied.

The simulation waveforms of Figure 9 show that discharging happens much faster than charging of the ac-side capacitors and therefore, the midpoint voltage is a non-linear function of phase-shift time. In addition, change in midpoint voltage is most rapid when $v_{\mathrm{mid}} < \sqrt{2}/2 v_{\mathrm{in}}$ simply by the fact that ac-main voltage forces midpoint voltage to rise

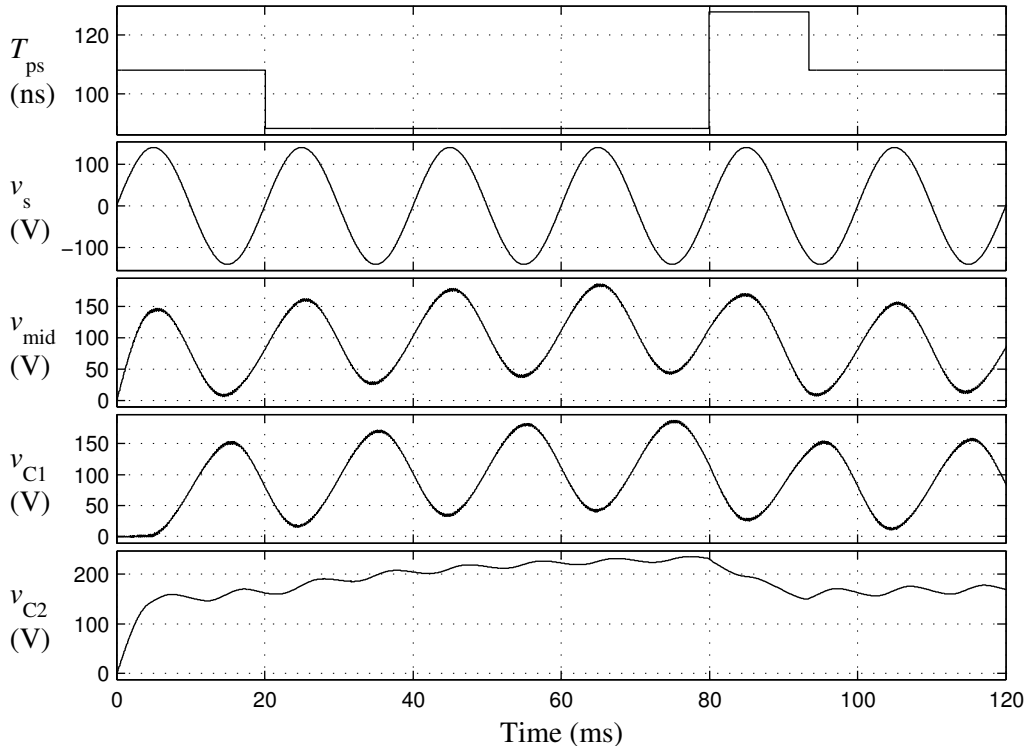


Figure 9: Step-response of midpoint voltage.

until it exceeds this value.Furthermore, charging and discharging waveforms have a low-frequency component at ac-main frequency. The rising of midpoint voltage occurs mostly during input voltage peak values while as midpoint voltage decreases around input voltage cross-overs.

Figure 10 shows the open-loop step-response of midpoint voltage when zero phase-shift is applied between the gate signals. The step-response waveform reminds of an approaching exponent function that reaches its maximum value at $v_{\max}$. The midpoint voltage cannot go above this value as discharge caused by the leakage current is as equal as the voltage transient during dead-time. However, with high input voltage the maximum values are unrealistic as power switches would result in failure caused by overvoltage.

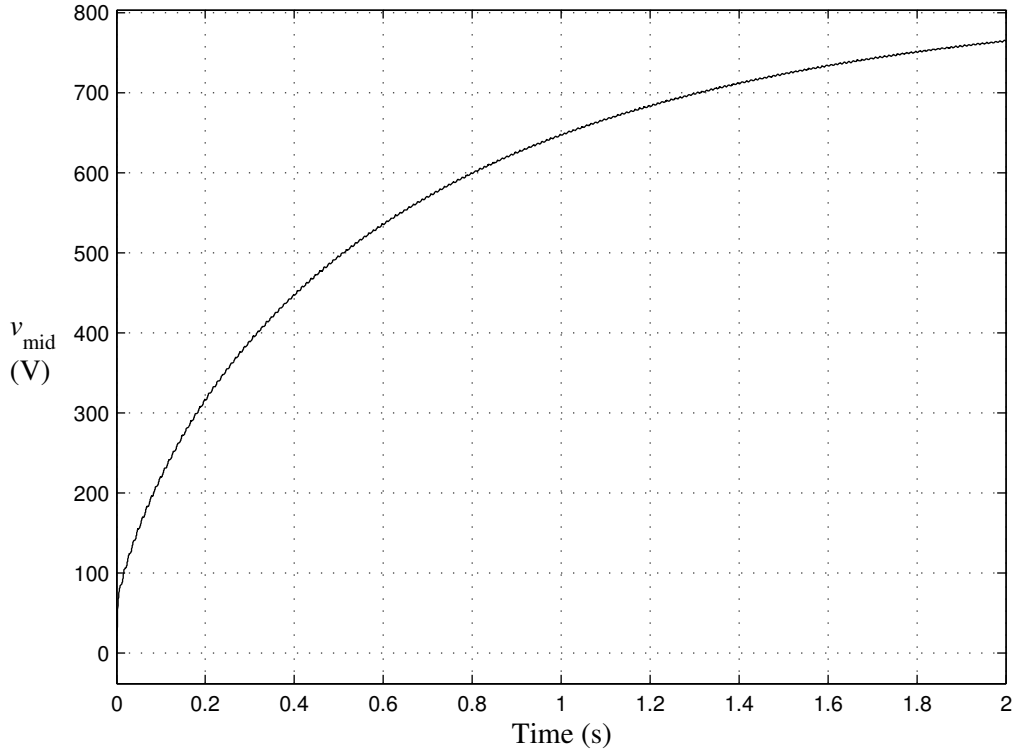


Figure 10: Simulated open-loop step-response of the system showing increase of midpoint voltage with zero phase-shift.

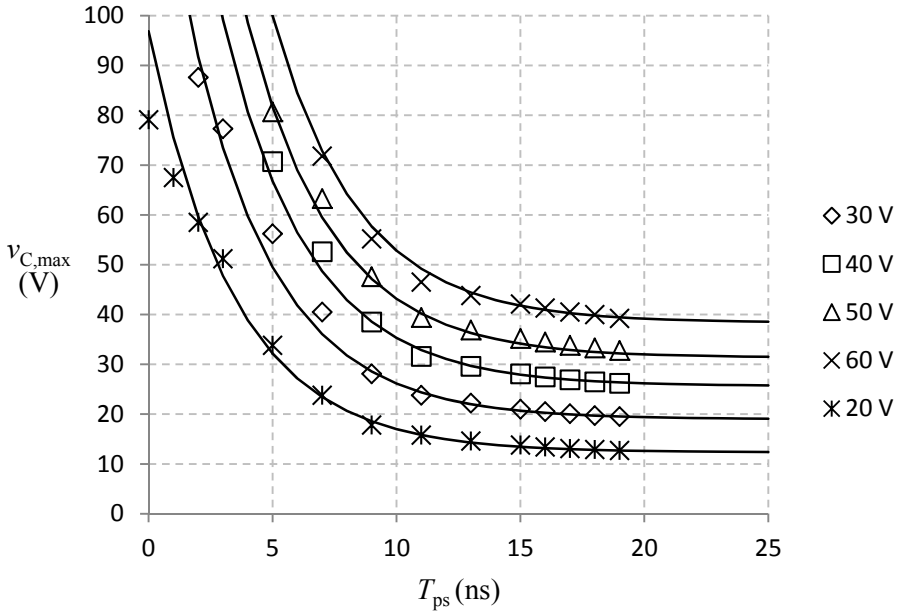


Figure 11: v_{max} as function of T_{ps}. The data points are measured values from an experimental setup

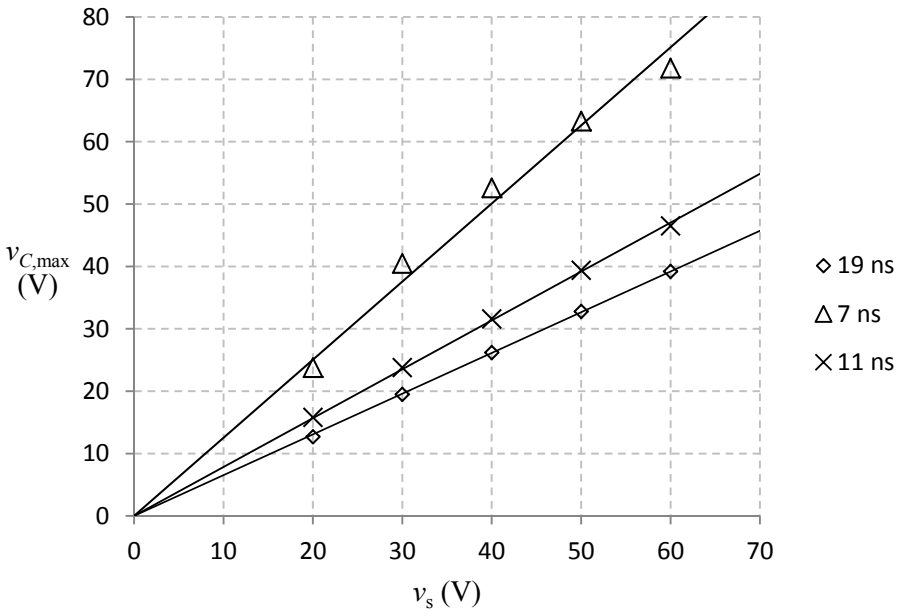


Figure 12: v_{max} as function of v_s. The data points are measured values from an experimental setup.

To further illustrate the charging and discharging phenomena Figure 11 shows $v_{\max}$ as a function of T_{ps} with various input voltage values. The data was calculated by keeping phase-shift constant and let the capacitor voltage reach its maximum value. Phase-shift time has not much effect on the midpoint voltage when phase-shift is in range of $T_{\text{ps}} = 30 \ldots 50$ ns. However, when phase-shift time is further decreased over 15 ns, the maximum capacitor voltage value starts to increase more rapidly. The relation of midpoint voltage is similar to decreasing exponent value as phase-shift is increases. Phase-shift is non-linear to maximum capacitor voltage, since the slope does not stay constant in the dead-time range $0 \ldots 50$ ns. However, maximum capacitor voltage can approximated to be linear when operation is limited to small range of T_{ps}.

Figure 12 shows dependence of $v_{\max}$ as a function of input voltage with various constant phase-shift time values. We can clearly see that dependence is linear as a trendline can be fitted between the data points. The lines meet at the origin but radiate further apart from each other as input voltage is increased.

If we omit the low-frequency component included in midpoint voltage, we can approximate the waveforms of Figure 10 with an approaching exponent function that can be described with a following equation:

$$v_{\text{r}}(t) = \left(1 - e^{-t/\tau}\right) v_{\max} \,, \tag{4.1}$$

where $v_{\max}$ denotes the maximum capacitor voltage that can be achieved by charging. From Figure 10 we can approximate a value for parameter a:

$$a = \frac{1}{\tau} = \frac{1}{0.38} = 2.63 \,. \tag{4.2}$$

By taking Laplace transforms of equations (4.1) we get the following equation:

$$U(s) = \frac{1}{s} \frac{b}{s+a} \,, \tag{4.3}$$

where $a = 1/\tau$ and b is gain of the system [11]. The coefficient $1/s$ corresponds to the unit step signal applied to input and hence, from (4.3) the transfer function of the plant can be written from input t to the output y as follows:

$$G(s) = \frac{Y(s)}{T(s)} = \frac{b}{s+a} \,, \tag{4.4}$$

which corresponds to a first order transfer-function having a single pole at $s = -a$.

If steady-state value of midpoint voltage corresponds to $T_{\text{ss}} = 2T_{\text{dt}}$, then a decrease in

phase-shift from steady state value results in increase of midpoint voltage. On the contrary, an increase in phase-shift from steady-state value results in decrease of midpoint voltage. This means that the gain b of the system is negative, since input to the system results in action of opposite direction. [12]

If we assume that the controller operation is limited around the steady-state value, then the gain of the system stays relatively small as can be seen from Figure 11 with phase-shift values in range of $T_{\text{ps}} = 15 \ldots 25$ ns. This would lead to a system gain of:

$$b = -\frac{v_{\text{mid}}}{v_{\text{in}}} = -\frac{\sqrt{2}/2\, v_{\text{in}}}{v_{\text{in}}} \approx -0.707. \tag{4.5}$$

With higher phase-shift values the gain would not predict the system behavior very well. However, as long as steady-state voltage is maintained, the approximation can be considered sufficient.

4.2 Controller Design

Since the dc-voltage is roughly proportional to added phase-shift, a simple PI-controller with a feedback control loop as illustrated in Figure 13, can be designed to keep the dc-voltage of the ac-side capacitors at a constant level. The PI-controller adjusts the phase-shift time T_{ps} of the gate signals so that the error signal e is close to a desired reference value V_{ref}. A PI-controller is feasible, since the steady-state error can be driven to zero and dynamic requirements are not so high [11]. The derivative part of a traditional PID-controller is omitted to make the controller less sensitive to noise [13].

The transfer function of the feedback is considered as one, since the error and measurement lag can be considered small compared to the dynamics of the system.

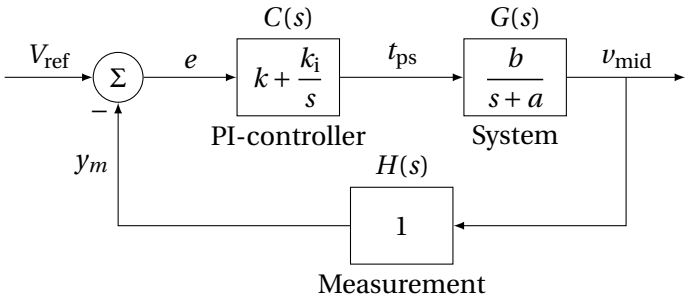


Figure 13: PI-controller with negative feedback designed for regulating the dc-voltage of ac-side capacitors.

From Figure 13 we get the loop transfer function of the system:

$$L(s) = C(s)G(s) = \frac{kbs + k_i b}{s(s+a)}\,, \tag{4.6}$$

where k is proportional gain, k_i integral time constant. [12] The transfer function of the closed-loop system from reference r to output y is given by

$$\frac{Y(s)}{R(s)} = \frac{b(ks + k_i)}{s^2 + (a+bk)s + bk_i}\,. \tag{4.7}$$

By rewriting the characteristic equation of the denominator in (4.7) as follows:

$$s^2 + 2\zeta\omega_0 s + \omega_0^2\,, \tag{4.8}$$

we can find the parameters for k and k_i:

$$k = \frac{2\zeta\omega_0 - a}{b} \tag{4.9}$$

$$k_i = \frac{\omega_0^2}{b}\,, \tag{4.10}$$

where ζ is a damping ratio and ω_0 is natural frequency. Since the model is of first order it is more convenient to tune the controller by having ζ and ω_0 as parameters. The parameter ζ determines the shape of response and ω_0 the speed of response. [12]

A small proportional gain value is selected to prevent small variation in midpoint voltage from affecting controller behavior. In most cases it is desirable to have a moderate overshoot which means that the damping ratio ζ should be in the range of 0.5 to 1. [12] By selecting $k = 0.1$ and $\zeta = 0.7$ we can calculate the natural frequency by using (4.9) as $\omega_0 = 2.1$. From (4.10) we get the integrator gain value as $k_i = 6.19$.

By using the above data, we get a following closed-loop transfer function:

$$\frac{Y(s)}{R(s)} = \frac{0.707s + 4.377}{s^2 + 3.337s + 4.377}\,. \tag{4.11}$$

By adding integral term we can make sure that the output sets to a reference value in steady state.

4.3 Closed-loop Performance of The Controller

Figure 14 shows the root locus for the system in (4.7). Plot contains one zero and two poles that are located on the right half plane of the y-axis. Because of this property the system can be considered stable. Figure also shows dashed lines for different damping coefficients. As the gain is increased the two poles move around the zero, until they coincide at −10.9, and after that another pole moves toward the zero and the other towards infinity. With different gain values K the damping factor ζ does not change much as the locus of the imaginary roots moves close to the a line in the figure with constant damping factor of 0.72.

Figure 15 shows the closed-loop step response of the system simulated with PSCAD software. Reference voltage is set to $V_{\text{ref}} = 150$ V. This corresponds to roughly 15 V for the error signal e that is fed to the PI-controller at the initialization. Since the error is negative, the output c of the PI-controller is negative and starts to decrease and making charging period shorter and increasing the slope of midpoint voltage. The waveform of T_{ps} shows that 50 ns is added to the input of the converter to balance the controller at this point, since it corresponds to twice the value of dead-time and in steady state voltage of v_{mid}.

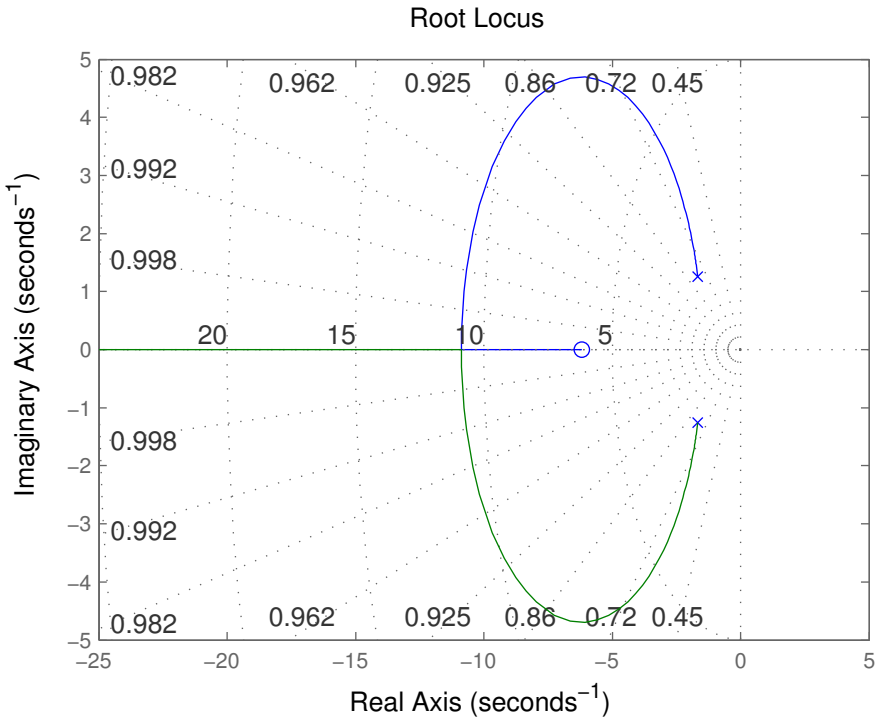


Figure 14: Root locus of closed-loop system.

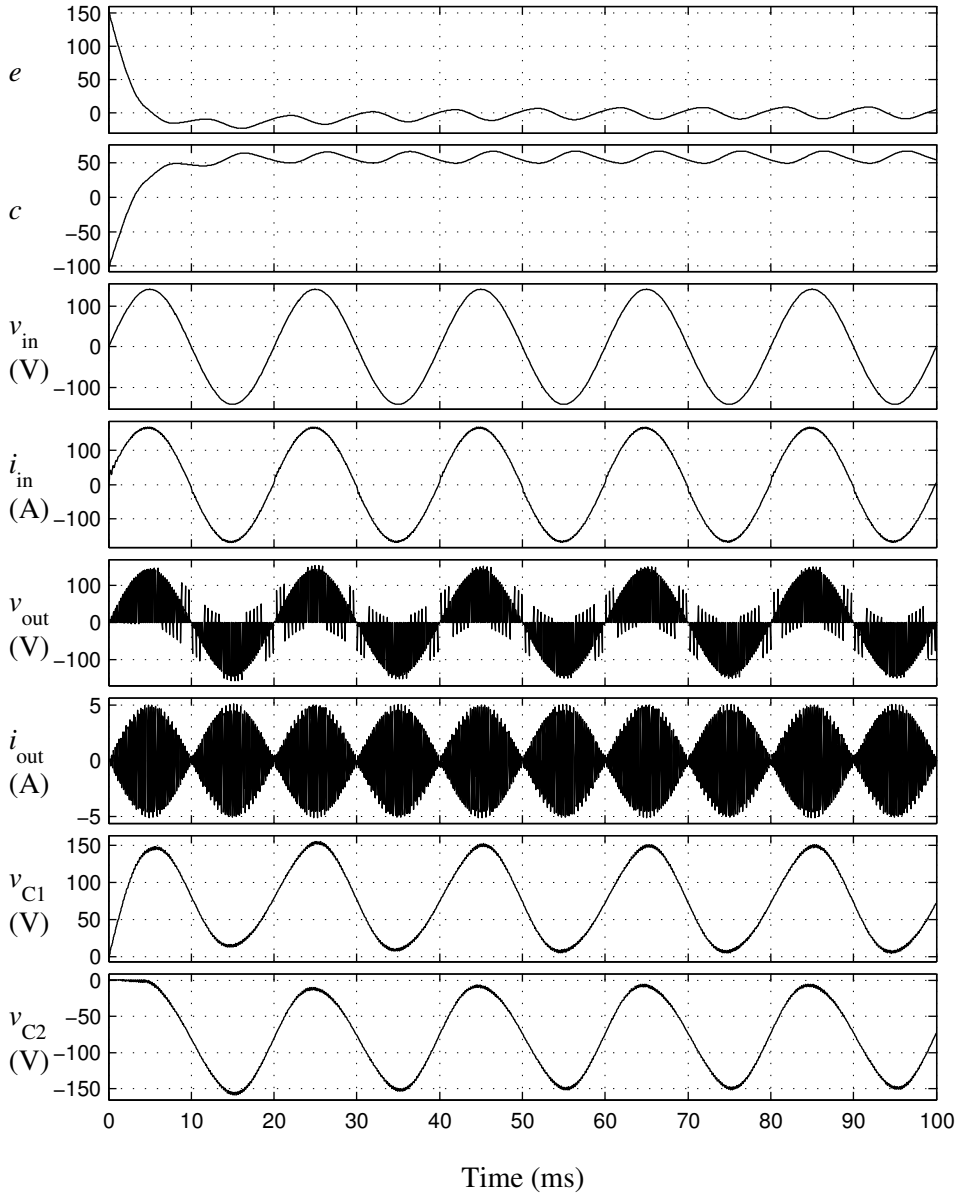


Figure 15: Closed-loop step-response simulated with PSCAD software.

5 RESULTS

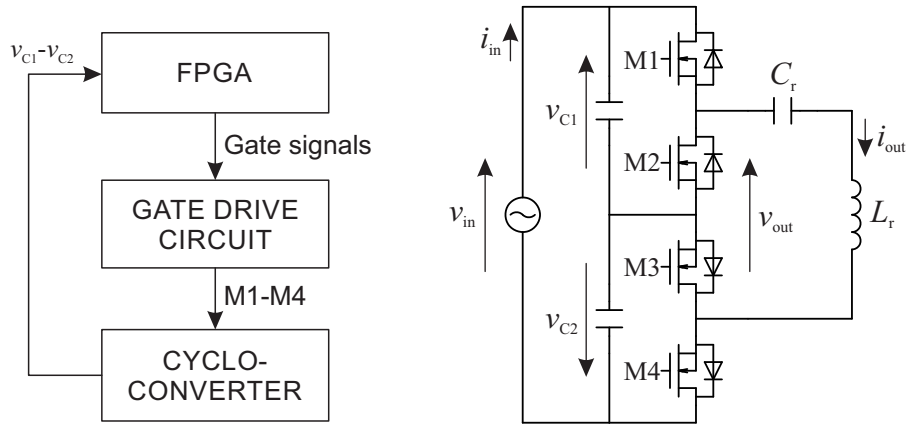
5.1 Experimental Setup

Figure 16 shows the experimental setup used in measurements. The component values are listed in the Table 2. The ac main voltage is selected as 100 V (RMS). Super junction power MOSFETs (IXFB170N30) rated at 170 A and 300 V are chosen as switching devices. The MOSFETs have a very low on-state resistance of 18 mΩ that allows to reduce on-state power losses. A small-rated filter inductor L_s = 100 μH is added in series with ac-main.

The filter capacitors are metalized polypropylene film capacitors with capacitance C_1 = C_2 = 5 μF, that is 50 times the resonant capacitance C_r. With the known load values, C_r = 0.1 μF and L_r = 135.5 μH, we can calculate the characteristic frequency as f_r = 43.2 kHz. The operating frequency was set to 47 kHz which is slightly higher than the resonant frequency f_r of the series resonant circuit.

Optically isolated voltage sensors are used to detect capacitor voltages v_{C1} and v_{C2} which are then feed through an A/D converter to a Field Programmable Gate Array (FPGA). FPGA calculates corresponding phase-shift time that minimizes the error feed to the PI-controller logic.

An auto-transformer is used to slowly increase the ac main voltage from low to high voltage level (100 V, RMS). The auto-transformer adds a small series inductance L_{var} in ac main side and does not effect the measurement results, since a much bigger inductor L_s is installed in series with it to prevent the high-frequency current from flowing through ac main.



(a) Block diagram of the experimental setup showing the signal flow.

(b) Circuit configuration of the experimental setup.

Figure 16: Flowchart and the experimental setup used in the measurements.

Table 2: Parameters of the experimental setup.

Parameter	**Value**
C_r	0.1 μF
L_r	135.5 μH
R_r	16.9 Ω
V_{in}	100 V, 50 Hz
f_r	43.2 Hz
f_{sw}	47 kHz
C_1, C_2	5 μF

5.2 Experimental Results

The experimental voltage and current waveforms are shown in Figure 17. The PI-controller succesfully prevents capacitor voltages v_{C1} and v_{C2} from rising and therefore, the midpoint voltage achieves a steady-state value of v_{mid} = 150 V which is close to the ac-main and capacitor peak-values. The midpoint voltage almost equals to v_{C1} at input voltage peak-values as the v_{C2} is close to zero.

By comparing Figure 17 to Figure 11, midpoint voltage at zero phase-shift and 20 V ac-main voltage we can clearly see that the controller removes overvoltage and makes the operation in synchronous mode possible. With zero phase-shift and 100 V ac-main, the capacitor voltages would already result in breakdown of the MOSFETs having a breakdown voltage of 300 V.

The midpoint voltage has a steady-state dc-bias that contains low-frequency component at twice the frequency of ac-main voltage as energy is transferred back and forth in the capacitors. v_{mid} rises from a minimum value to ac-main voltage peak value as the opposite capacitor (C_2 for positive v_s) is charged by ac-main current i_s when resonant current $i_r > i_s$. On the contrary, midpoint voltage decreases between the peak values of ac-main voltage. As a result, the resonant current amplitude rises slightly around input voltage crossing point.

AC-main current i_s is almost in phase with the ac-main voltage v_s and the shape of waveform is almost sinusoidal thus, resulting in a very high input power factor. The ac-side capacitors have an opposite polarity against each other and both have dc-value of $v_{mid}/2$. The sum of the capacitor voltages equals to v_s.

The waveform of the high-frequency output voltage v_{out} is drawn without the voltage transients. A close-up waveform shown in Figure X shows that voltage transients still occurs. To overcome this, the dc-bias of the capacitors should be removed by further increasing the phase-shift between input voltage peak-values. If the capacitor voltage (C_2 in case of positive input voltage) equals to input voltage, no transient occurs and switching losses can be minimized.

The resonant current amplitude has a low-frequency component and its magnitude will change according to ac-main voltage v_s. Furthermore, no low-frequency oscillation of resonant current is observed during the operation. No low-frequency current flows to resonant load, as the impedance of resonant load is high compared to the impedance of ac-side capacitors.

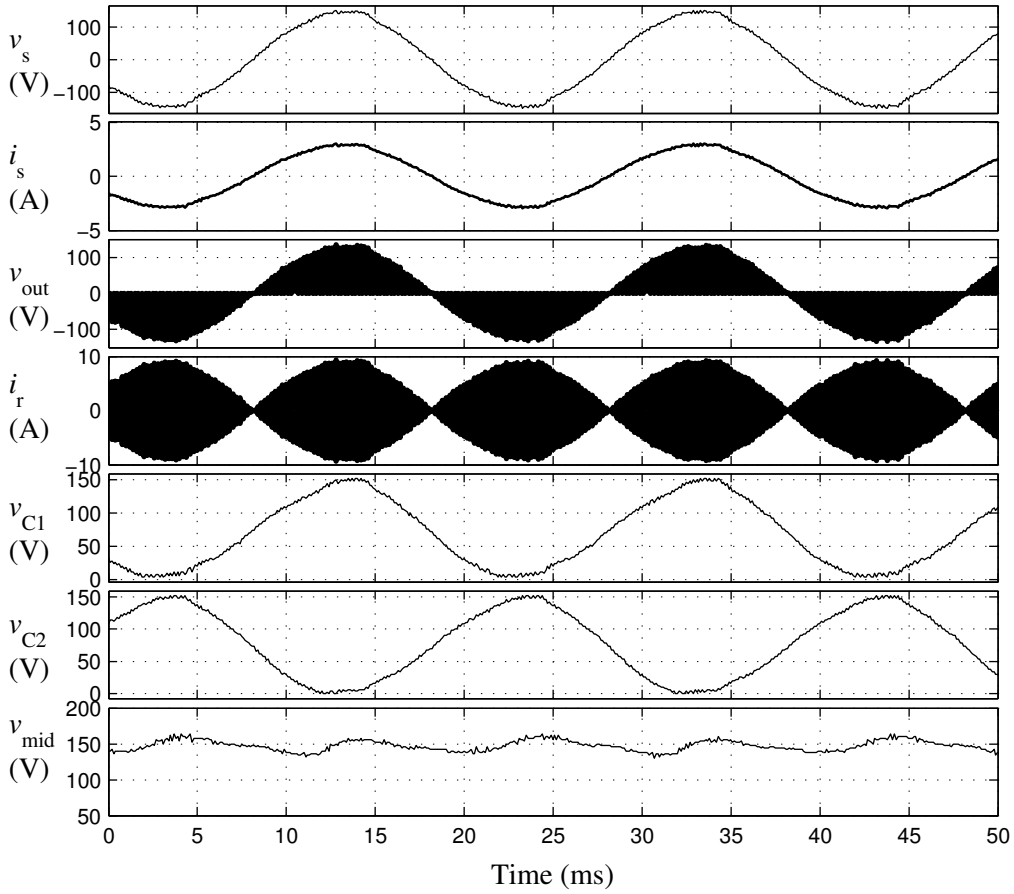
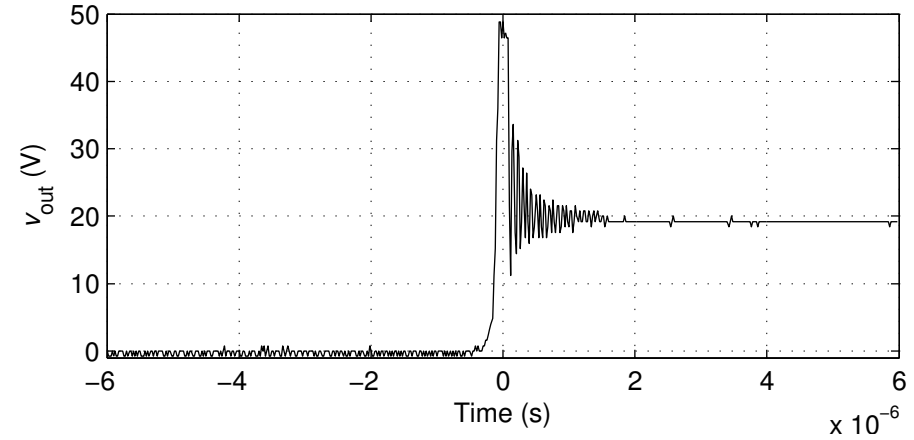


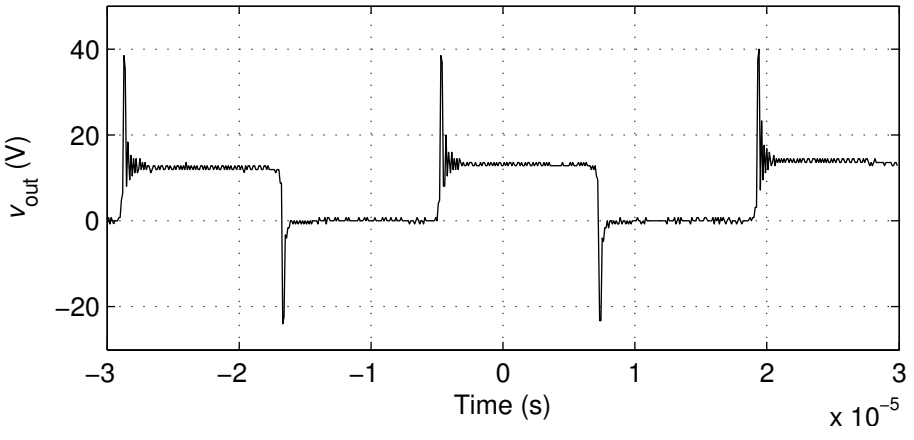
Figure 17: Experimental results for steady-state. The midpoint voltage can be calculated with $v_{\text{mid}} = v_{\text{C1}} - v_{\text{C2}}$.

Figure 18 shows the close-up waveform of the output voltage. During phase-shift time at time instant $t = 0$, the output voltage corresponds to dc-capacitor voltage $v_{\text{out}} = v_{\text{C1}} =$ 47 V. After phase-shift is finished, the output voltage is decreases to input voltage level as MOSFETs M1 and M4 are both on. However this will result in relatively large voltage and current ringing as can be seen in 18(a). Figure 18(b) shows that ringing occurs after phase-shift is ended on the high pulse of v_{out}; at this transition M3 turns off and as a result ringing occurs. In addition, since dc-bias exists in midpoint voltage, zero-voltage switching is not guaranteed. To overcome this, midpoint voltage should be regulated to zero voltage so that the voltage during phase-shift equals to input voltage.

The capacitor voltage v_{C1} equals to high-frequency output voltage in switching mode 1 where M1 is conducting. Then the resonant current i_{out} flows through the capacitor C_1, but its direction is opposite to the direction of the ac-main current i_{in}. The output voltage is nearly zero in switching mode 2. Then, the capacitor C_1 is charged by the ac-main current. During this period, the negative resonant current flows through the series resonant circuit, switch M2, and the body diode in anti parallel with M3.



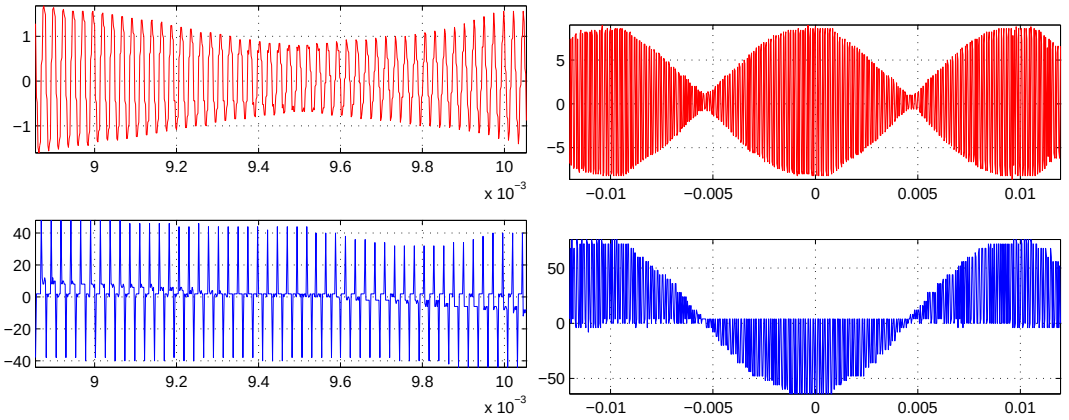
(a)



(b)

Figure 18: Output voltage transient showing current ringing at turn-on of the switches M1 and M4.

Figure 19 shows experimental waveforms when cycloconverter is driven with a sinusoidal phase-shift signal. The peak value of the phase-shift signal is set between the peak values of input voltage, thus the highest phase-shift value is achieved at the input voltage crossover. Figure clearly shows that with greater phase-shift values than dead-time, the resonant current amplitude can be improved. The output voltage contains a voltage transient caused by the dc-bias as can be seen in Figure 19(a). In figure 19(b) the voltage transient still occurs but is not displayed here for illustration purposes.



(a) A close-up waveforms of output current and voltage during ac-main voltage cross-over.

(b) Output current and voltage during a cycle of ac-main voltage.

Figure 19: Experimental results of output voltage and output current.

6 CONCLUSION

Simulation waveforms and experimental results show that by introducing phase-shift between the gate-signal pairs of M1–M2 and M3–M4, it is possible to regulate the dc-capacitors' voltages and prevent it from reaching overvoltage levels. The designed PI-controller sets the steady-state value so that the capacitor voltages have opposite voltage against each other during operation. This will guarantee that the capacitors voltages are in reverse direction to the adjacent anti-parallel diodes of the MOSFETs. As a result, the diodes prevent releasing the charge stored in the capacitors (negative charge of C_2 in case of positive input voltage). In spite of the controller, some dc-bias still remains in the capacitors between input voltage peak values. It is possible to regulate the bias voltage close to zero if phase-shift is futher increased from the steady-state value. To be able to achieve this with a voltage sensing controller, a much faster response is required. Experimental results also show that it is possible to improve the output current amplitude by introducing phase-shift between gate signals.

Design and tuning of the PI-controller is relatively easy, if the system can be modeled with a first order transfer function. In addtition, the time constant of the system is relatively long; time constant increases as the ac-side capacitance increases. Longer dead-time results in slower dynamics of the system and hence the controller does not have to be as fast. The controller parameters depends on the size of the ac-side capacitors, switching frequency, dead-time and the parameters of the resonant load.

The presence of dc-bias in midpoint voltage results in relatively large voltage and current ringing in MOSFETs. Since dc-bias exists in midpoint voltage, zero-voltage switching is not guaranteed. To overcome this, midpoint voltage should be regulated to zero so that the voltage during phase-shift is close to input voltage. It is possible to achieve this, by keeping the resonant current centered around its zero crossing, so that the increasing midpoint voltage transient equals to decreasing voltage transient of v_{mid}. It is possible to design a controller that adjust the phase-angle of resonant current by directly sensing the phase-angle between the resonant current and output voltage,

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