LAPPEENRANTA UNIVERSITY OF TECHNOLOGY
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MODELING FRONT END ELECTRONICS FOR A GAS ELECTRON MULTIPLIER DETECTOR

Examiners: Professor Tuure Tuuva
Professor Jero Ahola
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ABSTRACT

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Modeling Front End Electronics for a Gas Electron Multiplier Detector

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The Large Hadron Collider (LHC) in The European Organization for Nuclear Research (CERN) will have a Long Shutdown sometime during 2017 or 2018. During this time there will be maintenance and a possibility to install new detectors. After the shutdown the LHC will have a higher luminosity. A promising new type of detector for this high luminosity phase is a Triple-GEM detector. During the shutdown these detectors will be installed at the Compact Muon Solenoid (CMS) experiment.

The Triple-GEM detectors are now being developed at CERN and alongside also a readout ASIC chip for the detector.

In this thesis a simulation model was developed for the ASICs analog front end. The model will help to carry out more extensive simulations and also simulate the whole chip before the whole design is finished. The proper functioning of the model was tested with simulations, which are also presented in the thesis.

TIIVISTELMÄ

Lappeenrannan teknillinen yliopisto
Teknillinen tiedekunta
Sähkötekniikan koulutusohjelma

Henri Petrow

Simulaatiomalli Gas Electron Multiplier -ilmaisimen lukuelektroniikalle

Diplomityö

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53 sivua,35 kuvaa.

Tarkastajat: Professor Tuure Tuuva
Professor Jero Ahola

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Large Hadron Collider (LHC) Euroopan hiukkasfysiikan tutkimuskeskuksessa ajetaan alas huoltotoimenpiteitä varten jossakin vaiheessa vuosina 2017 ja 2018. Huollon aikana on myös mahdollisuus asentaa uusia havaitsimia. Huollon jälkeen LHC:lla tulee olemaan suurempi luminositeetti. Uusi lupaava havaitsintyyppi tälle suuremmalle luminositeetille on Triple-GEM havaitsin. Näitä havaitsimia tullaan asentamaan huollon aikana Compact Muon Solenoid (CMS) kokeeseen.

Triple-GEM havaitsimia kehitetään tällä hetkellä CERN:ssä. Samalla sille kehitetään myös lukuelektoniikkaa varten ASIC-piiri.

Tässä diplomityössä suunnitellaan simulaatiomalli ASIC:n analogiselle osalle. Mallin avulla piirille voidaan tehdä laajempia simulaatioita ja myös koko järjestelmää voidaan simuloida jo ennen kuin koko järjestelmä on suunniteltu. Simulaatiomallin oikea toiminta varmistettiin simuloimalla. Simulaatioiden tulokset on esittetty myös tässä diplomityössä.

Contents

Abbreviations

ASIC	Application Specific Integrated Circuit
ATLAS	A Toroidal LHC Apparatus
CBM	Calibration, Bias and monitoring
CERN	The European Organization for Nuclear Research
CFD	Constant Fraction Discriminator
CMS	Compact Muon Solenoid
ECAL	Electromagnetic Calorimeter
FIFO	First In First Out
GEM	Gas Electron Multiplier
HCAL	Hadron Calorimeter
HDL	Hardware Description Language
LEP	Large Electron-Positron Collider
LHC	Large Hadron Collider
LV1A	Level 1 Accept trigger
SRAM	Static Random Access Memory

1 Introduction

1.1 European Organization for Nuclear Research

The European Organization for Nuclear Research (French: Organisation européenne pour la recherche nucléaire), CERN. Is a European organization which aim is to advance nuclear research in Europe. At the moment it hosts the biggest particle accelerator in the world, the Large Hardon collider.

CERN was established in 1954 to the Franco-Swiss border near Geneva. CERN has 21 European member states. CERN has around 2500 staff members and it hosts more than 12000 fellows, associates, apprentices, visiting scientists and engineers, which represent 608 universities and 113 nationalities.

It hosts a wide variety of particle accelerators and experiments. A map of the accelerators and colliders is presentend in the figure 1[1]

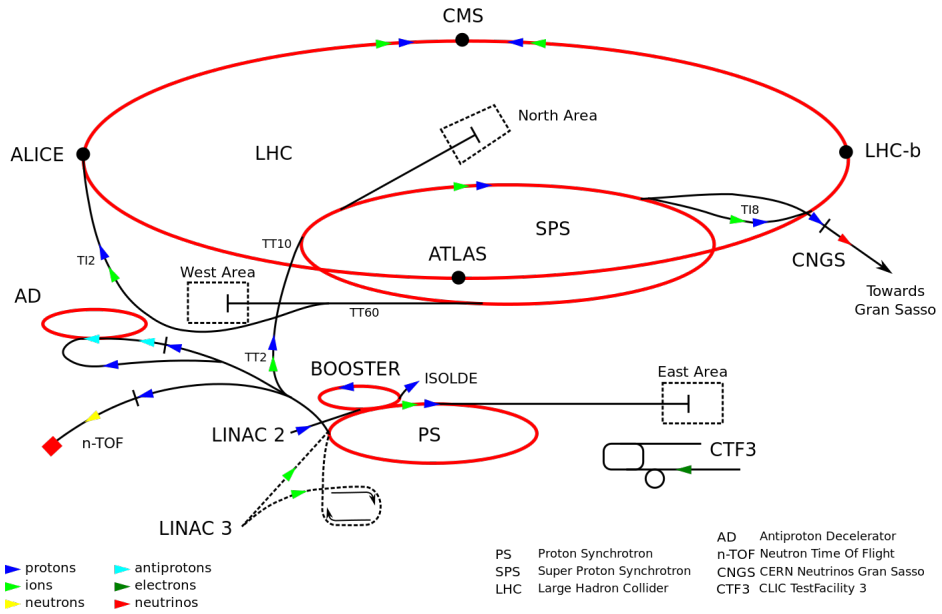

Figure 1: Map of the CERN accelerator complex.[1]

1.2 Large Hadron Collider

The Large Hadron Collider (LHC) is the largest and most powerful particle collider in CERN and in the whole world. The construction lasted for ten years, from 1998 to 2008. It has a circumference of 27 km and at deepest it travels at the depth of 175 meters below the ground. It is similar in size to it predecessor Large Electron-Positron Collider (LEP), which was dismantled in 2000 to make space for the LHC, which was built into the same tunnel previously occupied by LEP. The accelerator is designed to collide protons or lead nuclei. It hosts two beams, traveling to the opposite directions. The accelerator has three different types of magnets. One to bend the beams, so they travel a closed circle. One to focus the beam, so it stays in a tight bunch. And a third one just before the point of collision to squeeze the beam really dense, this helps to make the collisions more likely.

In the LHC there are bunches of particles traveling close to a speed of light. The bunches are separated from each other approximately by 25 ns, which make up a frequency of 40 MHz. The particles move close to speed of light so in 25 ns they travel about 7.5 m, which is the distance between the bunches. The LHC master clock is also defined to be 40 MHz and the detector electronics use this clock for operation.[3] The LHC has four points where the beams collide. In these points the seven experiments of LHC are located. The experiments are shown in the figure 2

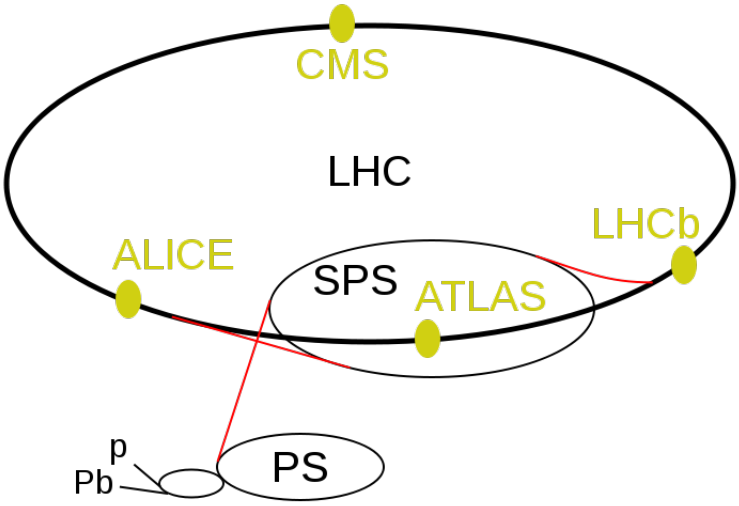

Figure 2: The experiments located in the LHC.[2]

The biggest experiments are A Toroidal LHC Apparatus (ATLAS) and Compact Muon Solenoid (CMS), which are both general purpose experiments.[2]

1.3 Compact Muon Solenoid

The Compact Muon Solenoid (CMS) is one of the largest international scientific collaborations in history, involving over 4000 physicists, engineers, technicians and other staff. It weights about 12500 tonnes and it is build around one huge solenoid magnet, a biggest of its kind in the world.

CMS is a general purpose experiment and it is supposed to study a wide variety of physics, including the search for Higgs boson and extra dimensions.It has the same scientific goals as the ATLAS experiment, but it uses a different technical approach. This allows the experiments to verify their results. The CMS is designed to see a wide range of particles and phenomena produced in the high-energy collisions in the LHC. It has several layers of detectors to measure different particles and make up a detailed image of the

collision. There is a system for detecting and measuring muons, a method to detect and measure electrons and photons, a central tracking system to give momentum results and a calorimeter to prevent particles from escaping.

The heart of the CMS is the solenoid magnet. It is essentially a coil of superconducting wire that creates a magnetic field when electricity runs through it. The higher momentum a charged particle has, the less its path gets curved in a magnetic field. So for the high energy particles of LHC a strong magnetic field is required to accurately measure the momentums. The large size of the magnet also allows a number of layers of muon detectors to be installed. Inside the coil by the tracking devices and outside by the muon chambers. In the figure 3 a slice of CMS detector is shown with the paths of the different particles.

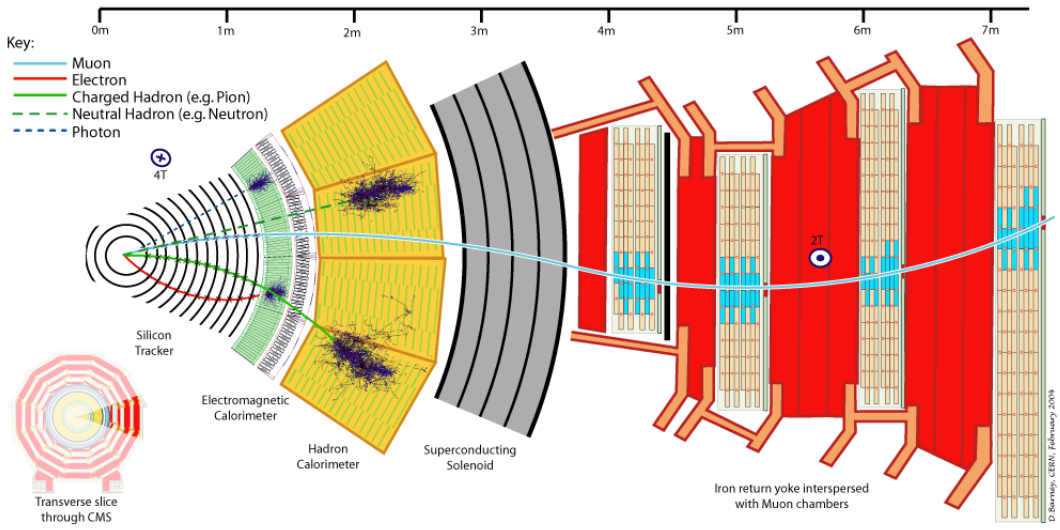

Figure 3: A slice of the CMS, showing where different particles are detected.[4]

A particle emerging from the collision encounters first the silicon strip detectors, which measure the track of the passing particle. Next the particles encounter the calorimeters ECAL and HCAL, which measure the energy of

the particles. The ECAL detects particles which interact electromagnetically and the HCAL, particles which interact by the strong force. Most of the emerging particles are absorbed by the calorimeters. Muon is a particle which passes both of the calorimeters. For muon detection, there are muon chamber detectors, which are the outermost detectors in the CMS.[4]

1.4 Triple-GEM Detector

A triple-GEM detector is made up of three Gas Electron Multiplier (GEM) layers. A GEM consists of a thin, metal-clad polymer foil, chemically pierced by a high density of holes. On application of a difference of potential between the two electrodes, electrons released by radiation in the gas on one side of the structure drift into the holes, multiply and transfer to a collection region.[5] In a triple-GEM detector there is three GEM layers and between them there is a gas. When a particle ionizes the gas in the first chamber, the GEM foil accelerates the freed electrons to the next chamber, where they ionize the gas and produce more electrons, this creates an avalanche of electrons and creates a signal, which can be measured. The working principle of a triple-GEM detector is shown in the figure 4

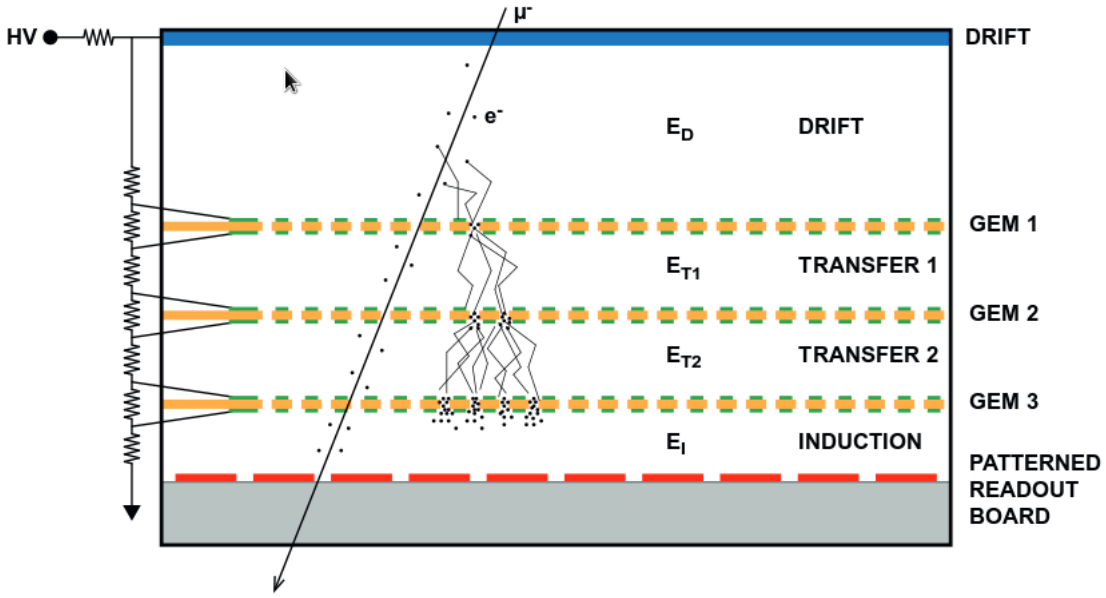

Figure 4: A principle of the triple-GEM detector operation. A passing muon ionizes the gas, creating an avanche of electrons in the structure.[6]

Triple-GEM detectors offer an excellent spatial and time resolution. This allows the detector to be used in both triggering and tracking for the muon. [7]

1.5 Verilog-AMS

Hardware description languages (HDLs) exist to describe hardware. Typical programming languages often describe algorithms. They are based on central CPU which processes the sequential instructions and performs the instructed functions accordingly. HDLs on the other hand are often parallel in nature. And they have two main functions: simulation and synthesis of hardware. With simulation you can test your system with different stimuli and understand the operation of complex systems. In synthesis the aim is to actually implement the hardware. With the HDL you can implement the functions on a higher level and the synthesis tool converts the operation to

the transistor level. This has has boosted the design of complex circuits and allows the design of modern extremely complex sytems, with billions of transistors..

Verilog-AMS is a modelling language for mixed signal systems. The Verilog-AMS hardware description language combines the digital Verilog HDL and analog Verilog-A languages. This is shown in the figure 5.

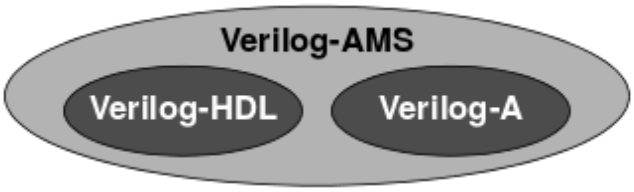

Figure 5: The relation of the different Verilog languages. [9]

The traditional digital Verilog HDL was developed already in 1984 and it is one of the most popular hardware description languages. It was developed for digital systems, where signals usually has just two values and the system is made up of logic circuits. Verilog-A hardware description language is a derivative of the original Verilog HDL and it allows user to use analogue signal. Analogue signals are continuous in nature. But it allows simulation of analog circuits including amplifiers, shapers and filters.

The Verilog-AMS was developed by combining the analogical continuous time features of the Verilog-A and the digital features of the traditional Verilog HDL.The Verilog-AMS language is a mixed signal language. The term mixed-signal indicates that the system has both digital and analogical parts. So the Verilog-AMS is able to handle both discrete time signals as well continuous time signals, which makes it a powerful tool on the design of mixed signal systems such as analog to digital converters. The Verilog-AMS is expected to have a big impact on the design process of mixed signal

Application Specific Integrated Circuits (ASICs).[9][8]

1.6 Motivation

The LHC is planned to go on the second Long Shutdown sometime during 2017 and 2018. During this shutdown maintenance and detector upgrades will be done. After the shutdown the LHC will have a higher luminosity and there is a need for more novel detectors to take advantage of this. New detectors are now being designed that could be installed during this Long Shutdown.

The triple-GEM detectors promise higher resolution for tracking and operation in high particle rates, which is needed in the high luminosity phase. In the CMS there is a vacant places in the muon sector. This allows to add new detectors to the existing muon system. [10] [11]

Readout electronics for the triple-GEM detectors are needed. They are at the moment under design and simulation.

1.7 Research Objectives and Methods

The objective of the study is to create a Verilog-AMS simulation model for the analog front end of the read out electronics. This model can then be used in the place of the actual analog front end design. This serves two purposes. The analog front end is still under design, so the simulation model allows to perform simulations with the whole system before the actual analog front end is finished.

The second purpose of the simulation model is to be more light weight than the actual design. The less requirement for processing power allows more extensive and faster simulations for the rest of the system. The model is also

planned to evolve with time to a more complex design. When the parameters of the actual design start to become more clear, the simulation model can be refined to accommodate the actual design more precisely. For this the model should be easy to modify and expand.

The design and simulations are made by using Virtuoso analog design environment (ADE), which is part of the Cadence IC design package. The Virtuoso ADE offers powerful tools to explore, analyze and verify an analog design. It also provides a extensive support on mixed-signal design with Verilog-AMS, which makes it a suitable tool for this study.[12]

1.8 Structure of the Study

The study is divided into five parts. The first part (Chapter 1) gives an introduction to the basic background of the study and introduces the objectives and methods. The second part (Chapter 2) gives an overview of the whole read out electronics system, which the model will be part of. The third part of the study (Chapter 3) introduces first the requirements of the simulation model and then describes how the model was designed. The fourth part (Chapter 4) is dedicated to the simulation of the system. Fifth part (Chapter 5) gives a brief summary and conclusions of the study.

2 VFAT3 ASIC

VFAT3 is an ASIC designed as a readout electronics for multiple type of detectors, although it will be optimized for the use of triple-GEM detectors. The VFAT3 is a successor for the older VFAT2 design. A simple block diagram of the different components of the VFAT3 design is shown in the figure 6[13]

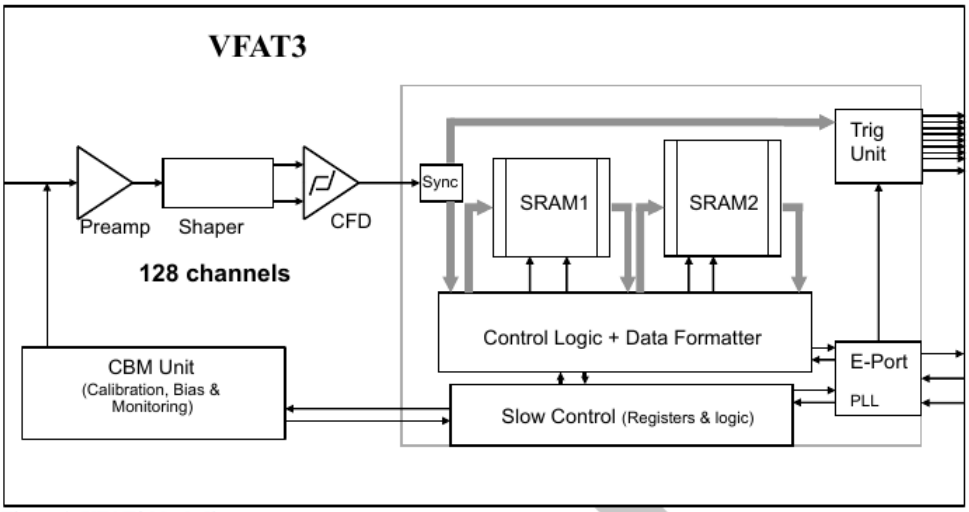

Figure 6: A block diagram of the VFAT3 ASIC.[13]

VFAT3 is composed of 128 channels which all include a analog front end. This analog front end is made up of three parts: a charge sensitive amplifier, a shaper and a constant fraction discriminator (CFD). Following the CFD there is a synchronization unit, which synchronizes the comparator result with the systems 40 MHz clock.

The VFAT3 provides trigger signals to outside through the trigger unit. The triggering unit can access all the 128 bits before or after the synchronization unit. The 128 bits are encoded to a 320 Mbps stream of data through the E-port. The triggering unit provides "Fast OR" combinations of groups of 2 or 4 channels with synchronization to the 40 MHz clock. This fixed latency information is then provided to external detector systems.

The data from the 128 channels is also used as a tracking data. The tracking data is fed through two Static Random Access Memories (SRAMs). The SRAM 1 samples all the 128 channels at the 40 MHz sampling rate. The triggered events are then transferred to the SRAM 2 with a time stamp. From the SRAM 2 the data is then converted to data packets, suitable for

transmission through the E-port.

All external communications with the VFAT3 is done through the E-port. This includes Slow Control commands, fast triggers, the clock, synchronization data and the data packets.

In the following sections the essential parts of the VFAT3 chip are introduced in more detail.[13]

2.1 Analog Front End

The analog front end includes the pre-amplifier, shaper and CFD, which are included in all of the 128 channels. The Analog front end is optimized for the readout of gaseous detectors, but can also be used to read out silicon detectors. A basic block digram of the front end is shown in the figure 7.

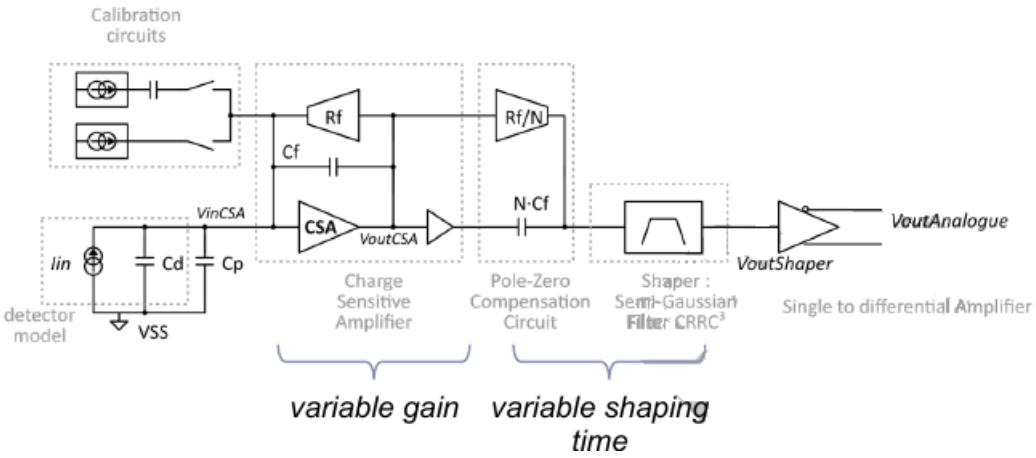

Figure 7: A diagram of the analogue front end.[13]

The front end is designed to accept both negative and positive signals from the detector, so holes or electrons can both be used to produce the input signal. In the output a differential signal is produced by the differential buffer.

The front end pre-amplifier and shaper have many programmable features to offer flexibility for different uses. This programmability allows the readout chip to be used for many different detectors and applications. The input characteristics can be programmed to suit the current detector or application. The programmable parameters are pre-amplifier gain, shaper peaking time, input signal polarity and differential buffer gain.

2.2 Constant Fraction Discriminator

The constant fraction discriminator (CFD) digitizes the differential signal coming from the shapers differential buffer. The CFD has a programmable threshold voltage into which the incoming shaper signal is referred. Signals above the threshold are passed as 1 and signal below the threshold are passed as 0.

The constant fraction discriminator works by splitting the signal into two parts. One part is inverted and delayed and the other part is left untouched. The two signals are then added together.[13]

2.3 Synchronization Unit

The analog front end and the CFD run asynchronously. To use the signal in the synchronized digital parts of the chip, the signal must be synchronized to the internal 40 MHz clock. The synchronization unit provides the interface between the two parts of the chip. The figure 8 shows the basic principle of the synchronization unit. The unit takes in the unsynchronized output from the CFD. The synchronization unit checks the output periodically with the 40 MHz clock. The output is then changed to 1 if CFD gives a signal. The output of the synchronization unit is then set back to zero after predetermined count of clock signals. This allows the unit output to be stretched to

accommodate different applications.

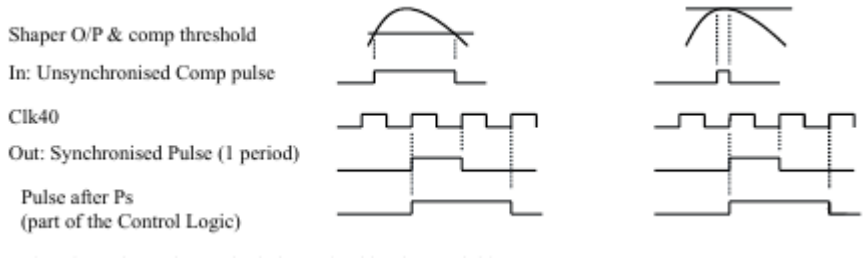

Figure 8: The basic principle of the synchronization unit.[13]

The synchronization unit also has some programmable features to allow versatility in the different uses of the chip. The programmable options include:

- "Mask", to suppress an individual channel, this is useful if a channel is particularly noisy.
- "MSPolarity", to change polarity of the sync stage.
- "UnSyncTrig" allows synchronized or unsynchronized data to be fed to the unit.

The synchronization unit divides the signal in to the two different data paths, one being fixed latency path for the Fast OR triggers and one is the variable latency path for the tracking information.[13]

2.4 Fixed Latency Trigger Path

From the synchronization unit a fixed latency trigger signal is obtained. The path of this signal is presented in the figure 9. In the figure the the path is highlighted and it runs from the synchronization unit to the triggering unit.

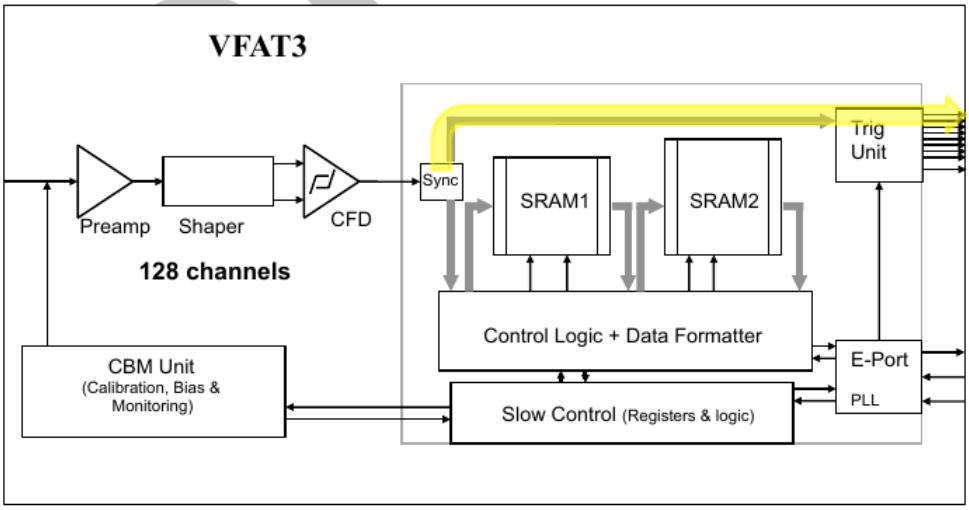

Figure 9: The fixed latency trigger path is highlighted in the block diagram.[13]

The purpose of the path is only to provide a fast "hit" information, which is synchronous with the 40 MHz clock. The trigger signal contains no time stamp, but it is synchronized with the LCH 40 MHz clock, so the "hit" information can be compared with other chips and detectors in the system. [13]

2.5 Variable Latency Path

The other data path after the synchronization unit is the variable latency path. This path is shown in the figure 10. The path is highlighted in the figure and it goes from the synchronization unit, through the SRAMs to the E-port.

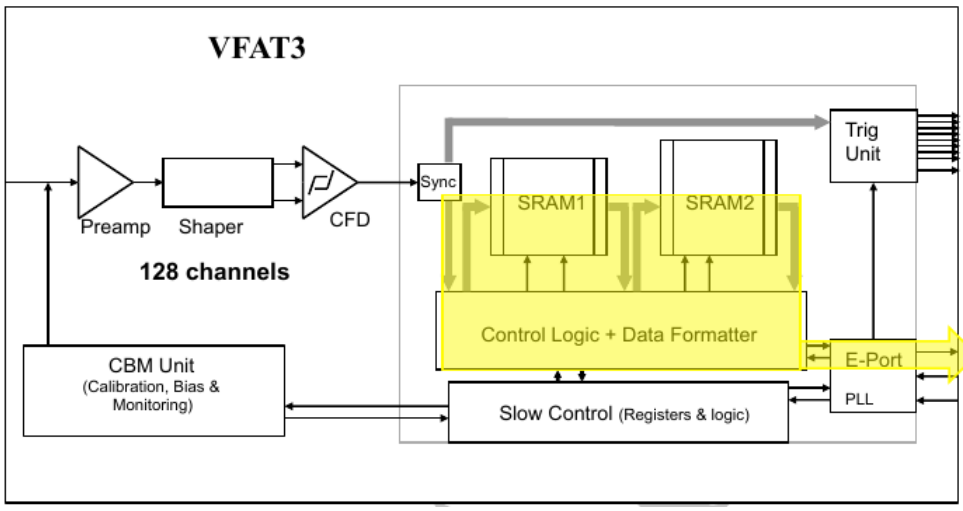

Figure 10: The variable latency trigger path is highlighted in the block diagram.[13]

The variable latency path is used to collect the tracking information of the hits. The 128 bit output of the synchronization unit is stored periodically to the SRAM 1. If a trigger signal is provided, the corresponding data is the sent to the SRAM 2 where from it is encoded to the E-port.

The variable latency path is used to feed full granularity data to the E-port. The data is accompanied with the time stamp information, so the packet can be associated with the right bunch crossing of the LHC. The data can also be collected by using the self-triggering option of the chip. In this case the chip provides the triggering for the memories and the desired data can be collected.[13]

2.6 The SRAMs

The VFAT3 has two main SRAMs for the data collection. The SRAM 1 reads the output of the synchronization unit periodically and stores the data. When triggering signal is provided the corresponding data is the stored to

the SRAM 2, which is a FIFO type storage. From the SRAM 2 the data is then fed to the E-port. The both SRAMs are protected against radiation effects with the use of hamming encoding.[13]

2.7 Control Logic

The VFAT3 control logic has 5 main functions:

- Creation of the self triggering.
- Pulse stretching.
- Controlling the SRAMs.
- Building the data packets.
- Interfacing with the E-port.

The internal self trigger enables the VFAT3 to provide full granularity data packets through the tracking data path. This can be useful for example when using test setups. The choice between LV1A triggering and self triggering is made with programmable parameter ST.

The SRAM control controls both the content and the read/write signals of the both SRAMs. It determines the operation of the SRAMs. It also adds information by providing partition data information and time tag information.

The data formatter checks if the SRAM 2 status is "not empty" and formats the data from SRAM 2 for the data packets. There are several different data formats available for the data to be used.

The E-Port interface provides hand shaking between the Control logic and the E-port.[13]

2.8 Calibration, Bias and Monitoring (CBM)

The CBM unit takes care of the calibration, biasing and monitoring the system.

The calibration system is used to help in the production test and characterization phase and also during the detector set-up and commissioning. The system provides internal charge pulses for the front end pre-amplifiers. The magnitude, phase and polarity of the pulse can be programmed. Also the channel into which the pulse is inserted can be determined.

The biasing provides programmable current and voltages for the pre-amplifier, shaper, and the constant fraction discriminator.

The monitoring allows internal currents and voltages to be monitored through the slow control. [13]

2.9 The Slow Control System

The slow control system is essentially a large register bank from which slow control commands allow read and write access. It is also able to send control commands to internal modules. It is called "slow" control since it relates to commands that need to be executed occasionally and have no relation to the LHC bunch crossing. However the commands themselves are transmitted over the same optical and E-link path as the fast control data.[13]

3 Model for the Analog Front End

A simulation model for the analog front end was designed. The model was written using Verilog-AMS HDL language. First in this section the specifications for the model are presented, then the design of the model is presented

in detail.

3.1 Specifications

The analogue front end includes the pre-amplifier and shaper parts of the VFAT3 design. In this chapter the given specifications for the front end are presented. These specifications are the basis on which the analogue front end simulation model will be designed.

3.1.1 Time constants

Peaking time or shaping time is defined as the time between 1% and 100% of the signal peak value. So the time it takes for the signal to rise from 1% of the peak maximum value to the maximum value. This definition is shown in the figure 11.

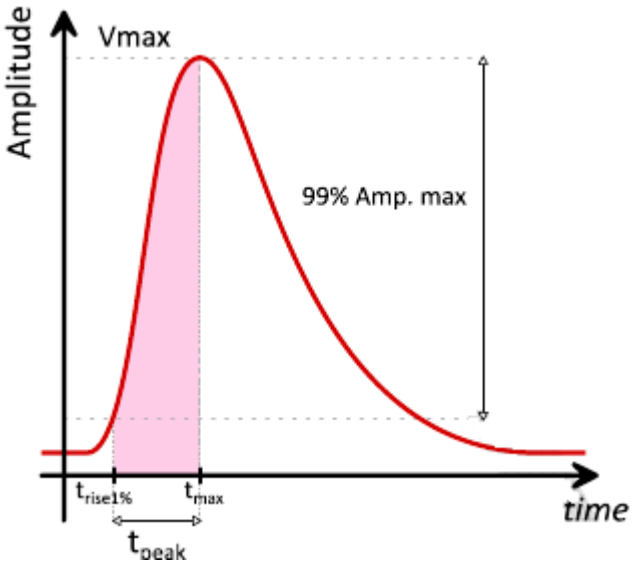

Figure 11: Definition of the shaping time.[14]

The peaking times are chosen so that the VFAT3 chip can be used in variety

of different detectors. The chip will be optimized for 100 ns peaking time, which corresponds to the empirical optimum for gaseous detectors. The programmable peaking times for the chip will be 25 ns, 50 ns, 75 ns, 100ns.

Shaper baseline recovery is defined as the time it takes for the shaper output to fall from maximum peak value to 1% of the maximum peak value. This is shown in the figure 12.

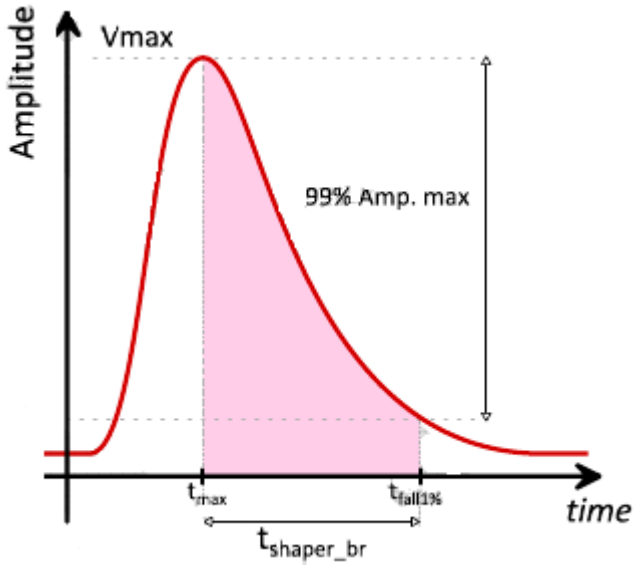

Figure 12: Definition of the shaper baseline recovery.[14]

For the baseline recovery no specific value was given. The baseline recovery should happen in a time that prevents pile-up of the pulses.

The charge sensitive amplifier baseline recovery is defined as the the time it takes for the signal to fall from the maximum peak value to 5% of the maximum peak value. The definition of the baseline recovery is shown in the figure 13.

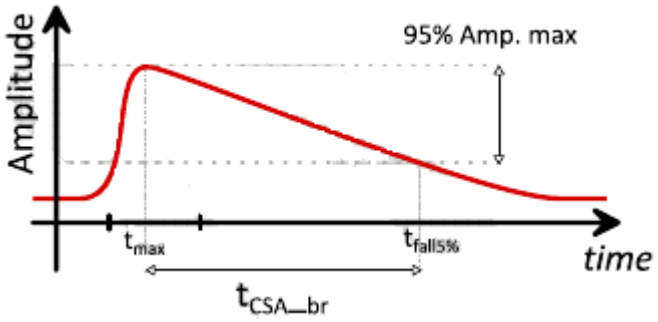

Figure 13: Definition of the charge sensitive amplifiers baseline recovery.[14]

To avoid pile-up of the pulses, the baseline recovery should be achieved in less than 10 us.

The front end should have a dynamic range up to 200 fC of input charge. For the full dynamic range the linearity error should be less than 5%. For charges up to 100 fC the linearity error should be less than 1%. The gain of the front end should be programmable from 1.25 mV/fC to 50 mV/fC, with four different values. The front end should also be able to take both positive and negative signals as an input.[14]

3.2 Structure of the Model

The model has been implemented purely by transfer functions and it is written in Verilog-AMS. The model consists of a three separate blocks. The blocks can be seen in the Figure 14. The blocks are pre-amplifier, shaper with pole zero cancellation and a differential buffer.

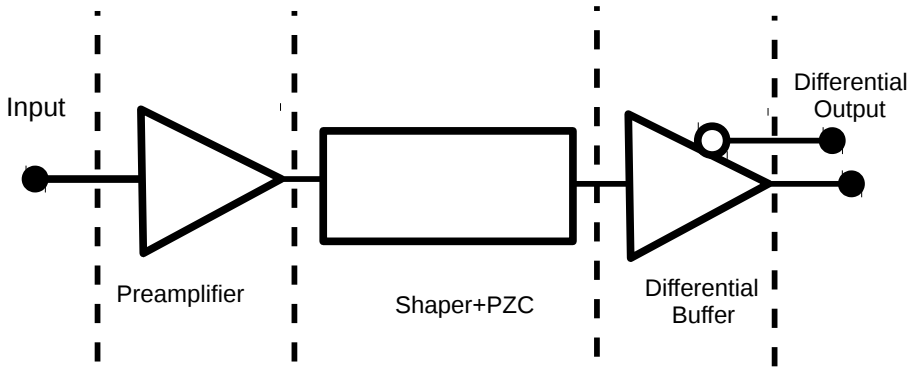

Figure 14: Model of the front end. It consist of a pre-amplifier, a shaper with zero pole compensation and a differential buffer.

In the next subsections the blocks are introduced in more detail.

3.2.1 Pre-amplifier

Pre-amplifier takes in the pulse from the detector and integrates it to a step function. The step function should have a slow decay and eventually return to baseline.

A transfer function for a simple integrator is

$$G_I(s) = \frac{1}{s}. \tag{1}$$

For a decay, the pole of the integrator needs to be moved on the left. This can be done with a transfer function in the form

$$G_I(s) = \frac{1}{1 + t_p s} \tag{2}$$

where the time constant t_p defines the rate of the decay.

The pre-amplifier is a rather simple block. It acts as a slowly decaying integrator. The block takes in a current pulse and uses Verilog-AMS *laplace_nd* function to integrate the pulse according to a transfer function

$$G_I(s) = g_p \frac{1}{1 + t_p s}. \tag{3}$$

The time constant t_p and gain g_p was chosen so, that the requirements in the design overview [14] for the settling time were met.

The pre-amplifier has also a high gain to provide a step function-like input for the next stage, which is the shaper. The shape of the pre-amplifier output is shown in the Figure 15

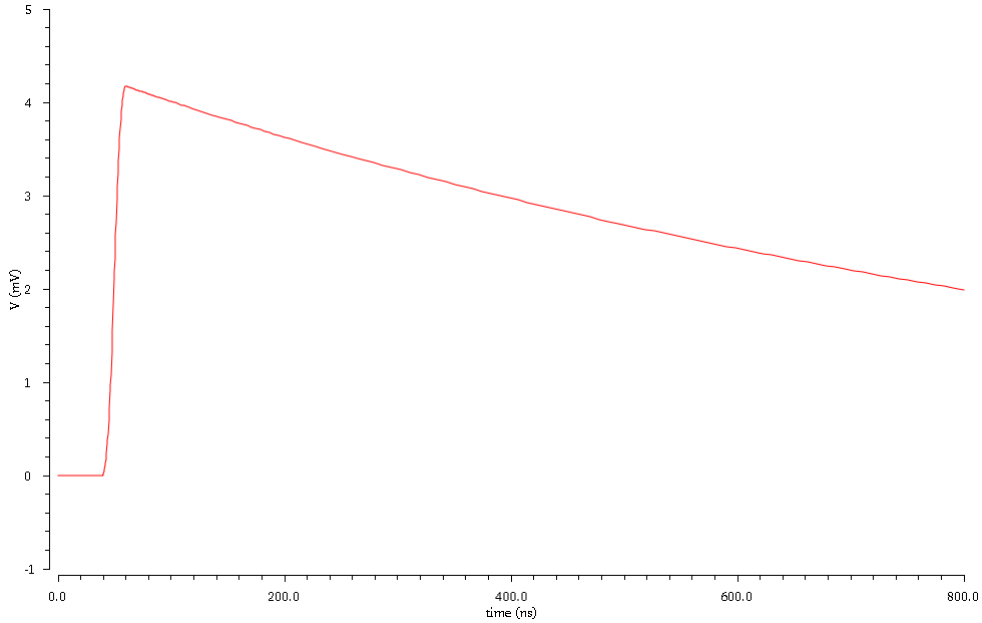

Figure 15: Signal after the pre-amplifier. The shape is a slowly decaying step function.

3.2.2 Shaper and the Pole Zero Cancellation Unit

The shaper provides a desired pulse shape for the constant fraction discriminator. The input is shaped by a third degree CR-RC filter, which is also known as a semi-gaussian filter [15]. In a CR-RC shaper, there is first a derivation part, which is then followed by multiple integrating parts. A typical CR-RC filter design is shown in the Figure 16

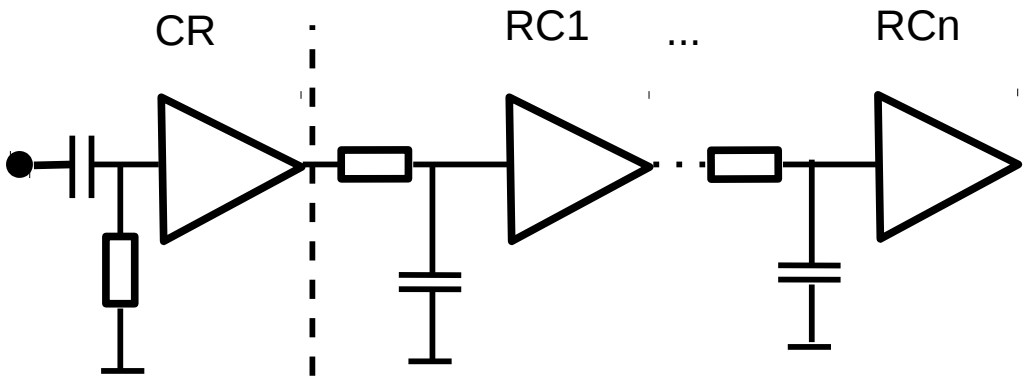

Figure 16: Typical design for a CRRC-filter. It first has a derivator, which is followed by multiple integrators.

The transfer function for the filter is in the form

$$G_s(s) = g_s \frac{s}{(1 + t_s s)^n}, \tag{4}$$

where t_s is a time constant, which affects the signals peaking time and the n represents the number of integrators in the shaper. The n is also known as the degree of the filter.

Because of the slow decay of the pre-amplifier signal, the filtered signal will

have a tail which goes below baseline. This is why a zero must be added to the transfer function to cancel the pole. The placement of the zero should match the added pole. This we can achieve with a transfer function

$$G_s(s) = g_s \frac{1 + t_p s}{(1 + t_s s)^n}. \tag{5}$$

This zero should have a time constant matching the decay in the pre-amplifiers integrator.

For our design, a third degree filter was used. So the transfer function becomes

$$G_s(s) = g_s \frac{1 + t_p s}{(1 + t_s s)^3}. \tag{6}$$

The transfer funtion is used in the Verilog-AMS block with the *laplace_nd()* -function. In the block it is also possible to choose the gain from 4 different values.

- 3'b000 -> 1.25 mV/fC
- 3'b001 -> 10 mV/fC
- 3'b011 -> 30 mV/fC
- 3'b111 -> 50 mV/fC

Also the peaking time can be chosen with the following values:

- 4'b0000 -> 25 ms
- 4'b0001 -> 50 ms

- 4'b0010 -> 75 ms
- 4'b0011 -> 100 ms
- 4'b0111 -> 200 ms
- 4'b1111 -> 400 ms

The signal after the shaper and the zero pole cancellation is shown in Figure 17

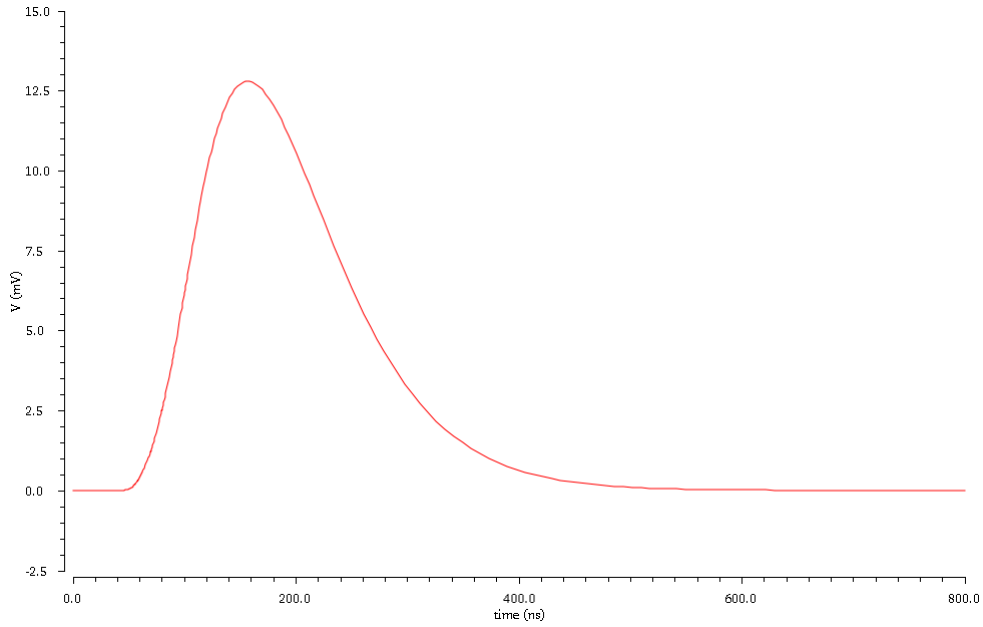

Figure 17: Signal after the shaper. The shape is now a semi-Gaussian.

From the figure it can be seen that the output of the shaper is a semi-Gaussian signal.

3.2.3 Differential Buffer

The purpose of the differential buffer is to give the signal additional amplification and split it into a differential signal. This is done to make the signal

suitable for the next stage, which is the constant fraction discriminator. The gain in the buffer is programmable with the following values:

- 3'b000 -> 1
- 3'b001 -> 2
- 3'b011 -> 3
- 3'b111 -> 4

Also the DC-offset can be adjusted by an external reference voltage. The shape of the signal after the differential buffer is shown in Figure 18.

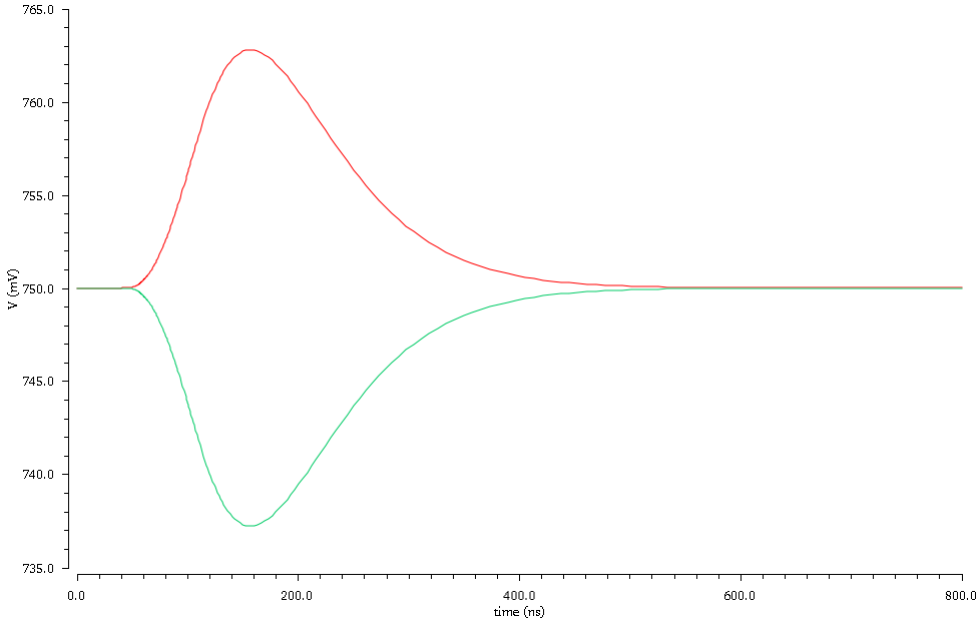

Figure 18: Signal after the differential buffer.

With these three introduced parts, the model is now complete. It takes in a positive or negative current pulse and outputs a differential semi-Gaussian signal, which height corresponds to the charge of the input signal.

4 Simulations

Several simulations were performed for the designed analog front end model to verify the operation. First a triangular input pulse was fed to the model. This pulse has constant time width but varying current value. This input is mainly to test the variation in the gain in the model.

The next input is a square pulse. It has a constant current but the width of the time varies. The aim of this simulation is to test the variation in the shaping time.

As the last simulation a approximation of a realistic Triple-GEM signals were fed to the model. There are three different signals, which have been obtained from the simulations of the Triple-GEM detector [16]

4.1 Trianglular Pulse

The first input for the simulation was a triangular current pulse with rise and fall time both 1 ns. The varying parameter was the pulse height, which was sweeped from -100 uA to 100 uA. This gives us the range of 0 to 100 fC for the input. The negative currents were added so the simulation would cover both hole and electron signals. The sweep was done with ten equally spaced steps, so the simulated input currents were:

- -100 uA
- -77.78 uA
- -33.33 uA
- -11.11 uA
- 11.11uA

- 33.33 uA
- 77.78 uA
- 100 uA

The input sweep is shown in the Figure 19.

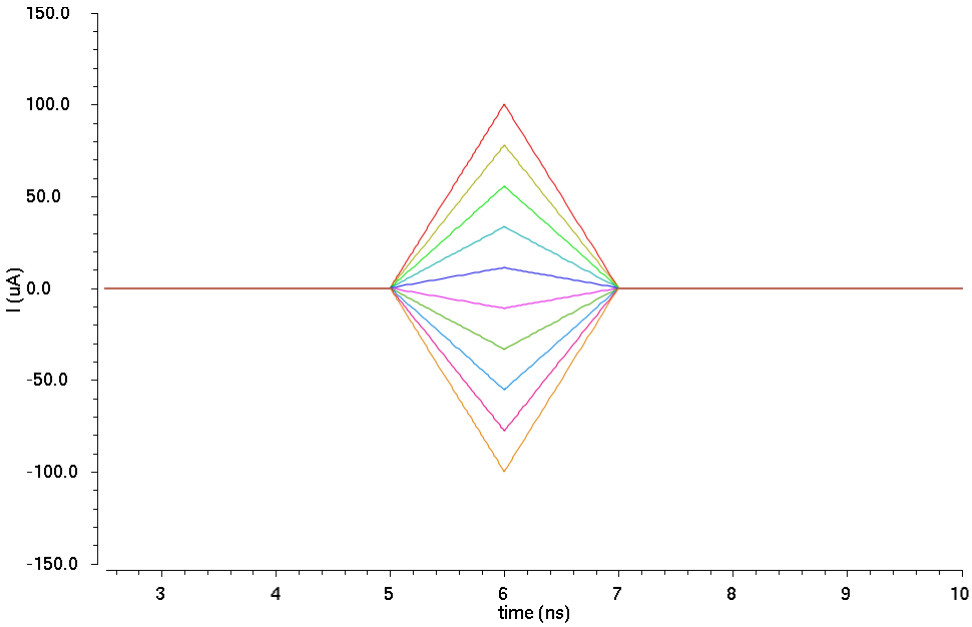

Figure 19: The input current signal. It goes from -100 uA to 100 uA with 10 equal steps.

Output of the pre-amplifier is presented in the Figure 20.

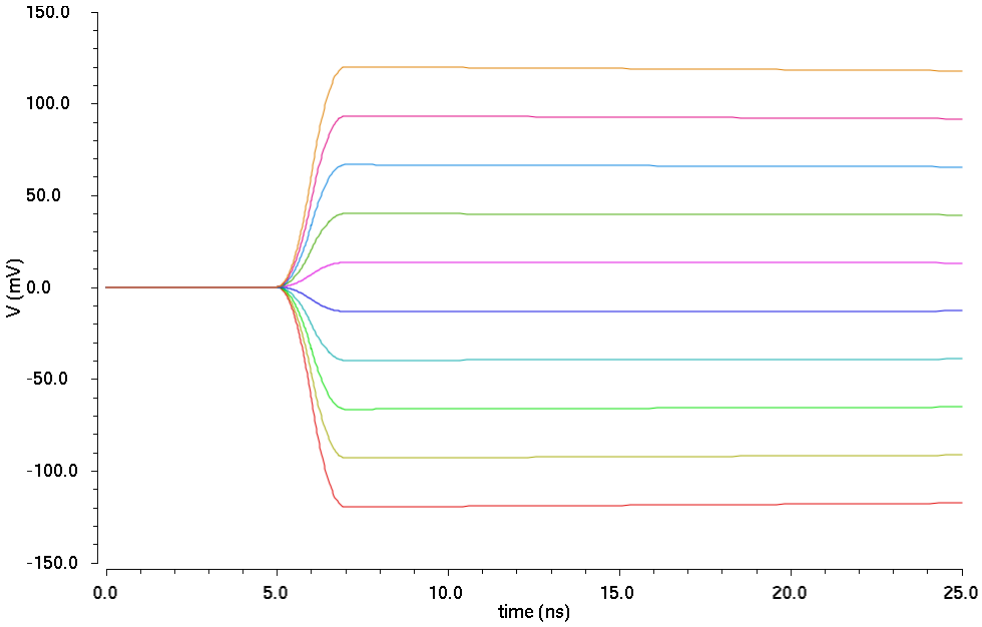

Figure 20: Signal after the pre-amplifier. The shape is a slowly decaying step function.

From the figure it can be seen that the pre-amplifier itegrates the incoming signal and then start to slowly decay.

In the figure 21 the linearity of the pre-amplifier output gain can be seen. The gain is about 1.2 mV/fC and the linearity error is minuscule.

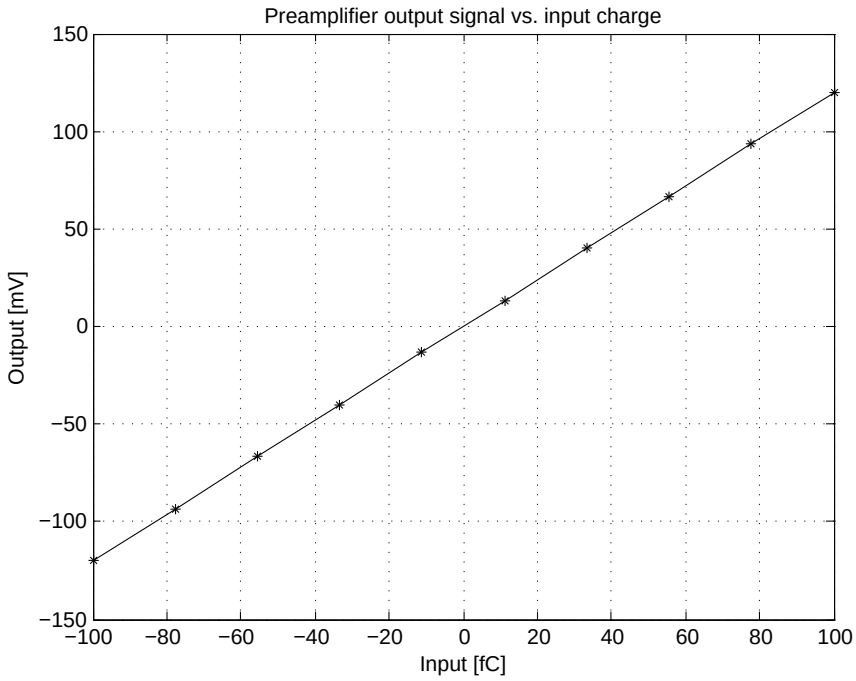

Figure 21: The linearity of the pre-amplifier output gain.

The baseline recovery for the pre-amplifier was defined as the time it takes from the signal to drop from the maximum peak to 5 percent of the signal. The baseline recovery can be seen in the figure 22.

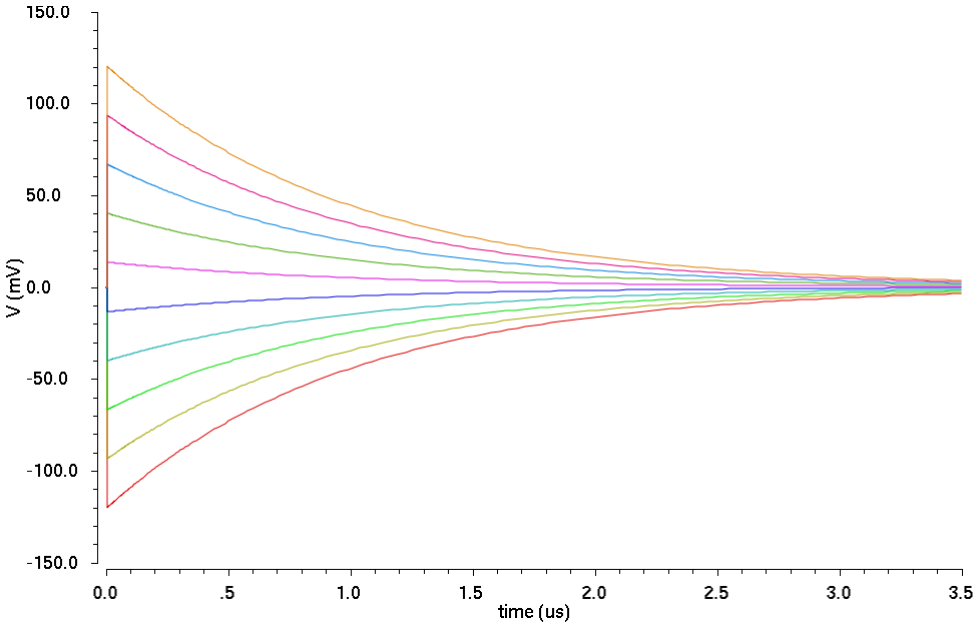

Figure 22: The baseline recovery of the pre-amplifier signal.

From the figure it can be seen that the recovery to the baseline happens in the signals at the 3us point, which is well under the specified maximum value.

Shaper output with the sweep is presented in the figure 23. The peaking time in 100 ns and the variation of the peaking time over the range is less than 0.5 ns. Gain is 30 mV/fC with a variation of 0.2 mV/fC.

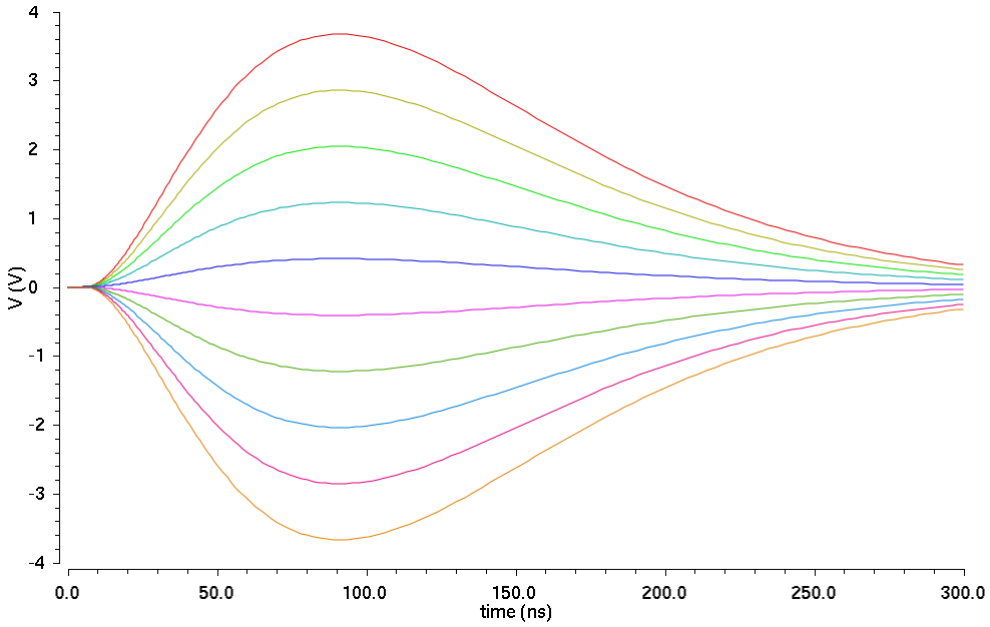

Figure 23: Signal after the shaper, with the gain of 30 mV/fC.

Another shaper output with the sweep is presented in the figure 24. The peaking time in 100 ns and the variation of the peaking time over the range is less than 0.5 ns. Gain is 1.25 mV/fC with a variation of 0.2 mV/fC.

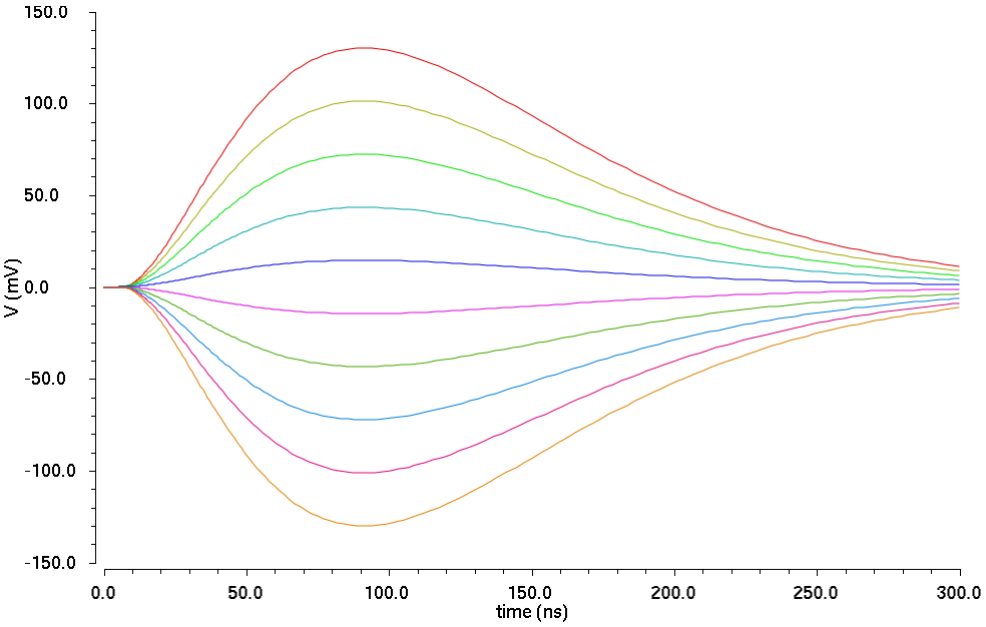

Figure 24: Signal after the shaper, with the gain of 1.25 mV/fC.

With this simulation it can be seen that the behavior of the model is as expected and well in the limits specified in the requirements.

4.2 Square Pulse

The next simulation was done with a square current pulse, which has a constant height. Height of the pulse is 2 uA.

The rise and fall times are also in this case both 1 ns. The varying parameter is the pulse width, which goes from 1 ns to 50 ns with 10 equally spaced steps. The time step parameters are:

- 1ns
- 6.33 ns
- 11.67 ns

- 17 ns
- 22.33 ns
- 27.67 ns
- 33 ns
- 38.33 ns
- 43.67 ns
- 49 ns

With these parameters we get the range of input charges from 2 fC to 100 fC.

The input signals with the duration growing with 10 equal steps can be seen in the figure 25.

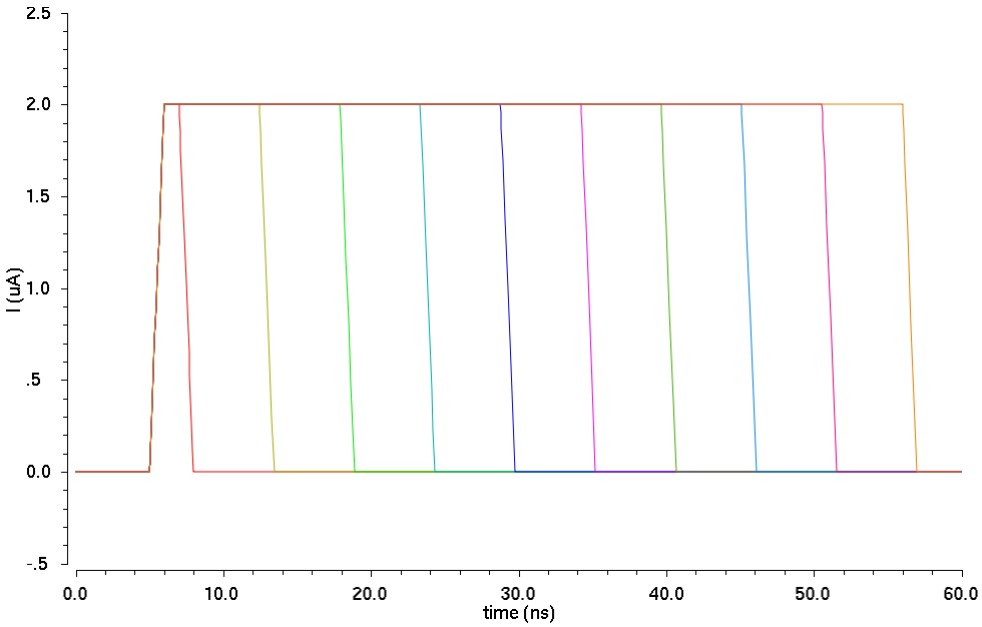

Figure 25: The square input signals with ten equal steps.

In the figure 26 the output of the pre-amplifier can be seen. The amplification is around 2.5 mV/fC.

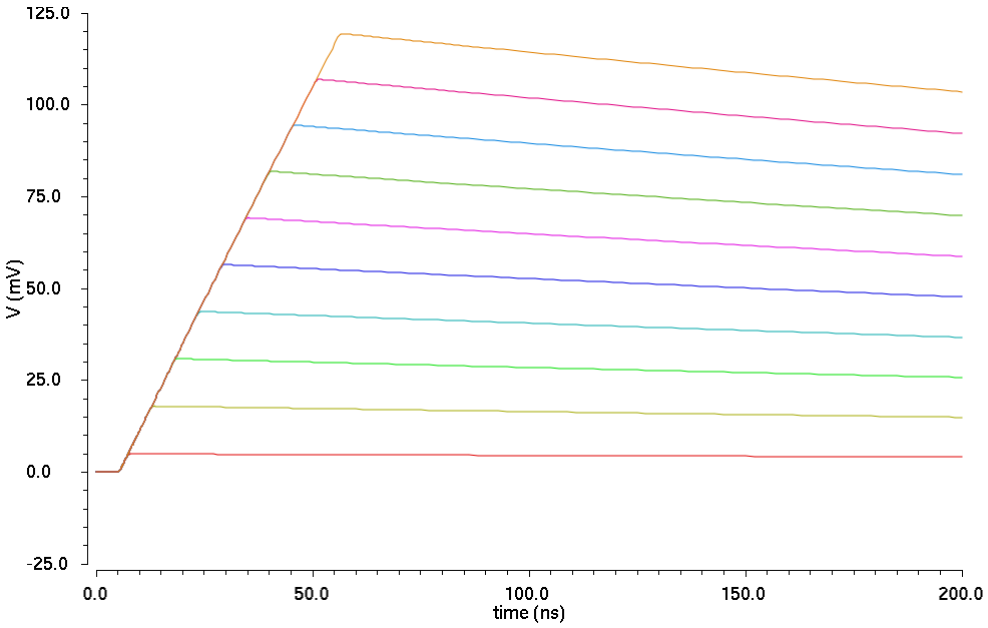

Figure 26: Signal after the pre-amplifier. The shape is a slowly decaying step function.

From the figure it can be seen that the integration time grows with length of the input signal.

The output of the shaper is shown in the figure 27. The amplification is 1.25 mV/fC with a variation of 90 uV/fC.

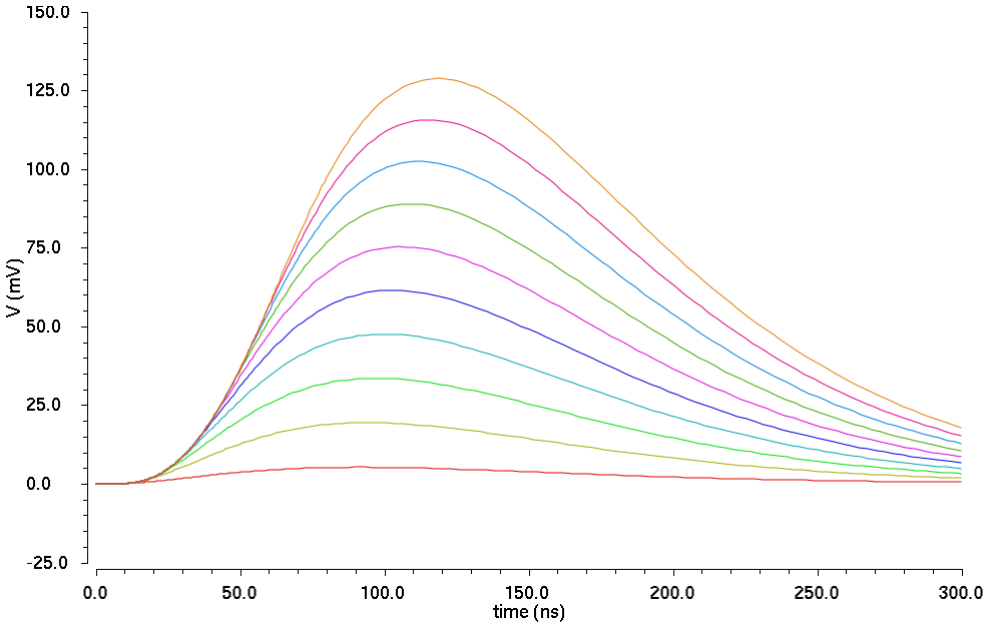

Figure 27: Signal after the shaper.

From the figure it can be noticed that the shaping time varies between the steps. The variation is plotted in the figure 28.

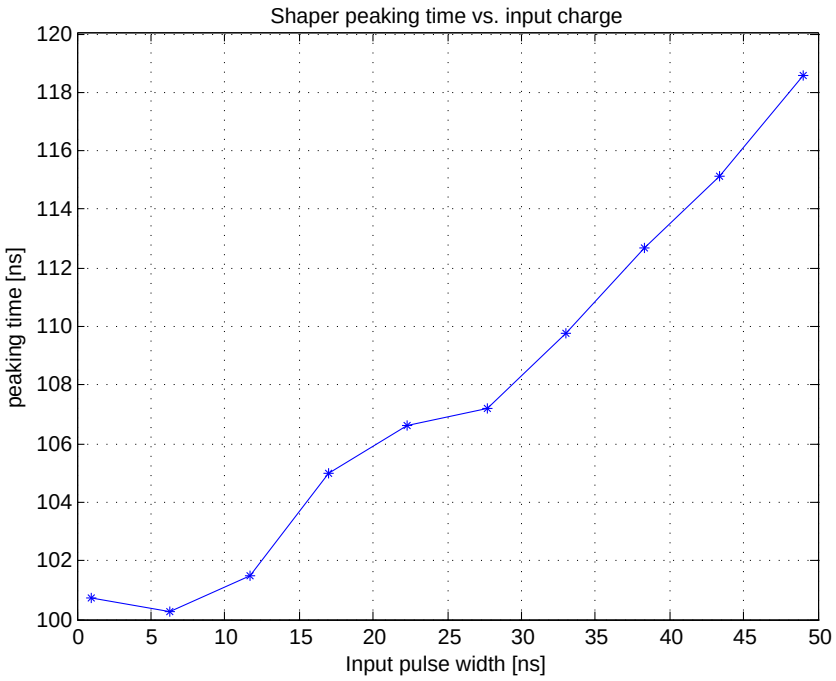

Figure 28: Model of the front end. It consist of a pre-amplifier, a shaper with zero pole compensation and a differential buffer.

The variation over the whole range is 18 ns. This is quite much, but it was expected. Because the longer pulse takes more time for the pre-amplifier to integrate, moves the peaking time accordingly.

The shaping time of the model is now optimized so that the right peaking time is achieved with short pulses. This optimization can be easily adjusted with the model parameters to accommodate the desired behavior.

4.3 Realistic input pulse

Simulations have been made for the output signal of triple-GEM detectors[16]. Three results of these simulations are presented in the figure 29

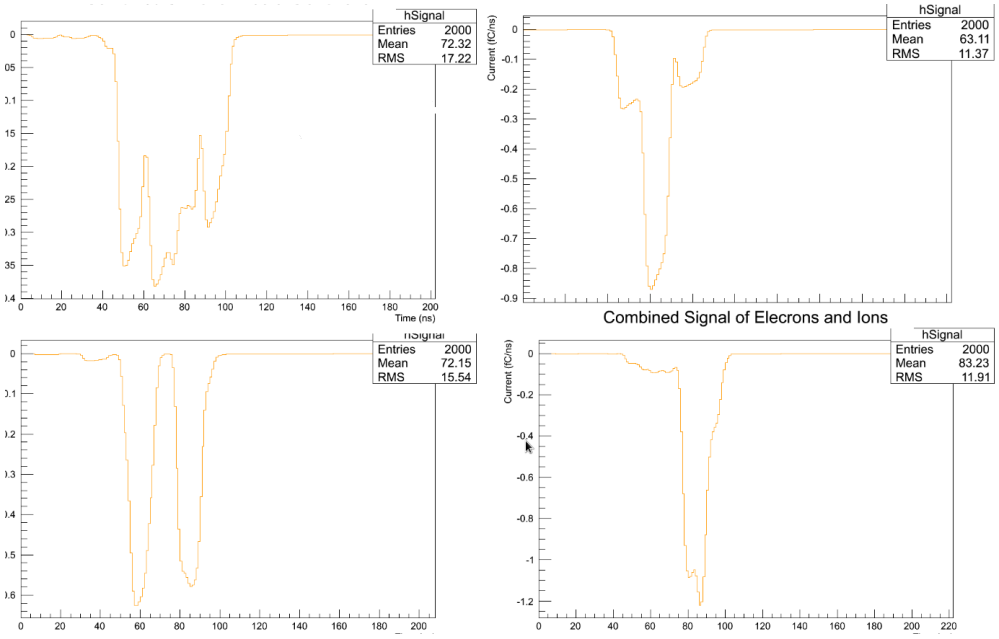

Figure 29: Simulation results of the triple-GEM deterctor output signals.[16]

Three inputs approximating the simulated results were fed to the analog front end model. The peaking time was set to 100 ns and the gain to 1.25 mV/fC. The first signal has three peaks with roughly equal height. The input charge of this signal is 10.2 fC. The input and the output signals are shown in the figure 30

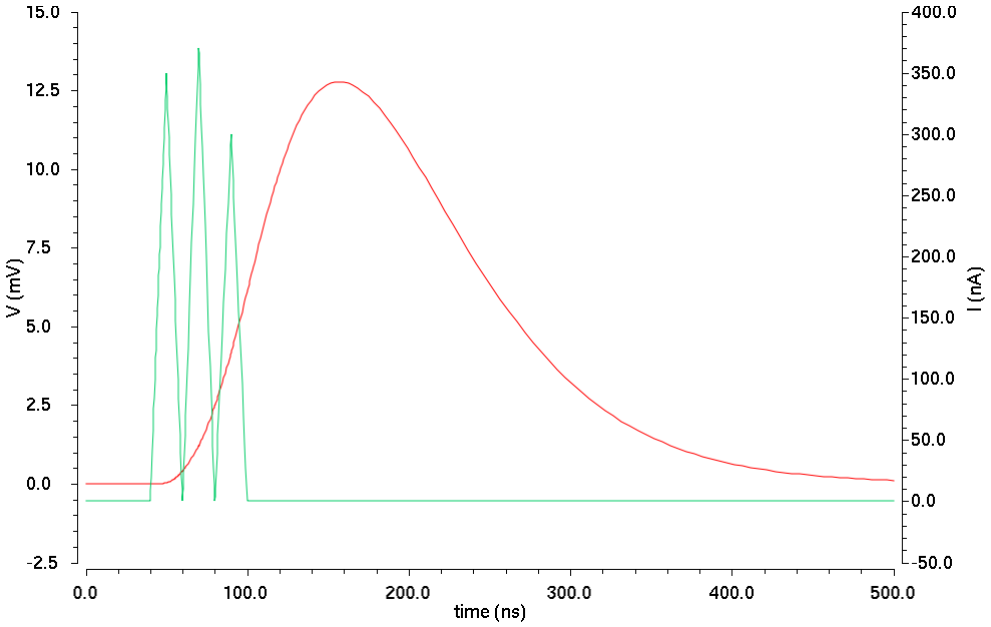

Figure 30: Model behaviour with a realistic 10.2 fC signal.

The peaking time of the shaper output is 102.7 ns and the peak voltage is 12.75 mV. With the 10.2 fC input charge the gain becomes 1.25 mV/fC.

The output of the pre-amplifier is shown in the figure 31

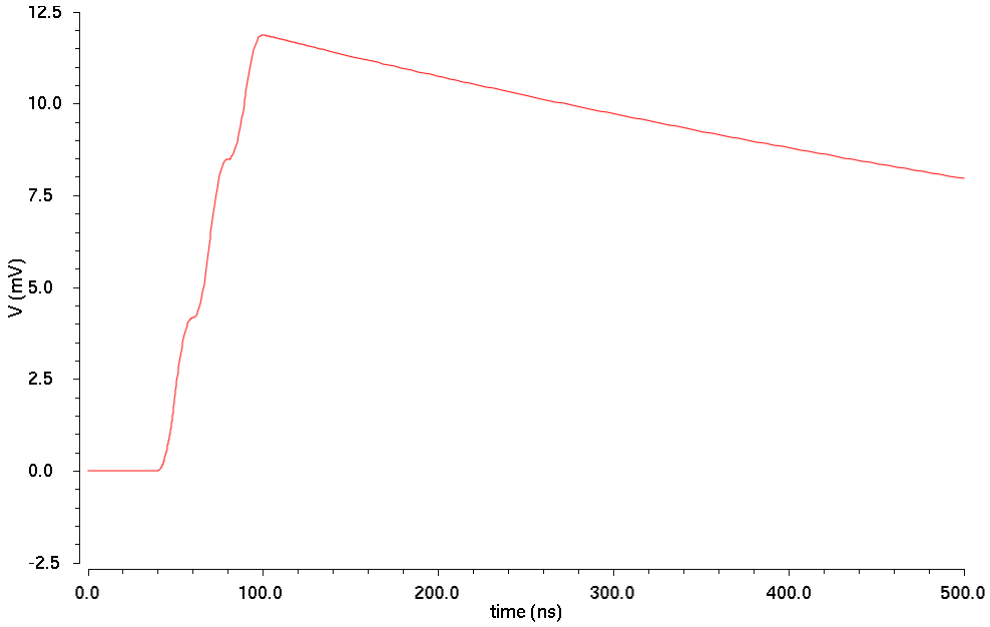

Figure 31: Output of the pre-amplifier with a realistic three peak signal.

From this figure the effects of the multi peak input signal can be seen. The rise of the integration part is not a constant but varies with the peak height and steepness.

The second input signal has also three peaks. Two lower peaks and a higher one in the middle. The charge of this signal is 13.5 fC. The input and the output signals are shown in the figure 32

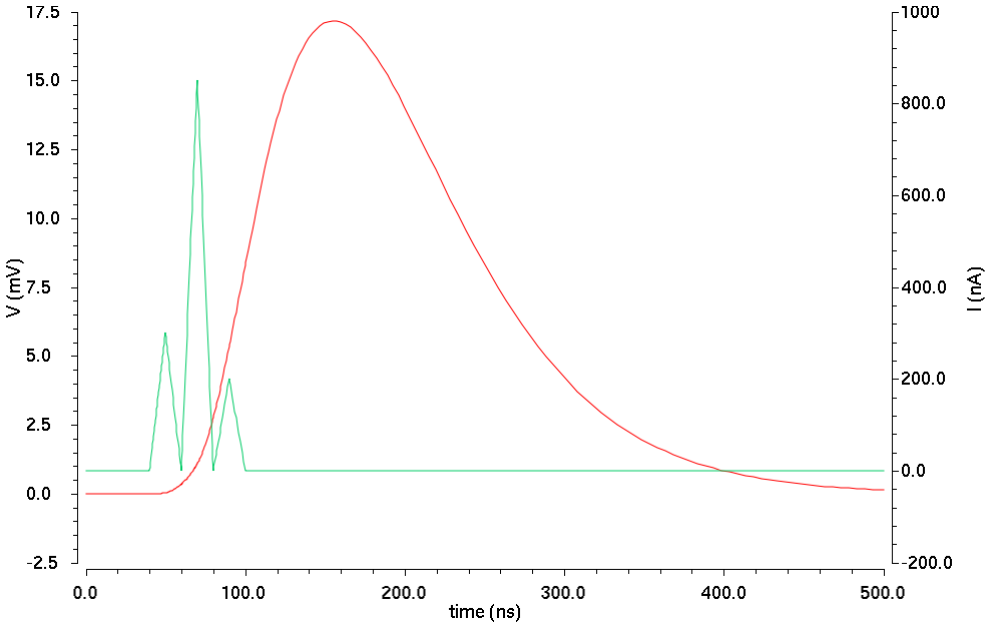

Figure 32: Model behaviour with a realistic 13.5 fC signal.

The shaper has a peaking time 98.5 ns and a maximum voltage of 17.15 mV. Which gives us the gain of 1.27 mV/fC.

The output of the pre-amplifier is shown in the figure 33

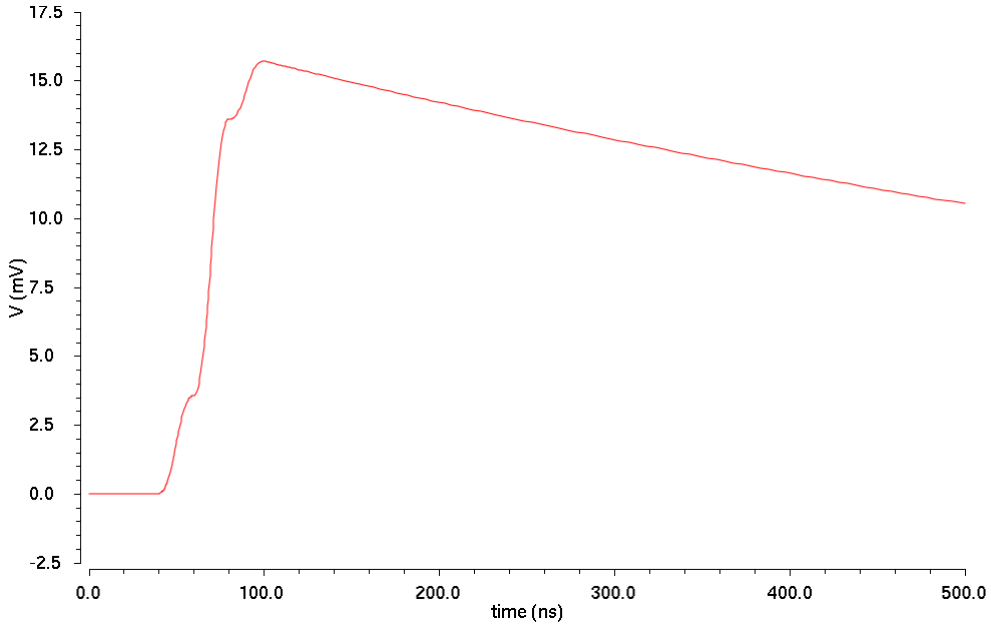

Figure 33: Output of the pre-amplifier with a realistic three peak signal.

The effect of the peaks is visible in this case.

The last signal has two equal height peaks. The charge of this signal is 12 fC. The input and the output signals are shown in the figure 34

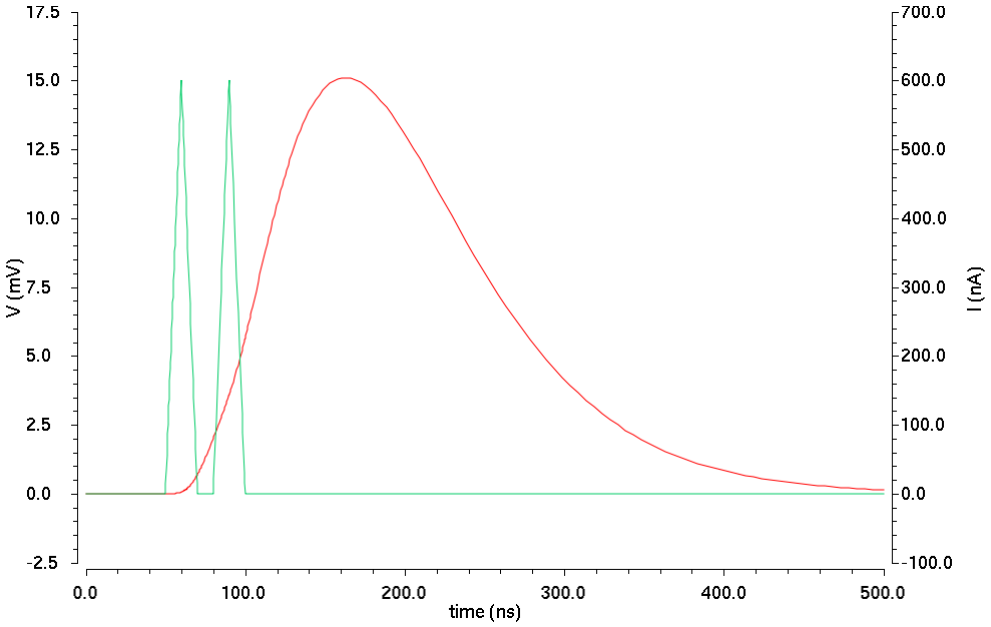

Figure 34: Model behaviour with a realistic 12 fC signal.

In this case the peaking time 100.7 ns and the peak voltage is 15.08 mV. This gives us a gain of 1.26 mV/fC.

The output of the pre-amplifier is shown in the figure 35

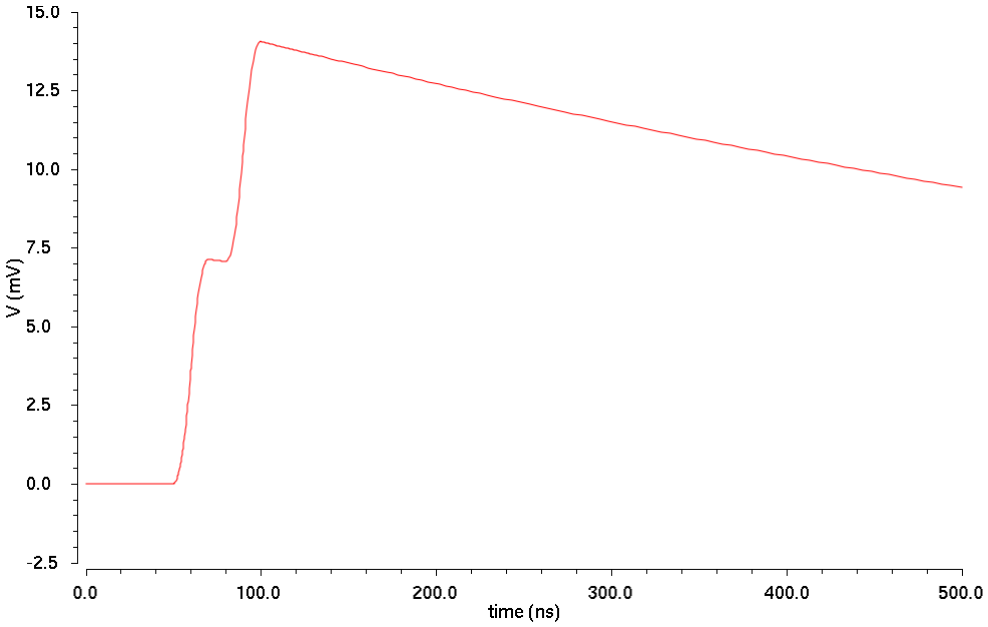

Figure 35: Output of the pre-amplifier with a realistic two peak signal.

In this case the effect of the peaks is clear. After the first peak, the pre-amplifier signal is already starting to decay. Then the next peak occurs and the pre-amplifier signal is raised even higher before the eventual decay phase.

From all of the simulation results it can be seen that the shaping has variation between the signals, which is expected. The linearity of the gain is rather good between the different cases.

5 Conclusions

The aim of the study was to design a Verilog-AMS simulation model for the analog front end. And The actual front end is still under design, so the model should have been easily modifiable to accommodate the final front end design.

The designed model accommodates well the given design parameters. With

the use of transfer functions, the design is also light weight in terms of simulator processing power. This allows it to be used extensively in the simulations of the whole VFAT3 chip. Also by adjusting the model parameters, the model can be optimized to accommodate the parameters of the future analog front end design.

In the future the model can also be developed further to include more specific details.

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