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Janne Hannonen

APPLICATION OF AN EMBEDDED CONTROL SYSTEM FOR AGING DETECTION OF POWER CONVERTER COMPONENTS

Thesis for the degree of Doctor of Science (Technology) to be presented with due permission for public examination and criticism in Room 2305 at Lappeenranta University of Technology, Lappeenranta, Finland, on the 2nd of December, 2016, at noon.

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Abstract

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In modern power conversion applications, the converter fault tolerance and the reliability of a power supply have become key requirements. Condition monitoring of power supplies has been suggested to support these reliability-related requirements in order to indicate and predict an imminent fault resulting from known precursors of component aging. By implementing the power supply control with programmable controllers, enhanced design flexibility and higher integration can be achieved when compared with traditional analog and distributed control systems. In addition, an embedded control system enables condition monitoring to be used in parallel with its main purpose, system control.

In this doctoral dissertation, one solution to digital control implementation for an AC/DC power supply is proposed. The digital control system is applied to condition monitoring in three approaches, the first of which uses a state observer and the two latter output voltage excitations in order to detect aging precursors. The condition monitoring applications only exploit those measurements that are also used for the system control, and thus, no changes to the system hardware are required. The study focuses on analyzing the feasibility of the alternative approaches to detect the converter output stage capacitor aging. In addition, detection

of increased losses in the converter main circuit is investigated by taking the state observer approach.

Each method is tested experimentally as a proof of concept by using the power supply prototype. In the tests, the methods are studied applying artificially generated variations in the components, which are considered to emulate the component aging during the converter lifetime. Thus, the results set a basis for further research on the feasibility of the methods in actual converter aging tests. In addition to the feasibility study, the burden caused by each method on the microcontroller processing resources is assessed.

Keywords: Condition monitoring, Embedded control, Power supply, Aging

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Espoo, November 1st, 2016

Janne Hannonen

Contents

List of publications

This doctoral dissertation is based on the following publications. The rights have been granted by the publishers to include the papers in the dissertation.

I Hannonen J., Ström J. P., Honkanen J., Räisänen S., Pokkinen O., and Silventoinen P. (2013), "Design of digitally controlled isolating 1–phase AC/DC converter by using centralized processing unit," in *15th European Conference on Power Electronics and Applications (EPE)*, Lille, France, pp. 1–10.

II Hannonen J., Honkanen J., Ström J. P., Räisänen S., and Silventoinen P. (2014), "Luenberger state observer based condition monitoring method in digitally controlled switching mode power supply," in *16th European Conference on Power Electronics and Applications (EPE'14-ECCE Europe)*, Lappeenranta, Finland, pp. 1–8.

III Hannonen J., Honkanen J., Ström J. P., Kärkkäinen T., Räisänen S., and Silventoinen P. (2016), "Capacitor Aging Detection in a DC–DC Converter Output Stage," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3224–3233.

IV Hannonen J., Honkanen J., Ström J. P., Korhonen J., Räisänen S., and Silventoinen P. (2016), "Capacitance measurement method using sinusoidal voltage injection in isolating phase-shifted full-bridge DC–DC converter output stage," *IET Power Electronics*, vol. 9, no. 13, pp. 2543–2550.

List of Symbols and Abbreviations

Roman letters

$\boldsymbol{A}$	State space system matrix
a,b,c	Second-order system coefficient
$\boldsymbol{B}$	State space system input matrix
$\boldsymbol{C}$	State space system output matrix
C	Capacitor, capacitance [F]
c	Expected value
d	Duty cycle
$\boldsymbol{e}$	State observer error vector
f	Frequency
$\boldsymbol{I}$	Identity matrix
$\hat{i}$	Current amplitude
i	AC current
I	Current [A]
k	Discrete sample of the kth time instant
$\boldsymbol{L}$	State observer gain matrix
L	Inductance [H]
L	Observer gain matrix coefficient
N	Number of uncertainty elements
n	Transformer turns
Q	Semiconductor switch

$\boldsymbol{r}$	Observer residual
R	Resistance, Resistor [Ω]
r	Second-order system root
s	Laplace transform variable
t	Time
$\hat{u}$	Voltage amplitude
$\boldsymbol{u}$	State space system control vector
U	Voltage
u	Uncertainty
$\hat{\boldsymbol{x}}$	State observer states
$\boldsymbol{x}$	State space system state vector
x	Variable
$\hat{\boldsymbol{y}}$	State observer output
$\boldsymbol{y}$	State space system output vector
Z	Impedance

Greek letters

λ	System eigenvalue
μ	Error in measurement

Subscripts

AC	Alternating current
add	Additional
b	Boost
C	Capacitor
c	Expected value
cal	Calibration
ctrl	Control
DC	Direct current, DC link
end	End of procedure
eq	Equivalent

ESR	Equivalent series resistance
est	Estimation
filt	Filtering
HB	H-bridge
i	AC current
in	Input
k	Leakage
L	Inductor
load	Converter load
loss	Losses
m	Matrix row
n	Matrix column
max	Maximum
meas	Point of measurement
min	Maximum
out	Output
PFC	Power factor correction
r	Ripple
res	Resolution
RMS	Root mean square
s	Sample
sc	Semiconductor
sec	Secondary
start	Start of step excitation
step	Start of step response
sw	Switching
T	Temperature
tot	Total
u	AC voltage

zvs	Zero voltage switching

Acronyms

PF	Power factor
AC	Alternating current
ADC	Analog-to-digital converter
DC	Direct current
EMI	Electromagnetic interference
ESR	Equivalent series resistance
EU	European Union
FPGA	Field programmable gate array
MCU	Microcontroller unit
PFC	Power factor correction
PI	Proportional–integral
PWM	Pulse width modulation
RMS	Root mean square
SMPS	Switching mode power supply
SNR	Signal-to-noise ratio
THD	Total harmonic distortion
VHDL	Very high speed description language
ZVS	Zero voltage switching

Chapter 1

Introduction

Practicality, flexibility, durability. These are commonly required features of power electronics equipment. Power converters are the modern way of interfacing the mains with electrical devices throughout the scale of power levels, from low-power consumer electronics through high-power industrial-scale applications to power transmission. Modern energy politics and markets are spurring more efficient ways to use energy. In the cases where electricity is the dominating factor of the total energy consumed, it is also an attractive target for savings. Power electronics offers solutions to reduce losses in the power conversion process. Loss minimization can also be viewed from an alternative perspective; in power production such as solar, water, and wind power systems, the loss minimization equals a higher energy yield.

Energy costs are not the only driving force to boost the development of power electronic devices. Climate actions such as Kyoto Protocol (United Nations, 1998; UN Framework Convention on Climate Change, 2009), the 20-20-20 EU climate action (European Commission, 2008), and the EU Energy Efficiency Directive (European Parliament, 2012) are prompting more efficient ways to use electricity and energy in general. These regulations and objectives have been indisputably beneficial to the power electronics research and development.

When it comes to the technical aspects and the system-level analysis of the power conversion process, the process efficiency is one of the most important factors: losses generate heat, which has to be removed from the system. Therefore, it is obvious that by reducing losses generated in the power conversion process, the cooling system can also be scaled down, and the system as a whole can be designed lighter and smaller in size. It has also been found that the less the system is exposed to thermal stress (e.g. temperatures close to the specified limit of a specific component, or temperature swings resulting from the cyclic use of power electronics), the better reliability of the power conversion process can be achieved (Ma et al., 2012).

Despite the fact that the modern power converter design aims at more and more reliable systems, the vast majority of technical devices will ultimately wear out and break down as

they age. The wear-out is seen as degraded performance or an increase in disturbances in the system operation. Thus, interest in fault detection and condition monitoring in power converters has been increasing as the role of power converters has become more crucial in the industrial and consumer devices.

This doctoral dissertation focuses on the development of practical condition monitoring methods for power converter systems, which can be used to warn the user of aging-based degradation of operation or a risk of a fault. The objective of the work is to study and develop practical methods for power supply condition monitoring in a digitally controlled power supply. Further, the target of the study is to detect indicators of converter aging such as the reduction of electrolytic capacitance and an increase in losses. The methods are developed so that additional instrumentation or measurements for aging detection are not required. Instead, only the measurements that are primarily used for system control are applied to converter condition monitoring.

1.1 Power conversion process

The power conversion paradigm shift from the bulky line frequency transformer–rectifier power supply towards high-frequency switching power conversion has been made possible by the rapid development of semiconductors, passive components, and control systems. One of the key factors in increasing the power electronic device power density is the use of high-frequency switching of semiconductors. The high-speed switching in combination with the use of magnetic materials with a capability of high flux densities offers significant size reduction in magnetic components compared with their mains-frequency counterparts.

The primary objective in power conversion is to modify the input power of the power converter to the level and form that meet the requirements of the load or power distribution medium. A solar power system, for example, inherently produces direct current (DC) and hence DC power. In order to use the currently available power distribution infrastructure for the electrical energy generated by solar panels, the DC power has to go through power conversion. The DC power is converted into alternating current (AC) with a constant RMS voltage and frequency that meet the grid standards such as 230 V, 50 Hz in the European area. On the other hand, the mains voltage level is usually unsuitable to be directly used in a device. Therefore, power conversion is needed to convert the supply voltage from the mains to a suitable level. A mobile phone battery charger is an example of a small-scale power converter, which rectifies the mains voltage and converts the voltage down to a few volts of DC.

Power conversion can be understood as energy transfer between components, which are able to temporarily store electrical energy. The most crucial circuit components in power converters are the semiconductor switches, capacitors, inductors, and transformers. The circuit comprised of these components is called the main circuit, which provides the path for the throughput power of the converter. The semiconductor switches are used to control the energy balance between the input, output, and main circuit components, thereby controlling

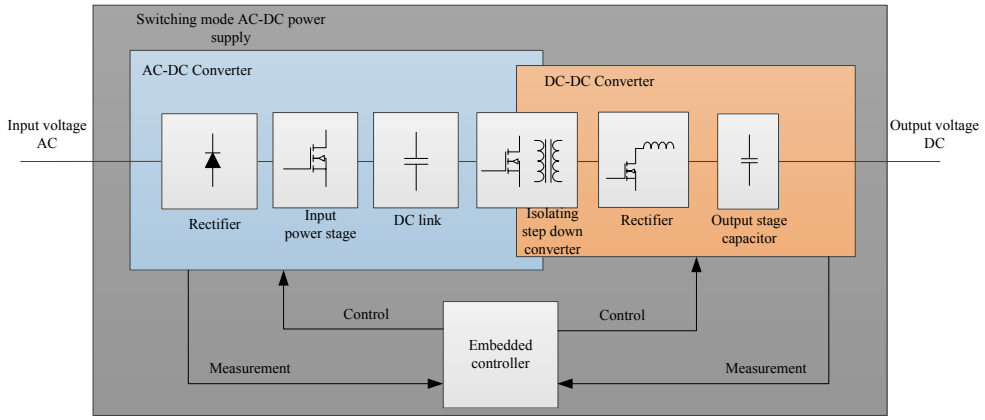

Figure 1.1. Block diagram of a power converter. The model illustrates the key functional elements of a digitally controlled AC/DC power supply.

the power conversion so that the desired functionality is achieved. Obviously, the converter topology, for instance the structure of the main circuit, decides the system operation in the first place.

The main circuit operation is determined by the system control, which gives the switching instructions for the semiconductor switches at the main circuit. The system control itself is a procedure that adjusts the controlled parameter to the given reference according to the feedback signal, which, in most cases, is measurement of the controlled signal such as the converter output voltage. The feedback control objective is to neglect the error value between the reference and the output signal by providing suitable switching instructions for the semiconductor switches in the converter main circuit. The control is also used to keep the converter operation stable within the specified operating range and to produce the required system dynamics. For example in the mobile phone battery charger, the control is needed to maintain the system output voltage stable regardless of the load.

Power system control, as a procedure, is implemented by a controller, which is a physical unit that provides the control among other functions that are required for the power converter operation. Traditional power converter controllers are generally integrated analog circuits, which for example produce the control and switching instructions for certain parts in the main circuit. As the embedded solutions have evolved rapidly, they have become a common approach for power system controllers also in the field of power converters. Embedded control in power conversion applications is generally implemented using microcontrollers (MCU) or field programmable gate arrays (FPGA). Figure 1.1 illustrates a simplified block diagram of an AC/DC power converter, which consists of various active and passive power stages and main circuit components.

1.2 Embedded systems in power conversion

As mentioned above, an embedded controller is an alternative to an analog approach in terms of system control. The embedded system offers a reprogrammable and flexible platform for the power converter control design, yet it requires detailed knowledge of the overall system operation, control implementation, and embedded system design. One of the major benefits of the embedded control system is the easier approach to advanced control methods such as nonlinear, predictive, or robust control compared with analog implementation (Suntio, 2009; Brod and Novotny, 1985; Skogestad and Postlethwaite, 2005). Further, higher integration can be obtained as multiple power stage controls can be implemented into one MCU.

The advantage of the integration is that the system information such as measurement and power stage control data is available, which can be used to obtain nonmeasurable information. This can be done by applying a system model, which is executed during the converter operation. The model can be used to produce an advanced system control or to detect system operation anomalies for example by using state observers and parameter estimation (Isermann, 2011; Algreer et al., 2012).

A digital control system has to be capable of executing time-critical tasks such as system control functions in a given time window. This requirement is referred to as hard real-time operation (Sozanski, 2013). Further, the execution time of the control loop depends on the control bandwidth. Within the control task, the embedded controller generates new switching instructions for the power stage semiconductor switches at the converter main circuit. Modern MCUs are capable of providing not only the computational resources to meet the hard real-time requirement, but also supporting and auxiliary functionalities like a user interface and communication. Self diagnostics and awareness of the operating conditions such as assessment of the converter health and grid quality may be also implemented (Ji et al., 2015; Granados-Lieberman et al., 2011).

1.3 Reliability, fault tolerance, and condition monitoring—state of the art

The reliability and availability have become key issues in power electronics as power converters are widespread throughout the industry and power production. The need for enhanced availability in power conversion processes has resulted in various approaches, such as designs for reliability and system condition monitoring, to improve not only the device reliability, but also the system awareness of its health (Yang et al., 2010; Wang et al., 2012).

Often, the terms and concepts in the discussion on reliability are mixed, and there may be some inconsistency and ambiguity in the use of these terms. Such terms are for example reliability, availability, and lifetime. On the other hand, also condition monitoring is often mixed with reliability.

The concept of reliability can be defined as an ability of an item or a system to work as expected throughout its lifetime in the specified operating conditions. Ideally, a reliable system never fails. Reliability is often quantified by analyzing failure probability or frequency of failures under certain operating conditions (Wang et al., 2012).

In this context, availability means accessibility, in other words, that the power conversion system is not in a faulty state, and thus, it is available for power conversion. The metric for availability is the percentage of the device up-time with respect to the device lifetime. Lifetime, again, is a concept that refers to the total time that the device has potentially been able to operate. Therefore, the device lifetime is the sum of up-time and down-time, counted from the first moment when the device has been installed and set available.

As a concept, condition monitoring is able to detect the phenomena that introduce anomalies to the expected operation over time. Often, this means that the condition monitoring is suitable to prevent failures that are caused by component wear-out, meaning that the components gradually degrade before failure. Thus, the probability to detect early failures, or unexpected faults caused by sudden component failures is low, as these failures show no detectable symptoms of degradation in the same extent as the component wear-out.

In various applications redundancy is used to ensure the system availability. Adding redundancy to the system leads to the concept of fault tolerance. In practice, this means for example adding an extra phase leg to the motor drive inverter, which steps in when one of the normally operating phase legs fails (Bolognani et al., 2000). Redundancy at the system level is also common in critical environments. In these systems, parallel converters are applied for power conversion. Therefore, one converter failure does not compromise the whole system operation.

1.3.1 Approaches to condition monitoring in power electronics

From the perspective of improved availability, a great number of methods have been developed to increase the system robustness and to reduce the risk of failure. In critical applications such as power production, transportation, and telecommunication, the system failure may lead to perilous situations and significant economic issues caused by the non-available system. In these cases, condition monitoring, which detects a degraded performance of system components, can help to foresee the upcoming need for maintenance, and thus improve the availability of the system by avoiding failures in the system (Huang and Mawby, 2013; Ji et al., 2015).

According to (Yang et al., 2011; Lahyani et al., 1998), the most unreliable components in power electronics are the semiconductor switches and the electrolytic capacitors. The most common failure mechanism in semiconductor switches is the solder layer fatigue and liftoff of bond wires as a result of deformation of the solder joint (Ciappa, 2002; Ji et al., 2015). In the case of an electrolytic capacitor, the main reason for degradation is the evaporation or degradation of the electrolyte (Kulkarni et al., 2012; Lee et al., 2008; Harada et al., 1993). The aging effects in capacitors can be seen as higher equivalent series resistance (ESR) and

a decrease in capacitance (Kulkarni et al., 2012).

Numerous methods for observing system health have been presented in the literature. As the electrolytic capacitors and the semiconductor switches are the most frequent fault sources in power conversion devices, they are the most commonly studied subjects in the field of condition monitoring. For example, in (Chen et al., 2014; Xiang et al., 2011), the focus is on detection methods that apply temperature estimation or direct measurement to evaluate changes in the junction temperature, and thus, use the information for monitoring the semiconductor switch health. The switching voltage harmonic analysis has also been shown to be feasible for detecting solder fatigue in semiconductor switches, as the switching characteristics vary with respect to varying junction temperature (Xiang et al., 2012). A transient thermal impedance method has also been found applicable to detect solder fatigue and bond wire liftoff in semiconductor switches (Ji et al., 2015).

The failure mechanisms, capacitor structures, and methods to detect capacitor aging have been exhaustively studied in (Imam, 2007). Commonly, the detection of capacitor aging is based on detecting the increase in the equivalent series resistance (ESR) (Amaral and Cardoso, 2012; Bourgeot, 2010; Harada et al., 1993; Lahyani et al., 1998). In these methods, the ESR is analyzed by using either the ripple voltage over the capacitor or by applying model-based parameter estimation. It has also been suggested that the capacitor ESR is examined directly by measuring the capacitor voltage and current, thereby evaluating the losses, which are directly linked to the ESR value (Aeloiza et al., 2005). In motor drive applications, it has been proposed that the DC link capacitor wear-out can be detected by using current injection to the motor stator current reference (Nguyen and Lee, 2015; Pu et al., 2013).

An emerging method to detect faults in power electronic systems is to monitor component acoustic emissions during system operation. This approach is based on the assumption that the acoustic noise emitted by the component varies with respect to component aging. The acoustic emission is monitored using wide-bandwidth acoustic sensors. The method has been studied for semiconductor power modules and capacitors (Karkkainen et al., 2014, 2015; Smulko et al., 2011).

In addition to detecting faults, the estimation of the remaining useful lifetime with respect to the obtained data has gained interest. As the models are derived for quantitative parameters such as the number of certain power cycles at known temperatures, the models can be applied to assess the remaining useful lifetime of the components by using the measurement data. The models developed for the lifetime estimation are regularly obtained by experimental tests of component degradation (Ciappa, 2002). The model input parameters are gathered by various methods. For example in (Abdennadher et al., 2010), an online capacitor lifetime estimation model has been presented, where the capacitance and the ESR are first estimated by a Kalman Filter approach. The results are then used with models that calculate the development of the equivalent series resistance and capacitance, and estimate the rate of component aging and the remaining hours before a failure in the prevailing operating conditions. In another example, the DC link capacitor equivalent series resistance and capacitance are analyzed in a motor inverter in the idle state of the system (Yu et al., 2012). The proposed method provides a current injection into the load, in this case into the motor phases, and evaluates the

response using a recursive least squares analysis in order to obtain the capacitor parameters. The lifetime estimation is performed by applying a derived model, which can estimate the remaining capacitor lifetime in the prevailing temperature.

1.4 Review on aging mechanisms in different capacitor technologies

In this section, the most common mechanisms for capacitor aging are introduced in brief. Each capacitor technology has its unique advantages and disadvantages in terms of robustness and lifetime. The review covers the most common capacitor technologies used in power converters: electrolytic capacitors, film capacitors, and ceramic capacitors.

1.4.1 Electrolytic capacitors

Electrolytic capacitors are often used in applications where high capacitance per volume is required. The disadvantage of an electrolytic capacitor is that it is polarized and thus not suitable for AC use. The electrolytic capacitor also has a significantly lower lifetime expectancy compared with film or ceramic capacitors. The main reason for aluminum electrolytic capacitor degradation is the evaporation or degradation of the electrolyte (Kulkarni et al., 2012; Lee et al., 2008; Harada et al., 1993). The result of degradation is a decrease in capacitance and an increase in capacitor series resistance (Kulkarni et al., 2012).

The electrolytic capacitor lifetime is the shorter, the higher is the operating temperature, and the higher ripple current through the capacitor is applied. The use of the capacitor in elevated temperatures speeds up the evaporation and degradation of the electrolyte liquid (Kulkarni et al., 2012). The ripple current has a direct impact on the losses defined by the capacitor ESR. The power loss raises the capacitor internal temperature and thus speeds up the electrolyte evaporation process. Figure 1.2. illustrates application- and manufacturing-based root causes of electrolytic capacitor failure. The figure shows that the electrolytic capacitor use with overvoltage, reverse voltage, ripple current, and cyclic use, in addition to various manufacturing process flaws, together constitute the most common root causes for the capacitor failure. Most of the presented failure modes cause a temperature rise inside the capacitor, which again leads to a rise in the inner pressure in the capacitor. The most visible result of the inner pressure rise in the capacitor is the swollen exterior, and in an extreme case, leaked electrolyte caused by an opened vent (Nichicon).

1.4.2 Film capacitors

Film capacitors are used in applications demanding AC use, high insulation resistance, high capacitance stability, large current rating, and pulsed operation capability. Self-healing prop-

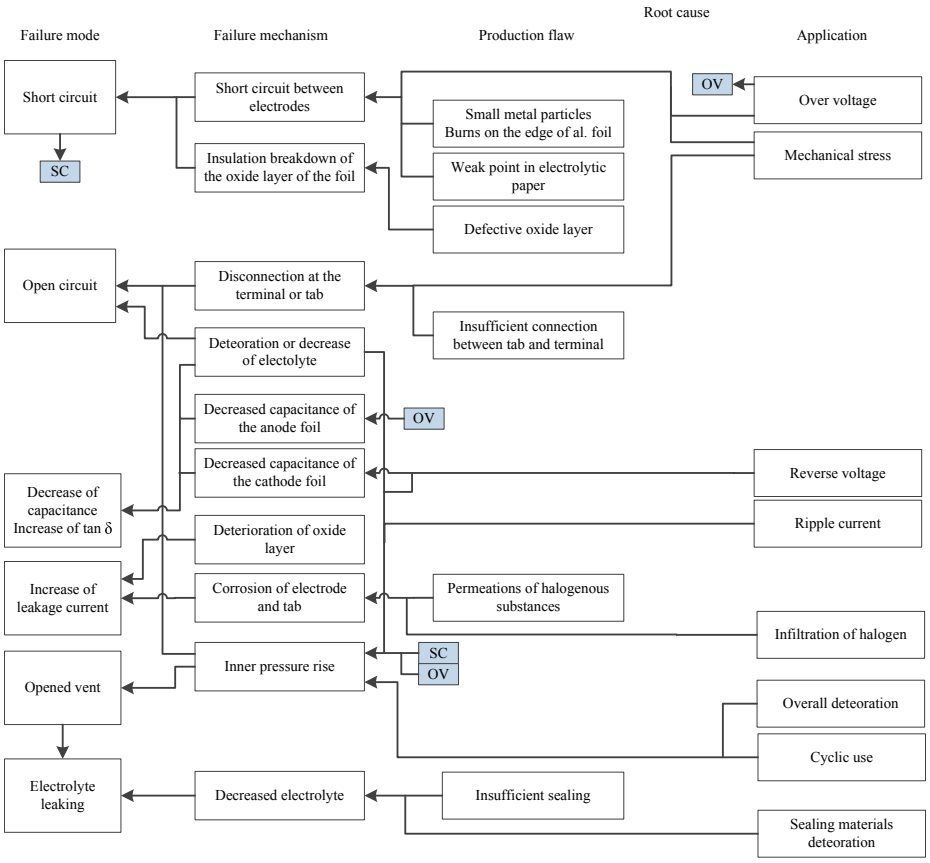

Figure 1.2. Root cause of failures, failure process, and the failure modes of an electrolytic capacitor. The figure is reproduced from (Nichicon).

erties can also be obtained when metallized film capacitors are used (Vishay, 2012).

The most common aging symptom of a film capacitor is the drop of capacitance below the required tolerance. The drop of capacitance often occurs together with an increase in the losses generated in the capacitor. (Gallay, 2014)

In general, the film capacitors are more robust against aging and degradation when compared with electrolytic capacitors. The most common root causes for film capacitor aging are the use of overvoltage, overtemperature, or application in high-humidity environments. As the film capacitors are quite robust against application flaws, the most common root causes for failures and aging arise from manufacturing and design. Design flaws such as too thin a dielectric film, too small an insulation distance, and too large metallization layer tolerances may cause premature failure and reliability issues in film capacitors. In addition, too loose tension control during winding, insufficient drying, and inadequate sealing are factors that may reduce the film capacitor lifetime. Humidity either in the manufacturing process or in

the atmosphere in which the capacitor is used introduces three different failure modes (Gallay, 2014):

1. Electrode corrosion. The corroded electrodes increase the capacitor ESR and thus increase losses generated in the capacitor. The increased temperature resulting from elevated losses speeds up the decrease in capacitance as the capacitor dielectric strength drops with respect to the temperature.

2. Corona. Corona sparking is caused by a decrease in the dielectric strength between the films caused by gas bubbles in the dielectric material, or manufacturing flaws, where the space between the films is not controlled properly. The problem is the more serious, the larger is the void between the electrodes.

3. Decrease in insulation resistance. A decrease in insulation resistance is seen as an increased leakage current.

1.4.3 Ceramic capacitors

Ceramic capacitors are nowadays most often used as surface-mounted components in printed circuit board assemblies. The most common applications are bypass, filtering, and decoupling. The ceramic capacitors are often favored because of their good capacitance per volume ratio. Benefits of the ceramic capacitors are a high stability in capacitance, a low ESR, and good frequency characteristics. The downside with the ceramic capacitors is the brittleness of the capacitor ceramic structure. Thus, the ceramic capacitor type is sensitive to mechanical damage.

The aging phenomenon seen in ceramic capacitors is usually related to a mechanical rupture in the ceramic capacitor body. The most common reason for the capacitor premature aging and failure is cracking, which may occur in manufacturing, assembly, or use. Cracking can be caused by thermal-stress-based micro cracks at the capacitor terminals caused by too hot or too long soldering, impact in the component placing stage of assembly, or mechanical stress caused by a shock force or board flexing (Davis et al., 2000; Gormally et al., 2007).

1.5 Motivation of the study

Nowadays, the power supply control is shifting towards digital control as the embedded control platforms are equipped with sufficient processing power to meet the hard real-time requirements of the power supply control. The excess processing resources outside the control loop allow the execution of system analysis and condition monitoring. In the literature, several different approaches have been proposed for condition monitoring in the field of power electronics, as it was shown above.

Often, the condition monitoring methods are presented and analyzed only from a theoretical perspective, but their feasibility in terms of required processing power is not discussed. For example, the methods that are based on complex models to evaluate the system health usually need a lot of processing time from the digital signal controller. This can compromise the system hard real-time operation, if it is necessary that the condition monitoring system is running in the same control unit as the system control, and the condition monitoring applications require processing at the control loop time level. Further, numerous methods reported in the literature use additional instrumentation, which is specifically designed for condition monitoring purposes only. This leads to a higher burden on the analog circuit system design because of the additional need for measurement signal conditioning and AD conversions.

In this doctoral dissertation, practical condition monitoring methods are developed, and their feasibility for detecting indications of wear–out during converter operation is studied. As the condition monitoring is expected to run alongside the converter power stage control, the applied aging detection methods must be efficient in terms of the processing time requirement. Only the measurement signals used for system control are exploited for condition monitoring, and thus, no changes are required at the hardware level.

The focus of the work is on the detection of a decrease in capacitance and an increase in losses in the output stage of a particular DC/DC converter topology. The aging detection is addressed using three methods, one model-based and two excitation-based methods, which are developed for an experimental, digitally controlled power converter prototype. In the model-based method, a state observer is used to detect the changing system component parameters. The excitation methods are studied by producing a known excitation to the converter output voltage and evaluating the output stage capacitor condition from the response.

This work is part of an industry-driven project, done in collaboration with Lappeenranta University of Technology, and a Finnish power supply manufacturer Powernet Oy. In the project, a digital control was designed and implemented for a power supply, which was originally controlled using traditional analog control methods and integrated circuits. In addition to the primary objective, which is to improve the control system scalability, one target of the project was to study and develop methods that bring additional value for the converter by the use of an embedded system alongside its primary function, that is, the power supply control.

The converter used in the study is originally a power supply platform applied to product development by the above-mentioned cooperation partner. The applied converter technology is designed to supply auxiliary power for train control equipment. This introduces the demand for a high availability of the system, as a complete failure of the power supply system may lead to substantial economical losses and can even introduce a danger for life.

The power supply under study is a standalone converter unit, which also allows it to be connected in series or parallel with similar converters. Different variations of power supply construction can be used to meet the required voltage level and supply capacity. As a set of individual power supplies together constitute a larger unit that provides power for the application, the system-level reliability and availability are arranged with redundancy. In order to reduce the need for excessive redundancy, information of the power supply health at

the unit level is required so that proactive maintenance can be carried out before any failure caused by component wear-out occurs.

1.5.1 Research questions and the applied research methods

The feasibility of the developed condition monitoring methods is evaluated by studying how well they are able to detect aging, what their limitations are, whether the methods are usable with the presented converter with both AC and DC power inputs, and how much processing resources the method requires in the control loop. The developed methods are experimentally verified, and therefore, also the presentation of the experimental device is emphasized.

The main research questions of the doctoral dissertation are:

- Which indicators of aging can be detected without using external instrumentation?
- Which kinds of excitations are required to detect aging of the output stage capacitor?
- Considering each proposed method, how does the DC link voltage ripple caused by the AC power input affect the feasibility of the method?
- What are the requirements that the proposed methods set for the controller processing resources?

In the study, research methods such as mathematical analysis, simulations, and experimental tests are used. A mathematical approach is adopted to derive models, to validate the operation of the method, and to assess parameter sensitivity. Each of the presented aging detection methods is verified experimentally with a digitally controlled prototype. In the analysis, also simulation tools such as Matlab Simulink are used.

1.5.2 Outline of the doctoral dissertation

In addition to the introductory chapter, the dissertation comprises five chapters: Chapters 2–5 follow the publications that are linked to this work. The condition monitoring methods presented in this doctoral dissertation are experimentally studied using a converter prototype, the key parameters and control system design aspects of which are shown in Chapter 2. In Chapter 3, the model of the DC/DC converter is introduced, and the model is applied to condition monitoring using a state observer. The feasibility of the method to detect a decreasing output stage capacitance and increased losses at the DC/DC converter is assessed. Chapters 4 and 5 focus on excitation-based condition monitoring methods that are used to detect capacitor degradation at the DC/DC converter output stage. Finally, in Chapter 6, conclusions are drawn from the key results of the work, and suggestions for future work are given.

1.6 Scientific contributions

The contributions of the doctoral dissertation are linked to the journal and conference publications listed in Table 1.1.

Table 1.1. Conference and journal publications comprising the doctoral dissertation.

	Publication I	**Publication II**	**Publication III**	**Publication IV**
Title	Design of Digitally Controlled Isolating 1-phase AC/DC Converter by Using Centralized Processing Unit	Luenberger State Observer Based Condition Monitoring Method in Digitally Controlled Switching Mode Power Supply	Capacitor Aging Detection in DC-DC Converter Output Stage	Capacitance Measurement Method Using Sinusoidal Voltage Injection in Isolating Phase-Shifted Full Bridge DC-DC Converter Output Stage
Authors	J. Hannonen, J.-P. Ström, J. Honkanen, P. Silventoinen, S. Räisänen, O. Pokkinen	J. Hannonen, J. Honkanen, J.-P. Ström, P. Silventoinen, S. Räisänen	J. Hannonen, J. Honkanen, J.-P. Ström, T. Kärkkäinen, P. Silventoinen, S. Räisänen	J. Hannonen, J. Honkanen, J.-P. Ström, J. Korhonen, P. Silventoinen, S. Räisänen
Forum	15th European Conference on Power Electronics and Applications (EPE), Sept. 2013	16th European Conference on Power Electronics and Applications (EPE'14-ECCE Europe), Aug. 2014	IEEE Transactions on Industry Applications, July 2016.	IET Power Electronics, Oct. 2016.
In brief	Overview of a digitally controlled AC/DC converter: Presentation, topology, digital controller, and control principle.	Application of a converter model and a state observer for detecting aging of the secondary circuit components in an isolating DC/DC converter.	Output voltage step method for electrolytic capacitor aging detection in the output stage of the DC/DC converter.	Using sinusoidal voltage injection on the DC/DC converter output and evaluating the capacitor size by the capacitor impedance

Publication I addresses the implementation and use of a digital control system in power supply control. As a case study, a digital control system is implemented on an isolated AC/DC converter using a centralized control unit. The system operation is verified by experimental tests, the results of which are used to analyze the feasibility of the designed digital control system. In the publication, the focus is on the signaling, measurements, and control of the power stages of the converter. Further, the feasibility of several embedded system platforms in power converter applications is discussed.

The author's contribution to Publication I: the principal author of the paper. The sections 'PFC control' and 'Phase Shifted Full Bridge' have been written by Jari Honkanen, M.Sc.

Publication II presents a model-based approach to detect the aging effects of a phase-shifted DC/DC converter. The DC/DC converter used in the study is the isolating converter part of the AC/DC converter in Publication I.

The converter health is monitored by analyzing the error parameter behavior between the state observer output and the measured value. The analytical model of the converter produces a reference value, which ideally corresponds to the measured value of the inverter. It is expected that the measurements start to deviate from the model output with respect to aging of the components in the converter main circuit. Because of the modeling errors and nonmodeled

features such as the reduced model order, a state observer (a Luenberger observer) is used. The observer error value is introduced with variations as the components in the main circuit age and their parameters vary. The error value variation is used as an indicator of wear-out or a fault.

The publication provides an analytical model of the DC/DC converter and the observer design, which are executed online alongside the main circuit control. The paper discusses detection of an increase in losses and aging of the output filter capacitor applying the proposed observer method. As a conclusion, the paper suggests that the method is suitable for the detection of an increase in losses in the DC/DC converter.

The author's contribution to Publication II: the principal author of the paper.

Publication III introduces a practical method for defining the capacitor condition by producing a voltage step at the converter output voltage and analyzing the response. When an electrolytic capacitor ages, the capacitance decreases and the equivalent series resistance increases, which have an effect on the dynamics of the output circuit. Hence, the capacitor degradation is detected from an increase in the voltage, which is measured in a predefined and constant evaluation point of the step response.

The publication reports the design, sensitivity analysis, implementation, and experimental tests of the voltage step method. The study has been conducted on the DC/DC part of the AC/DC converter shown in Publication I. The publication discusses the feasibility of the proposed method. It is stated that the method in the suggested form is suitable only in a system where the load is either resistive, or it has a known, unchanging reactive behavior. This is due to the fact that the load capacitance has a direct impact on the measurement, as it is parallel to the capacitance in the converter.

The author's contribution to Publication III: the principal author of the paper.

Publication IV proposes a practical method to assess the capacitance at the converter output stage. The capacitance is evaluated by producing a single-frequency sinusoidal voltage injection into the converter output voltage reference. The sinusoidal voltage component at the converter output voltage generates a sinusoidal current through the output stage capacitor. The generated current amplitude depends on the capacitor impedance, which, again, is defined by capacitance, assuming that the injection signal frequency is significantly lower than the capacitor self-resonance frequency.

The publication provides the analysis, implementation, and experimental verification of the method. The analysis describes the principle of the detection method and discusses the issues associated with the capacitor aging detection based on equivalent series resistance. The practical part addresses implementation issues such as how to obtain the capacitor current in a converter system where the converter secondary current has to be estimated.

In the publication, the results are presented and analyzed by taking into account the measurement uncertainty in order to show the feasibility of the method against known sources of

errors and undefined disturbances that cause variation on the measured result. The uncertainties are evaluated from environmental and implementation perspectives, and the results are reported following the established practices according to (JCGM, 2008).

The scientific contribution of the paper is to show the feasibility of the method to detect aging of the output stage capacitor during converter operation. One key result is that the method is insensitive to the load structure. This is demonstrated experimentally by testing the proposed method with several load currents using resistive and capacitive loads. Another key result is the method validation in contrast to traditional methods, where the assessment of increasing ESR has been used to detect the capacitor aging.

The author's contribution to Publication IV: the principal author of the paper. The topics presented in the publications have been developed in collaboration with the first two authors of the paper.

1.6.1 Other publications and contributions

The author of the doctoral dissertation has contributed to other publications in the field of power electronics and system monitoring, which are not appended to this work. These publications are listed in the following.

Powernet Oy (2015), "On-line DC-DC Converter Output Stage Capacitor Aging Detection Method Using Stepwise Excitation Signal," Inventors: Hannonen, J., Honkanen, J. Finnish patent application 20145486, issued Jan. 11, 2015.

A patent regarding Publication III has been granted. The author's contribution: the principal author of the invention.

Hannonen J., Honkanen J., Ström J. P. , Kärkkäinen T., Räisänen S., Silventoinen P. (2015), "Capacitor aging detection in DC-DC converter output stage," In *IEEE Energy Conversion Congress and Exposition (ECCE)*.

The publication is the earlier conference paper version of Publication III. The author's contribution: the principal author of the paper.

Honkanen, J., Hannonen, J., Ström, J-P., Räisänen S., Silventoinen, P. (2015), "Active Power Factor Control Design Based on Lyapunov Theory," In *Proceedings of the 17th European Conference on Power Electronics and Applications (EPE).*

The publication introduces a power factor correction control design based on a one-phase AC-DC converter boost-rectifier applying Lyapunov stability criteria. The author's contribution: participation in the writing process and contributing to the experimental tests.

Sankala, A., Korhonen, J., Hannonen, J., Ström J-P., Silventoinen, P. (2014), "Flux and Winding Current Balancing Control for a Medium-Frequency Six-Winding Transformer," In *IECON 2014 – 40th Annual Conference of the IEEE Industrial Electronics Society.*

The publication proposes a 6-winding one-phase transformer flux control method for medium-voltage applications. The method is used to prevent the flux walking phenomenon, which could lead to the core saturation and a possible system malfunction. The author's contribution: participation in the writing process and the presenter of the paper at the conference.

Kärkkäinen, T. J., Talvitie, J. P., Kuisma, M., Hannonen, J., Ström, J-P., Silventoinen, P. (2014), "Acoustic Emission in Power Semiconductor Modules - First Observations," *IEEE Transactions on Power Electronics*, Volume: 29, Issue: 11.

The publication provides a new approach to identify an IGBT module using acoustic emission. The author's contribution: participation in the paper writing process.

Chapter 2

Digital Power Supply Control

Traditionally, the control of switching mode power supplies (SMPS) has been implemented using integrated analog circuits. Despite the fact that analog circuits provide a feasible and simple approach for converter control, digital controllers have started to gain ground in control systems. This is because of the higher integration, better scalability, and enhanced design flexibility of control algorithms when a digital control system is used (Totterman and Grigore, 2012; Suntio, 2009; Balogh, 2005).

This chapter introduces the switching mode power supply and the control platform applied to study the detection of aging in the following chapters. The control system under study is tested experimentally by assessing the converter performance both in static and dynamic operation. In addition, embedded control operation is investigated in terms of the processing resources required by the digital controller.

In the discussion section, the feasibility of the applied control system is analyzed. Further, signal conditioning problems in digital control systems are addressed and discussed. The chapter is related to the study presented in Publication I.

2.1 AC/DC Power converter

The converter used in the study is an AC/DC power supply, which produces an isolated 24 V DC voltage and a maximum of 125 A load current when using a 230 V, 16 A AC input. In addition to a passive diode rectifier at the converter primary, the system consists of three actively controlled power stages:

- Parallel boost converter for power factor correction (PFC) and DC link voltage control

- Isolating step-down converter, using a phase-shifted H-bridge and zero voltage switching (ZVS)
- Current doubler synchronous rectifier

The first item constitutes the AC/DC converter together with the passive diode rectifier at the converter input. The two latter items comprise the isolating step-down DC/DC converter. In Figure 2.1, the construction of the converter main circuit and the measurement circuits are presented.

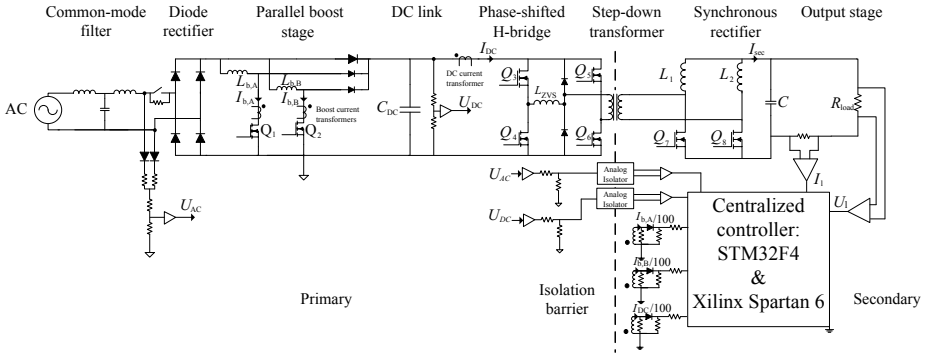

Figure 2.1. Main circuit of the AC/DC power supply and the measurement signals for the system control. The control unit is placed on the isolated secondary side of the converter.

The first active power stage on the mains side of the converter is the boost stage, which provides power factor correction and DC link voltage regulation. The power stage modifies the converter input current to correspond to the mains voltage waveform, and thus, the power factor in an ideal case is 1.

The PFC power stage is implemented by two interleaved parallel boost converters, meaning that two boost converters are operated 180° phase shifted. The topology reduces the conduction losses (I^2R) and current stresses in the switching components compared with a single-switch boost topology as the current is divided between two switches instead of one (Choudhury et al., 2013). Further, the current ripple seen at the mains is significantly lower than in the single switch boost topology, because the interleaved parallel boost converters generate current ripple in opposite phases. As a result, the apparent switching frequency is doubled, and partial current ripple cancellation is achieved (Jang and Jovanovic, 2007).

The second active main circuit element is the primary-side phase-shifted H-bridge, which operates the step-down transformer. This power stage provides output voltage control, galvanic isolation, and voltage level conversion between the primary and the secondary. The H-bridge is operated in ZVS conditions, which reduces switching losses compared with a hard-switched topology. The current range for the soft switching ZVS conditions is defined by the transformer series inductance, which consists of an external ZVS inductance L_{ZVS} and the transformer leakage L_σ. In general, the converter produces zero voltage switching with the lower current, the larger is the series inductance at the transformer. The soft switching

range in a phase-shifted H-bridge with respect to load current has been discussed in (Yan et al., 2003).

The third active part in the main circuit is the secondary current doubler circuit with synchronous rectification. In the rectifier bridge topology under study, the high-side diodes of a conventional rectifier are replaced with inductors as shown in Figure 2.1. The topology effectively divides the rectifier input voltage by two and doubles the input current (Kutkut et al., 1993).

The use of a synchronous rectifier reduces rectification losses compared with passive, diode-based rectification. The synchronous rectifier is implemented using MOSFETs, which are controlled synchronously with the primary switches. The rectifier switch Q_8, shown in Figure 2.1, is controlled with the same switch command as Q_3, and correspondingly, the switch Q_7 with the switch command of Q_4 (Mappus, 2003). This topology introduces a resistive path for the rectifier current so that the power stage losses are proportional to the switch on-state resistance rather than the rectifier diode threshold voltage. By choosing and paralleling switches with a low on-state resistance, losses can be minimized when the rectification is compared with a diode rectifier, the losses of which are correlated with the PN junction voltage drop (Chiu et al., 2004). In the presented experimental converter case, three parallel MOSFETs correspond to the switches Q_7 and Q_8.

The converter operation is controlled using an embedded controller, which is located on the isolated secondary side. In the proposed converter design, all signals required for the system control are measured using an MCU internal analog to digital converters (AD converters). Therefore, all the primary-side measurement signals and primary-side switch command signals have to be isolated. The isolation is achieved by various different solutions: a silicon dioxide barrier isolation is used for the primary-side voltage measurement, current transformers for the current measurement, optical isolation for the PFC switch command, and pulse transformers for the H-bridge switch command signals. In addition to various primary-side measurement and control signals, the converter load current and the output voltage are measured for control purposes.

In Figure 2.2, the prototype converter is illustrated, and the key elements of the experimental device are indicated. Table 2.1 shows the converter parameters.

2.1.1 Embedded control system

The converter control is implemented using a control unit, which consists of a floating-point MCU and FPGA. A XynergyXS embedded control system was chosen for the converter control because of the performance of the ARM Cortex-M4 STM32F407 controller and flexibility offered by the Xilinx Spartan 6 FPGA (DSP Systeme GmbH, 2012). The approach is referred to as a centralized control system, where all the control signals, starting from the measurement signals and leading to the semiconductor switching commands are executed on a single platform. The control unit operation is divided between the MCU and the FPGA so that the MCU is used for the system control algorithms, measurements, communications, and

Table 2.1. Parameters of the AC-DC converter.

Parameter	Symbol	Value	Unit
Input voltage	U_{AC}	230	$\mathrm{V_{RMS}}$
DC link voltage	U_{DC}	400	V
H-bridge switching frequency	f_{HB}	60	kHz
PFC switching frequency	f_{PFC}	100	kHz
Nominal output voltage	U_{out}	24	V
Maximum output current	I_{max}	125	A
Nominal output power	P_{out}	3	kW
Transformer turns ratio	n	9.68	-
Secondary inductance	$L_{1,2}$	30	µH
Nominal output capacitance	C	23.7	mF
Nominal DC link capacitance	C_{DC}	1.5	mF
ZVS inductance	L_{zvs}	13	µH
Transformer leakage inductance	L_{σ}	2	µH
PFC boost inductance	L_{b}	500	µH
Microcontroller AD resolution	–	4096 (12 bit)	
AC current measurement resolution	$I_{\mathrm{DC,res}}$	0.008	A / bit
DC link current measurement resolution	$I_{\mathrm{DC,res}}$	0.008	A / bit
AC voltage measurement resolution	$V_{\mathrm{AC,res}}$	0.1	V / bit
DC link voltage measurement resolution	$V_{\mathrm{DC,res}}$	0.12	V / bit
Output current measurement resolution	$I_{\mathrm{load,res}}$	0.004	A / bit
Output voltage measurement resolution	$V_{\mathrm{out,res}}$	0.0078	V / bit

other application algorithms, while the FPGA provides the pulse width modulation for each power stage and generates synchronous current measurement timing signals. A more detailed presentation of power stage control operations such as the modulation and measurement triggering procedure is given in Publication I.

The power stage control system consists of PFC and H-bridge controllers, both of which are implemented as cascaded voltage and current controllers. In addition to producing sinusoidal input current on the mains, the PFC stage boosts the converter DC link voltage from rectified 1-phase AC to 400 V. The converter is expected to produce 24 V output voltage with ± 1 V voltage regulation. There is also a requirement to limit the output power to the maximum of 3 kW in overcurrent situations. Each control loop is implemented using a PI control structure except for the H-bridge current control, which is carried out using robust optimal control. The objective of the robust control is to take into account the uncertainty and unknown dynamics in the control system. The PFC control design is discussed in (Honkanen et al., 2015), and the optimal robust H-bridge control design will be described in future publications. A more detailed presentation of the PFC and H-bridge controls is outside the scope of this doctoral dissertation.

Hard real-time operation is required for control loop execution in digital control systems. This means that the microcontroller must be capable of executing the power stage control

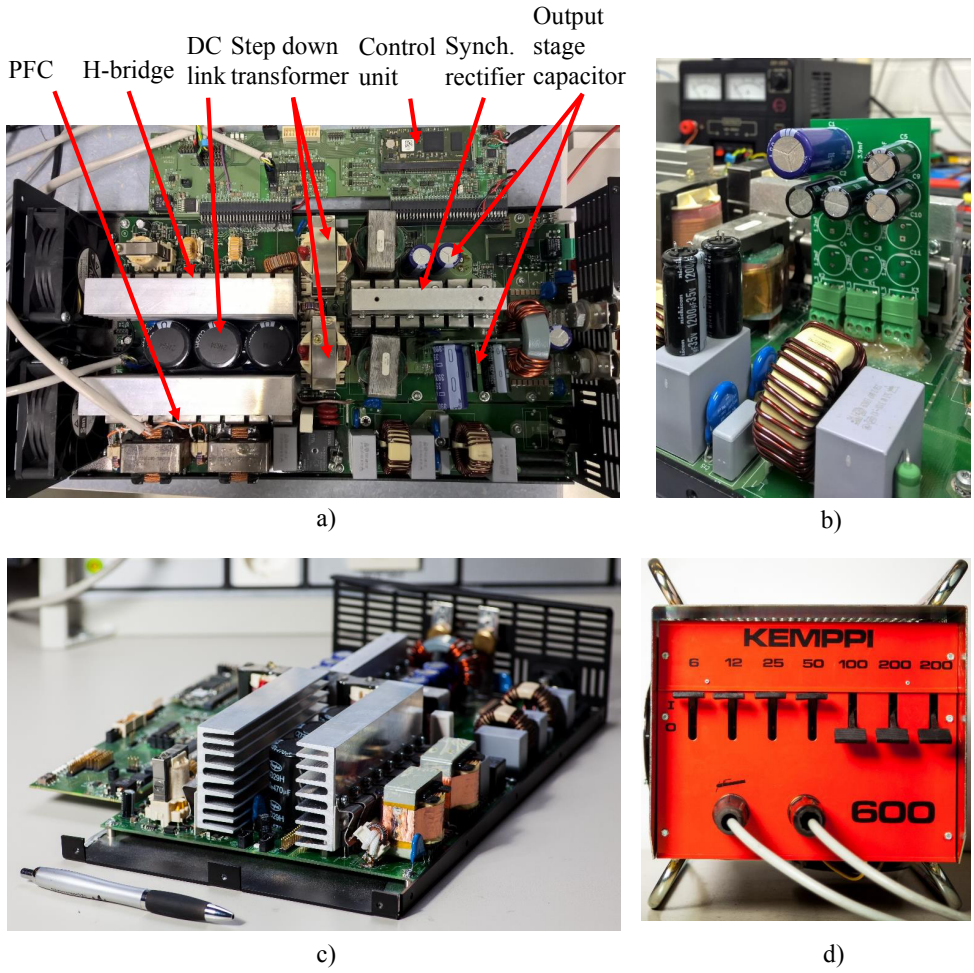

Figure 2.2. AC/DC converter prototype used in the experimental tests. In a), the main functional parts of the converter prototype are illustrated; in b), the experimental capacitor variation board is shown, which is used in the following chapters for emulating the capacitor degradation; c) depicts the converter with a pen for scale, and d) presents the resistor bank, which is used as a converter load in the experimental tests.

within a specified time span. In this work, a 50 kHz control loop frequency is used for all power stage controls, except for the PFC voltage control, which is executed with a 5 kHz frequency. In addition to power stage controls, measurement signal conditioning and data logging are running at the 50 kHz control loop time level. The data logging is capable of saving 4000 samples of six arbitrarily chosen variables.

Figure 2.3 illustrates the flow chart of the control loop execution.

At the start of the control loop, the AD conversion results are copied into variables, which are

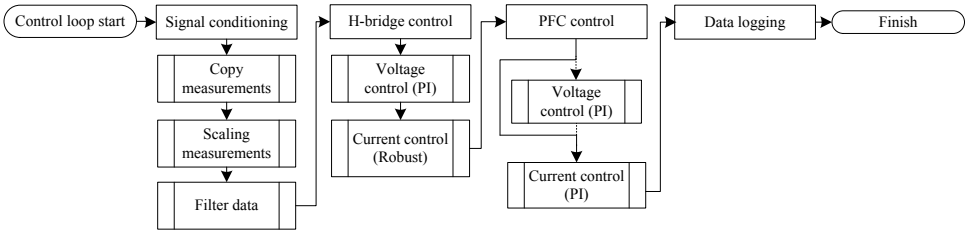

Figure 2.3. Control loop execution procedure. Each main task is shown in a column of its own, including the name of the task at the top and the corresponding functionalities below. First, the measurement signal conditioning is carried out, which is followed by power stage control functions for the H-bridge and the PFC. The PFC voltage control, indicated by a dashed line, is executed with 5 kHz. All other tasks are executed with a 50 kHz frequency. Various signals such as measurements or control states can be logged for analysis purposes. The data logging functionality is executed at the end of the control loop.

only used within the control loop in order to avoid problems with shared resources, as some of the AD conversion results are updated autonomously. Some of the measured signals require filtering such as a moving average or median filter in order to improve the signal-to-noise ratio (SNR) of the signal.

2.2 Experimental tests

The feasibility of the digitally controlled power supply is tested experimentally in dynamic and steady-state operating conditions. The implementation of the control and signal conditioning has been completely upgraded since Publication I, and thus, the overall system performance is now essentially higher. In addition to the control upgrade, the converter control operation is enhanced by the improvement in the signal conditioning and the measurements in the analog domain. Because of the improved SNR, the control bandwidth has been increased, which boosts the dynamic performance of the converter.

The following instrumentation is used for the external measurements in the experimental tests:

- Agilent DSO 6104A oscilloscope
- Tektronix PS5205 differential voltage probe for output voltage measurement
- Tektronix PS5210 differential voltage probe for input voltage measurement
- Agilent Technologies N2781A 150A/10MHz current probes for input and output current measurements

PFC performance is analyzed by measuring the input power factor in a steady state with

various load currents. The power factor is calculated as a product of the input AC current distortion and displacement factors (Erickson and Maksimovic, 2001). The power factor is thus

$$PF = \frac{1}{\sqrt{1+\mathrm{THD}^2}}\cos(\phi_\mathrm{u} - \phi_\mathrm{i}) \tag{2.1}$$

where ϕ_u denotes the voltage phase, ϕ_i the current phase, and THD the AC current total harmonic distortion.

The power factor is determined from 500 000 externally measured samples of grid voltage and current data using 5 MHz sampling. This yields 0.1 s length of data and 10 Hz frequency resolution. The sampled data contain five 50 Hz fundamental cycles. The phases of the grid voltage and current are determined by calculating a Fourier transform from the measured voltage and current signals and defining the phase angle of the 50 Hz frequency component of both signals.

The grid current THD is calculated as a root mean square (RMS) of the harmonic components against the 50 Hz fundamental frequency component. The first 50 fundamental component harmonics are used to define the total harmonic distortion of the input current. Figure 2.4 shows the power factor, which is evaluated with several power levels of the converter, of which the 300 W and 3 kW waveforms are illustrated.

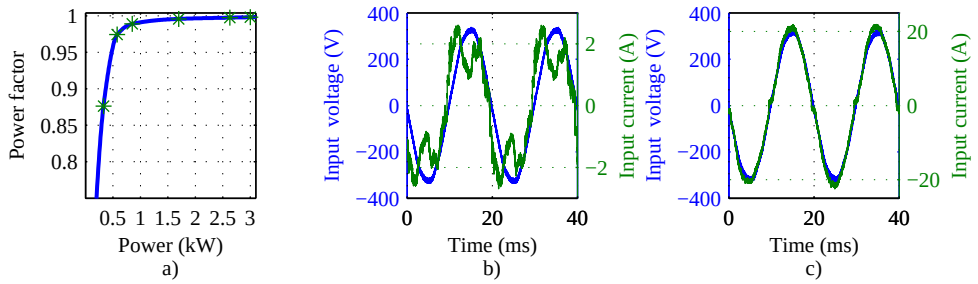

Figure 2.4. PFC operation in a steady state. Subfigure a) illustrates the input power factor as a function of output power. Subfigures b) and c) show the mains current and voltage waveforms with 300 W and 3 kW, respectively. The power factor is close to unity when the power is higher than 20 % of the nominal.

The input power factor against the output power, shown in Figure 2.4a, shows that the power factor is more than 95 % when the power supply is operating above 20 % of the nominal power. The displacement factor with power levels below 20 % of the nominal is affected by an approximately 1.6 A capacitive RMS current, which flows through the EMI filter at the converter input. Therefore, the apparent power is relatively high compared with the real power, and thus, a considerable phase shift between the input voltage and current is seen. When moving towards higher power levels, the effect of reactive power on the power factor is negligible.

The distortion at the input current is also significant with low currents, as seen in Figure 2.4b. The distortion is mainly due to certain drawbacks of the boost converter current measurement such as noise and inaccurate measurement of a current pulse with a low amplitude, which causes nonlinearity and thereby distortion in the input current. When moving towards higher power levels, the most significant effect on the power factor results from the crossover distortion of the input current, which can be seen in Figure 2.4c. The crossover distortion is due to the duty cycle limitation of the PFC power stage to the maximum of 83 % in order to prevent the core saturation of the current transformers, which are used for current measurement.

The dynamic performance of the converter is assessed by applying load steps. The output voltage, DC link voltage, and input current behavior are analyzed during load current transients of 15 A to 100 A and 100 A to 15 A. These load steps are the maximum single steps that can be produced using the load resistors shown in 2.2c. Figure 2.5 illustrates the load step effect on the output voltage, DC link voltage, and input current.

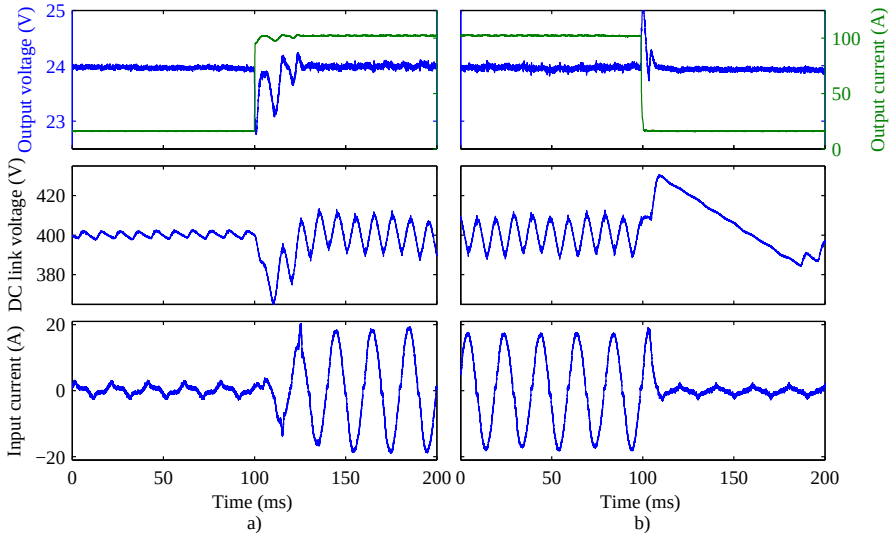

Figure 2.5. Output voltage response to the load step. In a), a load step from 15 A to 100 A, and correspondingly in b), a load step 100 A to 15 A are presented.

The DC link voltage dynamics on the load current steps is defined by the PFC voltage control. The control bandwidth is limited to approximately 5 Hz in order to prevent mains current distortion in the converter steady state. Because the voltage control gain at the 100 Hz frequency significantly affects the power distortion, the 5 Hz control bandwidth was found to be a compromise between the dynamics of the DC link and the input current distortion. The adverse effect of the slow DC link control on the system operation can be seen in the load transients.

During the load step from 15 A to 100 A, shown in Figure 2.5a, the DC link voltage drops. The voltage drop is due to the fact that the PFC voltage control is not fast enough to react to the sudden change in the converter load. Therefore, also the input current amplitude is affected by the delay. Moreover, the effect of the slow voltage control is seen with the load

current step from 100 A to 15 A, shown in Figure 2.5b, where the DC link voltage increases. In this case, the PFC control keeps pushing energy to the DC link after the load step, which is seen as a sudden increase in the DC link voltage. When the DC link voltage exceeds 425 V, the PFC power stage is disabled in order to prevent a hazardous overvoltage at the DC link, yet maintaining the normal output stage operation of the converter. Thus, the DC link voltage settles back to the normal operating range.

The dynamic performance of the output voltage is defined by the control bandwidth of both the H-bridge and the PFC voltage controllers. It can be seen that the 85 A load step causes a 1 V transient to the output voltage in both cases. The nonlinearity, which is seen as an output voltage sag during the load step-up is caused by the DC link voltage drop. The H-bridge is not capable of producing constant 24 V voltage to the converter output as there is not enough voltage in the DC link because of the slow PFC voltage control. The overshoot at the load step-down is due to the insufficient gain of the H-bridge voltage controller, which is limited in order to neglect the effect of the voltage measurement noise on the output voltage in the converter steady-state operation.

2.2.1 Analysis on the required processing resources of the power supply control

The time consumption of the system control loop processing is analyzed by measuring the execution time taken by each control loop task. This test gives information on how much free processing time is available after the control loop processing. It is emphasized that the shown analysis is heavily dependent on the control system implementation and the applied microcontroller. Therefore, the test can only be used as a reference for further execution time consumption analyses reported in this dissertation, and it does not yield precise information on the presented control method requirements in general. The analysis is made for the system in which code optimization for performance is used. Further, an optimization level O2 and code compilation optimization for the execution time are applied (Keil, 2009).

In the analysis, the processing resources required for the following tasks are considered:

- PFC control; consists of the voltage and current PI controller.
- H-bridge control; consists of the PI voltage controller and the 4th-order optimal robust current controller.
- Measurement scaling; consists of multiplications of the AD-converted results with the AD conversion resolution.
- Filtering and data processing; consists of two moving average filters and one median filter. Each of these is five samples long.

Figure 2.6 presents the processing requirements of the above tasks.

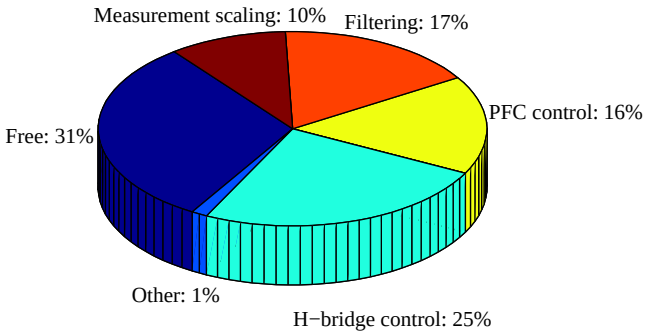

Figure 2.6. Worst-case execution time requirement of different tasks in the power stage control loop.

The execution time required for each task in the control loop may vary because of the uncertainty of the measurement method. Sources for uncertainty are an unequal sample rate of the timer clock compared with the MCU master clock, variations in control loop execution times as a result of a lower execution rate of some control loops (e.g. PFC voltage control), and the conditional execution within the control loop. Therefore, the worst-case scenario, that is, the peak consumption of processing resources observed in the measurements is used as a result of the analysis.

The H-bridge control is the major processing time consumer in the control loop. This is explained by the use of a robust control system for the H-bridge current control. The robust controller contains more executable code and arithmetical operations compared with a PI control structure used in other controllers. Further, the robust control is of a higher order (4th order) than the other control loops (1st order).

The second major contributor of the power stage control loop is the PFC control. The lower time consumption compared with the H-bridge control is due to the fact that the voltage and current controllers are both implemented using a 1st-order PI structure, which requires less processing resources than the current controller used in the H-bridge.

According to the results, the measurement signal conditioning is the third heaviest task running in the control loop. The measurement data are filtered to improve the signal-to-noise ratio (SNR). In order to remove impulse noise caused by EMI from the measured output voltage signal, a median filter is used. Wide-bandwidth measurement noise is filtered from the input and DC link voltage using moving average filters.

In order to avoid AD-converted signal corruption resulting from the shared data problem, the AD conversion results used for the system control are copied into control loop specific variables while the updating of AD conversion results is disabled. In addition to the measurement data copying, the measured values are scaled with a corresponding measurement gain

to represent the correct values, as it was shown in Figure 2.3. This procedure accounts for the fourth-largest proportion of resources used in the control loop.

The rest of the required resources are consumed by conditional execution such as the safety trip functionality, which halts the converter operation if the measured value exceeds the maximum allowed limit.

The control loop time level with the presented control system uses approximately 69 % of the maximum applicable processing time. Therefore, it can be deemed that the hard real time requirement for the system control is met with the proposed system running at the 50 kHz control loop frequency. The rest 31 % of the processing resources are thus available for other tasks. It should be noted that the lower-priority tasks such as the user interface communication do not need time critical execution, and consequently, they do not share the execution time directly with the control loop. This means that they can run when the microcontroller is not executing any higher-priority task.

2.3 Discussion

An embedded system control for a power supply has been studied considering power converter operation and the feasibility of a centralized controller system. The discussion focuses on the system operation and the suitability of the chosen control platform for the power supply control under study.

The use of an embedded control system has several advantages over an analog control system, especially when the system control is carried out using a single embedded controller platform. Comprehensive information on the system state enables the use of a supporting functionality for the power supply. Applications such as condition monitoring, fault detection, and prognosis of the remaining useful lifetime of a power conversion unit are examples of auxiliary processes that can be implemented to run along with the converter control. A downside of the digital control system is that the requirement of hard real-time operation of the control loop must be met in all situations in order to ensure the proper operation of the converter.

The experimental results show that the proposed digital control approach combining the MCU with the FPGA is a feasible solution for power supply control as the required power supply functionalities are achieved. It has been shown that the control is capable of producing output voltage with less than 100 mV voltage ripple in the steady state. Further, the embedded control approach has been demonstrated to have an ability to control multiple power stages, which is beneficial from the perspective of system integration. On the other hand, the results also reveal the shortcoming of control operation; in load transients, the converter control is not able to provide 1 V voltage regulation reliably throughout the power scale of the converter. This is due to the limited bandwidth of the output voltage control loop.

The execution of the control loop requires approximately 69% of the available resources when

the 50 kHz control loop frequency is used. This is considered a relatively high consumption of the processing power in contrast to the overall performance of the MCU as the applied control does not require highly complex algorithms in terms of processing power. Therefore, the high consumption of processing resources cannot only be explained by the control or signal processing. For example, the H-bridge control loop (voltage and current control) execution uses a maximum of 200 assembly commands when the disassembly of the compiled code is analyzed. The maximum execution time for one assembler command is three clock cycles of the 168 MHz master clock as no divisions, square roots, or over 32-bit precision for variables are used (ARM Ltd., 2009). Even when considering the extreme worst-case approximation, in which each command takes three clock cycles, the maximum usage of the H-bridge control loop should not account for more than 17 % of the control loop execution time. This indicates that the context switch such as a function call with the applied controller is a relatively expensive operation from the viewpoint of execution time.

It is seen that the execution of both power stage control sequences, PFC and H-bridge together, take 41% of the available execution resources. Both of these control structures include cascaded voltage and current control loops, which are all executed individually. As both the current and voltage control in the PFC control loop are implemented using only the most simple PI structure, 16% of the execution resources can be considered the minimum for the execution of one power stage control sequence with the chosen microcontroller. In the H-bridge case, the chosen robust control algorithm increases the requirement by 9 percentage points. Therefore, even with the simplest, fully digital control structure, 32% of the reserved processing resources are required purely for controlling the power stages in the presented power supply. This value with this specific digital controller could be cut down only by optimizing the code by directly writing the control functions with assembler, or replacing some of the power stage controls with an analog control.

It is mentioned in the conclusions of Publication I that signal conditioning is one of the key issues calling for special attention when a power supply system is designed. The measurement circuitry in a noisy environment such as a power supply is highly prone to EMI. The noise induced in the measurement signal reduces the measurement SNR, which, again, has a direct effect on the design of the power stage control system and the obtainable system dynamic performance. In the converter system under study, the EMI heavily affects the converter input, DC link, and output voltage measurements. The EMI issues are mitigated by digital filtering. As shown in Figure 2.6, the filtering consumes approximately 17 % of the processing resources available for the control loop. In contrast to this result, reducing the EMI issues in the analog domain is highly beneficial from the viewpoint of the processing resources of the digital control and embedded systems.

The choice of a centralized control unit for the converter in question is a feasible but not ideal solution for the control application under study. The applied MCU has several benefits such as versatile peripherals in the communications and the analog-to-digital converter (ADC). On the other hand, the chosen MCU is lacking in PWM peripherals, which makes the use of an external circuit for PWM mandatory. In this case, modulation was implemented on the FPGA, which, in general, provides flexibility in the system, but increases the programming effort and system complexity. Therefore, it is obvious that this method is slower to develop

than the single MCU method, which has the peripherals required for the digital power supply control. The chosen platform gives a lot of freedom for the development of the power supply control, but it is not a cost-optimized solution. The modern state-of-art microcontrollers are equipped with the required peripherals so that they can be used to control a similar power supply with a fraction of the price of the control unit chosen for this prototype application.

Chapter 3

State-Observer-Based Condition Monitoring in a DC/DC Converter

In digitally controlled power supplies, the free processing resources can be exploited to monitor system health and condition. A viable approach to monitor an appliance health and to determine potential faults is to use a state observer to compare the system operation against a reference model. In power converter applications, for instance, the system states can be reconstructed by applying a system model, and then compared with measurements of the corresponding signals (Isermann, 2011).

In model-based condition monitoring, the design parameters of the converter define the reference model and thereby the reference operation for the converter. In an ideal case, the converter model produces output signals, which are equal to the measurements. Therefore, the difference between the measured and modeled parameters can be assumed to indicate a system fault or altered system parameters, which, again, may be signs of component aging (Isermann, 2011).

In practice, the converter model output does not completely correspond to the measured signals because of modeling uncertainties such as component tolerances, environmental effects, nonlinearity, and a reduced-order model. These effects can be seen as unequal dynamics and a steady-state error at the model output with respect to measurements. The error between the model outputs and the measured values of the converter can be compensated for by using a state observer, which produces a correction factor, residual, defined by the error between the modeled and measured values. The other way around, the residual equals the need for adaptation in order to match the model output with the measurements.

When the DC/DC converter part of the AC/DC system shown in Chapter 2 is considered, an averaged state space DC/DC converter model with a state observer is used for condition monitoring. Precursors to system aging can be detected when evaluating the state observer

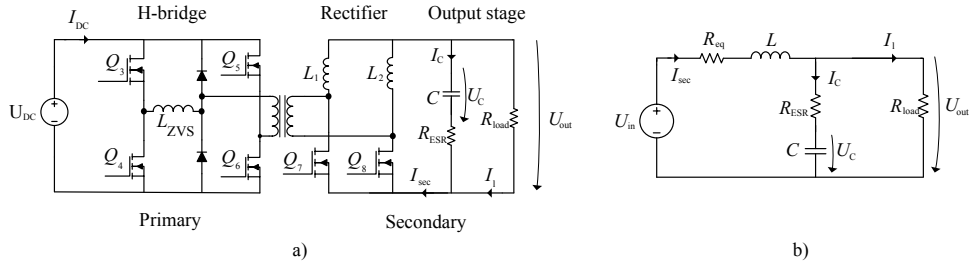

Figure 3.1. DC/DC converter main circuit in subfigure a) and the corresponding equivalent circuit in b).

residual operation with respect to changes in the system hardware.

This chapter is a continuation of the study presented in Publication II. The state observer design aspects such as the stability analysis are in the focus of attention, and the experimental tests are revised. The method operation both with an AC and a DC power input is assessed to determine the method sensitivity against DC link voltage ripple. In the study, the aging phenomena of the converter DC/DC circuit such as a decrease in the output stage capacitance and an increase in losses in the main circuit are examined with experimental tests. The revised tests are carried out in the converter steady-state operation, as in Publication II. In addition, the applicability of the method to detect changes in converter dynamics is assessed by load transient tests. Further, the effects of the model on the free processing resources of the embedded system are evaluated.

3.1 Equivalent model for a phase-shifted DC/DC converter

The model-based condition monitoring is implemented to detect the degradation of components in the secondary circuit of the converter presented in Chapter 2. The condition monitoring functionality is achieved by monitoring changes in the converter secondary-side current ($I_{\mathrm{sec}}(t)$) and the capacitor voltage ($U_{\mathrm{C}}(t)$), for which a model of the DC/DC converter is derived. The model incorporates an equivalent circuit representation of the primary-side DC link, the phase-shifted ZVS H-bridge, the step-down transformer operation, the secondary-side synchronous rectifier with the current doubler circuitry, and the output stage. The main circuit of the DC/DC converter and the corresponding equivalent model are shown in Figure 3.1. The converter model is derived adopting an approach exhaustively discussed in (Cao, 2007). In the present study, only minor modifications have been made to the model shown in (Cao, 2007) such as taking into account the rectification losses in the DC/DC converter secondary.

The converter behavior is presented using a first-order system model, which averages the converter operation over one switching period. The model uses parameters of the main circuit components such as the secondary inductance (L), the secondary-side capacitor (C), the capacitor equivalent series resistance (R_{ESR}), the series resistance (R_{eq}), and the resistive load

(R_{load}). In addition, the system is affected by the duty cycle (d), the DC link voltage (U_{DC}), and the transformer turns ratio (n), which together define the equivalent model input voltage (U_{in}). In the representation, the parameters U_{DC} and thereby U_{in}, and the capacitor current (i_{C}) and voltage (U_{C}) are time dependent. For the sake of clarity, the time dependency is not incorporated in the model. The first time derivative is denoted by a dot; for instance, the first time derivative for the secondary current is written as $\dot{I}_{\text{sec}}$.

It has been shown in (Cao, 2007) that the current doubler circuit provides a parallel connection of the inductors when the system is averaged over one switching period. The secondary inductance is thus expressed as

$$L = \frac{L_1 L_2}{L_1 + L_2}. \tag{3.1}$$

U_{in} corresponds to the equivalent circuit input voltage, which is defined by

$$U_{\text{in}} = \frac{U_{\text{DC}} d}{n}. \tag{3.2}$$

From the equivalent circuit point of view, the input voltage and the secondary current (I_{sec}) can be expressed as

$$U_{\text{in}} = R_{\text{eq}} I_{\text{sec}} + L\dot{I}_{\text{sec}} + U_{\text{out}} \tag{3.3}$$
$$I_{\text{sec}} = i_{\text{C}} + I_{\text{load}} \tag{3.4}$$

where $\dot{I}_{\text{sec}}$ is the first time derivative of the secondary current. By representing (3.3) applying (3.2) and writing (3.4) by using C, U_{out}, and R_{load}, the voltage and current equations are obtained

$$\frac{dU_{\text{DC}}}{n} = R_{\text{eq}} I_{\text{sec}} + L\dot{I}_{\text{sec}} + U_{\text{out}} \tag{3.5}$$
$$I_{\text{sec}} = C\dot{U}_{\text{C}} + \frac{U_{\text{out}}}{R_{\text{load}}}. \tag{3.6}$$

where $\dot{U}_{\text{C}}$ corresponds to the first time derivative of the capacitor voltage. U_{out} can also be expressed using I_{sec} and U_{C}

$$U_{\text{out}} = I_{\text{sec}} \frac{R_{\text{load}} R_{\text{ESR}}}{R_{\text{load}} + R_{\text{ESR}}} + U_{\text{C}} \frac{R_{\text{load}}}{R_{\text{load}} + R_{\text{ESR}}}. \tag{3.7}$$

By writing (3.7) using (3.5) and (3.6), the voltage and current equations can be expressed as

$$I_{\text{sec}} \frac{R_{\text{load}}}{R_{\text{load}} + R_{\text{ESR}}} = C\dot{U}_{\text{C}} + \frac{U_{\text{C}}}{R_{\text{load}} + R_{\text{ESR}}} \tag{3.8}$$

$$\frac{dU_{\text{DC}}}{n} = (R_{\text{eq}} + \frac{R_{\text{load}} R_{\text{ESR}}}{R_{\text{load}} + R_{\text{ESR}}}) I_{\text{sec}} + L\dot{I}_{\text{sec}} + U_{\text{C}} \frac{R_{\text{load}}}{R_{\text{load}} + R_{\text{ESR}}}. \tag{3.9}$$

When I_{sec} and U_{C} are chosen for state variables and d is the controlled system input variable, a state space representation of the converter can be written

$$\begin{aligned} \overbrace{\begin{bmatrix} \dot{I}_{\text{sec}} \\ \dot{U}_{\text{C}} \end{bmatrix}}^{\dot{\boldsymbol{x}}} &= \overbrace{\begin{bmatrix} -\frac{R_{\text{a}}}{L} & -\frac{R_{\text{load}}}{LR_{\text{b}}} \\ \frac{R_{\text{load}}}{CR_{\text{b}}} & -\frac{1}{CR_{\text{b}}} \end{bmatrix}}^{\boldsymbol{A}} \overbrace{\begin{bmatrix} I_{\text{sec}} \\ U_{\text{C}} \end{bmatrix}}^{\boldsymbol{x}} + \overbrace{\begin{bmatrix} \frac{U_{\text{DC}}}{Ln} \\ 0 \end{bmatrix}}^{\boldsymbol{B}} \overbrace{d}^{\boldsymbol{u}} \\ \overbrace{\begin{bmatrix} y_1 \\ y_2 \end{bmatrix}}^{\boldsymbol{y}} &= \overbrace{\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}}^{\boldsymbol{C}} \overbrace{\begin{bmatrix} I_{\text{sec}} \\ U_{\text{C}} \end{bmatrix}}^{\boldsymbol{x}} \end{aligned} \tag{3.10}$$

where

$$R_{\text{a}} = R_{\text{eq}} + \frac{R_{\text{load}} R_{\text{ESR}}}{R_{\text{load}} + R_{\text{ESR}}} \tag{3.11}$$

and

$$R_{\text{b}} = R_{\text{load}} + R_{\text{ESR}}. \tag{3.12}$$

3.1.1 Effect of the duty cycle loss on the averaged model

The converter is exposed to a duty cycle loss because of the primary-side inductance, which consists of the leakage inductance of the transformer and the additional series inductance with the transformer. The additional series inductance is used to extend the primary-side current range in order to achieve the ZVS. The amount of pulse width reduction is dependent on the ZVS inductance and the converter load current, and thus, the throughput power. Figure 3.2 depicts a simulated representation of the relation between the DC link current and the duty cycle loss seen in the transformer secondary with respect to variation in the primary-side ZVS inductance and the load current.

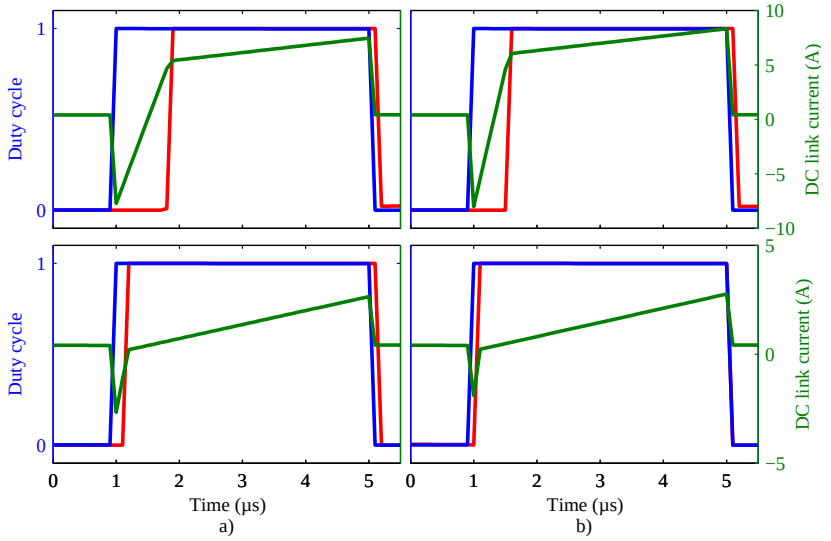

Figure 3.2. Duty loss phenomenon caused by the primary ZVS inductance. In the figure, the primary duty cycle pulse is indicated by blue, the secondary duty cycle by red, and the DC link current by green. In subfigure a), the converter operation is presented with 15 µH L_{zvs} and in b) with 5 µH L_{zvs}. In the upper figures the converter load current is 100 A, and 25 A in the lower figures. It can be seen that both the load current and L_{zvs} have an effect on the duty cycle loss seen in the transformer secondary.

Figure 3.2 shows that the pulse width seen in the secondary is reduced with respect to the load current and the primary-side inductance. The loss of the duty cycle is caused by the time required to change the direction of the primary current, as the ZVS inductance is resisting the change in the primary current (Hua et al., 1991). It has been noted in (Cao, 2007; Tsai, 1993) that the duty cycle loss can be approximated by

$$d_{\mathrm{loss}} = \frac{(L_{\mathrm{k}} + L_{\mathrm{zvs}}) I_{\mathrm{load}} f_{\mathrm{t}}}{n U_{\mathrm{DC}}}, \tag{3.13}$$

where L_{k} denotes the transformer leakage, L_{zvs} is the primary ZVS inductance, and f_{t} is the switching frequency. A more in-depth analysis of the duty cycle loss in an isolated DC/DC converter is given in (Sun et al., 2014)

As the averaged model expresses the converter operation integrated over one switching period, the dynamics of L_{ZVS} in terms of reactive component is negligible in the model. The pulse width loss has an effect on the averaged model in terms of loss of volt seconds, which, again, is seen in the secondary side as reduced power. As the pulse width loss is thus current dependent, it is modeled in the secondary circuit as a series resistance (Cao, 2007)

$$R_{\mathrm{loss}} = \frac{2(L_{\mathrm{k}} + L_{\mathrm{zvs}}) f_{\mathrm{sw}}}{n^2}. \tag{3.14}$$

In order to keep the R_{loss} model simple, the switching losses are assumed negligible in contrast to conduction losses, as the converter is operating in ZVS conditions above 15 % of the nominal current. It is therefore expected that the switching losses will introduce uncertainty into the model at low loads, where the ZVS conditions are not met. By expressing the semiconductor on-state resistance by R_{sc}, the equivalent series resistance in the equivalent converter circuit is written as

$$R_{\text{eq}} = R_{\text{loss}} + R_{\text{sc}}. \tag{3.15}$$

3.1.2 State observer

The state observer is defined for a state space model by

$$\begin{aligned} \hat{\boldsymbol{x}} &= \boldsymbol{A}\hat{\boldsymbol{x}} + \boldsymbol{B}\boldsymbol{u} + \boldsymbol{L}(\boldsymbol{y} - \hat{\boldsymbol{y}}) \\ \hat{\boldsymbol{y}} &= \boldsymbol{C}\hat{\boldsymbol{x}} \end{aligned} \tag{3.16}$$

where $\hat{\boldsymbol{x}}$ denote the state variables estimated with the observer, $(\boldsymbol{y} - \hat{\boldsymbol{y}})$ is the error between the observer output $\hat{\boldsymbol{y}}$ and the measured value $\boldsymbol{y}$ at the converter, and $\boldsymbol{L}$ is the observer gains. Figure 3.3 shows the state observer as block diagrams, which demonstrate how the state estimation is related to the converter (plant) operation, and how the residuals ($\boldsymbol{r}$) are formed.

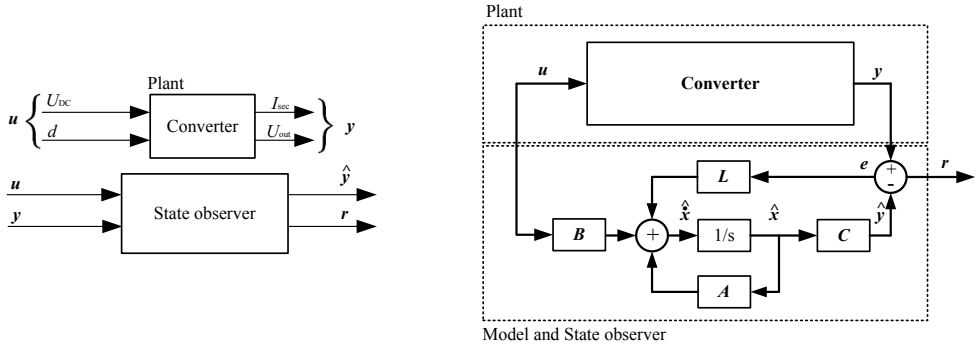

Figure 3.3. Block diagram of the state observer. In subfigure a), the relation of the converter input and the measurement signal to the state observer signals is shown. Subfigure b) illustrates a block diagram of the state observer and the generation of the residual $\boldsymbol{r}$. Subfigure b) is reproduced from (Isermann, 2011).

The designed observer system works alongside the converter control loop operation, but the observer states are not used for converter control. Thus, the observer has no effect on the

converter operation. As shown in Figure 3.3b, the state observer produces an estimate of the plant measurements according to the system matrix $\boldsymbol{A}$ and the input $\boldsymbol{Bu}$. The error $\boldsymbol{e}$ is equal to the residuals used for condition monitoring in this study.

The state observer uses a gain coefficient matrix $\boldsymbol{L}$ in the error feedback loop, which defines the compensation dynamics for the observer. The coefficient matrix can be chosen arbitrarily, when the stability criteria are met. The observer system is stable when the roots of the characteristic equation have a negative real part. In the (3.16) case, the characteristic equation roots are the system eigenvalues. The system is thus stable when

$$\det(\lambda \boldsymbol{I} - (\boldsymbol{A}\text{-}\boldsymbol{LC})), \mathrm{Re}(\lambda) < 0. \tag{3.17}$$

In a matrix representation, this can be written as

$$\left| \begin{bmatrix} \lambda & 0 \\ 0 & \lambda \end{bmatrix} - \left(\begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} - \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} \right) \right| < 0. \tag{3.18}$$

The Routh-Hurwitz stability criterion (Hurwitz, 1895; Goodwin et al., 2001) states that the characteristic equation roots are negative in a second-order system of the form

$$a\lambda^2 + b\lambda + c \tag{3.19}$$

when a,b,$c > 0$. By converting (3.18) into a second-order representation and separating the λ coefficients, the observer system is stable when

$$\begin{aligned} a &: 1 > 0 \\ b &: L_{11} - A_{11} + L_{22} - A_{22} > 0 \\ c &: L_{12}A_{21} - L_{11}A_{22} + L_{21}A_{12} - L_{22}A_{11} + \\ &\quad A_{11}A_{22} - A_{12}A_{21} + L_{11}L_{22} - L_{12}L_{21} > 0. \end{aligned} \tag{3.20}$$

As it can be seen, there is no unique solution for the $\boldsymbol{L}$ values in order to obtain a stable system, as there are two degrees of freedom considering solutions for (3.20)b and (3.20)c, when it is assumed that the system is observable.

In practical observer designs, the feedback gain $\boldsymbol{L}$ is often defined by iterative methods to achieve satisfactory performance of the observer. The observer performance is defined by its capability to follow the converter dynamics but to neglect the measurement noise. Therefore, in the experimental system case of this study, the required gain matrix for proper observer operation is obtained by a trial and error method by comparing the measured value from the converter with the observer output. The observer gains used in the study are

Table 3.1. Parameters of the DC-DC converter used in the modeling.

Parameter	Symbol	Value	Unit
DC link voltage	U_{DC}	400	V
Switching frequency	f_{sw}	60	kHz
Control loop frequency	f_{ctrl}	50	kHz
Model sample time	t_{s}	20	µs
Nominal output voltage	U_{out}	24	V
Maximum output current	I_{max}	100	A
Transformer turns ratio	n	9.68	-
Secondary equivalent inductance	L	15	µH
ZVS inductance	L_{zvs}	13	µH
Primary leakage inductance	L_{k}	2.55	µH
Nominal output capacitance, total	C	27.6	mF
Nominal output capacitor ESR, total	R_{ESR}	7.8	mΩ
Secondary MOSFET on-state resistance, total	R_{sc}	1.0	mΩ

$$\boldsymbol{L} = \begin{bmatrix} 43518 & -66303 \\ 41.964 & 24825 \end{bmatrix}. \tag{3.21}$$

When the stability is analyzed with the system matrix $\boldsymbol{A}$ composed of the parameters shown in Table 3.1, the state observer can be shown to be stable within the complete load current range used in the study.

3.2 Experimental verification of the model-based condition monitoring method

The applicability of the model-based condition monitoring system to detect abnormal system behavior is studied by tracking variations in the residual behavior of the state observer. The residual values are first defined with a system in pristine condition for reference. Then, external modifications are made to the output stage capacitance and the synchronous rectifier to produce variation in the converter operation. Thus, conclusions can be made on the capability of the method to detect either an increase in losses, resulting from a malfunction of the synchronous rectifier, or deviating converter dynamics caused by a decreased capacitance at the output stage.

In Publication II, the method was evaluated with different input parameters than the ones used in this study, and therefore, all the experimental results shown here are revised. In Publication II, only the losses caused by the disabling of the synchronous rectification were assessed experimentally. It was shown by simulations that the method is not capable of detecting a reduction in capacitance in the steady-state operation.

To continue the work conducted in Publication II, in the present study, the decrease in capacitance and the increased losses in the secondary are studied experimentally in the converter steady-state operation and in a load transient. The steady-state operation is investigated using 15 A, 25 A, 50 A, 75 A, and 100 A load currents. In the transient tests, the output current is stepped up from 15 A to 60 A. The step size of 45 A was used to avoid nonlinearity in the output voltage caused by an insufficient DC link voltage at the load step, as presented in Figure 2.5a in Chapter 2.

The study is carried out by applying the converter first with a DC power input and then with an AC input to determine the effect of sinusoidal voltage ripple in the DC/DC converter on the feasibility of the method. In the tests, the capacitance is varied from 23.7 mF to 16.5 mF. More losses are generated when the secondary-side rectification is performed using the parasitic diodes of the MOSFETS. As the diode has a constant forward voltage of 0.7 V, the losses in the secondary may vary between 15 and 70 W depending on the load current.

The converter model and the observer, presented in (3.10) and (3.16), are implemented to run at the control system time level alongside the system control functions. The time domain model (3.16) is discretized using a forward Euler method by

$$\hat{\boldsymbol{x}}[k] = (\boldsymbol{I} + \boldsymbol{A}t_\mathrm{s})\boldsymbol{x}[k-1] + t_\mathrm{s}\boldsymbol{B}\boldsymbol{u}[k-1] + t_\mathrm{s}\boldsymbol{L}(\boldsymbol{y} - \hat{\boldsymbol{y}})[k-1], \tag{3.22}$$

where t_s is the sample time, and k denotes the sample instant of the corresponding signal. In the real-time model execution, the load resistance R_load is calculated according to the measured load current and output voltage. Therefore, the $\boldsymbol{A}$-matrix varies according to the load current. The model state variables U_C and I_sec are not directly measured at the converter. The capacitor voltage is expected to be identical to the output voltage as the effect of the voltage loss caused by the capacitor ESR is negligible compared with the output voltage.

The secondary current, on the other hand, has to be estimated through the DC link current measured at the converter primary. The secondary current has the same dynamics as the DC link current, and thus, I_sec is obtained by using a scaled DC link current. The relation between the DC link current and the secondary current is nonlinear especially at low currents because of the measurement circuit and the measurement technique applied. The DC link current is measured synchronously at the peak of the DC link current waveform.

The scaling function for I_sec is obtained by measuring the DC link and the output current in the steady-state operation. The DC link current is measured by using the internal AD converter of the microcontroller, and the output current by an oscilloscope. In the steady state, the output current and the secondary current have a matching DC value. Thus, by defining the relation between the DC link current measurement and the known load current in the steady state, the scaling function from the DC link current to the secondary current is obtained. In order to avoid excessive disturbance in the measurement, the DC power input is used to determine the scaling function. Figure 3.4 presents I_sec graphically as a function of the AD-converted DC link current measurement scaled between [0,1].

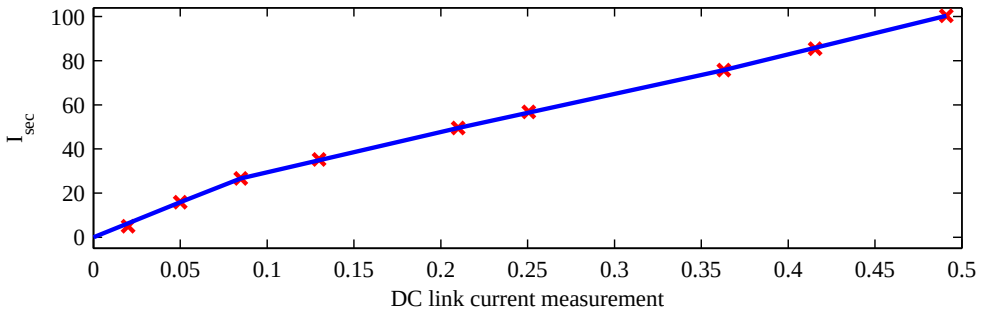

Figure 3.4. Experimentally defined scaling function for I_{sec}. The function is nonlinear when the converter is operating at an I_{sec} below 25 A.

3.2.1 Results of the capacitor variation tests

The capability of the method to detect the capacitor degradation is assessed by experimental tests. The MIL-C-62 standard specifies that electrolytic capacitors with an operating voltage lower than 100 V have met their end of life condition with a 20% decrease in capacitance compared with their value in pristine condition. To evaluate the capability of the detection method to distinguish a healthy capacitor from a faulty one, 30 % variation in capacitance is used in the study.

The steady-state tests are carried out by first defining the initial behavior of the observer residual. This is done by saving the residual values of a converter in pristine condition with each load current mentioned above. The purpose of this is to define how the residual value behaves only with respect to a varying output current in a healthy converter. The steady-state operation analysis uses the absolute average value of 4000 sequentially measured residuals at the control loop time level as a reference. Thus, the residual used in the analysis can be written as

$$\boldsymbol{r}(I_{\text{load}}) = \left| \frac{1}{4000} \sum_{k=1}^{4000} \boldsymbol{L}(\boldsymbol{y} - \hat{\boldsymbol{y}})[k] \right|. \tag{3.23}$$

After defining the reference, the capacitance at the converter output stage is reduced by changing the number of parallel capacitors. The observer residual values are saved again with the corresponding load currents that were used to define the reference operation. Figure 3.5 shows the state observer residuals with respect to load current in the converter steady-state operation. In the figure, the residual behavior is illustrated with respect to load current using DC and AC power inputs with 23.7 mF and 16.5 mF output stage capacitors.

Transient tests for the variation of the observer residual value are performed to determine the

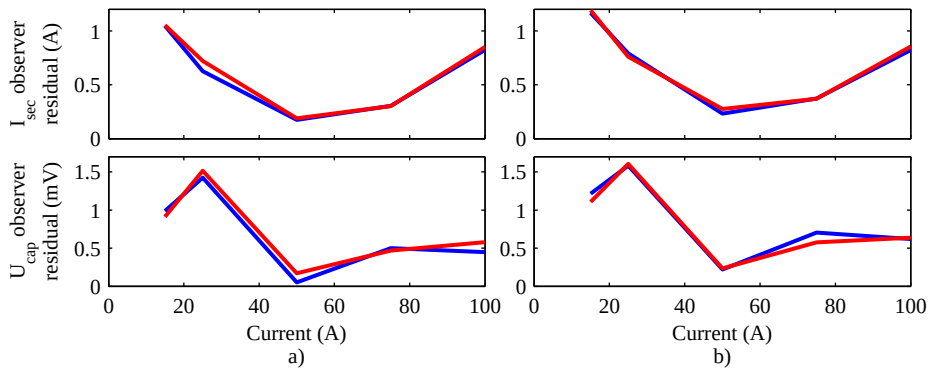

Figure 3.5. Observer residual variation with respect to load current. In subfigure a), the secondary current and capacitor voltage residuals are shown using a DC power input and in b) by using an AC power input. In all figures it can be seen that when the degraded capacitor operation (red) is compared with the pristine condition operation (blue), no significant variation can be detected.

changes in the residuals at a load transient. As the converter is normally used with a constant output voltage, the transient situation is achieved by applying a load step at the converter output. During the load transient, the residual values of both I_{sec} and U_{C} are analyzed. Figure 3.6 depicts the load transient from 15 A to 60 A and the corresponding effect on the observer residual values both in pristine condition and the degraded capacitor case.

The results presented in Figures 3.5 and 3.6 show that the decreased capacitance only affects the residual transient behavior in all the studied cases. According to the results obtained with the capacitor tests, the decrease in the capacitance causes only a 0.0015 V variation in the residual value. When the steady-state results are considered, there is practically no difference in the residuals in either the DC or AC power input cases.

In the load transient tests, there is a small variation in residuals during the transients. When the results measured with the AC and DC power inputs are compared, it can be seen that the DC link ripple has a very negligible effect on the method behavior. It can be concluded that the altering output dynamics resulting from a lower capacitance can be seen in the load transient, yet the difference is not significant. Therefore, numerous load transients would be required to reliably define the changed dynamic conditions at the output voltage. It is also worth mentioning that a reactive load has an effect on the output stage dynamics, and therefore, the load structure has to be known in order to obtain reliable information on the output stage capacitor condition with the presented method.

3.2.2 Results of the tests on variation in the secondary stage losses

In Publication II, also the feasibility of the state observer method to detect increased losses in the system was studied. Losses in the system are for example caused by degradation or a fault

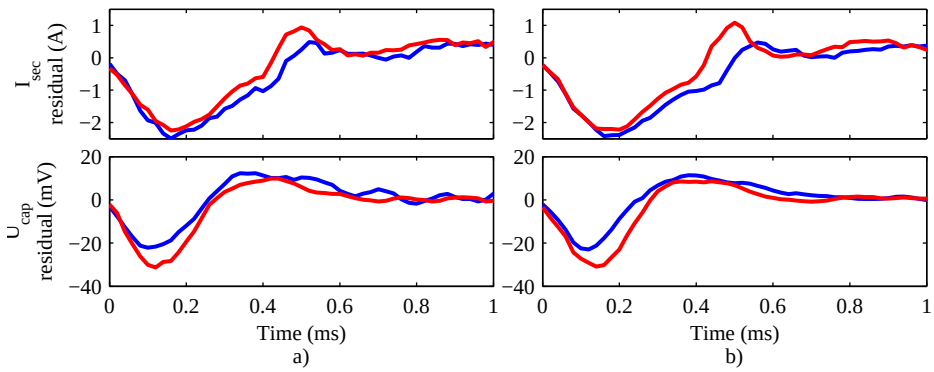

Figure 3.6. Residual behavior in the nominal (blue line) and decreased capacitance tests (red line) using a load current transient from 15 A to 60 A. Subfigure a) shows the residual behavior with a DC and b) with an AC power input. Small variations in residuals can be seen only during the transient.

of switching semiconductors or their driver circuits in the secondary. In order to emulate the output stage switching fault, the secondary-side synchronous rectifier is disabled to generate more losses.

Here, the test methods are the same as in the capacitor degradation case: 4000 samples at each operating current are measured in the steady-state tests, and 45 A load current steps are used in the transient tests. Figure 3.7 shows the steady-state measurement results of the test with increased losses at the converter secondary-side rectifier stage.

The steady-state results show that the residuals involve a deviation when the pristine-condition converter is compared with a converter with elevated losses. Considering the obtained results, the voltage residual deviates from the results presented in Publication II. In the presented results, the capacitor voltage deviation is on the scale of a few millivolts, which is negligible compared with the measurement resolution (0.0078 V/bit) of the output voltage. Therefore, the results cannot be considered feasible for condition monitoring purposes.

Figure 3.8 shows the effect of a load step on the state observer residual when the secondary-side losses increase. The results show that the offset at the converter residual is evident in the I_{sec} case, which was also detected in the steady-state tests. When the healthy and faulty cases are compared, it can be seen that the increased losses do not cause any significant variations to the residual dynamics.

3.2.3 Analysis of the execution time requirements

The execution time requirement of the state observer method considering the applied MCU is related to the amount of free resources, which was analyzed in Section 2.2.1. Figure 3.9 presents a chart where the effect of the condition monitoring method applying a state observer

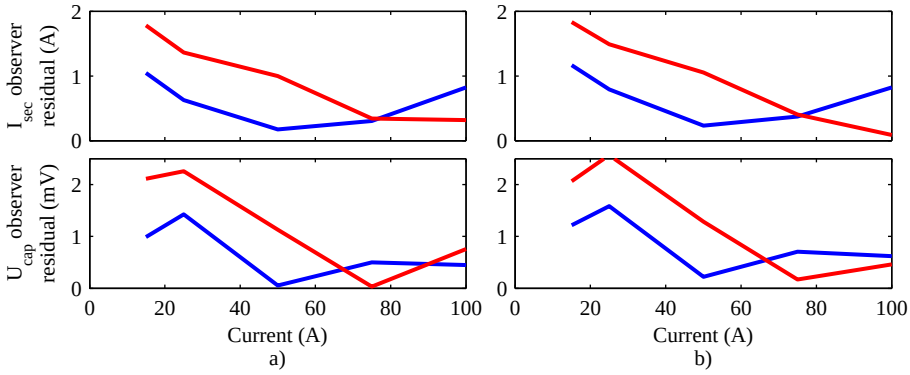

Figure 3.7. Relative change in the state observer residual with respect to load current. The normal behavior of the observer residual is indicated by blue and the case of increased losses by red. In subfigure a), the secondary current and capacitor voltage residuals are shown using a DC power input and in b) by using an AC power input. The increased losses introduce a considerable deviation into the residual value especially in less than 75 A load current operation.

is evaluated with respect to the free resources available at the control loop time level.

As shown in Figure 3.9, the execution of the state observer method requires 7 % of the available processing resources from the microcontroller. The chart only shows the effect of the model and observer execution on the control loop execution.

To be able to apply the detection procedure to online evaluation of converter aging, the behavior of the residuals has to be analyzed throughout the converter lifetime. This requires capacity to save and process the measurement data. On the other hand, the aging analysis and residual data processing do not require time-critical execution, and consequently, they can be performed outside the control loop time level. Therefore, the data analysis is not considered to have an effect on the control loop operation and thus, it is omitted from the analysis of the execution time requirement.

3.3 Discussion

It has been shown that the increased losses in the system produce a detectable change in the residual behavior. The study applied a worst-case scenario with the secondary stage, because all the secondary-stage switches were disabled at once in order to increase losses in the system. In normal operation with this converter secondary power stage topology, it should be noted that if the switching component is completely malfunctioning and there is no current path through the body diode, it is not possible to detect a component malfunction with this method. In the converter case, the method can be considered feasible because the output stage consists of several parallel switching components. Owing to the redundancy, a complete

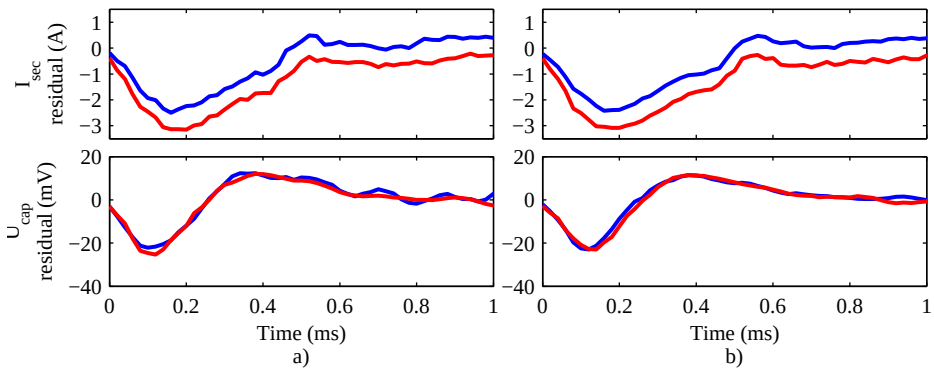

Figure 3.8. Residual behavior in the cases of normal (blue line) and increased losses (red line) in a 55 A load transient. Subfigure a) shows the residual behavior with a DC input and b) with an AC power input. Variations in residuals can be seen only during the transient.

malfunction of one switch does not compromise the rectifier operation, but increases losses in the remaining switches.

The results show that there are only minor differences in the method operation between AC and DC power inputs when the observer residual values are compared. Figures 3.5–3.8a and b show the DC and AC operation, respectively. When these figures are compared, it can be seen that the method is insensitive to voltage ripple at U_{in}. This is due to the fact that the model is accurate enough at the 100 Hz frequency, at which the DC link ripple occurs. Therefore, practically no error between the model and the measured signal is seen.

As shown, the method is able to detect changes in the converter operation only at the system level. By applying this method, it is not possible to explicitly define the mechanism or the single component causing variation in the state observer residuals. The system-level condition monitoring method, such as the presented one, is beneficial in those applications where it is relevant to detect the variation from the known and expected operation. This is for example the case in the condition monitoring of systems where the health of a single converter unit is assessed on the scale of normal operation, or the device operation has changed considerably, or the device is soon about to fail, rather than assessing the unit at a more detailed, component level. The usefulness of the method is thus clear in those cases where the complete converter unit will be changed when anomalies in the operation are detected, rather than replacing the faulty components on site during the maintenance.

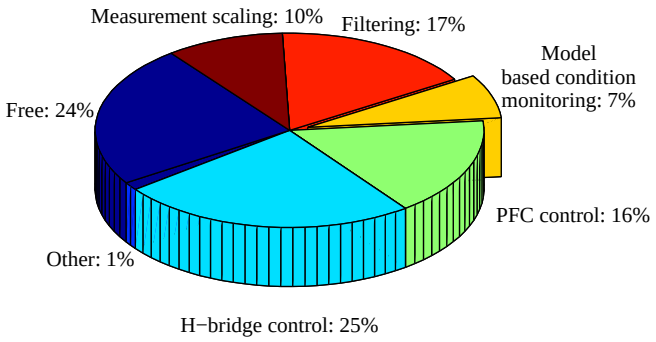

Figure 3.9. Analysis of the execution time requirement, where the worst case of the required computational resources of the model-based condition monitoring method is shown.

Chapter 4

Output Voltage Step Method for Detection of an Output Stage Capacitor Aging in a DC/DC Converter

Electrolytic capacitors are widely used in power converter applications as they offer a high capacitance in relation to their volume (Aeloiza et al., 2005). The disadvantage of the electrolytic capacitors is that they are among those main circuit components that are most prone to aging in a switching mode power supply (Kulkarni et al., 2012; Yu et al., 2012; Bourgeot, 2010; Lee et al., 2008; Aeloiza et al., 2005; Lahyani et al., 1998; Harada et al., 1993). Capacitor aging is a nonlinear process, where the increased losses resulting from an increased ESR in the capacitor accelerate the degradation process (Harada et al., 1993; Lee et al., 2008).

This chapter describes a procedure to detect the aging of the capacitor at the DC/DC converter output stage. To this end, an output voltage transient method is proposed to detect a change in dynamics in the converter output stage circuit. The content of this chapter is related to Publication III, which addresses the analytical background, sensitivity analysis, simulations, and experimental tests when using a DC/DC converter. In this chapter, the key points of the method are presented, and the feasibility of the method is studied with an AC/DC converter introduced in Chapter 2. Further, solutions to enhance the feasibility of the method and make it more robust against measurement noise and other disturbances are considered. The effects of the method on the required computational resources are also discussed.

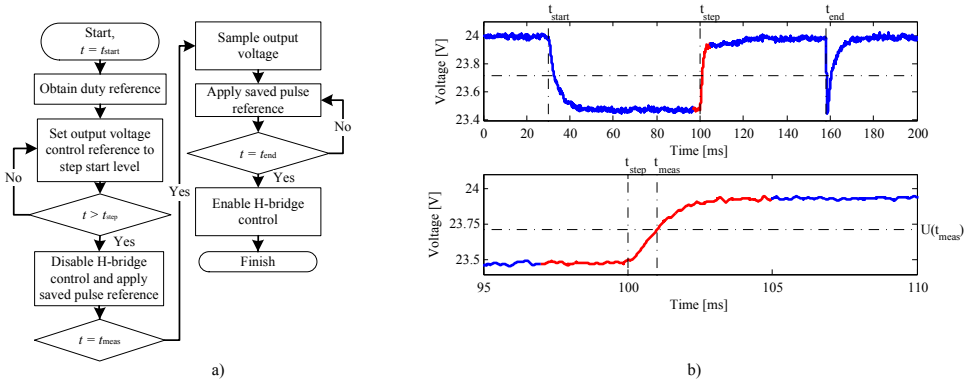

Figure 4.1. Flow chart representation of the step process in subfigure a) and the corresponding waveform in b). The beginning of the step excitation is denoted by t_{start}, the beginning of the step response by t_{step} and the end of the procedure by t_{end}. The bottom plot of subfigure b) shows an enlargement of the step response. The step voltage is sampled at t_{meas} =1 ms after t_{step}, which is plotted on the magnified graph.

4.1 Step response for output capacitor condition monitoring

The condition of the output stage capacitor of the converter is evaluated in the dynamic state of the output voltage. It is expected that a decrease in the converter output capacitance alters the converter output voltage dynamics so that the voltage response to a fixed-size step excitation becomes faster. In order to remove the effect of the power stage control on the voltage dynamics, the control must be deactivated during the step response. Figure 4.1 shows the step voltage production with a flow chart representation and the corresponding waveform, which is generated to define the output voltage dynamics.

The step excitation, response, and sampling process, shown in Figure 4.1, consist of the following key points:

1. When entering the procedure at t_{start}, save the duty cycle reference that corresponds to the controlled steady-state output voltage in the prevailing operating conditions.

2. Reduce the converter output voltage to the step start level by changing the output voltage control reference, in this case from 24 V to 23.5 V. Wait for a steady state.

3. Disable output stage control at t_{step}. Apply the duty cycle obtained in 1. A voltage step defined by the output circuit dynamics is generated.

4. Sample the output voltage in the predefined evaluation point t_{meas} so that $U_{\text{meas}} = U_{\text{out}}(t_{\text{meas}})$.

5. System control can be enabled again after sampling. In this case it is done at t_{end}.

6. Compare the U_{meas} with a known reference measured with a converter in pristine condition in the corresponding operating point.

Analytical evaluation of the method under study can be carried out by using the converter model presented in Chapter 3 and Publication III. In the analytical study, the capacitor voltage U_{C} is used instead of the output voltage in order to emphasize the relation between the capacitor voltage and the decrease in the capacitance in the studied case. In practical applications, the voltage over the capacitor cannot be separated from the voltage over the equivalent series resistance. Therefore, it is assumed that the difference between the capacitor voltage and the output voltage is negligible.

From the model (3.10) shown in Chapter 3, a transfer function from the duty cycle to the capacitor voltage can be derived when $\boldsymbol{A}$ and $\boldsymbol{B}$ are assumed constant. An input to output transfer function for a linear system is defined by

$$G(s) = \boldsymbol{C}_m(s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B}_n, \tag{4.1}$$

where the identity matrix is denoted by $\boldsymbol{I}$, the input parameter vector by $\boldsymbol{B}_n$, and the output vector by $\boldsymbol{C}_m$. In this system, the output voltage and thereby the capacitor voltage are defined by a controlled duty cycle of the H-bridge. Therefore, the transfer function from d to U_{C} is used, which can be denoted with respect to (4.1) as (Cao, 2007)

$$G(s) = \frac{U_{\text{C}}(s)}{d(s)} = \frac{U_{\text{DC}}R_{\text{load}}}{CLnR_{\text{b}}k(s)} \tag{4.2}$$

where, the $k(s)$ is

$$k(s) = s^2 + (\frac{R_{\text{a}}}{L} + \frac{1}{CR_{\text{b}}})s + \frac{R_{\text{a}}}{CLR_{\text{b}}} + \frac{{R_{\text{load}}}^2}{LC{R_{\text{b}}}^2}. \tag{4.3}$$

By using the transfer function (4.2), it can be shown that a monotonic decrease in the output stage capacitance produces a monotonic increase in the voltage measured in a constant measurement point t_{meas}. The analytical verification is presented in Appendix A.

In Publication III, the sensitivity of the output stage voltage step dynamics is analyzed with respect to variations in C, L, R_{ESR}, R_{eq}, and R_{load}. In brief, the sensitivity analysis indicates that the key contributors to the step voltage dynamics are the variations in the secondary-stage capacitance and the secondary-side inductance. The study also shows that changes in R_{eq} and R_{ESR} have a negligible effect on the output voltage dynamics. Figure 4.2 demonstrates the effect of L and C variation on the step response.

The decrease in the output stage capacitance increases $\text{d}U_{\text{C}}/\text{d}t$ and thereby the voltage sampled at t_{meas}. It is shown in Figure 4.2 that a decrease in the secondary inductance has a

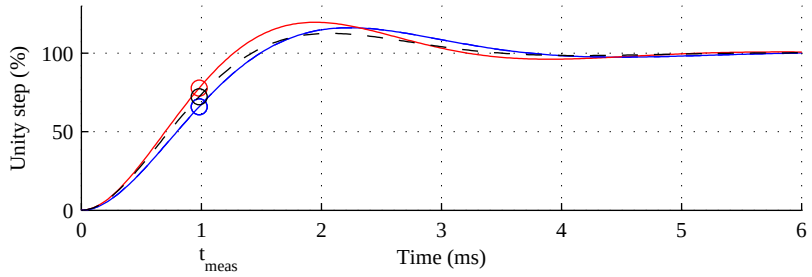

Figure 4.2. Unity step response using nominal converter parameters (blue), 20 % reduced capacitance (red), and 20 % reduced secondary inductance (dashed black). The capacitor degradation has the most significant impact on the step response, as can be seen from the curve in red, having the highest value at t_{meas}.

similar influence on the step response as the capacitor degradation. The inductance variations are mainly caused by the core material saturation when the inductors use soft magnetic core materials such as ferrite. Therefore, the decrease in the inductance in the converter output stage is a function of throughput current. With ferrite materials, it has been shown that excessive temperature fluctuations, for instance thermal shocks, may cause fractures in the core material, yet ferrite core fractures are very unlikely in normal operating conditions (De Graaf et al., 1995). Therefore, it is improbable to observe an inductor aging phenomenon, at least to the same degree as capacitor aging, during the expected useful lifetime of the converter.

On the other hand, it is evident that the fluctuation in inductance resulting from magnetic core saturation affects the converter output stage dynamics. If it is assumed that the secondary-side inductors are subject to inductance fluctuations, a nonlinear behavior of the step response $U_{\mathrm{out}}(t_{\mathrm{meas}})$ with respect to the load current can be assumed.

4.2 Sources of uncertainty in the voltage step

Publication III describes the basic principles of generating a voltage step and analyzing the capacitor condition from the voltage step response. As the purpose of the publication is to introduce the method and analyze its feasibility, disturbances outside the sensitivity analysis are not discussed in detail.

Practical issues such as ripple in the H-bridge duty cycle and insufficient PWM resolution cause consistency problems to the resulting voltage step. Because these limitations lead to variations in the uncontrolled voltage step, they directly produce uncertainty in the sampled U_{meas}. In the following, the above-mentioned sources of uncertainty are discussed.

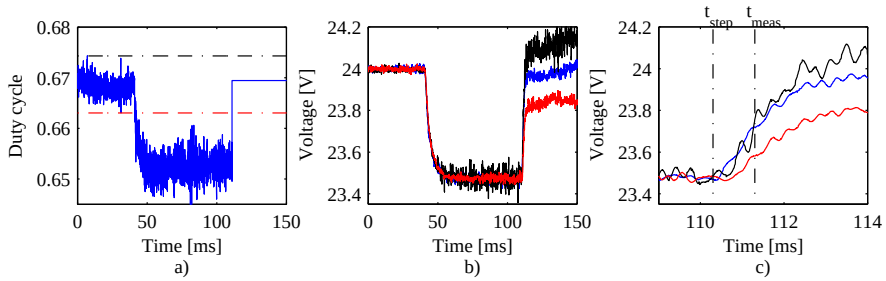

Figure 4.3. Effect of duty cycle variation on the step response. Subfigure a) illustrates the variation in the duty cycle during steady-state operation before entering the step process. Blue color shows the produced step, which corresponds to the averaged duty cycle. Red and black colors indicate the minimum and maximum values of the duty cycle variation, respectively. Subfigure b) shows the effect of duty cycle variation on the step voltage in the maximum and minimum duty cycles, and subfigure c) presents an enlargement of subfigure b) illustrating the effect of variation on the step voltage at t_{meas}.

4.2.1 Duty cycle variation

During normal converter operation, the system control determines the duty cycle, which corresponds to the output voltage reference in the prevailing operating conditions such as the load current. Ideally, the duty cycle reference in steady-state operation is constant, but disturbances such as measurement noise and input voltage ripple cause variation in the duty cycle. This is caused by the system control, which is mitigating the effect of those disturbances that are within the controller bandwidth. Figure 4.3 illustrates the duty cycle variation at the H-bridge and depicts the corresponding effect of the duty cycle variation on the voltage step response of the experimental device under study.

When analyzing the effect of the duty cycle on the step voltage shown in Figure 4.3, it can be seen that it is not convenient to only use the latest value of the controlled duty cycle to generate the output voltage step as it introduces a significant possibility of variation into the resulting step size. It is shown that the 0.5 V step size is subject to variation of $\pm$ 0.2 V, which is 40 % of the overall step size. This directly decreases the accuracy of U_{meas}, as seen in Fig. 4.3c.

In order to improve the consistency of the measurement results, rather than taking only one duty cycle sample before starting the step process, an average value of multiple duty cycle reference samples should be used to produce the voltage step. This eliminates the high-frequency variation from the duty cycle shown in Figure 4.3a. In addition to averaging the duty cycle reference, numerous sequential U_{meas} values should be measured, and their average value should then be used to analyze the dynamics of the output voltage.

4.2.2 Insufficient PWM resolution

In Publication III, it is stated that the size of the output voltage step is not a crucial parameter when considering the feasibility of the method. This statement is valid when it is assumed that the resolution of the pulse width modulator is sufficient to produce a negligible error in the step size.

The resolution of the pulse width modulator generates similar step size issues as shown in Figure 4.3b. In general, the modulator resolution presents the maximum accuracy that can be achieved with the corresponding number of bits. For example with the experimental system of this study, the H-bridge modulator is implemented with 11-bit resolution. The converter and thus the modulator are designed to generate a maximum of 32 V output voltage with the 100 % duty cycle, which yields an output voltage resolution of

$$V_{\text{res}} = \frac{32\,\text{V}}{2048} = 15.6\,\text{mV}. \tag{4.4}$$

This means that the step voltage has an inherent uncertainty of 15.6 mV in the step size even if it assumed that the applied saved duty cycle reference generates a perfect, correctly sized voltage step. The issue of the PWM resolution is demonstrated in Table 4.1, which shows how accurately the output voltage could be presented with respect to the PWM resolution of 8–12 bits.

Table 4.1. Effect of PWM resolution on the output voltage.

Bits	8	9	10	11	12
Resolution (mV)	125.0	62.50	31.25	15.63	7.8125

As shown in Table 4.1, the resolution defines the minimum level of error in the voltage step. According to the results, it can be stated that the lower the PWM resolution is, the larger is the step size required to avoid a significant error in U_{meas}.

4.3 Feasibility of the method with an AC/DC converter

In Publication III, the feasibility of the voltage step method was studied and analyzed using a DC/DC converter. In this study, the feasibility assessment is extended to the AC/DC converter presented in Chapter 2.

When the AC power input is used, sinusoidal ripple of two times the mains frequency is generated into the converter primary-side DC link voltage. This ripple is caused by the sinusoidal input current. Thus, the ripple amplitude in the DC link is defined by the DC link capacitance and the throughput power. Figure 4.4 shows the ripple voltage in the DC link in the DC/DC and AC/DC converter cases when using 15 A and 100 A load currents.

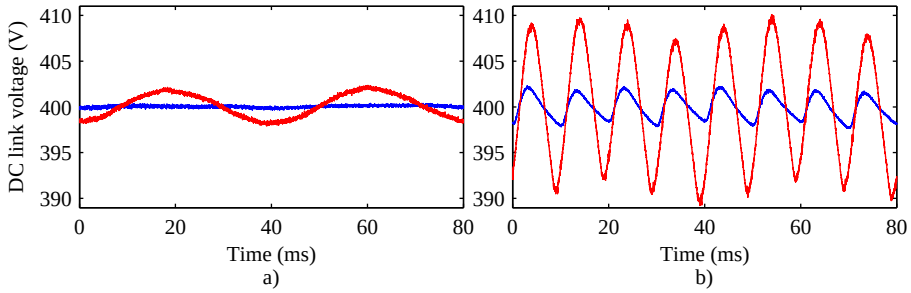

Figure 4.4. DC link voltage in two different loading conditions with the DC power input in subfigure a) and the AC power input in b). Blue color indicates 15 A and red 100 A load current.

Considering the method under study, the DC link voltage ripple poses challenges as the ripple effect is directly seen at the secondary current and thus at the output voltage when the system control is disabled. This can be shown analytically by using the model of (3.10). The model states that the secondary current is defined by

$$\dot{I}_{\text{sec}} = -\frac{R_{\text{a}}}{L} I_{\text{sec}} - \frac{R_{\text{load}}}{L R_{\text{b}}} U_{\text{C}} + \frac{dU_{\text{DC}}}{Ln}. \tag{4.5}$$

As stated above, in the AC input case, sinusoidal voltage variation of twice the mains frequency is produced in the DC link voltage; the DC link voltage can be defined as

$$U_{\text{DC}} = U_{\text{DC,ref}} + U_{\text{r}} \cos\left(4\pi f_{\text{m}} t + \phi_{\text{m}}\right), \tag{4.6}$$

where U_{DC} is the reference DC link voltage, U_{r} is the ripple voltage amplitude, f_{m} is the mains frequency, and ϕ_{m} is the mains phase. Now, when U_{DC} in (4.6) is substituted with (4.5), it can be seen that during the voltage step, in which the duty cycle is constant, the ripple voltage in the DC link has a direct impact on the secondary current. As the output voltage is also a function of secondary current, as shown in (3.10), the output voltage is subject to sinusoidal oscillation. Figure 4.5 depicts the output voltage step when the DC link voltage contains 100 Hz ripple of an amplitude dependent on the load current.

The ripple in the DC link and thus in the output voltage, caused by the AC power input, is directly proportional to the load current. With the 100 A load current, significant sinusoidal oscillation is introduced into the voltage step, as can be seen in Figure 4.5. The issues are evident when the ripple amplitude is large enough to have an effect on the step response. This is the case for example in Figure 4.5b, as the step voltage in t_{meas} is defined by the voltage ripple rather than by the dynamics determined by the output stage. The results show that the 0.5 V step size, which was used in the DC input power case, is insufficient to detect a degradation of the capacitor condition by this method.

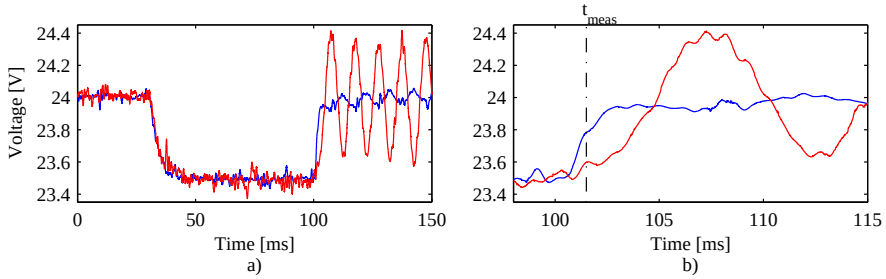

Figure 4.5. Effect of the DC link ripple on the output voltage step response at 15 A (blue) and 100 A (red) load currents with a 0.5 V step size and the nominal output stage capacitance. The ripple defines $U_{\text{out}}(t_{\text{meas}})$ at the 100 A load current.

4.3.1 Measurement results with the AC power input

In the AC power input case, the DC link ripple is dominated by the input current amplitude, which, in turn, is dependent on the converter load. Therefore, with increased load currents, the DC link ripple compromises the method feasibility if the step behavior is dominated by the DC link voltage ripple rather than by the physical conditions of the output circuit. Therefore, the method with the AC power input is applied by using a 1 V step size in order to proportionally reduce the ripple voltage amplitude versus the voltage step size.

The measurements have been carried out in a similar fashion as in the DC power input case, reported in Publication III. The step voltage is assessed with the converter, the parameters of which are given in Table 3.1 in Chapter 3. In the experimental converter, the output capacitance is produced by using 3 x 3.9 mF and 10 x 1.2 mF capacitors in parallel. The capacitor aging is emulated by reducing the number of 1.2 mF capacitors, and consequently, a decrease in C and an increase in R_{ESR} are achieved. The C and R_{ESR} values used in the experimental tests are listed in Table 4.2.

Table 4.2. Absolute and percent variation of capacitance and capacitor equivalent series resistance in the experimental tests

C_{tot} (mF)	C_{tot} (%)	R_{ESR} (mΩ)	R_{ESR} (%)
23.7	100	1.30	100
22.5	95	1.36	105
21.3	90	1.42	109
20.1	85	1.48	114
18.9	80	1.54	118
17.7	75	1.60	123
16.5	70	1.66	128

The output voltage measurements are obtained using the built-in AD converters of the microcontroller. The duty reference used for the step response is averaged over 100 controlled duty cycle references before entering the step response procedure. The output voltage step

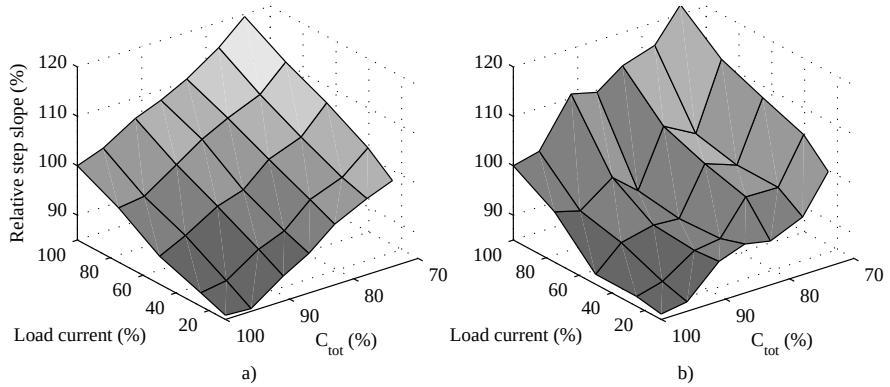

Figure 4.6. Step response measurement results with respect to a varying load current and a decrease in the output stage capacitance. In subfigure a) the DC input and in b) the AC input results are presented.

is sampled at $t_{\text{meas}} = 1\,\text{ms}$ after t_{step}. 100 sequential voltage steps are generated, and the corresponding average value of U_{meas} samples is used as a measurement result.

The variation in capacitance is examined with load currents of 100 %, 75 %, 50 %, 25 %, and 10 % with respect to 100 A. In the tests, the load current was changed by varying the load resistance. Figure 4.6 illustrates U_{meas} with respect to variations in the load current and a decrease in the output capacitance. In the figure, the 100 % load current represents 100 A and 100 % C_{tot} corresponds to 23.7 mF. The measurement result with the DC power input, the analysis and results of which are comprehensively discussed in Publication III, is taken as a reference at which the measurement results can be compared with the AC power input results.

The comparison of Figures 4.6a and b shows that when the step response is evaluated with the AC power input, significant uncertainty in the result can be observed compared with the results measured with the DC power input. Despite the fact that the step response in the AC case is performed using a 1 V step instead of a 0.5 V step in the DC case, the result includes considerable variations between different load currents and capacitor conditions. Nevertheless, the result with the AC input exhibits a similar trend with respect to the degradation of the capacitor as shown with the DC power input.

4.4 Discussion

As it was demonstrated in Publication III and in the results above, the feasibility of the method depends on various aspects. It was shown that the method is affected by several factors, which cause considerable measurement uncertainty. Therefore, it is obvious that no one measurement sample provides sufficient information on the capacitor condition. When the data considering output voltage behavior are collected over a long period of time, a trend in

the change in dynamics can be detected.

In the study, an analytical model was used to determine the feasibility of the method in the presented converter. With the model, it is possible to evaluate the sensitivity of the voltage seen over the capacitive part of the capacitor so that any of the parameters affecting the step voltage behavior can be investigated individually. In the study, it is assumed that the impedance of the ESR does not have a significant impact on the step voltage behavior. On the other hand, it has been mentioned in (Cao, 2007) that the ESR together with the capacitance will produce a zero in the transfer function (4.2). If the zero is at those frequencies where the capacitive part of the capacitor impedance dominates the step behavior, the step voltage response will rise faster. When considering the applicability of the method, this is beneficial, as an increase in the ESR pushes the zero towards lower frequencies and thereby makes the step response to rise even faster, thus emphasizing the aging effect seen with the decreasing capacitance.

In the following, the effects of the AC power input and converter load construction on the feasibility of the method are discussed. Further, the effect of the method on the microcontroller processing resources is assessed in the experimental converter case of this study.

4.4.1 Feasibility of the method with the AC input

It has been shown that the sinusoidal variation in the DC link voltage generates considerable uncertainty into the step measurement result. When the AC measurement results shown in Figure 4.6b are analyzed, it is evident that the measured step voltage can vary up to 10 %, within one 1.2 mF decrease in the capacitance. Thus, the application of the obtained data for condition monitoring is not straightforward.

As it was mentioned in Section 4.2.1, the duty cycle used to produce the voltage step has to be averaged over a large number of controlled samples to obtain a consistent step. In the AC case, the controlled duty cycle of the H-bridge oscillates with the DC link ripple frequency, which is normal as the voltage control rejects the DC link ripple at the converter output voltage. In order to generate uniform sequential voltage step responses, the duty cycle to be applied has to be averaged at least over one fundamental oscillation cycle of the DC link voltage ripple before entering the step excitation process at t_{start}.

Yet another consistency-related issue arises from the timing of the step response with respect to the phase of the DC link ripple. If the step response is produced randomly with respect to the DC link voltage ripple phase, the voltage step will also include step size deviations. The step size variation can be expected to be evenly distributed, and thus, by averaging of a large number of step samples, the variation can be eliminated. Another approach to reduce the effect of the DC link ripple on the step response size is to synchronize the step response to start at a certain DC link ripple oscillation phase. Preferably, the step is carried out in the DC link ripple phase when the ripple $\mathrm{d}u/\mathrm{d}t$ is at the minimum. Thus, the step is affected by the DC link ripple as little as possible, when it is assumed that the step has faster dynamics than the DC link ripple.

In order for the method to be feasible with the AC power input, a large number of measurement data are required to define the system operation because of the large variation in the measurement results. By using a large amount of data, long-term averaging is able to reveal the trend in increasing transient dynamics in the converter output stage despite the significant inconsistencies seen in the results.

4.4.2 Effect of a load on the feasibility of the method

In the experimental tests on the method presented in Publication III and in this chapter, a resistive load was used. In an actual application, a load may also include reactive elements, which have an effect on the output voltage dynamics. Considering the feasibility of the method, the effect of a load cannot be separated from the converter internal dynamics, which is a fundamental limit of the shown method. For example, a capacitive load is seen directly parallel to the output stage capacitor. It should be noted that the load capacitance with the converter under study has to be in the range of 500–1000 µF to have an effect on the step response behavior. This is because the failure criterion, 80 % of the pristine condition output stage capacitance, equals a 4.7 mF change in the capacitance. Thus, variations in the range of tens to hundreds of microfarads in the load capacitance do not have a significant effect on the applicability of the method. In those cases where the capacitive load is significant compared with the internal capacitor, the effect of a load on the system must be known, and it may not have varying dynamics that would affect the output voltage behavior in order to find the shown method feasible.

Another issue with the method is that it cannot be used when the converter is operated at loads that are not stable in an uncontrolled state. In these cases, the system would exhibit sustained oscillation because of inadequate damping. Examples of such cases are constant current and constant power loads such as another converter.

4.4.3 Effect of the detection method on the system total execution time

The effect of the detection method on the control loop execution was analyzed by the same methods as in Chapter 2. Figure 4.7 presents a worst-case scenario of the processing resources required of the key tasks in the control loop, including the method for detecting capacitor aging.

The voltage step method for detecting capacitance variation was shown to be efficient in the sense of execution time consumption. The method requires 6 % of the available resources at the control loop time level with the implementation chosen for the converter prototype. This can be considered rather a low requirement when compared with other tasks executed in the control loop.

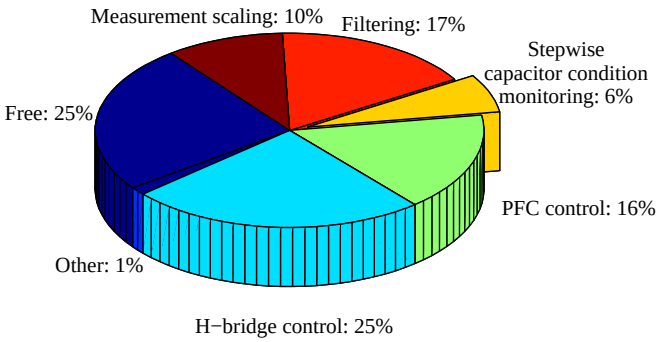

Figure 4.7. Analysis of execution time requirements, where the worst case of the computational resources required by the capacitor detection procedure is emphasized.

Chapter 5

Sinusoidal Voltage Injection Method for Detection of an Output Stage Capacitor Aging in a DC/DC Converter

Detection of capacitor aging has traditionally been carried out by monitoring changes in the ESR of the capacitor. Various authors have proposed that the aging-based increase in R_{ESR} can be evaluated by observing the increased switching ripple amplitude seen in the capacitor voltage (Kulkarni et al., 2012; Amaral and Cardoso, 2012; Lee et al., 2008; Lahyani et al., 1998; Harada et al., 1993).

According to Ohm's law, capacitor impedance is expressed as the relation between voltage and current with respect to frequency. For a capacitor, impedance is defined by capacitance, parasitic inductance, and resistance, which are determined by the capacitor structure and materials applied. Now, when the capacitor is operated in a frequency range where the capacitance and the parasitic inductance are in series resonance, the impedance is at its minimum. The minimum impedance in an actual capacitor is defined by the equivalent series resistance.

The R_{ESR} detection is feasible when the self-resonance frequency of an electrolytic capacitor is close to the converter switching frequency. In this case, the ripple current and thus the ripple voltage amplitude are defined by the R_{ESR} according to Ohm's law. Therefore, it is relevant to monitor the increase in the voltage ripple amplitude, as it can be directly linked to an increased R_{ESR}, which is an effect of capacitor aging-based degradation.

Nowadays, the switching frequencies, especially in power supplies, are often in the range of tens to hundreds of kilohertz. Therefore, it is not always certain that the switching frequency and thereby the switching-based voltage ripple are close to the capacitor self-resonance fre-

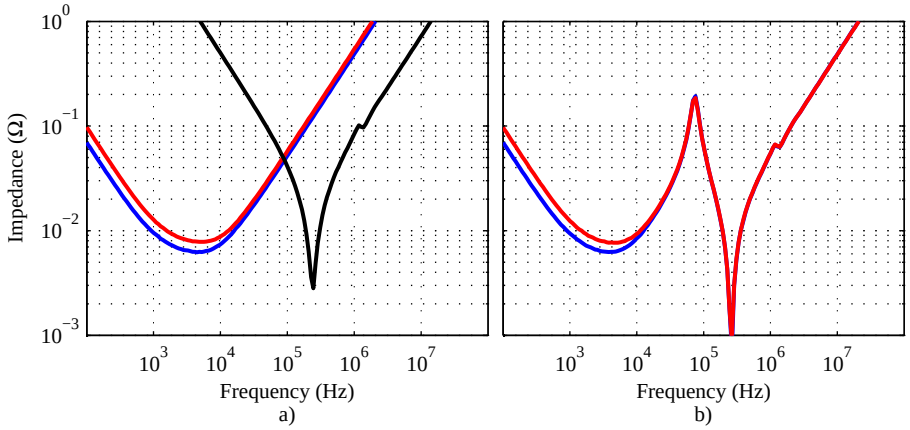

Figure 5.1. Capacitor impedance as a function of frequency. In subfigure a), the impedances of a film capacitor of 33 µF (black) and electrolytic capacitors of 23.9 mF (blue) and 16.7 mF (red) are presented when measured separately. In subfigure b), the parallel connection of the film capacitor with 23.9 mF (blue) and 16.7 mF (red) electrolytic capacitors is shown. The parasitic inductance of the electrolytic capacitor dominates the impedance at frequencies between 10 and 100 kHz, and for the film capacitor above 100 kHz in the parallel-connected case.

quency. Again, the aging detection using only R_{ESR} involves certain issues, if capacitors of different dielectric materials such as film capacitors are used in parallel with the electrolytic capacitor under study. In this case, it is not evident that the impedance behavior of the parallel-connected capacitors is defined by the electrolytic capacitor in the proximity of the switching frequency.

In order to illustrate the behavior of capacitor impedance with respect to frequency, the impedance of a single film capacitor of 33 µF and two sets of parallel-connected electrolytic capacitors with a total capacitance of 23.7 mF and 16.5 mF are studied using an impedance analyzer. The capacitors of 23.7 mF and 16.5 mF correspond to the nominal output stage capacitance and approximately 30 % decreased capacitance of the experimental converter, respectively. The 16.5 mF one emulates an aged capacitor, which, according to (Defense Logistics Agency and Maritime, 2008), is beyond the specified operating range of a low-voltage capacitor. A 33 µF film capacitor is chosen to illustrate the effect of a parallel-connected film capacitor on the impedance behavior of the capacitor. The electrolytic capacitors used in this study are specified for a 35 V operating voltage range. The total nominal capacitance consists of 3x3.9 mF and 10x1.2 mF parallel-connected electrolytic capacitors. Figure 2.2b shown in Chapter 2 illustrates the capacitors and the experimental platform used to vary the output stage capacitance.

In the impedance analysis, all the three above-mentioned combinations of capacitors are first measured separately, and then, two electrolytic capacitor sets are measured with the parallel-connected film capacitor. Figure 5.1 shows the impedance in each measured combination.

Figure 5.1a shows that the impedance of the electrolytic capacitor is determined by the ESR only within the 5–10 kHz frequency span. In the frequency range above 10 kHz, the capacitor impedance is defined by the parasitic inductance of the electrolytic capacitor, which shows no difference between the two measurements. When the capacitors are evaluated in parallel in Figure 5.1b, it can be seen that at frequencies above 100 kHz the impedance is completely determined by the film capacitor.

When it comes to the switching frequency ripple, it can be assumed that the capacitor introduces the lowest impedance for the switching frequency voltage ripple. When Figure 5.1 is analyzed, it can be seen that there is practically no difference in the impedance in the frequency band of 10 kHz and above. Therefore, the voltage ripple amplitude at frequencies above 10 kHz is not affected by an increase in R_{ESR} nor a decrease in C, which are the commonly used precursors of capacitor aging.

5.1 Capacitance evaluation using sinusoidal voltage injection

As shown in Figure 5.1, in the case under study, a change in the impedance with respect to the change in the electrolytic capacitor capacitance can be seen at frequencies below 1 kHz. The impedance of the capacitor in this frequency span is given by

$$Z_{\mathrm{C}} = \frac{1}{2\pi f C}, \tag{5.1}$$

where f is the applied frequency. A single frequency voltage produces a corresponding current through the capacitor, which is determined by the capacitor impedance. The impedance can be defined by the relation of the applied voltage injection and the corresponding capacitor current by

$$Z_{\mathrm{C}} = \frac{\hat{u}}{\hat{i}}, \tag{5.2}$$

where $\hat{i}$ and $\hat{u}$ are the amplitudes of the capacitor AC current and AC voltage, respectively. The capacitance can thus be solved from (5.1) and (5.2) by

$$C = \frac{\hat{i}}{2\pi f \hat{u}}. \tag{5.3}$$

In actual converter systems, the capacitor current is not generally measured for control purposes. Considering the experimental converter shown in Figure 3.1 in Chapter 3, the capacitor current can be obtained by

$$I_{\mathrm{C}} = I_{\mathrm{sec}} - I_{\mathrm{load}}. \tag{5.4}$$

Considering that the converter load can have unknown reactive components, it is beneficial to measure the load current, and thus, the current of the reactive load is neglected when the capacitor current is obtained by (5.4). It is also common that only either the load or the secondary current is measured for control purposes, which is also the case with the experimental device studied here. The secondary current can be estimated using the DC link current measurement from the primary as the DC link current and the secondary current have only a negligible difference in dynamics. Therefore, by scaling the DC link current from the primary to the secondary, the secondary current is obtained.

In some cases, as in the experimental case of this study, the DC link current measurement technique shown in Publication I and the current measurement circuit in the analog domain produce nonlinearity in the measured current, which is emphasized in operation at low powers. Therefore, the secondary current is obtained by using an experimentally defined nonlinear gain function for the DC link current. The DC link current for the secondary current scaling was discussed in Chapter 3.

5.1.1 Method implementation on the experimental device

In the experimental system, the 50 Hz sinusoidal signal injection into the output voltage is performed at the control loop time level. A smooth sinusoidal output voltage oscillation with an amplitude of 150 mV is obtained by modifying the output voltage controller reference with a sinusoidal signal, the samples of which are precalculated in a look-up table. In each control cycle, one sample is added to the output voltage reference until the required amount of signal injection is achieved. In this experimental case, one period of 50 Hz sinusoidal signal consists of 1000 samples. Thus, producing four times of 1000 samples of injection corresponds to four fundamental cycles of 50 Hz sinusoidal oscillation as the control loop is executed at 50 kHz. The sample size of 4000 samples is chosen based on the applied data logging buffer length. It is pointed out that the injected signal frequency must be within the band of the voltage control loop.

During the injection, the measured samples of the secondary and load currents are stored for the capacitor current calculation. The calculated capacitor current is not directly suitable for capacitance evaluation as the data contains disturbance caused by the DC link ripple, switching frequency ripple, and measurement noise. Therefore, the calculated capacitor current is filtered using a bandpass filter with a narrowband at the sinusoidal voltage injection frequency.

When the signal injection procedure and the corresponding samples of the secondary and load currents are stored during the injection, the capacitor current is calculated and filtered outside the control loop. During the filtering, the peak amplitude of the filtered capacitor current is determined. The output stage capacitance is defined according to (5.3) using the peak values

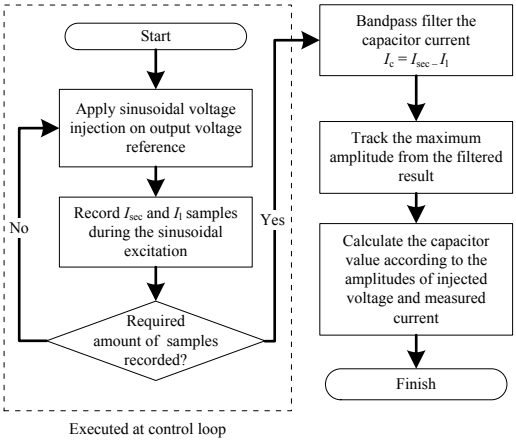

Figure 5.2. Flow chart representation of the sinusoidal voltage-injection-based capacitance evaluation. The injection is carried out by adding precalculated sinusoidal values from a look-up table to the output voltage reference until the injection of 4000 samples has been executed. Only the signal injection and measurement sampling are carried out within the control loop execution. The obtained data are analyzed outside the control loop in order to avoid excessive processing at the control loop time level.

of the filtered current ($\hat{i}$) and the injection voltage amplitude ($\hat{u}$). Figure 5.2 shows a flow chart representation of the proposed capacitance evaluation procedure, and Figure 5.3 presents the signal injection and the corresponding current response obtained by the presented algorithm.

The capacitor current is filtered using a digital 2nd-order bandpass IIR filter, designed using the Butterworth algorithm. The filter passband crossover frequencies are set to 44–58 Hz in order to obtain an adequate filtering result for the 50 Hz current component and a satisfactory time domain performance. Figure 5.4 illustrates the filter frequency response and the time domain step response.

As shown in Figure 5.4, the applied filter requires at least 160 ms of settling time before the filtered result has less than a 0.5% error. As the 4000 saved samples of data correspond to a 80 ms length of data because of the 50 kHz sample rate, the saved data have to be run through the filter three times to achieve less than a 0.5 % uncertainty. Figure 5.5 shows an example of the filtering procedure and peak value detection for the capacitor current.

The experimental tests for the feasibility of the method are carried out by varying the operating conditions. In the tests, the load current, the secondary capacitor size, and the load structure are varied. The capacitor aging is emulated by reducing the capacitance by physically removing capacitors from the converter secondary in the range of 23.7 mF–16.5 mF with 1.2 mF steps. With each output capacitance, the method is assessed with an array of load currents: 15 A, 25 A, 50 A, 75 A, and 100 A. The proposed method is also verified using a capacitive load structure where a 12.6 mF capacitor is placed in parallel with the resistive load. The 12.6 mF load capacitance corresponds to a 53 % increase with respect to the nominal output stage capacitance, thus representing a large enough change to be able to assess the conclusions on the applicability of the method with capacitive loads. In the capacitive load

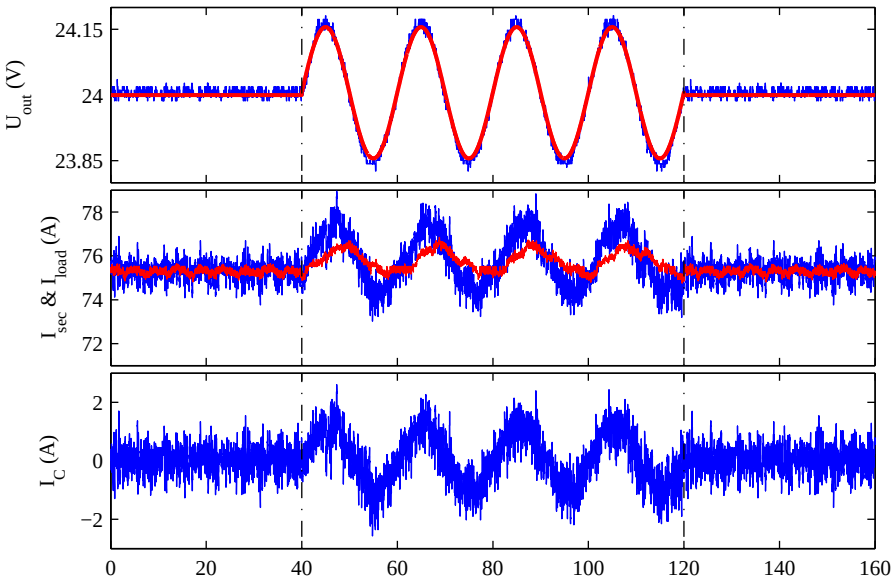

Figure 5.3. Sinusoidal voltage excitation and the corresponding response. In the upper subplot, the controlled output voltage oscillation (blue) and the corresponding voltage controller reference (red) are depicted. The output voltage oscillation produces oscillation at the secondary current (blue) and the output current (red), which are shown in the subplot in the middle. The subtraction of these currents equals the capacitor current, which is demonstrated in the bottom subplot.

tests, the converter secondary capacitances of 23.7 mF, 20.3 mF, and 16.5 mF are used. The measurements are carried out by producing a sinusoidal signal injection 50 times at 0.2 second intervals for each load current and capacitance. This is done in order to get information on the statistical variations in the capacitance evaluation.

Measurement results with the DC power input

The tests with the DC power input are made using the DC/DC part of the AC/DC converter presented in Chapter 2. Because of the limited capabilities of the laboratory instrumentation, the maximum load current of the converter is limited to 100 A. The results of the study are presented with combined standard uncertainty, which includes statistical variations of the measured results and the known and evaluated static uncertainties. The uncertainties are caused by environmental effects, measurement noise, and method implementation such as filtering of the current. The measurement uncertainty is evaluated according to a combined uncertainty analysis, shown in (JCGM, 2008), which takes into account the A- and B-type uncertainties in the measurements.

The experimental tests were made in a steady room temperature of 22°C. Because of losses generated in the capacitors, the capacitor temperatures are expected to have minor variation.

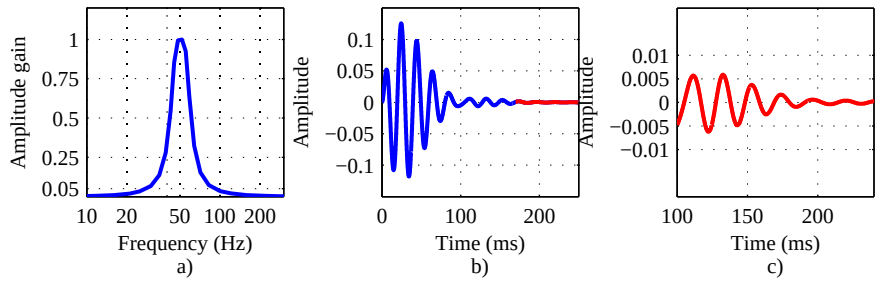

Figure 5.4. Frequency response of the bandbass filter for detecting the 50 Hz component in the capacitor current shown in subfigure a) and the time domain step response in b) and c). Subfigure c) depicts an enlarged filter time domain response of the response indicated by red in b). Subfigure c) shows that the filter requires at least 160 ms in order to produce a less than 0.5 % error in the result.

According to (Epcos AG, 2014), the effect of temperature variation in the range of 20–100°C is less than 10 % on the electrolytic capacitor capacitance. Therefore, in this study, it is assumed that the temperature variation in the output stage capacitors produces a 1 % uncertainty at most in the calculated capacitance.

As shown in Figure 5.4c, the filter time-domain response produces some variation in the filter output. Therefore, the filtering result is assumed to cause a maximum of 0.5 % uncertainty in the capacitor current. The major static source of uncertainty is caused by the secondary current estimation, which has a direct impact on the uncertainty in the capacitor current. In the experimental tests, a 4 % uncertainty was determined for the secondary current estimation.

Other error sources such as AD conversion uncertainty, output voltage fluctuation at the DC link ripple frequency, and measurement circuit temperature drifting are considered to cause statistical variations between the sequential measurements. Therefore, 50 sequential samples of capacitance to be assessed are collected for each measurement result, and the standard deviation between the samples is defined and then used for the uncertainty analysis.

Figure 5.6 illustrates graphically the measurement data where the output stage capacitance value is assessed 50 times at each load current used in the test. The capacitance is evaluated with a resistive converter load and a DC power input. In the figure, capacitance measurement data with 23.7 mF, 21.3 mF, 18.9 mF, and 16.5 mF output stage capacitances are shown as an example.

The measurements shown in Figure 5.6 are also carried out with 22.5 mF, 20.1 mF, and 17.7 mF output stage capacitances. All the measured capacitance values are analyzed statistically in order to define standard uncertainty for the results. All the measured capacitances and their corresponding standard uncertainties are presented in Table 5.1, where the capacitances are assessed using a resistive load. An example of the uncertainty calculation is given in Appendix B. In addition, Table 5.2 shows measurement results using capacitances of 23.7 mF, 20.1 mF, and 16.5 mF when a 12.6 mF capacitive load used in parallel with the resistive load.

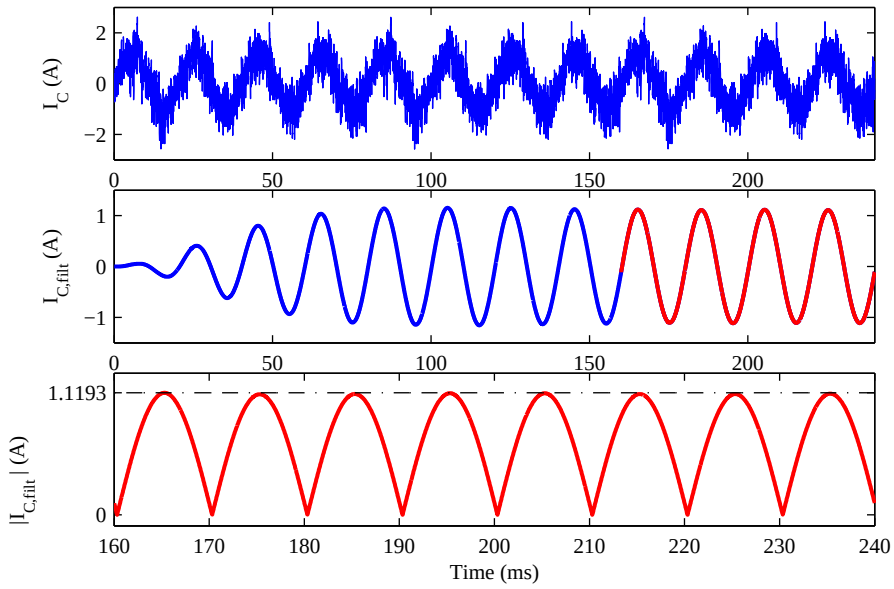

Figure 5.5. Detection of the peak amplitude from the obtained capacitor current. First, the capacitor current shown between the dashed lines in the bottom subplot of Figure 5.3 is filtered three times through the bandpass filter. This consists of 160 ms of data, seen in the filter input in the upper figure. The figure in the middle presents the corresponding filter output current. The absolute value of the last 4000 samples (indicated in red in the middle subplot and magnified in the bottom subplot) is used to determine the peak capacitor current.

Table 5.1. Measured capacitance in various loading conditions for a resistive load using a DC input power. Each result is the mean value of 50 measured samples ± the combined standard uncertainty. All capacitance values are given in mF.

Expected C	C 15 A	C 25 A	C 50 A	C 75 A	C 100 A
23.7	23.5 ± 0.6	23.7 ± 0.7	23.9 ± 0.9	23.8 ± 0.8	24.0 ± 0.8
22.5	22.3 ± 0.7	22.6 ± 0.8	22.8 ± 1.0	22.4 ± 0.7	22.9 ± 0.7
21.3	21.2 ± 0.8	21.4 ± 0.7	21.4 ± 0.7	21.3 ± 0.7	21.3 ± 0.7
20.1	20.1 ± 0.7	20.2 ± 0.6	20.2 ± 0.6	20.1 ± 0.7	20.1 ± 0.7
18.9	19.0 ± 0.6	19.1 ± 0.7	18.7 ± 0.7	19.0 ± 0.7	19.0 ± 0.6
17.7	17.5 ± 0.6	17.9 ± 0.7	17.3 ± 0.6	17.6 ± 0.5	17.6 ± 0.6
16.5	16.5 ± 0.6	16.6 ± 0.6	16.3 ± 0.6	16.5 ± 0.5	16.8 ± 0.6

AC input results

The method is also tested by using an AC power input. As it was shown in Chapter 2, the AC input generates DC link voltage ripple of twice the mains frequency. In addition, the voltage

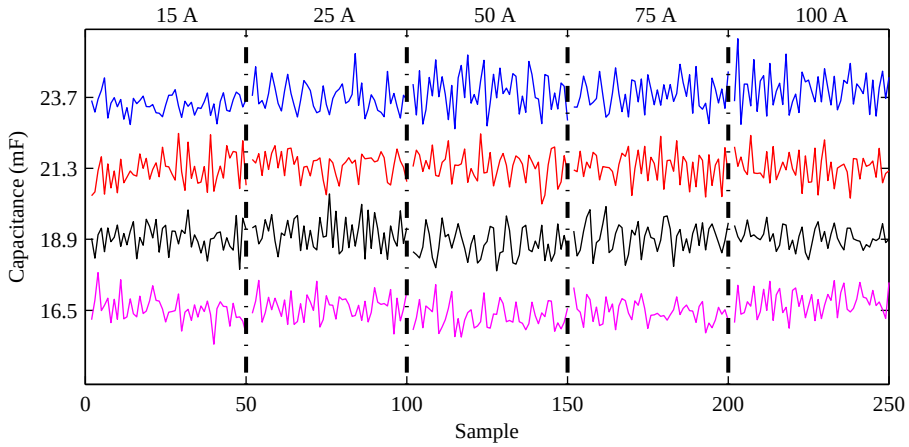

Figure 5.6. Capacitance measurement results with 23.7 mF, 21.3 mF, 18.9 mF, and 16.5 mF output stage capacitance. The x-axis depicts measured samples of the output stage capacitance. The results are given in sections indicated by dashed lines. Each section consists of 50 samples with a load current shown above in the corresponding section. The ticks on the y-axis indicate the expected capacitance value.

Table 5.2. Measured capacitance in various loading conditions for parallel capacitive and resistive loads using DC input power. Each result is the mean value of 50 measured samples ± the combined standard uncertainty. All capacitance values are given in mF.

Expected C	C 15 A	C 25 A	C 50 A	C 75 A	C 100 A
23.7	24.0 ± 0.7	24.2 ± 0.9	24.0 ± 0.7	23.8 ± 0.8	23.3 ± 0.8
20.1	20.7 ± 0.6	20.8 ± 0.7	19.9 ± 0.6	20.1 ± 0.6	20.0 ± 0.8
16.5	17.1 ± 0.7	17.0 ± 0.6	15.9 ± 0.6	16.5 ± 0.5	16.7 ± 0.5

ripple amplitude in the DC link depends on the throughput power. Therefore, the effects of ripple on the operation of the proposed method have to be defined.

The tests with the AC input are carried out in a similar fashion as in the DC input case. Tables 5.3 and 5.4 show the capacitance evaluation results of resistive and capacitive load tests, respectively, with the corresponding uncertainties when an AC power input is used.

The AC results show that the feasibility of the method does not change considerably when the measurement with the DC power input is used as a reference. The difference can be seen in the uncertainties, which gradually increase when moving towards higher load currents. This is due to the DC link current ripple, which has the higher amplitude, the higher power level is used.

Table 5.3. Measured capacitance in various loading conditions for a resistive load using AC input power. Each result is the mean value of 50 measured samples ± the combined standard uncertainty. All capacitance values are given in mF.

Expected C	C 15 A	C 25 A	C 50 A	C 75 A	C 100 A
23.7	23.8 ± 0.7	23.8 ± 0.7	23.8 ± 0.6	24.3 ± 0.6	23.4 ± 1.0
22.5	22.9 ± 0.7	22.7 ± 0.6	23.4 ± 1.0	23.0 ± 1.0	21.8 ± 0.9
21.3	22.2 ± 0.6	21.7 ± 0.6	22.0 ± 0.8	21.9 ± 1.0	21.0 ± 1.0
20.1	20.4 ± 0.6	20.5 ± 0.6	20.5 ± 0.8	21.1 ± 1.0	20.1 ± 1.0
18.9	19.5 ± 0.7	19.3 ± 0.6	19.1 ± 0.8	19.6 ± 1.0	18.9 ± 0.9
17.7	17.9 ± 0.5	17.6 ± 0.5	18.2 ± 0.7	18.4 ± 1.0	18.2 ± 1.0
16.5	16.9 ± 0.7	16.9 ± 0.5	16.1 ± 0.5	16.1 ± 0.4	16.2 ± 0.8

Table 5.4. Measured capacitance in various loading conditions for parallel capacitive and resistive loads using AC input power. Each result is the mean value of 50 measured samples ± the combined standard uncertainty. All capacitance values are given in mF.

Expected C	C 15 A	C 25 A	C 50 A	C 75 A	C 100 A
23.7	24.2 ± 0.6	24.1 ± 0.7	24.5 ± 0.9	23.8 ± 1.1	23.3 ± 1.0
20.1	20.1 ± 0.5	20.0 ± 0.6	20.4 ± 0.8	19.8 ± 0.5	19.9 ± 1.0
16.5	16.7 ± 0.6	16.7 ± 0.6	16.6 ± 0.4	16.2 ± 0.5	16.5 ± 1.0

5.1.2 Effect of the detection method on the system total execution time

The execution time requirement of the method is compared with the total resources reserved for control loop execution. Figure 5.7 shows a chart where the effect of the presented algorithm on the required processing resources is emphasized.

The results in Figure 5.7 show that the method requires only 4 % of the control loop execution time resources. This requirement of processing resources only represents the method-caused burden on the control loop execution, even though the method also requires processing time outside the control loop, as can be seen in Figure 5.2. For this reason, the execution time required by the analysis is not included in the chart. The analysis of execution time resources demonstrates that the method is highly efficient in terms of required processing resources when compared for example with the other tasks executed in the control loop.

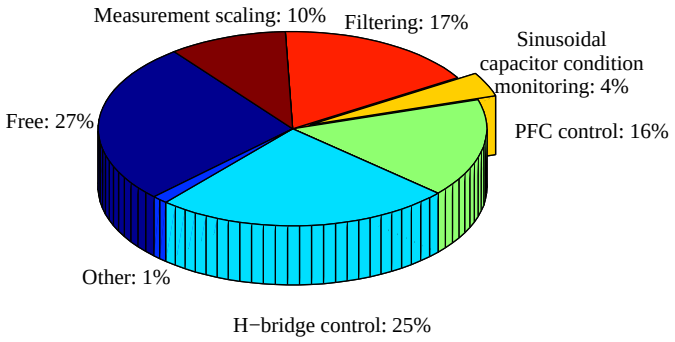

Figure 5.7. Execution time requirement chart, which shows the worst-case effect of the condition monitoring method of sinusoidal voltage injection on the control loop execution time.

5.2 Discussion

The feasibility of the method in the experimental converter system under study is highly dependent on the capacitor current accuracy. It was stated above that the secondary current in the system is estimated, as there is no direct measurement available. Because of the limited number of experimentally obtained samples used for determining the scaling function, there is residual between the actual and estimated secondary currents, which directly leads to an error in the capacitor current. Considering the secondary current estimation, discussed in Chapter 3, it can be approximated that the issue is emphasized at low operating powers, as the relation between the DC link current and the secondary current is more nonlinear compared with operation at higher powers, and thus, higher currents. Despite this, a constant 4 % error in the capacitor current was used in the uncertainty analysis throughout the operating range to simplify the analysis.

The overall feasibility of the method can be analyzed using the highest obtained uncertainty for each capacitance value regardless of the load current. In practice, according to the presented results, this decides how accurately the method can define the size of the output capacitor. Figure 5.8 illustrates the worst-case analysis using error bars with both the AC and DC input power cases.

Based on the results, it is evident that the method is capable of detecting a decreasing capacitance with a sufficient accuracy. This means that less than 20 % variation in capacitance is detectable, which, according to the military specification (Defense Logistics Agency and Maritime, 2008), is the maximum decrease for capacitance. As the capacitance measurement system is evaluated with 1.2 mF steps at the output stage capacitance, it can be concluded that a 2.4 mF change in the output capacitance is indisputably detectable, as shown in Figure 5.8. Therefore, the method can detect 10 % variation in the converter output stage capacitance

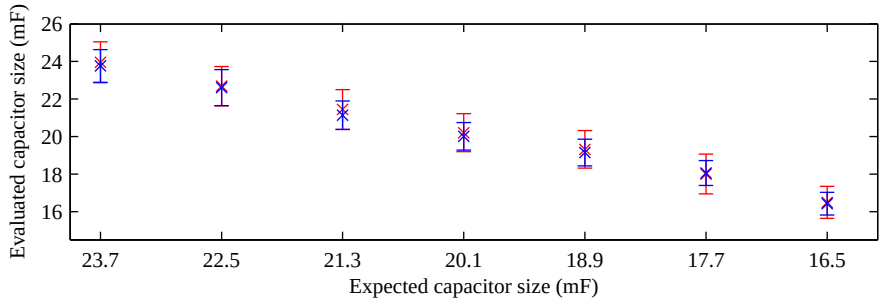

Figure 5.8. Expected and evaluated capacitance value with the corresponding worst-case error bars. The presentation shows the effect of the increased uncertainty between the DC (blue) and AC (red) power inputs.

under consideration.

Chapter 6

Conclusions

This doctoral dissertation introduced applications to be used for the condition monitoring of a power supply. The proposed state observer and output voltage excitation methods are suitable for monitoring system health during operation, and they can be implemented without any extra measurement instrumentation in addition to the ones used for converter control. The dissertation summarized, discussed, and elaborated on the system design and condition monitoring methods reported in Publications I–IV.

In Publications II–IV, the condition monitoring methods were presented using an isolating DC/DC converter. In these publications, the DC/DC converter applied was the isolating converter part of the AC/DC converter shown in Publication I and Chapter 2. In this dissertation, the applicability of the methods discussed in the publications was assessed using an AC power input and thereby an AC/DC power conversion stage in addition to the DC/DC converter. The use of the AC power input and the power stage for power factor correction produces disturbance in the DC/DC converter operation. Therefore, conclusions on the sensitivity of each method against the DC link voltage disturbance can be made. Besides the feasibility study, the burden caused by each method on the microcontroller processing resources was evaluated.

According to the results, the aging phenomenon in this converter type can be detected without additional measurement instrumentation. The main contribution and thus the scientific impact of the doctoral dissertation is that aging of the DC/DC-type converter output capacitor of this kind as well as increased losses in the main circuit can be detected during the converter operation. When the results are analyzed against the objectives of the study, it can be stated that the study provides new information on aging detection methods and their applicability.

Considering the main research questions of this work, it has been shown that increasing system losses and decreasing capacitance are aging precursors that can be detected without any measurement hardware modifications, assuming that measurements from the converter are accessible as described in this doctoral dissertation.

The methods studied in this doctoral dissertation bring benefits both to the manufacturer and the power supply customers. The condition monitoring methods raise the value of the converters as a result of the increased functionality. For example, condition monitoring decreases the need for maintenance, which is based only on the expected lifetime of certain components in the converters. On the other hand, devices with degraded condition can be taken care of before a serious failure in the system occurs. This benefits the customer as the unexpected process interruptions caused by an unexpected power converter failure decrease.

6.1 Conclusions on the feasibility of the studied methods

The model-based aging detection was studied in the converter steady-state and load transient operation. It was found that the method is feasible for detecting increased losses in the DC/DC converter secondary, but the degraded capacitor has a slight effect on the residual behavior in the operating conditions used in the tests. Considering the feasibility of the method, it can be stated that the method can be used to determine the converter output stage degradation only at the system level. This means that the method cannot distinguish the root cause of the fault, nor it can identify the component that is causing anomalies in the system operation. This is due to the fact that there are various factors in the converter main circuit components that have an effect on the output voltage and the secondary current behavior. Therefore, it is only possible to narrow down the possible degraded components that are causing variations in the converter operation when variation with respect to normal operation in the state observer residual parameter is detected.

In the studies, it was found that the detection of the aged output stage capacitor requires dynamic conditions in terms of change in the capacitor voltage, whereas increased losses in the secondary stage can be detected in the converter steady-state operation without affecting the converter behavior. Thus, to determine the output stage capacitor health, two output voltage excitation methods were presented: output voltage step and sinusoidal voltage injection. The output voltage excitations directly produce disturbance in the output voltage and thereby in the converter operation. This is an inevitable disadvantage of the presented excitation-based capacitance aging detection methods.

Considering the voltage step method, the operation with a DC input power has been found to be feasible for detecting capacitor aging. The decrease in capacitance at the converter output stage increases the step response dynamics in a predictable manner. According to the tests with an AC power input, it was found that the method is highly sensitive to primary-side DC link voltage oscillation. Therefore, when an AC power input is used, the feasibility of the method is compromised. It has been shown that the method requires a large enough step size to mitigate the effect of the DC link voltage ripple when an AC power input is used. In general, with an AC power input, the step size has to be larger than the step size that can be used with a DC power input. In addition, the load structure affects the feasibility of the method as a reactive load has a direct influence on the output voltage dynamics. Thus, when a converter is operated with reactive loads, the effect of load on the voltage dynamics must be identified or known in order to find out whether the voltage step method is feasible for

detection of output capacitor aging.

When the method of sinusoidal voltage injection is considered, the results confirm that the method is feasible for detecting a decreased capacitance at the converter output stage. In addition, it was demonstrated that the method is insensitive to capacitive loads, which makes the method suitable for systems where the converter load structure may change in terms of reactive parts. It was also shown that the method can be used with both AC and DC power inputs without any major issues considering the uncertainty in the capacitance evaluation. It has been established that the method can determine the output stage capacitance with a 2.4 mF accuracy with the converter used in this study. The drawback of the method is that the load current measurement and the secondary current estimation accuracies affect the result uncertainty, because the capacitor current is calculated as a subtraction of these currents. Therefore, proper validation of these current signals is essential when considering the feasibility of the method.

When the two voltage-excitation-based capacitor aging detection methods are compared, it can be seen that the sinusoidal method overcomes the majority of the issues of the step excitation method. When the prototype converter under study is considered, only 150 mV sinusoidal signal injection amplitude is needed, while the step voltage method requires up to 1 V step size to obtain reliable measurement results.

The condition monitoring methods reported in this work have been studied only using a specific isolating AC/DC converter topology. Despite this, the methods can also be applied to detect the degradation with other topologies. In general, the capacitor voltage must be measured to apply any of the methods presented in this dissertation, yet the model-based and sinusoidal voltage injection methods also require current measurement information.

The application often defines the limits, for example the output voltage and output current ripple. Thus, when the excitation methods reported in this study are applied, it must be first determined whether the excitations within the allowed range of variation are able to show any symptoms of aging for instance in a capacitor. In this study, approximately a 2% step size was used with the step method, which yielded a 0.5 V step size. When the method is used in a low-voltage case, such as a 3.3 V output voltage system, the 2% step size equals 69 mV. In order to find the method feasible, the measurement system has to be of adequate quality to distinguish the changes caused by capacitor aging from the background noise.

The methods shown in this study can be viable for detecting the degradation of DC link capacitors, yet variations in the DC link may cause significant disturbance to the converter operation. When the step method is applied, the step size should be selected such that the output voltage regulation is not compromised. In practice, this means that there has to be enough voltage in the DC link during the step so that the output voltage can still be controlled, as it was shown in Chapter 2. In AC input systems, such as the converter presented in this study, the DC link is inherently introduced with AC ripple, which can be exploited for condition monitoring. In this case, the current through the capacitor is directly the subtraction of the input and output currents, which are both measured. Thus, the DC link capacitor capacitance can be assessed without any additional excitation or extensive calculation, if it is assumed

that the mains frequency is constant.

By applying the condition monitoring methods presented in this dissertation, it is not possible to detect individual component aging in those cases where the observed phenomenon, such as an increase in step dynamics, is caused by multiple components. For example in the presented converter case, it cannot be defined by the presented methods whether the faster step dynamics is caused by a single failed capacitor, or whether all the capacitors have degraded to the same extent. The methods are applicable at the system level, where it is irrelevant from the viewpoint of practical system maintenance which single component has deteriorated.

6.1.1 Conclusions on computational resources

The computational requirements for the converter control system and condition monitoring were evaluated in each case under study. It was shown that the power stage control algorithms and digital signal processing of the measurement signals require 69 % of the available processing time of the microcontroller. The rest, 31 % of the available resources can be used for supporting and upkeep functions. It is emphasized that the lower-priority tasks such as the user interface are not included in the analysis, as they are not running at the control loop time level.

The study on the computational resources required by the condition monitoring methods shows that the heaviest method in terms of resource consumption is the model-based method, which uses 7 % of free resources. From the perspective of control loop execution, the lowest processing resources are required from the microcontroller by the sinusoidal excitation method, which consumes only 4 % of the available resources. However, it is pointed out that the measured requirements are heavily dependent on the digital implementation of each proposed condition monitoring method.

In general, none of the presented condition monitoring methods takes an extensive amount of processing resources. This can be seen when comparing the requirement of processing resources of any of the methods with any other task in the control loop. Thus, it can be concluded that these methods can run alongside the converter core control functions without compromising the hard real-time demand for the control loop operation in the presented experimental system case.

6.2 Suggestions for further studies

Besides the method sensitivities to the AC and DC power input, no other parameters were considered in this doctoral dissertation. The motivation of the study was to develop new approaches and procedures to condition monitoring without making changes to the system hardware. Therefore, the methods proposed in this dissertation were tested only as a proof of concept. For this reason, the methods were not assessed in various environmental operating

conditions such as extreme temperatures, which will have an effect on the behavior of the output stage electrolytic capacitors. In order to determine the robustness of the methods against varying environmental conditions, further research is needed.

In this study, the aging effects were emulated by modifying the converter main circuit components and their operation. In future studies, the methods should be verified by proper component aging tests, where the converter components are subjected to actual aging instead of artificial faults or aging emulation.

Considering the excitation-based methods, further research is needed to obtain more consistent results and minimize the uncertainty in the measurements. This is especially crucial with the voltage step method when AC input power is used. Further, the load capacitance identification system should be established to make the step voltage method feasible regardless of the load construction. In order to ensure the applicability of the step method with an AC power input, a method for eliminating the effect of DC link voltage ripple from the voltage step has to be developed. Some promising preliminary results have already been obtained by using a step duty cycle modification method, where scaled-down DC link ripple is injected into the step duty cycle reference in an opposite phase.

In this work, the methods were presented from analytical and practical implementation viewpoints. Nevertheless, it was not considered how the obtained information can be used to analyze the converter health in the long term. Therefore, in future studies, the assessment of the remaining useful lifetime, that is, prognostics of the converter by using the information acquired by these methods should be investigated.

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Appendices

Appendix A

Proof of a monotonic increase in the step voltage in a constant measurement point with respect to a decrease in capacitance

It can be shown that a monotonic decrease in the secondary capacitance produces a monotonic increase in the voltage measured in a constant measurement point t_{meas}, which is located on the rising edge of the step response. This can be shown by using a canonical differential equation

$$G(s) = \frac{U_{\text{out}}}{U_{\text{in}}} = \frac{1}{(as^2 + bs + c)}, \tag{A.1}$$

where a, b, and c corresponding to (4.2) are obtained upon substitution of (4.3) into (4.2).

$$\begin{aligned} a &= CLnR_{\text{b}}, \\ b &= n(CR_{\text{a}}R_{\text{b}} + L), \\ c &= n(R_{\text{a}} + \frac{R_{\text{load}}}{R_{\text{b}}}). \end{aligned} \tag{A.2}$$

The system is stable because $L, C, R_{\text{load}}, R_{\text{b}}, R_{\text{a}} > 0$, and thus, also $a, b, c > 0$ (Hurwitz, 1895). The canonical transfer function can be expressed as

$$\begin{aligned} G(s) &= \frac{y}{u} = \frac{1}{as^2+bs+c} \\ G(s) &= ays^2+bys+cy = u. \end{aligned} \tag{A.3}$$

A homogeneous differential equation is generated by denoting $u = 0$ as the input does not affect the system dynamics. Therefore, the homogeneous differential equation is written as

$$y'' + \frac{b}{a}y' + \frac{c}{a}y = 0. \tag{A.4}$$

A homogeneous differential equation can be solved by the corresponding characteristic equation. The characteristic equation for (A.4) is

$$r^2 + Br + C = 0, \tag{A.5}$$

where

$$B = \frac{b}{a},\ C = \frac{c}{a}. \tag{A.6}$$

The roots r_1 and r_2 of the quadratic equation (A.5) are directly the system poles that affect the system dynamics. The second-order characteristic equation can have the following solutions:

1. $r_1 \neq r_2, r_1, r_2 \in \mathbb{R}$

$$y = C_1 e^{r_1 t} + C_2 e^{r_2 t} \tag{A.7}$$

2. $r_1 = r_2 = r, r_1, r_2 \in \mathbb{R}$

$$y = (C_1 t + C_2) e^{rt} \tag{A.8}$$

3. $r_1 = \alpha + i\beta, r_2 = \alpha - i\beta$

$$\begin{aligned} y &= e^{\alpha t}(C_1 \cos(\beta t) + C_2 \sin(\beta t)) \\ &= e^{\alpha t}(C\cos(\beta t + \theta)), \\ C &= \sqrt{\alpha^2 + \beta^2} \\ \theta &= \frac{\beta}{\alpha}, \end{aligned} \tag{A.9}$$

where $C_{1,2}$ represent constants of integration.

The direction in which the slope of the step response changes at t_{meas} is dependent on the sign of the derivatives of the solution (A.7)–(A.9). The system step response slope changes in a certain direction with respect to a monotonic parameter drift of the circuit components, for example a decrease in capacitance or an increase in equivalent series resistance, if the derivatives of (A.7)–(A.9) are monotonic. It is pointed out that the analysis does not give information of a simultaneous parameter drift if the drifting parameters have an opposite effect on the step response slope.

Equations (A.7)–(A.9) provide functions that define the root r with respect to time t and constants $C_{1,2}$. Providing that the analyzed system is stable, $\text{Re}(r) < 0$ must apply. The first time derivatives $\dot{y}$ for (A.7)–(A.9) can be expressed respectively

1.
$$\dot{y} = r_1 C_1 e^{r_1 t} + r_2 C_2 e^{r_2 t} \tag{A.10}$$

2.
$$\dot{y} = (C_1 + rC_1 t + rC_2) e^{rt} \tag{A.11}$$

3.
$$\dot{y} = Ce^{\alpha t}(\alpha \cos(\beta t + \theta) - \beta \sin(\beta t + \theta)) \tag{A.12}$$

The constants $C_{1,2}$ can be expressed with system initial conditions. The derivatives can be analyzed by assuming that the starting point of the step response can be defined to be 0 in all three cases. Thus, the initial conditions can be expressed as

$$\begin{aligned} y(0) &= 0 \\ y'(0) &> 0. \end{aligned} \tag{A.13}$$

By solving the constants $C_{1,2}$ for (A.7)–(A.8) and (A.10)–(A.11), it can be noted that cases 1) and 2) are always monotonic as $r_{\text{x}} < 0$.

When case (A.12) is analyzed, it can be seen that the derivative is monotonic only on the rising edge of the step response. The step response is monotonically increasing before

$$\alpha \cos(\beta t + \theta) - \beta \sin(\beta t + \theta) = 0 \tag{A.14}$$

applies for the first time when $t > 0$.

As the third case represents an oscillating response that closes asymptotically the settling value as $\alpha < 0$ and $\beta > 0$ it also defines that the limits for t_{meas} must be located. The response sampling has to be done before (A.14) applies for the first time.

Appendix B

Example calculation of uncertainty

The analysis of the measurement result uncertainty is made applying practices shown in (JCGM, 2008). The combined standard uncertainty is used, which presents the cumulative error sum in the measurement considering both A and B type measurement uncertainties. The combined standard uncertainty is the square root of the combined variance

$$u_{\mathrm{c}}{}^{2}(y) = \sum_{i=1}^{N} \left(\frac{\partial f}{\partial x_{\mathrm{i}}} \right)^{2} u^{2}\left(x_{\mathrm{i}}\right) \tag{B.1}$$

where u_{c} is the standard uncertainty, f is the function to be partially derived according to the parameter x_{i}, and u is the uncertainty of the corresponding parameter of x_{i}. The uncertainty evaluation process used in this study assumes that each error source has equal upper and lower bounds, and consequently, the distribution is symmetrically rectangular within the uncertainty range. If the specific measurement errors considering the measurable parameter x are denoted by μ, the variance $u^2(x)$ can be calculated as a square sum

$$u^{2}(x) = \sum_{i=1}^{N} \frac{\mu_{\mathrm{i}} c}{\sqrt{(3)}} \tag{B.2}$$

where c denotes the expected value such as the mean value of the set of observations, and i the ith source of error affecting the parameter x.

The application of these functions can be presented by an example. Let us consider the following initial conditions as known parameters. The measured mean value of the set of 50 measurements for capacitance is C = 24.013 mF. The variance obtained from the measurements is u_{C}^{2} = $1.91 * 10^{-}7$. The capacitance is obtained with a current amplitude of $\hat{i}$ = 1.1057 A, which is also the mean value resulting from the set of 50 measurements.

Error sources in measurements:

- Temperature, 1 % of capacitance ($\mu_{\mathrm{C,T}}$)
- Filter, 0.5 % of capacitor current ($\mu_{\mathrm{i,filt}}$)
- Secondary current estimation, 4 % of capacitor current ($\mu_{\mathrm{i,est}}$)

It has been shown in Chapter 5 that the capacitance is calculated by

$$C = \frac{\hat{i}}{2\pi f \hat{u}}. \tag{B.3}$$

In this analysis, it is expected that only the current and the capacitance are influenced by the measurement uncertainty, as the capacitance is calculated using a fixed amplitude of $\hat{u} = 0.15\,\mathrm{V}$ and a fixed frequency $f = 50\,\mathrm{Hz}$. Therefore, according to (B.1), a partial derivative of (B.3) is only required with respect to $\hat{i}$ for combined uncertainty calculation. The partial derivative for (B.3) is

$$\frac{\partial C}{\partial \hat{i}} = \frac{1}{2\pi f \hat{u}}. \tag{B.4}$$

The variance for $\hat{i}$ is calculated as a squared sum

$$u^2(\hat{i}) = \left(\frac{\mu_{\mathrm{i,filt}}\hat{i}}{\sqrt{3}}\right)^2 + \left(\frac{\mu_{\mathrm{i,est}}\hat{i}}{\sqrt{3}}\right)^2. \tag{B.5}$$

Therefore, the total uncertainty considering the capacitance can now be defined

$$u_{\mathrm{c}}(C) = \sqrt{\left(\frac{1}{2\pi f \hat{u}}\right)^2 u^2\left(\hat{i}\right) + \left(\frac{\mu_{\mathrm{C,T}} C}{\sqrt{3}}\right)^2 + u_{\mathrm{C}}^2} \tag{B.6}$$

Substituting $\hat{i} = 1.0649\,\mathrm{A}$ and the given measurement error values into (B.5) yields

$$u^2(\hat{i}) = \left(\frac{0.005 * 1.1057}{\sqrt{3}}\right)^2 + \left(\frac{0.04 * 1.1057}{\sqrt{3}}\right)^2 = 6.6223 * 10^{-4}. \tag{B.7}$$

Now, by substituting (B.5) into (B.6), and using the rest of the given parameters,

$$u_c(C) = \sqrt{\left(\frac{1}{2\pi 50 * 0.15}\right)^2 * 6.6223 * 10^{-4} + \left(\frac{0.01 * 0.024013}{\sqrt{3}}\right)^2 + 1.91 * 10^{-7}} \\ = 0.71304 * 10^{-3} \tag{B.8}$$

a combined standard uncertainty of approximately 0.7 mF for the measurement is obtained.

Publication I

Hannonen J., Ström J. P., Honkanen J., Räisänen S., Pokkinen O., and Silventoinen P.

"Design of Digitally Controlled Isolating 1-phase AC/DC Converter by Using Centralized Processing Unit"

in *15th European Conference on Power Electronics and Applications (EPE),* August, 2013

Publication II

Hannonen J., Honkanen J., Ström J. P., Räisänen S., and Silventoinen P.

"Luenberger state observer based condition monitoring method in digitally controlled switching mode power supply"

in *16th European Conference on Power Electronics and Applications (EPE'14-ECCE Europe)*, September, 2014

Publication III

Hannonen J., Honkanen J., Ström J. P., Kärkkäinen T., Räisänen S., and Silventoinen P

"Capacitor Aging Detection in a DC–DC Converter Output Stage"

IEEE Transactions on Industry Applications, vol. 52, no. 4, pp. 3224–3233. April, 2016

Publication IV

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"Capacitance measurement method using sinusoidal voltage injection in isolating phase-shifted full-bridge DC–DC converter output stage"

IET Power Electronics, vol. 9, no. 13, pp. 2543–2550. October 2016

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