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Vladislav Marochkin

NOVEL SOLUTIONS FOR IMPROVING SOLID-STATE PHOTON DETECTOR PERFORMANCE AND MANUFACTURING

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Supervisor Professor Tuure Tuuva
LUT School of Engineering Science
Lappeenranta University of Technology
Finland

Reviewers Professor Jyrki Räisänen
Department of Physics
University of Helsinki
Finland

Docent Eija Tuominen
Detector Laboratory
Helsinki Institute of Physics
Finland

Opponent Professor Jyrki Räisänen
Department of Physics
University of Helsinki
Finland

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Abstract

Vladislav Marochkin

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Radiation is all around us and most of the time we are not able to see it, nevertheless it brings us valuable information about the world we live in, so it is very important to be able to detect it with high accuracy. This thesis explores the ways and brings solutions of improving performance and manufacturing of solid-state radiation detectors which are used for detecting photons (electromagnetic radiation) within various energy ranges: near-infrared light, visible light, ultraviolet light, x-ray and gamma radiation.

Solid-state radiation detectors have been under active development during the last 30 years. The development has been driven by needs of better spatial and energy resolution, higher readout speeds, and higher particle densities in fields and applications dealing with photon detection.

Radiation detectors have been evolving as new technologies were becoming available, as a result, more and more sophisticated detectors and systems of detectors were made available.

Nowadays, semiconductor detectors are used in a large variety of fields: science, including nuclear physics, elementary particle physics, optical and x-ray astronomy,

material testing; medicine, image sensors, technology and consumer applications. The number of applications grows continually.

There is a constant demand for solid-state radiation detector performance improvement from all the fields where they are used. The performance of a solid-state detector has improved significantly for last 30 years and nowadays there are many various concepts of a solid-state detector which are used in various applications: pin-photodiode, silicon drift detector, depleted p-channel field-effect transistor, charge coupled device, etc. But there is still room for improvement.

The goal of this work was to address known challenges and improve performance and manufacturability of solid-state radiation detectors.

As a result, several new concepts of solid-state detectors were developed. Performance of new structures was verified by 2D and 3D process and device simulations in Technology Computer Aided Design (TCAD) software. Proposed concepts considerably improve performance of solid-state radiation detectors in terms of removing issues with interface generated dark noise, reducing interface generated 1/*f* noise, reducing interface generated Random Telegraph Signal, improving quantum efficiency, reducing cross-talk, and improving signal-to-noise ratio. Developed concepts also make manufacturing of radiation-detectors easier since for most of the concepts a standard CMOS process can be used. Another valuable feature is a possibility of using another semiconductor materials, like for example germanium for manufacturing the same radiation detectors which was not possible previously due to interface related issues.

Keywords: backside illuminated, fully depleted, modified internal gate, silicon drift detector, detector chip design, process simulation, device simulation, 3D simulation, 3D detector, vertical drift detector.

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Espoo, Finland

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Publications

List of publications

This dissertation is based on four publications presented in international conferences and journals. The papers were first published by IOP Publishing Limited and SISSA Medialab Srl, which maintain the Version of Record, under the Creative Commons Attribution 3.0 License and are in open access. The following publications are referred to in the text by their numerals:

I. Aurola, A., Marochkin, V. and Tuuva, T. (2015), "Characterization of double modified internal gate pixel by 3D simulation study", Journal of Instrumentation, vol. 10, C01040, DOI: 10.1088/1748-0221/10/01/C01040.

II. Aurola, A., Marochkin, V., Golovleva, M. and Tuuva, T. (2015), "Novel silicon drift detector design enabling low dark noise and simple manufacturing", Journal of Instrumentation, vol. 10, C02047, DOI: 10.1088/1748-0221/10/02/C02047.

III. Aurola, A., Marochkin, V. and Tuuva, T. (2014), "A radiation detector design mitigating problems related to sawed edges", Journal of Instrumentation, vol. 9, C12019, DOI: 10.1088/1748-0221/9/12/C12019

IV. Aurola, A., Marochkin, V. and Tuuva, T. (2016), "A novel 3D detector configuration enabling high quantum efficiency, low crosstalk, and low output capacitance", Journal of Instrumentation, vol. 11, C03040, DOI: 10.1088/1748-0221/11/03/C03040

Author's contribution

The author is the primary author in Publications I-IV, which are based on original ideas of Artto Aurola. In these publications, the author performed 2D and 3D process and device simulations of novel semiconductor radiation detector structures. Besides that, the author has also contributed to the designs of novel detector structures by extensive discussions of results, suggestions on design improvements, literature review, and in case of Modified Internal Gate Field Effect Transistor (MIGFET) pixel design (Publication I) discussions with actual manufactures in order to make the detector design compatible with a real semiconductor process flow.

Nomenclature

Variables and constants

C_{ox}	gate capacitance	F
f	frequency	Hz
Δf	noise bandwidth	Hz
G_0	peak power gain of the system	dB
$G(f)$	power gain of the system as a function of frequency	dB
k	Boltzmann constant	J/K
L	lengh of the transistor channel	m
N_{dark}	number of charge carriers in MIG due to thermal generation	pcs
N_{illum}	number of charge carriers in MIG due to illumination	pcs
N_{sat}	maximum number of charge carriers that fits in the MIG	pcs
N_{sig}	number of charge carriers in MIG	pcs
n_{sn}	shot noise in terms of number of charge carriers in MIG	pcs
P_{tn}	maximum power (available noise power)	W
R_{tg}	thermal generation rate	pcs/s
$S_f(f)$	noise power spectral density	V^2/Hz
$S_t(f)$	power spectral density	V^2/Hz
T	temperature	K
V_{sn}	shot noise voltage (rms)	V
V_{th}	threshold voltage	V
W	width of the transistor channel	m

Subscripts

illum	illumination
ox	oxide
sat	saturation
sig	signal
sn	shot noise
tg	thermal generation
th	thresholds

Abbreviations

2D	two dimensional
3D	three dimensional
3T	three transistor
4T	four transistor
BSI	backside illuminated
CCD	charge coupled device
CCG	charge conversion gain
CDS	correlated double sampling

CdTe	cadmium telluride
CdZnTe	cadmium zinc telluride
CMOS	complementary metal oxide semiconductor
CsI	cesium iodide
CT	cross-talk
DEPFET	depleted p-channel field-effect transistor
EGRC	external gate readout configuration
FF	fill factor
FWC	full well capacity
FWHM	full width at half maximum
Ge	germanium
HgI_2	mercuric iodide
IG	internal gate
IGRC	internal gate readout configuration
ITO	indium tin oxide
JFET	junction field effect transistor
MIG	modified internal gate
MIGFET	modified internal gate field effect transistor
MOS	metal oxide semiconductor
NDCDSFWC	non-destructive correlated double sampling full well capacity
NDCDSR	non-destructive correlated double sampling readout
NIR	near infra-red
PSD	power spectral density
PVDD	pixelated vertical drift detector
QE	quantum efficiency
RTS	random telegraph signal
SDD	silicon drift detector
SF	source follower
Si	silicon
SiO_2	silicon dioxide
SNR	signal-to-noise ratio
TCAD	technology computer aided design
UV	ultraviolet
XFEL	X-ray free electron laser

1 Introduction

Radiation is all around us and most of the time we are not able to see it, nevertheless it brings us valuable information about the world we live in, so it is very important to be able to detect it with high accuracy. Radiation generally means the emission or transmission of energy in the form of waves or particles through space or through a material medium. The are several types of radiation which include:

- electromagnetic radiation, which includes radio waves, infrared light, visible light, ultraviolet light, x-rays, and gamma radiation (γ)
- particle radiation, which includes alpha radiation (α), beta radiation (β), and neutron radiation
- acoustic radiation
- gravitational radiation

When it comes to electromagnetic radiation, the radiation is detected through its interaction with matter. The following working principle is applicable to all radiation detectors. Photons interact with the detecting medium, the interaction is then transformed into signals, which are read out and usually recorded (Leroy and Rancoita, 2015).

The most suited detectors for detection of photons are made from semiconductor material, in particular silicon. Excellent intrinsic properties of these materials make it possible to combine precise position, time and energy measurements in well thought out detector concepts (Lutz, 2011).

The detecting media to be used for electromagnetic radiation detection has to be carefully selected depending on the radiation energy, taking into account that the thickness of a semiconductor radiation detector has certain limits.

Development and large scale use of silicon detectors has been initiated originally by particle physics where very good position measurement (in the range of several μm) and high rate capability (few hundreds kHZ) were required and could not be achieved by gas detectors available at that time. It was realized then that semiconductors offer the required capabilities and silicon strip detectors were developed. This development then rapidly increased so that today silicon strip detectors are used in many fields of science. Important features of this development were the introduction of more sophisticated detector concepts and the development of multi-channel low noise low power integrated readout electronics adapted to the requirements of strip detectors.

Another challenge in particle tracking was ambiguities occurring in case of high particle densities. This issue was dealt with by replacing the strip geometry by pixels. Hybrid pixel detectors became possible with the progress in miniaturization of electronics. Each pixel has its own readout channel. Detector and electronics with matched geometry are

connected face to face by bump bonding (Lutz, 2011). Integration of semiconductor detector with electronics was a big step in detector development history.

When the sufficient read out speed was achieved it made possible detection with high energy resolution, sometimes in combination with good position resolution. This development opened the door for semiconductor detectors in X-ray astronomy, synchrotron radiation experiments and in other fields.

A major step on this way was the invention of the semiconductor drift chamber by E. Gatti and P. Rehak (Gatti and Rehak, 1985, Gatti et. al., 1984 and Gatti et. al., 1985). This concept also became the basis for further new concepts such as the pnCCD (Strüder et. al., 1990, Bräuninger et. al., 1993 and Strüder et. al., 1997), the Silicon drift detector (Kemmer and Lutz, 1987) and the DEPFET (Kemmer and Lutz, 1987) that forms the basis for several types of pixel detectors with rather unique properties.

Since then, radiation detectors have been evolving as new technologies were becoming available, as a result, more and more sophisticated detectors and systems of detectors were made available.

Nowadays, semiconductor detectors are used in a large variety of fields: science, including nuclear physics, elementary particle physics, optical and x-ray astronomy, materials testing, medicine, image sensors, technology and consumer applications. The number of applications grows continually.

The success of semiconductor detectors is based on several unique properties that are not available with other types of detectors like for example gas detectors (Lutz, 2007). For example, because densities of solids are approximately 1000 times higher than those of gases, detector dimensions can be kept much smaller than the equivalent gas-filled detector for the measurement of high-energy electrons or gamma rays. The use of semiconductor materials as a radiation detection medium also results in a “much larger number of carriers for a given incident radiation event than is possible with any other common detector type” (Knoll, 2010). “The best energy resolution from radiation spectrometers in routine use is achieved using semiconductor detectors” (Knoll, 2010).

Examples of the unique properties of semiconductor materials according to (Tsoulfanidis and Landsberger, 2015) and (Lutz, 2007):

- the combination of precise position measurement and high readout speed;
- direct availability of signals in electronic form;
- the simultaneous precise measurement of energy and position;
- the possibility of integrating detector and readout electronics on a common substrate;
- the ability to resolve the energy of particles out of a polyenergetic energy spectrum;

- linear response (pulse height versus particle energy) over a wide energy range;
- detector dimensions can be kept much smaller than those of the equivalent gas-filled detector, because solid densities are approximately 1000 times higher than those of gases;
- possibility for special geometric configurations;
- fast pulse rise time (relative to gas-filled detectors);
- ability to operate in vacuum;
- insensitivity to magnetic fields;

The characteristics of a semiconductor detector depend not only on the type of material used - for example, silicon or germanium - but also on the way the semiconductor was made, shaped, and treated. The type, size, shape, and treatment of the crystal play a role in the operation and performance of a semiconductor detector.

Despite of excellent characteristics, there are some drawbacks of using semiconductor materials as detection medium. One of them is the limitation to small sizes and another one is the relatively high susceptibility of semiconductor detectors to performance degradation from radiation-induced damage (Knoll, 2010). The incoming radiation may inflict temporary or permanent damage to the detector material and readout electronics (Lutz, 2007).

At present, the most successful semiconductor detectors are made of silicon and germanium. However, starting in the 1990s, different materials have been tried, some with very good successes, for example, cadmium telluride (CdTe), cadmium zinc telluride (CdZnTe), often named CZT, cesium iodide (CsI), mercuric iodide (HgI2), and others (Tsoulfanidis and Landsberger, 2015).

Nowadays, newly constructed particle colliders may require tens of thousands of detectors to be used in the harsh radiation environment. “The production of this large number of detectors requires a simple design that can be produced economically and that can nevertheless cope with the drastic radiation-induced changes to material properties” (Lutz, 2007). A simple design, easier manufacturing, improved performance characteristics and in some cases better radiation tolerance of radiation detectors will benefit all of the fields where they are used.

2 Operational principle of solid state photon detectors

Photons are detected through their interaction with matter. The following working principle is applicable to every photon detector: photons interact with the detecting medium, the interaction is then transformed into signals, which are read out and usually recorded (Leroy and Rancoita, 2015).

The most suited detectors for detection of photons are made out of semiconductor material, in particular silicon. “Excellent intrinsic properties of these materials make it possible to combine precise position, time and energy measurements in well thought out detector concepts” (Lutz, 2011).

When a photon interacts with silicon it creates electron-hole pairs, the amount of which is dependent on photon energy. “The energy required to create an electron-hole pair in silicon is 3.6 eV. The band gap of silicon is 1.12 eV at room temperature and the average energy needed to create a single pair, called the radiation ionization energy, is empirically found to be about three times the band gap energy of the semiconductor. This is due to the phonon excitation, which is required for momentum conservation” (Luukka, 2006). Generated electrons or holes are then called signal charges which are then read out and stored. Based on the amount of signal charges the light intensity and/or photon energy can then be obtained and the penetration position of a photon is then obtained with the help of detector’s architecture.

2.1 Silicon Drift Detector

The Silicon Drift Detector (SDD) was introduced in 1984 by E. Gatti and P. Rehak, in a paper which presented the concept and experimental results (Gatti and Rehak, 1984).

SDDs have replaced simple diodes in demanding X-ray fluorescence applications like in element analysers capable of detecting light elements. The reason for this is that with similar collection area the SDDs have a much smaller output capacitance than diodes due to a much smaller anode size. Thus the SDDs provide much better Signal to Noise Ratio (SNR) at smaller signal levels than diodes. The small capacitance in SDDs is achieved by placing concentric rings around a miniature sized anode as shown in Figure 2.1a. These rings are biased such (Lechner et. al., 1996) that inside the SDD’s fully depleted bulk a radial electric field component is established guiding signal charges towards the anode.

Nowadays SDDs are used in large quantities on industrial scale in applications like electron microscopy (SEM-EDX) and X-ray fluorescence analysis (XRF). A low leakage current level allows to operate them close to room temperature with moderate cooling (PNSensor). An example of a typical SDD device is shown in Figure 2.1b.

The backside of the SDD serves as a radiation entrance window which is made up by a non-structured shallow implanted junction giving a homogeneous sensitivity over the whole detector area.

In contrast with old SDDs, newer designs integrate the front-end transistor of the amplifying electronics, which is usually a field effect transistor (FET), on the detector chip and connects it to the collecting anode by a short metal strip. This reduces the capacitance between anode and FET, which in turn reduces electronic noise.

"Due to the elaborated process technology used in the SDD fabrication the leakage current level is so low that the SDD can be operated with moderate cooling by means of a single stage Peltier element" (PNSensor).

(a) (b)

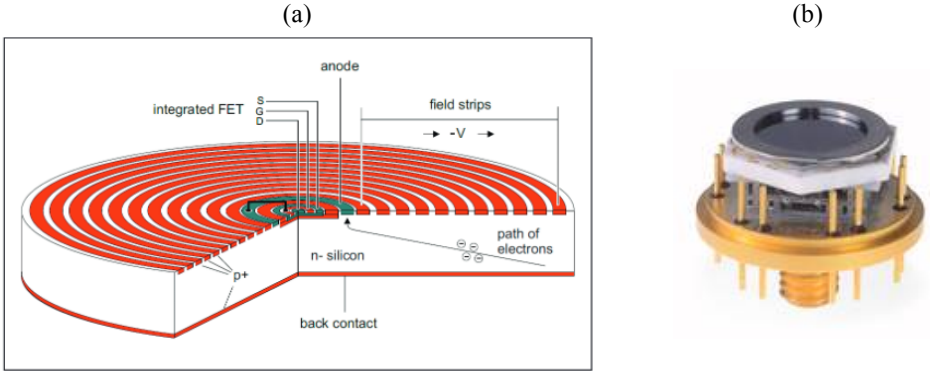

Figure 2.1: (a) Silicon drift detector example design (PNSensor), (b) a typical SDD device, the chip is mounted on a thermoelectric cooler which provides device cooling (http://www.ketek.net/products/vitus-sdd/vitus-r100/).

2.2 Modified Internal Gate Field Effect Transistor (MIGFET) pixel

The MIGFET structure was first patented by Artto Aurola in 2005 (Aurola, 2005a) and is based on the idea of MOSFET which has a buried internal gate (MIG) implanted directly underneath its conducting channel. Later the concept of a thick fully depleted BSI double MIGFET pixel was developed (Publication I) providing the possibility of a non-destructive correlated double sampling readout. The detector concept is well suited for Low-light imaging, X-ray spectroscopy, synchrotron and X-ray Free Electron Laser (XFEL) facilities. The front side view and the cross section of the developed double MIGFET pixel structure is presented in Figure 2.2.

Both MIGFETs in the pixel have a buried internal gate (MIG) implanted directly underneath their conducting channels. MIGs are used to store radiation induced signal charges (electrons in N-type device and holes in P-type device). In a double MIGFET pixel arrangement the signal charge can be transferred back and forth between the two MIGs of the pixel, which enables Non-Destructive Correlated Double Sampling Readout (NDCDSR). In between the MIG and the channel of the FET there is a depleted semiconductor material forming a potential barrier between charges in the channel and similar type signal charges located in the MIG. The signal charges in the MIG have a

measurable effect on the conductance of the channel. The channel conductivity is easy to measure and from it one can determine the charge in MIG.

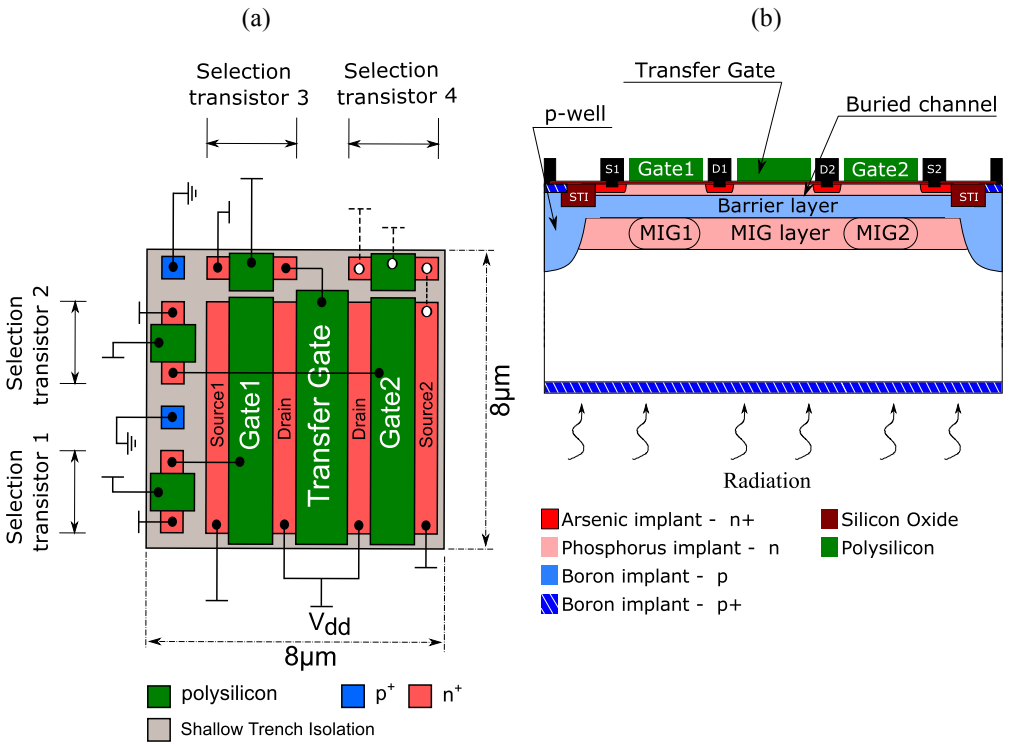

Figure 2.2: (a) Front side view of the Double MIGFET Detector wherein the four small transistors are optional selection transistors which can be utilised e.g. in order to create pixel specific reset. (b) Cross-section of the Double MIGFET Detector.

The potential barrier between the channel and the MIG prevents the mixing of signal charges with interface-generated charges meaning that a MIG sensor does not suffer from interface generated dark noise, which has been verified by 3D simulations in Publication I. Similarly, this potential barrier separates also the signal charges from the interface during signal charge transfer (transfer is required in NDCDSR). Thus the MIG image sensor is not prone to image lag. The potential barrier enables vertical anti-blooming, i.e., when the MIG starts to be full of signal charges then the excess charges will flow over the potential barrier to the drain preventing the signal charges from spreading into neighbouring pixels.

In general, the pixel operates in three steps. The first step is the reset of the pixel, when all charge present in the pixel is removed. The second step is integration: photons penetrate the pixel from the backside and generate electron-hole pairs, signal charges (for

example electrons in case of the structure in Figure 2.2) are collected in MIGs and minor charges (holes) are removed through the backside p+ layer. The third step is the non-destructive CDS procedure comprising non-destructive charge transfer from one MIG to another in between non-destructive readouts.

2.3 Three-dimensional (3D) semiconductor detectors

In order to provide high quantum efficiency for high energy X-rays and gamma-rays the radiation detectors should be as thick as possible. The maximum thickness and thus the maximum quantum efficiency of planar radiation detectors has been limited by the substrate doping concentration: the lower the substrate doping the thicker the detector can be before reaching the semiconductor material's electric breakdown field. Thick direct conversion three-dimensional (3D) semiconductor detectors comprising vertical three-dimensional electrodes protruding vertically through the substrate have been proposed (Parker, 1997) and further developed (Parker, 1999, Parker et. al., 2001, Parker et. al., 2011) by Sherwood Parker in order to promote rapid detection of radiation. An additional advantage of these detectors is that their thickness is not limited by the substrate doping, i.e., the maximum electric field value in the detector does not depend on detector thickness.

In standard planar sensors (Figure 2.3 bottom right), the electrodes are implanted on the top and bottom surfaces of the wafer, so that the depletion region grows vertically and the full depletion voltage depends on the substrate thickness. On the contrary, in 3D sensors (Figure 2.3 top and bottom left) the electrode distance and the substrate thickness can be decoupled: the depletion region grows laterally between the electrodes, whose distance is much smaller than the substrate thickness (Lange, 2015). This leads to a lower depletion voltage and a smaller drift distance, resulting in faster charge collection and thus less trapping at radiation-induced defects. At the same time, the sensor thickness can be kept at moderate values to allow sufficient charge deposition by ionising particles. As a result, the signal is still large at moderate voltages after heavy irradiation, making this technology very radiation-hard. Another advantage is that active or slim edges are a natural feature of the 3D technology, allowing to highly reduce the insensitive detector edge (Da Via et. al., 2012). Furthermore, photon absorption induced charge sharing between multiple pixels takes place only if the photon is initially absorbed at the pixel boundary, i.e., the charge sharing is independent of the 3D detector thickness. The reason for this is that the horizontal electric field effectively transports the signal charges towards a single electrode providing thus charge confinement and preventing horizontal charge spreading.

A photograph of a 177 µm thick 3D active-edge sensor having hexagonal cells with 50 µm long hexagon sides is presented in Figure 2.4 a and b.

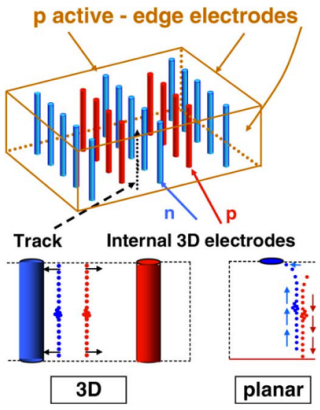

Figure 2.3: (top) Schematic diagram of 3D sensor with normally-incident track. (bottom) Schematic detail of tracks with an ionization cluster. Electrons drift to the left in the 3D sensor in the left diagram and up in the planar diagram on the right (Parker et. al., 2011).

(a) (b)

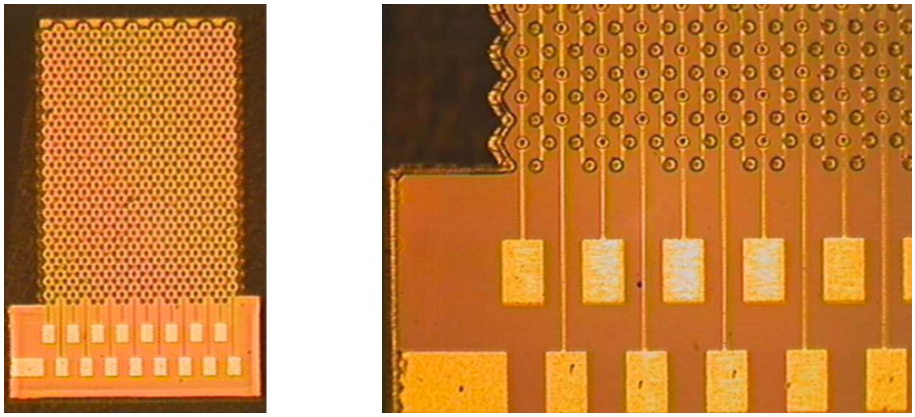

Figure 2.4: (a) 3D hexagon-cell active edge sensor tiled with 16 columns, each with 20 hexagons with sides of 50 µm connected to the 16 pads at the bottom. (b) Output pad end of 3D active-edge hexagon sensor. (Parker et. al., 2011).

3 Challenges in solid state photon detectors

3.1 Challenges in Silicon Drift Detectors

There are two basic problems related to the drift detectors which are the interface generated dark noise and positive oxide charge. Both of these problems can be removed with the SDD of Figure 3.1 wherein a resistor chain arrangement is utilized for biasing the p+ drift rings and intermediate n+ rings. This biasing configuration ensures that the n+ rings are always reverse biased when compared to the neighbouring p+ rings. The n+ rings collect the interface generated electrons. The proper biasing of the n+ rings prevents electron injection from the n+ rings into the substrate as well as hole current flow from one p+ ring to another. The latter feature ensures proper operation of the resistor chain and the former one prevents the formation of interface generated dark noise. Important design aspects are the separation of the p+ rings, the size of the n+ ring, the voltage drop across individual resistors, the resistivity of the substrate, and to some extent also the amount of positive oxide charge. Particularly, a relatively large reverse bias must be applied between the n+ and the neighbouring p+ rings in order to prevent electron flow from the n+ ring to the substrate as well as hole flow from one p+ ring to another.

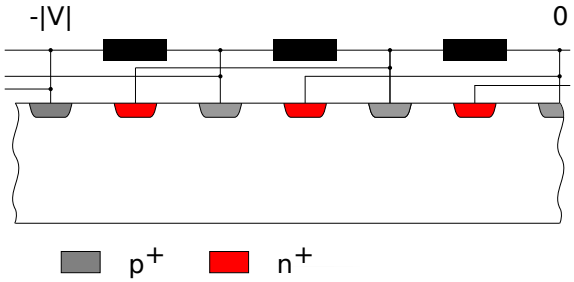

Figure 3.1: A typical SDD ring arrangement utilizing a resistor chain for the biasing of the p+ and n+ rings. The p+ rings act as drift rings and collect interface generated and radiation-induced holes. The purpose of the n+ rings is to collect interface generated electrons.

In addition, in the SDD of Figure 3.1 it is important to utilize a large enough reverse bias between the innermost p+ ring and the n+ anode for three different reasons. Firstly, it is important to prevent punch-through hole current flow from the innermost p+ rings to a backside p+ layer. Secondly, it is important to avoid radiation-induced electrons being absorbed by the innermost n+ rings. Thirdly, the relatively high reverse bias between the n+ and p+ rings results in an undulating potential profile reaching relatively deep inside the substrate causing problems close to anode where radiation- induced electrons are transported relatively close to the front surface. With the aid of a large enough reverse bias between the anode and the innermost p+ ring the radiation induced electrons can be pushed next to the anode deeper into the substrate wherein the undulating potential profile has no effect.

Another procedure to mitigate problems related to undulating potential profile next to anode is to utilize a larger drift field (i.e. higher potential difference between adjacent p+ rings) close to the anode than in areas located further away from the anode. Directly beneath the anode the high reverse bias between the innermost p+ ring and the anode complicates the vertical transport of the radiation-induced electrons towards the anode, which can be overcome by providing a large enough anode.

The relatively high reverse bias between the p+ and n+ rings means that the dead volume, i.e. the region from which the n+ rings collect radiation induced electrons, extends relatively deep into the high resistivity substrate (roughly to the width of the n+ ring) resulting in the formation of a relatively large low drift field region at the border of the dead volume underneath the n+ rings. This fact increases the number of split events enlarging somewhat the Full Width at Half Maximum (FWHM) of the X-ray peaks except for low energy X-rays. In a split-event an X-ray is absorbed in the low drift field region and part of the X-ray induced electrons are collected by an n+ ring and another part by the anode. Before the introduction of the large area radiation entry window on the backside (Kemmer et. al., 1987) the relatively large low drift field region at the front side corresponding to gaps in the p+ doping used to increase somewhat also the FWHM of higher energy X-ray peaks besides severely impairing the FWHM of low energy X-ray peaks.

By reducing the separation between the p+ rings problems related to the undulating potential profile and the dead volume could be mitigated. This means, however, that inside the substrate there is a higher risk for punch-through current flow from one p+ ring to another unless reasonably high reverse bias is applied between the n+ ring and the neighbouring p+ rings. On the other hand, in case the separation between the p+ rings are reduced the width of the n+ rings should be also diminished but this is challenging from the manufacturing point of view in case contact aligner is utilized in the manufacturing process.

A fact is that the X-rays and high-energy particles increase the amount of positive oxide charge. The bigger the amount of positive oxide charge is and the larger the reverse biases between the n+ and p+ rings as well as between the anode and the innermost p+ ring are, the larger is the maximum electric field value at the interface. If the maximum electric field at the interface exceeds a certain manufacturing process dependent limit then avalanche breakdown follows limiting the lifetime of the detector. Thus the SDD structure of Figure 3.1 needs to be designed and manufactured carefully in order to guarantee long lifetime in X-ray and/or particle detection applications. One way to reduce the effect of the build-up of positive oxide charge is to utilize a large area p spray implant on the front side of the SDD.

In the SDD of Figure 3.1 an extra process step is required for the realization of the resistor chain that may not be standardly available in the manufacturing facility. The resistor chain (as well as the n+ rings) can be avoided in the SDD of (Chen et. al., 1992) wherein the p+ drift rings comprise gaps as depicted in Figure 9 in (Chen et. al., 1992). The positive

oxide charge in these gaps enables the formation of electron “rivers” next to the interface, i.e., due to the positive oxide charge there is a potential minimum for electrons at the oxide interface in the gaps of the p+ drift rings as well as in areas between adjacent p+ drift rings. The gap in the p+ drift ring allows interface generated electrons to move in these electron “rivers” towards an additional anode situated in between the two innermost p+ drift rings (the innermost p+ drift ring does not comprise a gap). The additional anode collects all interface-generated electrons except the ones generated between the anode and the innermost p+ drift ring reducing thus significantly the interface generated dark noise.

The interface and part of bulk generated holes are collected by the p+ rings and are transported from one p+ ring to another towards the outermost p+ ring in electron potential barriers located underneath the space in between adjacent p+ rings, i.e., the punch-through effect between the p+ drift rings can be exploited in a structure with a resistor chain. The formation of aforesaid electron potential barriers depends on the amount of positive oxide charge, on the separation between the p+ drift rings, and on substrate doping concentration. As already previously explained the barriers prevent also interface-generated electrons from flowing into the substrate if they can be removed e.g. with aforesaid “electron river” approach.

The benefits of the SDD design of (Chen et. al., 1992) are that no resistor chain is required, that the dead volume is smaller, and that the undulating potential profile underneath the rings is less severe than in the case of the structure presented in Figure 3.1. The design of (Chen et. al., 1992) is, however, highly dependent on the amount of positive oxide charge in the gaps piercing the p+ drift rings and in between the p+ drift rings. This is likely to complicate the manufacturing, to lower the yield, and to reduce the effective lifetime of the detector.

Instead of using gaps in the p+ rings one could alternatively use a p doped spiral wherein the p spiral itself acts as a resistor providing thus a potential gradient inside the p ring and consequently also outside the p spiral. In this design the interface generated electrons are flowing at the interface next to the p spiral towards an additional anode collecting interface-generated electrons. The benefit of the design is that the resistor chain is avoided but on the other hand the design is very much dependent on the amount of positive oxide charge at the interface next to the p spiral. Consequently, further away from the anode the radiation-induced electrons would flow radially towards the anode but close to the anode, depending on the amount of positive oxide charge, the radiation-induced electrons would be prone to follow a spiral path. Since the build-up of positive charge during manufacturing and in use cannot be well controlled and since this spiral device is highly dependent on positive oxide charge the design is likely to have manufacturing issues, low yield, and reduced lifetime.

3.2 Challenges in pixelated CMOS and CCD radiation detectors

It is generally known that gamma rays, X-rays, and electrons with energies below the minimum threshold for bulk defects (≈ 300 keV) generate only defects in the dielectrics, at the dielectric silicon interface, and the interface between dielectrics (Zhang, 2013). The build-up of the interface damage increases dark current generation from depleted interfaces. If the interface-generated dark current can mix with the signal charges the build-up of the interface damage will increase the dark noise and thereby reduce the Signal to Noise Ratio (SNR) as well as the useful lifetime of the detector and particularly so in X-ray (and/or electron) detection applications or imaging applications utilized in radioactive environments. The radiation-induced interface damage also affects the read noise in surface channel or shallow buried channel devices since it increases the amount of interface defects and thereby interface generated 1/*f* and RTS noise.

Besides having low dark and read noise it is important for X-ray detectors and for silicon Near Infra-Red (NIR) optimised image sensors to have a thick fully depleted Back-Side Illuminated (BSI) design. The full depletion is important in order to ensure that no charge is lost due to recombination and in order to minimize crosstalk by preventing diffusion. BSI is required in order to provide a thin homogeneous radiation entry window, which enables 100% fill factor and the detection of very low energy X-ray photons. A thick detector, on the other hand, improves the Quantum Efficiency (QE) for NIR light and higher energy X-rays (important e.g. in X-ray fluorescence spectroscopy).

There are currently a number of pixelated detector architectures, which are described in more detail below. None of them offer, however, the combination of very low noise, low crosstalk, high QE for NIR light and X-rays, as well as durability against radiation damage. The reason for this is that a thick fully depleted BSI detector having very low read noise and being free of interface generated dark noise has not been realised so far. There are fully depleted backside illuminated Charge Coupled Devices (CCDs) utilising a regular gate architecture (Holland et. al., 2009 and Holland et. al., 2014) and CCDs (Granato et. al., 2013) utilising a pn gate architecture (the original pn gate CCD architecture was introduced in (Krambeck et. al., 1973)) enabling relatively low read noise. In thick fully depleted BSI CCDs interline transfer architecture is not feasible and thus the only options are full frame and frame transfer architectures. In case reasonable frame rate (e.g. video rate) is desired then the frame transfer architecture is the only option. The problem with frame transfer architecture is that it suffers from smear (Cai-qin and Zhong-bin, 2009) even though it is less prone to it than full frame architecture. The problem at least with architecture (Holland et. al., 2009 and Holland et. al., 2014) is also that it suffers from interface generated dark noise during the charge transfer period.

Thick fully depleted BSI pixels can be realised also with simple pin (p type, intrinsic, n type) pixels wherein an n^+ collection node is connected either to a hybridized readout chip or to pixel specific integrated readout circuitry. Both of them are typically realized with a three transistor (3T) Complementary Metal Oxide Semiconductor (CMOS) pixel architecture but the 3T pixel architecture suffers from interface generated dark noise and

high read noise (Seitz and Theuwissen, 2011 and Janesick et. al., 2006). The pinned photo-diode structure (Seitz and Theuwissen, 2011 and Fossum and Hondongwa, 2014) utilised in 4T CMOS pixels enables BSI configuration as well as more or less complete removal of the interface generated dark noise (Seitz and Theuwissen, 2011) (Janesick et. al., 2006). Thick fully depleted 4T pixels are, however, notoriously difficult to realise — the authors of Publication I are not aware of any being realised so far.

Another problem in CCDs and CMOS image sensor technologies is that they utilise a readout configuration which is hereby referred to as External Gate Readout Configuration (EGRC) since the signal charge is brought to a MOS gate of a readout transistor, i.e., the gate is not located inside the semiconductor substrate but on top of it. A formidable problem in EGRC is that in Correlated Double Sampling (CDS) readout procedure (which is a mandatory requirement for accurate measurements) the signal charge is destroyed when it is brought to the external gate. This means that the signal charge can be read out accurately only once and thus one cannot mitigate the read noise by performing multiple readouts. It is important to note that the read noise can be removed by signal amplification but on the other hand the amplification process itself increases considerably the noise manifested by excess noise factor (Seitz and Theuwissen, 2011 and Michalet et. al., 2007).

A disadvantage of EGRC is also that the effect of $1/f$ and RTS noise on the read noise and thus on SNR is difficult to mitigate. By far the major part of the $1/f$ and RTS noise stems from the interface and thus by utilizing a buried channel readout transistor (Wang, 2008) the $1/f$ and RTS noise can be reduced — the deeper the channel the smaller the $1/f$ and RTS noise. However, the deeper the buried channel in EGRC the smaller the signal and the available voltage swing. Another problem is also that in EGRC the spurious signal due to a charge trapped at the semiconductor interface beneath the gate is always larger than the signal produced by a signal charge on the sense node and the deeper the buried channel the larger this difference is. A third reason is that the smaller the amount of signal charges the shallower the buried channel is, meaning that the smaller the signal is the more there will be $1/f$ and RTS noise. This effect results in also non-linearity issues. These reasons reduce the beneficial effect of a deep buried channel on SNR in EGRC. One could also remove the interface generated $1/f$ and RTS noise in EGRC by utilising a JFET type diffusion gate instead of the MOS gate but this reduces considerably the available voltage swing and signal size as well as increases the depleted interface area next to doping belonging to the sense node. The latter fact increases the dark current generation rate at the sense node necessitating faster readout.

It is possible to reduce the read noise without introducing additional noise through NDCDSR, i.e., through accurate non-destructive signal readout. The NDCDSR has been demonstrated in DEPFET, a pixel with an Internal Gate Readout Configuration (IGRC) (Wölfel, 2007) (the initial IG readout architecture was introduced in (Brewer, 1978). The problem is, however, the very large and unpractical pixel size as well as manufacturability issues. The latter fact stems from the fact that in IGRC signal charges modulate an oppositely charged current running in the transistor channel, which is next briefly

explained. Let us assume that there is a fully depleted n doped Internal Gate (IG) collecting signal charges beneath a hole surface channel that is closed for the time being. Next let us assume that the n doping of the IG is larger at a certain location which means that at this location there are more positively charged dopant atoms beneath the channel increasing the potential at the IG and at the interface above, i.e. the IG at this location will be more attractive for signal electrons but it will be more difficult to open the hole channel at this location than at other locations. This means that it is very difficult to match the location of the minimum channel threshold of the readout transistor with the signal charge potential minimum leading to poor tolerance against process fluctuations.

In the IGRC of (Wölfel, 2007 and Tournier et. al., 2008) a surface channel readout transistor is utilized resulting in a high level of 1/*f* and RTS noise (Wang, 2008). The high 1/*f* and RTS noise means that a considerable amount of NDCDS measurements need to be performed in order to reduce the 1/*f* and RTS noise to a negligible level. The problem is that generally in IGRC a circular readout transistor is more or less mandatory in order to improve the manufacturability but the circular readout transistor inhibits the use of a deep buried channel. One could also reduce 1/*f* and RTS noise by utilizing a circular JFET in conjunction with the IGRC, but it would have a negative impact on the manufacturability.

3.3 Thickness limitation of planar semiconductor radiation detectors

The benefits of pixelated planar direct conversion semiconductor radiation detectors comprising a thick fully depleted substrate are that they offer low crosstalk, small output capacitance, and that the planar configuration simplifies manufacturing. In order to provide high quantum efficiency for high energy X-rays and gamma-rays such a radiation detector should be as thick as possible.

The maximum thickness of the depleted bulk in planar semiconductor radiation detectors is determined by the electric break down field and by the substrate doping concentration. This means that the planar semiconductor detectors have an upper detection efficiency limit for deeply penetrating radiation unless multiple fully depleted planar detectors are placed on top of each other. Another option to improve the detection efficiency of planar detectors would be to utilize multiple detectors and to point the detector edges towards the radiation source, which is, however, not a truly optimal arrangement unless the radiation is unidirectional. Furthermore, a problem in thick planar detectors is horizontal spreading of the signal charge, which increases the crosstalk and hampers spatial resolution unless the detector is operated in photon counting mode (Dinapoli et. al., 2011) and charge sharing is taken into (Hamann et. al., 2015 and Koenig et. al., 2013) account.

In a planar semiconductor radiation detector the maximum absolute value of the electric field, which should be always substantially smaller than the absolute value of the electric break down field, is present at a pn junction located in the vicinity of either surface. The depletion of the bulk semiconductor material is provided by the vertical electric field component, which absolute value decays along the vertical direction pointing towards the

inside of the bulk. If the semiconductor bulk is homogeneously doped then the absolute value of the vertical electric field component drops linearly in the vertical direction towards the interior of the bulk. In thick pixelated planar detectors there is essentially no horizontal field component except in the proximity of the surface. This means that the radiation induced charge cloud is not confined in the horizontal direction and thus it expands due to electric repulsion and random scattering events so that the charge may be shared amongst several pixels.

In Silicon Drift Detectors (SDDs) (Chen et. al., 1992, Publication II and Schlosser et. al., 2010), which are planar detectors, there is a horizontal electric field component present inside the bulk which is not responsible for depleting the detector but instead it acts as a drift field transporting signal charges towards a charge-collecting anode. In SDD the vertical electric field is responsible for the depletion of the detector and detector thickness is similarly limited by the electric breakdown field and the substrate doping concentration. In pixelated SDDs the horizontal drift field can be used for providing charge confinement in horizontal direction but the pixel aspect ratio (i.e. depth to pixel pitch ratio) cannot be very high since in high aspect ratio pixels the absolute value of the horizontal electric field component decays strongly towards the interior of the bulk.

In thick pixelated SDDs comprising high aspect ratio pixels the problem of the decaying horizontal electric field component could be somewhat relaxed if one could provide on both sides of the detector corresponding concentric SDD ring structures — this type of a detector is later on referred to as double-sided SDD. The difference in the SDD ring structure on the radiation entry side would be only that the charge collecting contact was replaced by an opposite type of doping. If the double-sided SDD pixel had n- bulk and p+ rings then the potential of the p+ rings on the radiation entry side would be shifted by a constant negative value when compared to corresponding rings on the opposite side in order to provide the necessary vertical drift field. Even in the double-sided SDD the pixel aspect ratio would need to be relatively small in order to withstand the effect of the decaying horizontal field since in high aspect ratio double-sided SDD pixels the lack of charge confining horizontal electric field in the central part of the pixel would anyhow cause horizontal charge spreading.

3.4 Challenges in thick 3D detectors

The aforesaid problems of planar detectors mentioned in section 3.3 can be avoided with three-dimensional (3D) semiconductor detectors (Parker, 1999, Parker et. al., 2001 and Parker et. al., 2011), and (Conder and Young, 1999) comprising 3D electrodes penetrating vertically through a semiconductor substrate. In (Conder and Young, 1999) a 3D Charge Coupled Device (CCD) is presented comprising 3D electrodes that are insulated from the substrate by an insulator layer. In (Parker, 1999), (Parker et. al., 2001) and (Parker et. al., 2011) which are referred to as conventional 3D detectors in this work a 3D detector is presented comprising highly doped n+ and p+ type 3D electrodes. The operational

principle and benefits of using conventional 3D detectors in high energy X-ray and gamma-ray applications are explained in Section 2.3.

The problem associated with the conventional 3D detector concept is, however, that in a thick detector the capacitance of the signal charge collecting 3D electrodes is relatively high due to the large surface area of the 3D electrodes and due to the small distance between the 3D electrodes. This means that the thicker the conventional 3D detector is the larger is the capacitance and the poorer is the energy resolution of the detector. In (Pennicard et. al., 2010) and (Raighne et. al., 2011) 3D detectors have been tested in X-ray detection and imaging confirming low charge sharing properties but also highlighting problems with non-uniform spatial response and geometrical inefficiencies. The problem of the 3D CCD is that the signal charge needs to be transported through the substrate multiple times from one 3D electrode to another. This means that in 3D CCD significant signal charge trapping tendency is resulted in by interface defects located at the semiconductor and insulator interface of the 3D electrodes.

3.5 Challenges related to sawed edges of the detector chips

In pixelated silicon radiation detectors that are utilized for the detection of UV, visible, and Near Infra-Red (NIR) light it is desirable to utilize a relatively thick fully depleted Back-Side Illuminated (BSI) detector design. The benefit of the BSI configuration is that structures on the front side such as conductors do not absorb light thus enabling 100 % Fill Factor (FF). The advantages of the fully depleted configuration are considerably reduced Cross-Talk (CT) due to lack of diffusion and improved Quantum Efficiency (QE) due to lack of recombination.

The thicker the fully depleted detector the better is the QE for NIR light. However, the thicker the fully depleted detector the more dark current is generated in the depleted bulk (which can be, however, mitigated by cooling), the higher bias at a conductive backside layer is required to fully deplete the bulk, and the bigger is the CT particularly at the boundary of the pixel matrix. Thus there is an optimal detector thickness depending mainly on the optics, the magnitude of the bias on the conductive backside layer, and the pixel size.

In case the detectors should be thinner than 300 µm it is more or less mandatory to make thinner the detector wafer from the backside after the front side of the detector has been processed and before the conductive layer is formed on the backside. One option is to bond the front side of the detector wafer to a support wafer. The problem is, however, that it is not trivial to reach the contact pads located on the front side of the detector wafer especially if the detector is thicker than 40 µm. This problem can be avoided in TAIKO thinning process since no support wafer is required but the detector thickness must be at least 40 µm. The TAIKO process is a wafer back grinding method developed by DISCO. The difference to conventional back grinding is that the TAIKO process leaves an edge (approximately 3 mm) on the outer most circumference of the wafer and grinds only the inner circumference. The TAIKO process has, however, the problem that lithographic

steps cannot be performed on the backside of the detector wafer. This means that the conductive backside layer must be homogenous throughout the wafer and that the contact to the conducting backside layer needs to be placed on the front side of the detector.

In order to provide good QE for blue and UV light the conductive backside layer should be as thin as possible and it should be of opposite doping type than the substrate (an inversion layer is generally not an option due to the relatively thick fully depleted substrate). Beside the use of TAIKO process it is hereby assumed that the detector chips are separated from the wafer by sawing which is a standard procedure in chip manufacturing. The problem with afore described arrangement is that it is difficult to bias the conductive backside layer from the front side. Another problem is typically that high leakage current is generated at the sawed chip edge, which may increase the dark noise and the power consumption.

4 Simulation tools in development of novel radiation detectors

"Technology Computer Aided Design (TCAD) represents our physical understanding of processes and devices in terms of computer models of semiconductor physics" (Armstrong and Maiti, 2007). TCAD is used to design, analyse and optimise semiconductor technologies and devices with fundamental and accurate models. 2D and 3D process and device simulations in TCAD software models semiconductor fabrication and semiconductor device operation. Semiconductor fabrication is modelled through the semiconductor process flow simulation, which models manufacturing steps such as oxidation, implantation, diffusion, etching, deposition and lithography. Device simulation is used for obtaining the characteristics, for example, static, time-dependent, large and small-signal frequency-dependent behaviour of semiconductor devices and their electrical behaviour and also SPICE parameter extraction. Device simulation models the electrical, optical, mechanical and magnetic behaviour of semiconductor devices using structures obtained from process simulation (Armstrong and Maiti, 2007).

The evolution of TCAD started in the 1970s and one-dimensional (1D) simulations of IC processes and devices were adequately sufficient for technologies of the 1970s with deeper junction depths and channel lengths of several microns. Since then with increased complexity of integrated circuits and technologies TCAD tools evolved and offer nowadays a possibility to simulate 10nm node 3D complex semiconductor devices.

TCAD simulation is the essential part of the semiconductor device development since it brings a considerable reduction in technology development costs by reducing the number of experimental lots and shortening development time for the semiconductor industry. There is no need to run a real semiconductor process to test a new variation in a semiconductor process or device structure. Real wafer fabrication can be emulated by process simulation, from which realistic device structures and doping profiles can be generated, and transistor performance can be predicted through device simulation with a reasonable accuracy. Everything is done virtually on the computer and the structure parameters can be changed many times until the desired device performance is achieved. Simulation results of course don't guarantee a 100% correlation to the device which will come out from the manufacturing line but simulations are based on highly accurate physical models and with the input of the right parameters, represent a real device with high accuracy.

Process simulation starts with the blank wafer and ends with device which structural and doping profiles are calculated based on the provided semiconductor fabrication process flow details, like ion implantation doses and energies, temperatures and times for

annealing processes, parameters for etching and deposition etc.

Advanced multi-dimensional process and device simulation would naturally require models that are comprehensive and physically based. But since the physics of many of the processes is highly complicated this task is usually difficult to achieve. In this case, empirically based models are used, with parameters chosen that are related to experiment. Both complex and computationally intensive first-principle models, as well as simple and empirically based models, play important roles in the simulation of semiconductor-related phenomena. Empirically based models, although limited in scope, are attractive because they are less computationally intensive than first-principle models (Armstrong and Maiti, 2007).

Atomistic modelling approaches based on molecular dynamics, Monte Carlo and quantum chemistry have also been developed in the past decade (Hoekstra and Kushner, 1998) and are available in modern TCAD software.

One of the important aspects of the numerical simulation of semiconductor devices is that it provides insights into complex phenomena that cannot be obtained through experimentation or simple analytic models. “Most of the physics phenomena involved in semiconductor processes can be described by partial differential equations (PDEs) and as a result, much of the TCAD software is based on the solution of PDEs” (Armstrong and Maiti, 2007). However, except in the case of simple and geometrically well-defined problems, most of these equations are intractable, so approximate methods are inevitably utilized. The most common used methods for solving these equations numerically are based on finite differences, finite boxes, or finite elements. Finite element methods utilize an integral form and finite difference methods approximate the solution to the governing PDEs with difference operators.

There are several providers of TCAD software including Synopsys and Silvaco.

In this work Synopsys Sentaurus TCAD (Synopsys) has been used for 2D and 3D process and device simulations. The whole silicon device manufacturing process was simulated creating a virtual silicon device which performance has been then simulated and valuable characteristics obtained such as electrostatic potential distributions, electron and hole current distributions, electron and hole density distributions in the device etc. The device performance can be then judged based on these simulation results and if the device performance does not meet the requirements the process parameters (like wafer resistivity, device geometry, doping energies and doses etc.) can be changed and the simulation process repeats again until the device performance meets the expected requirements.

5 Development of novel photon detectors

5.1 Novel silicon drift detector design

The basic operational principle of a silicon drift detector (SDD) was explained in Section 2.1 and challenges in SDD detectors were explained in Section 3.1. Taking into account challenges in a modern SDDs a novel SDD design was developed improving detector's performance by preventing the formation of interface dark noise and making it resistant to positive oxide charge. The manufacturing process was also made easier eliminating the need of a resistor chain.

The novel SDD detector is well suited for X-ray spectrometry and Electron microscopy.

The cross-section of the SDD ring structure and anode of the proposed modified SDD structure is presented in Figure 5.1 excluding the edge area. The front side of the modified SDD comprising also a possible edge configuration and alternative edge and edgeless detector configurations are presented in Publication II. The way to avoid any edge generated dark noise is also presented in Publication II.

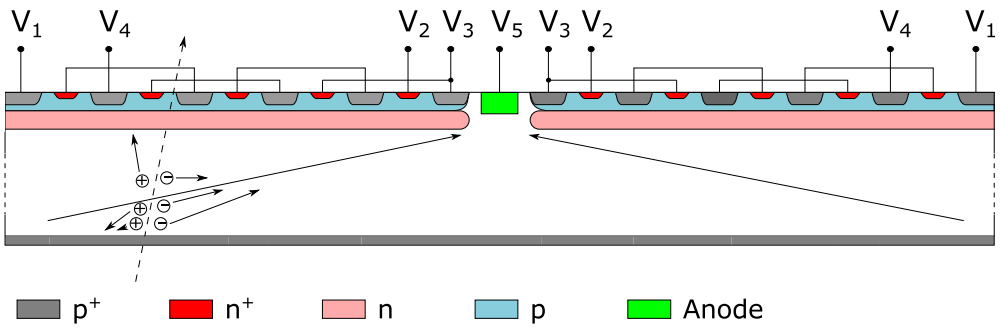

Figure 5.1: Schematic cross-section of the novel modified Silicon Drift Detector.

On the backside of the modified SSD there is a thin large-area p+ type doping functioning as a homogeneous radiation entry window which is preferably biased from the front side with the punch through biasing scheme (Kemmer and Lutz, 1989). On the front side of the device there is a large area deep low dose n type implanted layer and a large area shallower and higher dose p type implanted layer. These n and p type large area layers are preferably implanted with the same mask.

The n+ rings act as gates of very large concentric JFETs (Junction Field Effect Transistor). The p+ rings act as sources and drains of the very large concentric JFETs. The parts of the p layer situated underneath the n+ rings form the channels of the very large concentric JFETs. The role of the deep n layer is to vertically confine the p layer particularly at the location of the channel. Close to the anode the deep n layer prevents

also unwanted punch-through hole current flow from the front side p layer to the backside p+ radiation entry window. In addition, close to the anode the p layer functions also as a potential barrier preventing radiation-induced electrons from being absorbed by the innermost n+ rings.

Excluding the two outermost p+ rings the p+ rings are connected to an n+ ring of larger radius in such a manner that in between these interconnected p+ and n+ rings there is always one intermediate p+ ring and one intermediate n+ ring as depicted in Figure 5.1. This means that the electric potential of the intermediate p+ ring is always one JFET channel threshold voltage V_{th} (or slightly less) smaller than the electric potential of the interconnected p+ and n+ rings inclosing the intermediate p+ ring. Consequently, the electric potential of the interconnected rings reduces at steps of V_{th} towards the outer rim of the detector resulting in a horizontal drift field inside the substrate. The two outermost p+ rings do not have an n+ ring to be interconnected with. It is beneficial to have an electric contact on the second outermost ring that can be monitored externally. The anode is marked with green colour in Figure 5.1 because it could be replaced e.g. with a Modified Internal Gate (MIG) readout transistor (Aurola, 2005a and Aurola et. al., 2015a).

The more detailed operational principle and biasing scheme is presented in Publication II.

In order for the arrangement to work it is crucial that the innermost n+ ring is biased such that a hole current will run from the innermost p+ ring through the channel beneath the innermost n+ ring to the second innermost p+ ring and onwards towards the outermost p+ ring biased at V1. This current will ensure proper biasing of the SDD ring structure — without it the proposed SDD ring structure would likely break due to the build-up of a too high reverse bias between some of the SDD rings. Afore said current is somewhat analogous to air blown into an inflatable boat for the sake of providing necessary rigidity.

The purpose of the biasing of the SDD's electrodes (and the backside p+ layer) is first of all to fully deplete the semiconductor body underneath the SDD rings and secondly to create a necessary radial drift field transporting radiation-induced electrons towards the anode as depicted in Figure 5.1. The p+ rings and the backside p+ layer collect the radiation-induced and interface generated holes. The n+ rings collect the interface-generated electrons and thus the generation of dark noise at depleted interfaces is prevented except in the area next to the anode.

In the substrate beneath the deep n layer there is no undulating potential profile in the modified SDD. Instead a constant radial drift field is established in the substrate at relatively small distance from the deep n layer. This stems from the facts that in a p type JFET the electric potential of a conductive p channel is always about the same or smaller than the potential of the p+ source, that the drain is more negative than the source, and

that the drain acts as the source of the next JFET situated further away from the anode. On the other hand, the pn junction between the conducting p channel and the deep n layer forms a potential barrier for radiation-generated electrons drifting in the substrate preventing them from being absorbed by the innermost n+ rings. The very same barrier prevents also punch-through hole current flow from the innermost p+ rings towards the p+ backside layer. These aspects enable the radiation-induced electrons to drift next to anode relatively close to the innermost p+ ring meaning that a relatively small reverse bias can be applied between the anode and the innermost p+ ring enabling also a relatively small anode size.

In the modified SDD the maximum reverse bias between the n+ and p+ rings is $2\times V_{th}$, which is relatively small. Besides, the reverse biased pn junction between the conducting p channel and the n+ rings collecting the interface generated electrons acts as potential barrier for electrons located in the n+ rings preventing them from flowing into the substrate. Furthermore, in the modified SDD the biasing of the n+ and p+ rings is not dependent on the amount of positive oxide charge since the potential distribution of the SDD rings is defined by the JFET threshold voltage Vth which is not affected by the positive oxide charge but by the p type channel doping beneath the n+ ring as well as by the deep n layer and n type substrate doping. The reason is that the n+ ring situated in between the channel and the interface shields the channel from the influence of the positive oxide charges located at the interface above the n+ ring.

The facts that relatively small reverse biases between the anode and the innermost p+ ring as well as between the n+ and p+ rings may be utilised, that the operation is not affected by positive oxide charge, and that the formation of interface generated dark noise is prevented mean that the modified SDD should be relatively radiation hard. Yet another feature is that the width of the n+ or p+ rings does not play any crucial role in the modified SDD and can be thus chosen freely in different parts of the SDD (e.g. smaller width can be utilized close to anode).

In the proposed novel modified SDD altogether 4 electrodes (V1, V2, V3, and V4) are required for the biasing of the ring configuration whereas only 2 are required in the conventional SDD of Figure 3.1. In the modified SDD no resistor chain is, however, needed and it can be manufactured with standard process steps — beside the n+ and p+ regions only one additional implant mask is required for the large area p and n implanted layers.

The proposed modified SDD design was verified by performing 3D simulations in TCAD environment.

The simulated modified SDD structure is presented in Figure 5.2. Only half of the structure is needed for 3D simulations since the device is cylindrically symmetric — the

rotation axis is depicted in the figure. The width of the p+ drift ring is 5 µm, the width of the n+ ring acting as the gate is 2 µm, and the gap between the p+ and n+ rings is 2 µm. The radius of the n+ anode doping (n6) is 10 µm and the gap between the innermost p+ drift ring (p6) and the anode is 5 µm. The simulated device comprises an n- type 300 µm thick silicon substrate having a resistivity of 2 kΩcm. The effect of the fixed charge at the Si/SiO_2 interface is taken into account by defining an oxide charge concentration as 1e11 cm^{-3}.

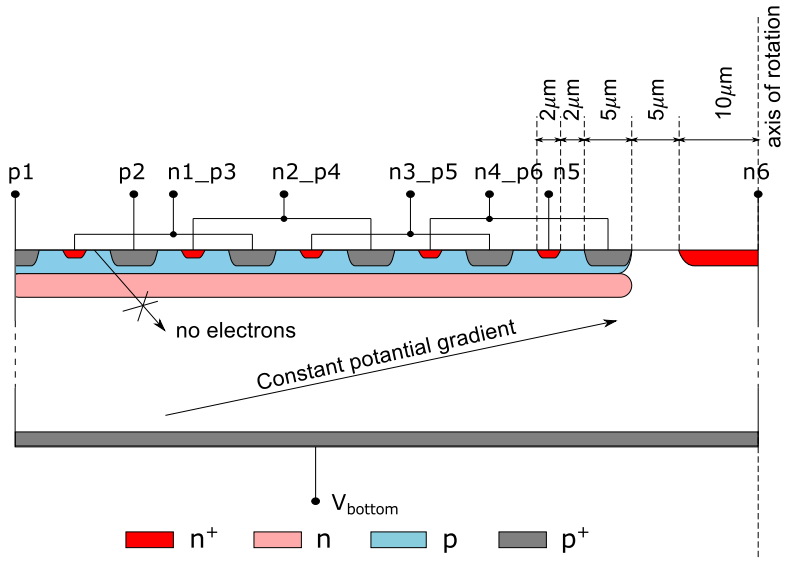

Figure 5.2: Schematic cross-section of the simulated cylindrically symmetric SDD. The rotation axis is depicted in the figure. Contacts p2, n1_p3, n2_p4, n3_p5 are not biased.

The electrostatic potential distribution and electron current distribution in the structure were obtained as simulation results and presented in Publication II. These results show that a constant radial drift field is established inside the substrate guiding signal charges towards the anode, i.e. an undulating potential profile is avoided, no interface-generated electrons are collected by the anode, i.e., there is no interface-generated dark noise in the simulated SDD structure.

5.1.1 Conclusions

The proposed modified SDD structure which has been simulated in this work comprises only a small number of rings surrounding the anode but it is sufficient to prove that the concept functions as intended. The proposed SDD has the advantages that no resistive chain is required, that the formation of interface dark noise is prevented, that the operation

is not sensitive to positive oxide charge, and that it should be relatively radiation hard. It should be also possible to utilise the proposed ring structure in detectors that are made from other semiconductor materials than silicon like e.g. germanium.

One should note that by incorporating similar large area p and n layers one should be able to provide largely the same benefits than with the proposed modified SDD albeit with the cost of an extra manufacturing step required for the formation of the resistive chain.

5.1.2 Suggestions for future work

Further verification of the proposed SDD design would require manufacturing of a demonstrator.

5.2 Novel double modified internal gate (MIG) pixel design

The challenges of pixelated CMOS and CCD radiation detectors are explained in Section 3.2. The goal of the work presented in Publication I was to develop a novel detector pixel design which would combine a very low noise, low crosstalk, high QE for NIR light and X-rays, as well as durability against radiation damage and easy manufacturing process on existing CMOS lines. The combination of all these features in one CMOS or CDD pixel design was not available at that time.

The developed of the novel pixel was successfully done and is well suited for Low-light level imaging, X-ray spectroscopy, Synchrotron, X-ray Free Electron Laser (XFEL) facilities.

The basic operational principle of the developed novel double modified internal field effect transistor (MIGFET) pixel is presented in Section 2. The cross-section and the top view of the pixel are presented in Figure 2.2.

The low 1/*f* and RTS noise is due to the fact that a deep buried channel can be utilized in a MIG sensor since non-circular readout transistor design is enabled. Besides the deeper the buried channel the bigger the signal is, and secondly, the smaller the signal the smaller the 1/*f* and RTS noise is. The latter fact is because the less there is charge in the MIG the deeper the buried channel is. The potential difference from the bottom of the buried channel to the interface has been found to be from 0.45 V to 0.68 V throughout the length of the buried channel.

Furthermore, the 50 μm thick fully depleted BSI pixel design offers several advantages such as 100% fill factor, high QE for NIR and visible light as well as low energy X-rays up to several keV, low crosstalk, anti-blooming, and very high readout speed. The last mentioned fact is due to the current mode readout as well as due to the fact that at reset and charge transfer stages there are no potential barriers hindering the signal charge transport.

Another reason for the low crosstalk is the fact that current mode readout (i.e. readout of source or drain current) is enabled meaning that capacitive coupling between pixels is minimised since during readout all the nodes of the pixel and all the lines connecting the pixel are held at constant designated potentials. Since only current signal and no potential signal is attached to the readout line (source or drain line) there is no capacitive coupling between the readout lines. In case source current in the source line and the drain current in the drain line are proceeding into opposite direction and the source and drain lines are located close to each other (e.g. on top of each other) there will be neither inductive coupling to the source and drain lines of neighbouring pixel columns. In voltage mode readout (typically Source Follower (SF) readout (Seitz and Theuwissen, 2011) the voltage along read lines (in the SF readout the readout line is the source line which is connected to a constant current source and the readout is performed by reading out the potential on the source line) couples to the sense nodes (in SF configuration the sense node comprises the floating diffusion, the gate of the source follower transistor, and the source of a reset transistor) of other pixels that are read out simultaneously. The reason why very fast readout is enabled stems from the fact that in current mode readout operation the readout lines are at constant potential. In voltage mode readout, on the other hand, the potential on the read lines is continuously altered and the capacitive charging of the read line takes time, which slows the readout process. The simulation demonstrates the charge to current conversion gain for source current readout to be 1.4 nA/e.

The good manufacturability stems from the fact that the current running in the channel of the readout transistor is composed of similar charges to the signal charges situated in the MIG modulating the current of the readout transistor. This arrangement is realized by placing a potential barrier formed of fully depleted semiconductor material in between the channel and the MIG. The advantage is that the location of lowest potential energy for signal charges in MIG is well aligned with the location of lowest channel threshold.

The NDCDSR enables very low read noise and it stems from the fact that the read noise is small (due to very low level of interface generated 1/*f* and RTS noise) and because it is further possible to average out the overall read noise by performing multiple CDS measurements meaning that the MIG sensors offer very good energy resolution for very low energy X-rays originating e.g. from lithium. The facts that the MIG sensors do not suffer from interface problems (no interface generated dark noise, very low level of interface generated 1/*f* and RTS noise, no image lag) means that MIG sensors are inherently tolerant to X-rays and electrons having energies below 300 keV. The lack of interface problems has also the additional benefit that it should enable very low noise detectors to be made from semiconductor materials (e.g. germanium) having much worse interface quality than silicon, which is often not possible with other detector technologies since they suffer from interface issues.

The anti-blooming is due to the fact that the potential barrier for signal charges situated in MIG is always much lower towards the drain than towards the neighbouring pixels (and towards source node which is important from noise point of view). In the measurement and transfer potential configuration the signal charges are located

underneath the gate biased at higher positive voltage than during integration and thus the anti-blooming protection is even better during other modes than during integration.

The statements written above concerning pixel design benefits and performance have been tested by simulation of pixel performance in 3D with the TCAD software tool (Sentaurus Device Used Guide, 2013, Sentaurus Process User Guide, 2013 and Sentaurus Structure Editor User Guide, 2013). Simulation results of the 8 µm pitch 50µ m thick fully depleted BSI double MIG pixel structure designed for a slightly modified 0.18 µm or smaller line width 5 V CMOS process were presented in Publication I (Aurola et. al., 2015a). The performance of the pixel has been studied by simulating operational steps at -40^{o}. The first step is reset of the pixel, when all the charge present in the pixel is removed. The second step is integration, when charge accumulates in the MIG. The third step is the non-destructive CDS procedure comprising non-destructive charge transfer from one MIG to another in between non-destructive readouts which is presented in Figure 5.3. In Figure 5.3 an effect of 964 electrons in the MIG on the conducting channel can be seen. The charge to current conversion gain can be then calculated as follows: $\frac{41.9\ \mu A - 40.5\ \mu A}{964\ e} = 1.4\ nA/e$.

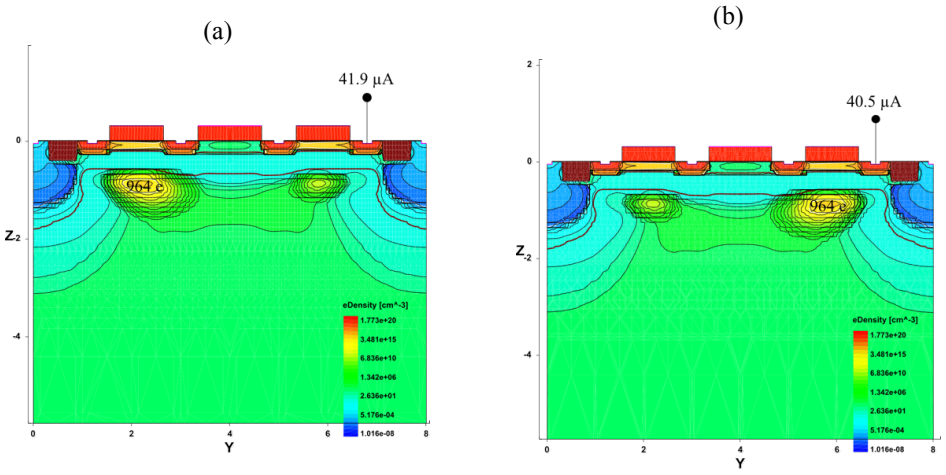

Figure 5.3: Measurement: (a) Electron density distribution on the cross-section of the 3D simulated pixel when 964 electrons are located in the left MIG. The current at the source (S2) of the right MIGFET is 41.9 µA. (b) Electron density distribution on the cross-section of the 3D simulated pixel when 964 electrons are located in the right MIG. The current at the source (S2) of the right MIGFET is 40.5 µA.

5.2.1 Conclusions

On the basis of this work, the pixel concept is suggested for use in low light imaging as well as low energy X-ray applications. The reason is that the pixel does not suffer from interface issues (i.e. there is no interface generated dark noise, no interface generated

image lag, and virtually no interface generated 1/ f and RTS noise). Furthermore, the 50 μ m thick fully depleted BSI pixel design offers several advantages such as 100% fill factor, high QE for NIR and visible light as well as low energy X-rays up to several keV, low crosstalk, anti-blooming, and very high readout speed.

Another conclusion arising from work carried out in Publication I (Aurola et. al., 2015a), is that based on the simulation results the transfer stage limits the Non-Destructive Correlated Double Sampling Full Well Capacity (NDCDSFWC) of the pixel, i.e., the maximum amount of signal charge that can be successfully stored, read out, and transferred from one MIG to another. The reason for this is that the barrier for signal charges located in the MIG to escape to drain or to an empty MIG is by far the smallest during the transfer stage. At the level of 964 signal electrons no charge loss was identified. The NDCDSFWC is estimated to be somewhere in between 1000 and 2000 electrons at -40^{o} C which relates to (3.6keV to 7.3keV). This may seem limited but one should acknowledge that the pixel design is preliminary. If a larger pixel size is used and/or the pixel design is optimised according to the FWC it is possible to considerably increase the NDCDSFWC.

5.2.2 Suggestions for future work

The current work presents only theoretical concept development and further verification by numerical simulations. Even though some earlier concept of the pixel has been manufactured and the basic operational principle has been measured and confirmed (Seppälä, 2010) there is a need for a full scale pixel matrix prototype to be manufactured in order to measure and test detector performance and obtain the first optical image. At the moment of writing of this thesis there is a preparation going on for manufacturing of the first pixel matrix prototype which will be then measured and reported in later works.

5.3 Novel 3D radiation detector design

In Publication IV (Aurola et. al., 2016) a novel Pixelated Vertical Drift Detector (PVDD) concept (Aurola, 2005b) was proposed to address issues described in Section 3.4. The schematic drawing of the PVDD is presented on Figure 5.4.

The proposed PVDD is well suited for high energy X-ray detection and gamma-ray detection.

The PVDD is based on the idea of providing resistive paths that reach from one surface throughout the semiconductor detector to the opposite surface. The presented PVDD design uses an n- type high-resistivity silicon substrate wherein holes having p type doped walls and reaching throughout the substrate are situated at the pixel borders play the role of resistive paths. The ways to manufacture holes in the substrate have been discussed in Publication IV. On the front side there are two types of dopants forming contacts — the first type (n+) dopants collect the radiation-induced charges (N2 contact) and the second type (p+) dopants form contacts (P2 contact) to the one end of the resistive paths and is

located inside a p type layer. On the backside there are second type dopants (p+) forming contacts (P1 contact) to the other end of the resistive paths and an optional first type dopants (n+) contact N1 that is located inside the backside p layer.

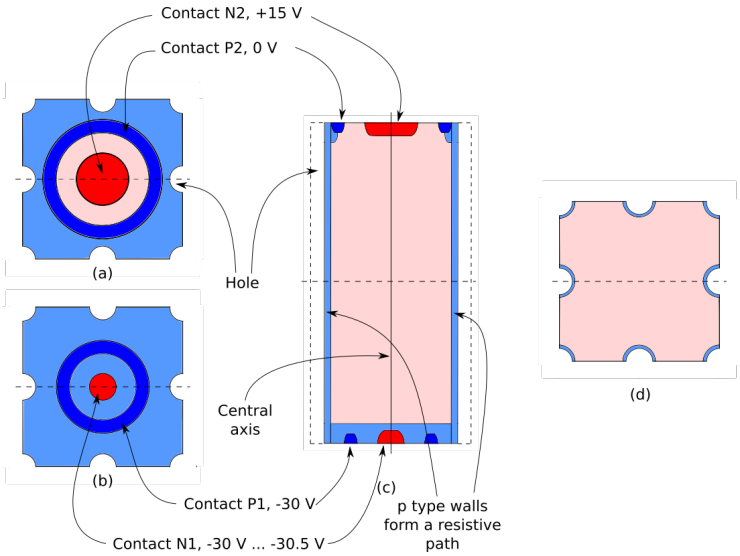

Figure 5.4: a) Front side of the Pixelated Vertical Drift Detector (PVDD), (b) backside of the PVDD, (c) vertical cross-section of the PVDD, and (d) central horizontal cross-section of the PVDD.

By implementing a relatively small reverse bias between the first and second type contacts on the front side a vertically invariant horizontal electric field component is generated around the resistive path that depletes the bulk of the PVDD. The application of a potential difference between the second type contacts that are connected to the opposite ends of the resistive paths and located at the opposite surfaces of the detector results in a current flow inside the resistive paths. In case the resistivity along the resistive path is approximately constant the current flow through the resistive path results in according to the Ohm's law a constant potential gradient inside the resistive path. This constant potential gradient in the resistive paths (assuming that the resistive paths are oriented vertically) results in also a constant vertical drift field inside the depleted semiconductor bulk transporting radiation-induced charges towards the charge collecting contact located on the front side. In order to establish the resistive path corresponding to the hole-walls it is important to have on the horizontal pixel cross-section more p type dopant atoms on the hole-walls than n type dopant atoms in the substrate. If this condition is met then p type hole-walls are not fully depleted even if the n type substrate is fully depleted.

The constant vertical electric field component transports radiation-induced charges towards output contacts located on one surface of the detector. The fact that the vertical electric field component is constant means that the detector thickness is not limited by the electric field enabling thus high detection efficiency. The small surface area of the charge collecting contacts enables low output capacitance that is not dependent on the detector thickness. The benefit of the small output capacitance is that it enables good energy resolution. The vertically invariant horizontal field inside the detector provides efficient confinement of radiation-induced charges even in thick detectors insuring thus low crosstalk and good spatial resolution. A constant vertical electric drift field and a vertically invariant horizontal electric field component inside the detector (excluding regions close to detector surfaces) provide a combination of high pixel aspect ratio, high detection efficiency, low crosstalk, and low noise (due to low output capacitance) in one pixel.

The working principle and operation of the proposed detector are presented in Publication IV.

It is important to note that the thicker the PVDD, the larger is the voltage that must be applied in order to ensure an adequate vertical electric field. On the other hand, by providing a thick enough PVDD it is possible to connect a voltage in between the first and second surface that greatly exceeds a voltage that can be connected to a conventional planar device having similar substrate doping, which is a novel feature in semiconductor applications.

It has been shown in the Publication IV that the current running in one hole-wall, in the structure where the pixel size is 100 µm and each of the holes has a radius 5 µm is approximately to 43 µA and remains the same for 300 µm and 600 µm structures if the electric field and the hole diameter remains the same for both structures.

The operation and performance of the proposed detector concept has been validated by performing simulations of the quarter of the whole pixel in 3D TCAD environment. It was possible to simulate only the quarter of the pixel due to its symmetry and by doing so required simulation time was considerably reduced. The simulated structures were 300 µm and 600 µm thick with holes having a radius 5 µm and next to the hole-wall there was a 1 µm thick p type layer which outer radius corresponded to 6 µm and which p-type dopant (boron) concentration corresponded to 2.2e15 cm^{-3}. The n type substrate dopant (phosphorus) concentration corresponded to 5e12 cm^{-3}.

As the simulation results show for 300 µm and 600 µm thick structures it was possible first to establish a horizontal electric field component inside the semiconductor substrate pointing towards the central axis of the pixel which resulted in depletion of the substrate and then to establish a hole-current flow along the p type hole-walls which resulted in a constant potential drop along the hole-walls generating a constant vertical electric field component throughout the PVDD. The constant vertical electrostatic potential gradient inside a 300 µm thick device can be seen on Figure 5.5(a) and Figure 5.5(b).

The barrier from the middle to the edge of the pixel is constant in the mid portion of the pixel and equalling to around 3 V (Figure 5.5(b)) which is more than enough to eliminate the blooming crosstalk. Corresponding simulation results for a 600 µm thick PVDD shows that the barrier equals to around 3 V as well meaning that the thickness of the pixel does not affect the barrier height.

By applying the voltage scheme described in Publication IV it is possible to establish an electron current running in the middle of the pixel which can be then used to fill traps before the device is exposed to the desired radiation. This would increase the signal particularly in detectors that are made of semiconductor materials being prone to trapping.

The performance and behaviour of the illuminated pixel was tested by illuminating the pixel with a 100 ns monochromatic 850 nm light pulse having an intensity of 1500 W/cm2. According to the simulation results the output current increases considerably during the light pulse. Furthermore, the photo induced excess output current dies off at around 23 nano-seconds after the termination of the light pulse.

The capacitance of the signal charge collecting contact N2 in the operational 300 µm thick device was simulated to be around 49 fF, which is exactly the same as in the 600 µm thick device meaning that in a thick enough PVDD the capacitance of the contact N2 is not affected by the device thickness.

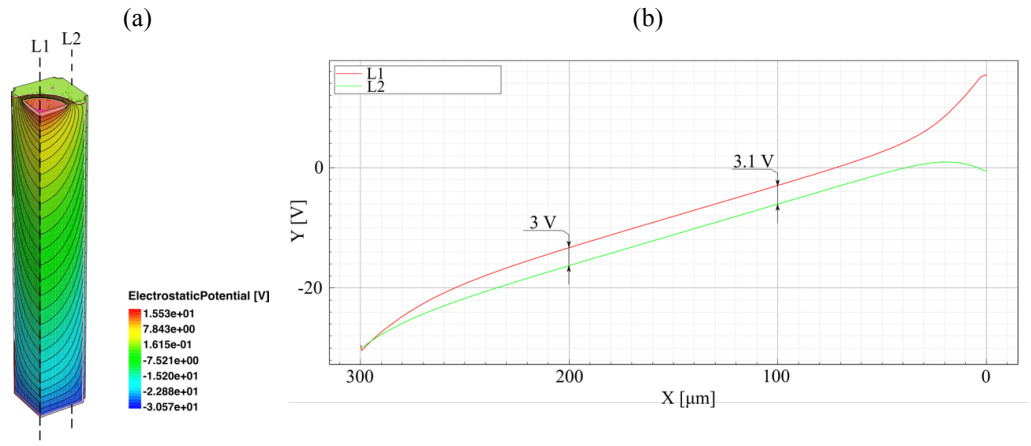

Figure 5.5: Simulation results for 300 µm thick PVDD: (a) Electrostatic potential distribution inside the PVDD quarter-pixel. Vertical cutlines L1 and L2 are illustrated. (b) Electrostatic potential on the vertical cutlines L1 and L2 corresponding to the case when P1 and N1 are biased at -30 V, N2 is biased at 15 V, and P2 is biased at 0 V.

5.3.1 Conclusions

Benefits of the developed PVDD concept are: high pixel aspect ratio, high detection efficiency, low crosstalk, low noise, the maximum absolute magnitude of the electric field is not dependent on the detector thickness and thus the detector thickness is not limited by the electric field, pixel specific trapping tendency is more predictable. An electron flow can be generated running through the pixel means that before the detector is exposed to radiation electron traps located along the electron drift path can be filled with electrons corresponding to the electron flow.

Presented benefits of the PVDD concept may enable to expand the operational range of silicon and germanium based direct conversion radiation detectors to higher energy X-ray applications without degrading the detector performance – e.g. a silicon based direct conversion detector reaching 90% conversion efficiency for 30 keV photons must be at least 9 mm thick, which was previously impossible to achieve. Thus in some applications it may be possible to use silicon or germanium detectors instead of compound semiconductor detectors which are expensive, difficult to process, and prone to lattice defects. On the other hand, the PVDD concept may also improve the performance of compound semiconductor detectors so that it could be possible in some applications to replace indirect conversion radiation detectors with direct conversion compound semiconductor radiation detectors. Yet another advantage of the PVDD in compound semiconductor applications is that the typical disproportion between the electron and hole mobilities can be exploited by choosing the electrons as signal charges and by choosing the holes as the charge type forming the resistive paths. In this manner the signal charge collection time as well as the power consumption could be minimized in the PVDD.

5.3.2 Suggestions for future work

In this work the concept presented on Figure 5.4 was simulated only using silicon as a substrate material. Thoughts expressed in this work that this concept can be applied to other semiconductor materials such as germanium or compound semiconductor materials have to be verified in a future work.

It is acknowledged that manufacturing challenges must be overcome before the basic PVDD concept could offer a practical alternative to existing radiation detectors. Furthermore, in order to bring forth the research a PVDD demonstrator would need to be manufactured. This is, however, out of reach at the moment and thus collaboration on the matter would be warmly welcomed.

It is important to note that by providing a thick enough PVDD it is possible to connect a voltage in between the first and second surface that greatly exceeds a voltage that can be connected to a conventional planar device having similar substrate doping, which is a novel feature in high voltage semiconductor applications and can bring a beneficial contribution to this field. Since authors are not from the high voltage semiconductor devices field they would encourage scientists from the field to verify and test the concept.

It should be possible to utilise the PVDD concept (comprising a detector edge functioning as a resistive path) in edgeless tileable detector configurations in such a manner that radiation induced charge generated inside an edge or corner pixel is also confined to it. In other words, the detector edge should not repel charge from edge or corner pixels to neighbouring pixels. This would, however, need to be verified with 3D simulations by checking that the horizontal potential barriers in the edge and corner pixels can be made large enough in order to prevent blooming of signal charge from one pixel to another.

Another idea that has been expressed in the work is that in case a point like radiation source is utilised the crosstalk can be further mitigated if one utilises tilted holes wherein the central axis of the holes is pointed towards the point like radiation source. The proposed designs are presented in Publication IV. The downside of the tilted holes is, however, that it is difficult to realise with existing standard manufacturing tools. Further work has to be done to verify these designs.

5.4 Novel detector design mitigating problems related to sawed edges

A detector edge structure has been developed dealing with the issues explained in Section 3.5.

A cross-section of the simulated edge arrangement of the thinned detector is presented in Figure 5.6 wherein the detector arrangement surrounded by the proposed edge area corresponds to a standard diode detector. The front view of the detector of Figure 5.6 is presented in Publication III.

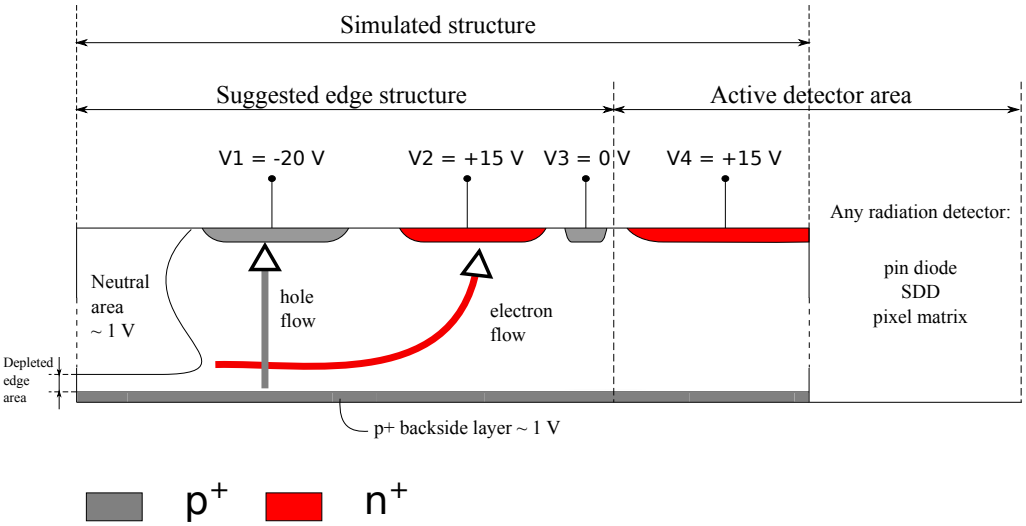

Figure 5.6: A schematic drawing of the proposed detector edge structure (the potential values correspond to simulations). The floating neutral area next to the edge minimizes the depleted edge area. The outermost p+ ring (at V_1) is used for punch-through biasing of the backside p+ layer

and for depleting the detector bulk. The n+ ring at V_2 is used for the collection of edge-generated electrons in particular. The p+ ring at V_3 is used to isolate the active detector area (at V_4) from the n+ ring at V_2 and from edge generated electrons.

The processing of a thinned detector structure that is not bonded to a support wafer necessitates that no lithographic steps can be performed after thinning. Therefore a maskless p+ implant is deployed on the backside of the detector's n type high resistivity substrate. The combination of oppositely doped substrate and conductive backside layer is utilised in order to achieve high QE for blue light. The biasing of the backside layer is performed from the front side utilising punch-through biasing. The punch-through biasing is achieved with the outermost p+ ring (at potential V_1) – when a large enough reverse bias is applied to this p+ ring the depletion region in the n- bulk around the p+ ring will extend to the backside p+ layer. At even larger reverse bias values the potential of the p+ backside layer will follow the p+ layer resulting in punch-through biasing of the p+ backside layer. Consequently, a sufficiently large reverse bias applied to afore said p+ ring will deplete the whole bulk between the p+ backside layer and the large area n+ doping (at potential V_4) as already explained in (Kemmer and Lutz, 1989).

Since there is no biased contact at the edge of the detector a floating neutral area will be formed next to the edge as depicted in Figure 5.6. The potential of this neutral area will follow closely the potential of the p+ backside layer (Kemmer and Lutz, 1989). The benefit of the neutral area next to the sawed edge is that it minimises the depleted area at the sawed edge and thereby the edge generated leakage current.

The excess electrons (including edge generated electrons) collected by the neutral area flow horizontally in a channel located in the proximity of the backside p+ layer and beneath the outermost p+ ring after which these electrons flow through the substrate and are collected by an n+ ring (at potential V_2) as is depicted by the red arrow in Figure 5.6. Excess holes collected by the p+ backside layer flow vertically to the outermost p+ ring as is depicted by the vertical grey arrow. An additional p+ ring (at potential V_3) prevents excess electrons originating from the edge area from entering into the large area n+ doping collecting the radiation-induced electrons.

The proposed detector edge design was verified by performing 2D simulations in TCAD environment.

The simulated device comprises an n-type 100 µm thick silicon substrate having a resistivity of 2 kΩcm. The effect of the fixed charge at the Si/SiO_2 interface is taken into account by setting the positive oxide charge concentration to 1e11 cm^{-3}. The bias voltages at V_1 = -20 V, V_2 = +15 V, V_3, = 0 V, and V_4 = +15 V presented in Figure 5.6 have been used in the 2D simulations. The value of around 1 V at the backside p+ layer and the

neutral area in Figure 5.6 corresponds to the 2D simulation results. One should note, however, that in reality the potential at the backside p+ layer and at the neutral area would differ more.

As an example, electrostatic potential distribution of the simulated structure is presented in Figure 5.7. The border of the neutral area situated next to the detector edge is depicted by a white line – elsewhere the detector is fully depleted excluding the n+ and p+ areas. It can be deduced from Figure 5.7 that the proposed detector edge structure functions as desired; there is a neutral area next to the detector edge, the depleted edge area is minimized, and beneath the anode the detector is fully depleted.

The simulation results presented in Publication IV show also that no edge generated electrons reach the active detector area, the punch through biasing effect is established as intended.

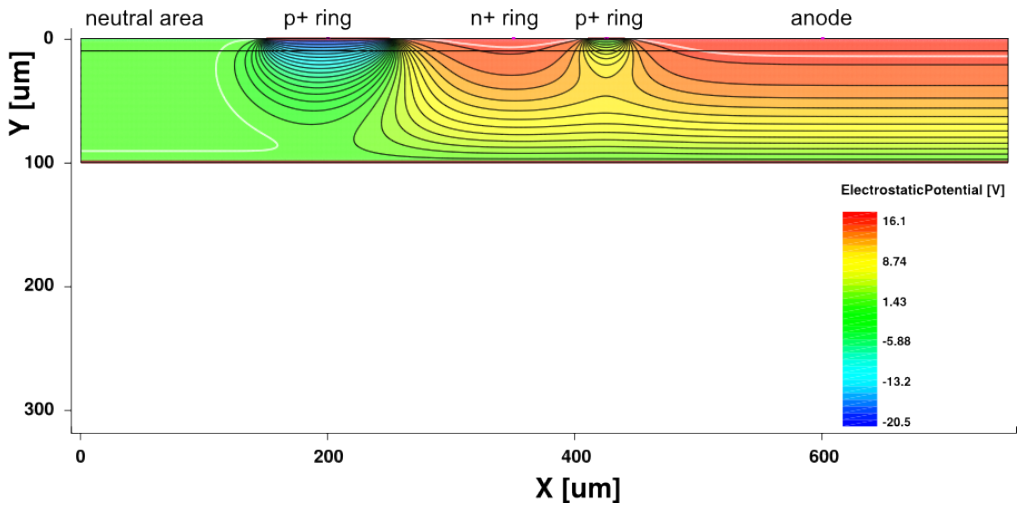

Figure 5.7: Electrostatic potential distribution in the simulated detector edge structure. The border of the neutral area situated next to the detector edge is depicted by a white line. The detector is fully depleted beneath the anode.

Publication IV also presents some examples of other radiation detectors having a homogeneous backside conductive layer of opposite doping type than the substrate or incorporating an inversion layer on the backside incorporating the proposed edge structure. One of these examples is a pixelated detector which incorporates on the backside a negatively charged insulator layer (Aurola and Kalliopuska, 2005) (formed e.g. of hafnium oxide) providing an inversion layer of holes underneath the interface.

Another example is the Silicon Drift Detector (SDD) presented. The proposed detector edge arrangement enables the biasing of the SDD's backside p+ layer, minimises the amount of edge generated leakage current, and prevents edge generated electrons from entering into the active SDD area, i.e., the SDD does not suffer from edge generated dark noise.

5.4.1 Conclusions

The proposed detector edge structure enables thinned detectors with good QE for blue and NIR light, low CT, low dark noise, simple manufacturing without the need for a support wafer or backside processing, as well as low edge generated leakage current. In order to maximise the benefits of the proposed detector edge structure neutron transmutated silicon (or germanium) wafers should be used.

5.4.2 Suggestions for future work

Further verification of the proposed edge design would require manufacturing of a demonstrator.

6 Conclusions

The purpose of this work was to develop new radiation detector concepts with improved performance and manufacturability and to utilize 2D and 3D process and device simulations to validate the operational principle and the benefits of the proposed radiation detector concepts.

It can be concluded that the goal was successfully achieved and four concepts were developed and verified and their benefits clearly shown. Major issues currently present in radiation detectors were dealt with and completely removed or their impact was considerably reduced. All of the designs can be manufactured using other than silicon semiconductor materials, i.e. germanium, due to absence of Insulator/Semiconductor interface issues. All of the designs are also radiation hard.

The designed double-MIGFET pixel does not suffer from interface issues, i.e. there is no interface generated dark noise, no interface generated image lag, and virtually no interface generated 1/*f* and RTS noise. The design offers 100% fill factor, high QE for NIR and visible light as well as low energy X-rays up to several keV, low crosstalk, anti-blooming, and very high readout speed. The design is suggested for use in low light imaging as well as low energy X-ray applications.

The designed modified SDD structure has the advantages that no resistive chain is required, that the formation of the interface dark noise is prevented, that the operation is not sensitive to positive oxide charge. The proposed MIGFET concept can be used as an anode in the proposed modified SDD structure to completely avoid any Insulator/Semiconductor interface issues.

The designed detector edge structure enables thinned detector with good QE for blue and NIR light, low CT, low dark noise, and low edge generated leakage current. The proposed concept can be also used with MIGFET design and modified SDD structure.

The designed PVDD concept offers several advantages. The maximum electric field is not dependent on the detector thickness and thus the detector thickness is not limited by the break-down electric field. The capacitance of the output node is small and does not depend on detector thickness. The crosstalk is mitigated. The proposed design may enable the operational range of silicon and germanium based radiation detectors to higher energies without degrading the detector performance or it can as well improve performance of compound semiconductor radiation detectors.

Though all proposed concepts display excellent characteristics based on the results of simulations, the physical demonstrators need to be manufactured to fully verify the concepts.

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Publication I

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Characterization of double modified internal gate pixel by 3D simulation study

A. Aurola,[a,b] **V. Marochkin**[a,b,1] **and T. Tuuva**[b]

[a] *Pixpolar,*
Tekniikantie 1, 02150, Finland
[b] *Lappeenranta University of Technology,*
P.O. Box 20, 53851, Finland

E-mail: Vladislav.Marochkin@pixpolar.com

ABSTRACT: We have developed a novel detector concept based on Modified Internal Gate Field Effect Transistor (MIGFET) wherein a buried Modified Internal Gate (MIG) is implanted underneath a channel of a FET. In between the MIG and the channel of the FET there is a depleted semiconductor material forming a potential barrier between charges in the channel and similar type signal charges located in the MIG. The signal charges in the MIG have a measurable effect on the conductance of the channel. In this paper a double MIGFET pixel is investigated comprising two MIGFETs. By transferring the signal charges between the two MIGs Non-Destructive Correlated Double Sampling Readout (NDCDSR) is enabled.

The proposed MIG radiation detector suits particularly well for low-light-level imaging, X-ray spectroscopy, as well as synchrotron and X-ray Free Electron Laser (XFEL) facilities. The reason for the excellent X-ray detection performance stems from the fact that interface related issues can be considerably mitigated since interface generated dark noise can be completely avoided and interface generated $1/f$ and Random Telegraph Signal (RTS) noise can be considerably reduced due to a deep buried channel readout configuration.

Electrical parameters of the double MIGFET pixel have been evaluated by 3D TCAD simulation study. Simulation results show the absence of interface generated dark noise, significantly reduced interface generated $1/f$ and RTS noise, well performing NDCDSR operation, and blooming

[1] Corresponding author.

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protection due to an inherent vertical anti-blooming structure. In addition, the backside illuminated thick fully depleted pixel design provides a homogeneous radiation entry window, low crosstalk due to lack of diffusion, and good quantum efficiency for low energy X-rays and NIR light.

These facts result in excellent Signal-to-Noise Ratio (SNR) and very low crosstalk enabling thus excellent X-ray energy and spatial resolution. The simulation demonstrates the charge to current conversion gain for source current readout to be 1.4 nA/e.

KEYWORDS: X-ray detectors; Photon detectors for UV, visible and IR photons (solid-state) (PIN diodes, APDs, Si-PMTs, G-APDs, CCDs, EBCCDs, EMCCDs etc); Radiation-hard detectors; Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc)

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1 Introduction

It is generally known that Gamma rays, X-rays, and electrons with energies below the minimum threshold for bulk defects ($\sim 300\,\mathrm{keV}$) generate only defects in the dielectrics, at the dielectric silicon interface, and the interface between dielectrics [1]. The build-up of the interface damage increases dark current generation from depleted interfaces. If the interface-generated dark current can mix with the signal charges the build-up of the interface damage will increase the dark noise and thereby reduce the Signal to Noise Ratio (SNR) as well as the useful lifetime of the detector and particularly so in X-ray (and/or electron) detection applications or imaging applications utilized in radioactive environments. The radiation-induced interface damage also affects the read noise in surface channel or shallow buried channel devices since it increases the amount of interface defects and thereby interface generated $1/f$ and RTS noise.

Besides having low dark and read noise it is important for X-ray detectors and for silicon Near Infra-Red (NIR) optimised image sensors to have a thick fully depleted Back-Side Illuminated (BSI) design. The full depletion is important in order to insure that no charge is lost due to recombination and in order to minimize crosstalk by preventing diffusion. BSI is required in order to provide a thin homogeneous radiation entry window, which enables 100% fill factor and the detection of very low energy X-ray photons. A thick detector, on the other hand, improves the Quantum Efficiency (QE) for NIR light and higher energy X-rays (important e.g. in X-ray fluorescence spectroscopy).

There are currently a number of pixelated detector architectures, which are described in more detail below. None of them offer, however, the combination of very low noise, low crosstalk, high QE for NIR light and X-rays, as well as durability against radiation damage. The reason for this is that a thick fully depleted BSI detector having very low read noise and being free of interface generated dark noise has not been realised so far. There are fully depleted backside illuminated Charge Coupled Devices (CCDs) utilising a regular gate architecture [2, 3] and CCDs [4] utilising a pn gate architecture (the original pn gate CCD architecture was introduced in [5]) enabling relatively

low read noise. In thick fully depleted BSI CCDs interline transfer architecture is not feasible and thus the only options are full frame and frame transfer architectures. In case reasonable frame rate (e.g. video rate) is desired then the frame transfer architecture is the only option. The problem with frame transfer architecture is that it suffers from smear [6] even though it is less prone to it than full frame architecture. The problem at least with [2, 3] is also that it suffers from interface generated dark noise during the charge transfer period.

Thick fully depleted BSI pixels can be realised also with simple pin (p type, intrinsic, n type) pixels wherein an n^+ collection node is connected either to a hybridized readout chip or to pixel specific integrated readout circuitry. Both of them are typically realized with a three transistor (3T) Complementary Metal Oxide Semiconductor (CMOS) pixel architecture but the 3T pixel architecture suffers from interface generated dark noise and high read noise [7, 8]. The pinned photo-diode structure [7, 9] utilised in 4T CMOS pixels enables BSI configuration as well as more or less complete removal of the interface generated dark noise [7, 8]. Thick fully depleted 4T pixels are, however, notoriously difficult to realise — the authors are not aware of any being realised so far.

Another problem in CCDs and CMOS image sensor technologies is that they utilise a readout configuration which is hereby referred to as External Gate Readout Configuration (EGRC) since the signal charge is brought to a MOS gate of a readout transistor, i.e., the gate is not located inside the semiconductor substrate but on top of it. A formidable problem in EGRC is that in Correlated Double Sampling (CDS) readout procedure (which is a mandatory requirement for accurate measurements) the signal charge is destroyed when it is brought to the external gate. This means that the signal charge can be readout accurately only once and thus one cannot mitigate the read noise by performing multiple readouts. It is important to note that the read noise can be removed by signal amplification but on the other hand the amplification process itself increases considerably the noise manifested by excess noise factor [7, 10].

A disadvantage of EGRC is also that the effect of $1/f$ and RTS noise on the read noise and thus on SNR is difficult to mitigate. By far the major part of the $1/f$ and RTS noise stems from the interface and thus by utilizing a buried channel readout transistor [11] the $1/f$ and RTS noise can be reduced — the deeper the channel the smaller the $1/f$ and RTS noise. However, the deeper the buried channel in EGRC the smaller the signal and the available voltage swing. Another problem is also that in EGRC the spurious signal due to a charge trapped at the semiconductor interface beneath the gate is always larger than the signal produced by a signal charge on the sense node and the deeper the buried channel the larger this difference is. A third reason is that the smaller the amount of signal charges the shallower the buried channel is, meaning that the smaller the signal the more there will be $1/f$ and RTS noise. This effect results in also non-linearity issues. These reasons reduce the beneficial effect of a deep buried channel on SNR in EGRC. One could also remove the interface generated $1/f$ and RTS noise in EGRC by utilising a JFET type diffusion gate instead of the MOS gate but this reduces considerably the available voltage swing and signal size as well as increases the depleted interface area next to doping belonging to the sense node. The latter fact increases the dark current generation rate at the sense node necessitating faster readout.

It is possible to reduce the read noise without introducing additional noise through NDCDSR, i.e., through accurate non-destructive signal readout. The NDCDSR has been demonstrated in an Internal Gate Readout Configuration (IGRC) [12] (the initial IG readout architecture was introduced in [13]). The problem is, however, the very large and unpractical pixel size as well as

manufacturability issues. The latter fact stems from the fact that in IGRC signal charges modulate an oppositely charged current running in the transistor channel, which is next briefly explained. Let us assume that there is a fully depleted n doped Internal Gate (IG) collecting signal charges beneath a hole surface channel that is closed for the time being. Next let us assume that the n doping of the IG is larger at a certain location which means that at this location there are more positively charged dopant atoms beneath the channel increasing the potential at the IG and at the interface above, i.e. the IG at this location will be more attractive for signal electrons but it will be more difficult to open the hole channel at this location than at other locations. This means that it is very difficult to match the location of the minimum channel threshold of the readout transistor with the signal charge potential minimum leading to poor tolerance against process fluctuations.

In the IGRC of [12, 14] a surface channel readout transistor is utilized resulting in a lot of $1/f$ and RTS noise [11]. The high $1/f$ and RTS noise means that a considerable amount of NDCDS measurements need to be performed in order to reduce the $1/f$ and RTS noise to a negligible level. The problem is that generally in IGRC a circular readout transistor is more or less mandatory in order to improve the manufacturability but the circular readout transistor inhibits the use of a deep buried channel. One could also reduce $1/f$ and RTS noise by utilizing a circular JFET in conjunction with the IGRC, but it would have a negative impact on the manufacturability.

As it will be shown in this work thick fully depleted BSI deep buried channel double MIG image sensors have several benefits: they offer NDCDSR, interface generated dark noise and image lag free operation, very low $1/f$ and RTS noise, 100% fill factor, excellent QE for low energy X-rays up to several keV as well as for NIR and visible light, very low crosstalk, inherent vertical anti-blooming mechanism, very fast operation, as well as good manufacturability with existing CMOS manufacturing lines.

The good manufacturability stems from the fact that the current running in the channel of the readout transistor is composed of similar charges to the signal charges situated in the MIG modulating the current of the readout transistor. This arrangement is realized by placing a potential barrier formed of fully depleted semiconductor material in between the channel and the MIG. The advantage is that the location of lowest potential energy for signal charges in MIG is well aligned with the location of lowest channel threshold.

The potential barrier between the channel and the MIG prevents also the mixing of signal charges with interface-generated charges meaning that a MIG sensor does not suffer from interface generated dark noise. Similarly this potential barrier separates also the signal charges from the interface during signal charge transfer (transfer is required in NDCDSR). Thus the MIG image sensor is not prone to image lag. The potential barrier enables vertical anti-blooming, i.e., when the MIG starts to be full of signal charges then the excess charges will flow over the potential barrier preventing the signal charges from spreading into neighbouring pixels.

The low $1/f$ and RTS noise is due to the fact that a deep buried channel can be utilized in a MIG sensor since non-circular readout transistor design is enabled. Besides the deeper the buried channel the bigger the signal is, and secondly, the smaller the signal the smaller the $1/f$ and RTS noise is. The latter fact is because the less there is charge in the MIG the deeper the buried channel is.

As already previously explained the good QE for NIR light and low energy X-rays up to several keV, the 100% fill-factor, and low crosstalk are due to the thick fully depleted BSI design.

Another reason for the low crosstalk is the fact that current mode readout (i.e. readout of source or drain current) is enabled meaning that capacitive coupling between pixels is minimised since during readout all the nodes of the pixel and all the lines connecting the pixel are held at constant designated potentials. Since only current signal and no potential signal is attached to the readout line (source or drain line) there is no capacitive coupling between the readout lines. In case source current in the source line and the drain current in the drain line are proceeding into opposite direction and the source and drain lines are located close to each others (e.g. on top of each others) there will be neither inductive coupling to the source and drain lines of neighbouring pixel columns. In voltage mode readout (typically Source Follower (SF) readout [7]) the voltage along read lines (in the SF readout the readout line is the source line which is connected to a constant current source and the readout is performed by reading out the potential on the source line) couples to the sense nodes (in SF configuration the sense node comprises the floating diffusion, the gate of the source follower transistor, and the source of a reset transistor) of other pixels that are readout simultaneously. The reason why very fast readout is enabled stems from the fact that in current mode readout operation the readout lines are at constant potential. In voltage mode readout, on the other hand, the potential on the read lines is continuously altered and the capacitive charging of the read line takes time, which slows the readout process.

The NDCDSR enables very low read noise and it stems from the fact that the read noise is small (due to very low level of interface generated $1/f$ and RTS noise) and because it is further possible to average out the overall read noise by performing multiple CDS measurements meaning that the MIG sensors offer very good energy resolution for very low energy X-rays originating e.g. from Lithium. The facts that the MIG sensors do not suffer from interface problems (no interface generated dark noise, very low level of interface generated $1/f$ and RTS noise, no image lag) means that MIG sensors are inherently tolerant to X-rays and electrons having energies below 300 keV. The lack of interface problems has also the additional benefit that it should enable very low noise detectors to be made from semiconductor materials (e.g. Germanium) having much worse interface quality than silicon, which is often not possible with other detector technologies since they suffer from interface issues.

2 Double modified internal gate field effect transistor detector

In the thick fully depleted BSI deep buried channel double MIGFET pixel the signal charge can be transferred back and forth between the two MIGs of the pixel. Both MIGFETs have a buried internal gate (MIG) implanted directly underneath their conducting channels. As can be seen from the cross-section on figure 1(b), Source 1 (S1), Gate 1 (Gate1), Drain 1 (D1) and MIG1 belong to the first MIGFET and Source 2 (S2), Gate 2 (Gate2), Drain 2 (D2) and MIG2 belong to the second MIGFET. Between these two MIGFETs there is a Transfer Gate enabling transfer of the stored signal charge between the two MIGs, which is necessary for the NDCDSR. One or preferably both nodes S1 and S2 are connected on separate vertical lines, which are connected to separate CDS readout circuits. The D1 and D2 can be both connected to the same vertical line or to a node, which is common to the whole pixel matrix. The Gate1, Gate2, and Transfer Gate nodes are connected to separate horizontal lines. The top view of the pixel is presented in figure 1(a).

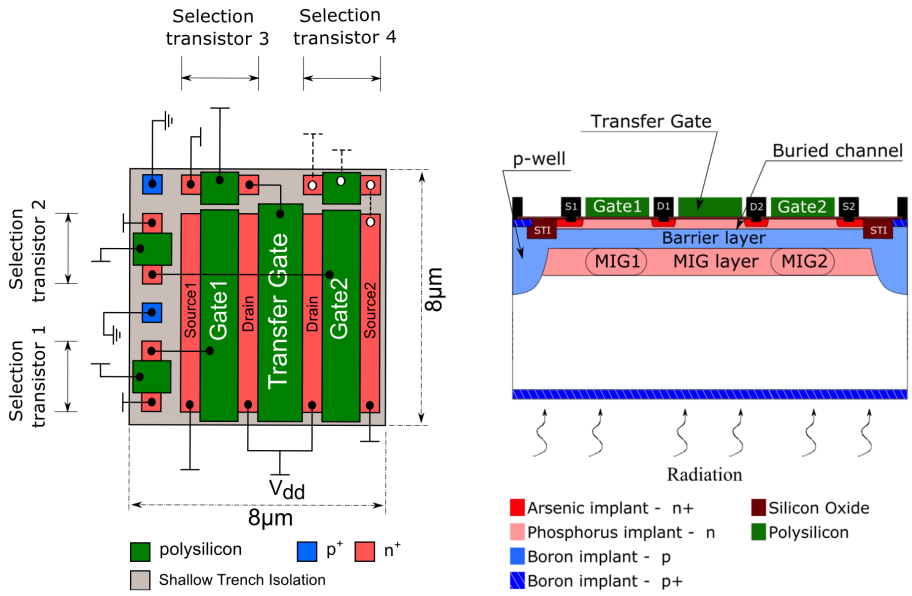


Figure 1. (a) Front side view of the Double MIGFET Detector wherein the four small transistors are optional selection transistors which can be utilised e.g. in order to create pixel specific reset. (b) Cross-section of the Double MIGFET Detector.

The pixel comprises a 50 μm thick fully depleted n^- type BSI silicon substrate and has dimensions of 8 by 8 μm^2. The front side of the device is manufactured utilizing a 0.18 μm or smaller minimum line width 5 V CMOS process. The only change that is required to the CMOS process is to adjust it to the lower substrate doping of high resistivity wafers (preferably 200 mm float zone wafers). The thinning of the wafer can be performed with TAIKO (a wafer back grinding process that uses a grinding method developed by DISCO) process [15] after which backside implantation, laser annealing, and chip sawing may be performed.

The upper part of the pixel (i.e. front side) comprises a stack of n-type buried channel and MIG layers in between of which there is a p-type barrier layer. It also has a Shallow Trench Isolation (STI) and a p-well surrounding the pixel. The p-well effectively reduces the crosstalk and prevents blooming. Besides, one can place n-type selection transistors into the p-well in order e.g. to enable pixel specific reset. There are additional n-type implants in the MIG layer beneath Gate1 and Gate2 referred to as MIG1 and MIG2 and used for the storing of signal electrons. In this design the p well is held always at 0 V, the D1 & D2 always at +5 V, the S1 & S2 always at +4.5 V, and the p^+ backside layer at −7 V. The operational range of the Gate1, Gate2, and Transfer Gate is from 0 V to +5 V.

3 Full 3D TCAD simulation study

The performance of the pixel has been studied by simulating operational steps. The 3D simulation results are obtained with the (Synopsys) TCAD software tool [16–18]. The first step is reset of the

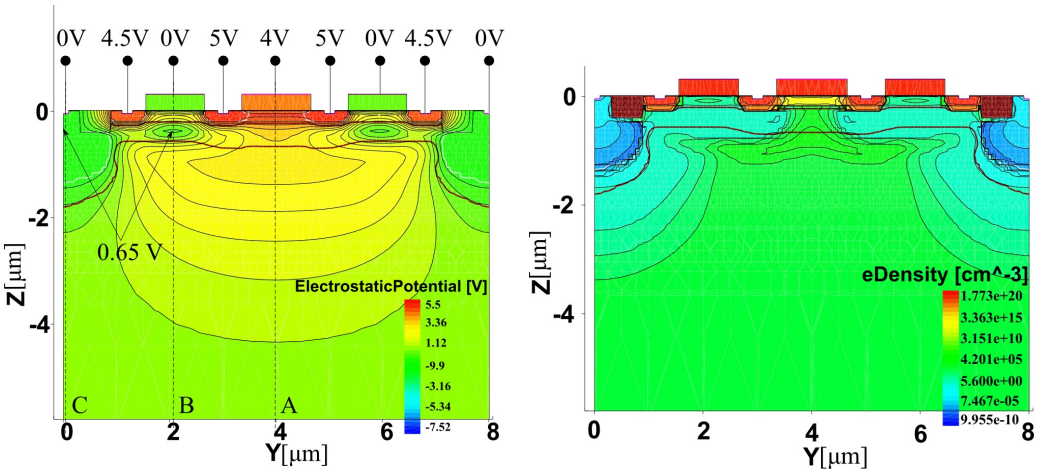


Figure 2. (a) Electrostatic potential distribution during reset on a 2D cross-section of a 3D simulation of the pixel structure. The potential curves on vertical cut lines A, B, and C are depicted on figure 3. (b) Electron density distribution during reset on a 2D cross-section of the 3D simulated pixel. There is no charge left in the MIGs.

pixel, when all the charge present in the pixel is removed. The second step is integration, when charge accumulates in the MIGs. The third step is the non-destructive CDS procedure comprising non-destructive charge transfer from one MIG to another in between non-destructive readouts. In this paper we present simulation results for the pixel at $-40°$C.

3.1 Reset

At first, the pixel reset operation is performed in order to remove any charge form the MIGs. The charge is removed into the nodes D1 and D2 by applying a reset potential configuration wherein the transfer gate is at $+4$ V ($+4.5$ V or $+5$ V could be equally well used) and nodes Gate1 and Gate2 are at 0 V. A two dimensional (2D) cross-section of the electrostatic potential distribution of the three dimensional (3D) simulation of the pixel in the reset potential configuration is shown in figure 2(a). Figure 2(b) represents the electron density distribution on the same cross-section. Electrostatic potential distribution on the vertical cut-lines A, B, and C indicated in figure 2(a) are presented in figure 3.

Based on figures 1 and 2(a) one can see that during reset there is no electrostatic potential barrier from the two MIGs (located underneath G1 and G2) towards the drain contact (D1 and D2) and thus complete and very fast reset is enabled. One can also deduce from figure 2(b) (and from 2(a)) that during reset electrons flow from the depleted substrate to the drains and that interface generated electrons do not flow into the substrate (there is a potential barrier that prevents electrons located at the interface or in the source, drain, or channel to enter into the substrate, MIG layer, or into the MIGs; this can also be deduced from the electrostatic potential distributions on cut-lines A and B presented in figure 3).

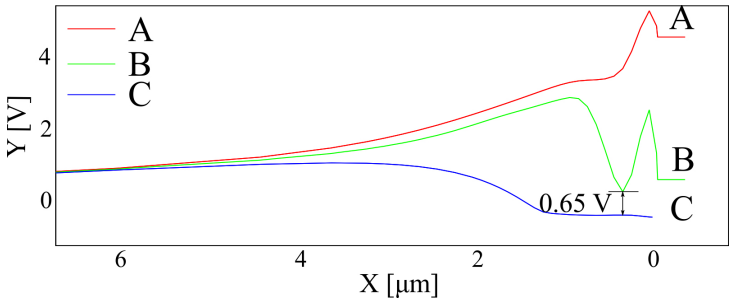


Figure 3. Electrostatic potential during reset on vertical cut-lines A, B, and C depicted on figure 2(a). No interface leakage current from the depleted gate oxide interface can enter into the MIG since there is a potential barrier between the channel and the MIG as can be seen from curve B. In curve B the potential difference between the potential minimum in the barrier layer and the p well is 0.65 V. The potential maximum on the right hand side of the barrier layer potential minimum is the buried channel and on the left hand side is the MIG. Afore described potential difference of 0.65 V means that at -40°C the barrier layer will be essentially depleted.

3.2 Integration

The reset of the pixel is followed by an integration period wherein the nodes Gate1 and Gate2 are simultaneously biased at $+1.5$ V and Transfer Gate is biased at 0 V (or alternatively at a slightly higher potential such as $+1$ V). The biasing of Gate1 and Gate2 nodes during integration is such that the channels underneath the gates are closed, i.e., the corresponding pixel row is not selected for readout.

In figure 4(a) the electrostatic potential distribution and in figure 5 the electron current distribution on a cross-section of the pixel is depicted at the end of the integration period. At this point 964 electrons are collected into the two MIGs (482 electrons in each MIG); the potential barrier from the MIG towards the drain contact is 0.74 V and the potential barrier in between the MIGs is 0.58 V. It can be deduced from figures 4(a) and 5 that the interface generated electrons are effectively prevented from entering into the MIGs and MIG layer. It can be also seen from figure 5 that there is a sufficient barrier between two pixels meaning that vertical anti-blooming mechanism is enabled.

3.3 Basic CDS measurement procedure

After the integration period and in the beginning of the readout period a readout potential configuration is first applied wherein the nodes Gate1 and Gate2 are at $+3.5$ V and the Transfer Gate is at 0 V. At this stage one can already measure with the first or second or both MIGFETs whether the pixel is in saturation and if so one could use the logarithmic dependence of the readout result to expand the dynamic range. The preferable way for readout in the proposed pixel is source current mode readout [19] wherein the value of the electric current at the source node is measured when all nodes of the pixel are held at fixed potentials as shown in figure 7(a).

Next a charge transfer procedure is applied to the pixel wherein 0 V is first applied to the Gate2. Then the Transfer Gate is set to $+2.5$ V — this potential configuration is referred to as the transfer stage, which is depicted in figure 6(a). Then the Transfer Gate is quickly set back to

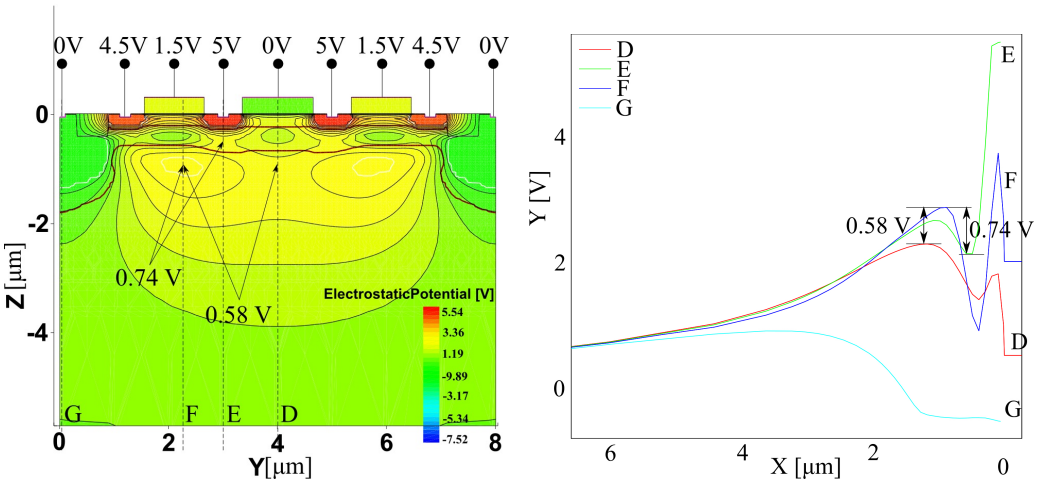


Figure 4. (a) Electrostatic potential distribution during integration on a 2D cross-section of the 3D simulated pixel when 964 electrons are located in the two MIGs (482 electrons in each MIG); the potential barrier from the MIG towards the drain is 0.74 V. The potential barrier between the two MIGs is 0.58 V. The potential curves on vertical cut lines D, E, F, and G are depicted on figure 4(b). (b) Electrostatic potential during integration on vertical cut-lines D, E, F, and G depicted on figure 4(a). The signal charges in the MIG have a much smaller barrier (0.74 V) towards the drain than towards neighbouring pixels (potential maximum of G subtracted from the local potential maximum of F at the depth of around 1 μm). This means that vertical anti-blooming mechanism is enabled, i.e., excess signal charges flow into the drain and not to neighbouring pixels (or to the source which would increase the noise).

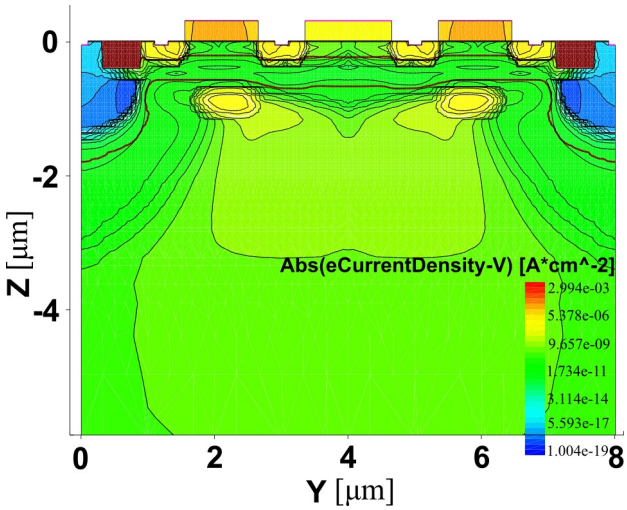
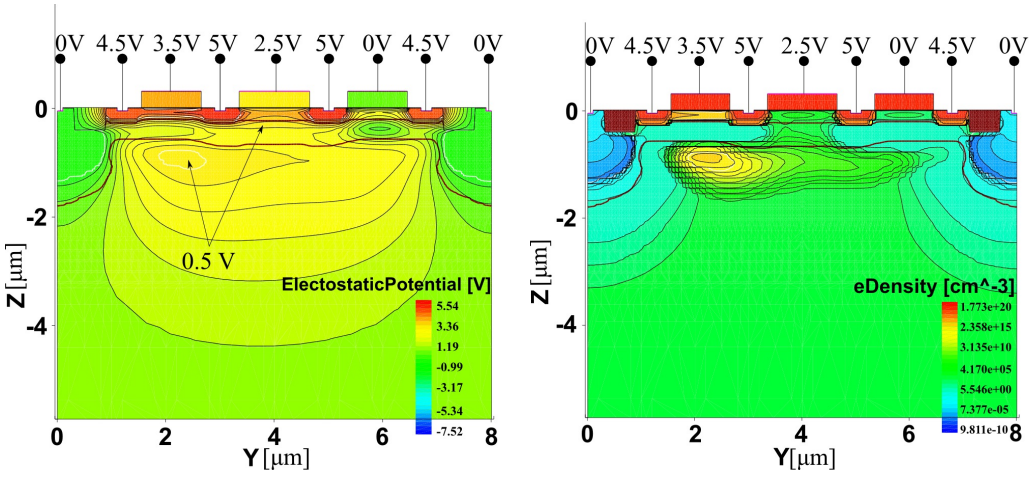


Figure 5. Electron current distribution during integration on a 2D cross-section of the 3D simulated pixel when 964 electrons are located in the two MIGs (482 electrons in each MIG). The interface leakage current is effectively prevented from entering into the MIG layer.



(a) (b)

Figure 6. (a) Electrostatic potential distribution in charge transfer potential configuration on a 2D cross-section of the 3D simulated pixel after signal charge electrons have been transferred to the left MIG. (b) Electron density distribution in charge transfer configuration after signal charge electrons have been transferred to the left MIG.

0 V, and finally the Gate2 is brought back to +3.5 V. At this stage the pixel is back to the readout potential configuration and all the 964 signal charge electrons are located in MIG1 as depicted on figure 7(b).

One can now perform the first part of the CDS procedure for the second MIGFET (located on the right hand side) by storing the readout result of the second MIGFET. Next the Gate1 is brought to 0 V, then +2.5 V is applied to the Transfer Gate, after which the Transfer Gate is brought back to 0 V, and finally the Gate1 is brought back to +3.5 V. The pixel is now back at the measurement stage but all 964 signal charge electrons are located in MIG2.

At this stage one can perform the second part of the CDS procedure for the second MIGFET by storing the readout result of the second MIGFET. The final CDS readout result for the second MIGFET is obtained by subtracting the first readout result from the second one (or vice versa). In our case it is $41.9\,\mu\text{A} - 40.5\,\mu\text{A} \approx 1.34\,\mu\text{A}$. The charge to current conversion gain is obtained by dividing $1.34\,\mu$A by 964 electrons resulting in 1.4 nA/e. It is important to note that during the CDS readout process of the second MIGFET all the potentials on the nodes of the second MIGFET remained fixed.

If desired one can perform during the second part of the CDS procedure for the second MIGFET also the first part of the CDS procedure for the first MIGFET by storing the readout result (obtained e.g. with different gain setting) of the first MIGFET. Then the Gate2 is brought to 0 V, next the Transfer Gate is set to +2.5 V after which it is brought back to 0 V, and then the Gate2 is brought back to +3.5 V after which one can perform the second part of the CDS procedure for the first MIGFET by storing the readout result of the first MIGFET. The final CDS readout result for the first MIGFET is obtained by subtracting the first readout result from the second one. If desired one can perform during the second part of the CDS procedure for the first MIGFET again

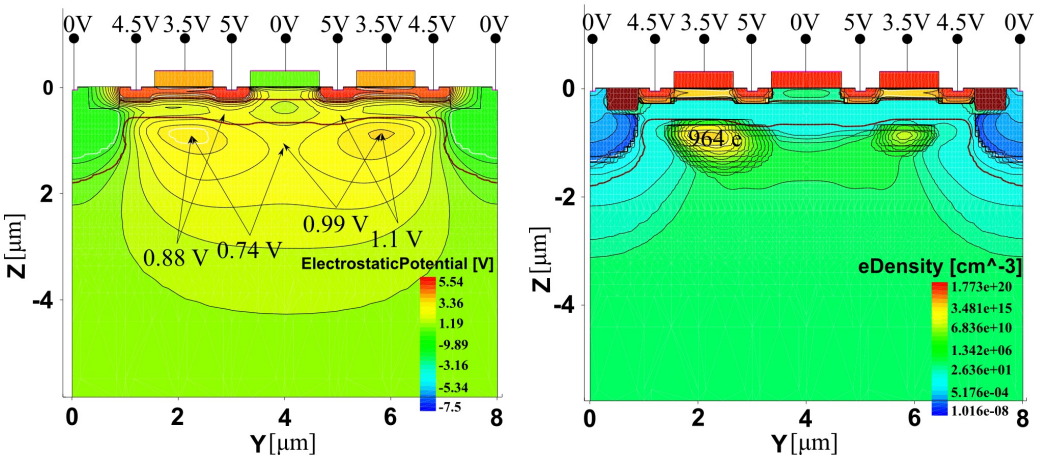


Figure 7. (a) Electrostatic potential distribution in the measurement potential configuration on a 2D cross-section of the 3D simulated pixel. The barrier from the MIG containing 964 electrons to the empty MIG is 0.74 V. The barrier from the MIG containing 964 electrons to the drain is 0.88 V. The barrier from the empty MIG to the full MIG is 0.99 V. The barrier from the empty MIG towards the drain is 1.1 V. (b) Electron density distribution in the measurement potential configuration on a 2D cross-section of the 3D simulated pixel. All the 964 signal charge electrons are located in MIG1.

the first part of the CDS procedure for the second MIGFET, i.e., one could sequentially perform as many CDS measurements as desired with both of the MIGFETs.

From the electrostatic potential distribution presented in figure 6(a) one can see that during the transfer stage there is no potential barrier from the energetically non-preferable MIG towards the energetically preferable MIG. The potential barrier from the energetically preferable MIG towards the drain contact is 0.5 V. The electron density distribution during the charge transfer is presented in figure 6(b) from which it can be deduced that all the 964 electrons are successfully transferred to the left MIG.

The electrostatic potential distribution during the measurement potential configuration when the 964 electrons are in the left hand side MIG is depicted in figure 7(a). The minimum potential barrier from the MIG having 964 electrons towards the drain contact is 0.88 V and the potential barrier from the MIG having 964 electrons to an empty MIG is 0.74 V.

4 Conclusions

The 8 μm pitch double MIG pixel structure designed for a slightly modified 0.18 μm or smaller line width 5 V CMOS process was presented and simulated in 3D. On the basis of this study, it is suggested for use in low light imaging as well as low energy X-ray applications. The reason is that the pixel does not suffer from interface issues (i.e. there is no interface generated dark noise, no interface generated image lag, and virtually no interface generated $1/f$ and RTS noise).

The reason for the lack of interface generated dark noise and image lag is due to the fact that in the simulated MIG pixel structure there is always a big enough potential barrier in between the signal charges and the depleted interfaces. The very low interface generated $1/f$ and RTS noise stems from the deep buried channel — the potential difference from the bottom of the buried channel to the interface is 0.45 V to 0.68 V throughout the length of the buried channel.

Furthermore the 50 μm thick fully depleted BSI pixel design offers several advantages such as 100% fill factor, high QE for NIR and visible light as well as low energy X-rays up to several keV, low crosstalk, anti-blooming, and very high readout speed. The last mentioned fact is due to the current mode readout as well as due to the fact that at reset and charge transfer stages there are no potential barriers hindering the signal charge transport.

The anti-blooming is due to the fact that the potential barrier for signal charges situated in MIG is always much lower towards the drain than towards the neighbouring pixels (and towards source node which is important from noise point of view) as can be seen from the cut-lines D, E, F, and G in figure 4(b). In the measurement and transfer potential configuration the signal charges are located underneath the gate biased at higher positive voltage than during integration and thus the anti-blooming protection is even better during other modes than during integration.

From the above results one can see that the transfer stage limits the Non-Destructive Correlated Double Sampling Full Well Capacity (NDCDSFWC) of the pixel, i.e., the maximum amount of signal charge that can be successfully stored, read out, and transferred from one MIG to another. The reason for this is that the barrier for signal charges located in the MIG to escape to drain or to an empty MIG is by far the smallest during the transfer stage. At the level of 964 signal electrons no charge loss was identified. The NDCDSFWC is estimated to be somewhere in between 1000 and 2000 electrons at -40°C which relates to (3.6 keV to 7.3 keV). This may seem limited but one should acknowledge that the pixel design is preliminary. If a larger pixel size is used and/or the pixel design is optimised according to the FWC it is possible to considerably increase the NDCDSFWC.

According to the 3D simulations the Charge Conversion Gain for 964 electrons at -40° Celsius is 1.4 nA per signal electron. The simulations also show that the thick fully depleted BSI MIG pixel design possesses considerably better spatial and energy resolution for low energy X-rays as well as better low light imaging capability than a previously simulated thin front side illuminated double MIG pixel structure [20].

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Publication II

Aurola, A., Marochkin, V., Golovleva, M., and Tuuva, T.
Novel silicon drift detector design enabling low dark noise and simple manufacturing

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Novel silicon drift detector design enabling low dark noise and simple manufacturing

A. Aurola,[a,b] **V. Marochkin**[a,b,*] **M. Golovleva**[b] **and T. Tuuva**[b]

[a]*Pixpolar,*
Tekniikantie 1, 02150, Finland
[b]*Lappeenranta University of Technology,*
P.O. Box 20, 53851, Finland

E-mail: Vladislav.Marochkin@pixpolar.com

ABSTRACT: The Silicon Drift Detectors (SDDs) have replaced simple diodes in demanding X-ray fluorescence applications like in element analysers capable of detecting light elements. The reason for this is that with similar collection area the SDDs have a much smaller output capacitance than diodes due to a much smaller anode size. Thus the SDDs provide much better Signal to Noise Ratio (SNR) at smaller signal levels than diodes. The small capacitance in SDDs is achieved by placing concentric rings around a miniature sized anode. These rings are biased such that inside the SDD's fully depleted bulk a radial electric field component is established guiding signal charges towards the anode.

Problems complicating the design of SDDs are positive oxide charge and interface dark noise. The latter is caused when leakage current generated at depleted interfaces mixes with the signal charge. It has been shown previously that by utilizing a chain of resistors connected to SDD's p+ drift rings and intermediate n+ rings both of these problems can be solved but the resistor chain arrangement requires an additional process step, which may not be standardly available. The interface generated dark noise and the requirement for a resistor chain can be removed by implementing suitable gaps in the p+ rings or with a resistive spiral as well as by implementing an additional anode for the collection of interface leakage current. Such SDDs are, however, vulnerable to accumulation of positive oxide charge complicating the manufacturing and likely reducing the effective lifetime of the detector.

We present an SDD design comprising a novel ring arrangement preventing the formation of interface dark noise, being resistant to positive oxide charge, and removing the need for a resistor

*Corresponding author.

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chain. In this work the design and operation principle of the proposed SDD is presented. The operation of the proposed SDD has been evaluated on TCAD with cylindrically symmetric 3D process and device simulations.

KEYWORDS: Solid state detectors; X-ray detectors; Radiation-hard detectors; Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc)

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4 Conclusions **11**

1 Introduction

The Silicon Drift Detector (SDD) was introduced first in 1984 by E. Gatti and P. Rehak [1]. The first satisfactory working devices were built in a collaborative effort by J. Kemmer at the Technical University of Munich, the Max Planck Institute in Munich, and the inventors (Rehak et al.) in 1985. They made the observation that the capacitance of the device is independent of the detector area, so that "very large area radiation detectors or photodiodes using this principle may have much improved noise performance when compared to traditional diode detectors". The first circular SDD, optimized for energy rather than position measurement, was described in 1985 by Rehak and Gatti et al. [2].

The early drift detectors used drift rings on both sides of the detector to produce the radial field. In 1987, Kemmer [3] introduced a design using a planar doping on one side and drift rings on the opposite side only. Such an SDD was easier to manufacture and provided a thin, unstructured homogeneous dead layer on the entrance side (backside radiation entry window). The manufacturability was further improved by introducing punch through biasing of the backside layer [4] removing the need to place a contact on the backside of the detector.

There are two basic problems related to the drift detectors which are the interface generated dark noise and positive oxide charge. Both of these problems can be removed with the SDD of figure 1 wherein a resistor chain arrangement is utilized for biasing the p+ drift rings and intermediate n+ rings. This biasing configuration ensures that the n+ rings are always reverse biased when compared to the neighbouring p+ rings. The n+ rings collect the interface generated electrons. The proper biasing of the n+ rings prevents electron injection from the n+ rings into the substrate as well as hole current flow from one p+ ring to another. The latter feature ensures proper operation of the resistor chain and the former one prevents the formation of interface generated dark noise. Important design aspects are the separation of the p+ rings, the size of the n+ ring, the voltage drop across individual resistors, the resistivity of the substrate, and to some extent also the amount of positive oxide charge. Particularly, a relatively large reverse bias must be applied between the n+ and the neighbouring p+ rings in order to prevent electron flow from the n+ ring to the substrate as well as hole flow from one p+ ring to another.

In addition in the SDD of figure 1 it is important to utilize a large enough reverse bias between the innermost p+ ring and the n+ anode for three different reasons. Firstly, it is important to prevent punch-through hole current flow from the innermost p+ rings to a backside p+ layer. Secondly, it is important to avoid radiation-induced electrons being absorbed by the innermost n+ rings. Thirdly, the relatively high reverse bias between the n+ and p+ rings results in an undulating potential profile reaching relatively deep inside the substrate causing problems close to anode where radiation-induced electrons are transported relatively close to the front surface. With the aid of a large enough reverse bias between the anode and the innermost p+ ring the radiation induced electrons can be pushed next to the anode deeper into the substrate wherein the undulating potential profile has no effect.

Another procedure to mitigate problems related to undulating potential profile next to anode is to utilize a larger drift field (i.e. higher potential difference between adjacent p+ rings) close to the anode than in areas located further away from the anode. Directly beneath the anode the high reverse bias between the innermost p+ ring and the anode complicates the vertical transport of the radiation-induced electrons towards the anode, which can be overcome by providing a large enough anode.

The relatively high reverse bias between the p+ and n+ rings means that the dead volume, i.e. the region from which the n+ rings collect radiation induced electrons, reaches relatively deep into the high resistivity substrate (roughly to the width of the n+ ring) resulting in the formation of a relatively large low drift field region at the border of the dead volume underneath the n+ rings. This fact increases the amount of split events enlarging somewhat the Full Width at Half Maximum (FWHM) of the X-ray peaks except for low energy X-rays. In a split-event an X-ray is absorbed in the low drift field region and part of the X-ray induced electrons are collected by an n+ ring and another part by the anode. Before the introduction of the large area radiation entry window on the backside [3] the relatively large low drift field region at the front side corresponding to gaps in the p+ doping used to increase somewhat also the FWHM of higher energy X-rays beside severely impairing the FWHM of low energy X-rays.

By reducing the separation between the p+ rings problems related to the undulating potential profile and the dead volume could be mitigated. This means, however, that inside the substrate there is a higher risk for punch-through current flow from one p+ ring to another unless reasonably high reverse bias is applied between the n+ ring and the neighbouring p+ rings. On the other hand, in case the separation between the p+ rings is reduced the width of the n+ rings should be also diminished but this is challenging from manufacturing point of view in case contact aligner is utilized in the manufacturing process.

A fact is that the X-rays and high-energy particles increase the amount of positive oxide charge. The bigger the amount of positive oxide charge is and the larger the reverse biases between the n+ and p+ rings as well as between the anode and the innermost p+ ring are, the larger is the maximum electric field value at the interface. If the maximum electric field at the interface exceeds a certain manufacturing process dependent limit then avalanche breakdown is resulted in limiting the lifetime of the detector. Thus the SDD structure of figure 1 needs to be designed and manufactured carefully in order to guarantee long lifetime in X-ray and/or particle detection applications. One way to reduce the effect of the build-up of positive oxide charge is to utilize a large area p spray implant on the front side of the SDD.

In the SDD of figure 1 an extra process step is required for the realization of the resistor chain that may not be standardly available in the manufacturing facility. The resistor chain (as well as the n+ rings) can be avoided in the SDD of [5] wherein the p+ drift rings comprise gaps as depicted in figure 9 in [5]. The positive oxide charge in these gaps enables the formation of electron "rivers" next to the interface, i.e., due to the positive oxide charge there is a potential minimum for electrons at the oxide interface in the gaps of the p+ drift rings as well as in between adjacent p+ drift rings. The gap in the p+ drift ring allows interface generated electrons to move in these electron "rivers" towards an additional anode situated in between the two innermost p+ drift rings (the innermost p+ drift ring does not comprise a gap). The additional anode collects all the interface-generated electrons except the ones generated in between the anode and the innermost p+ drift ring reducing thus very much the interface generated dark noise.

The interface and part of bulk generated holes are collected by the p+ rings and are transported from one p+ ring to another towards the outermost p+ ring in electron potential barriers located underneath the space in between adjacent p+ rings, i.e., the punch-through effect between the p+ drift rings can be exploited since there is resistor chain. The formation of afore said electron potential barriers depends on the amount of positive oxide charge, on the separation between the p+ drift rings, and on substrate doping concentration. As already previously explained the barriers prevent also interface-generated electrons from flowing into the substrate if they can be removed e.g. with afore said "electron river" approach.

The benefits of the SDD design of [5] are that no resistor chain is required, that the dead volume is smaller, and that the undulating potential profile underneath the rings is less severe than in the case of the structure presented in figure 1. The design of [5] is, however, highly dependent on the amount of positive oxide charge in the gaps piercing the p+ drift rings and in between the p+ drift rings. This is likely to complicate the manufacturing, to lower the yield, and to reduce the effective lifetime of the detector.

Instead of using gaps in the p+ rings one could alternatively use a p doped spiral wherein the p spiral itself acts as a resistor providing thus a potential gradient inside the p ring and consequently also outside the p spiral. In this design the interface generated electrons are flowing at the interface next to the p spiral towards an additional anode collecting interface-generated electrons. The benefit of the design is that the resistor chain is avoided but on the other hand the design is very much dependent on the amount of positive oxide charge at the interface next to the p spiral. Consequently further away from the anode the radiation-induced electrons would flow radially towards the anode but close to the anode, depending on the amount of positive oxide charge, the radiation-induced electrons would be prone to follow a spiral path. Since the build-up of positive charge during manufacturing and in use cannot be well controlled and since this spiral device is highly dependent on positive oxide charge the design is likely to have manufacturing issues, low yield, and reduced lifetime.

The novel SDD structure presented in section 2 prevents the formation of interface generated dark noise, is not sensitive to the amount of positive oxide charge, avoids the use of a resistor chain, enables simple manufacturing with standard process steps, does not suffer from an undulating potential profile inside the substrate, and is insensitive to the width of the rings.

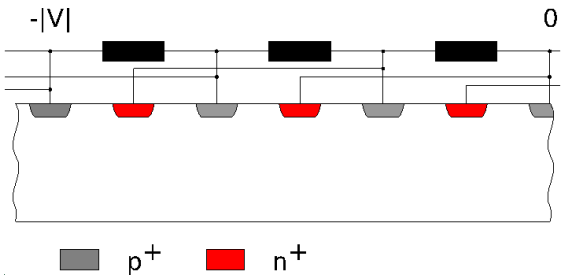


Figure 1. A typical SDD ring arrangement utilizing a resistor chain for the biasing of the p+ and n+ rings. The p+ rings act as drift rings and collect interface generated and radiation-induced holes. The purpose of the n+ rings is to collect interface generated electrons.

2 Modified silicon drift detector structure

The cross-section of the SDD ring structure and anode of the proposed modified SDD structure is presented in figure 2 excluding the edge area. The front side of the modified SDD is presented in figure 3 comprising also a possible edge configuration. In figure 3 the n+ area in the upper left corner is used for contacting a neutral area next to the detector edge and the p+ area in the lower left corner is used for contacting the backside p+ area via punch-through effect. The cross-section of the other half of the modified SDD equipped with a standard edge configuration is presented in figure 4. The leftmost n+ node (at V_6) contacting the neutral area next to the detector edge is biased at a slightly more positive potential than the potential would be in case the neutral area would be floating. In this manner the edge generated electrons are collected by the leftmost n+ node and not by the n+ anode (at V_5), i.e., there is no edge generated dark noise, while at the same time the depleted edge area and thus the edge generated leakage current will be kept at a relatively small level.

In figure 5 an alternative edgeless detector configuration [6] optimised for pixelated detectors is presented avoiding the formation of edge-generated electrons. The edge is covered with insulator and conductor layers and by biasing the conductor layer at a sufficiently low potential an inversion layer of holes is realised beneath the insulator layer preventing the formation of interface generated dark noise and enabling the biasing of the backside p+ layer.

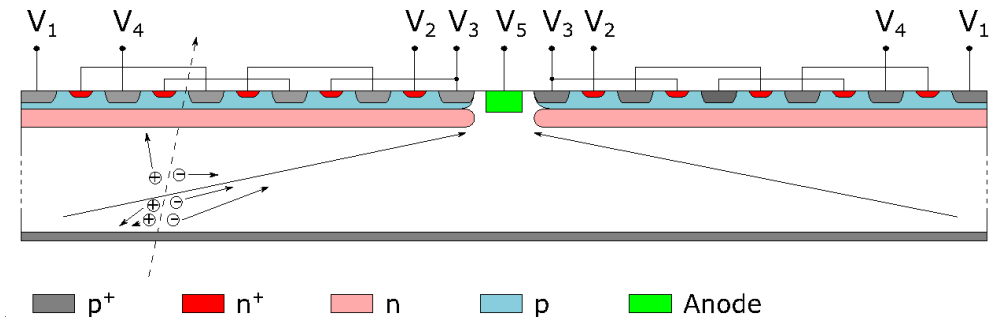


Figure 2. Schematic cross-section of the novel modified SDD.

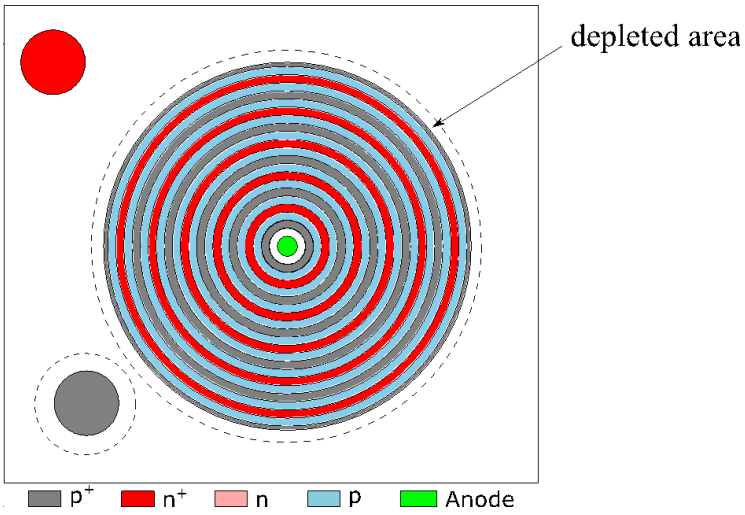


Figure 3. Schematic layout of the SDD structure including also the edge area. The cross-section of the area comprising the SDD rings is presented at figure 2. In the upper left corner of the detector chip there is an n+ node contacting a neutral area next to the detector edge (see also figure 4 and corresponding explanation). In the lower left corner of the detector chip there is a p+ node for punch-through biasing of the backside p+ layer.

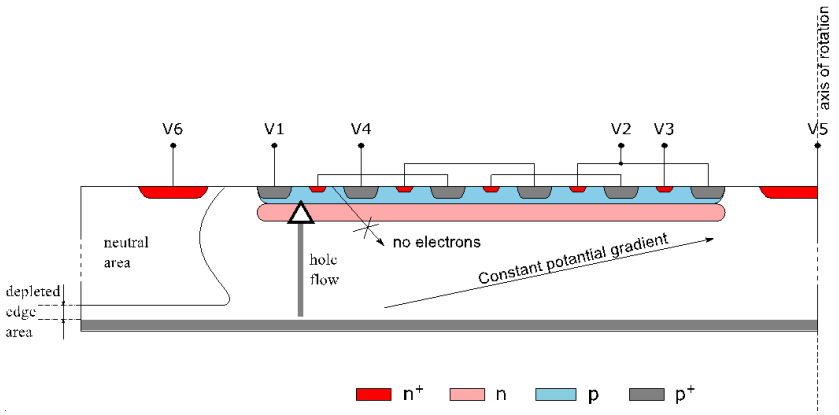


Figure 4. A modified SDD structure comprising a standard edge design. SDD operation is established by biasing properly the nodes at V_1, V_2, V_3, and V_5. The potential at the second outermost p+ ring (at V_4) is monitored in order to avoid electric break down. The n+ node (at V_6) contacting the neutral area next to the detector edge is biased at a slightly more positive potential than the potential would be in case the neutral area would be floating.

As usual on the backside of the modified SSD in figure 2 there is a thin large-area p+ type doping functioning as a homogeneous radiation entry window which is preferably biased from the front side with the punch through biasing scheme [4]. On the front side of the device there is a large area deep low dose n type implanted layer and a large area shallower and higher dose p type implanted layer. These n and p type large area layers are preferably implanted with the same mask.

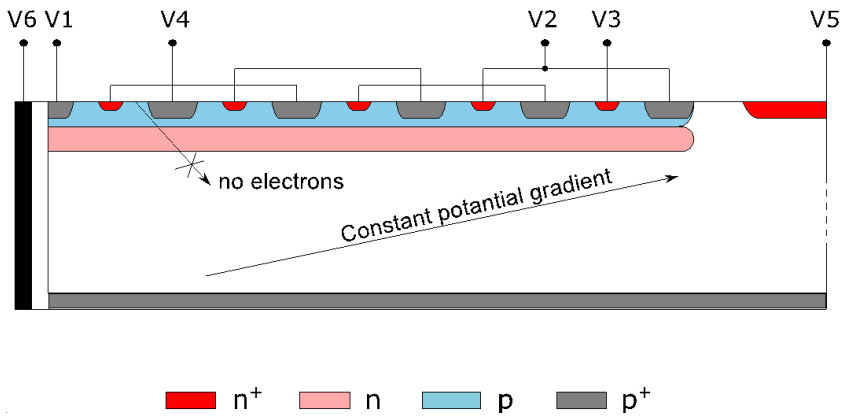


Figure 5. An edgeless modified SDD structure comprising an insulator conductor stack at the detector edge. A sufficiently negative potential on the conductor layer (at V_6) results in an inversion (or accumulation layer) of holes at the interface beneath the insulator preventing the formation of interface generated dark noise and enabling the biasing of the backside p+ layer.

Besides on the front side there are alternative p+ and n+ type rings surrounding the anode. The n+ rings act as gates of very large concentric JFETs (Junction Field Effect Transistor). The p+ rings act as sources and drains of the very large concentric JFETs — the wording very large concentric JFET is utilised to highlight that standard JFETs are much smaller in size. The parts of the p layer situated underneath the n+ rings form the channels of the very large concentric JFETs. The role of the deep n layer is to vertically confine the p layer particularly at the location of the channel. Close to the anode the deep n layer prevents also unwanted punch-through hole current flow from the front side p layer to the backside p+ radiation entry window. In addition close to the anode the p layer functions also as a potential barrier preventing radiation-induced electrons from being absorbed by the innermost n+ rings.

Excluding the two outermost p+ rings the p+ rings are connected to an n+ ring of larger radius in such a manner that in between these interconnected p+ and n+ rings there is always one intermediate p+ ring and one intermediate n+ ring as depicted in figure 2. This means that the electric potential of the intermediate p+ ring is always one JFET channel threshold voltage V_{th} (or slightly less) smaller than the electric potential of the interconnected p+ and n+ rings inclosing the intermediate p+ ring. Consequently, the electric potential of the interconnected rings reduces at steps of V_{th} towards the outer rim of the detector resulting in a horizontal drift field inside the substrate. The two outermost p+ rings do not have an n+ ring to be interconnected with. It is beneficial to have an electric contact on the second outermost ring that can be monitored externally. The anode is marked with green colour in figure 2 because it could be replaced e.g. with a Modified Internal Gate (MIG) readout transistor [7].

The SDD ring structure of figure 2 is operated by first biasing all the nodes (V_1, V_2, V_3, and V_4) of the SDD ring structure at the same potential. Next a suitable reverse bias is applied in between the anode (at potential V_5) and all the nodes of the SDD ring structure. Then the potential of the innermost n+ ring (V_2) is biased such that the channel underneath is slightly conductive, i.e., the source to gate biasing of the innermost JFET is set close to threshold bias. Next a decreasing

negative potential is applied to the node V_1 while the potential at V_4 is monitored. The negative potential at V_1 is decreased as long as the potential at V_4 is at around the same potential than V_1. At the onset when the potential at V_4 starts to be less negatively biased than V_1 one should stop decreasing the potential V_1 or to adjust V_1 at a value around V_{th} smaller than the potential at V_4. In case the potential at V_1 is further reduced there will be a too big voltage difference between the outermost n+ ring and the outermost p+ ring and the device will break, i.e., at some point the drain to gate bias of the outermost JFET would exceed the breakdown voltage.

Ideally the biasing of the backside p+ layer is punch-through biased from the front side by a separate large area p+ contact located outside the SDD ring structure e.g. in one corner of the modified SDD chip. In addition, punch-through hole current should be prevented from flowing either from the innermost p+ rings to the p+ backside layer or from the p+ backside layer to the p+ rings. This can be achieved by choosing properly the doping of the large area deep n layer, by adjusting properly the size of the anode, the distance in between the anode and innermost p+ ring, the reverse bias between the anode and innermost p+ ring, as well as by adjusting the substrate doping, the wafer thickness, the amount of concentric JFETs with respect to V_{th}, and the bias of the backside p+ layer.

In order for the arrangement to work it is crucial that the innermost n+ ring is biased such that a hole current will run from the innermost p+ ring through the channel beneath the innermost n+ ring to the second innermost p+ ring and onwards towards the outermost p+ ring biased at V_1. This current will ensure proper biasing of the SDD ring structure — without it the proposed SDD ring structure would likely break due to the build-up of a too high reverse bias between some of the SDD rings. Afore said current is somewhat analogous to air blown into an inflatable boat for the sake of providing necessary rigidity.

The purpose of the biasing of the SDD's electrodes (and the backside p+ layer) is first of all to fully deplete the semiconductor body underneath the SDD rings and secondly to create a necessary radial drift field transporting radiation-induced electrons towards the anode as depicted in figure 2. The p+ rings and the backside p+ layer collect the radiation-induced and interface generated holes. The n+ rings collect the interface-generated electrons and thus the generation of dark noise at depleted interfaces is prevented except in the area next to the anode.

In the substrate beneath the deep n layer there is no undulating potential profile in the modified SDD. Instead a constant radial drift field is established in the substrate at relatively small distance from the deep n layer. This stems from the facts that in a p type JFET the electric potential of a conductive p channel is always around the same or smaller than the potential of the p+ source, that the drain is more negative than the source, and that the drain acts as the source of the next JFET situated further away from the anode. On the other hand, the pn junction between the conducting p channel and the deep n layer forms a potential barrier for radiation-generated electrons drifting in the substrate preventing them from being absorbed by the innermost n+ rings. The very same barrier prevents also punch-through hole current flow from the innermost p+ rings towards the p+ backside layer. These aspects enable the radiation-induced electrons to drift next to anode relatively close to the innermost p+ ring meaning that a relatively small reverse bias can be applied between the anode and the innermost p+ ring enabling also a relatively small anode size.

In the modified SDD the maximum reverse bias between the n+ and p+ rings is $2 \times V_{th}$, which is relatively small. Besides, the reverse biased pn junction between the conducting p channel and the n+ rings collecting the interface generated electrons acts as potential barrier for electrons lo-

cated in the n+ rings preventing them from flowing into the substrate. Furthermore, in the modified SDD the biasing of the n+ and p+ rings is not dependent on the amount of positive oxide charge since the potential distribution of the SDD rings is defined by the JFET threshold voltage V_{th} which is not affected by the positive oxide charge but by the p type channel doping beneath the n+ ring as well as by the deep n layer and n type substrate doping. The reason is that the n+ ring situated in between the channel and the interface shields the channel from the influence of the positive oxide charges located at the interface above the n+ ring.

The facts that relatively small reverse biases between the anode and the innermost p+ ring as well as between the n+ and p+ rings may be utilised, that the operation is not affected by positive oxide charge, and that the formation of interface generated dark noise is prevented mean that the modified SDD should be relatively radiation hard. Yet another feature is that the width of the n+ or p+ rings does not play any crucial role in the modified SDD and can be thus chosen freely in different parts of the SDD (e.g. smaller width can be utilized close to anode).

In the proposed novel modified SDD altogether 4 electrodes (V_1, V_2, V_3, and V_4) are required for the biasing of the ring configuration whereas only 2 are required in the conventional SDD of figure 1. In the modified SDD no resistor chain is, however, needed and it can be manufactured with standard process steps — beside the n+ and p+ regions only one additional implant mask is required for the large area p and n implanted layers.

3 TCAD simulation study

The simulated modified SDD structure is presented in figure 6. Only half of the structure is needed for 3D simulations since the device is cylindrically symmetric — the rotation axis is depicted in the figure. The width of the p+ drift ring is 5 μm, the width of the n+ ring acting as the gate is 2 μm, and the gap between the p+ and n+ rings is 2 μm. The radius of the n+ anode doping (n6) is 10 μm and the gap between the innermost p+ drift ring (p6) and the anode is 5 μm. The simulated device comprises an n- type 300 μm thick silicon substrate having a resistivity of 2 kΩcm. The effect of the fixed charge at the Si/SiO_2 interface is taken into account by defining an oxide charge concentration as 1e11 cm^{-3}.

The electrostatic potential distribution in the modified SDD is presented in figure 6a and a magnification of the upper part of the device is presented in figure 6b. Electrostatic potential curves along vertical cutlines 1–11 of figure 6b are presented in figure 7 and electrostatic potential curves along the horizontal cutlines A and B of figure 6b are presented in figure 8. The horizontal cutline A intersects the n+ and p+ rings whereas the horizontal cutline B intersects the channel.

Based on figures 7 and 8 one can see that a constant radial drift field is established inside the substrate guiding signal charges towards the anode, i.e. an undulating potential profile is avoided. The electron current distribution on the cross-section of the modified SDD is presented in figure 9 based on which one can see that no interface-generated electrons are collected by the anode, i.e., there is no interface-generated dark noise in the simulated SDD structure.

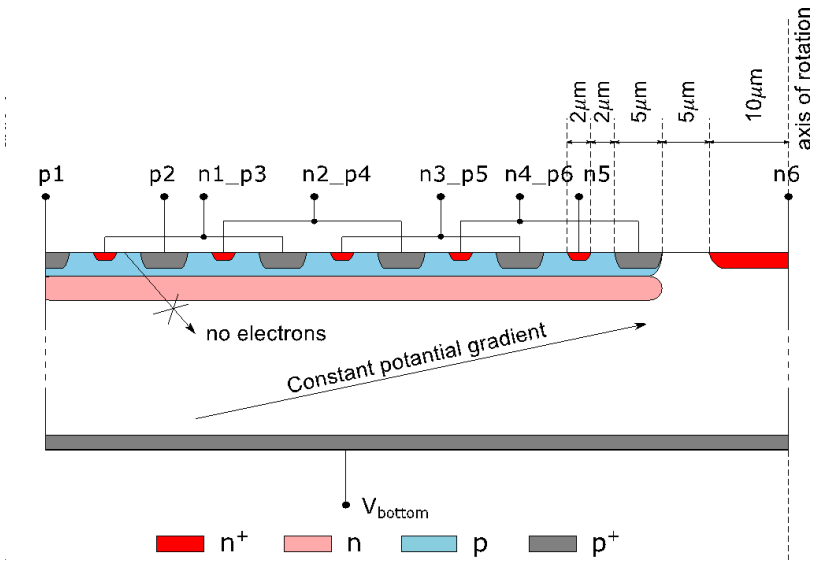
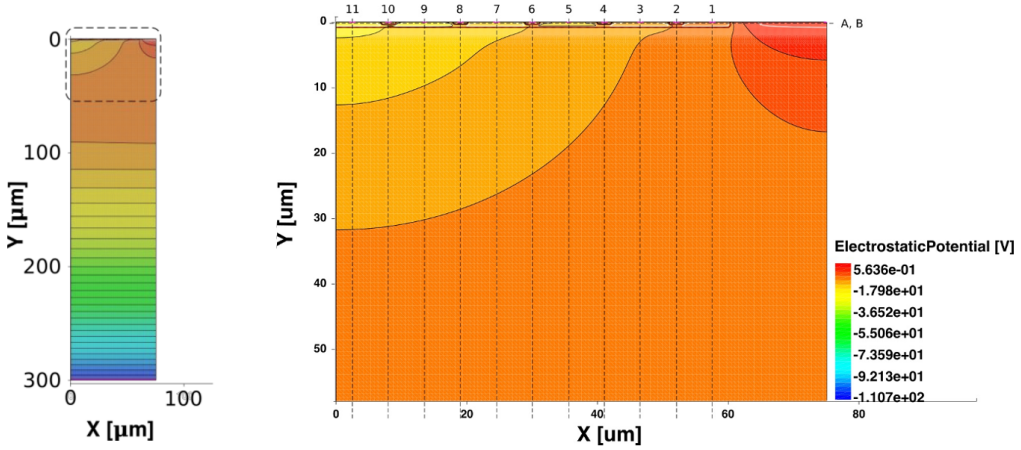


Figure 6. Schematic cross-section of the simulated cylindrically symmetric SDD. The rotation axis is depicted in the figure. Contacts p2, n1_p3, n2_p4, n3_p5 are not biased.



(a) (b)

Figure 7. (a) The electrostatic potential distribution on a cross-section of the simulated fully depleted SDD structure. (b) A magnification of the upper part of the figure 7a. Vertical cut-lines numbered from 1 to 11 are depicted in the figure 8. The horizontal cut-lines A and B are marked with one line only since the distance between the lines is very small. The horizontal cut-line A intersects the n+ and p+ rings whereas the horizontal cut-line B intersects the large area p type implanted layer along the conducting channels. The potential profiles on the cut-lines A and B are depicted in figure 9.

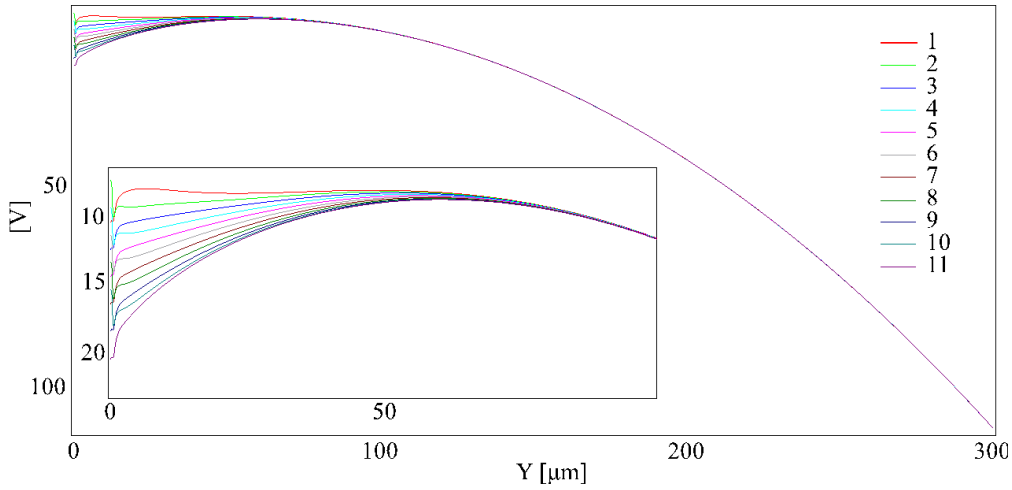


Figure 8. Electrostatic potential distribution on vertical cut-lines 1–11 depicted in figure 7b. A horizontal drift field is established inside the substrate due to the gradually diminishing potential of the p+ rings.

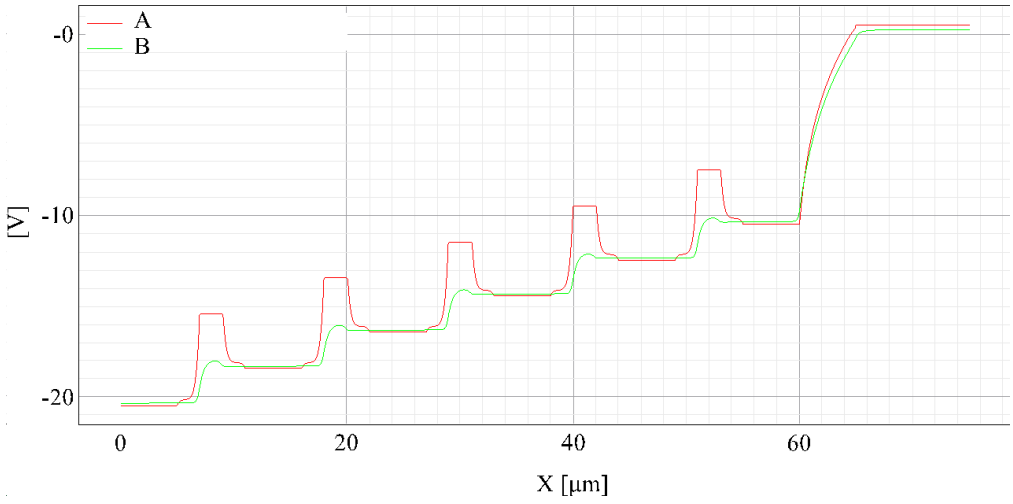
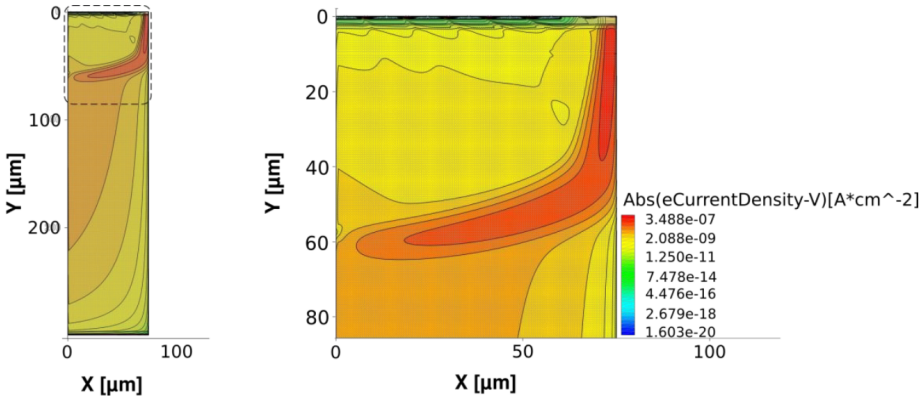


Figure 9. The horizontal cut-line A of figure 7b intersects both n+ and p+ rings and one can see from the corresponding potential profile that Vth of a concentric JFETs is around 2 V and that the potential of the n+ rings as well as of the p+ rings diminishes gradually towards the outer rim of the SDD. The horizontal cut-line B of figure 7b intersects the large area p type implanted layer along the channels and one can deduce from the corresponding potential profile that the channel and the source are approximately at the same potential, i.e., no undulating potential profile is established in the substrate underneath.



(a) (b)

Figure 10. (a) Electron current distribution on the cross-section of the simulated modified SDD structure. (b) Magnification of the upper part of figure 10a indicating that no interface-generated electrons are collected by the anode.

4 Conclusions

The simulated proposed modified SDD structure comprises only a small amount of rings surrounding the anode but it is sufficient to prove that the concept functions as intended. The proposed SDD has the advantages that no resistive chain is required, that the formation of interface dark noise is prevented, that the operation is not sensitive to positive oxide charge, and that it should be relatively radiation hard. It should be also possible to utilise the proposed ring structure in detectors that are made from other semiconductor materials than Silicon like e.g. Germanium.

One should note that by incorporating similar large area p and n layers one should be able to provide largely the same benefits than with the proposed modified SDD albeit with the cost of an extra manufacturing step required for the formation of the resistive chain.

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Publication III

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A radiation detector design mitigating problems related to sawed edges

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A radiation detector design mitigating problems related to sawed edges

A. Aurola,[a,b] **V. Marochkin**[a,b,1] **and T. Tuuva**[b]

[a] *Pixpolar,*
Tekniikantie 1, 02150, Finland
[b] *Lappeenranta University of Technology,*
P.O. Box 20, 53851, Finland

E-mail: Vladislav.Marochkin@pixpolar.com

ABSTRACT: In pixelated silicon radiation detectors that are utilized for the detection of UV, visible, and in particular Near Infra-Red (NIR) light it is desirable to utilize a relatively thick fully depleted Back-Side Illuminated (BSI) detector design providing 100% Fill Factor (FF), low Cross-Talk (CT), and high Quantum Efficiency (QE).

The optimal thickness of such detectors is typically less than 300 μm and above 40 μm and thus it is more or less mandatory to thin the detector wafer from the backside after the front side of the detector has been processed and before a conductive layer is formed on the backside. A TAIKO thinning process is optimal for such a thickness range since neither a support substrate on the front side nor lithographic steps on the backside are required. The conductive backside layer should, however, be homogenous throughout the wafer and it should be biased from the front side of the detector.

In order to provide good QE for blue and UV light the conductive backside layer should be of opposite doping type than the substrate. The problem with a homogeneous backside layer being of opposite doping type than the substrate is that a lot of leakage current is typically generated at the sawed chip edges, which may increase the dark noise and the power consumption. These problems are substantially mitigated with a proposed detector edge arrangement which 2D simulation results are presented in this paper.

KEYWORDS: Solid state detectors; X-ray detectors; Photon detectors for UV, visible and IR photons (solid-state) (PIN diodes, APDs, Si-PMTs, G-APDs, CCDs, EBCCDs, EMCCDs etc); Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc)

[1] Corresponding author.

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4 Examples of other detectors incorporating the proposed edge structure 7

5 Conclusions 9

1 Introduction

In pixelated silicon radiation detectors that are utilized for the detection of UV, visible, and Near Infra-Red (NIR) light it is desirable to utilize a relatively thick fully depleted Back-Side Illuminated (BSI) detector design. The benefit of the BSI configuration is that structures on the front side such as conductors do not absorb light thus enabling 100% Fill Factor (FF). The advantages of the fully depleted configuration are considerably reduced Cross-Talk (CT) due to lack of diffusion and improved Quantum Efficiency (QE) due to lack of recombination.

The thicker the fully depleted detector the better is the QE for NIR light. However, the thicker the fully depleted detector the more dark current is generated in the depleted bulk (which can be, however, mitigated by cooling), the bigger bias at a conductive backside layer is required to fully deplete the bulk, and the bigger is the CT particularly at the boundary of the pixel matrix. Thus there is an optimal detector thickness depending mainly on the optics, the magnitude of the bias on the conductive backside layer, and the pixel size.

In case the detectors should be thinner than 300 μm thick it is more or less mandatory to thin the detector wafer from the backside after the front side of the detector has been processed and before the conductive layer is formed on the backside. One option is to bond the front side of the detector wafer to a support wafer. The problem is, however, that it is not trivial to reach the contact pads located on the front side of the detector wafer especially if the detector is thicker than 40 μm. This problem can be avoided in TAIKO thinning process since no support wafer is required but the detector thickness must be at least 40 μm. The TAIKO process is a wafer back grinding method developed by DISCO. The difference to conventional back grinding is that the TAIKO process leaves an edge (approximately 3 mm) on the outer most circumference of the wafer and thin grinds only the inner circumference. The TAIKO process has, however, the problem that lithographic steps cannot be performed on the backside of the detector wafer. This means that the conductive backside layer must be homogenous throughout the wafer and that the contact to the conducting backside layer needs to be placed on the front side of the detector.

In order to provide good QE for blue and UV light the conductive backside layer should be as thin as possible and it should be of opposite doping type than the substrate (an inversion layer

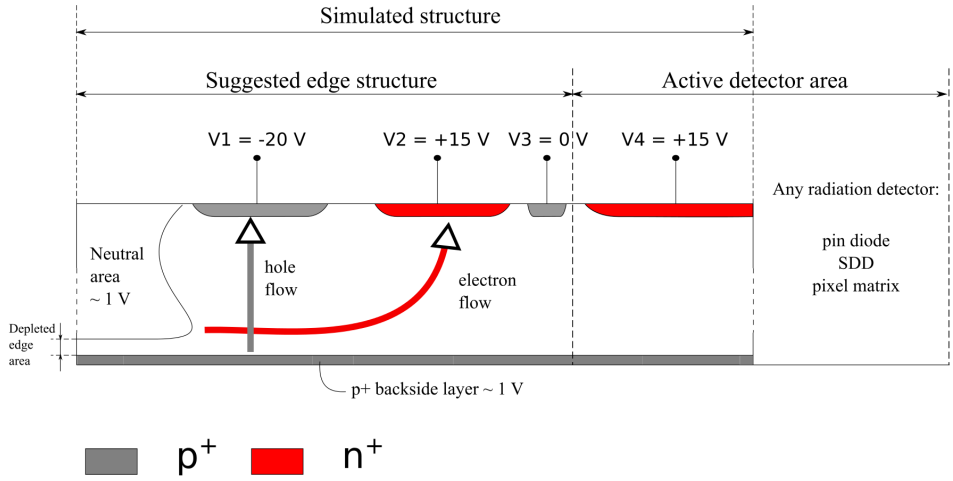

Figure 1. A schematic drawing of the proposed detector edge structure (the potential values correspond to simulations). The floating neutral area next to the edge minimizes the depleted edge area. The outermost p^+ ring (at V_1) is used for punch-through biasing of the backside p^+ layer and for depleting the detector bulk. The n^+ ring at V_2 is used for the collection of edge-generated electrons in particular. The p^+ ring at V_3 is used to isolate the active detector area (at V_4) from the n^+ ring at V_2 and from edge generated electrons.

is generally not an option due to the relatively thick fully depleted substrate). Beside the use of TAIKO process it is hereby assumed that the detector chips are separated from the wafer by sawing which is a standard procedure in chip manufacturing. The problem with afore described arrangement is that it is difficult to bias the conductive backside layer from the front side. Another problem is typically that a lot of leakage current is generated at the sawed chip edge, which may increase the dark noise and the power consumption.

In this paper we present 2D simulation results of a thick fully depleted BSI detector chip arrangement that is obtained with the TAIKO thinning procedure, that has a conductive backside layer on an oppositely doped wafer and that has less problems related to the sawed edges. The key aspect of the detector edge design is to maximise the neutral area on the chip edges.

2 Concept

A cross-section of the simulated edge arrangement of the thinned detector is presented in figure 1 wherein the detector arrangement surrounded by the proposed edge area corresponds to a standard diode detector. The front view of the detector of figure 1 is presented in figure 2. The processing of a thinned detector structure that is not bonded to a support wafer necessitates that no lithographic steps can be performed after thinning. Therefore a maskless p^+ implant is deployed on the backside of the detector's n type high resistivity substrate. The combination of oppositely doped substrate and conductive backside layer is utilised in order to achieve high QE for blue light. This complicates, however, the design since the biasing of the backside layer needs to be performed from the front side and one cannot simply bias the backside through a neutral substrate of opposite doping type (if the backside layer and the substrate were of the same doping type one could bias the back-

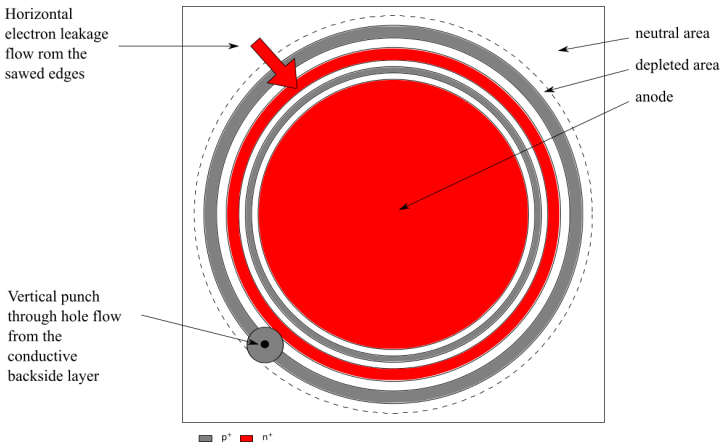

Figure 2. Top view of the detector presented in figure 1 comprising the proposed edge structure.

side layer through a neutral substrate). A preferable way to achieve the biasing of the conductive backside layer is to use punch-through biasing as explained in [1].

The punch-through biasing is achieved with the outermost p^+ ring (at potential V_1) — when a large enough reverse bias is applied to this p^+ ring the depletion region in the n^- bulk around the p^+ ring will extend to the backside p^+ layer. At even larger reverse bias values the potential of the p^+ backside layer will follow the p^+ layer resulting in punch-through biasing of the p^+ backside layer. When the potential of the p^+ backside layer starts to follow the potential of the outermost p^+ ring the junction between the p^+ backside layer and the n^- substrate starts to be reverse biased everywhere else than beneath the outermost p^+ ring. Consequently a sufficiently large reverse bias applied to afore said p^+ ring will deplete the whole bulk between the p^+ backside layer and the large area n^+ doping (at potential V_4) as already explained in [1].

Since there is no biased contact at the edge of the detector a floating neutral area will be formed next to the edge as depicted in figure 1. The potential of this neutral area will follow closely the potential of the p^+ backside layer [1]. The benefit of the neutral area next to the sawed edge is that it minimises the depleted area at the sawed edge and thereby the edge generated leakage current.

The excess electrons (including edge generated electrons) collected by the neutral area flow horizontally in a channel located in the proximity of the backside p^+ layer and beneath the outermost p^+ ring after which these electrons flow through the substrate and are collected by an n^+ ring (at potential V_2) as is depicted by the red arrow in figure 1. Excess holes collected by the p^+ backside layer flow vertically to the outermost p^+ ring as is depicted by the vertical grey arrow. An additional p^+ ring (at potential V_3) prevents excess electrons originating from the edge area from entering into the large area n^+ doping collecting the radiation-induced electrons.

It is important to note that in reality the substrate doping will differ at least slightly at different parts of the detector chip. The location where the excess electrons from the neutral area flow to the n^+ ring (at V_2) corresponds to the location wherein the substrate has the highest doping underneath the outermost p^+ ring. The location of the punch-through biasing of the backside layer corresponds, on the other hand, to the location having the smallest substrate doping underneath the outermost p^+

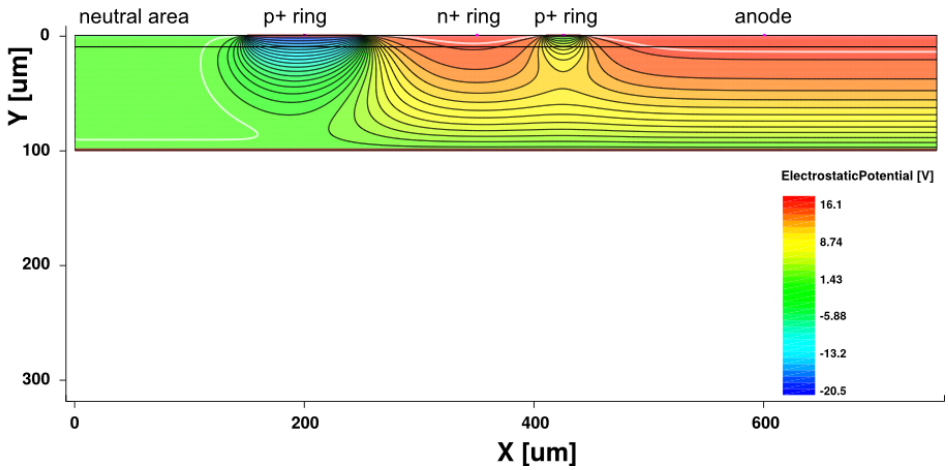

Figure 3. Electrostatic potential distribution in the simulated detector edge structure. The border of the neutral area situated next to the detector edge is depicted by a white line. The detector is fully depleted beneath the anode.

ring. These separate locations have been also drawn to figure 2. The higher the doping fluctuations underneath the outermost p^+ ring the larger the potential difference between the backside p^+ layer and the neutral area located next to the edge and thus the larger the edge generated leakage current. An efficient way to mitigate this problem is to use neutron trans-mutated Silicon (or Germanium) wafers.

3 TCAD simulation study

In this section 2D simulation results are presented and discussed. The simulated device comprises an n^- type 100 μm thick silicon substrate having a resistivity of 2 kΩ cm. The effect of the fixed charge at the Si/SiO_2 interface is taken into account by setting the positive oxide charge concentration to 1e11 cm^{-3}. The bias voltages at $V_1 = -20$ V, $V_2 = +15$ V, $V_3 = 0$ V, and $V_4 = +15$ V presented in figure 1 have been used in the 2D simulations corresponding to figures 3–7. The value of around 1 V at the backside p^+ layer and the neutral area in figure 1 corresponds to the 2D simulation results. One should note, however, that in reality the potential at the backside p^+ layer and at the neutral area would differ more as it is explained in conjunction with figure 2.

The electrostatic potential distribution of the simulated structure is presented in figure 3. The border of the neutral area situated next to the detector edge is depicted by a white line — elsewhere the detector is fully depleted excluding the n^+ and p^+ areas. It can be deduced from figure 3 that the proposed detector edge structure functions as desired; there is a neutral area next to the detector edge, the depleted edge area is minimized, and beneath the anode the detector is fully depleted.

The electron current distribution in the simulated detector edge structure is presented in figure 4. Electrons generated at the depleted edge and flowing from the neutral area through the depleted bulk are represented by the yellow arc located beneath the outermost p^+ ring and extend-

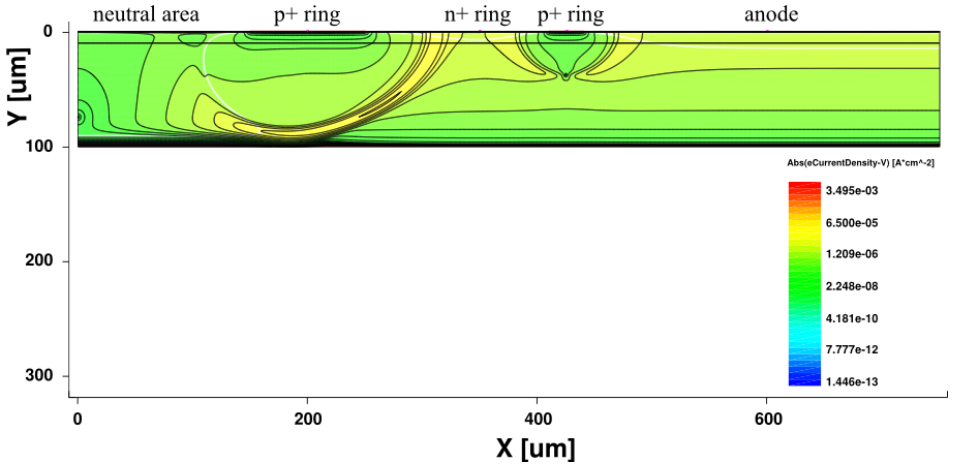

Figure 4. Electron current distribution in the simulated detector edge structure. Electrons flowing from the neutral edge area through the depleted bulk are represented by the yellow arc located beneath the p^+ ring and reaching to the n^+ ring. No edge generated electrons reach the n^+ doped anode.

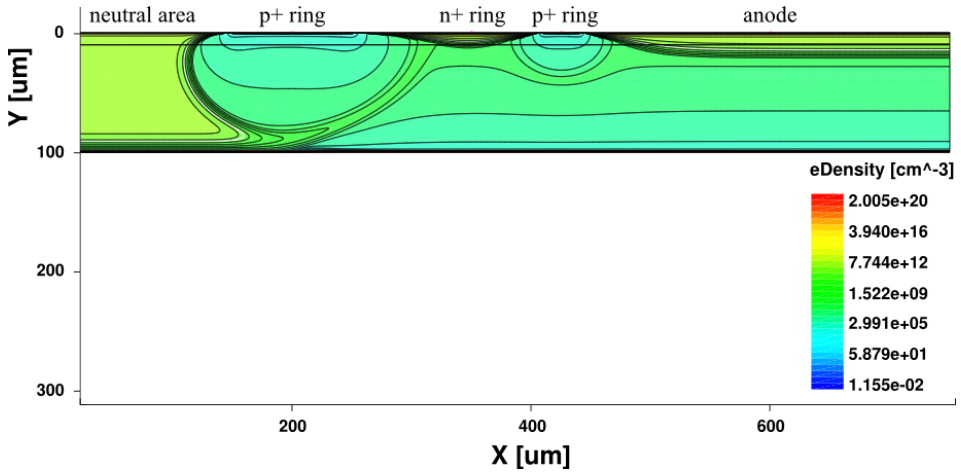

Figure 5. Electron density distribution in the simulated detector edge structure. The neutral area is next to the detector edge and the flow of electrons from the neutral area to the n^+ ring is represented by the arc located beneath the larger left hand side p^+ ring.

ing to the n^+ ring. It can be thus deduced that no edge generated electrons reach the active detector area, i.e., the n^+ anode doping.

The electron density distribution in the simulated structure is presented in figure 5. The neutral area is next to the detector edge and the flow of electrons from the neutral area to the n^+ ring (at V_2) can be easily identified. Thus one can deduce that the detector edge structure works as desired.

The hole current distribution in the simulated structure is presented in figure 6. A large reverse bias potential at the left hand side outermost p^+ ring provides punch-through biasing of the backside p^+ layer depleting thereby also the bulk. The punch-through hole current is represented by the

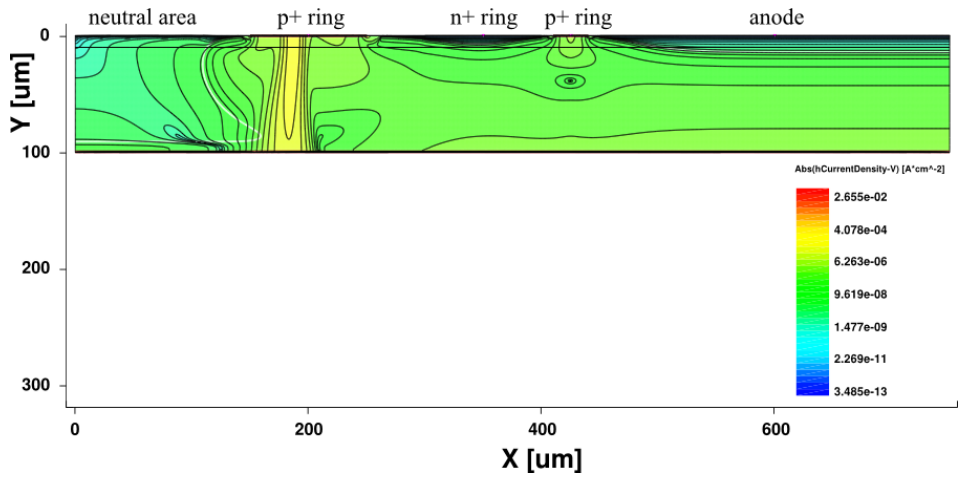

Figure 6. Hole current distribution in the simulated detector edge structure. A large reverse bias potential at the left hand side outermost p^+ ring provides punch-through biasing of the p^+ backside layer depleting thereby also the bulk. The punch-through hole current is represented by the yellow column beneath the left hand side p^+ ring.

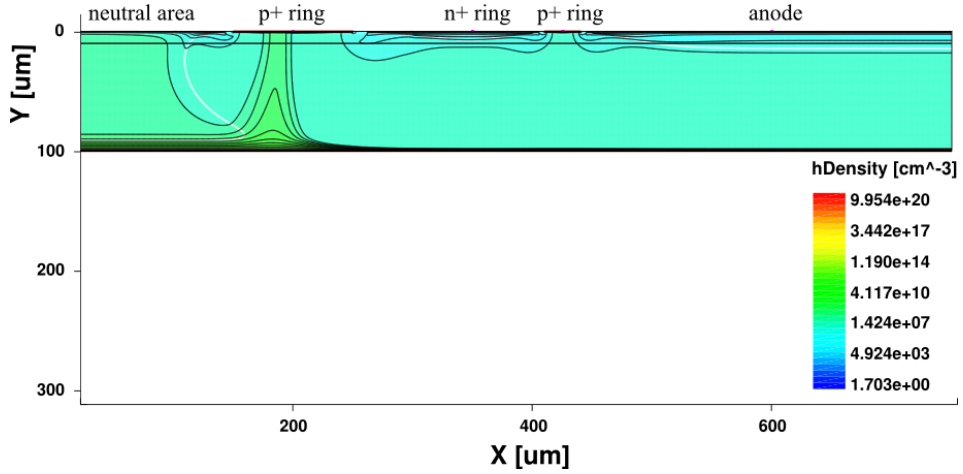

Figure 7. Hole density distribution in the simulated edge structure. The punch-trough hole current from the p^+ backside layer to the left hand side p^+ ring is represented by the green column beneath the left hand side p^+ ring.

yellow column beneath the left hand side p^+ ring. In other words, it can be clearly seen that the punch through biasing effect is established as intended.

The hole density distribution in the simulated structure is presented in figure 7. The punch-trough hole current from the p^+ backside layer to the left hand side p^+ ring is represented by the green column beneath the left hand side p^+ ring. This feature manifests also that the detector edge structure is working as designed.

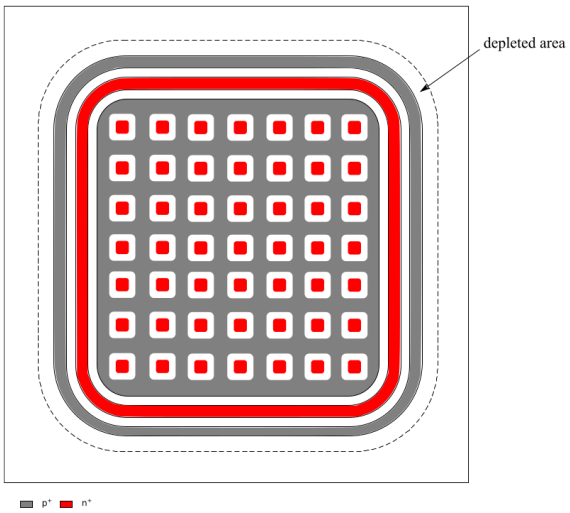

Figure 8. A top view of a pixelated detector comprising the suggested edge structure.

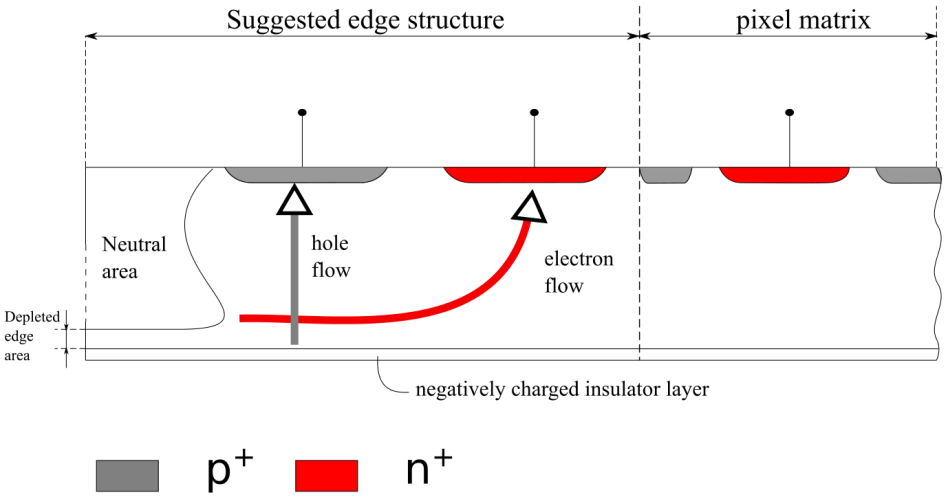

Figure 9. A cross-section of the edge of the pixelated detector shown in figure 8. The detector comprises the proposed edge structure.

4 Examples of other detectors incorporating the proposed edge structure

The proposed edge arrangement can be used with various types of radiation detectors having a homogeneous backside conductive layer of opposite doping type than the substrate or incorporating an inversion layer on the backside. One example is a pixelated detector which top view is shown in figure 8. A cross-section of the same pixelated detector is shown in figure 9. In this structure there is on the backside a negatively charged insulator layer [2] (formed e.g. of Hafnium oxide) providing an inversion layer of holes underneath the interface. In order to insure that the inversion layer is

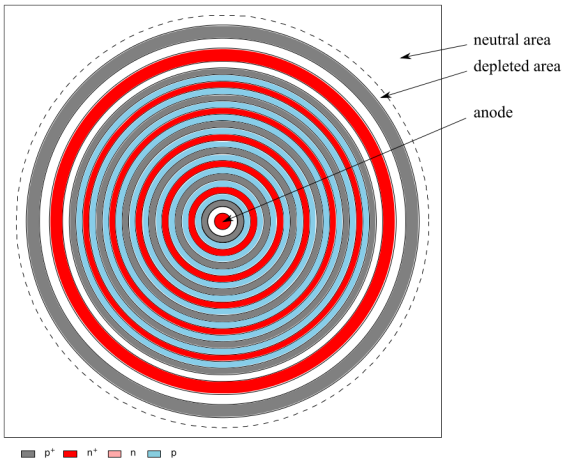

Figure 10. A top view of an SDD comprising the proposed edge structure.

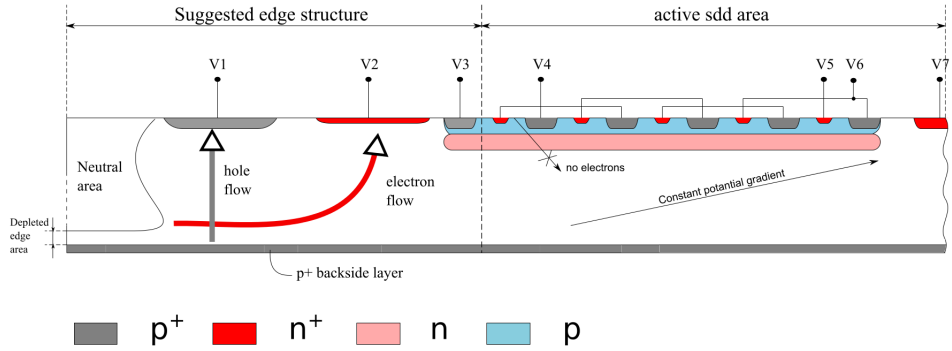

Figure 11. A cross-section view of a SDD comprising the proposed detector edge structure. The electrodes of the detector are biased such that the semiconductor body below the SDD rings is completely depleted and that a necessary horizontal potential gradient is created transporting radiation induced electrons underneath the SDD rings towards the anode.

established throughout the backside it may be necessary to place on top of the negatively charged insulator layer a transparent conductive layer like e.g. Indium Tin Oxide (ITO) or graphene. In case the negatively charged insulator layer is utilised to establish an inversion layer of holes it is highly likely that a very high resistive substrate (e.g. 10 kΩ cm or higher) is required in order to maintain an inversion layer still when the substrate reaches full depletion.

Yet another example is the Silicon Drift Detector (SDD) presented in figure 10. A cross-section of the same SDD is presented in figure 11. By biasing the nodes V_3, V_5, and V_6 properly a lateral drift field is established in the active SDD area guiding signal charge electrons generated underneath the SDD rings towards the anode. An additional benefit of the SDD of figure 11 is that interface generated electrons in the active SDD area (except next to anode) are collected by the SDD structure's n^+ and p^+ rings meaning that the SDD of figure 11 does not suffer from interface generated dark noise. The proposed detector edge arrangement enables the biasing of the backside

p^+ layer, minimises the amount of edge generated leakage current, and prevents edge generated electrons from entering into the active SDD area, i.e., the SDD does not suffer from edge generated dark noise.

5 Conclusions

The proposed detector edge structure enables thinned detectors with good QE for blue and NIR light, low CT, low dark noise, simple manufacturing without the need for a support wafer or back-side processing, as well as low edge generated leakage current. In order to maximise the benefits of the proposed detector edge structure neutron trans-mutated Silicon (or Germanium) wafers should be used.

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Publication IV

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A novel 3D detector configuration enabling high quantum efficiency, low crosstalk, and low output capacitance

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A novel 3D detector configuration enabling high quantum efficiency, low crosstalk, and low output capacitance

A. Aurola,[a,b] **V. Marochkin**[a,b,1] **and T. Tuuva**[b]

[a] *Pixpolar, Tekniikantie 1, 02150, Finland*
[b] *Lappeenranta University of Technology, P.O. Box 20, 53851, Finland*

E-mail: Vladislav.Marochkin@pixpolar.com

Abstract: The benefits of pixelated planar direct conversion semiconductor radiation detectors comprising a thick fully depleted substrate are that they offer low crosstalk, small output capacitance, and that the planar configuration simplifies manufacturing. In order to provide high quantum efficiency for high energy X-rays and Gamma-rays such a radiation detector should be as thick as possible. The maximum thickness and thus the maximum quantum efficiency has been limited by the substrate doping concentration: the lower the substrate doping the thicker the detector can be before reaching the semiconductor material's electric breakdown field. Thick direct conversion semiconductor detectors comprising vertical three-dimensional electrodes protruding through the substrate have been previously proposed by Sherwood Parker in order to promote rapid detection of radiation. An additional advantage of these detectors is that their thickness is not limited by the substrate doping, i.e., the size of the maximum electric field value in the detector does not depend on detector thickness. However, the thicker the substrate of such three dimensional detectors is the larger the output capacitance is and thus the larger the output noise is. In the novel direct conversion pixelated radiation detector utilizing a novel three dimensional semiconductor architecture, which is proposed in this work, the detector thickness is not limited by the substrate doping and the output capacitance is small and does not depend on the detector thickness. In addition, by incorporating an additional node to the novel three-dimensional semiconductor architecture it can be utilized as a high voltage transistor that can deliver current across high voltages. Furthermore, it is possible to connect a voltage difference of any size to the proposed novel three dimensional semiconductor architecture provided that it is thick enough — this is a novel feature that has not been previously possible for semiconductor components. Yet another feature of the novel three dimensional semiconductor architecture is that despite the thick substrate it can also be efficiently cooled.

[1] Corresponding author

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1 Introduction

The maximum thickness of the depleted bulk in planar semiconductor radiation detectors is determined by the electric break down field and by the substrate doping concentration. This means that the planar semiconductor detectors have an upper detection efficiency limit for deeply penetrating radiation unless multiple fully depleted planar detectors are placed on top of each other. Another option to improve the detection efficiency of planar detectors would be to utilize multiple detectors and to point the detector edges towards the radiation source, which is, however, not a truly optimal arrangement unless the radiation is unidirectional. Furthermore, a problem in thick planar detectors is horizontal spreading of the signal charge, which increases the crosstalk and hampers spatial resolution unless the detector is operated in photon counting mode [1] and charge sharing is taken into [2, 3] account.

In a planar semiconductor radiation detector the maximum absolute value of the electric field, which should be always substantially smaller than the absolute value of the electric break down field, is present at a pn junction located in the vicinity of either surface. The depletion of the bulk semiconductor material is provided by the vertical electric field component, which absolute value decays along the vertical direction pointing towards the inside of the bulk. If the semiconductor bulk is homogeneously doped then the absolute value of the vertical electric field component drops linearly in the vertical direction towards the interior of the bulk. In thick pixelated planar detectors there is essentially no horizontal field component except in the proximity of the surface. This means that the radiation induced charge cloud is not confined in the horizontal direction and thus it expands due to electric repulsion and random scattering events so that the charge may be shared amongst several pixels.

In Silicon Drift Detectors (SDDs) [4–6], which are planar detectors, there is a horizontal electric field component present inside the bulk which is not responsible for depleting the detector but instead it acts as a drift field transporting signal charges towards a charge-collecting anode. In the SDD the vertical electric field is responsible for the depletion of the detector and detector thickness is similarly limited by the electric breakdown field and the substrate doping concentration. In pixelated SDDs the horizontal drift field can be used for providing charge confinement in horizontal direction but the pixel aspect ratio (i.e. depth to pixel pitch ratio) cannot be very high since in high aspect ratio pixels the absolute value of the horizontal electric field component decays strongly towards the interior of the bulk.

In thick pixelated SDDs comprising high aspect ratio pixels the problem of the decaying horizontal electric field component could be somewhat relaxed if one could provide on both sides of the detector corresponding concentric SDD ring structures — this type of a detector is later on referred to as double-sided SDD. The difference in the SDD ring structure on the radiation entry side would be only that the charge collecting contact were replaced by an opposite type of doping. If the double-sided SDD pixel had n- bulk and p+ rings then the potential of the p+ rings on the radiation entry side would be shifted by a constant negative value when compared to corresponding rings on the opposite side in order to provide the necessary vertical drift field. Even in the double-sided SDD the pixel aspect ratio would need to be relatively small in order to withstand the effect of the decaying horizontal field since in high aspect ratio double-sided SDD pixels the lack of charge confining horizontal electric field in the central part of the pixel would anyhow cause horizontal charge spreading.

The aforesaid problems of planar detectors can be avoided with three dimensional (3D) semiconductor detectors [7, 8], and [9] comprising 3D electrodes penetrating vertically through a semiconductor substrate. In [9] a 3D Charge Coupled Device (CCD) is presented comprising 3D electrodes that are insulated from the substrate by an insulator layer. In [7] and [8] a 3D detector is presented comprising highly doped n+ and p+ type 3D electrodes. In the 3D detectors — excluding regions in the proximity of the detector surfaces — the electric field inside the semiconductor bulk has a vertically invariant horizontal component but no vertical component. The horizontal electric field depletes the substrate and the depletion voltage of the substrate depends on the substrate doping concentration as well as on the horizontal distance between the 3D electrodes but it is independent of the substrate thickness. Furthermore, photon absorption induced charge sharing between multiple pixels takes only place if the photon is initially absorbed at the pixel boundary, i.e., the charge sharing is independent of the 3D detector thickness. The reason for this is that the horizontal electric field effectively transports the signal charges towards a single electrode providing thus charge confinement and preventing horizontal charge spreading.

From this point onwards [7] and [8] are referred to as conventional 3D detectors, which have the advantage that the maximum drift path length of the signal charges depends only on the horizontal distance between the n+ and p+ electrodes, i.e., the drift length is independent of the thickness of the conventional 3D detector meaning that charge trapping is independent of the detector thickness. Since the distance between the 3D electrodes can be made much smaller than the thickness of the semiconductor substrate the conventional 3D detector enables high aspect ratio pixels that can be depleted with a small voltage and wherein charge sharing and trapping are minimized. Consequently, the conventional 3D detectors enable low crosstalk and good spatial resolution. The low depletion voltage is a substantial advantage when silicon based detectors are utilized in intense radiation environments like in particle accelerators. The reason is that the radiation generates acceptor states in silicon substrate which eventually impedes the full depletion of a thick planar detector whereas full depletion in a 3D detector can be maintained at substantially higher radiation dose levels due to the lower overall depletion voltage.

The problem associated with the conventional 3D detector concept is, however, that in a thick detector the capacitance of the signal charge collecting 3D electrodes is relatively high due to the large surface area of the 3D electrodes and due to the small distance between the 3D electrodes. This means that the thicker the conventional 3D detector is the larger is the capacitance and the poorer is the energy resolution of the detector. In [10] and [11] 3D detectors have been tested in X-ray

detection and imaging confirming low charge sharing properties but also highlighting problems with non uniform spatial response and geometrical inefficiencies. The problem of the 3D CCD is that the signal charge needs to be transported through the substrate multiple times from one 3D electrode to another. This means that in 3D CCD significant signal charge trapping tendency is resulted in by interface defects located at the semiconductor and insulator interface of the 3D electrodes.

In this paper a novel Pixelated Vertical Drift Detector (PVDD) concept [12] is proposed enabling high pixel aspect ratio, high detection efficiency, low crosstalk, and low noise (due to low output capacitance). This combination is enabled by providing inside the detector (excluding regions close to detector surfaces) both a constant vertical electric drift field and a vertically invariant horizontal electric field component. The constant vertical electric field component transports radiation-induced charges towards output contacts located on one surface of the detector. The small surface area of the charge collecting contacts enables low output capacitance that is not dependent on the detector thickness. The benefit of the small output capacitance is that it enables good energy resolution. The vertically invariant horizontal field inside the detector provides efficient confinement of radiation-induced charges even in thick detectors insuring thus low crosstalk and good spatial resolution. The fact that the vertical electric field component is constant means that the detector thickness is not limited by the electric field enabling thus high detection efficiency.

The PVDD is based on the idea of providing resistive paths that reach from one surface throughout the semiconductor detector to the opposite surface. On the front side there are two types of dopings forming contacts — the first type dopings collect the radiation-induced charges and the second type dopings form contacts to the one end of the resistive paths. On the backside there are second type dopings forming contacts to the other end of the resistive paths. By implementing a relatively small reverse bias between the first and second type contacts on the front side a vertically invariant horizontal electric field component is generated around the resistive path that depletes the bulk of the PVDD. The application of a potential difference between the second type contacts that are connected to the opposite ends of the resistive paths and located at the opposite surfaces of the detector results in a current flow inside the resistive paths. In case the resistivity along the resistive path is approximately constant the current flow through the resistive path results in according to the Ohm's law a constant potential gradient inside the resistive path. This constant potential gradient in the resistive paths (assuming that the resistive paths are oriented vertically) results in also a constant vertical drift field inside the depleted semiconductor bulk transporting radiation-induced charges towards the charge collecting contact located on the front side.

It is important to note that the thicker the PVDD, the larger is the voltage that must be applied in order to ensure an adequate vertical electric field. On the other hand, by providing a thick enough PVDD it is possible to connect a voltage in between the first and second surface that greatly exceeds a voltage that can be connected to a conventional planar device having similar substrate doping, which is a novel feature in high voltage semiconductor applications.

2 Pixelated Vertical Drift Detector

Figures 1a, 1b, and 1d illustrate the front side, the backside, and a central cross-section of the simulated device where the dashed lines correspond to the cross-section presented in figure 1c. The horizontal dashed line in figure 1c corresponds to the cross-section presented in figure 1d.

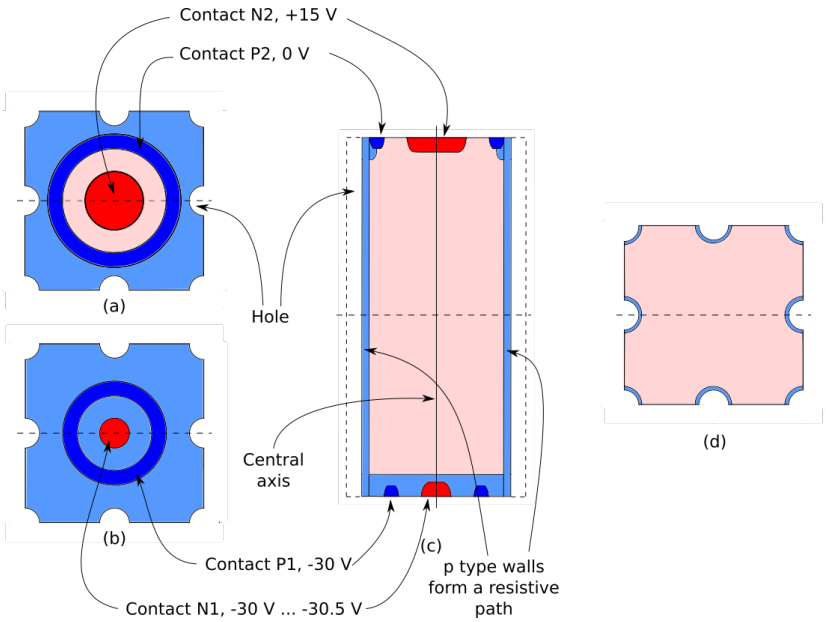


Figure 1. a) Front side of the PVDD, (b) backside of the PVDD, (c) vertical cross-section of the PVDD, and (d) central horizontal cross-section of the PVDD.

The simulated PVDD arrangement comprises an n- type high-resistivity silicon substrate wherein holes having p type doped walls and reaching throughout the substrate are situated at the pixel borders. On the backside there is a continuous p type layer to which a p+ type contact P1 is deployed. On the front side a p+ type contact P2 is deployed to a p type layer having a gap in the centre of the pixel wherein there is an n+ type contact N2 connecting to the n- type substrate. On the backside there is an optional n+ type contact N1 that is located inside the backside p layer. Between the p+ type contacts P1 and P2 there is a p type resistive path comprising the front and backside p layers as well as the p type hole-walls. The chip edges have preferably a similar p type doping than the hole-walls and establish a similar resistive path than the hole-walls. The backside is preferably the radiation entry side.

The holes having p type doped walls can be realized for example in the following manner. A Deep Reactive Ion Etch (DRIE) can be utilized for realizing high-aspect-ratio holes; in [13] 160:1 aspect ratio holes have been reported. Another possibility to realize the holes is to utilize laser-micromachining [14] enabling up to 100:1 aspect ratio holes, which has the benefit of enabling also the realization of tilted holes. Atomic Layer Deposition (ALD) and thermal drive-in by Rapid Thermal Annealing (RTA) as described in [15] could be utilized for realizing the doped hole-walls. For further reference double sided hole processing is described in [16]. Figure 2 illustrates central horizontal cross-sections of alternative hole arrangements which are not examined in this paper but which are likely more compatible to the DRIE process presented in [13].

In order to establish the resistive path corresponding to the hole-walls it is important to have on the horizontal pixel cross-section more p type dopant atoms on the hole-walls than n type dopant atoms in the substrate. If this condition is met then the p type hole-walls are not fully depleted even

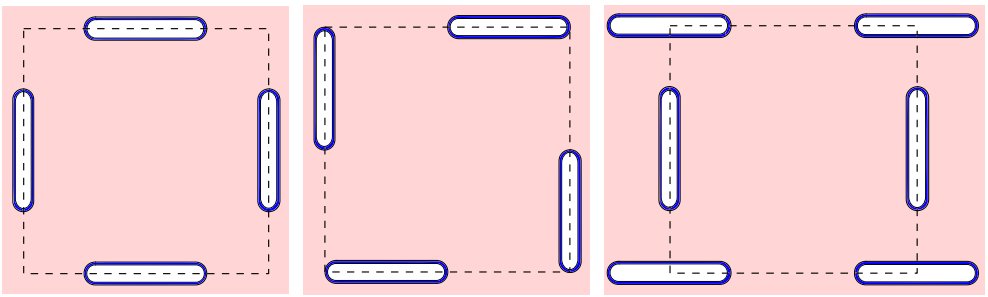


Figure 2. Figures (a), (b) and (c) illustrate central horizontal cross-sections of alternative hole arrangements.

if the n type substrate is fully depleted corresponding to the case that a sufficiently large reverse bias is applied between the n+ type contacts N2 with respect to the other p+ type contacts. In other words, even if the substrate is fully depleted part of the p type hole-walls will remain non-depleted meaning that a resistive path composed of holes (i.e. free charge carriers of positive type) is present along the hole-walls. When the substrate is fully depleted the amount of charge carrier holes on a horizontal cross-section of the pixel can be easily determined by subtracting the amount of n type dopant atoms from the p type dopant atoms on a horizontal cross-section of the pixel.

The PVDD is operated in the following manner. First a sufficiently large reverse bias (e.g. 15 V) is applied between the contacts P2 and N2 in order to fully deplete the n- type substrate resulting in a horizontal electric field component inside the semiconductor substrate pointing towards the central symmetry axis of the pixel. Next a negative bias (e.g. -30 V) is applied to the contacts P1 and N1 with respect to contact P2. The potential difference between the contacts P1 and P2 results in a hole-current flow along the p type hole-walls. If the resistivity of the hole-walls is approximately constant then the potential drops constantly along the hole-walls generating a constant vertical electric field component throughout the PVDD. It should be noted that since charge collecting electrodes will be connected to the input of a charge preamplifier in a read-out chip, which potential is typically at ~ 0 V, all voltages reported here should be shifted by 15 V towards negative values.

When radiation is absorbed inside the substrate the horizontal electric field component draws the radiation-induced holes into the p type hole-walls and pushes the radiation-induced electrons towards the symmetry axis of the pixel. The constant vertical electric field component transports the radiation induced holes inside the p type hole-walls towards the p type contact P1 (located on the backside) as well as radiation-induced electrons located at the symmetry axis of the pixel towards the N2 contact (located on the front side). The amount of electrons collected by the N2 contact is proportional to the amount of radiation absorbed in the pixel volume.

By applying a forward bias between the contacts N1 and P1 a vertical trap-filling electron flow from the contact N1 towards the contact N2 is established at the location of the symmetry axis of the pixel. This mechanism should benefit 3d detectors that are based on other semiconductor materials than silicon. According to [17] it has been observed for diamond detectors that device irradiation at room temperature with penetrating radiation such as X-rays or minimum ionising particles induces an increase of the detector signal resulting in from deep-trap filling in the whole volume of the

detector and being sensitive to the initial state of the device prior to operation. Therefore based on [17] trap filling can actually benefit detector operation depending naturally on temperature, how deep the trap levels are, and how often the traps are filled. The way in which the traps are filled is irrelevant, i.e., the trap filling could equally well be performed via current injection.

The proposed novel 3d structure could also be applied as a high voltage transistor if the device is thick enough since a large voltage difference could be utilised between the nodes N1 and N2 while the current running between the Nodes N1 and N2 could be adjusted by applying a suitable forward bias between the nodes N1 and P1. In this manner current could be transported when necessary across a large voltage difference. Particularly when the proposed novel 3d structure is utilised in a high voltage transistor application incorporating a thick substrate and large current flows efficient cooling may be important. Examples of cooling are presented in [18] and [19]. One possibility to establish cooling could be to provide a vertical flow of coolant gas like e.g. helium inside the holes. In photon detection applications it is important to note that like in conventional 3D detectors charge sharing takes place only initially when a photon is absorbed provided that the photon is absorbed at the pixel border [10].

The PVDD offers several advantages that are listed below.

1) The maximum absolute magnitude of the electric field is not dependent on the detector thickness and thus the detector thickness is not limited by the electric field.

2) The capacitance of the output node N2 is small and does not depend on detector thickness enabling thus low noise. Besides, in an integrating detector configuration the small capacitance enables high charge to signal conversion gain facilitating also low noise operation.

3) The facts that the holes can be tilted along a direction pointing towards the radiation source and that the radiation induced electrons are confined to the centre part of the pixel mean that crosstalk can be substantially reduced. It should be noted, however, that the realisation of the tilted holes is not trivial and that it may be out of the reach for current standard manufacturing tools.

4) The fact that transport of radiation-induced charges is confined to a narrow path along the pixel symmetry axis means also that pixel specific trapping tendency is more predictable.

5) The fact that an electron flow can be generated in the centre of the pixel running from N1 to N2 means that before PVDD is exposed to radiation electron traps located along the electron drift path can be filled with electrons corresponding to the electron flow. Depending on the temperature and whether the radiation source is operated in pulse mode trap filling could be performed in between the radiation pulses reducing thus trapping of radiation-induced electrons.

The first three points facilitate expanding the useful operation regime of direct conversion detectors to higher energy X-ray applications — e.g. a silicon based direct conversion detector reaching 90% conversion efficiency for 30 keV photons must be at least 9 mm thick. While thick detectors have been reported previously [20], it should be noted that the maximum thickness of wafers that present silicon processing tools in foundries can handle is typically around 1 mm. The

fourth and fifth point could facilitate the use of other semiconductor materials than silicon or germanium in direct conversion semiconductor radiation detector applications.

It should be noted that the resistance of the resistive path along the hole-wall can be described by the ohmic relation $U = I \times R = I \times \rho \times L/A$, where U is the potential difference between the opposite ends of the hole, I is the current running along the hole-walls, ρ is the resistivity of the p type hole-wall material, L is the vertical length of the hole, and A is the horizontal cross-section area of the p type hole-wall material. If the horizontal topology of the holes differs from one hole to another and/or if the resistivity ρ is different than planned, the magnitude of the vertical electric field component remains essentially the same. In case there were holes with different horizontal topologies the only difference would be that the currents running through the resistive paths formed by the hole-walls would differ in different topologies. In case the resistivity of the material forming the hole-walls were different than planned the only difference would be that the currents running through the resistive paths formed by the hole-walls would be changed throughout the detector by the same factor. The requirements to create the essentially constant vertical electric field component are that the quantity ρ/A is approximately constant along the vertical direction. This reasoning applies also to the detector edge, which can be considered simply as a large hole-wall.

As already previously said the direction of the holes can be aligned along the radiation source, i.e., the centre axis of the holes can be aligned along the 'local direction' of the radiation as depicted in figures 3 and 4. In case the radiation is not unidirectional but originates from a point source the arrangements of figures 3 and 4 enable considerable reduction in crosstalk if the alignment direction of all of the holes (and the edge in figure 3) converges towards the point source. In the arrangement of figure 3 all the pixels are functional and the detector edge acts as a resistive path similar to the hole-walls.

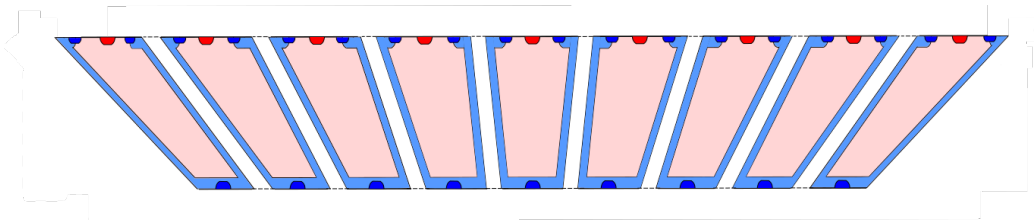


Figure 3. A PVDD design minimising the crosstalk when the observed radiation originates from a point source. The centre axis of the holes point towards the point source.

If the ratio of the detector size to the detector distance from the point source were relatively large then the detector edges on the front side would be relatively sharp — a case that is depicted in figure 3. The problem with the sharp edges is that it may hamper the manufacturability. In order to mitigate this effect the detector edge configuration of figure 4 could be used instead. In this configuration the outermost pixels at the detector edges are, however, not functional. The reason is that they collect radiation-induced charge also from the pixel-like structures that are truncated at the detector edges.

One should note that in the pixels of the detectors corresponding to figures 3 and 4 the previously used terms like horizontal and vertical direction are not anymore adequate. The direction of the drift path in the centre of the pixel pointing towards the point-source corresponds to a 'local vertical'

direction and directions on the plane orthogonal to the 'local vertical' direction correspond to 'local horizontal' directions. With the aid of these definitions it can be easily described that the radiation-induced charge is drifting along the 'local vertical' direction and that a potential barrier for the radiation-induced charge is formed along a 'local horizontal' direction.

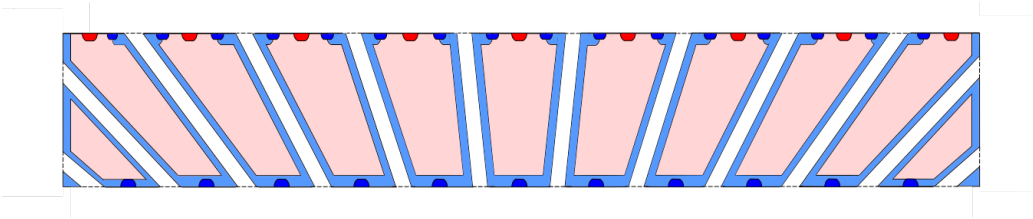


Figure 4. A PVDD design avoiding the formation of sharp edges as well as minimising the crosstalk when the observed radiation originates from a point source. The centre axis of the holes point towards the point source.

An observation that can be made from figures 3 and 4 is that the area of the pixel cross-section along the 'local horizontal' plane increases towards the front surface of the pixel. If the doping concentration in the substrate and in the hole-walls is constant and if the hole radius is constant then the amount of non-depleted p type dopant atoms (i.e. the amount of holes) inside the p type hole-walls reduces towards the front side of the detector. The reason for this is that the larger the 'local horizontal' cross-section of the pixel is the more p type dopant atoms are required to deplete the n type dopant atoms inside the substrate and thus the less there are holes inside the p type hole-walls. For this reason in the detector configurations of figures 3 and 4 the electric field component along the 'local vertical' direction is not strictly constant. Instead the electric field component is at maximum on the front side of the detector and the value inside the detector scales down by a factor of 'local horizontal' pixel area inside the detector divided by the 'local horizontal' pixel area at the front surface. Also the potential barrier on the 'local horizontal' plane from the drift path towards the pixel edge is the bigger the closer one is to the front surface.

3 3D TCAD simulation study

In this simulation study a PVDD pixel according to figure 1 is investigated. The performance of the pixel has been studied by simulating a quarter of the whole pixel using TCAD tools. It was possible to simulate only the quarter of the pixel due to its symmetry and by doing so the required simulation time was considerably reduced.

When the substrate is fully depleted the pixel's net hole concentration N_h per distance inside the hole-walls is given with the following equation

$$N_h = 3\pi \left(r_i^2 - r_o^2\right) \times C_p - \left(D^2 - 3\pi r_o^2\right) \times C_n, \tag{3.1}$$

wherein the pixel size D is 100 μm. Along the pixel boundary there are 8 partial empty holes corresponding to 3 entire holes, each of the holes having a radius r_i corresponding to 5 μm. Next to the hole-wall there is a 1 μm thick p type layer which outer radius r_o corresponds to 6 μm and which p type dopant (boron) concentration C_p corresponds to 2.2e15 cm^{-3}. The n type substrate

dopant (phosphorus) concentration C_n corresponds to 5e12 cm^{-3}. Based on (1) pixel's net amount of holes inside the hole-walls per hole length is around 1.8×10^9 cm^{-1} when the substrate is fully depleted, i.e., in each vertical hole forming the resistive path there are around 60000 holes per one micrometre thick hole-wall slab. The amount of hole current I_h running in one hole wall in room temperature can be calculated with the following equation

$$I_h = \mu_h \frac{U}{T} \frac{N_h}{3} e, \tag{3.2}$$

wherein μ_h is the hole mobility at room temperature and at 2.2e15 cm^{-3} boron concentration corresponding to 450 $cm^2V^{-1}s^{-1}$. The vertical electric field value inside the hole wall is given by the division U/T wherein U corresponds to 30 V potential difference between the opposite ends of the hole wall and T corresponds to the detector thickness 300 μm. The symbol e refers to the elemental charge corresponding to 1.6×10^{-19} C. N_h corresponds to equation (3.1) and the division by 3 takes into account that the current I_h corresponds to only one hole wall. Based on equation (3.2) the holes in the hole walls result in a current corresponding approximately to 43 μA running in one hole-wall. In case of a thicker device, like for example in a 600 μm thick device, the current running through the hole-wall will be the same if the electric field and the hole diameter remains the same (hole aspect ratio would increase from 30:1 to 60:1).

One of the main objectives of this paper was to test whether a constant vertical electric field component could be established inside the simulated PVDD pixel. In order to test this a reverse bias of 15 V was first applied between the contacts P2 and N2. Based on the simulation this was enough to fully deplete the 300 μm thick n- type substrate resulting in a horizontal electric field component inside the semiconductor substrate pointing towards the central axis of the pixel. Next a negative bias of −30 V was applied to the contacts P1 and N1 with respect to contact P2 (being at 0 V). According to the simulation the potential difference between the contacts P1 and P2 resulted in a hole-current flow along the p type hole-walls resulting in a constant potential drop along the hole-walls generating a constant vertical electric field component throughout the PVDD. This was naturally expected since the doping concentration and thereby the resistivity of the p type hole-wall material is constant. The constant vertical electrostatic potential gradient inside a 300 μm thick device can be seen on figures 5a and b. The constant vertical electrostatic potential gradient is even more pronounced in figure 6 corresponding to a 600 μm thick device wherein the backside contacts P1 and N1 are connected to −60 V, P2 is biased at 0 V, and N2 is biased at 15 V. Figure 5b represents the potential gradient on the symmetry axis (L1) and at the edge of the pixel (L2) of the 300 μm thick pixel when −30 V is applied to contacts P1 and N1, P2 is at 0 V, and N2 is at 15 V. It can be seen from the figure that a constant potential gradient, i.e. a constant vertical electric field component is created in the mid portion of the pixel (from 100 μm to 200 μm).

Another objective of the paper was to test whether a sufficiently large barrier could be created from the drift path towards the pixel edge in order to insure that no crosstalk is resulted in of signal charge blooming from one pixel to another. In figure 5b one can see two potential graphs which difference corresponds to the horizontal potential barrier, which is constant inside the mid portion of the substrate. The horizontal locations L1 and L2 wherein the potential graphs are taken can be seen in figure 7b. Figure 5b represents electrostatic potential distribution for the case when −30 V is applied to contacts P1 and N1, P2 is at 0 V, and N2 is at 15 V. The barrier from the middle to

the edge of the pixel being constant in the mid portion of the pixel and equalling to around 3 V is more than enough to eliminate the blooming crosstalk. Corresponding simulation results are presented for a 600 μm thick PVDD on figures 6b and 8b. From the figure 6b it can be seen that the barrier equals to around 3 V as well meaning that the thickness of the pixel does not affect the barrier height. Similarly one can deduce that a constant vertical drift field is established inside the substrate when the distance from the surface is around 100 μm or more.

The third objective of this paper was to test whether an electron flow can be established in the centre of the pixel running from the contact N1 to the contact N2 by applying a forward bias between the contacts N1 and P1. In the simulation result presented in figure 9 the contact N1 is biased at −30.5 V, P1 is biased at −30 V, P2 is biased at 0 V, and N2 is biased at 15 V, i.e. a forward bias of 0.5 V is applied between P1 and N1. The forward bias results in a flow of electrons running in the middle of the pixel — the white lines represent the border of a non-depleted area formed around the symmetry axis of the pixel. Figure 10a illustrates a horizontal cross-section of the PVDD quarter-pixel presented in figure 9. Figure 10b illustrates horizontal electrostatic potential barriers from the middle to the edge of the pixel when the forward bias between P1 and N1 is 0.1 V, 0.2 V, 0.3 V, 0.4 V, and 0.5 V. From 9b it can be easily deduced that in the simulated detector configuration the electron current running inside the pixel starts to alter the horizontal potential barrier between the middle and the edge of the pixel only when the forward bias between P1 and N1 is 0.5 V or higher. Even at 0.5 V forward bias the horizontal potential barrier from the middle to the edge of the pixel is reduced only slightly to 2.8 V.

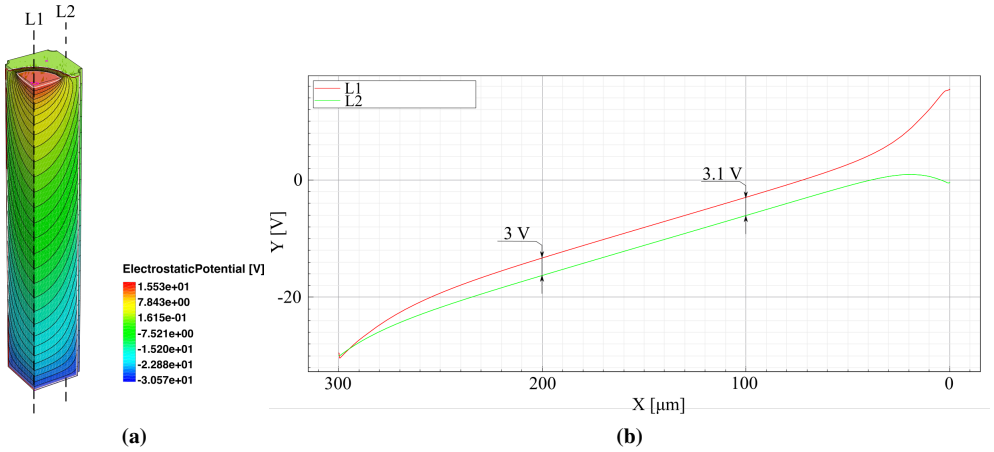
Figure 11 corresponds to a transient simulation wherein the 300 μm thick PVDD quarter-pixel is illuminated with a 100 ns monochromatic 850 nm light pulse having an intensity of 1500 W/cm^2. The curve in figure 11 represents the electron current at the n+ contact (N2) as a function of time. As can be seen from figure 11 the output current increases considerably during the light pulse. Furthermore, according to the curve in figure 11 the photo induced excess output current dies off at around 23 nano-seconds after the termination of the light pulse.

The capacitance of the signal charge collecting contact N2 in the operational 300 μm thick device was simulated to be around 49 fF, which is exactly the same as in the 600 μm thick device meaning that in a thick enough PVDD the capacitance of the contact N2 is not affected by the device thickness.

4 Conclusions

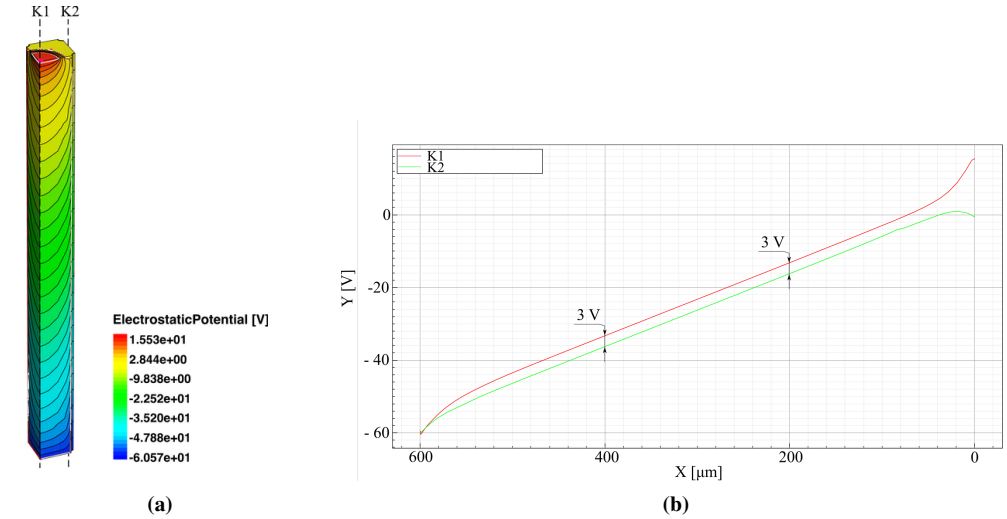
The purpose of this work was to utilize 3D simulations in order to validate the operational principle and the benefits of the PVDD concept. It is fair enough to say that this goal was successfully achieved.

As already stated the PVDD concept offers several advantages. The maximum electric field is not dependent on the detector thickness and thus the detector thickness is not limited by the break-down electric field. The capacitance of the output node is small and does not depend on detector thickness. The crosstalk is mitigated since the radiation induced electrons are confined to the centre part of the pixel, thus preventing signal charges from spreading into neighbouring pixels. In case a point like radiation source is utilised the crosstalk can be further mitigated if one utilises tilted holes wherein the central axis of the holes is pointed towards the point like radiation



(a) (b)

Figure 5. Simulation results for 300 μm thick PVDD: (a) Electrostatic potential distribution inside the PVDD quarter-pixel. Vertical cutlines L1 and L2 are illustrated. (b) Electrostatic potential on the vertical cutlines L1 and L2 corresponding to the case when P1 and N1 are biased at −30 V, N2 is biased at 15 V, and P2 is biased at 0 V. The figure 5b demonstrates that a potential barrier exists between the middle and the edge of the pixel essentially along the whole thickness of the pixel. When the distance from the surface is 100 μm or more the figure demonstrates that the barrier height is constant at around 3 V and that a constant vertical drift field is established inside the substrate.



(a) (b)

Figure 6. Simulation results for a 600 μm thick PVDD: (a) Electrostatic potential distribution inside the PVDD quarter-pixel. Vertical cutlines are K1 and K2 are illustrated. (b) Electrostatic potential on the vertical cutlines K1 and K2 corresponding to the case when P1 and N1 are biased at −60 V, N2 is at 15 V, and P2 is at 0 V. The figure illustrates the realisation of a constant 3 V horizontal potential barrier between the middle and the edge of the pixel as well as the realisation of a constant vertical drift field inside the substrate when the distance from the surface is 100 μm or more.

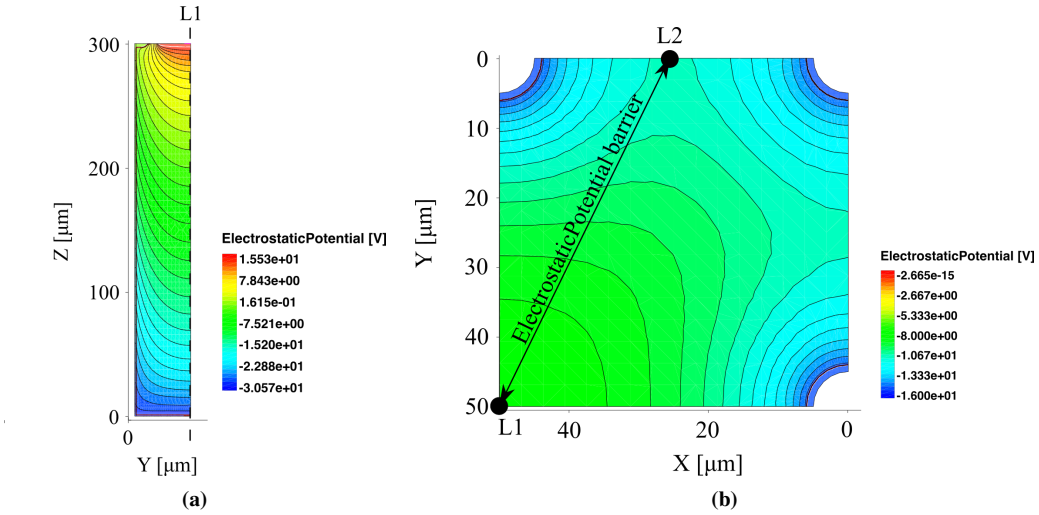


Figure 7. Simulation results for 300 μm thick PVDD: (a) Electrostatic potential distribution at a vertical 2D cross-section of the PVDD quarter-pixel. P1 and N1 are at −30 V, N2 is at 15 V, and P2 is at 0 V. The vertical cutline L1 is illustrated. (b) Electrostatic potential distribution on a central horizontal cross-section of the PVDD quarter-pixel of figure 5a. The figure illustrates the realisation of a horizontal electrostatic potential barrier between the middle (L1) and the edge (L2) of the pixel.

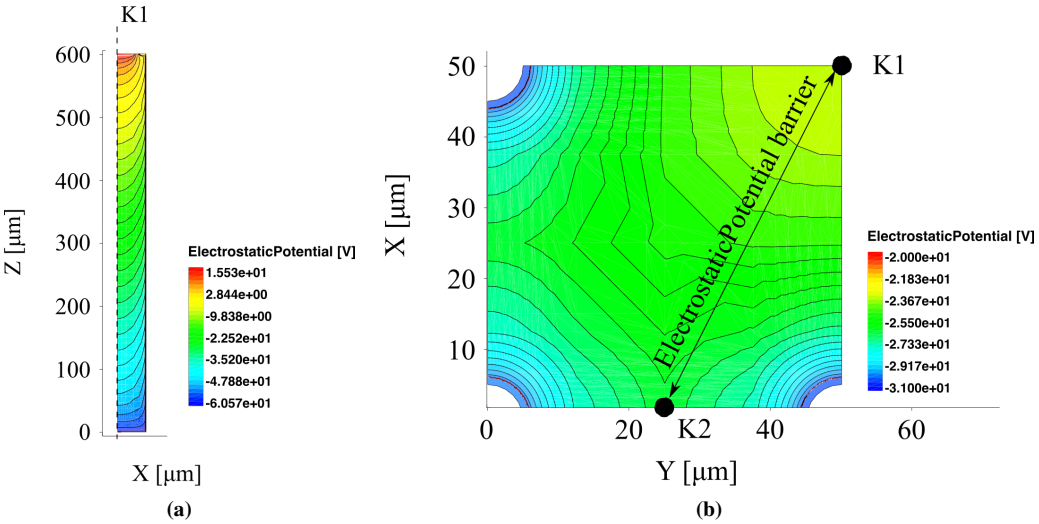


Figure 8. Simulation results for a 600 μm thick PVDD: (a) Electrostatic potential distribution at a 2D vertical cross-section of the PVDD quarter-pixel. P1 and N1 are at −60 V, N2 is at 15 V, and P2 is at 0 V. The vertical cutline K1 is illustrated. (b) Electrostatic potential distribution on the central horizontal cross-section of the PVDD quarter-pixel of figure 6a. The electrostatic potential barrier between the middle (K1) and the edge (K2) of the pixel is illustrated in the image.

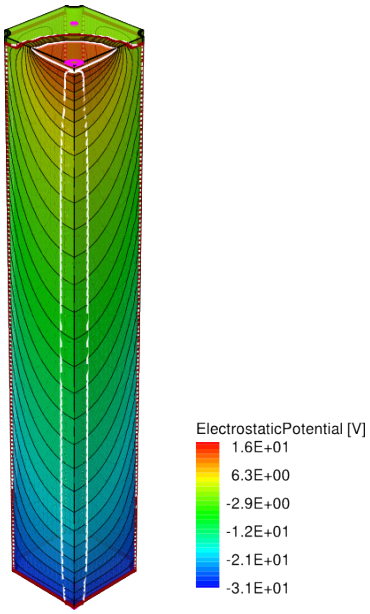


Figure 9. Electrostatic potential distribution inside the PVDD quarter-pixel when electrons are flowing from N1 to N2. P1 is at −30 V, N1 is at -30.5 V, N2 is at 15 V, and P2 is at 0 V. The electron flow at the centre of the pixel is so intense that a non-depleted area marked with white lines is formed around the symmetry axis of the pixel.

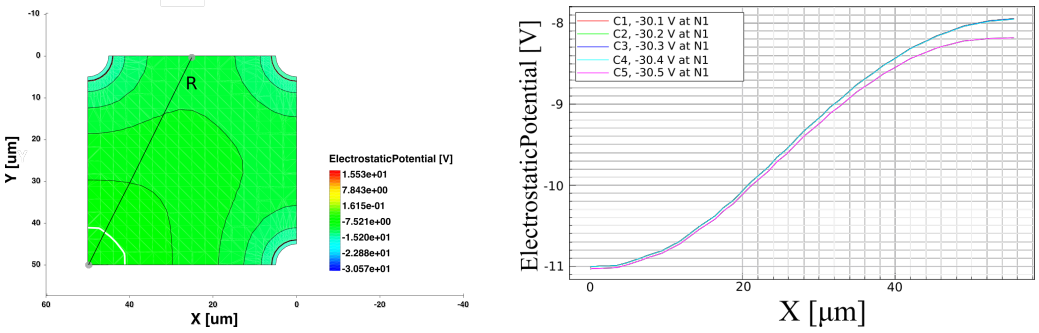


Figure 10. (a) Electrostatic potential distribution on a central horizontal cross-section of the PVDD quarter-pixel of figure 8. The border of the non-depleted n type substrate is depicted by the white line in the lower left corner of the figure. P1 is at −30 V and N1 is at −30.5 V, N2 is at 15 V and P2 is at 0 V. A cutline is presented with symbol R. (b) Electrostatic potential graphs C1, C2, C3, C4, and C5 on the cutline R. These graphs correspond to the cases when N1 is biased at −30.1 V, −30.2 V, −30.3 V, −30.4 V, and −30.5 V respectively. P1 is at −30 V, N2 is at 15 V, and P2 is at 0 V.

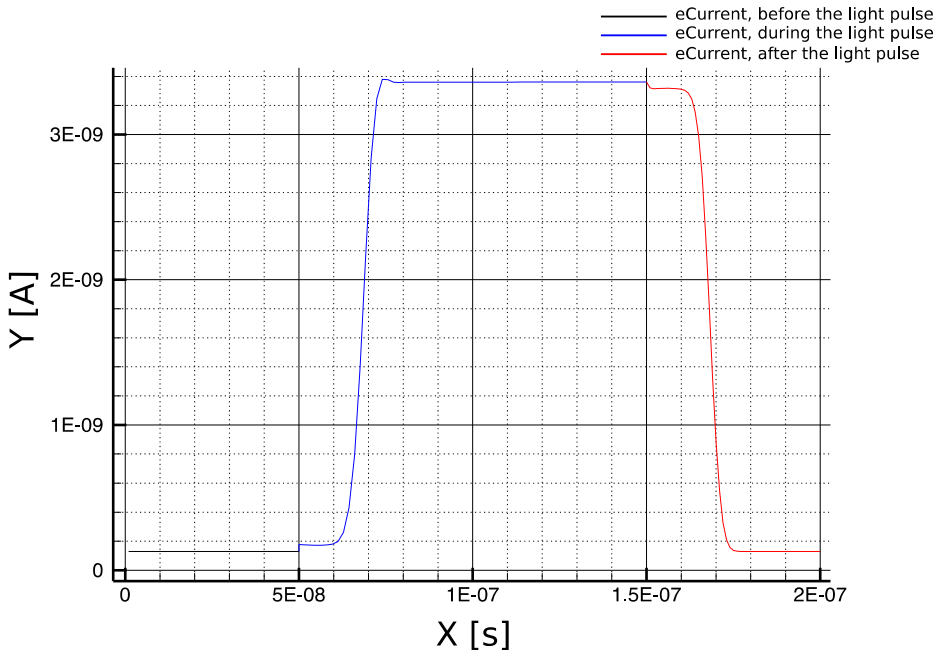


Figure 11. 100 ns light pulse simulation on a 300 μm thick PVDD quarter-pixel. The curve corresponds to the electron current at the n+ type contact N2 as a function of time. The change in the current is due to the light pulse.

source. The downside of the tilted holes is, however, that it is difficult to realise with existing standard manufacturing tools. In case the PVDD is operated in pulsed manner so that an electron flow is generated sporadically along the pixel drift path then it is possible to fill the electron traps located along the drift path. This would increase the signal particularly in detectors that are made of semiconductor materials being prone to trapping.

Afore said benefits of the PVDD concept may enable to expand the operational range of silicon and germanium based radiation detectors to higher energies without degrading the detector performance. Thus in some applications it may be possible to use silicon or germanium detectors instead of compound semiconductor detectors which are expensive, difficult to process, and prone to lattice defects. On the other hand, the PVDD concept may also improve the performance of compound semiconductor detectors so that it could be possible in some applications to replace indirect conversion radiation detectors with direct conversion compound semiconductor radiation detectors. Yet another advantage of the PVDD in compound semiconductor applications is that the typical disproportion between the electron and hole mobilities can be exploited by choosing the electrons as signal charges and by choosing the holes as the charge type forming the resistive paths. In this manner the signal charge collection time as well as the power consumption could be minimized in the PVDD.

It should be possible to utilise the PVDD concept (comprising a detector edge functioning as a resistive path) in edgeless tileable detector configurations in such a manner that radiation induced charge generated inside an edge or corner pixel is also confined to it. In other words the detector

edge should not repel charge from edge or corner pixels to neighbouring pixels. This would, however, need to be verified with 3D simulations by checking that the horizontal potential barriers in the edge and corner pixels can be made large enough in order to prevent blooming of signal charge from one pixel to another.

The authors acknowledge that manufacturing challenges must be overcome before the PVDD concept could offer a practical alternative to existing radiation detectors. Furthermore, in order to bring forth the research a PVDD demonstrator would need to be manufactured. This is, however, out of reach for the authors of this paper and thus collaboration on the matter would be warmly welcomed.

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