



Heikki Järvisalo

APPLICABILITY OF GAN HIGH ELECTRON MOBILITY TRANSISTORS IN A HIGH-SPEED DRIVE SYSTEM



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Supervisors Professor Pertti Silventoinen
LUT School of Energy Systems
Lappeenranta–Lahti University of Technology LUT
Finland

Dr. Juhamatti Korhonen
LUT School of Energy Systems
Lappeenranta–Lahti University of Technology LUT
Finland

Reviewers Associate Professor Jiří Háze
Department of Microelectronics
Brno University of Technology
Czech Republic

Associate Research Professor Wensong Yu
Department of Electrical and Computer Engineering
NC State University
USA

Opponent Associate Professor Jiří Háze
Department of Microelectronics
Brno University of Technology
Czech Republic

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Abstract

Heikki Järvisalo

The applicability of GaN high electron mobility transistors in a high-speed drive system

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Lossless operation and instantaneous switching are properties of an ideal power electronic switch. Wide band gap devices based on gallium nitride (GaN) are the current peak performers in regard to losses and switching speeds; rising and falling times in the order of nanoseconds are attainable with commercial GaN high electron mobility transistors (HEMTs). Despite their exceptional switching characteristics, GaN HEMTs have not managed to challenge the dominance of silicon (Si) devices. This is due to the uncertainties associated with GaN HEMTs, the main drawback being the current collapse phenomenon, where the drain current temporarily decreases after a high off-state voltage stress.

In compressor and blower applications, high-speed permanent magnet synchronous motors (PMSM) are an appealing option owing to their high efficiency and power density, along with a small physical size. When pairing up a motor with an inverter, a bulky output filter is usually a necessity. However, with a high inverter switching frequency, the output filter size can be reduced. Furthermore, a high switching frequency inverter provides sinusoidal current to the motor, leading to lower motor losses and torque ripple.

In this doctoral dissertation, the effect of current collapse on the static channel resistance of GaN HEMTs is studied on a macro timescale. The GaN switches are stressed with different switching conditions, and after the stress, the channel resistances are measured with a power device analyzer. Furthermore, this dissertation presents the design of a high-speed electrical drive, consisting of a three-level active neutral-point-clamped inverter (ANPC) applying GaN HEMTs and a high-speed PMSM.

It is shown in the doctoral dissertation that the current collapse phenomenon increases the static channel resistance of GaN HEMTs after a switching stress without current stress. However, after a recovery period in the range of minutes, the channel resistance has recovered to its original value. The applied switching frequency and stress time influence the increase and recovery speed of the channel resistance. Alternatively, it is shown that the current stress during switching effectively nullifies the effect of the current collapse phenomenon on static channel resistance.

The findings in this doctoral dissertation suggest that GaN HEMTs are applicable to high switching frequency three-phase inverters, as the experimental results of the ANPC inverter exhibit sinusoidal output voltages and currents. Because of the 1 MHz switching frequency of the prototype, the volume of the realized output filter is 5% of the volume of a sine wave filter paired with a similarly rated commercial inverter, demonstrating the superior power density potential enabled by GaN HEMTs. However, the voltage transition times in the order of nanoseconds require careful attention to the minimization of stray inductances in the PCB design. Otherwise, the resulting ringing could produce excessive amounts of EMI, or even destroy the inverter.

Keywords: gallium nitride (GaN), current collapse, high-speed drive, permanent magnet synchronous motor (PMSM)

Acknowledgments

My journey towards a top hat started in September 2013, as I started working as a junior researcher at the Laboratory of Applied Electronics at LUT University, Finland. However, the initial research had little to do with the work presented in this doctoral dissertation. In late 2015, an epiphany shifted my focus towards the study of gallium nitride, and as a result, this dissertation research was carried out between the years 2016 and 2019.

I would like to express my deepest gratitude to my supervisor Professor Pertti Silvenoinen. You gave me the idea to study gallium nitride and its applications, and furthermore, your encouragement and advice during this process were vital. You had confidence in me, even during my initial academic meandering in the realm of gate drivers... I want to thank my preliminary examiners Associate Professor Jiří Háze and Associate Research Professor Wensong Yu for their insightful comments and suggestions, which helped in improving this dissertation.

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Heikki Järvisalo
December 2019
Lappeenranta, Finland

*Gallium nitride,
Super fast switching action,
Really awesome?*

- hesus

Contents

Abstract

Acknowledgments

List of Symbols and Abbreviations **11**

1 Introduction **13**

1.1	Gallium Nitride High Electron Mobility Transistors	14
1.2	GaN-based power electronics	17
1.3	Motivation of the study	22
1.4	Outline of the doctoral dissertation	23
1.5	Scientific contributions	23
1.6	Scientific publications	24
1.7	Scientific methods	25

2 Macro timescale channel resistance behavior of GaN HEMTs **27**

2.1	Prototype implementation	29
2.2	Measurement setup	31
2.3	Measurement results	34
2.3.1	Zero current stress	34
2.3.2	Current stress	38
2.3.3	Conclusions on the macro timescale $R_{DS,on}$ phenomena	39

3 Design and implementation of the drive system **41**

3.1	Inverter topology	41
3.2	Implementation of the ANPC prototype	44
3.3	Control system for the high-speed drive	49

4 Simulation results of the sensorless motor control **53**

5 Experimental results of the ANPC inverter **59**

6 Conclusions **65**

6.1	Key results	65
6.2	Future work	66

References **67**

Appendix A Additional measurement results **73**

List of Symbols and Abbreviations

Roman letters

C	Capacitance	[F]
D	Duty cycle	
e	Back-EMF	[V]
f	Frequency	[Hz]
i	Current	[A]
K_E	Back-EMF constant	
K_P	PI controller proportional term	
K_i	PI controller integral term	
L	Inductance	[H]
m	Modulation index	
p	Differential operator	
Q	Quality factor	
R	Resistance	[Ω]
u	Voltage	[V]

Greek letters

ε	Error signal	
θ	Angle	[rad]
ψ	Flux linkage	[Wb]
ω	Angular speed	[rad/s]

Subscripts

α	Alpha-axis
β	Beta-axis
d	Direct-axis
ds,on	Dynamic channel resistance
est	Estimated value
f	Filter
ON	Static channel resistance
PM	Permanent magnet
q	Quadrature-axis
r	Rotor
ref	Reference value

Acronyms

2DEG	Two-dimensional electron gas
AlGaN	Aluminium gallium nitride
AMB	Active magnetic bearing
ANPC	Active neutral-point-clamped
CHB	Cascaded H-bridge
CMTI	Common-mode transient immunity
DC	Direct current
du/dt	Voltage transition speed
EMF	Electromotive force
EMI	Electromagnetic interference
FC	Flying capacitor
FOC	Field-oriented control
GaN	Gallium nitride
HEMT	High electron mobility transistor
IGBT	Insulated gate bipolar transistor
IMC	Internal model control
IR	Infrared
MOSFET	Metal-oxide semiconductor field effect transistor
NPC	Neutral-point-clamped
PCB	Printed circuit board
PLL	Phase-locked loop
PMSM	Permanent magnet synchronous motor
PWM	Pulse width modulation
Si	Silicon
SiC	Silicon carbide
VHF	Very high frequency radio range

1 Introduction

The everlasting pursuit of higher efficiencies and power densities has been an immense driving force in the development of power electronics, including semiconductor materials and devices. Silicon (Si) has been the primary choice for semiconductor device manufacturers. However, in recent years, wide band gap semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN), have emerged as viable candidates for the next generation of power semiconductor devices. After all, SiC and GaN power devices offer superior switching performance and lower channel on-resistance, when compared with similarly rated Si devices (Millan et al., 2014). This difference in performance originates from the electrical properties of the various semiconductor materials, presented in Table 1.1.

Table 1.1: Electrical properties of silicon, gallium nitride, and silicon carbide (Chow, 2015).

Material	Electric breakdown field [MV/cm]	Energy band gap [eV]	Electron velocity [10^7 cm/s]	Electron mobility [cm^2/Vs]	Thermal conductivity [W/cmK]
Si	0.2	1.12	1.0	1350	1.5
GaN	3.75	3.39	2.5	2000	1.3
SiC	2.0	3.26	2.0	720	4.5

A high electric breakdown field enables the semiconductor device to have a high voltage rating using a thinner drift region, which results in a low drain-source channel on-resistance. A high energy band gap, along with a high thermal conductivity, translates into a higher operating temperature owing to the temperature dependence of the energy band gap. The high temperature narrows the band gap, thus making it possible for the electrons excited by the thermal energy to cause unwanted current conduction. Moreover, the off-state leakage current is smaller in semiconductors with a high energy band gap. The high electron mobility makes it possible to build the device with a small die size, resulting in lower device input and output capacitances. With the small capacitances and high electron mobility, the semiconductor device is capable of high switching speeds; commercial GaN switches can have rise and fall times in the order of nanoseconds (GaN Systems, 2018b). However, the reliability and applicability of these emerging wide band gap devices have to be thoroughly researched before they can be viewed as a potential replacement for Si-based power devices.

Electrical motors are the workhorses of the industry, used in applications such as blowers, compressors, pumps, and conveyers. They can be divided into two main categories: constant- and variable-speed drives. A constant-speed drive is an electrical motor always

used at its nominal rotational speed, and the output power can be adjusted with mechanical throttles. A variable-speed drive system consists of an inverter paired up with an AC motor, whose rotational speed is controlled by the inverter, thus providing the wanted output power or rotational speed at all times. In blower and compressor applications, high-speed permanent magnet synchronous motors (PMSM) are an appealing option because of their small physical size, high power density, and high efficiency. Currently, industry standard drive systems employ inverters with Si-IGBTs, whose characteristics limit the usable switching frequency to the order of kilohertz. On the other hand, SiC and GaN power switches are capable of switching frequencies in the order of hundreds of kilohertz.

With the increased switching frequency, the physical size of the inverter system can be decreased, mainly because of the increased cut-off frequency of the output filter. This translates into lower filter inductor and capacitor values, which means smaller component sizes. However, the heat sink volume does not significantly change, as the increase in switching frequency also increases the switching losses. A further benefit is that an inverter with a high switching frequency produces sinusoidal current to the motor, thereby reducing the motor losses and torque ripple. Furthermore, a swift inverter response to the control signal command is due to the high switching frequency. Although high-speed switching edges may produce motor overvoltages, they can be mitigated with short motor cables and suitable inverter output filtering.

1.1 Gallium Nitride High Electron Mobility Transistors

GaN-based power semiconductor technology has made significant advancements in the last decade, with high electron mobility transistors (HEMTs) as the current superior device (Millan et al., 2014). Consequently, the commercial availability of GaN power switches has increased lately; products are available via online ordering from manufacturers such as EPC, Panasonic, Transphorm, and GaN Systems. EPC and GaN Systems have the widest product range, with switches capable of 100 V/90 A and 650 V/60 A. A more comprehensive review of commercial GaN power devices has been presented in (Jones et al., 2016).

HEMTs are field effect transistors, which means that they have a similar operating principle with MOSFETs. However, GaN HEMTs are capable of reverse conduction without an intrinsic body diode, while having no reverse recovery charge. An example of the reverse conduction characteristics of a GaN HEMT is presented in Figure 1.1.

The reverse conduction characteristics depend on the gate voltage; a negative gate voltage increases the reverse conduction threshold voltage. This means an increase in the conduction losses; however, a negative gate voltage is worthwhile to mitigate the possibility of a false turn-on in a bridge leg configuration. The optimum gate voltage in regard to false turn-on mitigation has been studied in (Xie et al., 2017).

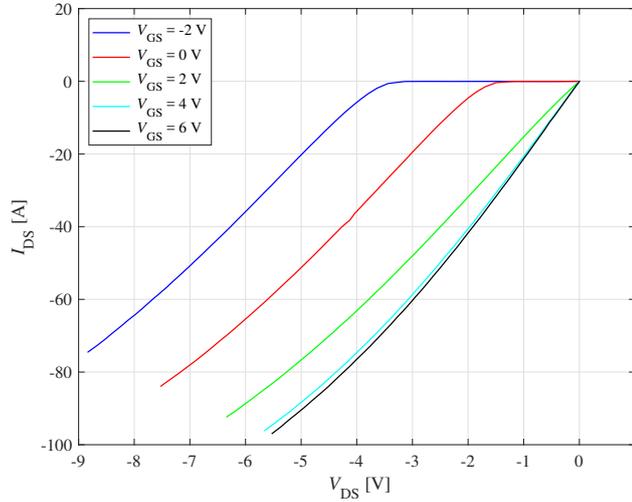


Figure 1.1: Measured reverse conduction characteristics of a GaN Systems GS66508T.

GaN semiconductor devices have an inherent feature called current collapse, where the drain current temporarily decreases after application of a high drain-source voltage (Joh et al., 2008), in other words, the on-state resistance of the channel increases. According to (Mizutani et al., 2003), the current collapse phenomenon, also known as dynamic on-resistance, is caused by electrons injected from the gate to the surface states in the gate-drain region. This hypothesis is supported by the research of (Meneghesso et al., 2006). In (Badawi et al., 2016), the authors suggest that the current collapse is caused by hot carrier injection during the switching events, which reduces the amount of channel charge carriers. A more in-depth review of the mechanics of current collapse is presented in (Jin and del Alamo, 2013). In (Joh et al., 2014), the authors state that current collapse is completely recoverable at a high temperature or under light, which further implies that the current collapse is related to electron trapping effects.

Many studies demonstrate that the current collapse phenomenon is caused by electron trapping. Furthermore, the magnitude of the trapping effects has been associated with different factors, such as:

- off-state drain-source voltage,
- off-state voltage stress time,
- field plate structure of the device,
- switching frequency,
- on-state gate voltage, and
- current stress during switching.

The impact of the off-state voltage magnitude and time has been studied in (Badawi et al., 2016), (Joh and del Alamo, 2011), and (Ishibashi et al., 2015). It is shown that the current collapse can increase up to 30% from a few hours of off-state stress with the nominal blocking voltage (Joh and del Alamo, 2011). The authors of (Ishibashi et al., 2015) state that a higher off-state voltage increases the current collapse phenomenon, which is backed up by the findings reported in (Badawi et al., 2016). In (Liao et al., 2015), it is shown that the device capacitances are also affected by the drain-source voltage stress.

The study by Saito et al. (2010a) discusses the effect of different field plate structures on the amplitude of the current collapse phenomenon. According to the study, a structure employing both a source and a gate field plate reduces the current collapse.

The effects of trapping and detrapping times, that is, the switching frequency and duty cycle, on the dynamic on-resistance of a commercial GaN HEMT have been studied in (Li et al., 2018). Similar studies have been presented in (Cai et al., 2017) with three commercial GaN switches. It is concluded that the detrapping time is longer than the trapping time, which indicates that a higher switching frequency increases the dynamic on-resistance. This conclusion is supported in (Ishibashi et al., 2015) and (Badawi et al., 2016).

In (Wang et al., 2017), the authors study the effect of gate voltage on current collapse. It is shown with a commercial GaN HEMT that a gate voltage of 5 to 6 V is enough to suppress the current collapse. However, the current collapse increases significantly with a lower gate voltage.

According to (Joh et al., 2014), the current collapse is smaller with hard switching, because holes generated by impact ionization under a high voltage and current stress compensate the trapped electrons, thus recovering the current collapse under hard switching. It is also discussed that the main cause of soft switching current collapse is surface trapping by gate leakage current. Alternatively, experimental evaluation in (Li et al., 2019) suggests that the current collapse and its relation to the switching current stress depend on the device structure.

Several studies have been conducted on the current collapse, and factors affecting the phenomenon have been identified. However, the studies have focused on the submicrosecond timescale phenomena associated with switching events. The long-term behavior of the channel resistance, from now on referred to as static channel resistance R_{ON} , has been studied only to a limited extent. A hint of static channel resistance behavior is presented in (Saito et al., 2010b). A 7 h switching test caused an R_{ON} increase between 7% and 15% on different samples, and after a rest period of two weeks, the channel resistances had not recovered to their initial states. These findings raise questions such as

- How drastically does R_{ON} increase with different switching conditions?
- What kinds of recovery characteristics does R_{ON} have?

These questions have to be answered to assess the feasibility and reliability of GaN HEMTs. This knowledge will also further aid in estimating the losses of power electronic systems employing GaN HEMTs.

1.2 GaN-based power electronics

The applicability of GaN devices in the field of power electronics has been a hot topic for almost a decade, and has gained even more interest as the commercial availability of GaN switches has increased. Before the commercialization, the high switching frequency capabilities of power GaN switches were demonstrated by DC/DC converters employing self-fabricated switches. A 100 W one switch boost converter, presented in Figure 1.2, with a 850 kHz switching frequency was introduced by Das et al. (2011), whereas converters with a 1 MHz switching frequency were reported by Saito et al. (2008) and Wu et al. (2008), with 120 W and 300 W power ratings.

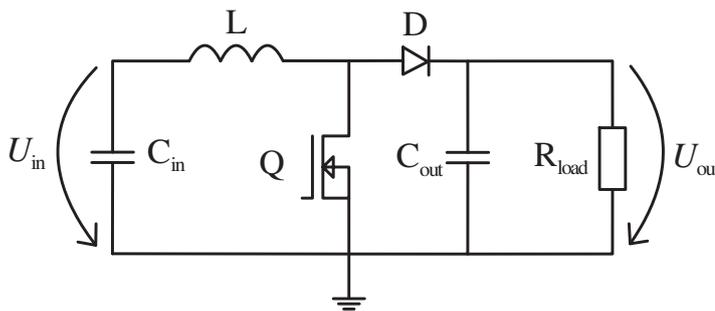


Figure 1.2: 1 switch boost converter topology.

Furthermore, a resonant converter was presented by Ueda (2014), with a 1 MHz switching frequency and a 1 kW power rating. The primary side consists of a full-bridge, connecting to the diode rectifier secondary side through a center-tapped transformer, depicted in Figure 1.3.

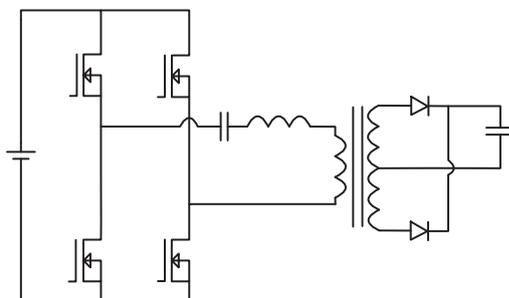


Figure 1.3: LLC resonant converter topology by (Ueda, 2014).

As an alternative, the high efficiency capabilities of power GaN switches were demonstrated in a 900 W three-phase inverter, shown in Figure 1.4, employing self-fabricated switches by Morita et al. (2011), with a reported peak efficiency of 99.3% using a 6 kHz switching frequency.

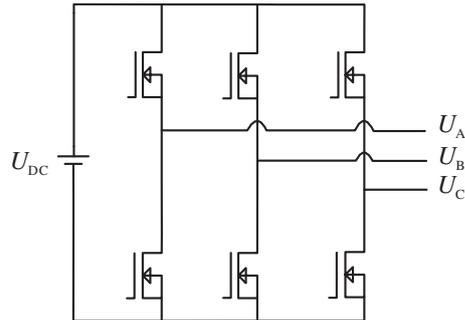


Figure 1.4: Three-phase inverter topology.

In recent years, several studies have been published on power converters applying commercial GaN switches. Different DC/DC converter topologies have been investigated, such as LLC resonant half- and full-bridges, along with isolated full-bridge buck and one-switch boost converters. The inverter studies have focused on one- and three-phase full-bridge topologies; however, three-level active neutral-point-clamped (ANPC) and T-type topologies have also been reported.

Huang et al. (2014) and Zhang et al. (2017) demonstrated 300 W LLC resonant converters consisting of primary and secondary side half-bridges, together with a secondary side center-tapped transformer. The prototype by Huang et al. (2014), shown in Figure 1.5, had 600 V switches (Transphorm TPH2002) on both bridges, a 1 MHz switching frequency, and 96% peak efficiency.

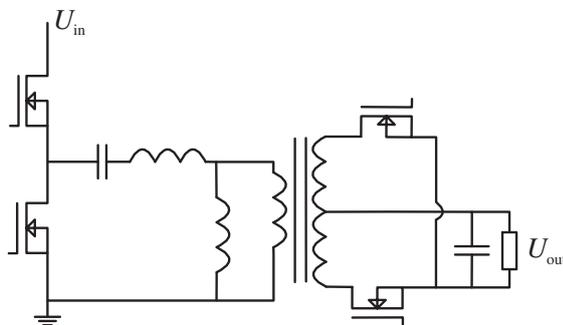


Figure 1.5: LLC resonant topology by (Huang et al., 2014).

Further, Zhang et al. (2017) implemented a prototype with 600 V switches (Transphorm TPH3006PS) on the primary side, and 40 V switches (EPC2015 by EPC) on the secondary side as shown in Figure 1.6. The switching frequency was 1 MHz and the peak efficiency 96.8%.

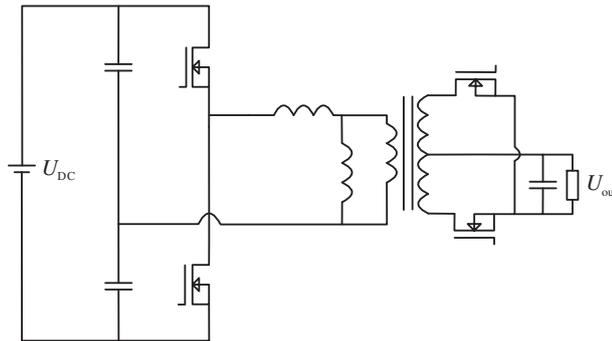


Figure 1.6: LLC resonant topology by (Zhang et al., 2017).

A 400 W, 1.2 MHz LLC resonant converter was introduced by Reusch and Strydom (2015), with a full-bridge on the primary side and a center-tapped transformer paired with a half-bridge on the secondary side, Figure 1.7. The primary side switches were EPC2001, 100 V, and the secondary switches were EPC2015, 40 V, with a peak efficiency of roughly 96.5%.

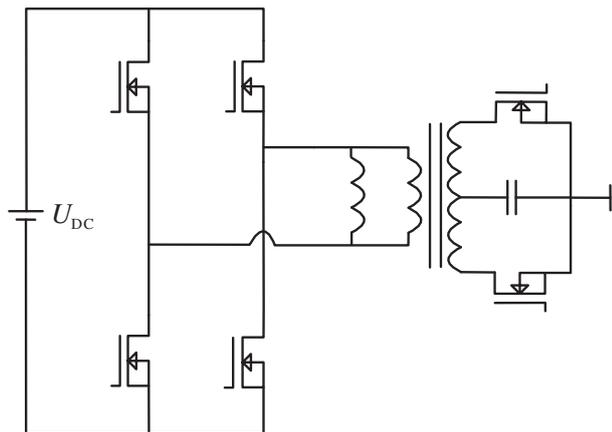


Figure 1.7: LLC resonant topology by (Reusch and Strydom, 2015).

Ramachandran and Nymand (2016) built a 2.4 kW, 500 kHz isolated full-bridge buck converter with full-bridges on both sides of the transformer, presented in Figure 1.8.

The primary switches were EPC2010C, rated at 200 V, and the secondary switches were EPC2001C, 100 V. The prototype exhibited a peak efficiency of 98.8%.

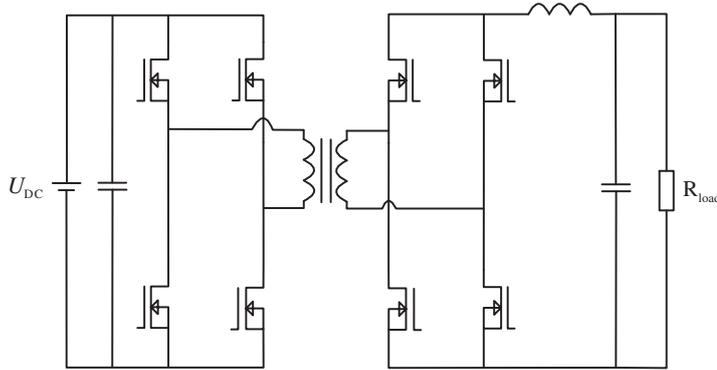


Figure 1.8: Isolated full-bridge buck topology presented in (Ramachandran and Nymand, 2016).

One-switch boost converters, shown in Figure 1.2, were also studied by Mitova et al. (2014) and Wu et al. (2014), with rated powers of 500 W and 3 kW. Mitova et al. (2014) used 600 V rated switches manufactured by Transphorm; however, the model was unspecified. The prototype was operated with a 25–500 kHz switching frequency and achieved a peak efficiency of 98.8% with 100 kHz switching frequency. Wu et al. (2014) implemented their prototype with unspecified switches from Transphorm and achieved a 99% peak efficiency with a 100 kHz switching frequency and a 800 V output voltage.

One-phase full-bridge inverters, demonstrated in Figure 1.9, have been studied in (Lin et al., 2015) and (Zhao et al., 2016), both of which used a 100 kHz switching frequency. Lin et al. (2015) built a 500 W inverter with Transphorm TPH3002 switches, and achieved a peak efficiency of 98%, whereas Zhao et al. (2016) measured a 97.6% peak efficiency from their 2 kW prototype, which used GaN Systems GS66508T switches.

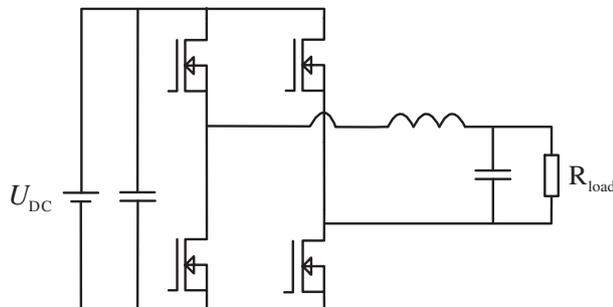


Figure 1.9: One-phase full-bridge inverter topology.

A 850 W one-phase ANPC inverter prototype, illustrated in Figure 1.10, was constructed by Gurpinar et al. (2016a), employing GaN Systems GS66508T switches and a 10 kHz switching frequency, with a measured peak efficiency of 99.7%.

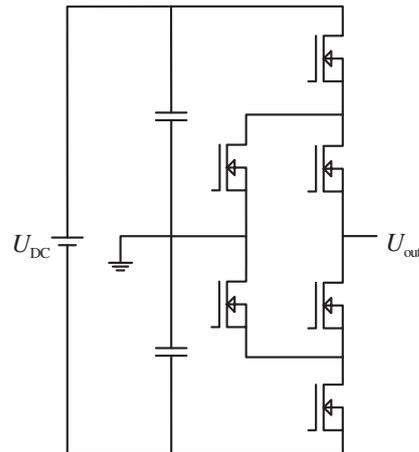


Figure 1.10: One-phase active neutral-point-clamped inverter.

A T-type inverter, shown in Figure 1.11, rated at 2.5 kW power, was reported by Gurpinar and Castellazzi (2016), reaching a 97.3% peak efficiency with a 160 kHz switching frequency, and 99.2% with 16 kHz. The GaN HEMTs used in the study were Panasonic PGA26A10DS.

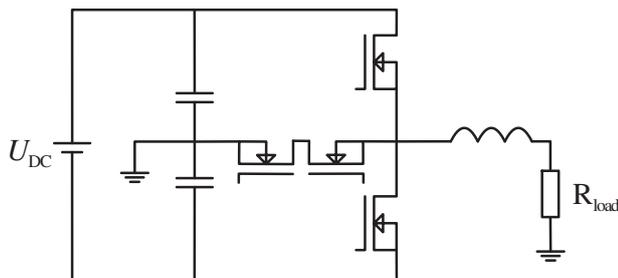


Figure 1.11: One-phase T-type inverter topology.

Studies on a three-phase two-level inverter, presented in Figure 1.4, have been conducted by Lautner and Piepenbreier (2016), Shirabe et al. (2014), and Li et al. (2016). The prototype by Lautner and Piepenbreier (2016) was constructed with GaN Systems GS66508T switches and a 100 kHz switching frequency. The rated power was 1.5 kW and the measured peak efficiency 97%, which included the losses of the output sine wave filter. Shirabe et al. (2014) introduced a 2 kW inverter with a 97.98% peak efficiency, including the output sine wave filter losses, built with 100 kHz and Transphorm TPT3044M

switches. The 10 kW inverter implemented by Li et al. (2016) employed GaN Systems GS66516T switches with a 50 kHz switching frequency, and achieved a 98.8% peak efficiency.

Overall, several reports have been published of power electronic converters employing commercial GaN switches from different manufacturers, whilst reaching high efficiencies. With the high-speed switching capabilities of GaN HEMTs, it is possible to achieve systems with higher power densities and smaller sizes than similarly rated Si-based converters.

1.3 Motivation of the study

Usually, electrical power is transferred through several power electronic stages, whether the final destination is in the industry or in domestic applications. Owing to this chaining, the overall efficiency of the process is dependent on the individual efficiencies of the power electronic stages. Thus, even a marginal efficiency improvement of a single power stage may result in considerable energy savings in the bigger picture. With higher efficiencies, the power electronic stages have less losses, which translates into smaller cooling systems, i.e., higher power density.

GaN HEMTs are an emerging technology for high efficiency, high power density applications. However, the uncertainties created by the current collapse phenomenon are an obstacle to the broad acceptance of GaN HEMTs. Therefore, it is vital to identify the long-term behavior of the current collapse and its effect on the channel resistance, and furthermore, the implications for the losses of GaN HEMTs. Once these issues are solved, GaN HEMTs can be viewed as a real competitor for Si-based devices.

The high-speed switching capabilities of GaN HEMTs are excellent, as has been demonstrated with DC/DC converter prototypes. However, to the author's knowledge, these capabilities have so far not been displayed in high rotational speed electrical drives, even though a high switching frequency enables the drive to have less bulky filter components, thus decreasing the overall system size. Moreover, a high switching frequency inverter provides the motor with sinusoidal current, reducing the motor losses and torque ripple. Therefore, the potential of GaN HEMTs in high switching frequency electrical drive systems is an extremely attractive topic.

1.4 Outline of the doctoral dissertation

Besides the first introductory chapter, the outline of this doctoral dissertation is as follows:

Chapter 2 addresses the study of the channel resistance behavior of GaN HEMTs on a macro timescale. The prototype constructed in the study is introduced together with the measurement equipment and procedures. The effects of different switching conditions on the channel resistance of the GaN HEMTs are demonstrated by measurement results.

Chapter 3 presents the design of the high-speed drive system, which is based on PMSM specifications. The drive design consists of inverter topology selection, PCB design, output filter dimensioning, and sensorless motor control design and tuning.

Chapter 4 reports simulation results of the sensorless motor control. The field-oriented control signals, such as dq-axis currents and voltages, along with the estimated motor rotational speed are presented. Moreover, the operation of the DC link control is shown.

Chapter 5 provides experimental results of the ANPC inverter, including the line-to-line voltage, line-to-neutral voltage, and load current. Additionally, thermal images of the prototype are shown.

Chapter 6 summarizes the conclusions of the doctoral dissertation. Further, suggestions for future work are presented.

1.5 Scientific contributions

The research done in this doctoral dissertation can be divided into two parts; the study into the current-collapse-induced phenomenon on the GaN HEMTs, and the implementation of the high-speed drive system employing GaN HEMTs.

The current collapse phenomenon has been studied on a timescale associated with switching events; however, the mechanisms causing the phenomenon suggest that the trapped electrons accumulate over longer time periods. This results in an increase in the static channel resistance, which directly translates into increased conduction losses. The experimental results presented in this dissertation provide insight into the channel resistance behavior after varying switching stresses, which ultimately can be used to estimate the actual conduction losses of GaN HEMTs.

Three-phase inverters employing GaN HEMTs have been reported with a maximum switching frequency of 100 kHz. The three-phase ANPC inverter prototype built in this doctoral dissertation was operated with a 1 MHz switching frequency, making it a trailblazer in the field of high switching frequency three-phase inverters. The 1 MHz switching frequency enables the volume of the output filter to be decreased to a fraction of the volume of an

output filter paired with a similarly rated commercial inverter employing Si IGBTs. This proves the superior power density potential of GaN HEMTs in electrical drives. Furthermore, sinusoidal inverter output voltage and current waveforms, which would result in low motor losses and torque ripple in an electrical drive, were observed.

The scientific contributions of this doctoral dissertation can be summarized as follows:

- Knowledge about the increase in static channel resistance induced by current collapse on a macro timescale,
- Design of a high-speed drive system and its control system,
- Implementation of a 1 MHz switching frequency three-phase ANPC inverter employing GaN HEMTs,
- Assessment of the applicability of GaN HEMTs in a high-speed electrical drive system.

1.6 Scientific publications

This doctoral dissertation contains material from the following publications.

- Järvisalo, H., Korhonen, J., Honkanen, J., and Silventoinen, P., "Considerations for a high-speed PMSM drive featuring a GaN-ANPC inverter," *Proceedings of the 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Warsaw, September 2017
- Järvisalo, H., Korhonen, J., Aalto, H. M., and Silventoinen, P., "Macro Timescale $R_{DS,on}$ Phenomena in GaN HEMTs," *Proceedings of the 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, Riga, September 2018
- Järvisalo, H., Korhonen, J., Nykyri, M., and Silventoinen, P., "Channel resistance behavior of GaN HEMTs: an experimental study", *Proceedings of the 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA 2019)*, Raleigh, October 2019

The publications are peer reviewed and presented in the premier conferences in the fields of power electronics and wide band gap devices and their applications. The author of this doctoral dissertation is the main author in all the publications.

1.7 Scientific methods

The scientific methods applied in this doctoral dissertation are simulations and experimental measurements. The operation of the high-speed drive system is simulated with MATLAB Simulink; the simulations comprise control system tuning as well as verification of the filter design and the sensorless motor control. The simulation parameters used in the study are explained in detail in Chapter 4.

To investigate the current-collapse-induced channel resistance behavior of GaN HEMTs, a full-bridge prototype is built. Different switching stresses are applied to the GaN HEMTs, and the channel resistance is then measured using a power device analyzer. A further analysis is done with the aid of MATLAB. A more detailed description of the measurement setup and procedure is provided in Chapter 2.

To assess the applicability of GaN HEMTs in high switching frequency high speed electrical drives, a 1 MHz switching frequency three-phase ANPC inverter prototype is implemented. The design of the prototype is presented in Chapter 3. Experimental measurements are performed with an oscilloscope to evaluate the inverter output voltage and current waveforms, which are further analyzed with MATLAB. The measurement setup is presented in full detail in Chapter 5.

2 Macro timescale channel resistance behavior of GaN HEMTs

The first AlGaIn/GaN HEMT was reported by Asif Khan et al. (1993). From there on, the development was directed toward microwave power devices, and a HEMT with a power density of 1.1 W/mm was demonstrated by Wu et al. (1996). After a decade of research, a GaN HEMT with a power density of 40 W/mm was presented in (Wu et al., 2006). These results in high power microwave applications propelled the research in the field of power electronic switches, and GaN HEMTs suitable for power electronics were displayed in (Wu et al., 2008) and (Saito et al., 2008). With the continued advancements in the design and fabrication processes, commercial power GaN HEMTs have become readily available in the 2010s. However, the issues caused by the current collapse phenomenon have not been decisively solved yet.

It is postulated in several studies that the current collapse phenomenon is caused by electron trapping effects, more precisely, induced by surface states. To help to understand the mechanics of the electron trapping effects, a basic structure of a normally-off power GaN HEMT is illustrated in Figure 2.1.

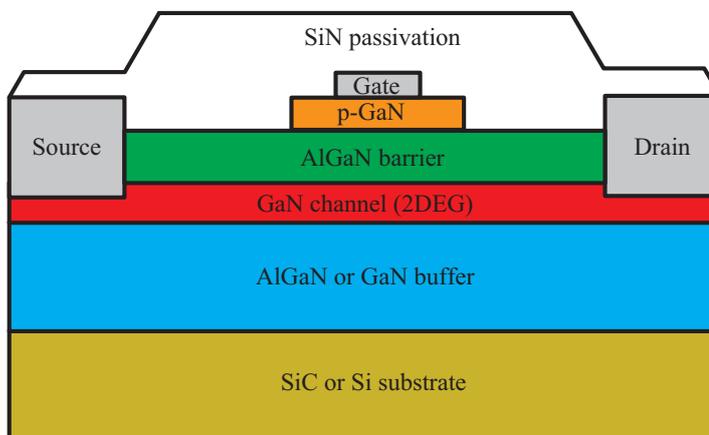


Figure 2.1: Basic structure of a normally-off GaN HEMT with a p-GaN gate (Badawi et al., 2016).

In a nutshell, the operation principle of the GaN HEMT is based on the two-dimensional electron gas (2DEG) formed in the AlGaIn-GaN heterojunction, which acts as the channel for the charge carriers during a gate-source forward bias.

In an AlGaIn-GaN heterostructure, charge sheets of opposite polarity at the surfaces of the AlGaIn layer are caused by spontaneous and piezoelectric polarization effects (Ambacher et al., 1999). However, a positive charge sheet has to be present at the AlGaIn surface for the 2DEG to form in the GaN channel. This positive charge can be acquired by donor-like

surface states located at an appropriate energy level (Ibbetson et al., 2000). With a negative charge on the AlGaN surface, the channel is depleted of electrons, further extending the gate depletion region and forming a "virtual gate" (Vetury et al., 2001). These virtual gates lead to delayed I_D switching, that is, current collapse.

Because of the potential barrier at the AlGaN-GaN heterojunction, the low-energy electrons in the channel are unable to interact with the surface states. However, during a high drain voltage stress, hot electrons in the channel can gain enough energy to overcome the potential barrier and get trapped at the surface. Furthermore, electron tunneling from the gate to the surface states can occur (Meneghesso et al., 2004).

These hypotheses are supported by the results in (Hwang et al., 2013) and (Joh et al., 2014). Both studies show that the gate leakage electrons during off-state operation are a significant reason for the current collapse phenomenon. In addition, hot electrons in the channel during switching are trapped on the AlGaN layer surface, rather than the buffer layer (Hwang et al., 2013).

It has been concluded that the origin of the current collapse phenomenon is related to electron trapping effects. Trapping occurs during GaN HEMT blocking mode operation, and correspondingly, detrapping takes place during the conduction mode (Li et al., 2018). However, it has been discovered that the detrapping process is slower than the trapping process, as illustrated in Figure 2.2.

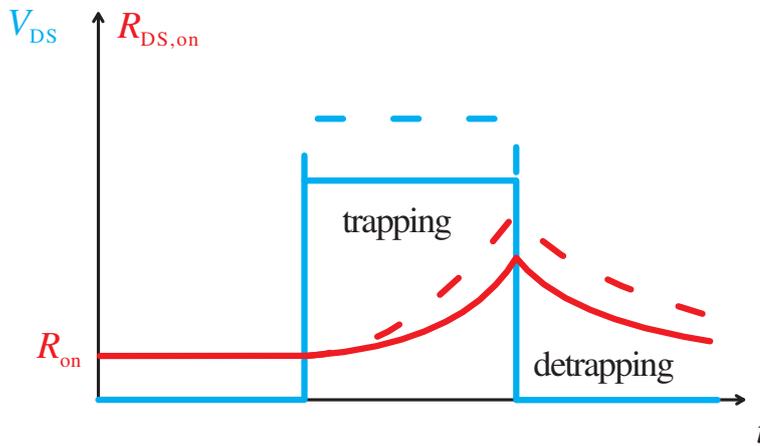


Figure 2.2: GaN HEMT $R_{DS,on}$ behavior caused by electron trapping effects (Li et al., 2018).

Even though the bulk of the detrapping happens on a submicrosecond timescale, some electrons remain trapped for a longer time period, which means an increase in the static channel resistance R_{ON} . To study the channel resistance behavior of GaN HEMTs on the macro timescale, a practical approach was adopted. A prototype was built to apply

different switching stresses to the GaN HEMTs, and after those stresses, the channel resistance behavior was studied with a power device analyzer.

2.1 Prototype implementation

The channel resistance measurements were carried out with a Keysight B1505A power device analyzer. The commercial switches under research were GaN Systems GS66508T, which were in a GaN^{PX}® surface-mount package, depicted in Figure 2.3. The power device analyzer has a plug-in slot compatible with TO-220 and TO-247 packaged devices. Therefore, the GaN switches were soldered into TO-247 adapters for compatibility.

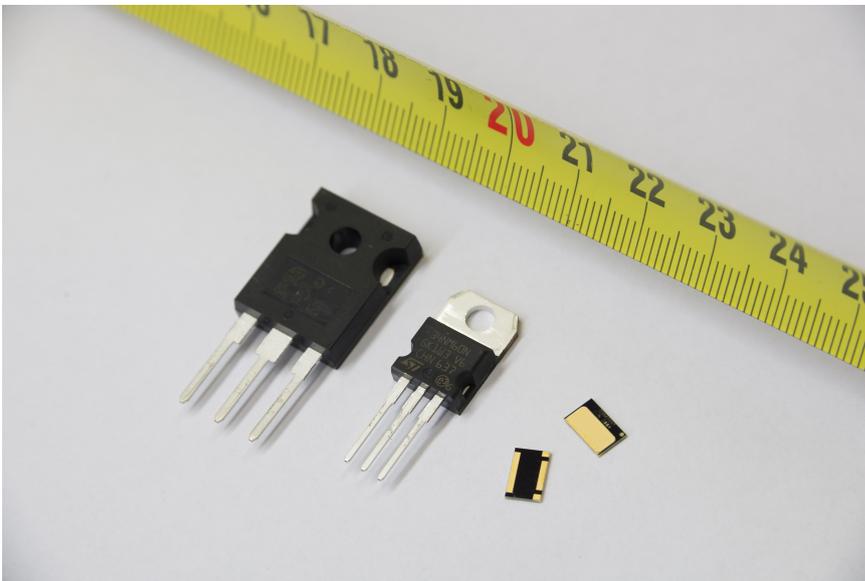


Figure 2.3: Comparison of similarly rated (650 V / 30 A) switches. On the left a TO-247 packaged MOSFET, in the middle a TO-220 packaged MOSFET, and on the right GaN Systems GS66508T.

A full-bridge converter prototype, shown in Figure 2.4, was built to stress the GaN HEMTs with different switching conditions. The switch connections were implemented with screw terminals to achieve fast detachability and a low mechanical and thermal stress on the GaN devices when they are moved from the full-bridge prototype to the power device analyzer.

To induce the current collapse phenomenon on the GaN HEMTs, the switches were put under different stresses. The variables were stress time, current stress, and switching frequency. The stress setups were performed with a 400 V DC link voltage, which corresponds to a 400 V off-state voltage stress on each HEMT. The tests without current stress

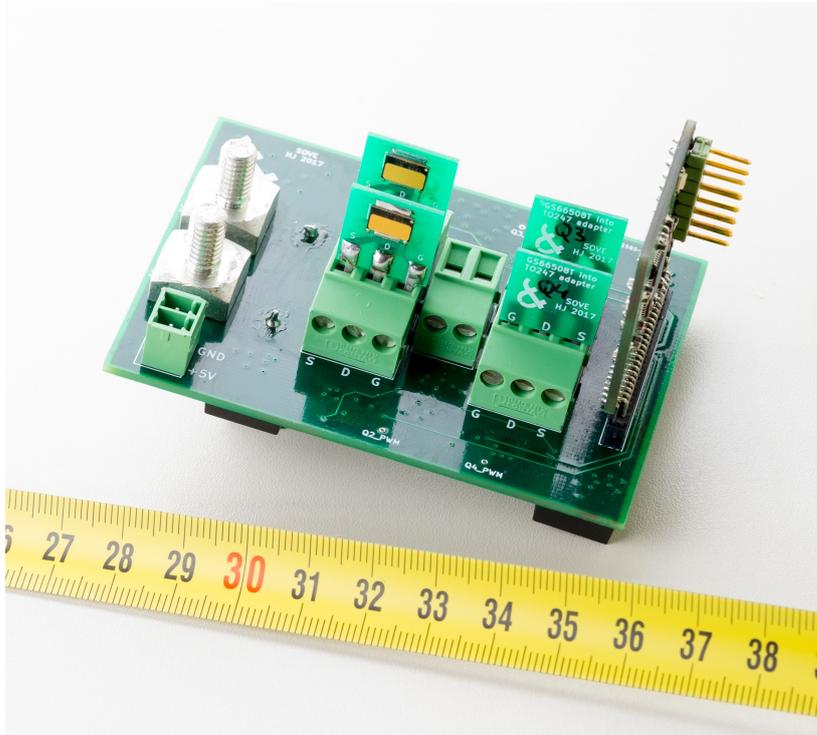


Figure 2.4: Prototype of the full-bridge converter with pluggable GaN HEMTs.

were carried out using a half-bridge configuration, presented in Figure 2.5. Correspondingly, the tests with current stress were done with a full-bridge configuration, as shown in Figure 2.6.

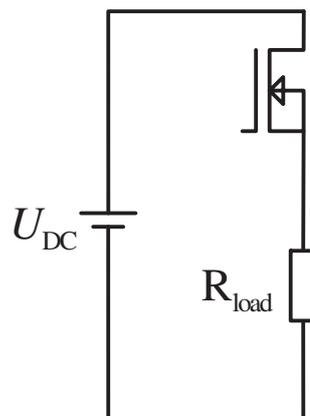


Figure 2.5: Half-bridge topology used for zero current stress.

Because of the time-critical nature of the current collapse phenomenon, only one switch was stressed at once, and a duty cycle $D=0.5$ was used. The lower switch was replaced with a $100\text{ M}\Omega$ resistor to ensure zero current conduction.

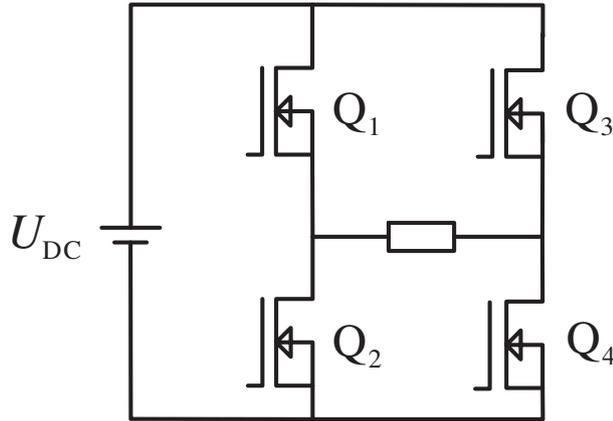


Figure 2.6: Full-bridge topology used for current stress.

The full-bridge was operated with bipolar PWM, that is, Q_1 and Q_4 conduct simultaneously, while Q_2 and Q_3 are in the blocking mode, and vice versa. The switches were hard switched, and $D=0.75$ was employed for Q_1 and Q_4 , and correspondingly, $D=0.25$ for Q_2 and Q_3 . Although four switches were stressed simultaneously, the R_{ON} change was measured from only one switch because of the restrictions set by the power device analyzer used in the study.

2.2 Measurement setup

After the switching stress, R_{ON} of the stressed GaN HEMT was measured with the power device analyzer using a four-wire measurement. Each stress test was performed on four different switches. There was approximately a 1 min delay between the stress test and channel resistance measurement, which was caused by the transfer of the stressed switch from the PCB prototype to the power device analyzer.

In the channel resistance measurement, a constant gate voltage of 6 V was used, and $10\ \mu\text{s}$ current pulses up to 50 A were conducted through the channel at 1 s intervals. The drain-source voltage was measured during each current pulse, and the channel resistance was calculated from the measured voltage and current. An example of the measurement results, with the measurement accuracy at a confidence interval of 95 %, is presented in Figure 2.7.

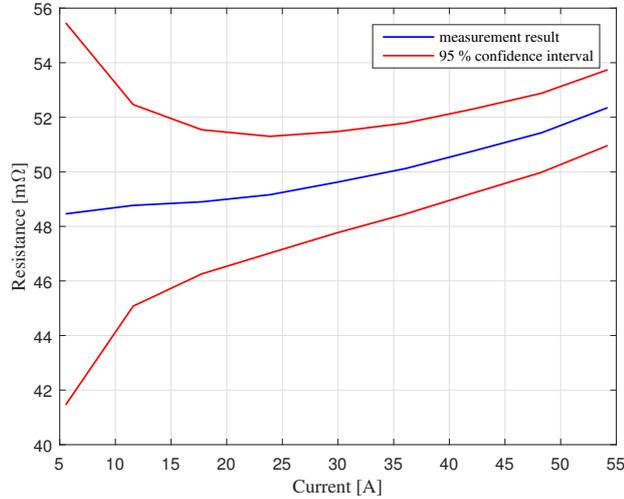


Figure 2.7: R_{ON} measurement results of a single GaN HEMT.

As can be seen from Figure 2.7, the measurement accuracy increases with higher current values; the highest accuracy with the 95% confidence interval ($\pm 1.5 \text{ m}\Omega$) is achieved around 50 A current. The precision of the power device analyzer is adequate for identifying the current collapse phenomenon; however, the measurement accuracy is not enough to definitively assess the channel resistance value.

Owing to the time-critical nature of the current collapse phenomenon, the recovery behavior was observed with consecutive R_{ON} measurements. Forty measurements were performed for one switch, which corresponds to a recovery time of approximately 10 min. Because each GaN HEMT has a unique channel resistance value, the channel resistance behavior was studied in percentages. For each individual switch, a prestress R_{ON} curve was measured and then compared with the curve measured after stress. The R_{ON} value at the 50 A current was studied from each of the curves. These values were then plotted against time. The measurement and data analysis procedure is illustrated in Figure 2.8.

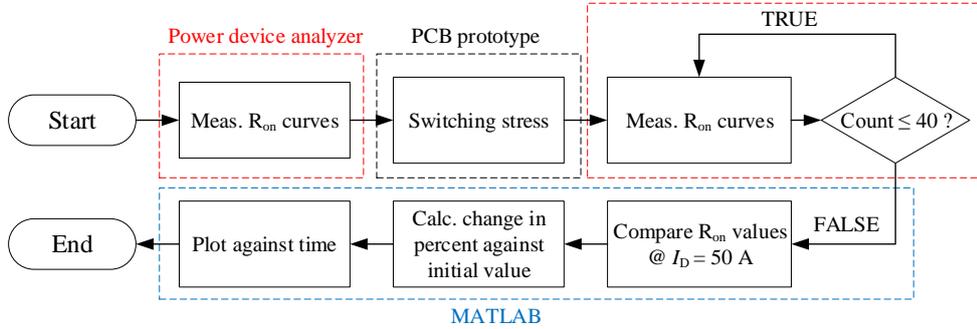


Figure 2.8: Flowchart of the measurement procedure of a single GaN HEMT.

The procedure presented in Figure 2.8 was performed four times on different GaN HEMTs for each test to improve the reliability of the results and decrease the statistical variance.

According to (Joh et al., 2014), current stress on the channel recovers the current collapse. Therefore, it is possible that the measurement process of the power device analyzer has an effect on the recovery characteristics of the channel resistance. To identify this relation, the measurement procedure was performed on five unstressed GaN HEMTs. The results are shown in Figure 2.9.

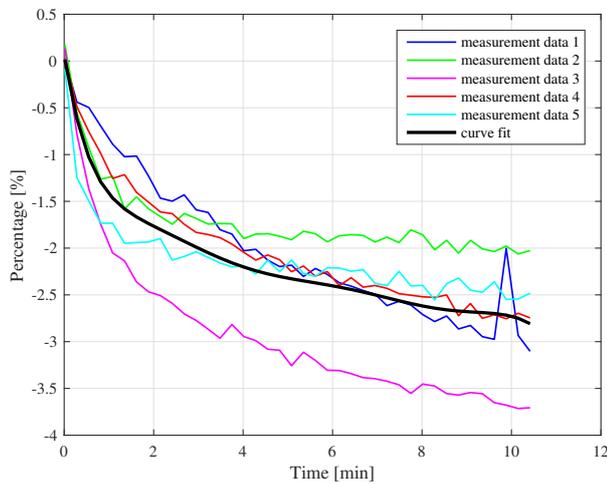


Figure 2.9: R_{ON} behavior caused by the power device analyzer measurement process.

It can be seen that the measurement process of the power device analyzer decreases the channel resistance of the measured GaN HEMT. A mean value curve is fitted based on the measurement data. This curve is used to compensate the effect of the measurement process on future results.

2.3 Measurement results

The measurement results of the R_{ON} behavior of GaN HEMTs are presented in this section. The effects of stress time, switching frequency, and current stress were studied.

2.3.1 Zero current stress

One of the factors affecting the magnitude of the current collapse phenomenon is the off-state drain-source voltage stress. Thus, it is relevant to study the R_{ON} behavior after DC stress. GaN HEMTs could be exposed to long DC stresses for example when employed in a solar inverter when the sun is not shining, or in a running electrical vehicle that is stationary. Measurement results after DC voltage stresses are depicted in Figure 2.10.

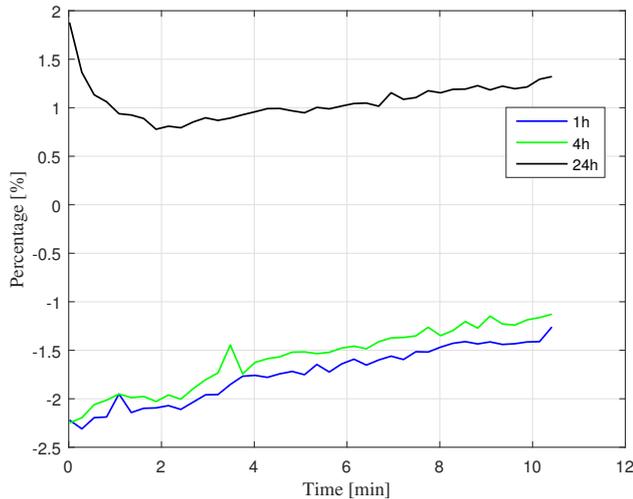


Figure 2.10: R_{ON} values after DC voltage stress with different stress times.

It can be interpreted from Figure 2.10 that DC voltage stress actually reduces the channel resistance with shorter stress times. However, with a 24 h stress time, R_{ON} is approximately 2% higher than the measured prestress value immediately after the stress. For the first 2 min of recovery after the 24 h stress, R_{ON} decreases, but after that it reaches a steady rate of change, similar to the recovery speeds of the 1 and 4 h stress tests.

After the DC stress tests, the HEMTs underwent different switching stresses. The HEMT was used in a half-bridge configuration (shown in Figure 2.5) with no load. The applied switching frequency was varied, and then continuously switched for the respective stress time. After this, the HEMTs R_{ON} characteristics were measured with the power device analyzer.

Low frequencies (under 1 kHz) experienced by the switches may be encountered for example in an ANPC converter, in which switches 1 and 4 are in off-state for the duration of a half-cycle of the fundamental frequency. Hence, stress tests with 50 Hz and 750 Hz switching frequencies were performed, whose measurement results are presented in Figure 2.11.

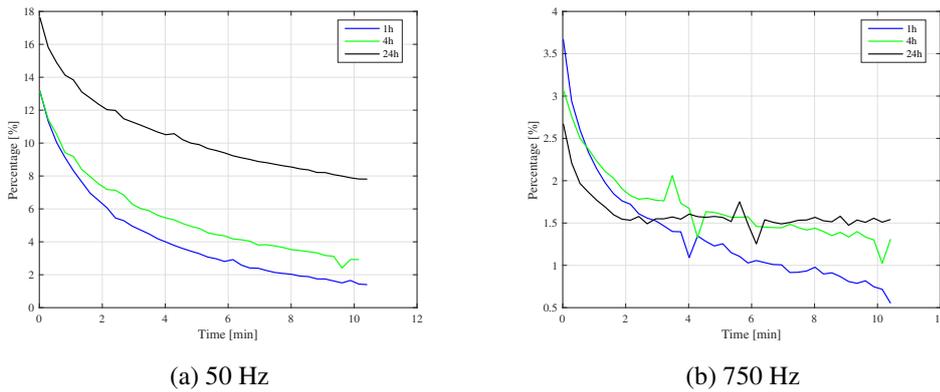
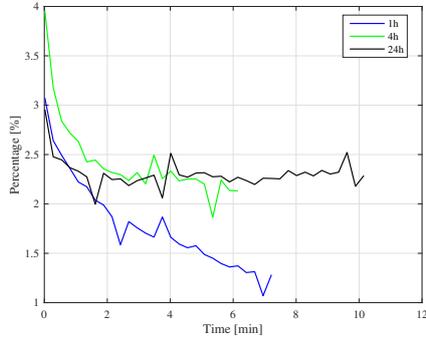


Figure 2.11: R_{ON} values after low switching frequency stresses.

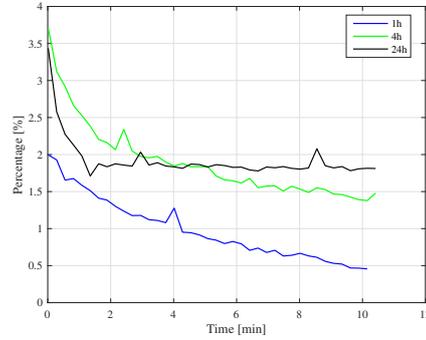
From Figure 2.11a, it can be seen that the 50 Hz switching frequency has a significant effect on the channel resistance of the GaN HEMTs under study. After 1 and 4 h stress times, the initial increase in R_{ON} is 13%. This increase recovers to approximately 1.5% in 10 min for the 1 h stress test, and correspondingly, to 3% for the 4 h stress test. As for the 24 h stress time, the first measurement has an R_{ON} increase of slightly under 18%. During the 10 min measurement period, the channel resistance recovers to an 8% increase. Thus, it can be stated that a longer switching stress time increases R_{ON} . Further, the recovery rate is slower for longer stress times.

The results in Figure 2.11b show that the highest initial increase in R_{ON} , roughly 3.5%, occurs with the 1 h stress test, followed by the 4 h test (3% increase), and finally, the 24 h test (2.5% increase). However, the recovery rate follows the same pattern as in the 50 Hz stress test; with the lowest stress time, the recovery rate is the highest. After the 10 min measurement period, the channel resistance has recovered by 3% for the 1 h test, roughly 1.5% for the 4 h test, and 1% for the 24 h test. Interestingly, the R_{ON} behavior after the 24 h test differs from the behavior of the shorter tests; after 2 min, the channel resistance settles to a constant value, whereas the R_{ON} keeps decreasing for the shorter test times.

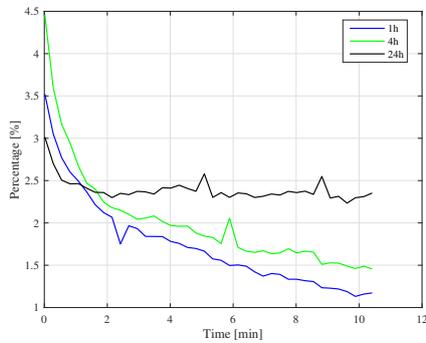
To identify the effect of plausible switching frequencies used in a converter, stress tests were performed with 100 kHz, 200 kHz, 500 kHz, and 1 MHz switching frequencies. The channel resistance measurement results are depicted in Figures 2.12 and 2.13.



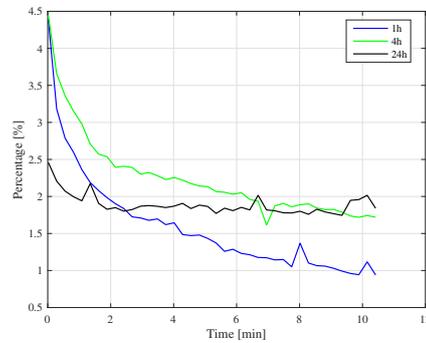
(a) 100 kHz



(b) 200 kHz



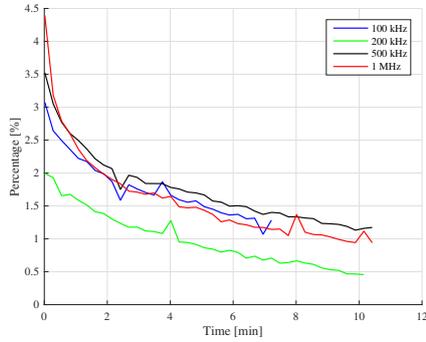
(c) 500 kHz



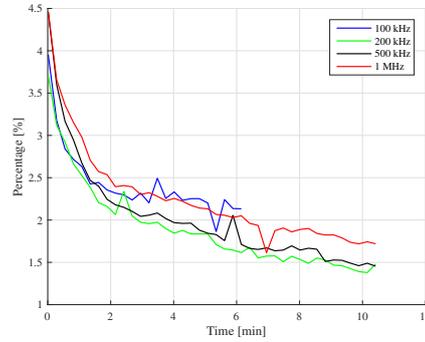
(d) 1 MHz

Figure 2.12: R_{ON} values after high switching frequency stresses.

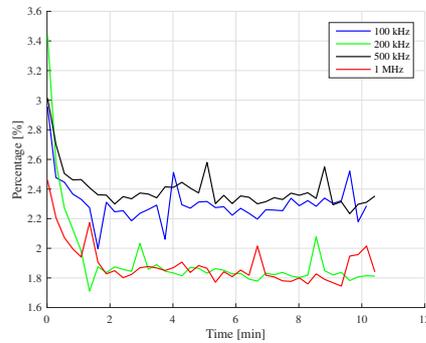
Based on Figure 2.12, it can be stated that with all the different switching frequencies, the stress time has a similar effect on R_{ON} . After 1 and 4 h stress times, the channel resistance recovers towards its prestress value. The recovery rate is slightly higher after 1 h tests than after 4 h tests. However, R_{ON} does not fully recover to its prestress value in 10 min. After the 24 h stress tests, R_{ON} decreases to a constant value in 2 min, which remains higher than the prestress value during the 10 min measurement period.



(a) 1 h stresses with different frequencies



(b) 4 h stresses with different frequencies



(c) 24 h stresses with different frequencies

Figure 2.13: Comparison of the R_{ON} values after different stress times.

The stress tests with the same stress time exhibit uniform R_{ON} recovery behavior, regardless of the switching frequency, as can be interpreted from Figure 2.13. Some variance is observed in the initial measurement values between different frequencies, yet the R_{ON} recovery rate is consistently similar. The differences in the initial values could be caused by the time taken to transfer the stressed HEMT from the PCB prototype to the power device analyzer; after all, the recovery characteristics are very time-critical. After the 10 min measurement period, the R_{ON} values of the 1 h tests are between 0.5 and 1.2%, whereas the R_{ON} values of the 4 h tests are between 1.5 and 1.7%, and for the 24 h tests between 1.8 and 2.4%. These findings further confirm that a longer stress time results in a slower recovery. The applied switching frequency does not have a great significance on the R_{ON} behavior of the stressed GaN HEMTs.

2.3.2 Current stress

The current collapse phenomenon is very apparent in the zero current 50 Hz tests. Therefore, the effect of current stress was studied with a 50 Hz switching frequency and a 1 h stress time. Four switches were operated with $D=0.25$, and correspondingly, four switches with $D=0.75$. The current stress was 1 A. The measurement results are illustrated in Figure 2.14.

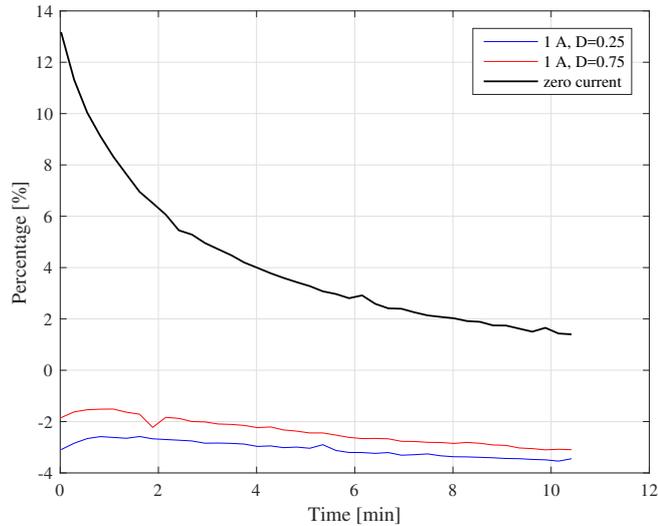


Figure 2.14: R_{ON} values after 1 h 50 Hz switching stresses.

It can be interpreted from Figure 2.14 that even a 1 A current stress effectively nullifies the current collapse phenomenon as the poststress R_{ON} values in percentage are negative. When comparing the results with and without current stress, the differences in the channel resistance behavior are very distinct. Additionally, differences in R_{ON} between different duty cycles are observed, and contrary to the theory presented in Figure 2.2, the tests with a lower duty cycle, that is, a longer trapping time, resulted in a lower channel resistance.

2.3.3 Conclusions on the macro timescale $R_{DS,on}$ phenomena

The measurement results show that after switching with no current stress, R_{ON} increases as a result of the current collapse phenomenon. However, the increase in the channel resistance is not permanent but recovers in the time range of minutes. The phenomenon is evident with low switching frequencies such as 50 Hz, where the highest R_{ON} increase was 18%. However, with switching frequencies ranging from 750 Hz to 1 MHz, the maximum R_{ON} increase is 4.5%. In this frequency range, the measurement results also suggest that the difference in the R_{ON} behavior between various switching frequencies is not too significant. Instead, the stress time is the decisive factor in the static channel resistance behavior; with longer stress times, the recovery rate of the channel resistance is lower. However, in all cases, the static channel resistance recovers to its prestress value.

The measurement results after switching with current stress show differing R_{ON} behavior when compared with the zero current measurement results. After current stress, the channel resistance is nearly constant, and the change in the R_{ON} value in percent is smaller. Based on these findings, it can be stated that current stress in the channel significantly mitigates the current collapse.

Based on these results, it is suggested that the current collapse phenomenon affects the static channel resistance R_{ON} ; however, the effect is not permanent but recovers during a rest period of minutes. Nonetheless, it has to be taken into account when evaluating conduction losses of GaN HEMTs. A channel resistance of at least 10% higher than nominal should be considered in the thermal design. Moreover, the dynamic on-resistance $R_{DS,on}$ increases the switching losses, but its effect cannot be assessed with the results in this doctoral dissertation.

3 Design and implementation of the drive system

The basis of the drive system design was the available high-speed PMSM. The inverter was implemented according to the motor specifications, presented in Table 3.1.

Table 3.1: Specifications of the PMSM used in the study.

Power	3.5 kW
Rotational speed	45 krpm
Torque	0.74 Nm
Pole pairs	1
Electrical frequency	750 Hz
Phase voltage	230 V
Phase current	5.6 A

The design procedure of the 3.5 kW PMSM is described in (Uzhegov et al., 2016). The motor has active magnetic bearings (AMB). In this chapter, the design and implementation of the high-speed drive system is addressed.

3.1 Inverter topology

The inverter design was based on the necessary voltage fed to the motor and the applied voltage and current ratings of the switches. The rated RMS voltage of one motor phase is 230 V, which means a phase-to-phase RMS voltage of 400 V, and furthermore, a peak voltage of 565 V. The GS66508T GaN HEMT manufactured by GaN Systems was chosen, with a voltage rating of 650 V and a current rating of 30 A. Even though the voltage rating of the chosen GaN HEMTs is 650 V, the recommended operation voltage is 400 V (GaN Systems, 2018b). Therefore, the inverter topology has to be multilevel or have a series connection of switches to avoid excess voltage stress. With the high switching speed of the GaN HEMTs, timing of the switching of the series-connected transistors could prove problematic. Therefore, only multilevel inverter topologies were considered.

A review of multilevel converters has been provided in (Franquelo et al., 2008). Neutral-point-clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) converters are the most common multilevel topologies, illustrated in Figure 3.1.

CHB converters require multiple isolated DC sources, and are therefore ruled out. For NPC topologies, the DC link capacitor voltage balance is essential. With unbalanced capacitors, the neutral point shifts and causes undesirable distortion in the output voltage waveform. However, this drawback can be solved with an appropriate modulation method, or a DC link control scheme. One variant of the NPC topology is the active neutral-point-clamped (ANPC) topology, in which the clamping diodes are replaced with

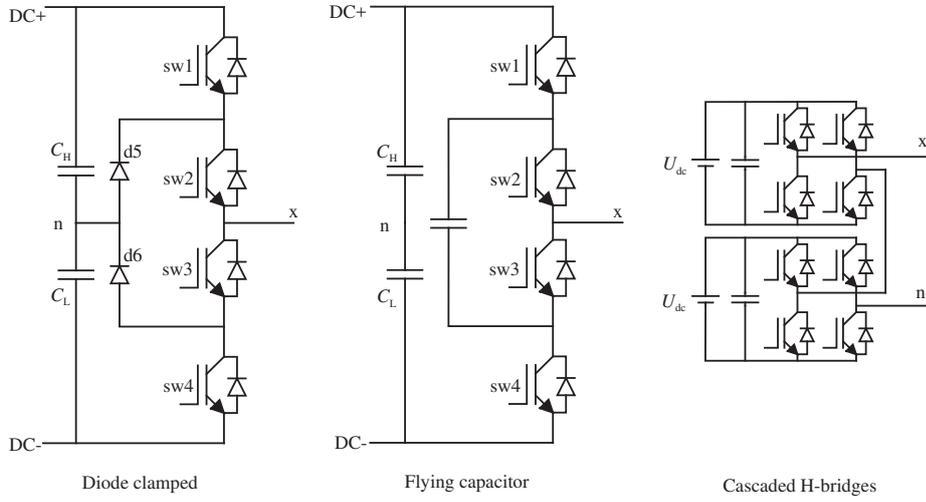


Figure 3.1: Common multilevel converter topologies (Franquelo et al., 2008).

switches, as shown in Figure 3.2.

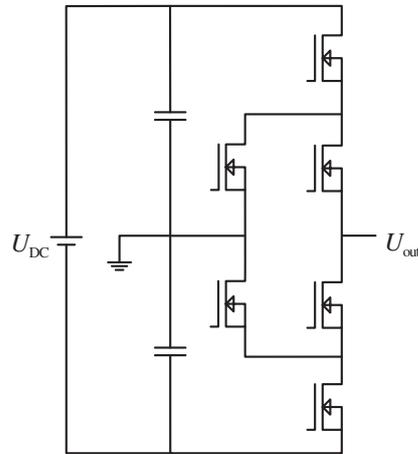


Figure 3.2: One phase of the ANPC topology.

The ANPC topology requires more switches than the traditional NPC, thus producing more switching losses. However, with the low switching energies of GaN HEMTs, the losses are smaller when compared with similarly rated Si devices. Furthermore, proper modulation ensures that the losses can be distributed more evenly over the fundamental cycle.

FC topologies do not have the neutral point capacitor voltage unbalance problem. However, without proper modulation, the flying capacitor voltage can drift. In addition, the

flying capacitors have to be charged near their nominal operating voltage before starting up the converter. The flying capacitor has to provide the full phase current, which requires a bulky component at lower switching frequencies. However, with switching frequencies allowed by GaN HEMTs, FC topologies could be made very compact.

Although the flying capacitor topologies have fewer active components than the neutral-point-clamped topologies and would be very suitable for high switching frequency operation, a neutral-point-clamped topology is chosen to be studied in this dissertation. When using GaN devices, ANPC is the obvious choice over NPC, because power GaN diodes are not commercially available. Therefore, a three-level ANPC inverter topology is chosen.

A traditional ANPC modulation scheme, without a thermal model or feedback, was used. The switching states of the chosen modulation strategy are given in Table 3.2.

Table 3.2: Three-level ANPC switch states (Bruckner et al., 2005).

	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆
State "+"	1	1	0	0	0	1
State "0U2"	0	1	0	0	1	0
State "0U1"	0	1	0	1	1	0
State "0L1"	1	0	1	0	0	1
State "0L2"	0	0	1	0	0	1
State "-"	0	0	1	1	1	0

The switching losses can be distributed evenly among switches 1 to 4 if they are cycled correctly. The switching state sequences are presented in Figure 3.3.

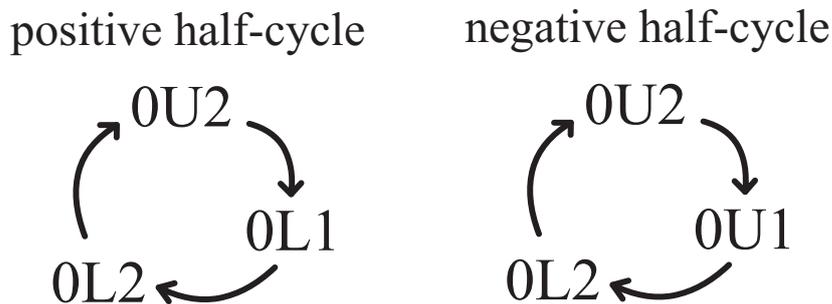


Figure 3.3: ANPC modulation state sequences.

A high switching frequency decreases the distortion of the inverter output voltage, but on the other hand, increases the switching losses because of the increased number of switch-

ing operations. However, with low switching energies of the GS66508T, $E_{\text{on}} = 47.5 \mu\text{J}$ and $E_{\text{off}} = 7.5 \mu\text{J}$ at 400 V / 15 A (GaN Systems, 2018b), the increase in switching losses is not a problem. Hence, to investigate the applicability of GaN HEMTs in high switching frequency inverter operation, a switching frequency of 1 MHz was chosen.

3.2 Implementation of the ANPC prototype

The chosen GaN HEMTs are capable of switching speeds of over 100 V/ns (GaN Systems, 2018a). With high du/dt switching edges, voltage overshoots and oscillations caused by parasitic inductances become increasingly problematic, causing incidents in the inverter such as false turn-on of the switch, possibly leading to a phase leg short-circuit. In addition, unwanted oscillations degrade the converter efficiency. Therefore, minimization of the stray inductances is essential to ensure proper converter operation and a high efficiency. Low-inductance PCB designs have been presented in (Reusch and Strydom, 2014) and (Gurpinar et al., 2016b), which further highlight the effect of stray inductances on the converter efficiency and switch voltage overshoot.

High du/dt switching edges can also have undesirable effects on the whole drive system, such as damage to the motor insulations as a result of overvoltages induced by cable reflection (Persson, 1992). Nevertheless, this issue can be mitigated by suitable inverter output filtering and short motor cables. On the other hand, the amount of electromagnetic interference (EMI) also increases with higher du/dt values, as shown in (Oswald et al., 2014). Conducted EMI emissions and their mitigation in a drive system have been studied in (Akagi and Shimizu, 2008). Even though the EMI issues are important, they are not the focus of this doctoral dissertation, but rather, of future work.

As the inverter topology and the switch components had been chosen, the next step in the prototype design was the selection of the gate drivers and their powers. The GaN Systems application note (GaN Systems, 2018a) was used as a guideline.

The optimal on-state gate voltage for GS66508T HEMTs is 6 V (GaN Systems, 2018b). However, the absolute maximum gate voltage is 7 V, which means that the gate voltages have to be properly regulated and overshoots have to be kept to a minimum, further highlighting the importance of the gate driver design. The GS66508T does not require a negative gate voltage to turn off; however, a negative gate bias mitigates the possibility of false turn-ons induced by gate voltage spikes. Even though reverse conduction losses are increased with a negative off-state gate voltage, -3 V was chosen as the negative gate drive voltage to minimize the possibility of false turn-ons. Because of the ANPC inverter topology, five of the six switches require floating gate drivers, and thereby, floating gate supply voltages. This was accomplished with isolated DC/DC converter chips for each switch, and PES1-S5-S9-M 5 V-to-9 V converters are chosen. The implementation of the +6 V / -3 V gate voltages fed to the gate driver is shown in Figure 3.4.

The PES1 converters are fed by a common +5 V supply voltage, and a voltage divider

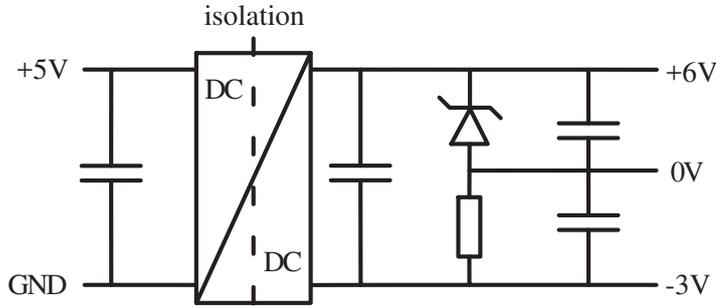


Figure 3.4: Implementation of the isolated +6 V / -3 V gate voltage.

consisting of a 6 V zener diode and a 1 k Ω resistor is connected to the 9 V output, which produces the +6 V / -3 V gate voltages and virtual ground potentials for the respective switches. Both the input and output of the PES1 converters are regulated with 4.7 μ F capacitors.

Owing to the 1 MHz switching frequency, an isolated gate driver with high common-mode transient immunity (CMTI), a low input-output capacitance, a low propagation delay, and low rise and fall times, was required. The SI8271GB-IS manufactured by Silicon Labs has a nominal CMTI of 350 kV/ μ s, 0.5 pF input-output capacitance, a maximum propagation delay of 60 ns, and maximum rise and fall times of 16 ns and 18 ns. Therefore, the SI8271GB-IS was chosen as the gate driver component in the study. There are separate outputs for pull-up and pull-down operation, which allows different slew rates for rising and falling edges by gate resistor dimensioning. A 10 Ω resistor was chosen for the positive output, and correspondingly, a 2 Ω resistor for the negative output. A ferrite bead was added to the immediate proximity of the GaN HEMTs gate to mitigate gate oscillations during switching events. The impedance of the bead should be 10–20 Ω at 100 MHz (GaN Systems, 2018a). Further, a 3.3 k Ω pulldown resistor is used.

In the PCB design, the gate drivers and their power supplies take a considerable proportion of the overall area, as the area taken by a single GaN HEMTs gate circuitry is approximately 22 x 24 mm², as opposed to the area occupied by the six switches of a phase leg, 19 x 27 mm². However, the GaN HEMTs are located on the bottom side of the board, and the gate driver circuitry is on the top layer, and therefore, the gate loop can be located as close as possible to its respective GaN HEMT. In this way, the actual gate loop, and thereby the stray inductance, is minimal, despite the proportionally large size of the gate driver circuitry. Moreover, multiple vias are used to attain a lower gate loop inductance, as demonstrated in Figure 3.5.

The layer structure of the designed PCB is depicted in Table 3.3. The top side of the PCB is occupied by the gate drivers and their respective power supplies. In addition, the control card connectors, bypass capacitors, and output filter capacitors are on the top side. The

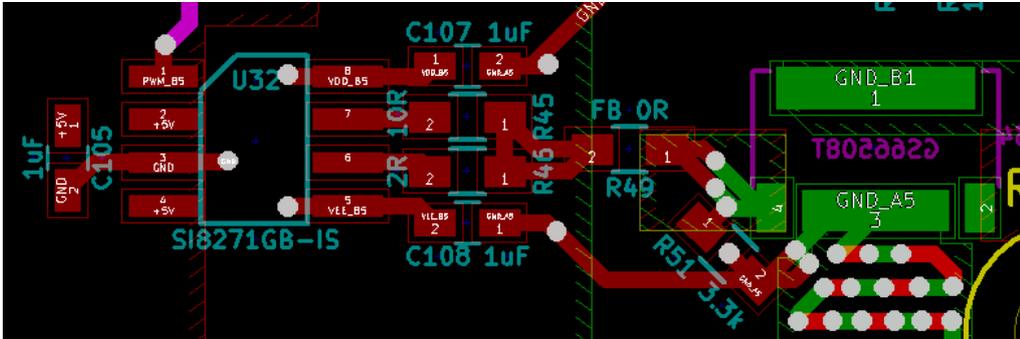


Figure 3.5: PCB design of the gate loop.

Table 3.3: Layer structure of the implemented six-layer PCB.

top	supply voltage, gate driver auxiliary power, control card
layer 1	GND
layer 2	measurement and gate signals
layer 3	neutral point
layer 4	DC- plane, filter common point
bot	DC+ plane, GaN HEMTs

top copper layer consists of the 5 V voltage plane and the floating gate voltages for each GaN HEMT. Layer 1 is dedicated to the ground plane, and layer 3 to the neutral point. The logic-level signals, such as measurements and gate signals, are routed between the two ground planes in layer 2 to shield them from EMI. The DC link negative rail, together with the output filter common point, are located in layer 4. Correspondingly, the positive DC link rail is on the bottom layer, ensuring minimal commutation loops. Finally, the GaN HEMTs are located on the bottom layer.

Because of the high du/dt switching edges of the GaN HEMTs, the output voltage of the ANPC inverter has to be filtered to mitigate the high frequency harmonic content possibly harmful to the motor. To provide the motor with a sinusoidal voltage, a sine wave filter, illustrated in Figure 3.6, was chosen as the output filter.

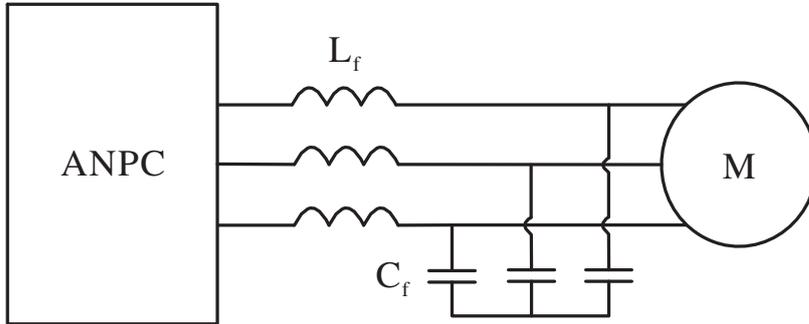


Figure 3.6: ANPC and its sine wave output filter paired with a motor.

A rule of thumb for output filter dimensioning is that the filter cut-off frequency should be one-tenth or less of the switching frequency, and at least ten times as high as the fundamental frequency (Skibinski, 2002). With a 1 MHz switching frequency and a fundamental frequency of 750 Hz, the filter cut-off frequency was set at 75 kHz. The cut-off frequency of a sine wave filter can be calculated by

$$f_c = \frac{1}{2\pi\sqrt{L_f C_f}}, \quad (3.1)$$

where L_f is the filter inductance, and C_f is the filter capacitance. The quality factor of the filter can be solved by

$$Q = \sqrt{\frac{C_f}{L_f}}. \quad (3.2)$$

A low quality factor essentially means a low circulating current in the filter. This is desirable, and therefore, the inductance of the filter should be higher than the capacitance. The inductance was chosen to be $L_f = 20 \mu\text{H}$, and the capacitance was derived from (3.1) to be $C_f = 0.22 \mu\text{F}$.

A helically wound ferrite core inductor and a polypropylene film capacitor were chosen for the implementation. The dimensions of a single inductor are 25.3 x 23.5 x 13 mm, and for a capacitor 41 x 13 x 24 mm, which combined make the total output filter volume of approximately 127 cm³ and a weight of 140 g. For reference, a sine wave output filter paired with a similarly rated commercial inverter has a volume of 2976 cm³ and a weight of 5.5 kg (ABB, 2008).

The implementation of the ANPC inverter prototype is shown in Figure 3.7. On the left there are the output connectors and the sine wave filter, whose capacitors are visible on the top side of the PCB. In the middle of the top side of the blue PCB are the gate driver circuits along with their respective power supplies, while the GaN HEMTs are on the bottom side. The red PCB in the middle is the control card. On the right there are the DC link capacitors (bottom side) and the input connectors.

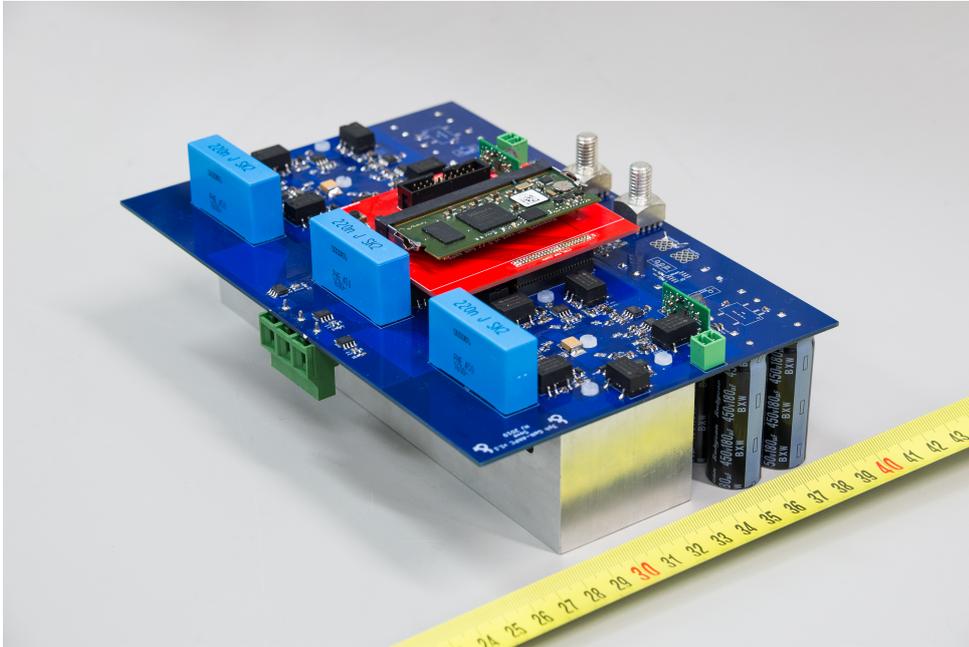


Figure 3.7: Prototype of the ANPC inverter.

The implemented ANPC inverter is a prototype whose focus is on testing the high switching frequency operation and applicability of GaN HEMTs in a three-phase system, whereas the optimization of power density is left for future studies. The DC link capacitors and gate driver circuits consume most of the PCB area, and the heat sink is dimensioned to both provide cooling and act as a support for the rest of the prototype.

3.3 Control system for the high-speed drive

In this section, the design and implementation of the high-speed drive system control is addressed. Because of the active magnetic bearings and the high rotational speed of the motor (45 krpm), a position sensor could prove problematic. Therefore, sensorless field-oriented control (FOC) and open-loop U/f control were viable alternatives. To achieve better performance in dynamic situations, the sensorless FOC was chosen.

The control design was based on the non-salient ($L_d = L_q$) PMSM mathematical model in the dq coordinate system

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} R + pL_d & -\omega_r L_q \\ \omega_r L_d & R + pL_q \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_r K_E \end{bmatrix}, \quad (3.3)$$

where u_d and u_q are the dq axis voltages, R the stator phase resistance, i_d and i_q the dq axis currents, L_d and L_q the dq-axis inductances, p the differential operator, ω_r the rotor angular speed, and K_E the back-EMF constant (Ichikawa et al., 2006). On the other hand, the back-EMF constant can be interpreted as the flux linkage generated by the permanent magnets, ψ_{PM} .

For a field-oriented control, the knowledge of the rotor angle and speed is essential, which has to be estimated in a sensorless application. By transforming (3.3) into the $\alpha\beta$ coordinate system (Chen et al., 2003)

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \begin{bmatrix} R + pL & 0 \\ 0 & R + pL \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \omega_r K_E \begin{bmatrix} -\sin\theta_r \\ \cos\theta_r \end{bmatrix}, \quad (3.4)$$

where the second term is the back-EMF, it can be seen that the second term contains the rotational speed and angle information. The back-EMF can be further rewritten as

$$\begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} = \omega_r K_E \begin{bmatrix} -\sin\theta_r \\ \cos\theta_r \end{bmatrix}. \quad (3.5)$$

Derived from (3.4) and (3.5), the back-EMF can be estimated in steady-state operation with

$$\begin{bmatrix} e_{\alpha,est} \\ e_{\beta,est} \end{bmatrix} = \begin{bmatrix} u_{\alpha,ref} \\ u_{\beta,ref} \end{bmatrix} - \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}. \quad (3.6)$$

Furthermore, the back-EMF estimation is based on the reference voltages generated by the control, thereby eliminating the need for phase voltage measurement. Using (3.6), the rotational speed and angle are estimated using a quadrature phase-locked loop (PLL), shown in Figure 3.8.

The PLL is essentially a PI controller, whose input signal is

$$\varepsilon = -e_{\alpha,est} \cos(\theta_{est}) + e_{\beta,est} \sin(\theta_{est}). \quad (3.7)$$

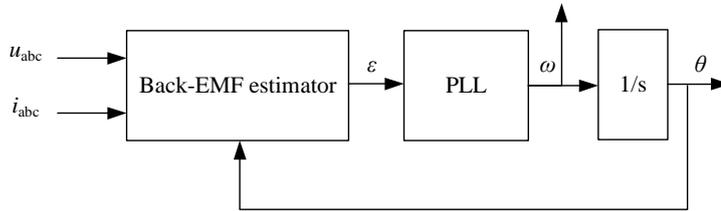


Figure 3.8: Structure of the speed and position estimator.

The PLL output is the estimated angular speed ω_{est} , which is then integrated to provide the angle information θ_{est} . The bandwidth of the PLL should be kept low to ensure the stability of the control system. The block diagram of the sensorless motor control is presented in Figure 3.9.

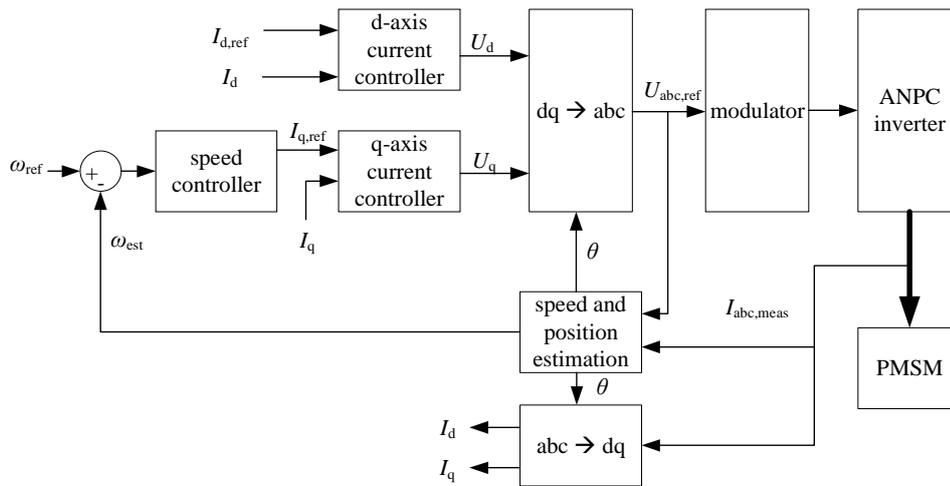


Figure 3.9: Field-oriented control block diagram.

The control system is a conventional FOC, consisting of a speed PI controller and two current PI controllers with two degrees of freedom. Traditionally, the $i_d = 0$ control principle is used to achieve maximum torque per ampere. However, for this application, rotational speed was considered to be more important than torque, and therefore, the $i_d = 0$ condition was not enforced. On the contrary, the direct-axis current controller reference was optimized for rotational speed performance. By introducing a negative i_d , the motor speed can be increased with the same voltage limit, as the d-axis current weakens the permanent magnet flux. However, the d-axis current is reactive, and should thus be kept as close

to zero as possible. This essentially means that the control is permanently in the flux weakening mode. Based on the simulation results, $i_{d,\text{ref}} = -\frac{1}{2}i_{q,\text{ref}}$ was optimal for the minimum d-axis current and the maximum speed performance.

Because of the back-EMF based speed estimation, very low speeds (i.e., start-up) have to be handled with an open-loop control. The motor is accelerated using a reference speed ramp to a constant low speed, such as 2 krpm, during which the motor voltages and currents have enough amplitude and frequency for the back-EMF estimation to work properly.

Because the inverter topology used in the study is ANPC, the neutral point stability must be ensured. The neutral point voltage always fluctuates with a frequency three times the output frequency, and may further drift during transients such as motor acceleration/deceleration. Therefore, a neutral point voltage control was employed. The capacitor voltage balance can be achieved with a single PI controller, whose output is added to the reference phase voltages produced by the motor control, as shown in Figure 3.10.

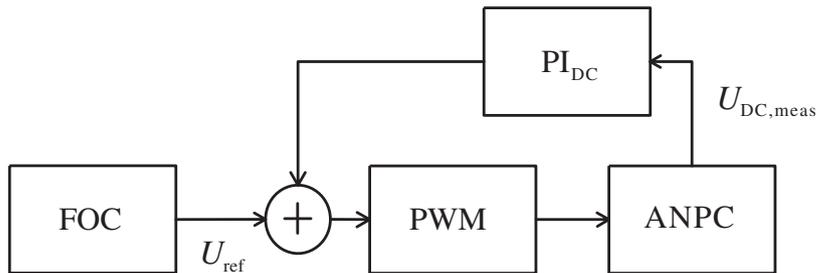


Figure 3.10: Block diagram of the DC link control.

DC link voltage measurements are required for the neutral point control. The measurements are also used in the brake resistor control, which is necessary during motor deceleration to consume the power stored in the permanent magnets of the motor.

The initial PI controller tuning for the FOC was based on the internal model control method (IMC) introduced by Harnefors and Nee (1998) for PMSM applications. After the IMC, the controller parameters were fine-tuned for the desired performance by experimental simulations. The PLL and DC link control tuning were performed completely experimentally. However, the control system stability was not mathematically studied, since it is not in the main focus of this dissertation. Rather, the control performance is demonstrated with simulation results in Chapter 4.

The control system was implemented on a XynergyXS module, featuring a STM32 Cortex-M4 microcontroller and a Spartan-6 FPGA. This combination offers the required computational performance for the high-speed drive. The microcontroller handles the sensorless

control and measurements, while the modulator is implemented on the FPGA. The structure is illustrated in Figure 3.11.

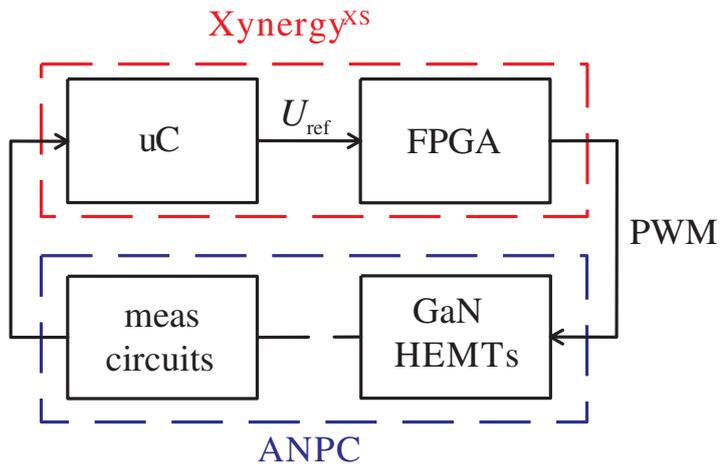


Figure 3.11: Block diagram of the control system implementation.

4 Simulation results of the sensorless motor control

The simulations were performed with MATLAB Simulink, and the model was constructed using SimPowerSystems blocks. A PMSM model was used, which was parametrized according to the existing motor values. The switch model used in the ANPC inverter was the SimPowerSystems MOSFET block. The control system and modulator were implemented in the discrete time domain. The control loop was implemented with a 100 kHz sampling frequency, and the modulator with the simulation sampling frequency. The inverter apparent switching frequency was 1 MHz.

A 20 s simulation with a 100 MHz sampling frequency was used to demonstrate the performance of the control system. The motor start-up acceleration to 2 krpm was handled by an open-loop reference, after which the sensorless control was enabled at 1.9 s. The speed reference and the motor speed response as well as the speed and angle estimation errors are presented in Figure 4.1. The voltage and current fed to one motor phase, and correspondingly, the dq axis voltages and currents are depicted in Figure 4.2. Finally, the DC link capacitor voltages are shown in Figure 4.3.

It can be seen from Figure 4.1 that the motor speed follows the reference. The acceleration/deceleration speed is defined by the current limit of the control as long as the voltage limit is not met. At 6.6 s (34.5 krpm speed), the control reaches its voltage limit, thus slowing down the acceleration as a result of the decreased current. Nevertheless, the speed reaches the reference value at 9.5 s.

During the motor start-up, the error between the actual and estimated speed oscillates, but after the sensorless control is enabled (1.9 s), the error remains under 50 rpm during the steady state, acceleration, and deceleration. However, momentary spikes are caused by the speed reference steps. The angle error is under 0.5% during steady-state operation, but during acceleration/deceleration it can be up to 25%. However, this is acceptable, as the angle and speed estimation is based on the steady-state PMSM equations.

The flux weakening operation and the angle estimation error can also be identified from Figure 4.2. Because of the negative i_d reference, the motor is in continuous flux weakening operation; however, it is easily distinguishable during the time frame of 6.6–9.5 s, when the dq axis voltage references are saturated at their limit. Additionally, the difference in actual and estimated dq axis currents highlights the angle estimation error.

It can be interpreted from Figure 4.3 that the DC link control works as intended. During motor acceleration and at a constant speed, the capacitor voltages are balanced, containing only frequency ripple typical for ANPC, whose amplitude is 200 mV. During motor deceleration, the voltages are slightly unbalanced, but kept within an appropriate level by the hysteresis control applying brake resistors.

The sine wave output filter operation was verified with steady-state simulations using

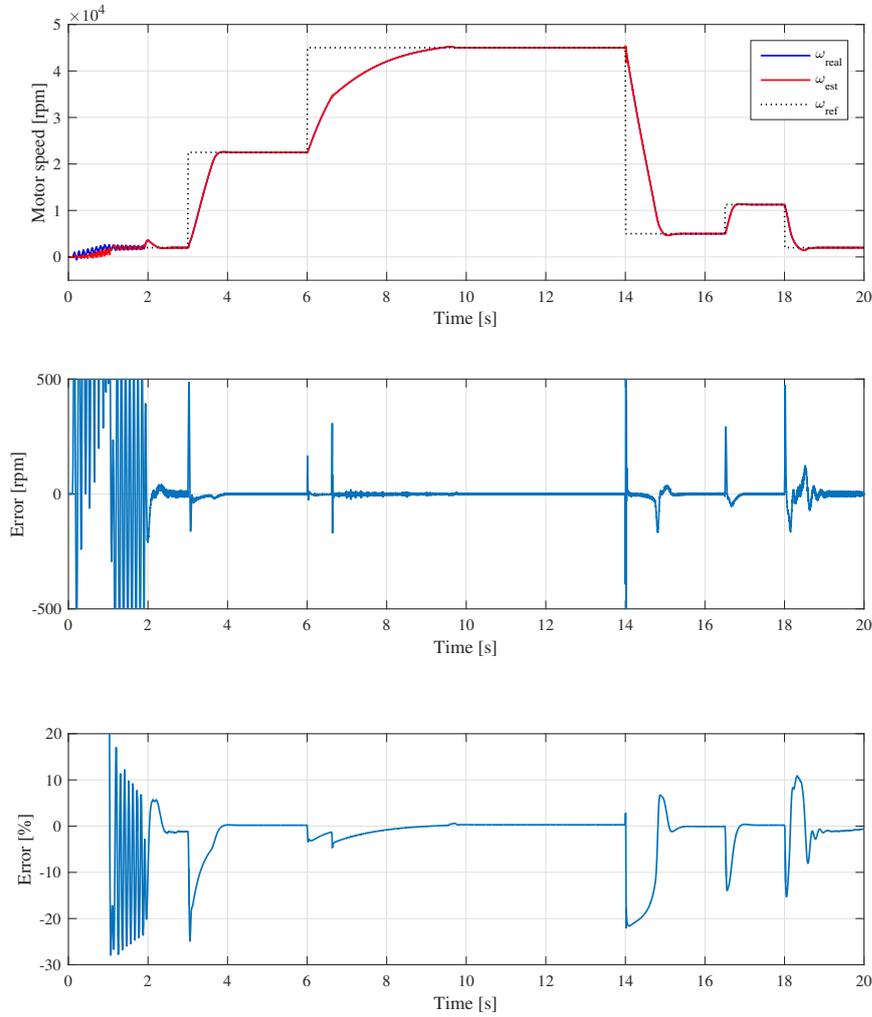


Figure 4.1: Actual, estimated, and reference motor speeds (top), the error between the actual and estimated motor speed (middle), and the error in percent between the actual and estimated angle (bottom).

a simulation sampling frequency of 1 GHz. Two different rotational speeds were used; 20 krpm and 45 krpm, which correspond to a 333 Hz and 750 Hz electrical frequency, respectively. The simulated currents of one phase of the inverter output (prefilter) and motor (postfilter) are depicted in Figure 4.4. Correspondingly, line-to-line load voltages and load currents for two motor speeds are presented in Figure 4.5.

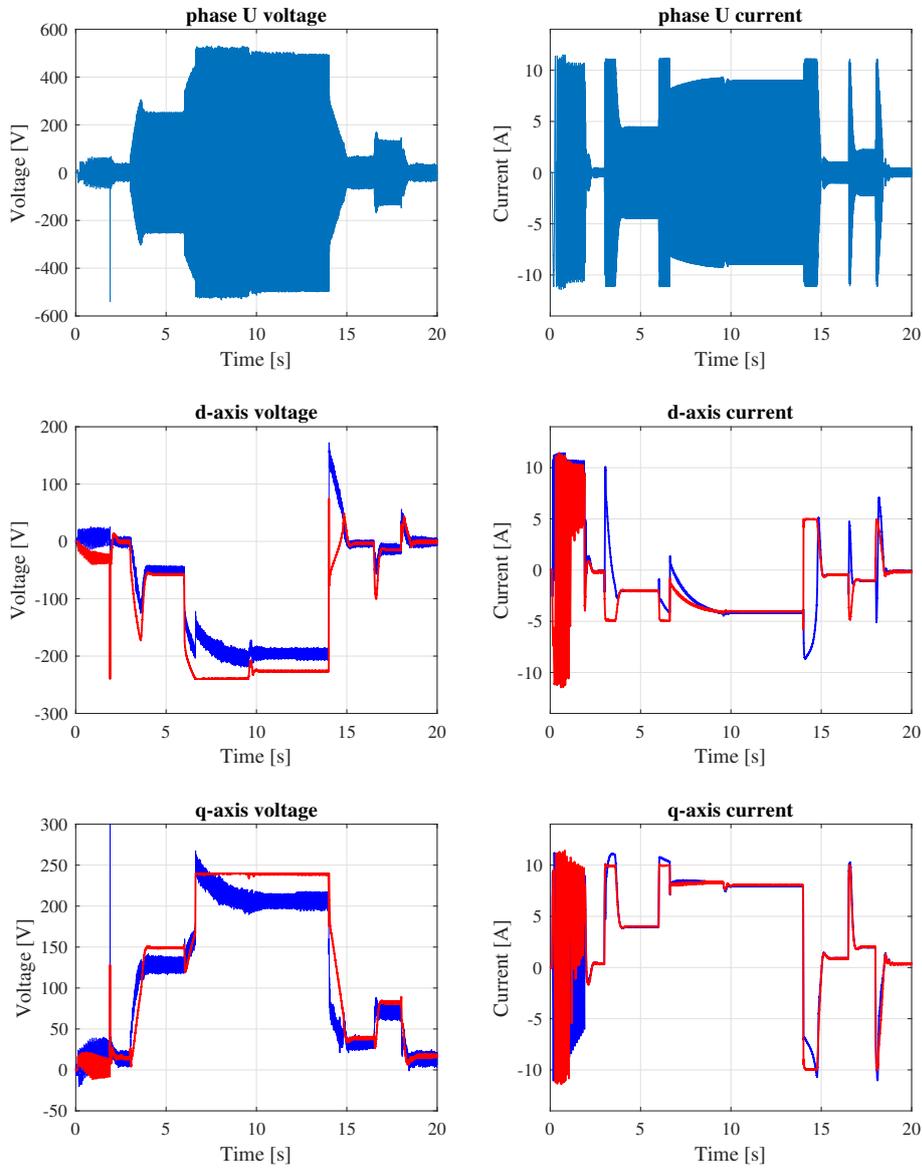


Figure 4.2: Phase U voltage and current, and the dq axis voltages and currents; the motor values are illustrated in blue, and the control voltage references and the estimated dq currents in red.

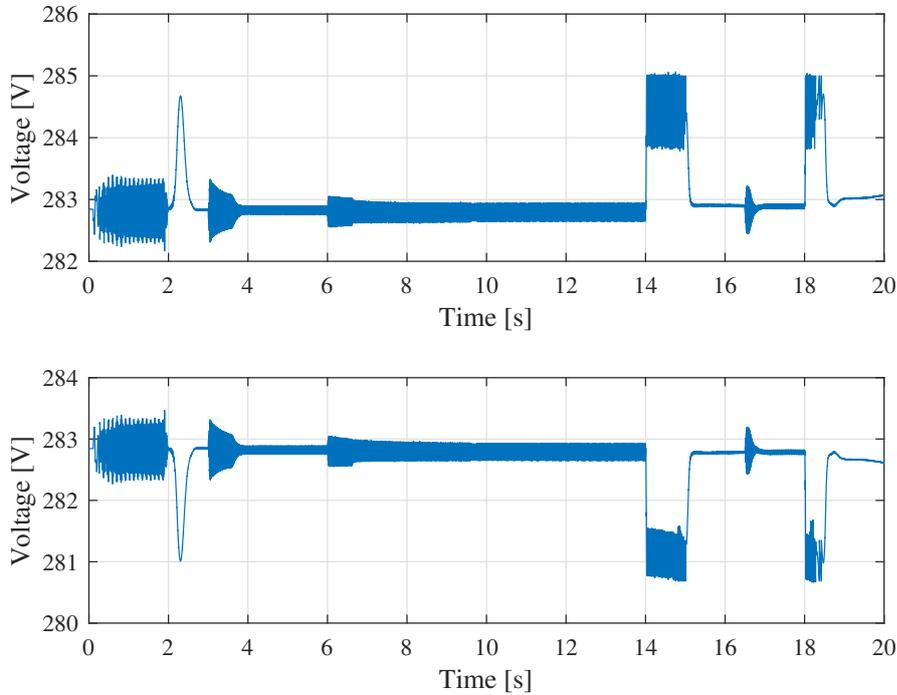


Figure 4.3: DC link voltages, DC+ to neutral point (top) and neutral point to DC- (bottom).

It is shown in Figure 4.4 that with the 20krpm motor speed, the prefilter current has a maximum current ripple of 1.3 A, and correspondingly, with the nominal motor speed of 45krpm, the maximum prefilter current ripple is 2 A. With both motor speeds, the filter circulating current is at an appropriately low level, and the postfilter current is sinusoidal.

Based on Figure 4.5, it can be stated that the sine wave filter functions as intended; the line-to-line load voltages and load currents are sinusoidal. The currents have no ripple, whereas the voltage ripple is approximately 1% of the peak value.

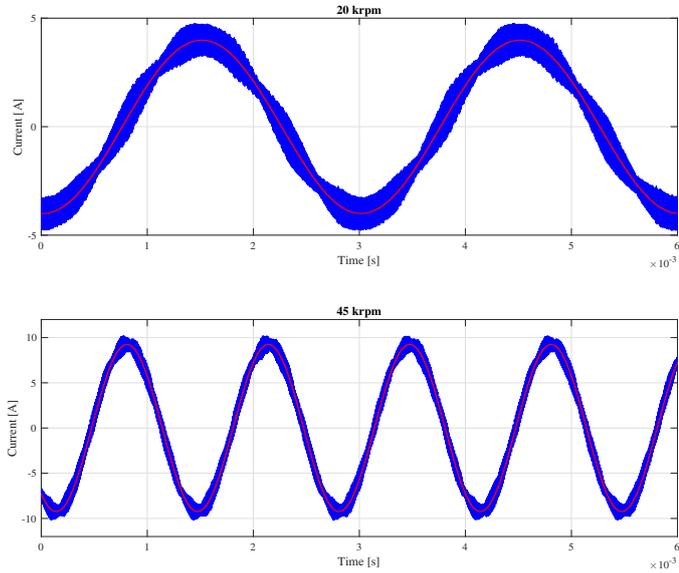


Figure 4.4: Simulated pre- (blue) and postfilter (red) currents at 20 krpm and 45 krpm motor speeds.

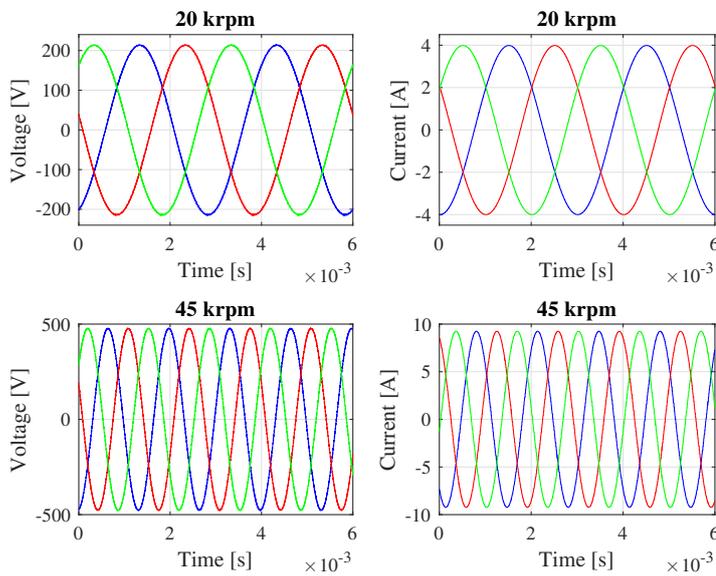


Figure 4.5: Simulated line-to-line load voltages and load currents at 20 krpm and 45 krpm motor speeds.

5 Experimental results of the ANPC inverter

At this stage of the research, the experimental results of the ANPC inverter were measured with a resistive load, instead of the PMSM. Nevertheless, the resistive load will emulate the proper operation mode of the inverter, as synchronous machines are designed to operate near the unity power factor. However, measurements performed with the PMSM were left for future work.

The measurement setup is shown in Figure 5.1. The measured variables were load line-to-line voltage, line-to-neutral voltage, and load current. The voltage measurements were performed with Tektronix P5205A differential voltage probes, which have a bandwidth of 100 MHz, whereas the current measurement was done with an Agilent N2774A 50 MHz bandwidth current probe. The oscilloscope was Keysight DSO6104A (1 GHz bandwidth).

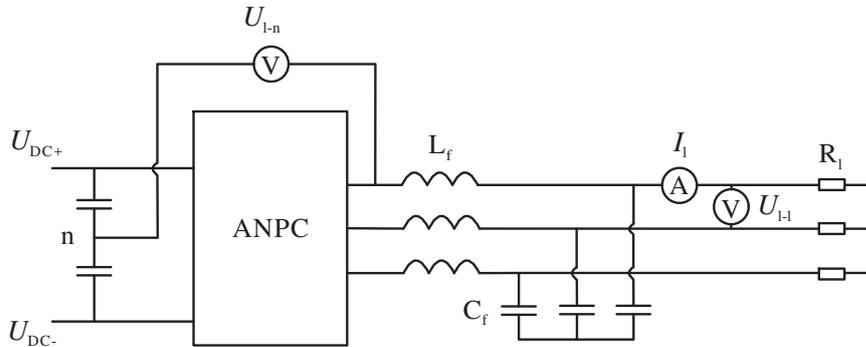


Figure 5.1: Measurement setup of the ANPC inverter with resistive load.

The ANPC inverter was operated with a 1 MHz switching frequency, a 750 Hz output frequency, a modulation index of $m = 0.9$, and a DC link voltage of 500 V. The three-phase load used in the study has a resistance of 27Ω per phase, which results in an output power of approximately 2.5 kW. The measured load line-to-line voltage, line-to-neutral voltage, and load current are presented in Figure 5.2. Additional measurement results in different operating points are presented in Appendix A.

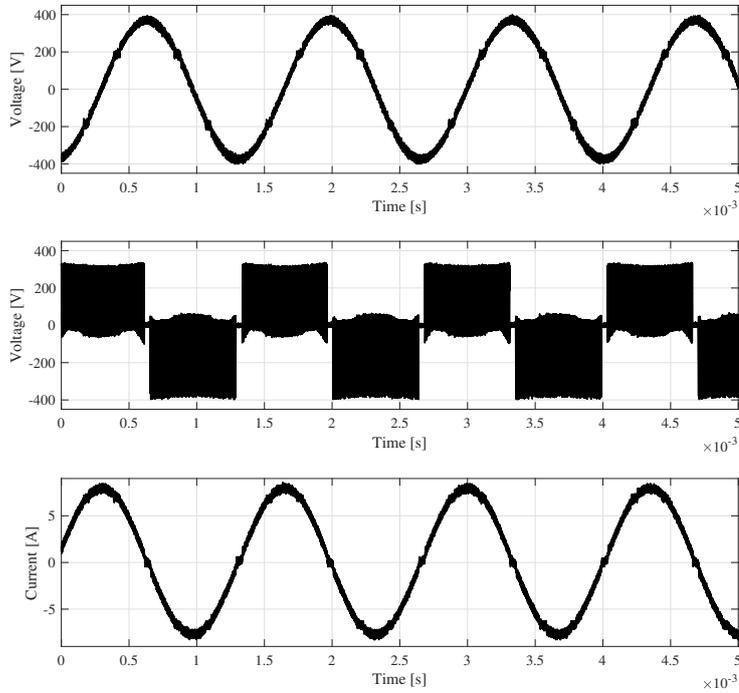


Figure 5.2: Line-to-line voltage (top), line-to-neutral voltage (middle) and load current (bottom).

Both the line-to-line voltage and the line current have sinusoidal waveforms; however, some distortions are observed during zero crossings. This is due to the 40 ns minimum pulse restriction of the modulator, which is 4 % of the switching period. The phenomenon is apparent in the line-to-neutral voltage, as there is a noticeable period of no switching events. The zero crossing distortions could be minimized with shorter minimum pulses, i.e., improved modulator design. These sinusoidal output waveforms also validate the operation of the sine wave filter. The line-to-neutral voltage, along with load current, is shown in Figure 5.3 on a microsecond timescale.

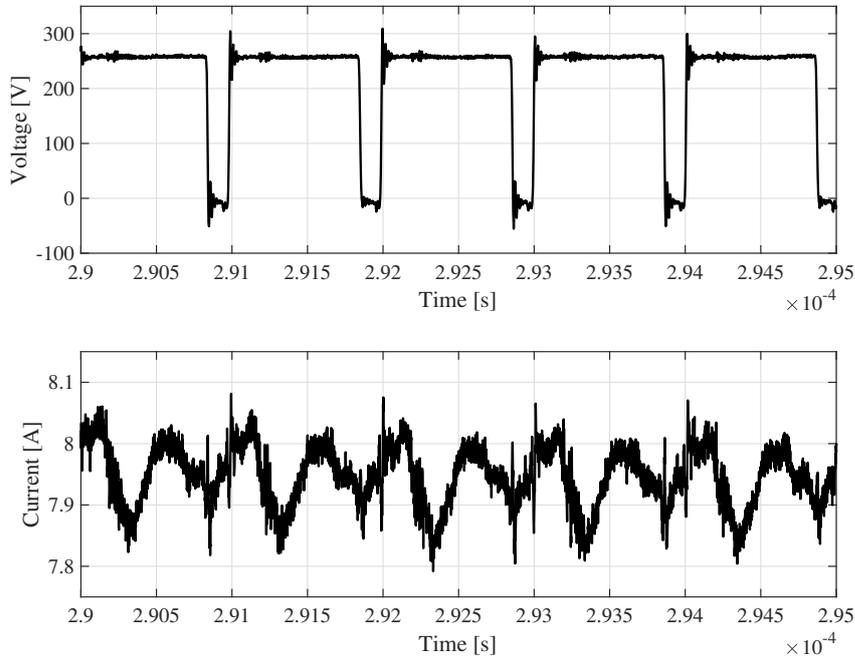


Figure 5.3: Line-to-neutral voltage (top) and load current (bottom).

The 1 MHz switching frequency is apparent in the voltage waveform; furthermore, overshoots and oscillations are observed during voltage transitions. Moreover, the oscillations caused by switching events of other phases are distinguishable from the voltage waveform. The current waveform exhibits a ripple of roughly 2%, and the 1 MHz switching frequency is also discernible. The voltage oscillations do not seem detrimental to the ANPC inverter; however, the produced EMI could prove problematic for more sensitive devices nearby. Therefore, the voltage transitions of the line-to-neutral voltage are more closely examined in Figure 5.4.

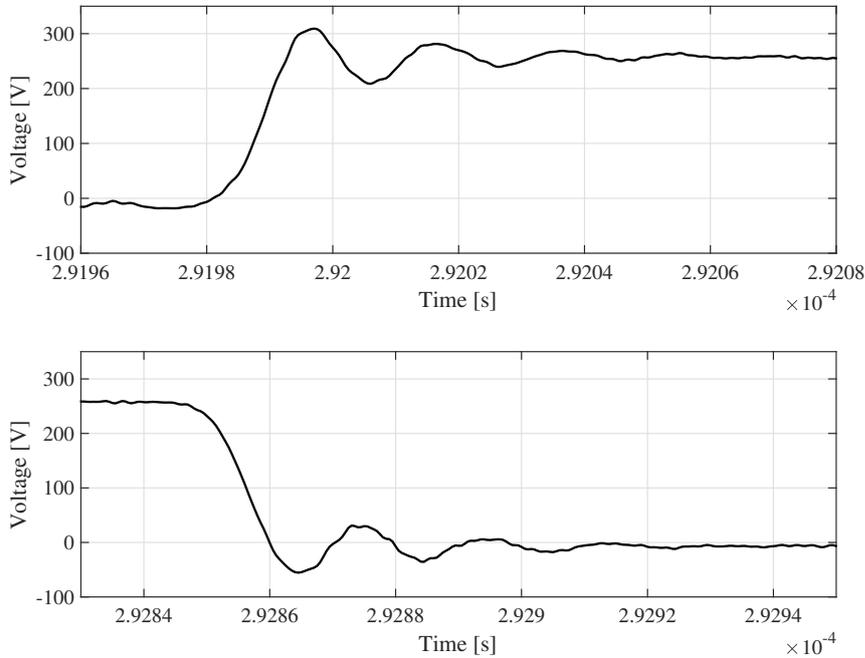


Figure 5.4: Line-to-neutral voltage rising edge (top) and falling edge (bottom).

The measured rise and fall times are 8 ns and 9 ns, whereas du/dts are 25 V/ns and 23 V/ns, respectively. The voltage transitions overshoot for 50 V and oscillate with a 50 MHz frequency. The produced EMI is thus in the very high frequency (VHF) range, 30–300 MHz, which is an unprecedented issue for a power electronics engineer. The bandwidth of the probe used in the study is 100 MHz, which means that the measurement results may have been attenuated, further meaning that the actual oscillation frequency and du/dts could be even higher than the measured values.

Lastly, thermal images of the ANPC inverter are shown in Figures 5.5 and 5.6. The images were captured with a Testo 869 infrared camera after a couple of minutes of operation. The temperatures most likely had not settled to their maximum values, which is acceptable as the objective of the thermal images was to only identify the hot spots.

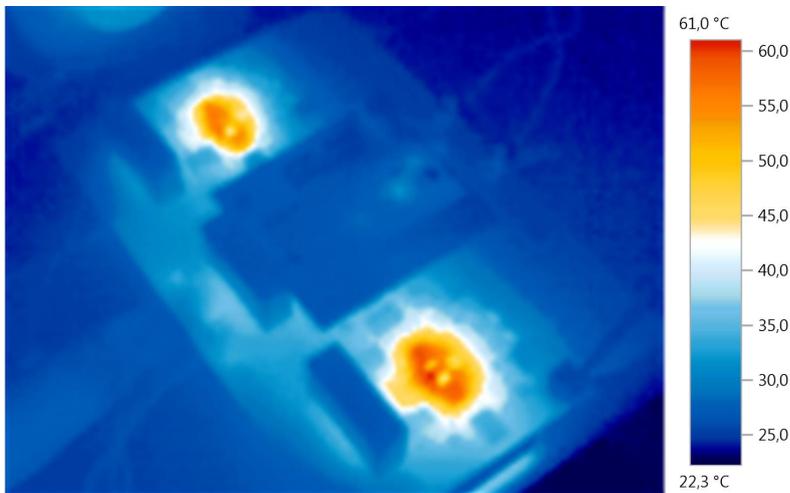


Figure 5.5: Thermal image of the ANPC inverter from above.

As can be seen in the top perspective in Figure 5.5, the hot spots, roughly 60 °C, are located around the phase legs. The GaN HEMTs located on the bottom side are likely hotter; however, it cannot be accurately assessed from the top view. The bottom view shown in Figure 5.6 displays the output filter inductors, whose temperatures are roughly 45 °C, as the hot spots. However, the thermal image is somewhat misleading, as the aluminium heat sink reflects the surrounding infrared radiation because of its low emissivity. Nevertheless, temperatures of roughly 40 °C are visible between the heat sink and the PCB (right side of the picture), where the GaN HEMTs are located.

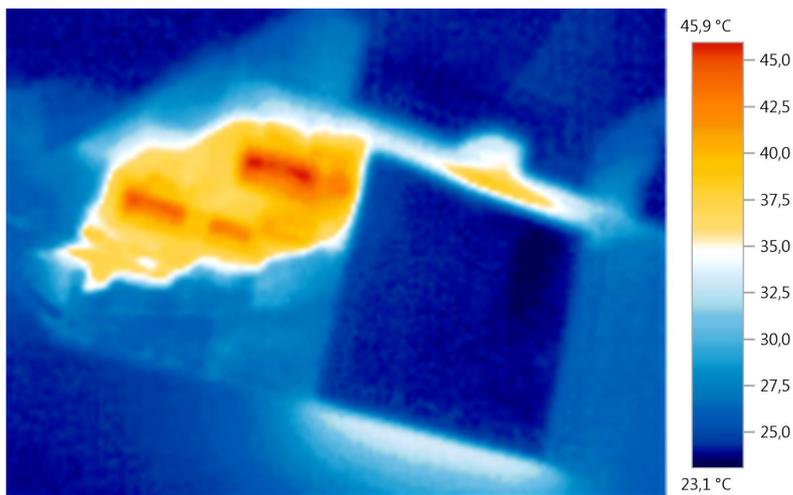


Figure 5.6: Thermal image of the ANPC inverter from below.

6 Conclusions

GaN high electron mobility transistors have excellent switching characteristics, which make them a prime contender for Si-based transistors. However, the novelty of the GaN technology in power semiconductor devices, along with the current collapse phenomenon, brings forth some uncertainties about the reliability and longevity of GaN HEMTs. These issues, together with the relatively high price and low availability of GaN HEMTs, hinder the breakthrough of GaN HEMT as the superior power semiconductor switch in low voltage inverters.

In this dissertation, the applicability of GaN HEMTs in a high-speed drive system was studied. The static channel resistance characteristics of GaN HEMTs after different switching stresses were investigated using a power device analyzer. Furthermore, a three-phase three-level ANPC inverter with a 1 MHz switching frequency was implemented to be paired up with a 45 krpm PMSM to form a high-speed electrical drive. A sensorless field-oriented control for the drive was designed and implemented. Simulations were conducted to validate the sensorless control and output filter design. Finally, the operation of the ANPC inverter was shown by experimental measurements.

6.1 Key results

The study regarding the static channel resistance behavior of GaN HEMTs indicates that after switching with no current stress, the static channel resistance R_{ON} increases as a result of the current collapse phenomenon. However, the increase is not permanent, but R_{ON} recovers to its prestress value in a rest period of minutes. The recovery characteristics are dependent on the stress time, rather than the switching frequency; longer stress times, such as 24 h, slow down the recovery rate, but switching frequencies higher than 100 kHz do not significantly increase R_{ON} . On the other hand, after a switching stress with a low switching frequency, such as 50 Hz, the increase in channel resistance is considerably higher. The measurement results after switching with current stress suggest that R_{ON} does not change, but instead, the current stress effectively mitigates the current collapse phenomenon on a macro timescale. Therefore, it is concluded that the current collapse phenomenon does not induce a lasting R_{ON} increase, as the channel resistance recovers to its initial value after a rest period of minutes. However, to be on the safe side, a R_{ON} 10% higher than nominal should be taken into account in the thermal design when using GaN HEMTs.

The implementation of the whole high-speed drive system was not achieved in this dissertation. However, the operation of the 1 MHz switching frequency ANPC inverter with a resistive load was presented. Sinusoidal output voltages and currents were observed, which suggests low motor losses and torque ripple in a drive system. Owing to the 1 MHz switching frequency of the prototype, the volume of the implemented output filter is 5% of the volume of a sine wave filter paired with a similarly rated commercial inverter, demonstrating the superior power density potential enabled by GaN HEMTs. However, an

oscillation frequency of 50 MHz was measured in line-to-neutral voltages during switching events. The resulting EMI is at radio frequencies, which presents a new kind of issue for power electronics engineers, as design principles from RF electronics have to be applied to power electronics. In addition, the minimization of PCB stray inductances has to be further emphasized. Moreover, when GaN HEMTs become more common, EMI regulations, and as a by-product, casings and their hole sizes have to be revised. All in all, GaN HEMTs enable higher switching frequencies and power densities than before, but at the same time, create new problems not present with the Si technology. Nevertheless, the results in this doctoral dissertation imply that GaN HEMTs are applicable to high-speed drive systems. As such, GaN HEMTs are likely the next breakthrough in the endless quest for higher efficiencies and power densities.

6.2 Future work

The application of GaN HEMTs in power electronics is still an emerging topic. Uncertainties such as current collapse phenomenon and its effect on reliability have not been definitively resolved yet. Although the measurement results in this doctoral dissertation indicate that GaN HEMTs are applicable to high switching frequency inverters, there is still much left to study; first and foremost, pairing up the ANPC prototype with the PMSM to form the designed high-speed drive. Moreover, the economical aspect should be assessed; even though the commercial availability of GaN HEMTs has increased, the price of GaN HEMTs still hinders their widespread adoption. In terms of initial cost and payback time, is it feasible to implement an inverter with expensive GaN HEMTs along with a small and low-cost filter, when compared with affordable Si switches accompanied by a bulky and costly filter? Additionally, does the higher efficiency provided by the GaN HEMTs outweigh the lower cost of the Si switches? From a technical perspective, EMI is an important matter because of the extremely fast switching edges of GaN HEMTs. An optimization problem in regard to maximum converter efficiency and minimum EMI should be solved. Additionally, multilevel flying capacitor converter topologies should be looked into, as the switching speeds of GaN HEMTs enable very high power densities. In addition, from a reliability standpoint, the channel resistance behavior of GaN HEMTs should be further investigated; the effect of different temperatures, current stresses, and duty cycles should be studied with larger sample sizes than the ones presented in this doctoral dissertation. Moreover, GaN HEMTs from different manufacturers should be compared.

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Appendix A Additional measurement results

More experimental results are presented in this appendix. The ANPC prototype was operated with a 1 MHz switching frequency, a DC link voltage of 500 V, and varying output frequencies and modulation indices. The resistive load used in the study has a resistance of 27Ω per phase. The measured load line-to-line voltage, line-to-neutral voltage, and load current are shown for each different operating point. Operating points with output frequency of 750 Hz are presented in Figures A.1 and A.2, with modulation indices of $m = 0.5$ and $m = 0.2$, respectively.

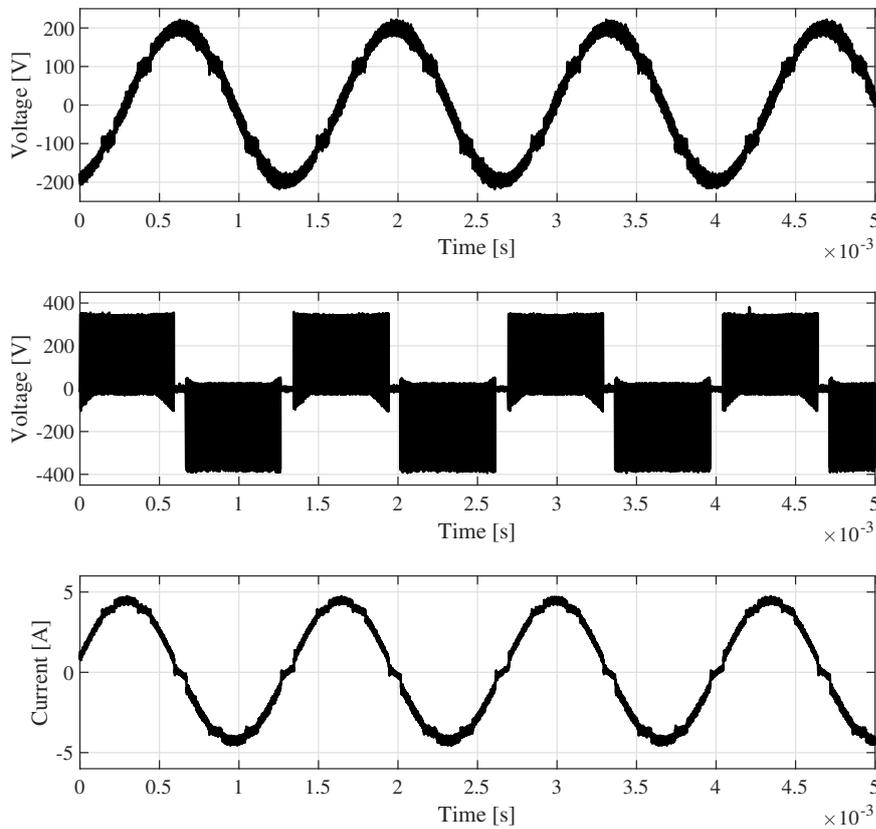


Figure A.1: Line-to-line voltage (top), line-to-neutral voltage (middle) and load current (bottom). $f_{\text{out}} = 750 \text{ Hz}$, $m = 0.5$.

Furthermore, measurement results with 300 Hz output frequency, along with modulation indices of $m = 0.9$ and $m = 0.2$ are displayed in Figures A.3 and A.4. Lastly, operating

points with an output frequency of 50 Hz, along with modulation indices of $m = 0.9$ and $m = 0.2$ are shown in Figures A.5 and A.6, respectively.

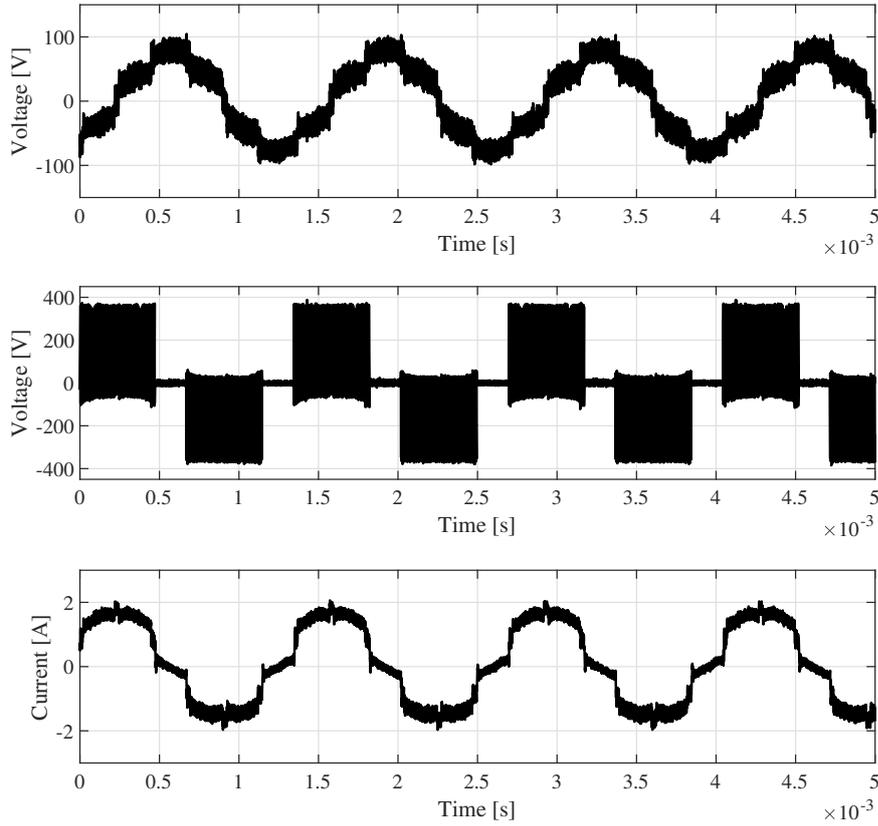


Figure A.2: Line-to-line voltage (top), line-to-neutral voltage (middle) and load current (bottom). $f_{\text{out}} = 750$ Hz, $m = 0.2$.

The distortion caused by the modulator minimum pulse width restriction is apparent on lower modulation indices. The line-to-line voltage and load current remotely resemble sinusoidal waveforms, and an extended time with no switching events is observable in the line-to-neutral voltage.

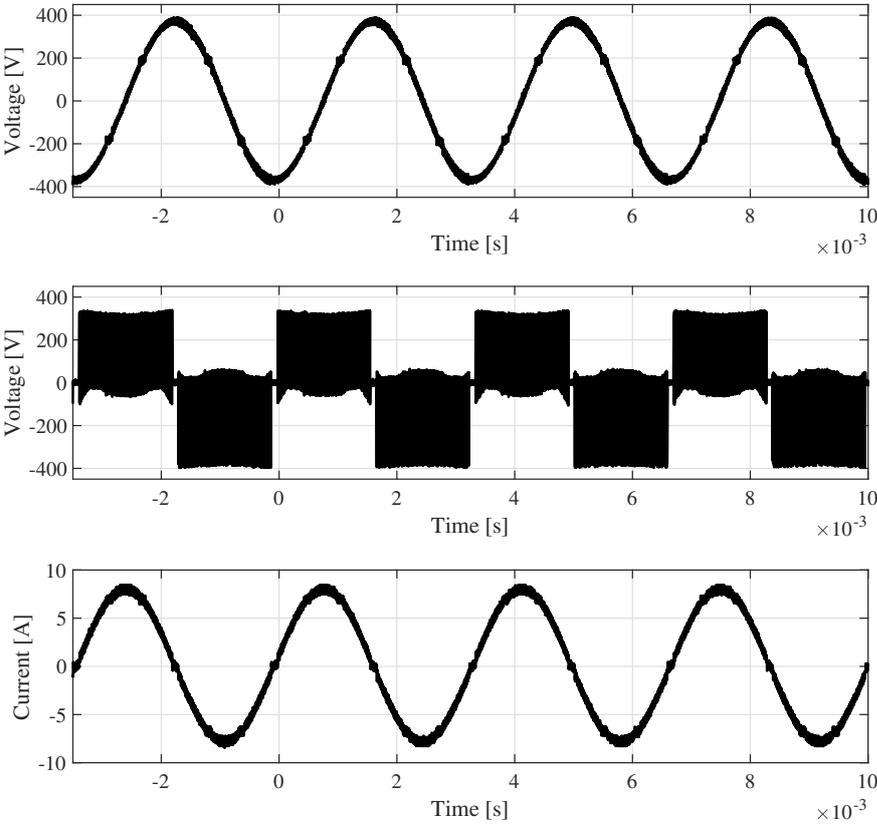


Figure A.3: Line-to-line voltage (top), line-to-neutral voltage (middle) and load current (bottom). $f_{out} = 300 \text{ Hz}$, $m = 0.9$.

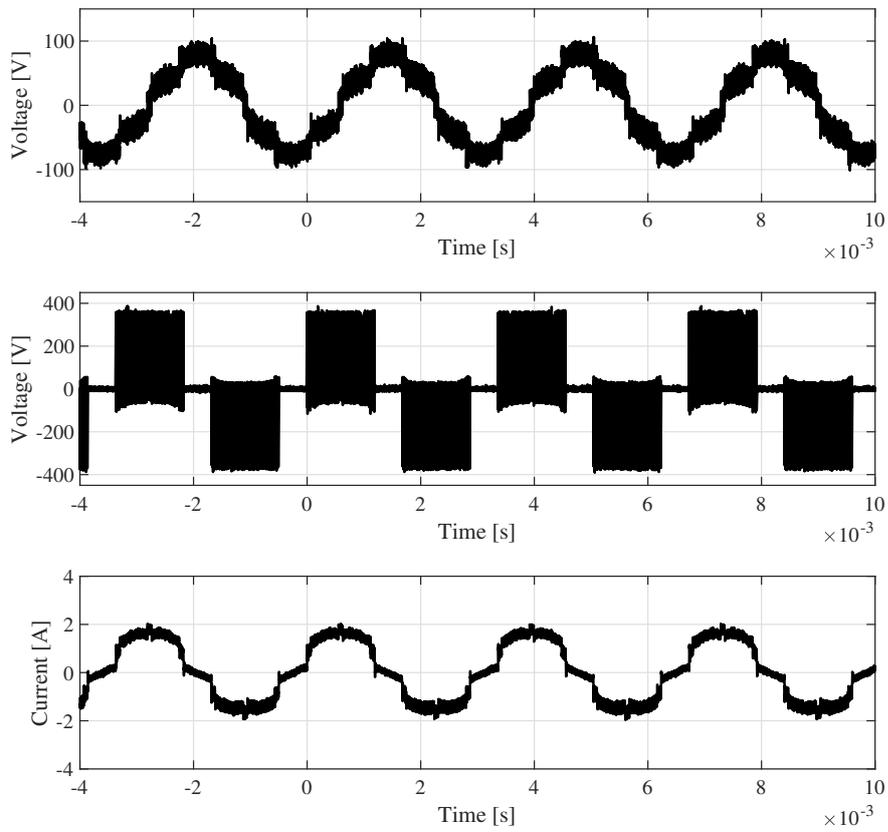


Figure A.4: Line-to-line voltage (top), line-to-neutral voltage (middle) and load current (bottom). $f_{\text{out}} = 300 \text{ Hz}$, $m = 0.2$.

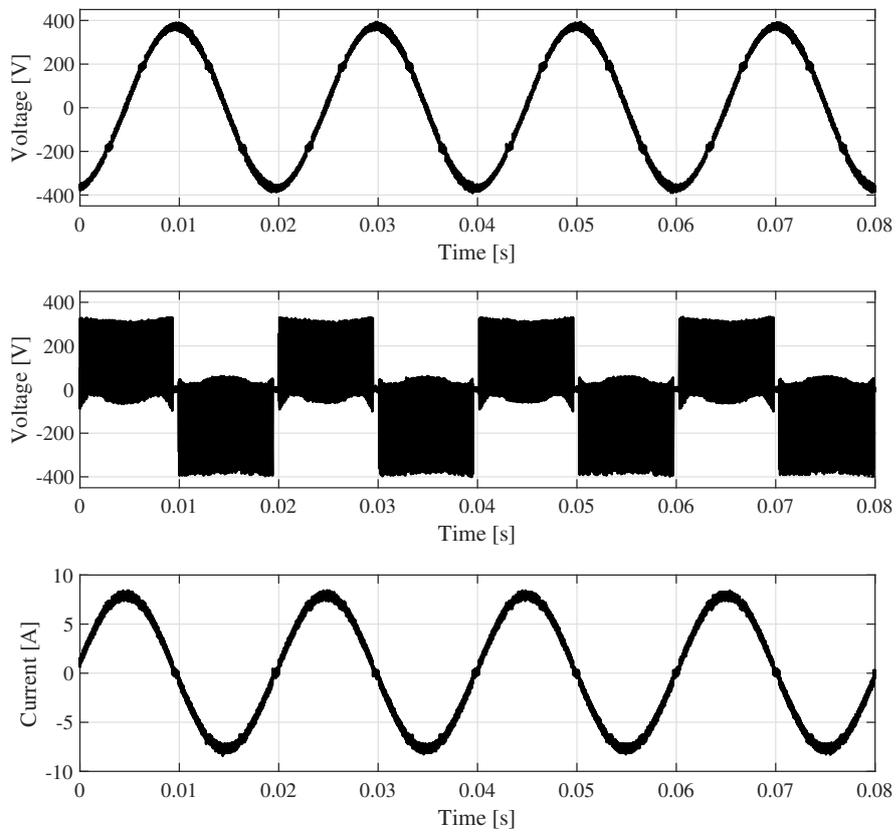


Figure A.5: Line-to-line voltage (top), line-to-neutral voltage (middle) and load current (bottom). $f_{\text{out}} = 50 \text{ Hz}$, $m = 0.9$.

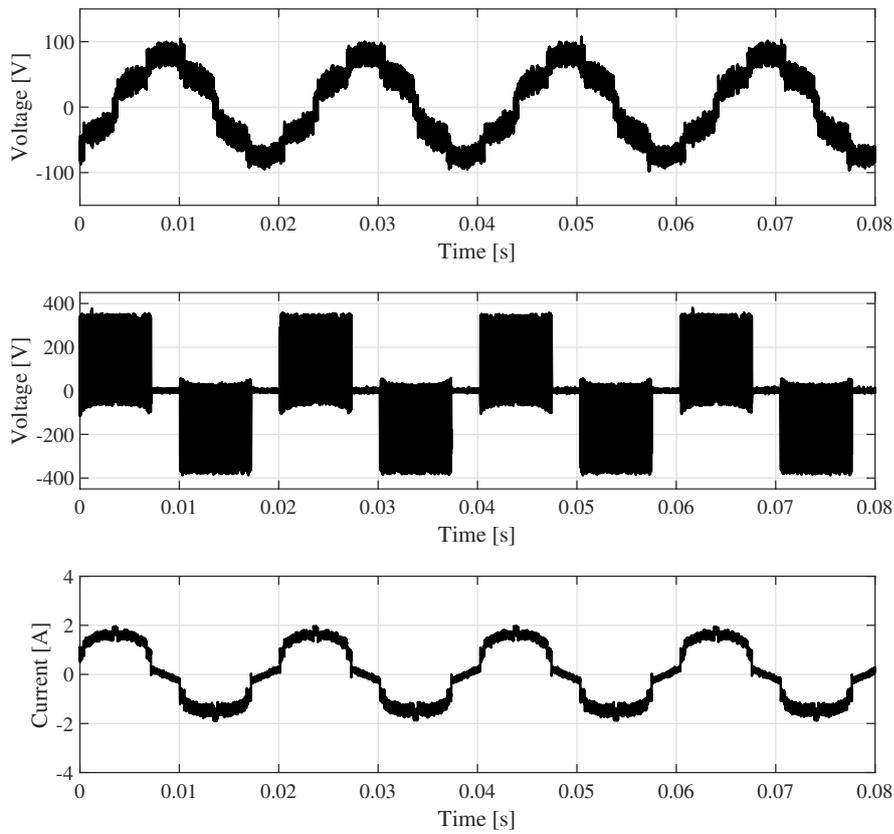


Figure A.6: Line-to-line voltage (top), line-to-neutral voltage (middle) and load current (bottom). $f_{\text{out}} = 50 \text{ Hz}$, $m = 0.2$.

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