Tatu Musikka

USABILITY AND LIMITATIONS OF BEHAVIOURAL COMPONENT MODELS IN IGBT SHORT-CIRCUIT MODELLING
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Dissertation for the degree of Doctor of Science (Technology) to be presented with due permission for public examination and criticism in the Auditorium of the Student Union House at Lappeenranta–Lahti University of Technology LUT, Lappeenranta, Finland on the 4th of September, 2020, at noon.
Abstract

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Power electronic device design and electrical system analysis can be enhanced by applying modern simulation tools, which make it possible to decrease the use of costly and time-consuming prototypes. One very critical component to be modelled is the semiconductor switch (e.g. an insulated gate bipolar transistor, IGBT) which significantly contributes to the circuit behaviour in power converter systems.

This doctoral dissertation studies behavioural IGBT circuit simulation models and their applicability to the analysis of device short-circuit operation. Commonly, short-circuit operation is modelled with complex device models, but also quite simple models can be used for this purpose. The aim of the study is to develop an IGBT model that can describe the component behaviour especially in short-circuit operation, while the characterization of the model can be performed with commercially available information. Moreover, an existing behavioural IGBT model is used as a reference model. The limitations of both the models in terms of short-circuit operation are analysed.

The IGBT short-circuit behaviour is investigated as a function of several external circuit parameters with circuit simulations, and the simulation results are compared with experimental results to validate the usability of the models and define their limitations. The busbar structure of the switching circuit is modelled with numerical methods, and the busbar model is implemented into the circuit simulator model that is used to model the rest of the switching circuit.

The simplicity of the models produces some inaccuracy in the simulation results, which can be seen particularly when the IGBT operating point deviates from the reference point. However, even with a simple model structure, the main points of an IGBT short-circuit can be described if the model characterization is carried out appropriately. According to the results of the study, the modelling accuracy of the IGBT capacitances and its thermal behaviour are the main contributors to the overall short-circuit modelling accuracy.

Taking into account the reported limitations, the models can be used for instance for short-circuit analysis of busbar structures of power converters or investigation of short-circuit protection functions in hardware-in-loop systems.

Keywords: IGBT, modelling, short-circuit, circuit simulation
Acknowledgements

The research work was carried out in two main parts. During the years from 2011 to 2016, the work was done at the School of Energy Systems of Lappeenranta University of Technology. From June 2016 onwards, the project was conducted as a part-time work or hobby as I moved to work in the industry. However, one long journey has now been completed, and it is time to head for new adventures.

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June 2020
Tampere, Finland
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Abstract

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# Nomenclature

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<th>Symbol</th>
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<tbody>
<tr>
<td>A</td>
<td>area</td>
<td>[m$^2$]</td>
</tr>
<tr>
<td>a</td>
<td>ratio</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>capacitance/thermal capacity</td>
<td>[F][J/K]</td>
</tr>
<tr>
<td>c</td>
<td>specific heat capacity</td>
<td>[J/(kgK)]</td>
</tr>
<tr>
<td>D</td>
<td>diffusivity</td>
<td>[m$^2$/s]</td>
</tr>
<tr>
<td>d</td>
<td>thickness</td>
<td>[m]</td>
</tr>
<tr>
<td>E</td>
<td>electric field strength/energy</td>
<td>[V/m][J]</td>
</tr>
<tr>
<td>g</td>
<td>transconductance</td>
<td>[A/V]</td>
</tr>
<tr>
<td>I</td>
<td>current</td>
<td>[A]</td>
</tr>
<tr>
<td>i</td>
<td>instantaneous current</td>
<td>[A]</td>
</tr>
<tr>
<td>J</td>
<td>current density</td>
<td>[A/m$^2$]</td>
</tr>
<tr>
<td>K</td>
<td>correction factor</td>
<td></td>
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<tr>
<td>L</td>
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</tr>
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<td>l</td>
<td>effective base width</td>
<td>[m]</td>
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<td>power</td>
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<td>Q</td>
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<td>elementary charge</td>
<td>[C]</td>
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<tr>
<td>r</td>
<td>radius</td>
<td>[m]</td>
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<tr>
<td>R</td>
<td>resistance/rate of change</td>
<td>[Ω]/[K/s]</td>
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<td>[s]</td>
</tr>
<tr>
<td>V</td>
<td>voltage</td>
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</tr>
<tr>
<td>v</td>
<td>velocity magnitude</td>
<td>[m/s]</td>
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<tr>
<td>W</td>
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<td>[W/s]/[m]</td>
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<tr>
<td>Z</td>
<td>impedance</td>
<td>[Ω]</td>
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## Greek alphabet

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<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Unit</th>
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<tbody>
<tr>
<td>α</td>
<td>current gain</td>
<td></td>
</tr>
<tr>
<td>γ</td>
<td>efficiency</td>
<td></td>
</tr>
<tr>
<td>Δ</td>
<td>change</td>
<td></td>
</tr>
<tr>
<td>ε</td>
<td>permittivity</td>
<td>[F/m]</td>
</tr>
<tr>
<td>μ</td>
<td>charge carrier mobility</td>
<td>[m$^2$/Vs]</td>
</tr>
<tr>
<td>ρ</td>
<td>resistivity/density</td>
<td>[Ωm]/[kg/m$^3$]</td>
</tr>
<tr>
<td>τ</td>
<td>time constant</td>
<td>[s]</td>
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## Superscripts

<table>
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<tbody>
<tr>
<td>+</td>
<td>highly doped</td>
</tr>
<tr>
<td>-</td>
<td>weakly doped</td>
</tr>
</tbody>
</table>
Subscripts

A  accumulation layer
a  ambient
BR breakthrough
C  collector
c  critical
CCG collector-gate capacitance
CE collector-emitter
CG collector-gate
CG0 initial collector-gate parameter
CH channel
CR critical
d  depletion layer/delay
DC direct current
dep depletion layer
E  emitter
eff effective
f  fall
FRM forward recovery maximum
G  gate
g  gate
GE gate-emitter
i  intrinsic
j  junction
knee knee point
L  load
max maximum
meas measured value
n  electron
off off transient
on on transient
OSC oscillation
OX oxide
p  hole
PNP pnp transistor part
r  rise
ref reference value
RR reverse recovery
sat saturated value
SC short-circuit
sim simulated value
tail IGBT tail current state value
th thermal
TH threshold
## Nomenclature

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
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<tr>
<td>VCE</td>
<td>collector-emitter voltage</td>
</tr>
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</table>

## Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
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<tbody>
<tr>
<td>ADE</td>
<td>ambipolar diffusion equations</td>
</tr>
<tr>
<td>BJT</td>
<td>bipolar junction transistor</td>
</tr>
<tr>
<td>DUT</td>
<td>device under test</td>
</tr>
<tr>
<td>EMI</td>
<td>electromagnetic interference</td>
</tr>
<tr>
<td>FS</td>
<td>field-stop</td>
</tr>
<tr>
<td>FWD</td>
<td>free-wheeling diode</td>
</tr>
<tr>
<td>GaN</td>
<td>gallium nitride</td>
</tr>
<tr>
<td>GDR</td>
<td>gate driver</td>
</tr>
<tr>
<td>GTO</td>
<td>gate turn-off</td>
</tr>
<tr>
<td>HIL</td>
<td>hardware-in-loop</td>
</tr>
<tr>
<td>HS</td>
<td>heat sink</td>
</tr>
<tr>
<td>IGBT</td>
<td>insulated gate bipolar transistor</td>
</tr>
<tr>
<td>IGCT</td>
<td>integrated gate commutated thyristor</td>
</tr>
<tr>
<td>JFET</td>
<td>junction gate field-effect transistor</td>
</tr>
<tr>
<td>MoM</td>
<td>methods of moment</td>
</tr>
<tr>
<td>MOSFET</td>
<td>metal-oxide-semiconductor field-effect transistor</td>
</tr>
<tr>
<td>NPT</td>
<td>non-punch-through</td>
</tr>
<tr>
<td>ODE</td>
<td>ordinare differential equations</td>
</tr>
<tr>
<td>PT</td>
<td>punch-through</td>
</tr>
<tr>
<td>SCSOA</td>
<td>short-circuit safe operating area</td>
</tr>
<tr>
<td>Si</td>
<td>silicon</td>
</tr>
<tr>
<td>SiC</td>
<td>silicon carbide</td>
</tr>
<tr>
<td>SOT</td>
<td>small outline</td>
</tr>
<tr>
<td>SPT</td>
<td>soft punch-through</td>
</tr>
<tr>
<td>STO</td>
<td>self turn-off</td>
</tr>
<tr>
<td>TCAD</td>
<td>technical CAD</td>
</tr>
<tr>
<td>TIGBT</td>
<td>trench gate IGBT</td>
</tr>
<tr>
<td>TO</td>
<td>transistor outline</td>
</tr>
<tr>
<td>XPT</td>
<td>extreme light punch-through</td>
</tr>
</tbody>
</table>
1 Introduction

Modelling of semiconductor switches continues to receive attention in the field of power electronics research. At present, insulated gate bipolar transistors (IGBTs) are widely used in various power electronic devices, and therefore, their modelling plays a key role in enhancing the design process of power electronic devices with virtual design tools.

Even though modelling of the IGBT has been widely studied and various IGBT switch models have been presented in the literature, there is still a need for a simple modelling method to describe the IGBT behaviour in extreme operating points, such as in a short-circuit. The main problem with the existing models is that detailed models capable of describing the IGBT behaviour in detail in a wide operating point range are very complex and difficult to characterize, whereas simple models that can be easily characterized cannot describe the IGBT behaviour in extreme operating points. To solve this problem, this study aims at finding a viable IGBT model that can be easily characterized and is fast to simulate, but can be used to describe the component behaviour also in extreme operating points.

1.1 Semiconductor switches

Currently, semiconductor switches are an essential part of many electrical devices and circuits. Even though the operation of an electrical device is affected by every component in the circuit, the semiconductor switch can be considered the heart of any power electronic system as it is responsible for the control of the current flow.

After the invention of semiconductor transistors, such as the junction-gate field-effect transistor (JFET) in 1926, the bipolar junction transistor (BJT) in 1948, and the metal-oxide-semiconductor field-effect transistor (MOSFET) in 1959, the use of power semiconductor switches has continuously expanded covering now almost all fields of electrotechnology, especially power converters. The reason for their popularity in the field of power conversion is that the semiconductor switches enable a very flexible way to control the power and current flow within or between system(s).

Depending on the voltage/current class and the switching frequency requirements, there are currently a wide variety of different switching components that apply different component technologies and semiconductor materials. In the lower voltage range, approximately when the device nominal collector-emitter voltage $V_{CE}$ is below 600 V, the MOSFET is the most common switch type because of its simple control by gate voltage, low switching losses, and high switching frequency. Its use at higher voltages is limited by the increased on-state losses generated mainly by the resistance of the wide N+ drift region of the component. However, the emerging device technologies that apply wide bandgap semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN), enable production of components with low power losses also for higher voltages. For example, according to (Millán et al., 2014), SiC MOSFETs with 1200 V and 100 A
ratings are already available in the market, and prototypes with 800 A current rating have been introduced.

Nevertheless, at present, the insulated-gate bipolar transistor (IGBT) is the most commonly used switch component in applications where $V_{CE}$ from 600 V up to 3.3 kV is required. As shown in Figure 1-1, MOSFETs dominate below 600 V and IGBTs above that. At the moment, GaN components are penetrating into low-voltage semiconductor markets, and SiC components are emerging for higher voltages.

![Figure 1-1 Typical operating area of semiconductor switches presented in terms of voltage and product range of voltage rating and product range (Gueguen, 2015).](image)

An advantage of the IGBT is that it combines the benefits of the MOSFET and the BJT, thus offering fast switching with a low control power and a low on-state voltage drop. Around and above the 3.3 kV voltage class, the thyristor components, such as the integrated gate commutated thyristor (IGCT) and the gate turn-off thyristor (GTO), are contenders of the IGBT. At the moment, commercially available IGBT wire bond modules can achieve as high as 3.6 kA rated current with 1200 V nominal voltage and 3 kA with the 3.3 kV voltage rating. The highest nominal voltage of wire bond modules in the market is 6.5 kV. Today, IGBT modules with the 1.7 kV nominal collector-emitter voltage are popular in many applications, such as wind turbines and photovoltaic inverters. Modules in this voltage range are available with the maximum collector current $I_C = 3.6$ kA.

The packaging of the component has a significant influence on the component behaviour, and the packaging type significantly depends on the component power class. In general, low-power components ($I_C < 100$ A, $V_{CE} < 1400$ V for Si IGBTs) can be directly assembled onto circuit boards and packaged into Transistor Outline (TO), Small-Outline Transistor (SOT), or similar packages. For a higher power class, there are generally two possible casing solutions; a wire bond module and a press-pack module. In the wire bond module, the external connections are on the top of the module, and at the bottom there is
1.2 Short-circuit types and commutation loop

A base plate, which is also used for heat transfer. Inside the module there are one or several parallel-connected semiconductor chips, which are connected by bond wires. The structure of press-pack modules is quite simple as they do not use bond wires to connect the paralleled chips. A press-pack component can be cooled from one or two sides. The benefits and disadvantages of different module types are discussed for example in (Oh et al., 2015) and (Deng et al., 2017).

From the modelling point view, the semiconductor switch can be divided into chip modelling and module modelling, which includes the chip model and the package model. Therefore, the packaging and chip technology should be considered carefully if a detailed model is to be achieved. Nevertheless, in the not-so-complex models that describe the component at the behavioural level, the chip technology is not so significant. However, contrary to the chip technology, the packaging type may be of importance from the modelling perspective, because parasitic components, generated as a result of packaging, can have a significant influence on the device behaviour and its coupling with the rest of the commutation circuit. Moreover, packaging is important especially from the viewpoint of the short-circuit behaviour, as a major part of the circuit parasitic inductance can result from packaging parasitics.

The semiconductor chip structure may vary considerably between IGBTs with different voltage ratings. In general, the voltage across the component is supported by the N-drift region, and if the voltage rating is increased, the thickness of the drift region should be increased, or its doping has to be modified as discussed in Section 2.1. From the perspective of modelling, the chip structure should be considered if the aim is to develop or investigate physics-based models. On the other hand, most of the IGBT models developed for general purposes do not take the device physics into account in detail, and thus, these models can be used in both low- and high-voltage devices. However, if for example a low-voltage device structure is used as a base for a general-purpose model, it can be assumed that it gives inaccurate results when used to model a high-voltage device.

1.2 Short-circuit types and commutation loop

A special feature of the IGBT is that because of its current limiting nature, it can operate under short-circuit conditions for a short time without immediate destruction. The origin of the current limiting characteristics is the metal-oxide-semiconductor field-effect transistor (MOSFET) channel on the component gate side and the channel interaction with the parasitic bipolar junction transistor (BJT). The IGBT structure and its operation in different operating modes are presented in detail later in this study. Different short-circuit types in a commutation cell are discussed widely in literature. More information can be found for example in (Lutz et al., 2018) and (Basler, 2014).

A common use of the IGBT is to control a current flow into/from a load and act as a part of a commutation circuit. Depending on the circuit topology, the commutation circuit is formed on the IGBT and a diode, or on the IGBT and some other controllable switching component where the load current commutates between the components. For example, in
the frequency converter, the first option (IGBT/diode commutation) is common. Figure 1-2 presents a simplified commutation circuit, which can be used to describe most of the commutation events that are significant from the viewpoint of the IGBT short-circuit behaviour. The components T_{1,2} and D_{1,2} are semiconductor switches that take part in the commutation, GDR is an abbreviation for the gate driver, L_{\sigma} is the commutation circuit parasitic inductance, and V_{DC} is the supply voltage source.

This kind of circuit is often used to drive an inductive load, and thus, it is assumed that the direction of the load current \( I_L \) cannot change instantaneously. In normal operation, the positive load current (from the supply to load) is flowing through the conducting T_1 when the output is connected to the plus potential \( V_{DC^+} \). When the output has to be connected to the minus potential \( V_{DC^-} \), T_1 is turned off and T_2 is turned on. Because the current direction cannot change abruptly, the load current is commutated from T_1 to D_2. If the load current direction is negative (from the load to the supply), the current is flowing through D_1 when the output is connected to \( V_{DC^+} \) and through T_2 when the output is connected to \( V_{DC^-} \).

Moreover, in normal operation, the load current is determined by the load conditions, whereas in a short-circuit the short-circuit impedance \( Z_{SC} \) defines the current through the switching components. However, the IGBT limits the current that is flowing through the component according to its output characteristics, and thus, also the short-circuit current \( I_{SC} \) is limited. During a short-circuit, a large amount of power losses is generated, which heat up the IGBT. Basically, component heating and the component temperature determine the maximum permissible short-circuit duration that the component can withstand without permanent damages.

In general, there are three short-circuit types that can occur in the circuit presented in Figure 1-2. The names Type I, Type II, and Type III will be used to distinguish the types from each other. The time of the short-circuit event relative to the IGBT turn-on time and
1.2 Short-circuit types and commutation loop

the current commutation path differ between the types. In Type I, a short-circuit already exists when the IGBT is turned on; in Type II, the output is short-circuited when the IGBT is conducting, and in Type III, the short-circuit occurs when the load current is flowing through the diode.

Figure 1-3 presents simplified current and voltage waveforms for each short-circuit type. The component that is stressed by the short-circuit is $T_1$ in Figure 1-2. The presented waveforms are the collector-emitter voltage $V_{CE}$, the collector current $I_C$, and the gate-emitter voltage $V_{GE}$ of the switch $T_1$. It is pointed out that the scale of $I_C$ is not the same in Figure 1-3a and b. Commonly $I_{C,max}$ is much higher in short-circuit Type II and III than in short-circuit Type I.

As $T_1$ is in the blocking state before $t_1$ in Type I, the voltage across it is approximately the DC voltage in Figure 1-3a ($V_{CE} \approx V_{DC}$). At $t_1$, the IGBT is turned on, and because a short-circuit already exists on the load side, the collector current $I_C$ starts to rise with a high $\frac{di_C}{dt}$ after the turn-on delay time. The current slope causes a voltage drop across the parasitic inductance $L_\sigma$, which can be seen as a drop in $V_{CE}$ after $t_1$. At $t_2$, the current reaches its maximum $I_{SC,max}$, which is determined by the gate voltage $V_{GE}$ and the component transconductance $g_m$. The dependence between current, $V_{GE}$, and $g_m$ will be discussed in the following chapters, but in general, a higher $V_{GE}$ enables a higher $I_{SC,max}$. As it can be seen from Figure 1-3a, the current decreases during the short-circuit (between $t_2$ and $t_3$). This is mainly due to the heating of the device because of the large amount of generated power losses. At $t_3$, the IGBT is switched off, and the $I_C$ starts to decrease with a decrease rate determined by the component transient behaviour and the gate drive conditions. The turn-off current slope produces, again, a voltage drop across $L_\sigma$, which can be seen as an elevated $V_{CE}$ during the transient. If the short-circuit is turned off too fast with a high $\frac{di_C}{dt}$, the amplitude of the turn-off voltage spike can reach high values and destroy the device.
Compared with Type I, in the Type II short-circuit, $V_{CE}$ has a very small value before the short-circuit (Figure 1-3b). In general, this value is the component on-state voltage, which is in the range of a couple of volts. This has a significant effect on the short-circuit operation of the device. The collector and gate of the IGBT are coupled together through the component capacitance $C_{CG}$, which is also called the Miller capacitance. The current through $C_{CG}$ tends to affect the $V_{GE}$ level, which, in turn, has an effect on $I_{SC,max}$. The value of $C_{CG}$ varies as a function of $V_{CE}$, reaching higher values when $V_{CE}$ is low (Luo et al., 2016), (Tan et al., 2017). Therefore, the effect of $C_{CG}$ on $V_{GE}$ is stronger with low $V_{CE}$ voltages. At $t_1$ in Figure 1-3b, a short-circuit occurs, $I_C$ starts to increase, and consequently, the IGBT voltage starts to desaturate. Before the short-circuit, the device is in the saturation phase, and at $t_1$ it starts to move into the desaturation phase where $I_C$ is not controlled by an external load circuit any longer. In the desaturation phase, $V_{CE}$ increases steeply according to the component output characteristics. The voltage slope $dV_{CE}/dt$ has an impact on the displacement current through $C_{CG}$ (Eq. (1.1)), causing an increase in $V_{GE}$. Because $I_{SC,max}$ is partly determined by $V_{GE}$, the higher $V_{GE}$ in the short-circuit Type II produces a higher $I_{SC,max}$ than in the case of Type I.

$$i_C = C_{GE} \cdot \frac{dV_{CE}}{dt} \quad (1.1)$$

After reaching $I_{SC,max}$ at $t_2$, the collector current starts to decrease towards its steady-state value. The decrease rate $di_C/dt$ generates a voltage drop over $L_C$, which can be seen as a high voltage spike in $V_{CE}$. The phenomenon is quite similar to the short-circuit current turn-off; however, it should be pointed out that at this stage, $di_C/dt$ is not controllable by the gate driver as it is at the turn-off. At $t_3$, the collector current reaches the steady-state short-circuit current, and after this point, the situation is similar to the Type I short-circuit.

The voltage and current waveforms in the Type III short-circuit are quite similar to the ones in Type II. Type III may occur if the load side is short circuited when the diode is conducting (D1 in this specific case) and for example providing a free-wheeling path for inductive current. Often in this state, the gate signal of the IGBT T1 is on even though the current is not flowing through it. If a short-circuit takes place during the diode conduction time, the current is rapidly commutated from D1 to T1 and the IGBT is turned on in a diode-like manner. This causes a forward recovery voltage peak $V_{FRM}$ that can be observed in $V_{CE}$ in Figure 1-3b (the dashed lines of $V_{CE}$ and $I_C$ are for Type III). This voltage spike excluded, the Type III short-circuit is very similar to the Type II short-circuit. However, before D1 is cleared from its reverse recovery state, both T1 and D1 are conducting current, and it can be hard to resolve how the current is distributed between the components.

In general, the short-circuit Types II and III are harder for the IGBT than Type I because higher dynamic short-circuit currents can be achieved. Furthermore, during the short-circuit, a collector-emitter voltage spike with a high amplitude, which is not controllable by an external circuit, may occur. When considering Figure 1-3a and b, it should be noted that the scale of $I_C$ is different between the figures.
This study focuses on investigating the IGBT modelling methods when the component is operating under a short-circuit instead of studying how it is stressed in different short-circuit types. Therefore, it is adequate to examine the device behaviour only for the short-circuit Type I as it can delineate most of the relevant short-circuit features of the device. In an ideal commutation circuit, Type I cannot be used to describe the Miller capacitance variation as a function of $V_{CE}$. However, in a non-ideal circuit, the effect of the commutation inductance $L_\sigma$ causes variation into $V_{CE}$, and thus, also the Miller capacitance has an effect on the device short-circuit behaviour, even though the effect is not as strong as in the Type II or III short-circuits.

### 1.2.1 IGBT failure types in the short-circuit Type I

The main topic of this study is to investigate and model the IGBT behaviour in the short-circuit Type I, and thus, destruction modes in this short-circuit type are discussed in brief. In Figure 1-4, the voltage and current waveforms for the short-circuit Type I are divided into four sections in which the IGBT can be destroyed by different mechanisms. Destruction mechanisms are discussed in numerous publications in the literature; an overview of these mechanisms is given in (Chen et al., 2018). More information about IGBT destruction in short-circuit conditions is presented in (Kopta, 2010), (Benmansour et al., 2007), and (Otsuki et al., 2003).

An IGBT can be destroyed at the beginning of the short-circuit as a result of a latch-up of the internal parasitic thyristor. The main reason for the latch-up is a high hole current that flows through the P-well section under the emitter contact of the IGBT. This current may trigger the parasitic npn transistor and consequently, the internal thyristor, formed from the pnp and npn transistors, is latched up and the current through the IGBT cannot be controlled by the MOS channel anymore. The risk of a latch-up can be reduced by an appropriate cell geometry and by adjusting the resistance of the P-well region by changing the doping concentration. In modern IGBTs, latch-up is not a serious problem.
The second destruction mechanism may occur when the short-circuit current has reached its maximum and decreased closer to the steady-state value. This mechanism is linked to negative differential resistances and current filamentation as explained in (Chen et al., 2018) and (Lutz and Basler, 2012). This destruction mode is called self turn-off (STO), and usually, it may happen during the short-circuit Type II or the short-circuit Type I with a large parasitic inductance. A similar failure mode may also occur during a short-circuit turn-off.

An IGBT can also be destroyed at any time during a steady-state short-circuit current by a current filaments due to high electric field strength. According to (Baburske et al., 2014), the current filamentation causes destruction because of localised heating. However, if the short-circuit duration $t_{SC}$ is too long, also thermal runaway may destroy the component during short-circuit pulse.

The third destruction mechanism may take place during a short-circuit turn-off if the inductance of the commutation circuit and the decrease rate of the short-circuit current are too high. These two together can increase the collector-emitter voltage, and if it exceeds the rated $V_{CE}$ value, the component may be destroyed. The turn-off failure is investigated for example in (Li et al., 2009). By using a suitable clamping circuit, the amplitude of the collector-emitter voltage spike can be significantly reduced.

The IGBT can also be destroyed after a successful short-circuit turn-off. This is indicated by the fourth section in Figure 1-4. In this case, the root cause of destruction is thermal runaway caused by an increased leakage current and a high DC voltage across the component. During a short-circuit, a high amount of energy is generated inside the component, and in many cases, this energy cannot be conducted away from the semiconductor chip fast enough, resulting in a rapid increase in the temperature of the chip. The temperature rise can be approximated by the energy generated during the short-circuit $W_{SC}$ and the chip thermal capacitance $C_{th}$. A high chip temperature increases the component intrinsic carrier density $n_i$, which causes a high leakage current through the component. The term critical energy $E_c$ is used in the literature to describe the amount of energy that causes the component destruction after a successful turn-off. If the short-circuit energy is kept below this value, the component can survive from thousands of short-circuit events, but if it is exceeded, the component is destroyed after one (or a few) short-circuit as presented in (Lefebvre et al., 2005). The IGBT short-circuit failures are discussed in more detail in Chapter 2.

### 1.3 Modelling of the semiconductor switch

The behaviour of the semiconductor switch has a significant effect on the behaviour of the whole power electronic circuit, and if the circuit behaviour has to be modelled, considerable effort should be put on the modelling of the switch. The difficulty in the semiconductor switch modelling comes from its highly non-linear nature and the fact that the switch behaviour significantly depends on the ambient conditions and the surrounding circuit properties. Modern semiconductor switches may have a very complex internal
1.3 Modelling of the semiconductor switch

structure including several semiconductor layers and junctions between the semiconductor material and metal, for example. Therefore, detailed modelling requires knowledge of the semiconductor and material physics. On the other hand, by investigating the switch behaviour only, it is possible to build a simplified model without deeper information of the component internal structure or physical background. Between these two extremes of the modelling methods there are a wide array of methods that combine properties from both of them.

Generally, the models can be divided into three categories depending on the basic modelling principle. The most accurate models are often based on some numerical method, such as the finite element method (FEM) or the methods of moment (MoM). These methods can also be used to describe two- or three-dimensional effects of the modelled component, but in that case, the need for computation power is significantly increased. However, this is currently not such an issue as in the past. Apart from the accuracy, one benefit of the numerical methods is that the information about component internal phenomena can be extracted. The main drawback is the need for detailed data of the component parameters.

Another main category is the models that apply analytical methods to describe the component behaviour. The basic principle of these methods is to use mathematical solutions derived from semiconductor physics to model the component. As in the case of numerical methods, also these methods require knowledge of physical parameters. Analytical models may become very complex if they are used to model multi-dimensional effects of the component, and thus, their use is often limited to one- or two-dimensional modelling. Some other simplifications into the component structure may also be needed in order for the analytical solution to be feasible. Compared with numerical methods, analytical models can be faster to solve.

The most straightforward models are the behavioural models. Often, these models concentrate on device features within some limited operating point range without taking the component internal structure or physics into account. The equivalent circuit presentation or some very simple analytical description are popular modelling methods among the behavioural models. The models can be characterized with a small number of parameters, and a short simulation time is common. As a drawback, the accuracy is not as high as with numerical or analytical models, and it may be necessary to re-characterize the model for different operating points to get reasonable results.

A schematic representation of different modelling methods is presented in Figure 1-5.
In addition to the three main categories, there is also a large group containing models that apply modelling methods from several main categories. The group is called mixed models, which may additionally include numerous sub-categories such as seminumerical, semimathematical, and compact models.

Often in the mixed models, one part of the component is described by applying a method from one main model category and another component part by a method from another main model category. For example, the wide drift region of the power switch can be modelled analytically and the emitter/gate region by using numerical methods, and the methods applied are combined into one component model.

1.4 Motivation of the work

Currently, the IGBT component is used in a wide range of electrical applications covering electrical drives in industry, household appliances, and electrical power transmission, to mention but a few. In many cases, the first stage of the design and research & development work of these applications is carried out with virtual design tools, where the device is modelled for example by using circuit simulation software and multidimensional numerical methods. The IGBT component model is an essential part of the virtual design of the electrical part of the device, but because dissimilar applications and design tasks set distinct requirements for the model, it may be hard to find a suitable solution for modelling. Generally speaking, there is no universal IGBT model that is applicable to all tasks. Furthermore, as the use of IGBT components is continuously expanding, there is also an increasing demand for IGBT modelling and there are also more and more persons who need to model IGBTs, but they do not have in-depth knowledge of semiconductors.
1.4 Motivation of the work

For those persons, many behavioural component models, which can be used and characterized without detailed knowledge of semiconductor physics, have been developed.

The main motivation of this study is to investigate the usability of behavioural models, the limitations of the models, and approaches to improve the models to enhance their usability. The study is limited to the short-circuit operation because it is one of the most critical operating points for the IGBT, and because complex phenomena occur inside the component during that operation. On the other hand, it is more demanding to design a device that can handle short-circuit operation or whose operation is predictable under a short-circuit than a circuit or a device that works correctly in normal operation. Commonly, prototypes are needed to investigate the device short-circuit operation, and this can be costly and time consuming, which is not desirable if a cost-effective design process is pursued. Compared with prototyping in general, short-circuit investigation with prototypes is even more costly, because in many cases the prototype device may break down during the prototype tests.

Moreover, in the literature, the IGBT short-circuit behaviour is mainly investigated with analytical or numerical models, which both require detailed information of the semiconductor materials and the structure of the IGBT chip. In many cases, this information is not available for an engineer who has to model a power electronic circuit as a part of the design work or for an engineer who has to investigate IGBT short-circuit events with hardware-in-loop (HIL) systems. Thus, it is important that also behavioural models and their usability are investigated in detail regarding short-circuit events, as characterization of these models can be done with commercially available data. Initially, it can be assumed that the accuracy of behavioural models is not as high as that of more complex models, but in several cases, it suffices to know the limitations of the model. The motivation behind this work is that, to the author’s knowledge, no studies on behavioural IGBT models in short-circuit operation have been published so far, and the limitations of the models are not reported from the perspective of a short-circuit. Furthermore, behavioural models are not commonly developed for short-circuit modelling, one motivating factor being thus to fill this gap.

1.4.1 Virtual design

Depending on the engineering field, the term “virtual design” may have different meanings, but generally, it refers to the design and prototyping of a device or equipment in a uni- or multidisciplinary simulation environment. The common factor for all engineering fields is that by using a virtual design method, different design variants can be investigated without a need to build a separate prototype for each variant. Furthermore, some phenomena are difficult or impossible to be investigated even with prototypes, but they can be studied in a virtual design environment. One example of such a problem from the field of electrical engineering is the internal current distribution of a semiconductor component. A further benefit is that an automated design optimization procedure can be used to achieve an optimal solution. However, economy and time saving are often the
most important drivers to use virtual design. Moreover, presently, the availability of computational power enables the use of this design method for more complex systems and by a larger group of designers.

In semiconductor modelling, virtual design can be performed at several levels depending on the size of the unit to be modelled. Semiconductor chip manufacturers use virtual design to investigate how variation in semiconductor parameters or operating conditions affects the chip behaviour. In this case, for example the physical parameters of the chip, such as layer thicknesses, gate geometry, and doping profiles, can be varied to optimize the operation of the chip. The next level is to take the device packaging into account in the virtual design process. At this level, the parasitic effects arising from the package are considered, and the device behaviour can be predicted in the form in which it is delivered for example to a company that produces and designs power electronic systems. As the high-power semiconductor modules have quite large packaging, also parasitic effects increase because of the larger dimensions of the module internal busbars and the parallel connection of the semiconductor chips inside the module. If the virtual design process is extended to consider even larger units, also the external circuit that surrounds the module should be included in the process. In principle, this can be a simple commutation circuit presented in Figure 1-2, but similarly, it can be the whole main circuit of a power electronic system that includes control electronics, snubber circuits, and power supply.

The design process depends thus on the system to be designed and the required level of details. The virtual design can be extended to cover the power electronic system, the surrounding network, and the electric grid, and basically, there is no limit for the scale of the system to be designed. In summary, virtual design can save costs in the design process, and in some cases also increase safety, and it can be used both for small details and larger ensembles. In this study, the virtual design tools are used to model the IGBT module behaviour in a commutation circuit that is providing short-circuit current for an external load. The study does not include the design process itself, and thus, it is not relevant to present any optimum solution to improve the circuit behaviour. In contrast, the aim was to determine the usability of the tools that was used.

1.4.2 Reliability

From the perspective of reliability, investigation of the IGBT short-circuit is of importance as simultaneous high current and voltage may cause great damage to the device. On the one hand, the high amount of power losses and the generated heat can destroy the component at once; on the other hand, the reliability of the component is affected by mechanical stresses caused by electromagnetic forces during the short-circuit. The latter is especially true in high-power bond-wire module types, where a complex internal busbar system is applied. An example of such a module internal structure is presented in Figure 1-6. Furthermore, repetitive short-circuit pulses can reduce the IGBT voltage blocking capability as presented in (Bhojani et al., 2019).

In addition, the displacement current through the Miller capacitance can increase the gate-emitter voltage above the safety limit that the gate oxide can tolerate. Presently, in many
1.4 Motivation of the work

cases, the maximum allowed $V_{GE}$ specified by component manufacturers is $\pm 20...30$ V. Another phenomenon that may cause exceeding of the $V_{GE}$ limit is the gate-side oscillations that are caused by the capacitance/inductance resonance circuits at the gate circuit. Because many of the parameters vary for instance as a function of voltage or temperature, the oscillations can be triggered by many phenomena during the short-circuit. Nevertheless, modern gate drivers often include some safety function that limits the $V_{GE}$ within the permissible limits, and thus, excessive $V_{GE}$ values seldom cause reliability problems.

Even though $V_{GE}$ can be kept in control, the component reliability can be decreased as a result of gate oxide degradation. During a short-circuit, a high electric field across the N-drift region may accelerate the carriers that eventually penetrate into the gate oxide and affect its operation. The phenomenon in which the carriers are trapped into the oxide is called the hot carrier effect, first observations of which were presented in (Abbas and Dockerty, 1976) and (Ning, 1977). In a MOSFET structure, the hot carrier effect causes an increase in the threshold voltage $V_{TH}$ and thereby a decrease in current in the MOSFET channel. In an IGBT device, this means also a decrease in the collector current.

This effect is widely investigated in the literature; more information can be found for example in (Hu et al., 1985), (Moens et al., 2004) and (Grasser, 2015).

![Figure 1-6 Internal busbar structure of a high-power bond-wire IGBT PrimePACK module.](image)

There are also other issues caused by the short-circuit that can break the component. One of these is the $V_{CE}$ voltage spike at the short-circuit turn-off. As was discussed in Section 1.2.1, the increased voltage is produced as a result of the high $di/dt$ and parasitic inductance in the commutation circuit. If the voltage exceeds the maximum voltage rating of the component, it may go into avalanche breakdown (Chokhawala et al., 1995) and (Grbovic, 2007). In an avalanche, carriers are accelerated by a high electric field, and they can collide into semiconductor lattice atoms and then produce new charge carriers. This multiplying phenomenon may introduce an exponential current increase and destroy the
component. Nevertheless, an avalanche at the short-circuit turn-off can be avoided by proper gate drive control or by using a clamping circuit to attenuate the amplitude of the voltage spike.

The short-circuit pulse energy $E_{SC}$ (Eq. (1.2)) is crucial from the perspective of reliability because in many cases the root cause for the device failure is that excessive energy cannot be transferred from the component, and some destructive thermal breakdown mechanism occurs as a result of the increased temperature. $E_{SC}$ can be defined by integrating the short-circuit power $P_{SC}$ over the short-circuit duration $t_{SC}$

$$E_{SC} = \int p_{SC}(t) dt = \int_{0}^{t_{SC}} v_{CE}(t) i_{C}(t) dt.$$  \hspace{1cm} (1.2)

In (Lefebvre et al., 2005) and (Arab et al., 2008), the IGBT behaviour under repetitive short-circuit pulses is investigated; the studies show that exceeding the device-dependent critical energy $E_c$ causes an instant breakdown, whereas the device can tolerate even thousands of short-circuit pulses if $E_{SC}$ is below $E_c$. In the experimental part of the studies, $E_{SC}$ is varied by adjusting the DC voltage $V_{DC}$ and the short-circuit duration $t_{SC}$ in the Type I short-circuit and stressing the component with similar pulses until failure. An example of the results for a 600 V NPT IGBT is presented in Figure 1-7.

![Figure 1-7 Experimental results of the IGBT failure under repetitive short-circuit pulses (Lefebvre et al., 2005).](image)

For the given single chip IGBT component (SGW15N60), the critical energy $E_c$ in the 125 °C case temperature is 0.62 J, and at 25 °C, $E_c$ is 0.81 J. As it can be seen, $E_c$ is lower if the temperature is increased.
Even though the studies concentrate on single chip components and thus, all the conclusions are not directly applicable to module-type switch devices, a similar destruction phenomenon may occur if a single chip inside the module is considered. Furthermore, the device may fail because of different mechanisms depending on the $E_{SC}$ value proportional to $E_c$. If $E_{SC} < E_c$, the device fails as a result of ageing effects and cumulative damage, and in this case, the actual breakdown occurs during the short-circuit turn-off. If $E_{SC}$ is much higher than $E_c$, the breakdown happens during the short-circuit as a result of thermal runaway (energy-limited failure). However, if $E_{SC} > E_c$ but close to $E_c$, the component is destroyed after a time delay $t_d$ after the short-circuit turn-off. The delay depends on $E_{SC}$ as presented in Figure 1-8. In the figure, different curves describe different short-circuit durations $t_{SC}$.

![Figure 1-8 Time delays for IGBT destruction as a function of short-circuit duration (Lefebvre et al., 2005).](image)

If $E_{SC} = E_c$, the number of repetitions required for a device failure is randomly distributed, and in this specific case, it is between 1 and approx. $10^4$ (Figure 1-7). In actual experimental tests, it is difficult to stabilize the test conditions so that $E_{SC}$ would always be exactly the same. Because of this, the results in this case are random as $E_{SC}$ can be slightly above or below $E_c$ in reality. Nevertheless, $E_{SC}$ is close to $E_c$, and therefore, the destruction mechanism is delayed destruction as in Figure 1-8, and the delay time $t_{df}$ is the highest possible.

In (Baburske et al., 2018), critical energy is investigated from the perspective of current filament. It is observed that two different failure modes, energy failure and electrical failure, in other words, current filaments, occur even when the short-circuit energy is the same. The distinctive parameter between the modes is the short-circuit current.
1.5 Objective of the work

The use of power electronics in all electricity use is continuously increasing, causing a growing demand to model the power electronic circuits. The requirements relating to accuracy, speed, and complexity of the modelling method depend greatly on the modelled application and objectives of the modelling. In general, models that are fast to simulate and easy to characterize are preferred in modelling of large systems, whereas more complex models that require detailed component information for characterization can be more applicable in the modelling of smaller units.

As an individual component, the IGBT (or other solid-state semiconductor switch) causes a major part of failures in power electronic circuits. For example, in (Spinato et al., 2009), it has been reported that frequency converter failures account for 25% of the total failures in wind turbines. Moreover, according to (Choi et al., 2015), semiconductor switch and soldering failures cause 34% of the total power electronic converter faults. If the device stress in extreme operating points can be modelled and predicted already in the design stage in a virtual design environment, the costs caused by failures can be decreased.

The main objective of this work is to study behavioural IGBT models and how these models can be used to describe the device behaviour in extreme operating points such as under short-circuit conditions, where a very large current is flowing through the device. Owing to the nature of the behavioural models, all the IGBT characteristics cannot be described with a single model, but instead, the model can be constructed to incorporate features that are relevant from the model user’s perspective.

Many behavioural models give accurate results in the normal operating point, some of them also in current saturation. With high collector currents, however, there may be special features that are difficult to capture by using a simple model structure. For example, the IGBT behaviour in the short-circuit with the collector-emitter voltage much below the nominal voltage of the device can be very difficult to model without a detailed device model. One objective of the study is to detect these features and discover their origin.

Furthermore, a new behavioural IGBT model specially for short-circuit modelling is developed in this study. The starting point for the model is that the model should describe the IGBT collector-emitter voltage and collector current waveforms in the short-circuit Type I with a reasonable accuracy, and that the model should be possible to be characterized with component datasheet information. This developed model is verified by measurements and compared with the IGBT model that is included in a commercial simulation software.

The objective of the work can be summarized by three research questions:

1. What is the feasibility of the behavioural models in the IGBT short-circuit modelling?
1.6 Outline of the work

2. How can the behavioral models describe the IGBT short-circuit operation as a function of operating point parameters?

3. What are the main features that have to be included in the IGBT behavioural model so that the short-circuit modelling yields accurate results?

1.6 Outline of the work

This doctoral dissertation consists of six chapters, which are organized as follows:

Chapter 1 gives an overview of the research topic. It includes background information of semiconductor switches, the basic commutation circuit, semiconductor switch modelling, and the short-circuit behaviour of the switch. In addition, the motivation, objectives, and scientific contributions of the work are presented.

Chapter 2 discusses the IGBT component as a switch in a power electronic circuit. The physical structure of the component is presented, and its operating principles are explained in detail in an analytical manner. Furthermore, different modelling methods for the IGBT are reviewed, and the benefits and drawbacks of each method are given. A literature survey of behavioural IGBT models is provided, and the application fields of the models are discussed. Further, the theoretical background of the IGBT failures that are caused by short-circuit conditions is given, and the effect of short-circuit pulses on the lifetime of the IGBT is studied.

Chapter 3 concentrates on describing the structures and characterization of the models that are used for short-circuit modelling in this study. Specific challenges of short-circuit modelling, such as collector current saturation as a function of voltage and IGBT self-heating are analysed from the perspective of modelling. Further, issues such as modelling of the IGBT module parasitic components (inductances and capacitances) and their effect on the modelling accuracy are addressed.

Chapter 4 is dedicated to the experimental part of the study and verification of the simulation model. The IGBT test setup for the short-circuit Type I experiments and the measurement devices are introduced. Moreover, problems in performing measurements and achieving accurate results in the IGBT short-circuit tests are discussed. Along with experimental results, simulation results are presented in this chapter. The simulation results are compared with the measurements as a function of four operating point parameters; collector-emitter voltage, gate turn-off resistor, short-circuit pulse length, and ambient temperature.

Chapter 5 presents the conclusions based on the study. Furthermore, contributions of the study for the field of IGBT short-circuit modelling are discussed.

Chapter 6 discusses future work that would probably advance the research but could not be accomplished within the framework of this doctoral dissertation.
1.7 Scientific contribution

The key scientific contribution of this study is the development of a methodology and knowledge that can be used to enhance the power electronics design process particularly from the perspective of IGBT short-circuit operation. To achieve this contribution, the following steps are taken:

- Development of a circuit simulation model for a high-power IGBT module commutation circuit when the device is operating under short-circuit conditions;
- Implementation of detailed internal and external busbar structure models, which are extracted from a numerical 3D model, into the circuit simulation model;
- Analysis of the IGBT module short-circuit behaviour in different operating conditions;
- Model verification with experimental tests and analysis of error sources when comparing experimental results with simulation results;
- Analysis of the critical IGBT/commutation circuit parameters that have a major effect on the short-circuit modelling accuracy when the model is developed without detailed information of the device structure and/or physical parameters.

This doctoral dissertation contains material from the following papers.


2 IGBT short-circuit behaviour and modelling methods

This chapter gives background information about IGBT short-circuit failure modes and IGBT semiconductor physics required in analysing the applicability of IGBT behavioural models in short-circuit modelling. This information is also needed to understand the physical phenomena behind the IGBT short-circuit operation described with the behavioural models. The latter part of the chapter provides a short review of semiconductor modelling methods and a literature survey of behavioural IGBT models. One objective of the chapter is to explain the phenomena modelled with the simulation models described in Sections 3.1 and 3.2 and present the theory needed when comparing simulation and measurements results in Section 4.4. Moreover, the outcomes of the literature survey is analysed to position the proposed simulation model in the research field.

2.1 Introduction to IGBT technologies

The main features of the physical phenomena inside an IGBT component and the device–circuit interaction are presented and described in this section. Furthermore, different chip technologies, such as punch-through (PT), non-punch-through (NPT), and field-stop (FS), are discussed. Considering the technologies, the emphasis is on FS chips because this technology is widely used in modern IGBTs and also the IGBT module investigated in this study is of FS type (Infineon, 2016). IGBT operation can be divided into several operating regions depending on the gate control state and external circuit conditions. The operating regions are first introduced in brief, and then, the IGBT operation in the active region, known as the current saturation region, and transient states are discussed in more detail, as they are more relevant in the short-circuit operation than the other operating regions.

The IGBT theory is discussed in numerous papers in academic journals, but most of the papers are concentrated on only one or a few details of the component. Therefore, a preferable way to get an overview of the IGBT structure and its behaviour is to examine textbooks on the IGBT. Detailed analytical investigation of the IGBT from the perspective of semiconductor physics is presented for example in (Baliga, 2019) and (Khanna, 2003). Moreover, information about the IGBT behaviour from the application perspective is given in (Lutz et al., 2018). In addition, several books published by IGBT manufacturers, such as (Volke et al., 2017) and (Wintrich et al., 2015), provide general information about the device behaviour and device–circuit interaction. The textbooks (Baliga, 2019) and (Lutz et al., 2018) with their relevant chapters are used as a background for this section.

According to (Lutz et al., 2018), the IGBT was invented by F. Wheatley and H. Becke in the United States of America in the early 1980s; the patent application was filed in 1980, and the patent was granted in 1982. In the same year, 1982, Baliga et al. presented an experimental demonstration of a practical IGBT structure (Baliga et al., 1982). According
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to (Khanna, 2003), the first IGBTs were available in the market in 1983, whereas (Lutz et al., 2018) states that the first IGBTs were commercially available (in Japan and Europe) approx. ten years after the first patents.

The basic idea of the IGBT is to combine the best features of the MOSFET transistor and the BJT, namely the easy switch controllability through the MOSFET gate and the low on-state losses of the BJT. The first IGBTs can be considered a MOSFET with the drain side N⁺ layer replaced with a P⁺ type layer. Owing to latch-up issues, this component type was modified to include a medium doped N-type layer (N-buffer) between the low-doped N⁺ drift region and the collector-side P⁺ layer. The result is a PT structure presented in Figure 2-1a. Because of the expensive manufacturing process, problematic parallel connection, and other drawbacks in the PT structure, the NPT structure was developed. In the NPT structure, no N-buffer layer is used, but to achieve the same voltage blocking capability, the N⁻ drift region is made wider. Thus, in the basic form, the NPT chip is thicker than the PT structure. However, the main benefits of the NPT structure are the less expensive manufacturing process, a good parallel connection because of the positive on-state temperature coefficient, and more robust short-circuit operation. The IGBT NPT structure is presented in Figure 2-1b. It is noteworthy that the PT and NPT structures in Figure 2-1 are not in scale. Commonly, the NPT structure is thinner than the PT structure if the voltage class is the same. The junctions between the semiconductor layers are denoted by J₁, J₂, and J₃ in the figure.

The PT and NPT structures can be improved by some further modifications. Nowadays, the field-stop (FS) technology is used in modern IGBTs to combine the advantages of the NPT and PT structures. In this technology, the component has an N⁻ drift region, an N⁺ field-stop (or buffer) layer, and a thin P⁺ region on the collector side. Because of the field-stop layer, the drift region can be thinner than in the NPT structure. In the FS and NPT structures, the manufacturing process is started with the N⁻ drift region substrate, whereas in the PT structure the process starts from the P⁺ substrate. Because of the differences in the manufacturing technology, the P⁺ region on the collector side in the FS structure can be made much thinner than in the PT structure. The manufacturing processes are explained for example in (Lutz et al., 2018). The FS structure has lower switching and conduction losses than the PT IGBT, but the short-circuit rating is similar to the NPT IGBT. Furthermore, owing to the positive temperature coefficient of the saturation voltage, the parallel connection of the components is easier than with PT IGBTs that have a negative coefficient. The FS IGBT structure is presented in Figure 2-2. Some manufacturers use their own brand names for the technologies discussed above. For example, the terms “soft punch-through” (SPT) or “extreme light punch-through” (XPT) are used for field-stop in some catalogues. SPT is used for example by ABB (ABB, 2020) and XPT by IXYS (IXYS, 2020).
Another commonly applied modification in the IGBT structure is the trench gate (TIGBT). In this structure, the planar gate contact is replaced by an embedded gate contact to reduce the on-state losses. With the planar gate, the charge carrier concentration decreases from the collector to the emitter, but with the trench gate, it can even increase towards the emitter. As a result, the carrier concentration almost equal to the PiN diode can be achieved with modern components. The construction of the trench gate IGBT is presented in Figure 2-2.

Even though the technology used in the IGBT chip has a significant effect on the component behaviour, it is not very relevant from the perspective of short-circuit modelling with simplified behavioural models. If more detailed models are to be developed, the chip technology and the chip internal structure have to be considered further. For example, the tail current of the IGBT has a very different behaviour depending on the chip technology. In the following, the physical background of the IGBT operation is described in order to understand what kinds of complex mechanisms are modelled with the behavioural models in this study.
2.2 Different operating points of IGBT

The internal phenomena of an IGBT component can be examined for example by using analytical equations derived from semiconductor physics. Owing to the complex three-dimensional structure of the IGBT chip, some simplifications have to be made to keep the investigation within reasonable limits. Also in simplification cases, analytical equations can be used to describe the internal physics of the IGBT to a sufficient extent. Because measurements cannot be performed inside the component, the analysis of internal processes has to rely on theory, and in some cases, simulations. Simulation methods are discussed in Section 2.4.

The operation of the IGBT can be divided into blocking mode, forward conduction mode, current saturation mode, and transient state. Furthermore, the transient state can be divided into turn-on and turn-off states. The blocking mode is not relevant from the perspective of short-circuit operation, and therefore, it is not discussed here. Basics of the forward conduction mode are needed to understand the current saturation mode, and therefore, they are discussed at a general level. In a short-circuit, the IGBT is operating in the current saturation mode, where the current through the component is limited to the value determined by the component structure, gate-side control, temperature, and voltage across the component. This is also designated as active region operation. The turn-on and turn-off transients are also significant in the short-circuit analysis. The following analysis concentrates on the current saturation mode and the turn-on/off transients. Simplified equivalent circuits are used to clarify the analysis.

2.2.1 Forward conducting mode

The IGBT can be transferred from the forward blocking state to the forward conducting state by increasing the gate-emitter voltage $V_{GE}$ above the threshold voltage $V_{TH}$ of the component. Under these conditions, a MOSFET channel from the emitter-side $N^+$ region
to the $N^-$ drift region is formed, which enables electron injection from the emitter into the drift region if the component collector potential is high enough. Furthermore, the increased electron density in the drift region enables hole injection from the collector through the $P^+$ collector/$N^-$ region junction. The concentration of the injected holes exceeds the doping concentration of the drift region, and the conductivity of the region increases rapidly (this is called conductivity modulation). The $N^-$ drift region is now operating under high-level injection conditions, and its resistivity becomes low.

If the gate-emitter voltage $V_{GE}$ is only slightly above the threshold voltage $V_{TH}$, the current through the MOSFET channel is limited and the collector current saturates to a value, which mainly depends on $V_{GE}$. In this state, the component is in the current saturation mode, or it is said to operate in the active region. This operating state is discussed further in Section 2.2.2.

If $V_{GE}$ is much larger than $V_{TH}$, the MOSFET channel is fully conducting, and the collector current is determined by the load conditions (excluding the short-circuit condition). In this case, the component is in the on-state, and it is said to operate in the linear region or in saturation. The collector-emitter voltage $V_{CE}$ is small in this state, which is desirable in order to achieve low on-state losses.

In a very simple form, the on-state operation of an IGBT can be modelled by a series connection of the MOSFET and the PiN diode as presented in Figure 2-3. The voltage drop in the forward conduction mode $V_{IGBT}$ of an equivalent circuit of this kind is the sum of the voltage drop $V_{MOSFET}$ of the MOSFET channel and the voltage drop $V_{PIN}$ of the PiN diode

$$ V_{IGBT} = V_{PIN} + V_{MOSFET}. $$

According to (Baliga, 2019), $V_{PIN}$ depends on the semiconductor material properties, the chip geometry, and the collector current density, whereas $V_{MOSFET}$ depends on the channel parameters, the collector current density, and the gate-emitter voltage. At low collector current densities the first term is dominant, and the collector current is increasing exponentially as a function of voltage. At higher current densities the effect of the second term increases as a result of the MOSFET channel resistance, and the collector current increases more linearly.

A one-dimensional PiN-diode/MOSFET equivalent circuit is adequate in simple cases. However, the voltage drop across the $N^-$ drift region cannot be described accurately without taking the 2D effects into account. In addition, as the IGBT is a bipolar component, both the electrons and the holes participate in the charge transport, which should also be considered in the voltage drop calculation. The current in the on-state concentrates on the drift region part below the gate contact, and the voltage drop in this part can be described by the PiN-diode model, but a part of the current travels through the chip in the region located below the deep $P^+$ base. This part is the hole current. The IGBT electron and hole current paths in the on-state are presented in Figure 2-4a. In actual
devices, the shape of the P⁺ base region on the emitter side is usually more complex than the shape illustrated in the figure. Often, the P⁺ base region has a thicker section straight under the emitter contact. This has an effect on the calculation of the voltage drop in the N⁺ drift region, and it also influences the voltage drop in the MOSFET part. In this case, however, the main principle is to separate the currents caused by electrons and holes and use them to define the voltage drops in different parts of the device.

With this kind of division, the voltage drop of the IGBT can be presented as

\[
V_{\text{IGBT}} = V_{\text{P+N}} + V_{\text{drift}} + V_{\text{MOSFET}},
\]

where \(V_{\text{P+N}}\) is the voltage drop of junction J₁, \(V_{\text{drift}}\) is the voltage drop of the N⁺ drift region, and \(V_{\text{MOSFET}}\) is the voltage drop of the MOSFET channel. The IGBT on-state voltage drop can be divided into these three parts in the PT, NPT, and FS structures; however, the values of the voltage drop terms vary between technologies.
When the IGBT is in the on-state, the N’ drift region is flooded with electrons supplied from the MOSFET channel, but to ensure charge neutrality, also holes are injected from the P’ region on the collector side to the N’ drift region. Thus, the charge carrier density in the N’ drift region is significantly increased, and the resistance of the region is reduced. This is called conductivity modulation, and the N’ drift region is operating under high-level injection conditions.

In principle, the voltage drop in the N’ drift region $V_{\text{drift}}$ can be solved by determining the electric field $E$ along the drift region and integrating it from junction $J_1$ to junction $J_2$. With simplifications, this can be done analytically in one dimension, but for accurate results, also two-dimensional effects have to be taken into account, because most of the current is flowing in the drift region part located directly under the gate (in planar gate structures). Furthermore, if a highly doped N’ region (N-buffer) is applied on the collector side, as is the case in the field-stop or punch-through technologies, the analysis of $V_{\text{drift}}$ is even more complicated because $V_{\text{drift}}$ includes voltage drops across the N’ drift region and the N-buffer region.

According to (Baliga, 2019) the voltage drop $V_{P\rightarrow N}$ in junction $J_1$ can be determined by solving the minority carrier concentration in the junction. However, if an N-buffer layer is applied, the voltage drop calculation becomes slightly more complicated, because if the N-buffer layer doping is high enough, it is no longer operating under high-level injection conditions, which affects the analysis.

In a simple form, the voltage drop $V_{\text{MOSFET}}$ across the MOSFET part can be determined by the channel resistance $R_{\text{CH}}$ as presented in Eq. (2.3).
where $L_{CH}$ is the channel length, $Z$ is the channel width orthogonal to the surface in Figure 2-4, $\mu_n$ is the electron mobility in the channel, $C_{OX}$ is the specific gate oxide layer capacitance (the capacitance is given per surface area), $V_{GE}$ is the applied gate-emitter voltage, and $V_{TH}$ is the threshold voltage.

Owing to the two-dimensional effects presented in Figure 2-4b, the voltage drop of the MOSFET $V_{MOSFET}$ includes three terms; the voltage drop in the channel $V_{CH}$, the voltage drop in the accumulation layer $V_A$, and the voltage drop in the JFET region $V_{JFET}$. The accumulation layer is formed in the region where the velocity of the electrons from the MOSFET channel is increased when arriving at the N$^-$ drift region, and the JFET region is formed between the P-base region, where the current through the IGBT is crowded. In many cases, the doping concentration of the N$^-$ drift region is increased to decrease the resistance of the JFET region. If the trench gate structure (Figure 2-2b) is applied, there is no JFET region in the component, and smaller on-state voltage drops can be achieved.

As presented above, an accurate analysis of the IGBT on-state voltage drop requires very detailed information about the component structure. However, the purpose of the previous analysis was to provide a general description of the IGBT behaviour in the on-state and show how the current flows in a simplified IGBT structure. This information is needed to understand the IGBT current saturation mode and the effect of temperature on the saturated current, which will be discussed in the following sections.

### 2.2.2 Current saturation mode

As described in the previous section, the IGBT can operate in the current saturation mode, which is also called the active region in the component operation. In this mode, the collector current saturates at a value that depends mainly on the gate-emitter voltage $V_{GE}$ and the saturation state transconductance $g_m$. From the perspective of the short-circuit behaviour, the analysis of this mode is of the most significance as it gives information about why the IGBT limits its current to a certain value, simultaneously supporting high voltage, and is able to tolerate this operation for a limited time period.

The best way to understand the IGBT behaviour in the current saturation mode is to use an equivalent circuit presentation that includes a MOSFET part on the component gate/emitter side with the parallel-connected BJT part on the component collector side as presented on the left in Figure 2-5. The advantage of this model is that it divides the collector current into two components; the electron current $I_n$ and the hole current $I_p$. The electron current flows through the MOSFET part, and the hole current flows through the BJT part. The current paths inside the simplified IGBT structure are presented on the right in Figure 2-5.
As it can be seen in Figure 2-5, the gate-side MOSFET drives the pnp part, providing the base current for it. The currents are linked together by the common base current gain $\alpha_{\text{PNP}}$ as

$$I_p = \left( \frac{\alpha_{\text{PNP}}}{1 - \alpha_{\text{PNP}}} \right) I_n,$$

(2.4)

As the emitter current $I_E$ of the IGBT is a sum of $I_n$ and $I_p$, and because of the high input impedance of the MOSFET, the gate current $I_G$ is almost zero, it can be assumed that the collector current $I_C$ is approximately the same as $I_E$:

$$I_E = I_n + I_p = \frac{I_n}{1 - \alpha_{\text{PNP}}} \approx I_C$$

(2.5)

In the current saturation mode, the electron current $I_n$ through the MOSFET channel is saturated as a result of the channel pinch-off phenomenon. Consequently, the pnp transistor base current is limited, which restricts the hole current $I_p$ through the transistor. Therefore, also the collector current $I_C$ is saturated.

The origin of the channel pinch-off is the finite resistivity of the channel. The principle for the channel formation in the IGBT is similar to the MOSFET device. An enlarged
MOSFET channel of the IGBT is presented in Figure 2-6 and Figure 2-7 to describe the channel and its pinch-off phenomenon.

The current flow between the n-type regions (N⁺ emitter and N' drift region) becomes possible when the inversion layer is formed into the p-type (P-base emitter) semiconductor. If the bias of the N' drift layer $V_{n'}$ is positive but there is no gate bias, a current flow is not possible. In this case, the voltage is supported by junction $J_2$. If the gate bias is increased above the threshold voltage $V_{TH}$, a conductive inversion layer under the gate is formed, and the channel enables the current flow. Thus, a positive bias in the N' drift region injects electrons from the emitter.

The charge at the channel $Q_{CH}$ depends on the oxide capacitance $C_{OX}$, the applied gate bias $V_G$, and threshold voltage $V_{TH}$ as

$$Q_{CH} = C_{OX}(V_G - V_{TH})$$  \hspace{1cm} (2.6)

A small $V_{n'}$ compared with the gate bias $V_G$ causes a uniform charge at the channel. Since the channel does not have infinite conductivity, the current through it causes a voltage drop along the channel. This voltage reduces the effect of the gate bias, and thus, the charge in the channel near junction $J_2$ becomes smaller. This is illustrated in Figure 2-6b as a shrunk inversion layer at its right end. The resistance of the channel $R_{CH}$ can be defined from the structural dimensions, material properties, and the applied gate bias as presented in (Baliga, 2019):

$$R_{CH} = \frac{L_{CH}}{Z\mu_n C_{OX}(V_G - V_{TH})},$$  \hspace{1cm} (2.7)

where $L_{CH}$ is the channel length, $Z$ is the depth of the cell, and $\mu_n$ is the electron mobility in the channel.
When the current through the channel increases further, the $V_{n-}$ bias also increases as a result of the voltage drop in the channel, and at some point, $V_{n-}$ is equal to $V_{G}-V_{TH}$, and there is no longer enough potential difference to produce an inversion layer near junction $J_2$. Thus, the channel is pinched off and the current is saturated to the value dependent on the gate bias.

If the voltage $V_{n-}$ still increases, the current remains at the same saturated value (in practice, it may increase slightly), and the excess $N^-$ drift region voltage is supported by a depletion region formed across junction $J_2$ and the channel area. Thus, the channel shrinks further as shown in Figure 2-7b. Even though there is no channel on the entire length between the $N$ regions, a current flow still exists, as electrons can be transported from the emitter into the channel and from the channel edge through the depletion region into the $N^-$ drift region by a vertical electric field.

The analytical solution of the saturated collector current requires a few assumptions about the channel and gate conditions. In (Baliga, 2019), the following assumptions have been made to achieve a solution:

1. The MOS structure is ideal and there is no charge transport through the gate dielectric.
2. The carrier mobility in the inversion layer is not affected by the transverse or vertical electric fields.
3. The P-base is uniformly doped.
4. The current transport through the channel takes place only by drift.
5. Leakage currents are negligible.
6. The transverse electric field is much higher than the vertical electric field.

By using these assumptions, based on the calculation of resistance (Eq. (2.7)) for an infinitely small channel width $dx$ and the calculation of charge along the channel length,
and assuming that the same current has to flow through the whole channel, the value for the linear region channel current $I_{CH}$ can be determined as

$$I_{CH} = \frac{Z\mu_n C_{OX}}{2L_{CH}} [2(V_G - V_{TH})V_{n-} - V_{n-}^2]. \quad (2.8)$$

When $V_{n-}$ is small compared with $V_G$, the latter term of the equation will become insignificant, and the channel resistance for this condition (linear region) can be defined as

$$R_{CH} = \frac{V_{n-}}{I_{CH}} = \frac{L_{CH}}{Z\mu_n C_{OX}(V_G - V_{TH})}. \quad (2.9)$$

This is the same expression that is used in Eq. (2.3), and it can be concluded from this form that the channel resistance can be decreased by increasing the gate voltage.

In a pinch-off condition, the $N^-$ drift region potential is equal to the difference between the gate bias and the threshold voltage ($V_{n-} = V_G - V_{TH}$). Thus, Eq. (2.8) modified for the saturation channel current can be written as

$$I_{CH,sat} = \frac{Z\mu_n C_{OX}}{2L_{CH}} (V_G - V_{TH})^2. \quad (2.10)$$

This is the electron current $I_n$ of the IGBT, and by substituting it into Eq. (2.5), the total saturated collector current of the IGBT can be given as

$$I_{C,sat} = \frac{I_n}{1 - \alpha_{PNP}} = \frac{Z\mu_n C_{OX}}{2L_{CH}(1 - \alpha_{PNP})} (V_G - V_{TH})^2. \quad (2.11)$$

The device transconductance in the current saturation mode is defined as a ratio of the collector current change and the gate voltage change:

$$g_m = \frac{dI_{C,sat}}{dV_G} = \frac{Z\mu_n C_{OX}}{2L_{CH}(1 - \alpha_{PNP})} (V_G - V_{TH}). \quad (2.12)$$

Because of the additional $1 - \alpha_{PNP}$ term in Eq. (2.11) and Eq. (2.12), $I_{C,sat}$ and $g_{m,sat}$ of the IGBT are approximately twice as high as the MOSFET equivalents if the same channel structure is used (Baliga, 2019).

The following equation is achieved if Eq. (2.11) is rearranged:

$$I_{C,sat} = \frac{1}{1 - \alpha_{PNP}} \cdot \frac{Z\mu_n C_{OX}}{2L_{CH}} \cdot (V_{GE} - V_{TH})^2. \quad (2.13)$$
The first term of Eq. (2.13) describes the current of the BJT part, and two latter terms the current of the MOSFET part. This presentation shows clearly that $I_{C, \text{sat}}$ depends on the BJT part current gain $\alpha_{\text{PNP}}$, the MOSFET channel parameters, and the gate-emitter voltage $V_{GE}$.

The common base current gain $\alpha_{\text{PNP}}$ for the IGBT can be defined as

$$\alpha_{\text{PNP}} = \gamma_p \cdot \alpha_T,$$

(2.14)

where $\gamma_p$ is the emitter injection efficiency of the pnp part, and $\alpha_T$ is the base transport factor.

According to (Baliga, 2019), the injection efficiency is independent of $V_{GE}$ and $V_{CE}$. However, the base transport factor changes as a function of $V_{CE}$, and consequently, also $I_{C, \text{sat}}$ changes as a function of $V_{CE}$. The voltage dependence of $\alpha_{\text{PNP}}$ will be discussed further in Section 2.2.3.

The exact form of $\alpha_{\text{PNP}}$ also includes a third term, the collector injection efficiency, but it does not become dominant until the $V_{CE}$ level is close to the breakdown voltage. Thus, in this case it is relevant to analyse $\alpha_{\text{PNP}}$ with two terms. In some references (e.g. (Baliga, 2019)), the collector injection efficiency is also called a multiplication factor.

### 2.2.3 Effect of $V_{DC}$ on $I_{C, \text{sat}}$

The component output and transfer characteristics define the behaviour of the collector current $I_C$ as a function of the gate-emitter voltage $V_{GE}$ and the collector-emitter voltage $V_{CE}$. This information is the basic information presented in the component datasheets, but in many cases the range of $V_{GE}$ and $V_{CE}$ is very limited from the perspective of short-circuit operation. The output characteristics define the static $I_C$–$V_{CE}$ behaviour of the IGBT. The output characteristics of the IGBT module used in the experimental part of this study are presented on the left in Figure 2-8.
As it can be seen in the figure, the range of the output characteristics $V_{CE}$ is limited to a few volts, and thus, the current saturation values of higher collector-emitter voltages lie outside the output chart. In the short-circuit operation, the whole DC link voltage is supported across the IGBT, and therefore, the output characteristics that also include short-circuit operation should be depicted for much higher voltages. For this particular component, a reasonable DC link voltage can be approx. 600–800 V. Extended idealized output characteristics up to the IGBT breakdown voltage $V_{BR}$ are presented on the right in Figure 2-8.

However, $I_{C,sat}$ does not remain constant as a function of $V_{CE}$, but it slightly increases with an increasing voltage. When taking the $I_{C,sat}$ dependence on $V_{CE}$ into account and adding the breakpoint behaviour, idealized output characteristics can be illustrated as in Figure 2-9.
2.2 Different operating points of IGBT

For example in (Basler, 2014) and (Kopta, 2010) it is stated that $I_{C,\text{sat}}$ slightly increases with an increasing $V_{CE}$. In (Basler, 2014), the IGBT chip $I_{C,\text{sat}}$ was measured with several $V_{CE}$ values; the results are presented in Figure 2-10. The study concentrated on high-voltage IGBT chips, but the origin of the phenomenon is from a basic IGBT structure, and thus, the assumptions made of high-voltage IGBTs are valid also for low-voltage IGBTs. The measurements were performed with a method where the self-heating effect during a short-circuit was mitigated. The self-heating effect will be discussed in more detail in Section 2.2.4.

![Figure 2-9 Full output characteristics of the IGBT with the $I_{C,\text{sat}}$ dependence on $V_{CE}$ included.](image)

![Figure 2-10 Measurement results of $I_{SC}$ as a function of $V_{CE}$ (Basler, 2014).](image)
Figure 2-10 shows that after the current saturation point, the collector current increases almost linearly with an increasing $V_{CE}$ until the breakdown point, and the current gradient increases as $V_{GE}$ increases.

The reason why $I_{C,\text{sat}}$ increases with higher $V_{CE}$ voltages is that the bipolar current gain $\alpha_{PNP}$ of the IGBT internal pnp transistor increases as a function of $V_{CE}$. $\alpha_{PNP}$ can be calculated by Eq. (2.15)

$$\alpha_{PNP} = \gamma_p \cdot \alpha_T, \quad (2.15)$$

where $\gamma_p$ is the emitter efficiency of the p-collector, and $\alpha_T$ is the base transport factor.

The emitter efficiency of the IGBT pnp BJT part basically describes the proportion of the hole current of the total emitter current. To clarify the terminology, when discussing the emitter of the IGBT pnp transistor part, the same terminal is also the collector of the IGBT (Figure 2-5). When the base-emitter junction is forward biased, the minority carriers are injected through the junction, in other words, electrons are injected from the base (n-type semiconductor) to the emitter region (p-type semiconductor), and holes are injected from the emitter to the base region. Holes that are injected from the emitter to the base produce current $I_{pE}$ across the junction, and thus, the emitter efficiency is

$$\gamma_p = \frac{\partial I_{pE}}{\partial I_E} = \frac{I_p}{I_p + I_n}, \quad (2.16)$$

where $I_E$ is the total emitter current, $I_p$ is the hole current at the base emitter junction, and $I_n$ is the electron current at the base emitter junction. The emitter efficiency is always less than 1 under high injection conditions. If the current through the component is large, a large amount of minority carriers are injected from the emitter to the base to maintain charge neutrality in the base region, and the minority carrier concentration can exceed the doping concentration of the base region. This is called high-level injection. Because the current density is high in the short-circuit, it can be assumed that high-level injection conditions are met, and the emitter efficiency is always less than 1 in the short-circuit.

The hole current at the base emitter junction is also related to the transport factor. This term is a ratio of the hole current at the base-emitter junction $I_{pE}$ to the hole current at the base-collector junction $I_{pC}$ as

$$\alpha_T = \frac{\partial I_{pE}}{\partial I_{pC}} \quad (2.17)$$

A part of the hole current at the emitter-base junction is diffused in the base region if the diffusion length of the holes $L_{ph}$ is shorter than the base width $W_B$. Usually, this condition holds in high-voltage IGBTs, where the N' drift region (which is the base for the pnp part) is made relatively wide so that the component can support high voltages without reach-
2.2 Different operating points of IGBT

through breakdown. Normally, also \( \alpha_T \) is less than 1. If the diffusion length is much larger than the base width, \( \alpha_T = 1 \).

The theoretical background of chancing \( \alpha_{PNP} \) as a function of IGBT collector emitter voltage is presented for example in (Basler, 2014) and (Baliga, 2019). The transport factor is given by

\[
\alpha_T = \frac{1}{\cosh \frac{l}{L_p}},
\]

where \( l \) is the effective base width, and \( L_p \) is the diffusion length of the holes.

As the electric field inside the IGBT during a short-circuit is expanding towards the IGBT collector when \( V_{CE} \) is increased, the effective base width \( l \) decreases, which causes an increase in \( \alpha_T \). Consequently, \( \alpha_{PNP} \) increases, which induces an increase in \( I_{C,sat} \). In IGBT structures with a buffer layer, the base transport factor consists of two terms, \( \alpha_{TN} \) and \( \alpha_{TB} \). The first one is the base transport factor of the N drift region, and the latter one is the base transport factor of the buffer layer (which is independent of \( V_{CE} \))

\[
\alpha_{PNP} = \gamma_p \cdot \alpha_{TN} \cdot \alpha_{TB}.
\]

When \( V_{CE} \) attains a level where the electric field inside the component reaches the buffer layer, also \( \alpha_{TN} \) becomes independent of \( V_{CE} \). After this \( V_{CE} \) level, \( I_{C,sat} \) is mainly determined by the multiplication factor (Baliga, 2019). The point where the electric field reaches the buffer layer causes a change in the \( I_{C,sat} \) gradient in the output characteristics, which can also be seen in Figure 2-10.

Because of the very non-linear behaviour of \( \alpha_{PNP} \), an exact analysis of the \( I_{C,sat} \) voltage dependence is quite a complicated task especially for components with a buffer layer. Thus, for example the early voltage effect, which can be used to estimate the BJT current in the saturation region, is not applicable to IGBTs with a buffer layer.

Transfer characteristics

Furthermore, the IGBT transfer characteristics (\( I_C \) as a function of \( V_{GE} \)) can be used to analyse short-circuit operation. However, the transfer characteristics are typically given only for a limited range of \( V_{GE} \) and determined with a low \( V_{CE} \). The transfer characteristics of the IGBT investigated in this study are presented in Figure 2-11. In this particular case, the characteristics in the datasheet are limited to the value \( V_{GE} = 12 \) V.
2.2.4 Effect of self-heating and temperature on $I_{C,\text{sat}}$

During a short-circuit, the IGBT is conducting a high current with a high voltage across it. This causes a large amount of power losses generated inside the semiconductor chip. Consequently, this can introduce a very rapid temperature rise in the chip. Usually, the short-circuit withstand rating given in manufacturer datasheets is in the range of 8–10 µs for low-voltage IGBTs, and thus, self-heating has to be considered on the same time scale.

An increased temperature of the component has an effect on the semiconductor properties, and for an IGBT it means that $I_{C,\text{sat}}$ is lower for higher temperatures, as shown in Figure 1-3.

The thermal network parameters for a Cauer- or Foster-type network from the chip junction to the module base plate are usually provided in the component datasheet. In many cases, however, the time constants of the network parameters are so large that they cannot be used for thermal modelling in short-circuit conditions, which take place on the microsecond time scale. Furthermore, if the parameters are given for a Foster-type thermal network, the parameters do not have physical significance, and thus, the network does not describe the thermal capacity of a semiconductor chip. Because a short-circuit event is a very fast process, it can be assumed that there is no heat transfer between the IGBT chip and the module baseplate.
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By assuming that the short-circuit is turned off within a couple of tens of microseconds or less, the increase in the chip temperature can be calculated by using the thermal capacity $C_{th}$ of the chip and the loss energy generated inside the chip $W_{SC}$

$$\Delta T_j = \frac{W_{SC}}{C_{th}} = \frac{I_{SC} \cdot V_{DC} \cdot t_{SC}}{C_{th}},$$

(2.20)

where $I_{SC}$ is the short-circuit current, $V_{CE}$ is the voltage across the device, and $t_{SC}$ is the duration of the short-circuit pulse. The following equation can be used to calculate $C_{th}$,

$$C_{th} = c_{th,Sl} \cdot \rho \cdot d \cdot A,$$

(2.21)

where $c_{th,Sl}$ is the specific heat capacity (of silicon in this case), $\rho$ is the density of silicon, $d$ is the chip thickness, and $A$ is the area of the chip.

The heat transfer during a short-circuit is discussed in (Jia et al., 2019) and (Cavallaro et al., 2018). According to these publications, there is no significant heat transfer from the IGBT chip to the backside material during a short-circuit, and thus, the assumption to use only one heat capacity in the thermal circuit to describe the chip temperature behaviour under short-circuit conditions is valid. However, it is suggested in these papers that the front-side cooling of the component could improve the short-circuit ruggedness, because there is also heat transfer through the bond wires (or other chip connection method). Thus, if the component short-circuit ruggedness is investigated in detail, it would be advisable to also include bond wires in the thermal model. But if the chip temperature behaviour is investigated only during a short-circuit, not after it, the effect of bond wires is not significant, as presented in (Jia et al., 2019). In the simulation results in (Jia et al., 2019), the bond wires start to heat up at $t = 1$ ms, and there is no notable heating at $t = 10$ µs when the short-circuit is turned off.
It is also pointed that the temperature increase of the chip $\Delta T_j$ is more critical for low-voltage components ($V_{CE,max} < 1700$ V) than for high-voltage ones. The reason is that the thickness of the N' drift region of the chip is mainly determined by the voltage rating, and it has to be increased to get a higher voltage rating. If the thickness of the N' region is increased, it increases the overall chip thickness $d$, which (according to Eq. (2.21)) then increases the thermal capacity $C_{th}$. Generally, high-voltage IGBT chips tolerate longer short-circuit pulses than low-voltage IGBTs because of their higher thermal mass.

An analytical investigation shows that the analysis presented above is not true in reality, even though it can be used to estimate the chip temperature as an initial approximation of the chip temperature for the self-heating effect. In (Baliga, 2019), it is stated that the top side of the chip suffers a much higher temperature at a short-circuit than the bottom side. Because it is assumed that there is no heat transfer during the short-circuit owing to the short time intervals and the high thermal capacity of the IGBT base plate, the bottom side of the chip is always at the base plate temperature.

Considering thermal runaway, the device is destroyed if the critical temperature $T_{CR}$ of the semiconductor material is exceeded (for silicon $T_{CR,SI} = 700$ K). By using the critical temperature, Eq. (2.22) can be used to calculate the maximum short-circuit time in which thermal runaway does not occur if a uniform temperature distribution is assumed. This, however, gives overestimated results because the temperature distribution is not uniform, and the hottest spot of the chip is located at the top of the chip.
\[ t_{SC,\text{max}} = \frac{\Delta T_j \cdot C_{th}}{I_{SC} \cdot V_{DC}} = \frac{(T_{CR} - T_{HS}) \cdot C_{th}}{I_{SC} \cdot V_{DC}}, \]  

(2.22)

where \( T_{HS} \) is the heat sink temperature.

According to (Baliga, 2019), the temperature distribution across the chip thickness \( y \) can be solved by using the thermal diffusion equation

\[ \frac{\partial T}{\partial t} = D_{th} \frac{\partial^2 T}{\partial y^2} + \frac{Q_{th}}{S_y}, \]  

(2.23)

where \( D_{th} \) is the thermal diffusivity, and \( Q_{th} \) is the power generated per unit volume. \( D_{th} \) is 0.9 cm\(^2\)/s for silicon.

By using the thermal diffusion length \( L_{th} \) and the rate of increase in temperature with the time \( R_T \), the solution for Eq. (2.23) can be expressed as

\[ T(y, t) - T_{HS} = (R_T \cdot t) e^{-(y/L_{th})}, \]  

(2.24)

The solution for the temperature increase rate \( R_T \) is then

\[ R_T = \frac{dT}{dt} = \frac{K_T \cdot I_{SC} \cdot V_{DC}}{C_{th}}. \]  

(2.25)

The constant \( K_T \) represents non-uniform temperature distribution along the wafer thickness.

If the maximum short-circuit time is calculated by assuming a uniform temperature distribution (Eq. (2.22)) with the parameters \( C_{th} = 0.033 \) Ws/K, \( V_{DC} = 800 \) V, \( I_{SC} = 5600/12 \) A = 466.67 A, and \( T_{HS} = 298.15 \) K, the result is \( t_{SC,\text{max}} = 35.52 \) µs, which is much more than the maximum short-circuit time defined in the datasheet.

When the temperature distribution over the chip thickness \( y \) is calculated by Eq. (2.24) for different short-circuit pulse lengths 5 µs, 10 µs, 15 µs, and 20 µs, the following results can be obtained. In the calculation, the constant \( K_T \) is assumed to be 3.5 (Baliga, 2019), and the chip thickness is 140 µm.
It can be seen that with the short-circuit pulse length $t_{SC} = 10 \, \mu s$, which is also the maximum pulse length given in the component datasheet, the maximum temperature is close to the critical temperature $T_{CR, Si}$ of silicon.

If $K_T$ is selected to be 1, the maximum temperature reaches $T_{CR, Si}$ with $t_{SC} = 35.52 \, \mu s$, which was also the result with Eq. (2.22) when a uniform temperature distribution was assumed.

As presented in Figure 1-3, the short-circuit current decreases during a short-circuit pulse as a result of the increasing chip temperature. In (Basler, 2014) and (Lutz et al., 2018), it is stated that three temperature-dependent parameters affect in the IGBT short-circuit: the bipolar current gain $\alpha_{PNP}$, the mobility of electrons $\mu_n$, and the threshold voltage $V_{TH}$. However, at higher voltages, $\mu_n$ is the main contributor to the $I_{C, sat}$ reduction.

The decrease in the electron mobility is caused by the local heating of the MOSFET channel during the short-circuit as presented in (Trivedi and Shenai, 1996) and (Trivedi and Shenai, 1998). The increasing temperature in the MOSFET channel decreases the electron mobility $\mu_n$, as shown in Figure 2-14, and consequently, the resistance of the MOSFET channel increases. The electron current flows also through the N' drift region, and thus, a decrease in $\mu_n$ also increases the resistance of the drift region. Hence, an increase in the overall resistance can be seen as a decrease in $I_{C, sat}$ during a short-circuit pulse. The temperature dependence of electron mobility is caused by carrier scattering in the semiconductor material (Lutz et al., 2018), which is the reason why it also depends on the carrier concentration. According to (Basler, 2014), the carrier concentration of
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3.5e17 cm$^3$ (dashed line in Figure 2-14) corresponds to the carrier concentration in the IGBT n-channel during a short-circuit.

![Figure 2-14 Temperature dependence of the electron mobility $\mu_n$ in silicon (Basler, 2014).](image)

2.2.5 Transient states

From the perspective of a dynamic state, the component capacitances have a significant effect on the component operation. In addition, the parasitic components of the IGBT module and the rest of the commutation circuit have a significant influence on the transient behaviour of the switch component. Moreover, the gate driver behaviour and its implementation to the main circuit should be taken into account in the IGBT dynamic state investigation.

IGBT capacitances

The internal capacitances of the IGBT are presented in Figure 2-15a (Infineon, 2015). Some of the capacitances are variable, that is, the value of the capacitance depends on the operating point. In Figure 2-15b, the IGBT terminal capacitances are presented with a MOSFET/BJT equivalent circuit presentation. Considering the equivalent circuit capacitances $C_{GE}$, $C_{CG}$, and $C_{CE}$, they all include one variable capacitance. The gate-emitter capacitance $C_{GE}$ is formed from the capacitances $C_1$, $C_3$, $C_4$, and $C_6$; the gate-collector capacitance $C_{CG}$ is formed from the capacitances $C_2$ and $C_5$; and the collector-emitter capacitance $C_{CE}$ is formed mainly from the variable capacitance $C_7$. The capacitance $C_3$ plays a key role as it describes the capacitive behaviour of the N$^+$ drift region of the device. When a voltage is applied across the component, a depletion region is formed into the N$^+$ drift region, and the depletion length is relative to the applied voltage. Thus, the value of the capacitance $C_3$ is relative to the applied voltage. Because
of $C_5$, the Miller capacitance $C_{CG}$ has a strong dependence on $V_{CE}$ (Luo et al., 2016). The $C_{CG}$ voltage (and current) dependence will be discussed in Section 2.2.6.

The gate-emitter capacitance $C_{GE}$ has a component $C_6$, which is formed in the P-base region, but it does not have as strong a voltage dependence (except at very low $V_{CE}$ values) as $C_5$, and therefore, in many cases, it suffices to consider $C_{GE}$ constant (Yang et al., 2015).

Moreover, the collector-emitter capacitance $C_{CE}$ is formed from $C_7$, which is formed in the N'-drift region under the P-base, and it is voltage dependent similarly to $C_{CG}$. However, $C_{CE}$ does not significantly contribute to the device behaviour in the short-circuit or transient operation, because no current is flowing through it during transient states. Thus, it can be neglected in this case. In some applications, more attention should be paid to $C_{CE}$, as it may affect the circuit resonance.

**Turn-on and -off waveforms in normal operation**

The load type connected to the commutation circuit naturally has an influence on the dynamic state behaviour of a switching component. The voltage and current waveforms in the resistive load switching differ significantly from the switching of an inductive load current. However, this section focuses on inductive load transients, because also in short-circuit operation there is some inductance as a load, and in a turn-off, short-circuit current is commutated from the IGBT to the free-wheeling diode. The IGBT turn-on behaviour is analysed for example in (Bryant et al., 2008), and the turn-off behaviour in (Ding et al., 2017) and (Xue et al., 2017).

A typical commutation circuit that can be used for inductive switching transient state analysis is presented with its main parasitic components in Figure 2-16.
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In Figure 2-16, $L_L$ and $R_L$ represent the load inductance and resistance, $L_a$ is the busbar inductance, $L_C$, $L_E$, and $L_G$ are the parasitic inductances of the IGBT main current connections, and $R_G$ is the gate resistance. When the IGBT is in the forward conduction state, the current through it is defined by $L_L$ and $R_L$. When the IGBT is turned off, the current commutates to the FWD and decays as a result of resistive losses in the circuit. In practice, in many applications, different gate turn-on and -off resistances are used instead of a single $R_G$. From here onwards, the turn-on and -off gate resistors are called $R_{g,on}$ and $R_{g,off}$, respectively.

The basic waveforms for $V_{CE}$, $V_{GE}$, and $I_C$ during an IGBT turn-on are presented in Figure 2-17.

At first, the gate circuit gets a turn-on control pulse, and $V_{GE}$ starts to rise according to the time constant determined by the turn-on gate resistor $R_{g,on}$ and the capacitances $C_{GE}$ and $C_{CG}$. At his point, $V_{CE}$ is still high, and consequently, $C_{CG}$ is small and can thus be neglected, and the time constant $\tau_{g,on}$ can be approximated by using only $C_{GE}$.
\[ \tau_{g,\text{on}} \approx R_{g,\text{on}} \cdot C_{\text{GE}}. \] (2.26)

Thus, the gate emitter voltage before \( t_1 \) can be approximated by

\[ V_{\text{GE}} = (V_{\text{GE,on}} - V_{\text{GE,off}}) \cdot (1 - e^{(-t/t_{g,\text{on}})}) + V_{\text{GE,off}}, \] (2.27)

where \( V_{\text{GE,on}} \) is the turn-on gate voltage, and \( V_{\text{GE,off}} \) is the turn-off gate voltage.

At \( t_1 \), \( V_{\text{GE}} \) reaches the threshold voltage \( V_{\text{TH}} \) and \( V_{\text{CE}} \) starts to decrease, while \( I_C \) starts to rise. Exceeding \( V_{\text{TH}} \) means that the MOS channel on the component gate side starts to conduct, which enables an electron flow to the drift region. Electrons recombine with holes when they reach the collector-side \( P^+ \) region, which further allows hole injection. Furthermore, the depletion layer starts to shrink and \( V_{\text{CE}} \) begins to decrease. The decrease rate is determined by the component depletion layer capacitances and the stray inductance \( L_S \), which in this case is a sum of the busbar parasitic inductance \( L_\sigma \) and the IGBT collector and emitter inductances \( L_C \) and \( L_E \) in Figure 2-16. Between \( t_1 \) and \( t_2 \), the collector current \( I_C \) increases almost linearly. As the load current \( I_L \) can be assumed to be approximately constant, the increase rate of \( I_C \) can be defined by using Kirchoff’s voltage law. According to Figure 2-16, the collector current gradient can be calculated by

\[ -V_{\text{DC}} + \frac{dI_C}{dt} L_S + V_{\text{CE}} = 0 \rightarrow \frac{dI_C}{dt} = \frac{V_{\text{DC}} - V_{\text{CE}}}{L_S}. \] (2.28)

The turn-on peak value of \( I_C \) attained at \( t_2 \) when the collector current is a sum of the steady-state load current and the diode reverse recovery current

\[ I_{\text{C,max}} = I_L + I_{\text{RR}}. \] (2.29)

The reverse recovery current at the diode turn-off is caused by a stored charge that remains inside the component. The stored charge must be removed before the voltage direction across the component can be changed. The current through the diode goes negative before all the charge is removed, which causes a negative reverse recovery current peak.

Between \( t_2 \) and \( t_3 \), the diode reverse voltage increases and \( V_{\text{CE}} \) further decreases. Moreover, the drift region charge is continuously increasing, and the depletion layer is shrinking towards the MOS end of the IGBT.

At \( t_3 \), the Miller capacitance \( C_{\text{CG}} \) increases along with the decreasing \( V_{\text{CE}} \), and consequently, \( V_{\text{GE}} \) remains almost unchanged. This stage is called the Miller plateau. An increase in the Miller capacitance effectively limits the decrease in the depletion layer width. During the time interval between \( t_3 \) and \( t_4 \), the decrease rate of \( V_{\text{CE}} \) is much smaller compared with the previous intervals. Owing to the high lifetime of the IGBT, the excess carrier density of the drift region is still low, which results in a high voltage drop.
After $t_4$, the collector-emitter voltage has reached its saturation value, $V_{GE}$ starts to rise again and finally reaches the steady-state value $V_{GE, on}$. Because $V_{CE}$ is still low, $C_{CG}$ has a high value, and consequently, both the input capacitance components $C_{GE}$ and $C_{CG}$ have to be included in the time constant calculation for the rising $V_{GE}$.

$$\tau_{g, on2} \approx R_{g, on} \cdot (C_{GE} + C_{CG})$$

(2.30)

A similar analysis can be performed for the turn-off transient. The turn-off overvoltage and the effect of the gate resistance and the junction temperature are investigated for example in (Chen et al., 2019). A collector-emitter voltage spike caused by the inductive load current and the commutation inductance and turn-off losses are the issues that can make the turn-off incident problematic. The basic waveforms of the collector-emitter voltage $V_{CE}$, the gate-emitter voltage $V_{GE}$, and the collector current $I_C$ during a turn-off are presented in Figure 2-18. The whole switching event can be divided into five intervals, indicated by $t_1$–$t_5$ in the figure.

![Figure 2-18 Basic current and voltage waveforms at the IGBT turn-off.](image)

The current turn-off is started by the gate capacitance discharge occurring within the time interval $t_1$–$t_2$. At this point, the $V_{GE}$ decrease rate is defined by the time constant, which is defined by the device input capacitance $C_{les}$, which is a sum of $C_{GE}$ and $C_{CG}$, and the gate resistance $R_{g, off}$. The time constant for this period is

$$\tau_{g, off1} \approx R_{g, off} \cdot C_{les} = R_{g, off} \cdot (C_{GE} + C_{CG})$$

(2.31)

During the $C_{les}$ discharge period $V_{CE}$ and $I_C$ remain unchanged.

The interval from $t_2$ to $t_3$, where $V_{GE}$ stays nearly constant, is the Miller plateau as was also in the turn-on case. During this plateau, the Miller capacitance $C_{GC}$ decreases as a function of the slightly increasing $V_{CE}$, which is the reason why $V_{GE}$ remains unchanged. As was shown in Figure 2-15a, $C_{CG}$ is formed from $C_2$, which is the oxide layer capacitance, and $C_3$, which is the depletion layer capacitance. When $V_{CE}$ starts to rise, the depletion region increases, which reduces the capacitance $C_3$.

At $t_3$, $V_{GE}$ starts to decrease with a steep slope, which also causes shrinking of the MOSFET channel. This decreases the IGBT current slightly, and the component starts to
support the voltage across it, and thus, \( V_{CE} \) rises rapidly after \( t_3 \). According to (Lutz et al., 2018) the time from \( t_3 \) to \( t_4 \), \( \tau_{g,off2} \) can be estimated by Eq. (2.32). It should be noted, however, that the value of \( C_{CG} \) changes significantly during the period, and thus, Eq. (2.32) does not give a very accurate result

\[
\tau_{g,off2} \approx R_{g,off} \cdot C_{CG}.
\]  
(2.32)

At \( t_4 \), \( V_{CE} \) reaches the \( V_{DC} \) level and the current from the IGBT starts to commutate to the free-wheeling diode, and as a result, the fall rate of \( I_C \) is very high. \( V_{GE} \) is below \( V_{TH} \), and thus, the electron current through the MOSFET channel (the electron current of the IGBT) is removed. Because of the commutation inductance \( L_{\sigma} + L_C + L_E \) and a high \( \frac{dI_C}{dt} \), the voltage drop of the commutation inductance \( V_{L,\text{comm}} \) is added to \( V_{DC} \), and therefore \( V_{CE,max} = V_{DC} + V_{L,\text{comm}} \).

The last period (after \( t_5 \)) of the IGBT turn-off is a tail current period, where the remaining charge carriers (holes) in the base region decay as a result of recombination. All charge carriers are swept out from the component when the MOSFET channel is removed, but some charge carriers are left on the collector side of the \( N^+ \) drift region. The only way to remove these carriers is recombination. The time of recombination is determined by the carrier lifetime, and the recombination process is seen as a tail current at the end of the IGBT turn-off. The number of carriers that have to recombine can be affected by adjusting the IGBT on-state carrier density profile. For example, at the present, common IGBT technologies such as the trench gate and the collector-side buffer layer (the field-stop layer) produce a carrier density profile where the carrier density is lower on the collector side than on the emitter side. Consequently, most of the carriers can be removed from the component through the MOSFET channel, and the duration of the tail current is reduced. An example of carrier density profiles for a planar gate, a trench gate, and a trench gate with a field-stop layer are illustrated in Figure 2-19.

![Carrier density profiles](image_url)

Figure 2-19 Carrier density profiles for different IGBT technologies. The position coordinate along the chip thickness in \( \mu m \) is presented on the x-axis and the carrier density on the y-axis (Volke et al., 2017).

In the short-circuit, the terminal capacitances affect in a similar way to the normal operation turn-on and turn-off, and thus, a similar approach can be used for short-circuit
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operation. However, as will be presented in the following section, the capacitances are operating point dependent, which has to be taken into consideration when using capacitance values from the datasheet for short-circuit modelling. Furthermore, the $V_{GE}$ waveform is very different in short-circuit operation compared with normal operation. In (Li et al., 2019), it is proposed that a Miller plateau could be used for short-circuit detection. In the short-circuit Type I, the Miller plateau vanishes almost completely because the voltage variation is so small. Furthermore, the level of the plateau is current dependent, and thus, a change in the level indicates that the current is much different from normal operation. This is especially true for example in short-circuit conditions.

2.2.6 $C_{CG}$ voltage and current dependence

The dynamic behaviour of the IGBT is determined mainly by the capacitances of the component. Different capacitances of the semiconductor structure are charged and discharged during dynamic states, and consequently, the capacitances have an effect on the voltage and current gradients in the collector, emitter, and gate terminals. The effect of the IGBT terminal capacitances is especially important in short-circuit operation, because $C_{CG}$ has a significant impact for instance on the maximum collector current $I_{C,max}$ at the beginning of a short-circuit pulse. When $V_{CE}$ is changing because of a high current collector gradient, the current is flowing through $C_{CG}$, which has an effect on the $V_{GE}$ level. Furthermore, $V_{GE}$ mainly determines $I_{C,sat}$ according to the transfer characteristics, and thus, $C_{CG}$ contributes essentially to the IGBT short-circuit behaviour.

A well-known phenomenon of IGBT capacitances is their voltage dependence, and the topic is widely discussed in the literature (e.g. (Luo et al., 2016) and (Yang et al., 2015)). In particular, the Miller capacitance $C_{CG}$ which contributes significantly to the component switching waveforms, is strongly voltage dependent, and it should not be excluded from the model of the component. However, $C_{CG}$ also depends on current. There are a few studies on the topic; for example (Yang et al., 2015), (Tominaga et al., 2011), and (Tan et al., 2017). In (Yang et al., 2015) and (Tominaga et al., 2011), it is stated that by including current dependence in the $C_{CG}$ model, the simulated $V_{CE}$ and $I_C$ waveforms correspond better with the measured waveforms in normal operation mode switching. In both studies, $C_{CG}$ is modified to achieve a better match with the experiments, but there is no experimental proof of the $C_{CG}$ value when current is flowing through the component, because it cannot be measured in practice.

Nevertheless, the effect of current correction decreases with an increasing voltage. Figure 2-20a and b present the behaviour of $C_{CG}$ as a function of voltage for a model without a current correction, and for a model with a current correction.
The theoretical background of the $C_{CG}$ current dependence is discussed in (Tominaga et al., 2011) and (Yang et al., 2015). In (Tominaga et al., 2011), the current dependence is explained as follows. The $C_{CG}$ value depends on the depletion layer capacitance $C_{dep}$ and the oxide capacitance $C_{OX}$ according to Eq. (2.33)

$$C_{CG} = \frac{C_{OX} \cdot A \cdot a_i \cdot C_{dep}}{C_{OX} \cdot A \cdot a_i + C_{dep}},$$  \hspace{2cm} (2.33)

where $C_{dep}$ is

$$C_{dep} = \frac{\varepsilon_{Si} \cdot a_i \cdot A}{W_d},$$  \hspace{2cm} (2.34)

where $\varepsilon_{Si}$ is the permittivity of silicon, $a_i$ is the ratio of the inter-cell to the total die area, $A$ is the die area, and $W_d$ is the depletion layer width.

The depletion width depends on the depletion voltage $V_d$, Eq. (2.35)

$$V_d = \frac{q \cdot N_{eff} \cdot W_d^2}{2 \cdot \varepsilon_{Si}} \rightarrow W_d = \sqrt{\frac{2 \cdot \varepsilon_{Si} \cdot V_d}{2 \cdot N_{eff}}},$$  \hspace{2cm} (2.35)

where $q$ is the elementary charge, and $N_{eff}$ is the effective doping concentration.

From Eq. (2.35) it can be seen that if $N_{eff}$ is changing, the depletion width $W_d$ can change even if the voltage remains the same. The effective doping concentration can be calculated by the hole current $I_{p2}$ and the electron current $I_{n2}$ at the emitter end of the drift region according to Eq. (2.36)
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\[ N_{\text{eff}} = N_B + \frac{I_{p2}}{q \cdot v_{\text{sat}} \cdot A} - \frac{I_{n2}}{q \cdot v_{\text{sat}} \cdot A}, \]

where \( N_B \) is the drift region doping concentration and \( v_{\text{sat}} \) is the saturated drift velocity.

\( N_{\text{eff}} \) is obviously changing as a function of current, and thus, the depletion width may change even at the same applied voltage. However, in (Tominaga et al., 2011), it is stated that a change in \( N_{\text{eff}} \) cannot completely explain the \( C_{\text{CG}} \) current dependence. In (Tominaga et al., 2011), the \( C_{\text{CG}} \) value is adjusted by comparing the experimental and simulation data and finding a correct current-dependent factor for \( C_{\text{CG}} \). Nevertheless, no additional information of the theoretical background of the current dependence is given.

In (Yang et al., 2015), the authors propose that \( C_{\text{CG}} \) is proportional to the square root of \( I_C \)

\[ C_{\text{CG}}(I_C) = K_{\text{CCG}} \cdot \sqrt{I_C} \cdot C_{\text{CG0}}, \]

where \( K_{\text{CCG}} \) is the current dependence coefficient of \( C_{\text{CG}} \) and \( C_{\text{CG0}} \) is the initial value of \( C_{\text{CG}} \).

The same approach is used for \( C_{\text{CG}} \) in Model1 of this study. An initial capacitance value \( C_{\text{CG0}} \) can be found from the datasheet, and its voltage dependence is estimated by Eq. (2.38) (Infineon, 2015)

\[ C_{\text{CG0}}(V_{\text{CE}}) = \frac{C_{\text{CG}}(V_{\text{ref}}) \cdot \sqrt{V_{\text{ref}}}}{\sqrt{V_{\text{CE}}}}, \]

where \( C_{\text{CG}}(V_{\text{ref}}) \) is the \( C_{\text{CG}} \) capacitance value at the voltage \( V_{\text{ref}} \) given in the component datasheet.

Therefore, an estimate for \( C_{\text{CG}} \) can be calculated as a function of \( V_{\text{CE}} \) and \( I_C \) with Eq. (2.39)

\[ C_{\text{CG}}(I_C, V_{\text{CE}}) = \frac{C_{\text{CG}}(V_{\text{ref}}) \cdot \sqrt{V_{\text{ref}}}}{\sqrt{V_{\text{CE}}}} \cdot K_{\text{CCG}} \cdot \sqrt{I_C}. \]

Accurate determination of \( K_{\text{CCG}} \) requires either numerical simulation where \( C_{\text{CG}} \) at different \( I_C \) values is defined with a model that takes the IGBT chip geometry and physical semiconductor parameters into account, or extensive measurement series where \( C_{\text{CG}} \) vs. \( I_C \) dependence can be extracted. Neither of these methods is reasonable in this study, as the aim is to investigate the usability of simple IGBT models, where only a few measurements are needed for characterization. However, with the methods proposed in this study, determination of \( K_{\text{CCG}} \) cannot be carried out completely without measurements. The value for the current dependence factor can be found, with
appropriate accuracy, by a trial and error method where $K_{CG}$ is adjusted so that simulated and measured results match. In this doctoral dissertation, the adjustment is done in a single operating point where the component has the smallest gate resistance values and the collector-emitter voltage gets the highest value. The adjustment can be done for each or several operating points, but then, the aim of only a few measurements is not achieved.

2.2.7 **Short-circuit operation at low $V_{CE}$ levels**

Special questions may arise when the IGBT is stressed by a short-circuit with low $V_{CE}$ levels. Even though the short-circuit pulse energy is not high in this case, a destructive mechanism can occur on the gate side of the component as was discussed in Section 2.3. One very critical phenomenon is the high-frequency $V_{GE}$ oscillation, reported for example in (Reigosa et al., 2018) and (Wu et al., 2015); a similar oscillation is also observed in the measurements of this study.

At the time of writing this dissertation, the gate voltage oscillations during a short-circuit are intensively investigated by several research groups. Uncontrolled gate voltage oscillation may cause exceeding of the maximum gate voltage, and consequently, the device may be destroyed after a very short time from the beginning of the short-circuit event. In the other short-circuit fault modes, the collector emitter voltage is desaturated before the device destruction occurs, but if the device is destroyed by exceeding of the maximum gate voltage, the destruction may happen when $V_{CE}$ has only started to desaturate. Even though the behavioural models cannot normally describe these oscillations, it is important to understand the theory and origin of the phenomenon when discussing the limitations of the models and comparing the simulation and experimental results in Section 4.4. The short-circuit protection is often based on detection of the short-circuit incident followed by a safe device turn-off within allowed short-circuit duration determined by the manufacturer (often within 10 µs for state-of-art high-power IGBTs). However, the device (or the gate driver) may suffer considerable damage at a low-voltage short-circuit even though it is turned off within an appropriate time frame.

An oscillation is triggered when the gate-side inductance and the IGBT capacitance start to resonate, and the behaviour of $C_{CG}$ has a major contribution to this phenomenon. Several studies have shown that the probability for the oscillation increases when the $V_{CE}$ level is decreased (Reigosa et al., 2018) and (Treek et al., 2018). From the perspective of short-circuit operation, low-voltage operation may be possible for example in some multilevel topologies, where the voltage across the component can be much below the rated voltage. Furthermore, in the short-circuit Type II or Type I with a large commutation inductance, the voltage across the component changes from a very low level to the DC voltage during desaturation, and consequently, this can trigger an oscillation. In the measurements of this study, a high-frequency $V_{GE}$ oscillation is observed in the DC voltage range from 200 V to 300 V. When the DC voltage is increased to 350 V, no oscillation is observed.
From the perspective of the gate side, the IGBT is a strongly capacitive component, and its capacitances are voltage dependent. Especially the collector gate capacitance $C_{CG}$ (also known as the Miller capacitance) has a strong nonlinear dependence on $V_{CE}$, and it is mentioned in many studies as the main parameter that is related to the oscillation phenomenon. Furthermore, it is also presented that the oscillation amplitude is reduced when the temperature of the component is increased (Reigosa et al., 2018) and (Treek et al., 2018). Moreover, some studies show that circuit parasitics, such as gate inductance and commutation inductance, have an effect on the oscillation. For example, different gate-side inductances of individual IGBT chips in a multichip IGBT module are given as an explanation for the oscillation (Wu et al., 2015).

However, it is not exactly clear what triggers an oscillation. Studies such as (Wu et al., 2015) and (Reigosa et al., 2019) suggest that the oscillation can be eliminated by reducing the parasitic inductance of the main circuit around the IGBT, whereas in some studies, the descent of oscillations is proposed to be a parallel connection of the IGBT chips inside the IGBT module. Nevertheless, it is not unambiguous that the oscillation is caused by a parallel connection of the IGBT chips. In (Reigosa et al., 2019) and (Reigosa et al., 2018) high-voltage IGBTs are investigated, and the study includes both planar and trench gate chip structures. These studies show that the oscillation can occur even if a single IGBT chip is stressed by a short-circuit event.

Furthermore, (Reigosa et al., 2017) and (Treek et al., 2018) report that the oscillation decays when the temperature of the component is increased. This is linked to the temperature dependence of the IGBT transconductance for example in (Wu et al., 2015). In (Reigosa et al., 2017), the charge storage effect is proposed as an explanation for the $V_{GE}$ oscillation, which also explains why an oscillation occurs more probably at lower component temperatures.
In another line of research, the oscillations are proposed to originate from the IGBT chip itself, and they can be mitigated by changing semiconductor parameters and/or the internal structure. In (Reigosa et al., 2018) and (Reigosa et al., 2019), it is presented that devices with a low bipolar gain tend to become unstable at lower $V_{CE}$ voltages, and this phenomenon is dependent on the collector side and buffer layer design. The origin of the $V_{GE}$ oscillation is stated to be a time-varying $C_{CG}$ in the short-circuit operation, which is caused by the changing electric field gradient (also known as the Kirk effect). The change in the electric field gradient causes a charge storage on the emitter side of the IGBT, which can be associated with a change in the $C_{CG}$ value. An energy change occurs between the time-varying $C_{CG}$ and the gate-side inductance $L_{G}$, which can be seen as an oscillation in the gate-emitter voltage $V_{GE}$ and the gate current $I_{G}$ as reported in (Reigosa et al., 2018). The collector current can be assumed to be constant at a short-circuit when oscillations are investigated. The relation between the collector current density $J_{n}$, the electron velocity $v_{n}$, and the electron density $n$ is written as follows

$$J_{n} = q \cdot n \cdot v_{n},$$  \hspace{1cm} (2.40)

where $q$ is the elementary charge. $v_{n}$ is determined by the electric field strength $E$, and thus, if $E$ is lowered, $n$ should be increased so that a constant $J_{n}$ is maintained. Consequently, the electron density increases on the emitter side of the IGBT when the gradient of the electric field strength changes during a short-circuit as a result of the Kirk effect. As described in (Baliga, 2019), the current density that causes a change in the electric field gradient (Kirk current density) is smaller at lower $V_{CE}$ levels, and thus, the probability of a change in the electric field gradient and a high-frequency oscillation is increased at low $V_{CE}$ levels, which explains why the $V_{GE}$ oscillation is dependent on the voltage level.

From the viewpoint of reliability, it is important to prevent operation under a high-amplitude gate voltage oscillation, because it can damage the gate oxide, and thereby...
2.3 IGBT short-circuit failure modes

The classical way to categorize IGBT short-circuit failure modes in the short-circuit Type I was presented in Section 1.2.1. However, if the investigation is extended to include the short-circuit Type I with a large commutation inductance and modern IGBT chip technologies, such as trench gate and field-stop (FS) structures, the number of failure modes is increased from four. If also gate-side failures are considered, the number of short-circuit failure modes becomes eight as presented in (Chen et al., 2018). The categorization of the short-circuit failure modes is as follows (the categorization is modified from the categorization presented in (Chen et al., 2018)):

**Transient failure modes**

1. Turn-off failure during the desaturation process
2. Peak current failure
3. Self-turn-off failure
4. Short-circuit pulse failure initiated by the MOSFET mode
5. Turn-off failure during a steady state

**Failures related to the short-circuit pulse duration**

6. Thermal runaway failure during a steady state
7. Thermal runaway failure during a blocking state

**Gate-side failures**

8. Gate oscillation failure

Sometimes, some of the failure modes are linked to the short-circuit Type II, because the failure is triggered during the $V_{CE}$ desaturation. Normally, $V_{CE}$ is always close to $V_{DC}$ in the short-circuit Type I, and consequently, desaturation does not occur, but if the short-circuit Type I occurs in a circuit with a large commutation inductance, the behaviour is similar to the short-circuit Type II. Therefore, it is relevant to consider here all the eight failure modes even though this study concentrates on the short-circuit Type I.

Traditionally, the component manufacturer determines the component short-circuit safe-operation-area (SCSOA) for a specific maximum short-circuit withstand time $t_{SC,max}$, which is commonly 10 µs; however, this time is being reduced because of the reduced chip thickness in novel chip technologies. The maximum short-circuit duration $t_{SC,max}$ determined in the datasheet specifies the component short-circuit ruggedness from the perspective of chip temperature. During a short-circuit, a high current and voltage are...
simultaneously in effect, which causes extremely high losses in the chip, and consequently, a rapid elevation in temperature. If the temperature exceeds the critical temperature of the semiconductor material, the controllability of the component is lost when the component voltage blocking capability deteriorates. The temperature elevation is directly linked to the short-circuit pulse length, and if $t_{SC,max}$ and the SCOSA boundaries are not exceeded, the manufacturer promises that the component temperature does not exceed the critical temperature. Failure modes 6 and 7 are initiated if the chip temperature reaches the critical temperature.

However, even if the short-circuit pulse length is shorter than $t_{SC,max}$, the component may fail under some specific conditions because of transient failure modes, in other words, a failure can occur while the short-circuit energy $E_{SC}$ is very low. The failure modes 1–5 include the group of transient failure modes.

In the categorization of this study, the failure mode 8, gate voltage oscillation, has a category of its own. For instance, in (Chen et al., 2018), it is included in the transient failure modes, but as it is caused by the interaction of the chip gate side and the external gate circuitry, it is here separated into a category of its own.

Figure 2-23 presents idealized collector current and collector-emitter voltage waveforms during the short-circuit Type II or Type I with a large commutation inductance. The instance of a particular failure mode is indicated by the corresponding number.

![Figure 2-23 IGBT failure mode locations in the $I_C$–$V_{CE}$ short-circuit waveforms (Chen et al., 2018).](image)

**Turn-off failure during the desaturation process**

An IGBT turn-off failure may occur if the short-circuit turn off is initiated during the $V_{CE}$ desaturation process. This failure mode is linked to the latching up of the parasitic thyristor structure inside the IGBT, and because it occurs in a highly dynamic operating point, it is also called a dynamic latch-up failure. The phenomenon of a thyristor latch-up is very similar to the peak current failure, but in this case, the failure occurs before $I_{SC,max}$,
2.3 IGBT short-circuit failure modes

and $V_{CE}$ is still in the desaturation phase without reaching $V_{DC}$. In (Bhalla et al., 1998), it is proposed that the ratio between the hole and electron currents under the IGBT gate side is more equal when $V_{CE}$ reaches $V_{DC}$ after the desaturation phase, whereas if a short-circuit turn-off is initiated during the desaturation phase, the electron current decreases, and consequently, the hole current increases rapidly. A high hole current at the $P^+$ base may trigger the parasitic thyristor structure, thereby causing a turn-off failure during the desaturation phase. The turn-off failure during the desaturation process is explained in detail in (Bhalla et al., 1998) and (Chen et al., 2018).

**Peak current failure**

As the name of the failure suggests, this failure mode is triggered at the maximum short-circuit current or very close to it. The origin of the peak current failure is a latch-up of the internal parasitic thyristor structure. In principle, the IGBT structure includes a pnp/npn transistor structure as shown in equivalent circuit in Figure 2-24. The large N drift region acts as a base for the pnp transistor, and the deep p type layer on the emitter side acts a base for the npn transistor. If $I_{SC}$ is high enough, it can cause a voltage drop across the deep p-type layer, which produces enough current to turn the parasitic npn transistor on. This latches the parasitic thyristor structure, and the current through the device is no longer controlled by the MOSFET channel.

![Figure 2-24 Equivalent circuit IGBT presenting internal parasitic thyristor structure](image)

The improvements in the cell structure in the modern IGBT technologies have significantly reduced the probability of a peak current failure, and thus, this failure mode is no longer of great importance (Muller et al., 2005). However, under certain circumstances, current filamentation can cause a device latch-up if the short-circuit is turned off with too high a current as presented in (Toechterle et al., 2014).

**Self-turn-off failure**

In a self-turn-off (STO) failure, the IGBT starts to turn off during the $V_{CE}$ desaturation process without an actual turn-off signal to the component gate side. As this failure mode is related to the $V_{CE}$ desaturation, it may occur during the short-circuit Type II or Type I
with a large commutation inductance, and as presented in (Lutz and Basler, 2012), the STO failure is more pronounced with high-voltage IGBTs. In the STO failure, the $V_{CE}$ desaturation process leads to a positive gate current, which, as a result of the negative differential Miller capacitance, discharges the gate and reduces the gate-emitter voltage. If the reduction is great enough, the IGBT turns off even though the gate driver output is driven to the on-state. In normal cases, the current through the Miller capacitance $i_{CCG}$ is positive while $dV_{CE}/dt$ is positive, and it charges a gate, thereby increasing $V_{GE}$. However, under some circumstances, $i_{CCG}$ may become negative with positive $dV_{CE}/dt$ values, which leads to a decreasing $V_{GE}$, and if the decrease is large enough, to a self-turn-off and an STO failure. This negative $i_{CCG}$ with a positive $dV_{CE}/dt$ is called the negative differential Miller capacitance, and it is discussed in detail in (Böhmer et al., 2011).

Figure 2-25 presents the measured voltage and current waveforms from the IGBT STO failure during the short-circuit Type II. It is clearly seen that the sign of the gate current $i_G$ changes even if $dV_{CE}/dt$ remains positive, which indicates a change also in $i_{CCG}$.

![Figure 2-25 IGBT STO failure during the short-circuit Type II (Lutz and Basler, 2012).](image)

**Short-circuit pulse failure initiated by the MOSFET mode**

This failure mode is linked to the current filamentation on the collector side of the IGBT as presented in (Kopta et al., 2009). The root cause for the component to fail in this failure mode is the excessive local temperature inside the component, but it can occur without exceeding of the critical short-circuit pulse energy $E_c$. It is shown in (Kopta et al., 2009) that the current through the component can form filaments close to the collector side of the N drift region. This filamentation process is more likely to happen at lower voltages than at higher voltages, as shown in Figure 2-26, where this failure mode is simulated for a 3.3 kV IGBT.
2.3 IGBT short-circuit failure modes

The filamentation process is triggered by a lateral electron current flow caused by lateral potential differences inside the component. Possible potential differences can be caused for instance by deviations in the chip manufacturing process.

Turn-off failure during the steady state

During the short-circuit turn-off, a very high amplitude in $V_{CE}$ can occur as a result of $di_C/dt$ and the parasitic inductance of the electric circuit. If this voltage spike exceeds the maximum voltage rating of the IGBT, the component can experience a turn-off failure during a steady state. The root cause of this failure mode is an emitter-side avalanche as presented in (Baburske et al., 2016). The amplitude of the voltage spike is directly linked to the turn-off $di_C/dt$ and the circuit parasitic inductance $L_\alpha$, and therefore, a low $L_\alpha$ and a low $di_C/dt$ reduce the risk to confront this failure mode. However, (Benmansour et al., 2007) suggests that if the temperature of the IGBT chip is high enough at the beginning of the turn-off, also a thermal runaway can cause the component failure during a steady-state short-circuit turn-off.

Thermal runaway failure during the steady state

As a result of a simultaneously affecting high current and high voltage, extremely high-power losses are generated inside the switching device during a short-circuit, which causes a rapid chip temperature increase. If the short-circuit is not switched off on time, the temperature may exceed the critical temperature at which the device loses its voltage blocking capability as a result of changes in the semiconductor material behaviour. The manufacturer usually determines the maximum short-circuit withstand time $t_{SC,max}$ for the component in the component datasheet. $t_{SC,max}$ is determined under certain operating conditions, such as $V_{DC}$ and the chip junction temperature at the beginning of the short-circuit. If the short-circuit is turned off before $t_{SC,max}$, the chip temperature should not exceed the critical temperature, and the device survives from the short-circuit without destruction. The temperature increase during a short-circuit is directly linked to the chip
Thermal capacity. Low-voltage (< 1.7 kV) IGBT chips have a much smaller chip thickness and thereby a smaller thermal capacity than high-voltage chips, and thus, the thermal runaway failure is more common for low-voltage IGBTs than for high-voltage IGBTs. The thermal runaway failure mode during a steady state is investigated for example in (Trivedi and Shenai, 1998).

Thermal runaway failure during the blocking state

A thermal runaway failure may also occur after a successful short-circuit turn off. In this case, it is called a thermal runaway failure during the blocking state. In most of the applications there is no effective heat transfer path on the top of the component, and thus, its temperature during a short-circuit is higher than on the bottom side of the component, which is normally connected to a cooling element. After a successful short-circuit turn-off, the temperature of the bottom side (IGBT collector side) starts to rise as a result of heat diffusion, which causes an increase in the leakage current. The leakage current with a combination of a high blocking voltage generates further power losses inside the component, and consequently, the chip temperature rises. In some scenarios, this forms a self-amplifying loop, and eventually, the device runs into a thermal runaway and fails during the blocking state. An increase in the leakage current has a positive feedback from the increasing chip temperature, and the IGBT collector-side properties have a significant effect on this feedback loop. By changing the IGBT collector-side properties, the temperature dependence of the current gain, which mainly determines the leakage current, can be made negative, thereby reducing the probability of a blocking state thermal runaway (Voss et al., 2010), (Schulze et al., 2011). The thermal runaway failure mode during the blocking state is investigated for example in (Otsuki et al., 2003).

Gate oscillation failure

In addition to the failure modes listed above, an IGBT may fail during a short-circuit also by the gate oxide breakdown caused by an excessive gate voltage. A common reason for an excessive gate voltage is a gate voltage oscillation initiated by a resonance between the IGBT capacitive gate, the inductance of the gate leads, and the gate resistance. This failure mode can also be considered to belong to the group of transient failure modes, because a gate oscillation may destroy the device without exceeding of the critical maximum temperature of the IGBT chip.

The gate voltage oscillation in short-circuit conditions has been studied extensively in the literature, and many publications propose that the oscillation phenomenon is linked to the negative differential Miller capacitance (Ronsisvalle et al., 2013) and (Milady et al., 2009). Because the Miller capacitance has a voltage-dependent behaviour, triggering of an oscillation usually takes place in the short-circuit phase where the $V_{CE}$ voltage changes, and thus, in the short-circuit Type II or Type I with a large commutation inductance. (Abbate et al., 2015) reports that low- and high-frequency oscillations may occur during an IGBT short-circuit, but from the perspective of a gate oscillation failure, the high-frequency region is more critical, because in that region the required gate inductance for
the oscillatory conditions is smaller, in the range of gate inductances in practical applications. Furthermore, (Abbate et al., 2015) presents a stability map for gate oscillations, where stable and instable regions are determined as a function of gate inductance and resistance. It is also stated that the stability map changes as a function of collector-emitter voltage and short-circuit load conditions. The gate oscillation dependence on operating point conditions, such as $V_{DC}$ and the chip temperature, is reported in many studies, and for example (Reigosa et al., 2017) suggests that an oscillation probably occurs at a low $V_{DC}$ and a low temperature, where the device input capacitance is more likely to show a varying behaviour. The theoretical background of the input capacitance variation is given in (Reigosa et al., 2018), where it is stated that the variation occurs according to the strength of the electric field close to the emitter of the device.

2.4 IGBT modelling methods

Semiconductor behaviour can be modelled in various ways depending on the requirements set for the model. For example, a person working at the research and development department of a semiconductor component manufacturer may have dissimilar requirements for the component model to a person who is doing development work related to power converters, even though they may have to model the very same component. Often, the major requirements are related to the model accuracy, simulation speed, implementation, and parameter extraction.

Naturally, a high accuracy is desirable for all methods, but a higher accuracy often leads to increased complexity. For instance, if the main target of the modelling is to determine the power losses of the component, it suffices to correctly model the current through the component and the voltage across it. In this case, for example, the gate voltage and the divided electron and hole currents inside the component are not so relevant, and it is not necessary to model them accurately. Alternatively, if the main objective is to improve the component behaviour itself, the physical phenomena inside the component have to be modelled, and a more complex modelling method has to be chosen. Of course, if the component internal phenomena are modelled correctly, also the voltages and currents in the main connectors are correct.

Simulation speed may be a critical factor if an extensive system is modelled. It is not practical to use a detailed and accurate numerical component model for instance in a simulation intended for analysing the generator drive operations of a wind farm, which may include tens or hundreds of inverters and thousands of semiconductor switching components. Vice versa, if the purpose is to investigate a single switching event in a simple commutation circuit, the simulation speed may not be so crucial.

In general, IGBT modelling methods can be divided into three main categories; behavioural methods, analytical methods, and numerical methods, all having benefits and drawbacks of their own. Behavioural models describe the component behaviour without taking into account the component internal physics. Behavioural models can often be
optimized to a certain operating point, but the model accuracy decreases when the operating point is changed from the optimized one. Behavioural models are investigated in this study, and a broader survey of them will be presented in Section 2.5.

In the analytical methods, the component behaviour is described by using mathematical equations that are based on the device physics. Analytical methods are commonly employed, and analytical component analysis is discussed extensively in the literature.

Because modern semiconductor components have a relatively complex structure, the solution of an analytical method has to be simplified in most of the cases. For example, the problem can be solved as one-dimensional even though it is multidimensional in reality. An analytical component model is often composed by using discrete components, whose behaviour can be described by straightforward analytical equations. For instance, the IGBT behaviour can be described analytically by using an equivalent circuit that includes a series connection of the PiN diode and the MOS transistor or a cascade connection of the BJT and the MOSFET as shown in Section 2.2. It is possible to achieve very accurate results with analytical models, but the drawback is that very detailed information is needed about the semiconductor properties. Challenges related to the analytical modelling of the IGBT are discussed for instance in (Baliga, 2013).

In many cases, numerical methods can be said to be the most accurate modelling methods of semiconductor devices, as the use of a numerical method enables investigation of the phenomena inside the semiconductor material. The basic principle of the numerical methods is to compose a device model in one, two, or three dimensions and then divide the model into smaller elements and solve the required problem within these elements under particular boundary conditions. As computational power is nowadays easily available, also complex structures can be solved in two or three dimensions.

Generally speaking, numerical methods can be used to get an approximate solution for a mathematical problem that cannot be solved analytically, or an analytical solution is not reasonable. Numerical methods can be used to solve for example differential equations or partial differential equations. In the IGBT case, these methods can be used for example to solve an ambipolar diffusion equation that determines the excess carrier distribution of the drift region (Bryant et al., 2007). At the present, various technical CAD (TCAD) software are popular for semiconductor numerical modelling.

The benefit of numerical methods is that accurate solutions for complex problems can be achieved if the problem and boundaries are correctly defined. However, if numerical methods are used to investigate a semiconductor component, detailed information of the component dimensions, such as layer thicknesses and channel lengths, and physical semiconductor material properties, such as doping concentrations and carrier lifetimes, is needed. This is a drawback compared for example with behavioural models. In addition, accurate numerical solutions may take a long time to compute if the problem or the structure is complex. Nevertheless, these methods are very advantageous in semiconductor device studies that concentrate on investigating the component itself and
2.4 IGBT modelling methods

for instance the effects of structural changes on the component behaviour. When larger electrical systems are investigated, numerical methods are not often practical because of the high computational power requirement.

Analytical and numerical modelling methods are, however, not in the scope of this study. Thus, the following sections focus on behavioural modelling methods and the literature survey of behavioural models.

2.4.1 Behavioural modelling method

The basic characteristics of an IGBT from the perspective of the main connector are presented in (Sheng et al., 2000), which divides the IGBT output characteristics into three states: the blocking, linear, and current saturation state, as also discussed in previous sections of this study. These states are presented in Figure 2-27 (regions I–III). From the modelling perspective, regions II and III are, in most cases, the regions of interest. As presented by Eq. (2.2) in Section 2.2.1, the IGBT on-state voltage is composed of three voltage components. These components are the junction voltage \( V_{P-N} \), the conductivity-modulated base voltage \( V_{\text{drift}} \), and the voltage of the MOS-channel \( V_{\text{MOSFET}} \). In the case of an NPT-IGBT, \( V_{P-N} \) is the voltage of the collector-side P-N junction, but in the case of a PT-IGBT, also the buffer-base junction voltage should be taken into account. As a power switch, the normal operating region of the conducting IGBT is in the linear region (region II). Modelling of this region is important for example in the on-state loss calculation. In the linear region, the total on-state voltage is dominated by \( V_{\text{drift}} \), and its correct determination requires calculation of the excess carrier distribution and the conductivity modulation of the region. Furthermore, complex IGBT structures, such as the trench gate IGBT (TIGBT), may require modelling of the 2D effects. According to (Sheng et al., 2000), the parameters needed for the exact modelling of \( V_{\text{drift}} \) are the carrier distribution, the mobility of carriers (including carrier–carrier scattering), and the bandgap narrowing effect in the heavily doped collector.

![Figure 2-27 IGBT output characteristics as a function of gate-emitter voltage and different operating regions. Off-state (region I), linear region (region II), and current saturation region (region III) (Sheng et al., 2000).](image)

\[ V_{CE} \text{ [V]} \]
\[ I_c \text{ [A/mm}^2\text{]} \]

region I region II region III
In order to correctly calculate the IGBT on-state voltage in the current saturation mode (region III in Figure 2-27), a major effort has to be put to the modelling of the MOS-channel effects. The MOS-channel has a significant contribution also in region II, but in region III it has the largest effect on the total on-state voltage. In principle, two parameters define the MOS-channel voltage $V_{\text{MOSFET}}$. These are the channel transconductance $g_m$, which basically describes the component gain, and the threshold voltage $V_{\text{TH}}$. As presented in the previous section, the transconductance at current saturation can be calculated by Eq. (2.12).

### 2.4.2 Behavioural models

As the name indicates, the behavioural models aim at only describing the device behaviour without taking the physics into account in detail. In many cases, these models are composed of simple circuit elements, such as passive elements and current/voltage sources, and possibly semiconductor component models that are included in the circuit simulator software. In addition, one common characteristic of behavioural models is that they do not need detailed information about component physical parameters, such as structural dimensions and semiconductor material properties, which is the case with numerical or analytical models.

Owing to a lack of a physical base, behavioural models can seldom give accurate results in a wide operating point range. However, by proper characterization, a behavioural model can describe the device behaviour accurately within a limited range. In general, the characterization is carried out by applying information from datasheets and/or by extracting relevant parameters from experimental results. The generally available component information is often limited to the normal operating point region, and thus, it is necessary to apply for example some curve fitting method to extend the region for which the model can be characterized. Further, operating-point-dependent parameter variation can be implemented into the model by applying look-up tables.

Typically, behavioural models exploit a simplified equivalent circuit as a basis for the model. One of the simplest forms of IGBT models is a series connection of a controlled ideal switch, a voltage source (or diode), and a resistor. This model is suitable for analysing steady-state operation, but it does not give any information about the dynamics in transient states.

A straightforward way to describe also transient states is to compose the model of a controlled current source that provides the current through the component and add relevant capacitances across it (Figure 2-28a). The accuracy in the transients can be improved if the non-linearities of the capacitances are taken into account. The accuracy of the steady-state operation is defined by the current source implementation and how it generates the component current in different operating points. In a very basic form, the collector current is determined by the transconductance and the gate voltage as $I_c = g_m(V_{\text{GE}} - V_{\text{TH}})$. A model of this kind is presented for example in (Jin and Weiming, 2006).
2.4 IGBT modelling methods

![Figure 2-28 Examples of equivalent circuits of behavioural models. a) Simple model with fixed capacitances and b) more complex model with variable capacitances and a tail current description.](image)

Yet another, slightly more complex structure of a behavioural model is presented in (Wintrich et al., 2011). In this model, the steady-state characteristics are implemented by separating the saturation mode and transfer characteristics. Diode D1 in Figure 2-28b describes the saturation as the voltage drop across it is varied as a function of collector current. The transfer characteristics are carried out by a parallel connection of the controlled current source and diode D2. The current source is controlled by the applied gate voltage. The transient behaviour is governed by charging and discharging of the capacitances between the terminals. In particular, the gate-collector capacitance $C_{CG}$, which varies as a function of the gate-collector voltage $V_{CG}$, has a significant effect on the transient behaviour. $C_{tail}$ and $R_{tail}$ are used to describe the current tail at the IGBT turn-off.

From the perspective of the IGBT short-circuit modelling, the main issues to be modelled at the component level are the steady-state short-circuit current and the current gradients during the short-circuit turn-on and turn-off. Basically, this requires knowledge of the IGBT transfer characteristics and the component capacitances, and commonly, this information is given in the component datasheets. In addition, as presented in Sections 2.2.3–2.2.5, there are various complex phenomena in the IGBT short-circuit that have to be considered to achieve accurate modelling results. Information about the self-heating effect or the $C_{CG}$ voltage/current dependence of components cannot be easily found in publicly available material. Nevertheless, some simplified estimation methods can be used to model these phenomena, as will be shown in Section 3.

To sum up, behavioural models can be constructed to describe the component behaviour accurately within a limited operating point range. However, it is difficult to construct a
model that describes all the device features. Instead, the required features should be selected according to the requirements set for the model.

2.5 Literature survey of behavioural IGBT models

In the literature, a wide array of IGBT models have been presented.

An extensive list of IGBT models developed before year 2000 is presented in (Sheng et al., 2000). In the review, the models are divided into four classes according to their basic principles: mathematical models, semimathematical models, behavioural models, and seminumerical models. Furthermore, the models are classified according to their complexity.

In addition to (Sheng et al., 2000), a couple of other reviews of IGBT and semiconductor modelling have been presented in the literature after the year 2000. The basic principles of physics-based compact models are presented in (Bryant et al., 2007). The paper discusses unipolar component models, such as MOSFETs and Schottky diodes, and bipolar component models, such as IGBTs and PiN diodes. According to the paper, the operation of bipolar components can be described by solving ambipolar diffusion equations (ADE) in a lightly doped drift region. The ADEs can be solved by many different methods, but all of them are based on transformation of the ADEs into ordinary differential equations (ODE). Furthermore, some methods to model the components that use silicon carbide (SiC) as a semiconductor material are presented in the study.

A brief review of the history of semiconductor modelling is given in (Ohashi and Omura, 2013). It also discusses how a comprehensive modelling of semiconductor components could improve the design process of power electronic devices.

Because the focus of this study is on behavioural models, only models of this type are discussed in the following section. Furthermore, the models are investigated especially from the perspective of short-circuit behaviour. Table 2-1 presents all the behavioural models that are included in the literature survey, also providing information on whether the model can describe current saturation or the full short-circuit operating region. As (Sheng et al., 2000) concerns the time period before year 2000, this survey concentrates on later publications and covers years from 2000 to 2020.

2.5.1 Behavioural models presented in the literature

Basically, behavioural models are simple and focus on describing only a couple of significant issues in the operation of the component. One very simple model is presented in (Tichenor et al., 2000), where the equivalent circuit of the device includes only five circuit components. The objective of this model is to describe the device high-frequency effects and oscillations in transients. Even though the method models different switching times as a function of gate drive conditions, the gate driver or the control itself is not modelled.
Another study that concentrates on EMI issues is reported in (Jin and Weiming, 2006). The model is based on a controlled current source with added component capacitances. The current and voltage waveforms in transients are assumed to be piecewise linear.

EMI issues are also investigated in (Zhu et al., 2012), where the IGBT is described only by a variable resistance and capacitance and a fixed inductance. All parameters for this model can be derived from the datasheet.

(Zhang et al., 2014) also investigates EMI modelling. In this case, a switching event is divided into sections, which all have capacitance values of their own. Depending on the operating point, a correct capacitance is connected to the equivalent circuit.

The built-in behavioural model of the Saber software is modified in (Zhang et al., 2000), where the behaviour of the model saturation region is improved by introducing an “early voltage” term. With this term, the collector current slightly increases as a function of $V_{CE}$ in the saturation region. An extraction tool for the model characterization is also presented in the paper.

(Charfi et al., 2002) proposes two methods to describe the IGBT behaviour in the saturation region. The first method is developed from the IGBT model included in Simulink, and the second uses the state flow method to describe the component. The focus of the study is on describing the investigated component behaviour in the off-state, linear region, saturation region, and breakdown.

In (Ammous et al., 2003), an averaged switch model is presented for inverter simulations. The switch model in the study includes the most important nonlinear effects, but the main objective of the model is to estimate for example component power losses. Furthermore, by applying this loss information, the junction temperature of the component can be approximated by a suitable thermal model.

Behavioural modelling methods also include some exceptional modelling approaches. One example is reported in (Consoli et al., 2004), which proposes a model where the steady- and transient-state models are separated, and a neural network is used in the parameter extraction. The model takes temperature effects into account, and general datasheet information and simple experimental tests added with the die size are needed for the characterization.

Simple parameter extraction is also desired of behavioural models. The behavioural model presented in (Oh and El Nokali, 2001) requires an accurately characterized Hefner model to define the parameters for the transient part of the model. To tackle this issue, (Kang et al., 2004) suggests a Matlab-based extraction method for the model proposed by Oh without a need for the Hefner model parameters. Another model based on Oh’s model and the Hammerstein configuration is introduced in (Asparuhova and Grigorova, 2006). In (Asparuhova and Grigorova, 2008) the operation in the saturation region is improved.
compared with the previously presented model; in this model, $I_C$ is slightly increasing as a function of $V_{CE}$ also in the saturation.

(Elwarraki and Sabir, 2007) proposes an electrothermal behavioural IGBT model composed of a SPICE-based MOSFET part and a separated BJT part. The paper provides details of the calculation, but the simulation results are not verified against experiments.

A very simple model characterized by applying a curve fitting method is presented in (Baraia et al., 2008). The paper shows quite simple methods to derive static-state parameters for the model from the output and transfer characteristics. The modelling of the dynamic states relies on the capacitance modelling, and extraction of the capacitance values is also discussed in detail. The whole model can be parametrized by using datasheet values and some measurements. Another curve-fitting-based method is reported in (Yi et al., 2009). This method calculates the transient state collector current as a function of $V_{GE}$ and two fitting parameters. Furthermore, $V_{GE}$ is calculated by using the input capacitance and the gate-side resistance and inductance. The static-state collector current only depends on $V_{CE}$, and $V_{GE}$ is assumed constant.

Some studies focus on enhancing the built-in component models of simulation software. (Rosu et al., 2008) applies the Ansys Simplorer IGBT model to describe the loss and temperature behaviour of the switch device. The electrical part of the model can be characterized by using an automated characterization tool that requires datasheet values as an input. The paper introduces an experiment-based method that can be used to interpolate and extrapolate datasheet values for different operating points and thereby extend the usable operating point range of the model. A Simplorer model is applied also in (Liu et al., 2012), which investigates the inverter behaviour in an electric vehicle application.

In (Mijlad et al., 2015), a Simulink-implemented behavioural model is presented. The model describes basic switching waveforms, but the results are not validated with experiments. The structure of the model is relatively simple, and it is constructed by using the blocks of the SimScape toolbox. The model is further investigated in (Mijlad et al., 2019), which reports simulation results as a function of several operating point parameters. The model is validated by comparing the output and transfer characteristics from the simulation and the datasheet.

A behavioural IGBT model is used to investigate a high-voltage IGBT series connection and voltage share in (Sang et al., 2014). The study models $C_{CG}$ as a piecewise linear capacitance with two constant values to model the switching event. A lot of effort is put to modelling of the tail current, because it has a significant effect on the voltage share at the end of the switching event. A good correspondence between simulations and measurements is achieved, even though the tail current modelling requires experimental verification.
An Ansly Simplorer IGBT model is used for transient state power loss estimation in (Oustad et al., 2016). The study concentrates on power losses in the normal operation range, not in the short-circuit. The results show that with initial characterization applying datasheet information, the model does not give accurate results, and therefore, the characterization is improved with information from additional measurements. However, the study does not discuss the commutation circuit inductance modelling, which has a significant influence on the IGBT switching behaviour.

In (Li et al., 2017), a behavioural IGBT model for predicting turn-on and turn-off losses of the component is composed by applying Shichman–Hodges equations for the MOSFET part and a simplified Ebers–Moll model for the BJT part. The proposed model shows quite good results in normal operation, but it is required that some of the model parameters are fitted against measured current and voltage waveforms, while most of the parameters can be characterized by datasheet values or simple experiments. For example, fitting of the current share between the MOSFET part and the BJT part and the output characteristics with higher $V_{CE}$ voltages is carried out with measured current and voltage waveforms.

Another model for IGBT loss estimation is presented in (Xu et al., 2018). In this case, the model is based on a switching loss look-up table and separated on-line and off-line simulation models. The model can be characterized with datasheet information. Power loss estimation gives quite reasonable results, but the simulated current and voltage waveforms do not match precisely with the experimental results. Especially, the simulated $V_{CE}$ waveform at the turn-off shows inaccurate results, and thus, it cannot be used to estimate for example a $V_{CE}$ spike during an inductive load turn-off. Current saturation operation is not discussed in the paper.

A Thevenin’s equivalent circuit for the IGBT and its antiparallel diode is presented in (Zhang et al., 2018). Depending on the control state, the model uses parameters of the IGBT or the diode to describe the component operation. According to the paper, the proposed model is fast to simulate, as both the components (IGBT and diode) are implemented into one model. The results are compared with a Matlab model, but they are not validated against measurements. The paper does not discuss the applicability of the model to current saturation modelling.

A detailed description of a behavioural IGBT model implemented to the FPGA is given in (Bai et al., 2019). The modelling method is based on separation of the IGBT steady state and the dynamic state, thus achieving a more suitable solution to on-line simulation for example in HIL systems. The results of the proposed method show a good agreement with the off-line simulation method implemented with the Saber model. The results are not compared with measurements, and the paper does not include any discussion about the current saturation mode operation.

In (Hanini and Ayadi, 2019) a Pspice model is used to model an IGBT/diode chopper circuit, and the results are validated with measurements. However, the paper does not
propose a method to model the IGBT or the diode, but it is based on methods presented in previous publications. Furthermore, no information about the characterization of the model is given.

The model developed in this doctoral dissertation is based on the model presented in (Denz et al., 2014). In the study, a behavioural IGBT model is implemented into the Modelica software. In the proposed method, the static operation of the IGBT is carried out with a current-controlled voltage source that implements the component output characteristics, and a voltage-controlled current source that implements the component transfer characteristics. The dynamic operation is performed by applying terminal capacitances $C_{GE}$, $C_{CG}$, and $C_{CE}$ in the static model. In (Denz et al., 2014), the model is not validated with measurements. However, the structure of the model is very simple, and with some added features it is applicable to modelling of short-circuit operation.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Characterization</th>
<th>Current saturation</th>
<th>Full SC operation</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Tichenor et al., 2000)</td>
<td>with measurements</td>
<td>no</td>
<td>no</td>
<td>A behavioural IGBT model to describe switching transients. Describes current saturation and its voltage dependence. Applies Early voltage, which does not describe the $I_{C,sat}$ voltage dependence correctly for modern IGBT technologies.</td>
</tr>
<tr>
<td>(Zhang et al., 2000)</td>
<td>datasheet and tuning with measurements</td>
<td>yes</td>
<td>(yes)</td>
<td>The model is validated in normal operation. Current saturation is mentioned as a topic of future work.</td>
</tr>
<tr>
<td>(Charfi et al., 2002)</td>
<td>not known</td>
<td>yes</td>
<td>no</td>
<td>An average IGBT model to simulate e.g. power losses and junction temperature.</td>
</tr>
<tr>
<td>(Ammous et al., 2003)</td>
<td>not known</td>
<td>no</td>
<td>no</td>
<td>A behavioural model with neural network characterization. Separated static and dynamic blocks in the model. Characterization procedure for an existing IGBT model.</td>
</tr>
<tr>
<td>(Consoli et al., 2004)</td>
<td>measurements and neural network</td>
<td>yes</td>
<td>no</td>
<td>An IGBT model based on the model in (Oh and El Nokali, 2001). Describes current saturation but not its voltage dependence.</td>
</tr>
<tr>
<td>(Kang et al., 2004)</td>
<td>with measurements optimized by Matlab algorithm</td>
<td>no</td>
<td>no</td>
<td>An IGBT model based on piecewise linearization for investigation of EMI issues.</td>
</tr>
<tr>
<td>(Asparuhova and Grigorova, 2006)</td>
<td>datasheet values with optimization</td>
<td>yes</td>
<td>no</td>
<td>An IGBT model that separates MOSFET and BJT parts. Based</td>
</tr>
</tbody>
</table>
2.5 Literature survey of behavioural IGBT models

<table>
<thead>
<tr>
<th>Reference</th>
<th>Data Source</th>
<th>Validation</th>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Ibrahim et al., 2007)</td>
<td>datasheet and measurements</td>
<td>yes (yes)</td>
<td></td>
<td>on a direct assumption that 90% of the IGBT total collector current is flowing through the MOSFET part. An electrothermal IGBT model implemented to Simplorer by using VHDL AMS. Only channel temperature is investigated in short-circuit operation.</td>
</tr>
<tr>
<td>(Asparuhova and Grigorova, 2008)</td>
<td>datasheet values with optimization</td>
<td>yes no</td>
<td></td>
<td>The saturation region operation is improved by adding $I_{C_{sat}}$ voltage dependence compared with the previously presented model in (Asparuhova and Grigorova, 2006).</td>
</tr>
<tr>
<td>(Baraia et al., 2008)</td>
<td>datasheet with measurements</td>
<td>yes no</td>
<td></td>
<td>A curve fitting behavioural model parametrized by experiments.</td>
</tr>
<tr>
<td>(Rosu et al., 2008)</td>
<td>datasheet</td>
<td>yes no</td>
<td></td>
<td>An averaged IGBT model from Ansoft. Used to simulate switching and conduction losses in the normal operating range. An Alonso model with improved transient state behaviour and an added diode model. Only simulation results presented.</td>
</tr>
<tr>
<td>(Michel et al., 2009)</td>
<td>datasheet</td>
<td>yes no</td>
<td></td>
<td>A simple behavioural model for a multi-chip IGBT module. Includes a couple of fitting parameters that are adjusted with experimental results. A Simplorer model used to simulate IGBT losses. The model is a part of larger system-level electric vehicle inverter model.</td>
</tr>
<tr>
<td>(Yi et al., 2009)</td>
<td>datasheet with measurements</td>
<td>yes no</td>
<td></td>
<td>A simple IGBT model that consists only of a variable resistor/capacitor and a fixed inductance used for EMI investigation.</td>
</tr>
<tr>
<td>(Liu et al., 2012)</td>
<td>datasheet</td>
<td>yes no</td>
<td></td>
<td>An IGBT model for EMI investigation based on different capacitances for different stages at switching.</td>
</tr>
<tr>
<td>(Zhu et al., 2012)</td>
<td>datasheet with measurements</td>
<td>no no</td>
<td></td>
<td>An HV IGBT series connection investigation with a behavioural model. Concentrates on tail current modelling.</td>
</tr>
<tr>
<td>(Zhang et al., 2014)</td>
<td>measurements</td>
<td>no no</td>
<td></td>
<td>The paper presents behavioural models for diode, MOSFET,</td>
</tr>
<tr>
<td>(Sang et al., 2014)</td>
<td>measurement</td>
<td>yes no</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2 IGBT short-circuit behaviour and modelling methods

<table>
<thead>
<tr>
<th>Reference</th>
<th>Type of Data Used</th>
<th>Including Datasheet</th>
<th>Including Measurements</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Mijlad et al., 2015)</td>
<td>datasheet</td>
<td>yes</td>
<td>no</td>
<td>A behavioural IGBT model implemented in Simulink by using SimScape blocks. Transient state results are not verified by measurements.</td>
</tr>
<tr>
<td>(Oustad et al., 2016)</td>
<td>datasheet and measurements</td>
<td>yes</td>
<td>no</td>
<td>An Ansys Simplorer IGBT model used to simulate waveforms and switching energies. An additional method to calculate switching energies is presented in the study.</td>
</tr>
<tr>
<td>(Li et al., 2017)</td>
<td>measurements</td>
<td>yes</td>
<td>(yes)</td>
<td>An IGBT model for static and transient state modelling. The model structure basically enables short-circuit modelling, but it is not studied.</td>
</tr>
<tr>
<td>(Xu et al., 2018)</td>
<td>datasheet</td>
<td>yes</td>
<td>no</td>
<td>A simple offline IGBT transient model used to simulate power losses. The simulated losses are used for an online simulation model.</td>
</tr>
<tr>
<td>(Zhang et al., 2018)</td>
<td>datasheet</td>
<td>no</td>
<td>no</td>
<td>The model is based on a Thevenin equivalent circuit. Validation is performed against a Matlab model. Voltage and current waveforms are not studied.</td>
</tr>
<tr>
<td>(Bai et al., 2019)</td>
<td>datasheet</td>
<td>yes</td>
<td>no</td>
<td>A simple behavioural model to be implemented to an FPGA real-time simulator. Online simulation results are compared with offline results.</td>
</tr>
<tr>
<td>(Hanini and Ayadi, 2019)</td>
<td>datasheet and measurements</td>
<td>yes</td>
<td>no</td>
<td>An IGBT model to simulate power losses. No details about the characterization process and no extensive comparison against experiments.</td>
</tr>
<tr>
<td>(Mijlad et al., 2019)</td>
<td>datasheet</td>
<td>yes</td>
<td>no</td>
<td>The same as in (Mijlad et al., 2015).</td>
</tr>
</tbody>
</table>

2.5.2 Conclusions of the literature survey

As presented in the survey above, most of the studies concentrate on behavioural IGBT models and focus on determining the power losses of the IGBT. Furthermore, the power losses are determined in the normal operating point region. Some of the proposed models are able to describe IGBT operation in the current saturation mode, because the modelled...
output characteristics show a good agreement with the information given in the datasheets or measurement results. However, in all cases where the output characteristics in the current saturation mode are discussed, the analysis is limited to the lower range of $V_{CE}$. The literature survey shows that behavioural IGBT models have not been investigated from the short-circuit operation perspective so far. Some publications mention the short-circuit operation or the current saturation operation in a wide $V_{CE}$ range, but in these cases, it is also pointed out that current saturation as a function of $V_{CE}$ is complicated to model and requires measurements if modelled with simple component models. Furthermore, according to the literature survey, there is no evidence that the self-heating effect is included in the behavioural IGBT models that also cover the current saturation mode modelling. From that perspective, the topic of this doctoral dissertation is novel and relevant.
3 IGBT behavioural models for short-circuit simulation

In this study, two behavioural circuit simulation IGBT models are used for the short-circuit operation modelling. The first model is based on models presented previously in the literature (Denz et al., 2014). Compared with the previous models, the model is improved and optimized for the short-circuit Type I operation. The model is designated as Model1. The baseline for Model1 is a behavioural IGBT model included in the commercially available simulation software Simplorer, a part of the Ansys product family. The Simplorer IGBT model is designated as Model2. The external circuit, such as DC and snubber capacitors, the busbar structure, and the gate driver are modelled in the same way with both the IGBT chip models, Model1 and Model2.

The most important criterion for the models to be applied is that the model should be characterized by using datasheet (or other commercially available) information, and in the best case, without measurements. Another essential requirement is that the model should, in principle, be able to describe the short-circuit behaviour of the device, that is, the current saturation mode. As presented in Section 2.2.2, this requires that the model is composed of separated MOSFET and BJT parts that are parallel connected to depict the internal structure of the device, or that other methods are used to describe the current saturation operation. Furthermore, because the objective of the study is to investigate IGBT modelling options for everyday research and development work, it is desirable that the model is included in or can be implemented into software that can be used to model larger systems than the semiconductor device itself.

Furthermore, commutation circuit inductances have a significant effect on the circuit operation in the short-circuit conditions, and therefore, also inductances have to be modelled. In this study, busbar and IGBT module inductances/resistances are estimated by modelling them in a three-dimensional structure with the Ansys Q3D Extractor software. The software is very suitable for modelling of this kind, as it defines the self-partial and mutual-partial inductances and resistances for each net in the model as a function of frequency. When the $RL$ parameters are solved, the model can be implemented into the circuit simulator schematics as a sub-circuit. Even though this type of commutation circuit inductance/resistance model is used with the IGBT models in this study, the modelling method is not in the focus of investigation. The modelling method of the busbar structure is discussed in (Smirnova, 2015).

3.1 Description of Model1

As described above, Model1 is not based on the physical behaviour of the IGBT but aims at describing its current and voltage behaviour as accurately as possible with information from the datasheet or commercially available data. Even though Model1 is based on the behavioural IGBT model presented in (Denz et al., 2014), it has added features that enable modelling of the IGBT short-circuit operation. In particular, the IGBT chip thermal model, the transfer characteristics as a function of $V_{GE}$, $V_{CE}$, and $T_j$, and the voltage and
current dependence of $C_{CG}$ are essential features that have to be included in the model to make short-circuit modelling possible.

A block diagram of the Model1 and the external circuit is outlined in Figure 3-1.

Figure 3-1 Block diagram of Model1 and the external circuit.

The model can be divided into six main sections: DC source, DC link capacitors, DC link busbars, snubber capacitors, IGBT module, gate driver, and load section.

A basic block diagram of the IGBT chip model is presented in Figure 3-2. A normal circuit simulator DC voltage source is used to model the DC source section. The DC and snubber capacitor sections are modelled by using lumped $RLC$ models. Four parallel-connected capacitors are used as an energy store in the test setup, and thus, the DC capacitor model includes four parallel $RLC$ branches. Because the IGBT module has doubled main current contacts (DC plus, DC minus, and phase out) and thus applies two snubber capacitors, the snubber capacitor model includes two parallel-connected $RLC$ branches. The $RLC$ parameters for the snubber capacitors are from the component datasheets, while the $RLC$ parameters for the DC capacitors are from the datasheet and frequency response analyser measurements.
3.1 Description of Model 1

The gate driver is modelled in a simple way by implementing only separate gate resistors with ideal series-connected diodes for the turn-on and turn-off and a gate voltage source as presented in Figure 3-3.

The IGBT chip is modelled with a current-controlled voltage source that implements the IGBT output characteristics, a voltage- and temperature-controlled current source that implements the IGBT transfer characteristics, and two terminal capacitances, $C_{CG}$ and $C_{GE}$, that determine the chip operation in transient states.

The current-controlled voltage source is controlled by the current $I_C$ that is flowing through the component. Because the voltage is always quite constant in the short-circuit Type I (excluding voltage drops/spikes caused by inductances in the commutation circuit), it is not necessary to accurately adjust the operation of this voltage source. If the model is used to model the short-circuit Type II or normal operation, where the voltage drop across the component is small, the output characteristics have to be adjusted more carefully. Implementation of the output characteristics is carried out with a look-up table, which includes an $I_C-V_{CE}$ curve.
The current source that implements the IGBT transfer characteristics is controlled by the gate-emitter voltage $V_{GE}$, the collector-emitter voltage $V_{CE}$, and the chip temperature $T_j$. To implement $I_C$ as a function of several variables, a multi-dimensional look-up table is used in the model as a control for the current source.

The chip temperature $T_j$ is determined by a simple thermal model of the IGBT chip. The chip thermal capacity is calculated by Eq. (2.21) as presented in Section 2.2.4. The short-circuit power losses $P_{SC}$ are calculated by multiplying $I_C$ and $V_{CE}$, and the losses are fed into the thermal model. When no heat transfer during the short-circuit and a uniform chip temperature are assumed, the chip temperature $T_j$ is directly the temperature of the chip thermal capacity. The chip dimensions can be found from the chip datasheet (Infineon, 2016). The specific heat capacity of silicon is 0.7 Ws/(g °C).

The gate-emitter voltage in transient states is affected by the terminal capacitances $C_{GE}$ and $C_{CG}$. As presented in Section 2.2.6, $C_{GE}$ can be modelled with a constant value, but $C_{CG}$ changes as a function of $V_{CE}$ and $I_C$, and therefore, a variable capacitance is used for the $C_{CG}$ model. The $C_{CG}$ voltage and current dependence is implemented into Model1 by using a multidimensional look-up table.

The inductance/resistance models for the main busbars and the IGBT module internal busbars are modelled with numerical methods and implemented into the circuit model. The inductance/resistance model is discussed further in Section 3.3.

Descriptions for all the components in Figure 3-2 are given in Table A-2 in Appendix A.

### 3.1.1 Model1 characterization

The first task in the characterization of Model1 is to extend the component transfer characteristics, which are given in the component datasheet (Infineon, 2016), to also include $V_{GE}$ levels that occur in the short-circuit operation. Commonly, the transfer characteristics in the datasheet are given only for lower $V_{GE}$ levels (12 V in this case). To be able to model the short-circuit operation, transfer characteristics are needed to describe up to approx. $V_{GE} = 15$ V–20 V, depending on the effect of $C_{CG}$ on $V_{GE}$. In Model1 characterization, the transfer characteristics from the datasheet (Figure 3-4a) are extrapolated up to $V_{GE} = 20$ V assuming that $I_C$ is linearly dependent on $V_{GE}$ after the gate threshold voltage $V_{GE,TH}$ (Figure 3-4b). In the component datasheet, the transfer characteristics are also given at temperatures of $T_j = 25$ °C, 125 °C and 150 °C. A similar extrapolation is done for $I_C$–$V_{GE}$ data at all three temperatures to include the self-heating effect in the transfer characteristics.
3.1 Description of Model1

However, the transfer characteristics from the component datasheet are valid only for very low $V_{CE}$ values ($V_{CE} = 20$ V in this case). Thus, the $I_{C,sat}$ dependence of $V_{CE}$ has to be included in the transfer characteristics. As presented in Section 2.2.3, accurate determination of $I_{C,sat}$ as a function of $V_{CE}$ requires very detailed information of the semiconductor chip properties and solving the ambipolar current gain $\alpha_{PNP}$ with an analytical or numerical method. Detailed information of chip properties is not commercially available, and therefore, some other method is needed to estimate $I_{C,sat}$ as a function of $V_{CE}$. During the model development it was found that this dependence cannot be solved with the information available, and therefore, the $I_{C,sat}$ dependence on $V_{CE}$ is determined from the measurements in this study. $I_{C,max}$ is defined from the measurements at $V_{CE} = 350$ V$–750$ V and a linear approximation for voltage dependence is extracted by applying these $I_{C,max}$ values. As presented in (Basler, 2014) and (Baliga, 2019), the $I_{C,sat}$ voltage dependence is not exactly linear, but for example for IGBTs with a collector-side buffer layer there are two different gradients in the IGBT output characteristics. Furthermore, different gradients occur for different $V_{CE}$ values as shown in Figure 2-10. Nevertheless, as the objective of this study is to develop a simplified method to model the IGBT short-circuit behaviour, it is assumed that $I_{C,sat}$ is linearly dependent on $V_{CE}$. With these steps, the transfer characteristics with the $V_{GE}$, $V_{CE}$, and $T_j$ dependence can be composed. These characteristics data are included in the look-up table that controls the current source implementing the transfer characteristics in Model1.

The IGBT output characteristics for higher $V_{CE}$ levels can be created after the transfer characteristics have been composed. However, because $V_{CE}$ is always quite high in the short-circuit Type I, the output characteristics at lower $V_{CE}$ levels do not have a significant influence on the model results. Nevertheless, if the model is also used for the normal operation simulation, the short-circuit Type II simulation, or the short-circuit Type I simulations with a large commutation inductance, the importance of the accuracy of the output characteristics increases significantly. Because the effect of the gate-side control

![Figure 3-4 IGBT module transfer characteristics a) from the datasheet (Infineon, 2016) and b) extended by linear estimation up to $V_{GE} = 22$ V.](image)
circuit is excluded from this study, the output characteristics have to be composed only for one \( V_{GE} \) level (\( V_{GE} = 15 \) V in this case).

To compose the output characteristics, some approximations have to be made. First, the current is assumed to increase linearly in the component active region until current saturation. With this assumption, the first part of the characteristics can be built. The current saturation level for a particular \( V_{GE} \) can be extracted from the transfer characteristics as discussed in the previous chapter. The level to be used is the level that is extrapolated from the original datasheet curves (\( V_{CE} = 20 \) V), not from the curves that are extrapolated for higher \( V_{CE} \) values. The intersection of the \( I_{C,sat} \) level and the linearly increasing \( V_{CE} \) line can be taken as the first knee point of the output characteristic curve. Next, the \( I_{C,sat} \) value with the highest \( V_{CE} \) should be taken from the transfer characteristics. As discussed previously, \( I_{C,sat} \) can be approximated to increase linearly between these two points. The knee point of the curve can be smoothed manually to prevent discontinuity points in simulations. By using datasheet information, it is not possible to estimate the non-linearity of the knee point, and thus, the curve has to be adjusted manually.

The transient state operation of Model1 is adjusted by capacitance characterization. As described in the previous section, the capacitances \( C_{GE} \) and \( C_{CG} \) determine the Model1 transient state behaviour at the chip level. \( C_{GE} \) does not vary significantly as a function of \( V_{CE} \), and thus, the datasheet value can be used to characterize \( C_{GE} \) in the model. \( C_{CG} \) has a very non-linear behaviour as a function of voltage and current (as presented in Section 2.2.6), and it has a considerable effect on the IGBT transient state behaviour. Thus, its characterization requires more effort than the characterization of \( C_{GE} \). As presented in Eq. (2.38), an estimate for the \( C_{CG} \) voltage dependence can be calculated by using the datasheet value and the square root of voltage across the capacitance (\( V_{CE} \) in the case of an IGBT). Furthermore, the current dependence of \( C_{CG} \) can be estimated by using the square root of \( I_{C} \) and the current correction coefficient \( K_{CCG} \) (Eq. (2.39)).

However, to the author’s knowledge, no simplified equation for the \( C_{CG} \) current dependence estimation with the help of datasheet values has been presented in the literature. Therefore, in this study, measurement results are used to adjust the \( K_{CCG} \) value. The same method is used for example in (Tominaga et al., 2011). \( K_{CCG} \) is optimized for short-circuit operation at \( V_{DC} = 750 \) V, \( T_a = 25 \) °C, \( R_{g,off} = 4.7 \) Ω, and \( t_{SC} = 12.5 \) µs. \( C_{GE} \) mainly affects delays at the beginning of the short-circuit turn-on and turn-off. In the Model1 characterization, it was found that \( I_{C} \) starts to increase too early if the datasheet value for \( C_{GE} \) is used. To make the delay correct, \( C_{GE} \) is increased so that the simulations correspond with the measurement results. Even though \( C_{GE} \) is relatively independent of \( V_{CE} \), it changes as a function of \( V_{GE} \) as presented in (Luo et al., 2016). This \( V_{GE} \) dependence may cause an error when the \( C_{GE} \) value from the datasheet is used. The \( C_{GE} \) dependence of \( V_{GE} \) is also highly non-linear, and its accurate determination requires, again, detailed information about the IGBT chip structure. Thus, in this study, to keep the model practical, \( C_{GE} \) is corrected by applying measurement results.

The main characterization steps for Model1 are as follows:
3.2 Description of Model2

1. Extend the transfer characteristics from the datasheet by linear estimation up to \( V_{GE} \) levels that may occur in short-circuit operation.
2. Determine \( I_{C,sat}-V_{CE} \) dependence from the measurements and compose transfer characteristics for the full voltage range (from the \( V_{CE} \) level that is used in the transfer characteristics in the datasheet up to the voltage level relevant for short-circuit operation).
3. Compose output characteristics up to the relevant \( V_{CE} \) level by applying the datasheet characteristics, transfer characteristics, and the \( I_{C,sat}-V_{CE} \) dependence.
4. Characterize capacitance values for \( C_{GE} \) and \( C_{CG} \) by applying Eq. (2.39) and measurement results.

Characterization parameters relevant for Model1 are presented in Appendix A.

3.2 Description of Model2

The other IGBT model, Model2 investigated in this study, is a Basic Dynamic IGBT model included in the Ansys simulation software package. The model includes several electrical and thermal parameters, which are fitted by the characterization tool according to the user-given data. When the necessary information is fed into the characterization tool, it performs fitting of the parameters and generates the IGBT model. The model behaviour can also be adjusted afterwards by changing the parameters, but in this study, the initial model parameters after the model characterization are used. The manual of the simulation software provides only limited information of the model and its parameters, and therefore, the model description given below is not complete. The analysis of Model2 is based on the software manual (Ansys, 2019), and it is complemented with conclusions that can be made from the model behaviour.

The basic structure of Model2 is presented in Figure 3-5.
As presented in the figure, the basic structure of the model is based on the MOSFET and pnp BJT part to model static operation, and capacitances to model the dynamic states. Furthermore, Model2 contains a dynamic FWD model and an IGBT tail current model, which also includes components to prevent oscillation of the model. It is pointed out that the names assigned to the parameters in the characterized IGBT model do not correspond to the names of the equivalent circuit, but other names are used in the basic dynamic IGBT parameter list.

According to the Ansys manual, the Schichman–Hodges model is used for the MOSFET part. The Schichman–Hodges model is also known as the MOSFET Level 1 model in the SPICE simulator (Schichman and Hodges, 1968). The MOSFET part provides base current for the BJT part, which is used to determine $I_C$ in the static state. All the MOSFET part parameters and some of the BJT part parameters are temperature dependent. However, information of the numbers of chips in the IGBT module or the chip thermal capacity cannot be given in Model2, but the thermal model is implemented by using a partial fraction Foster-type thermal network, which is a mathematical presentation of the thermal impedance from the chip junction to the IGBT module baseplate. Because the Foster-type thermal network does not describe the temperature inside the network, it can be assumed that it does not describe the chip temperature with high precision in a highly dynamic short-circuit event, in which heat transfer is negligible.

According to Figure 3-5, transient states are modelled with several capacitances in Model2. Nevertheless, only four capacitance values can be found from the parameter list of the characterized model. These capacitances are named $C_{IN0}$, $C_{IN1}$, $C_{R0}$, and $C_{R1}$, and they are off-switch input capacitance, on-switch input capacitance, off-switch feedback capacitance, and on-switch feedback capacitance, respectively. Thus, it seems that the model uses different capacitances for turn-on and turn-off. Furthermore, the
3.2 Description of Model2

capacitances that are visible for the model user are separated into the gate-side input capacitance and the feedback capacitance, which probably represents the Miller capacitance $C_{CG}$. The model parameter list includes several correction factors for the capacitances. With the correction factors, the capacitance values can be adjusted as a function of temperature, voltage, and current. The complete parameter list of Model2 is provided in Appendix B.

Because the internal busbar structure of the IGBT module is modelled with numerical methods, the external connector parameters are changed to zero in Model2.

The parts of Model2, excluding the IGBT chip model, are similar to Model1.

3.2.1 Model2 characterization

The Model2 characterization can be done semi-automatically by providing relevant information for the characterization tool included in the simulation software. Information for the characterization tool is typically available in the component datasheet, but if some information is missing, characterization can be done without a complete dataset. In that case, it can be assumed that the best accuracy of the model cannot be achieved. The following information is needed for the Model2 characterization:

- Nominal values ($V, I, t_j, \ldots$)
- Capacitance values ($C_{ies}, C_{res}, \ldots$)
- Resistance values ($R_{g,int}, \ldots$)
- Module parameters ($R_C, L_C, R_E, L_E, R_G, L_G, \ldots$)
- Transfer characteristics ($I_C(f, V_{CE})$ and $I_F(f, V_F)$)
- Output characteristics ($I_C(f, V_{GE})$)
- Parameters for the thermal network
- Switching energies ($E_{on}, E_{off}$)
- Switching times ($t_{d,on}, t_s, t_{d,off}, t_f$)

Because different module manufacturers may define the datasheet information slightly differently, a correct component manufacturer has to be chosen at the beginning of the characterization.

Furthermore, additional information, for example of switching energies in different operating points, can be given in the characterization tool to improve the model accuracy. However, in this study, only datasheet information is used for the Model2 characterization.
3.3 Busbar and IGBT module inductance model

The busbar model of this study consists of the internal busbars of the IGBT module and the external busbars that are connected between the DC link capacitors and the IGBT module. The resistance and inductance values of the structure are modelled with the Q3D software, which solves the self- and mutual inductances for the busbar parts of the model. The model of the IGBT module internal busbars is simplified by excluding bond wires.

At a general level, modelling of the inductance can be divided into two categories according to the current path: loop inductance modelling and partial inductance modelling. The difference between these methods is that in the loop inductance modelling the current return path is known, and the overall current path constitutes a loop between the source plus and minus connections, whereas in the partial inductance modelling the current return path is not exactly known when modelling the structure. The latter is especially useful in modelling of power electronics. For example, when modelling a circuit that includes semiconductor switches, the current path changes during the simulation if the current-conducting switch is controlled from the on-state to the off-state (or vice versa), and thus, the inductance model modelled as a loop inductance is no longer applicable. The theory of the loop and partial inductances is discussed in (Clayton, 2010).

Modelling of the $RL$ parameters of the busbar structure is started by constructing a 3D model of the busbars (Figure 3-6) and defining the excitation sources and sinks for each net in the model.
The \( RL \) parameters are then solved for the frequency range from 0 Hz to 100 MHz. Data from the solved numerical method model are then implemented as a space state subcircuit to the circuit simulator schematics. In this way, frequency-dependent resistance and inductance values can be used in the circuit simulator.

The software calculates the self-partial inductance and the mutual partial inductances for each net. The simulation results show that the inductances do not change significantly after a couple of tens of kilohertz. However, the resistance values increase considerably as the frequency increases as a result of well-known proximity and skin effects. A correct resistance value of the commutation circuit is of significance, as it acts as a damping element for resonances that occur during or around the short-circuit event.

**Busbar model validation**

Stray inductances in the commutation circuit with snubber capacitors constitute a resonance circuit, the effect of which can be seen as an oscillation in the \( V_{CE} \) waveform after the short-circuit turn-off. According to (Volke et al., 2017), the frequency of the oscillation \( f_{OSC} \) is

\[
f_{OSC} = \frac{1}{T_{OSC}} = \frac{1}{2 \cdot \pi \cdot \sqrt{\left(L_{\sigma,\text{CDC}} + L_{\sigma,\text{BUSBAR}} + L_{\sigma,\text{CSUB}}\right) \cdot C_{\text{SNUB}}}},
\]

where \( T_{OSC} \) is the time of the oscillation period, \( L_{\sigma,\text{CDC}} \) is the stray inductance of the DC capacitors, \( L_{\sigma,\text{BUSBAR}} \) is the stray inductance of the busbars, \( L_{\sigma,\text{CSUB}} \) is the stray inductance of the snubber capacitor, and \( C_{\text{SNUB}} \) is the capacitance of the snubber capacitor.

The busbar stray inductance can be solved from Eq. (3.1), and it can be calculated by applying measured values of oscillation. The stray inductance of the busbars extracted from Eq. (3.1) is

\[
L_{\sigma,\text{BUSBAR}} = \frac{(1/\left(2 \cdot \pi \cdot f_{OSC}\right))^2}{C_{\text{SNUB}}} - L_{\sigma,\text{CDC}} - L_{\sigma,\text{CSUB}}
\]

By using partial and mutual inductances for the plus and minus plates, the busbar stray inductance can be extracted from the Q3D model. Figure 3-7 depicts an inductance matrix from the Q3D model. The values are determined at 1 MHz.
3 IGBT behavioural models for short-circuit simulation

The total stray inductance of the busbars can be calculated by summing the self-inductances from the diagonal of the matrix and adding the mutual inductances from the off-diagonal of the matrix to the self-inductance value. In this case, the simulated total stray inductance $L_{\text{os,BUSBAR}}$ is

$$L_{\text{os,BUSBAR}} = 13.30 + 18.67 - 2 \cdot 12.09 = 7.79 \text{ nH} \quad (3.3)$$

From the short-circuit measurements and datasheets, the parameters in Table 3-1 can be determined and/or estimated. The measurements from the operating point $V_{\text{DC}} = 750 \text{ V}$, $T_a = 25 \degree \text{C}$, $t_{\text{SC}} = 5 \mu\text{s}$, and $R_{\text{g,off}} = 4.7 \Omega$ were used to determine the parameters in the table. The $V_{\text{CE}}$ waveform of this operating point is presented in Figure 4-22.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{\text{OSC}}$</td>
<td>388.3 kHz</td>
</tr>
<tr>
<td>$L_{\text{o,DCD}}$</td>
<td>30 nH</td>
</tr>
<tr>
<td>Total $L_{\text{o,DCD}}$</td>
<td>30/4 nH</td>
</tr>
<tr>
<td>$L_{\text{o,CSNUB}}$</td>
<td>25 nH</td>
</tr>
<tr>
<td>Total $L_{\text{o,CSNUB}}$</td>
<td>25/2 nH</td>
</tr>
<tr>
<td>$C_{\text{SNUB}}$</td>
<td>3 \mu\text{F}</td>
</tr>
</tbody>
</table>

Because there are four parallel-connected DC capacitors and two parallel-connected snubber capacitors, the total DC capacitor bank stray inductance is $L_{\text{o,DCD}}$ divided by four, and the total snubber capacitor bank stray inductance is $L_{\text{o,CSNUB}}$ divided by two. The total snubber capacitance value is twice the value of $C_{\text{SNUB}}$. The busbar stray inductance $L_{\text{os,M,BUSBAR}}$ from the measurements can be calculated by Eq. (3.2) and values from Table 3-1.
3.4 Limitations of the models

\[ L_{\sigma M, \text{BUSBAR}} = \frac{(1/(2 \cdot \pi \cdot 388.3 \, \text{kHz}))^2}{6 \, \mu\text{F} - \frac{30}{4} \, \text{nH} - \frac{25}{2} \, \text{nH}} = 7.24 \, \text{nH} \]  

When considering the calculation above, it is pointed out that it includes several simplifications and generalizations. For example, the capacitance value in Eq. (3.2) is valid only if the capacitance of the snubber capacitor is much smaller than the DC link capacitance. If the snubber capacitance is almost equal to the DC link capacitance, \( C_{\text{SNUB}} \) in Eq. (3.1) has to be replaced with a series connection of the snubber and DC link capacitances. Furthermore, the capacitor self-inductance given in the capacitor datasheet is commonly determined at a low frequency, and thus, it cannot be used directly in the busbar stray inductance calculation. In this doctoral dissertation, the DC link capacitor inductance is determined with a Venable frequency response analyser (FRA). The inductance for the \( L_{\sigma M, \text{BUSBAR}} \) calculation is determined at 1 MHz, which is the same as in the Q3D simulation. However, a similar frequency response measurement is not available from the snubber capacitors, and thus, \( L_{\sigma, \text{CSUB}} \) is estimated from the datasheet. Furthermore, Eq. (3.1) does not take into account for example different current paths between parallel-connected capacitors or stray inductances caused by connections. Therefore, Eq. (3.1) should be considered as an approximation of stray inductance, and because of simplifications, it cannot generally give accurate answers.

The analysis presented above shows that the inductance modelled with the Q3D corresponds with the measurements, and that the inductance modelling method is applicable to the IGBT short-circuit modelling.

3.4 Limitations of the models

Owing to the simple structure of Model1 and Model2, there are some limitations when considering the modelling accuracy. The most significant limitations from the perspective of short-circuit operation are listed below.

- High-frequency \( V_{\text{GE}} \) oscillation at low \( V_{\text{CE}} \) levels cannot be described correctly because the models do not describe the component behaviour by solving charge distribution inside the component. As presented in Section 2.2.7, the origin of the \( V_{\text{GE}} \) oscillation is the time-varying \( C_{\text{CG}} \) caused by the charge storage effect on the emitter side of the IGBT.

- The \( I_{\text{C, sat}} \) dependence on \( V_{\text{CE}} \) cannot be described precisely because its accurate modelling requires accurate modelling of the current gain \( \alpha_{\text{PNP}} \). As presented in Section 2.2.3, \( \alpha_{\text{PNP}} \) depends on the effective base width, which depends on \( V_{\text{CE}} \). Furthermore, the \( I_{\text{C, sat}} \) dependence on \( V_{\text{CE}} \) is not exactly linear for the components that have a buffer layer (for example the FS IGBT), and thus, exact modelling of \( \alpha_{\text{PNP}} \) requires very detailed information about the IGBT chip structure.
• The tail current at the short-circuit turn-off cannot be described, because it requires solving of the amount of charge carriers stored on the IGBT collector side during turn-off. An exact solution can be achieved with analytical or numerical methods if the IGBT structure and physical properties are known.

• In Model1, the chip temperature is assumed uniform along the chip. As presented in Section 2.2.4, this is not exactly correct, and thus, some inaccuracy can be assumed to be due to the thermal modelling. Furthermore, in Model1, the only temperature-dependent parameter is $I_{C,sat}$. In practice, there are more temperature-dependent parameters in the circuit used in this study.

Despite the limitations presented above, the models are applicable to short-circuit modelling. Nevertheless, it is important to understand the limitations when the simulation results are interpreted. It may be possible to remove some limitations, at least to some extent. Suggestions for improvements and conclusions are presented in Section 5.
4 Experimental results and simulation model verification

A single-shot IGBT test setup is used for the experimental part of this study. The structure and operation principle of the setup are described in the following sections. Moreover, special challenges that arise in the IGBT (or other semiconductor component) measurement are addressed and analysed.

The main contribution of this chapter is to compare the simulation results of two simulation models to the experimental data and evaluate the validity of the models in the short-circuit simulations.

4.1 IGBT measurements

At a general level, the IGBT short-circuit experiments can be performed by using a quite simple measurement setup, because only the following main components are needed: an energy source, a short-circuit busbar to be used as a load, a device under test (DUT), and a gate driver. However, in practice, there are special questions that should be considered in order for the results of the experiments to be reliable. These questions are discussed in the following section.

4.1.1 Special challenges in short-circuit measurements

The complexity of the IGBT test setup depends mainly on the short-circuit type that is of interest. The short-circuit Type I can be investigated by a simple setup that does not include additional switches and the only controllable switch that is needed in the circuit is the DUT. If the short-circuit Types II and III are investigated, the test circuit should include a switch that is used to switch on the short-circuit on the load side. This switch should be able to conduct the maximum short-circuit current and preferably also to switch it off reliably. This additional switch increases the complexity of the mechanical structure of the setup, but it also requires a more complex test sequence control.

Depending on the busbar structure of the setup, the current measurement can be difficult to implement. This is especially true if a planar busbar structure, which is common in power electronic equipment at present, is used. Often, in this structure, the distance between the DUT and the busbars is so small that it is almost impossible to use current clamps for the current measurement. Other options for the current measurement are a current shunt or a Rogowski coil. A benefit of the shunt is that it gives accurate results, but a drawback is that some modifications are required in the busbars. Modern Rogowski coils offer a small size and a good bandwidth, but they are sensitive to disturbances. For instance, an eccentric position of the current conductor relative to the measurement loop could cause erroneous measurement results. Rogowski coils are also sensitive to offset errors.
Especially the self-heating effect (discussed in Section 2.2.4) poses major challenges for reliable and reproducible short-circuit measurements. Very high instantaneous power losses during a short-circuit with a low thermal mass of the semiconductor chip produce high temperature gradients of the chip. Because of the highly dynamic temperature state and short time intervals, it is almost impossible to measure the exact chip temperature during a short-circuit without special arrangements in the test setup and modifications to the module under test (e.g. the use of a thermal imaging camera).

In many cases, the purpose of the measurements is to determine the short-circuit current $I_{SC}$ as a function of the gate emitter voltage $V_{GE}$. This relation is strongly temperature dependent, and thus, the chip temperature (junction temperature $T_j$) and $V_{GE}$ have to be known accurately to determine $I_{SC}$. Because of the high power losses and the small thermal capacity, the chip temperature increases rapidly, and to mitigate the effect of the temperature rise, $I_{SC}$ has to be determined as soon as it reaches a steady state. Furthermore, at the beginning of the short-circuit, $V_{GE}$ is also in a dynamic state. A high $\frac{di}{dt}$ combined with the parasitic inductance $L_ı$ of the commutation circuit also causes a change in the collector emitter voltage $V_{CE}$ (as presented in Figure 1-3). The main and gate circuits are coupled through the Miller capacitance $C_{CG}$, and the $\frac{dv}{dt}$ of $V_{CE}$ causes a current through $C_{CG}$, which results in a rise or a fall of $V_{GE}$. Knowledge of the whole output characteristics of the component from 0 V to the breakdown voltage $V_{BR}$ (as discussed in Section 2.2.3) is essential from the perspective of the short-circuit behaviour modelling. However, if the whole output characteristics are determined by experiments, $V_{GE}$ should be the same in all the measurement points of one curve of the characteristics (e.g. $V_{GE} = 15$ V). The above-mentioned $\frac{dV_{CE}}{dt} - V_{GE}$ coupling through $C_{CG}$ makes the determination of the output characteristics challenging.

In (Basler, 2014), a method was presented to determine the whole output characteristics of a high-voltage IGBT chip. In this method, the short-circuit current $I_{SC}$ is recorded as soon as the gate current $I_G$ reaches zero after the short-circuit turn-on. This ensures that the gate is in a steady state and it has reached the pre-set $V_{GE}$. The turn-on event is made as fast as possible by using a small turn-on resistor $R_{G,on}$. In this particular case, the self-heating effect is acceptably low because according to the analysis, the chip temperature increases less than 3 K before the $I_{SC}$ readout is recorded. Nevertheless, the temperature of the high-voltage chips tends to increase with a lower gradient than in the case of low-voltage chips because of a higher chip thickness, that is, a larger thermal capacity. If a similar method is used to determine the output characteristics of low-voltage chips, even a shorter pulse length and a faster turn-on have to be achieved to keep the temperature increase at an acceptable level. The self-heating effect and its mitigation in the output characteristics measurements is discussed in more detail for example in (Lopez and Elferich, 2006), (Jenkins and Sun, 1995), and (Nejad et al., 2011).

Furthermore, when measuring the short-circuit behaviour of an IGBT with a module-type package, the measurement results are affected by the IGBT chip itself and by the internal structure of the module. As discussed above, the internal structure of the module adds parasitic inductances and capacitances to the measurement circuit, which has to be taken
4.1 IGBT measurements

into account when comparing the simulation and measurement results. For practical reasons, the measurements are taken from the outer interface of the module. Thus, when interpreting the simulation results, it is important that the voltage and current recordings from the simulations are taken from the same interface.

One special challenge in all experimental studies on the semiconductor behaviour is the semiconductor parameter variation between the measured devices, which may cause different measurement results for different DUTs even though the DUT type and all the other measurement parameters are kept the same. The manufacturer usually provides typical, maximum, and minimum values for some parameters, for example for $V_{CE,sat}$ and $V_{GE,th}$, but normally, only typical values are given for the component characteristics curves and the short-circuit behaviour. The parameter variation range varies for instance between component types and manufacturers, and thus, it is very difficult to estimate the variation without experimental verification of a large number of DUTs. Nevertheless, the parameter variation between DUTs is outside the scope of this study. Hence, it is emphasized that the comparison between the simulation results and the experiments is valid only for the DUT that is used in these experiments.

In this study, a comparison of the short-circuit parameters is made by comparing results from two samples, IGBT1 and IGBT2. The results in Figure 4-1 and Figure 4-2 show that the $V_{CE}$ and $V_{GE}$ waveforms are basically the same between the IGBTs, but a significant difference can be observed in the $I_C$ waveforms in Figure 4-3. One possible reason for the difference in the $I_C$ waveform may be the variations in the test temperature, as the measurements were not performed during the same day. However, a value of the DUT temperature sensor (NTC) was recorded at the start of every test session, and the difference in the initial temperature between the IGBT1 and IGBT2 measurements was around 1 °C.
Figure 4-1 IGBT1 and IGBT2 $V_{CE}$ waveforms, $V_{DC} = 750$ V, $R_{g,off} = 4.7 \, \Omega$, $t_{SC} = 8.33$ µs, $T_a = RT$.

Figure 4-2 IGBT1 and IGBT2 $V_{GE}$ waveforms, $V_{DC} = 750$ V, $R_{g,off} = 4.7 \, \Omega$, $t_{SC} = 8.33$ µs, $T_a = RT$. 
The variation in the IGBT short-circuit behaviour between components has not been extensively studied in the literature, but for example in (Basler et al., 2011), several high-voltage IGBT chips were measured in a short-circuit. In (Basler et al., 2011), a collector current variation of ±50 A was discovered between parallel-connected chips that were measured under the same test conditions. The average maximum short-circuit current in the measurement was approx. 600 A (see Figure 4-4), while the nominal current of the chips was 50 A. If the maximum difference between the chips is 50 A, it is roughly 8.33 % of the average. Thus, it is obvious that as a result of parameter variation, different IGBT modules may have different short-circuit behaviours, as seen in Figure 4-3. In the measurements in (Basler et al., 2011) the effect of variation in auxiliary circuit parameters, such as the inductance of the connections and the gate resistance, was mitigated.

The simulation models in this study are characterized by applying datasheet values, and thus, the models represent the average behaviour of the component. However, the simulation results are compared with the measurement of a single IGBT module, and therefore, when making conclusions from the comparison, this statistical parameter variation has also to be considered. The DUT in the experiments of this study includes several parallel-connected IGBT chips, which mitigates the effect of statistical variation between the chips when the total collector current of the module is investigated.
4 Experimental results and simulation model verification

Figure 4-4 Short-circuit current variation between similar four parallel-connected high-voltage IGBT chips (Basler et al., 2011).

4.2 Experimental setup

The experimental part of this study is performed by using a single-shot IGBT short-circuit test setup, shown in Figure 4-5, and Figure 4-6 depicts the detailed locations of the measurement probes. The switching event in the motor drives and the grid converters can be investigated by using a simplified circuit of the commutation block, which basically consists of an energy source and two semiconductor switches containing commutation and a load, as shown in Figure 4-7. A single-shot test setup imitates this kind of commutation block. In Figure 4-7, \( C_{DC} \) is the DC link capacitance, \( L_0 \) is the parasitic inductance of the busbars, \( R_{load} \) and \( L_{load} \) are the load resistance and inductance, respectively, and GDR is the IGBT gate driver.
4.2 Experimental setup

Figure 4-5 Single-shot test setup for IGBT short-circuit measurements.

Figure 4-6 Measurement probe locations in a single-shot test setup.
Experimental results and simulation model verification

The DC capacitor bank in the setup acts as an energy source that provides energy for the short-circuit pulse. In this study, the energy source is composed of four parallel-connected 1300 µF/1500 $V_{DC}$ film capacitors, and thus, the total capacitance of the capacitor bank is 5.4 mF. The capacitors are connected to the IGBT module under study with a laminated copper busbar structure made from 1 mm copper sheet. The IGBT module consists of two series-connected IGBTs with parallel-connected FWDs. In the single-shot setup, high-side components are used only as a free-wheeling path, that is, the gate of the high-side IGBT is short circuited to its auxiliary emitter connection, and the low-side IGBT operates as an actual switching component, which is referred to as the device under test (DUT). The load side of the setup is simply a small copper sheet, which is connected across the high-side IGBT. The IGBT module has double main connectors, and thus, the clamp circuit is composed of two separate clamp capacitors, which are connected directly to the IGBT module DC plus and DC minus connections. Each clamp capacitor has a capacitance of 3 µF, resulting in a total clamping capacitance of 6 µF. The purpose of the clamp capacitors is to reduce the amplitude of the collector-emitter voltage spike at the short-circuit turn-off by decreasing the commutation inductance seen from the IGBT module connectors.

The DUT is controlled by a custom-made gate driver (GDR). The structure of the GDR is made very simple, and it does not include any safety functions. In principle, the GDR only provides $V_{GE, on}$ and $V_{GE, off}$ voltages for the DUT gate side. The $V_{GE, on}$ and $V_{GE, off}$ voltages are fixed, but the gate resistances $R_{g, on}$ and $R_{g, off}$ can be varied. A signal generator is used to provide the control signal for the GDR. The short-circuit pulse length $t_{SC}$ is determined directly by the length of the signal generator pulse. A schematic of the GDR is presented in Appendix C.

The $V_{CE}$ and $V_{GE}$ voltages are measured with differential voltage probes, and Rogowski coils are used for the collector current measurement. As the DUT has double main...
4.2 Experimental setup

connectors, also two Rogowski coils are needed to measure the total current through the DUT. Owing to practical limits, the current through the DUT is measured from the emitter side of the lower IGBT. Two voltages ($V_{CE}$ and $V_{GE}$) and two currents ($I_{C1}$ and $I_{C2}$) are recorded with a four-channel oscilloscope. The total current is calculated from the measured currents with the math operations of the oscilloscope ($I_{C} = I_{C1} + I_{C2}$). A list of the test setup component types and types of measurement devices is presented in Appendix D.

An IGBT module of the type FF1400R12IP4 is chosen as the DUT, because it is widely used in power electronics connected to 690 V or 400 V grids in industrial and renewable energy applications. Even though the module type is not the newest one, it is still in production and a potential alternative to new module types. The chip technology applied in the module (trench gate/field-stop) is also the most popular one in the market at the moment. The type of the IGBT chip used in the module is IGC142T120T8RH. According to the chip datasheet (Infineon, 2016), the voltage rating of the chip is 1200 V and the nominal current 150 A. The die size is 140.05 mm$^2$, and the silicon thickness 140 µm. The die size and the thickness are used to approximate the chip thermal capacitance as presented in Section 2.2.4. The IGBT module consists of 12 parallel-connected IGBT chips.

The internal structure of the IGBT module used in the experimental part of this study is presented in Figure 1-6. The internal layout of the module is composed of six parallel-connected IGBT/diode packages, and each package has two parallel-connected IGBT chips for the upper/lower IGBT and two parallel-connected diode chips for their FWDs. Consequently, both the main circuit IGBTs are composed of 12 parallel-connected IGBT chips, and both the main circuit FWDs of 12 parallel-connected diode chips.

The chip applies trench gate and field-stop (FS) technologies (Infineon, 2009). The basic structure of the chip is presented in Figure 4-8.

![Image of the IGBT chip](image)

Figure 4-8 Basic structure of the trench gate field-stop IGBT chip.
Both the trench gate and the field-stop layer improve the component $V_{CE,sat} - E_{off}$ trade-off curve compared with the PT and NPT structures. Furthermore, the FS layer reduces the turn-off energy by reducing the length and amplitude of the tail current. Furthermore, the use of the trench gate enables a higher cell density in the semiconductor chip.

### 4.3 Experimental and simulation results

The experimental part of this study can be divided into five sections as presented below. Sections 2–5 have only one changing operating point variable in order for the effect of change to be unambiguous.

1) Operation at the normal collector-emitter operation voltage
2) Operation at a different collector-emitter operation voltage
3) Operation with different gate turn-off resistances
4) Operation with different pulse lengths (self-heating effect)
5) Operation at an ambient temperature higher than room temperature

In all sections, the experimental results are compared with the results of Model1 and Model2.

In the first section of experiments, the IGBT module short-circuit operation is investigated with the DC voltage $V_{DC} = 650 \text{ V} - 750 \text{ V}$. Even though the nominal collector-emitter voltage $V_{CE}$ of the device is 1200 V, in practical applications the voltage across the device is in the range of 650 V–750 V. The reason for this is that the component voltage stress should be limited below its nominal voltage in any situation, and if the DC voltage of the supply circuit is increased above that range, problems may arise for example at the turn-off of the device. As discussed in Sections 1.2 and 2.2.5, the collector-emitter voltage $V_{CE}$ may increase much above $V_{DC}$ at a turn-off because of the parasitic components in the commutation circuit. Thus, the DC supply voltage has to be reduced significantly from nominal $V_{CE}$ in practice, for example when the device is used as a switching component in a two-level inverter main circuit. In the measurements of this first case, the $V_{DC}$ is varied within a limited range, and the pulse length is kept at 5 µs.

In the second section of experiments, the device operation is investigated with lower DC voltages. In practice this means that $V_{DC}$ is increased by small steps from a very small value (50 V in this case) to close to the normal operation voltage (650 V), the results are observed and recorded, and it is analysed whether any abnormal phenomena can be noticed. The device under test has a complex internal structure (Figure 1-6), and it includes many paralleled systems. It is thus probable that the variation in the voltage level may trigger unwanted phenomena.

The third section of experiments and simulation results deals with the variation in the gate turn-off resistor $R_{g,off}$. In simple gate driver circuits, $R_{g,off}$ significantly contributes to the
current slope at a turn-off, and consequently, the $V_{CE}$ voltage spike during a turn-off incident. In the experiments and simulations, $R_{g,off}$ was varied from 4.7 Ω to 22 Ω.

In the previous cases, the short-circuit pulse length was kept at 5 µs. With such a short pulse, the self-heating effect is not clearly visible, as the reduction in $I_C$ after the maximum current is mainly caused by a reduction in the gate-emitter voltage. Longer short-circuit pulses are investigated in the fourth section of experiments. By investigating the IGBT behaviour with longer pulse durations, the self-heating effect becomes more evident. The results are presented for pulse lengths 6 µs, 8.33 µs, 10 µs, and 12.5 µs. The maximum short-circuit pulse length given in the component datasheet is 10 µs.

In the fifth section of experiments, the device short-circuit operation is investigated at higher ambient temperatures. Usually, the device datasheet defines the component operation at ambient temperature ($T_a = 25 ^\circ C$), which is also called room temperature. Even though the datasheets give some of the device parameters at higher junction temperatures $T_j$, the device operation at different ambient temperatures cannot be precisely extracted from these values. Furthermore, information about the device short-circuit operation at different temperatures is seldom given in the datasheet, and the parameters determined at higher temperatures are valid only for normal operating conditions, where the device current and voltage are below the nominal values. To determine the device behaviour at a higher $T_a$, the whole IGBT test setup is assembled into a chamber whose temperature can be controlled. A traditional way to investigate the operating temperature dependence of a device is to heat or cool the switching component baseplate and perform the measurements with different baseplate temperatures $T_{base}$. However, this method does not describe a situation in which the device is operating at different ambient temperatures, because in that case, usually also the control electronics, energy storage (capacitors), and other circuit components are operating at the same ambient temperature. Owing to the temperature limits of the measurement equipment and control electronics, the highest ambient temperature that could be reached in this study was 40 ^\circ C. Nevertheless, this is high enough to give information about the short-circuit operation temperature dependence of the device.

4.4 Analysis of the simulation and measurement results

The results of Model1 and Model2 are compared with the experimental results and figures where the simulated voltage and current waveforms are presented with experimental waveforms. For example, in a design process of an electrical drive, the most interesting waveforms are the collector-emitter voltage $V_{CE}$, the collector current $I_C$, and the gate-emitter voltage $V_{GE}$, because they basically define how good a design is from the perspective of short-circuit operation. Even though a direct comparison of the waveforms provides a general overview of the accuracy of the simulation model, it is necessary to compare the simulation and experimental results by using specific quantities derived from the waveforms. In this study, a comparison is made by using the nine quantities presented below.
4 Experimental results and simulation model verification

- Maximum collector-emitter voltage, $V_{CE,\text{max}}$
- Maximum collector current, $I_{C,\text{max}}$
- Turn-off collector current, $I_{C,\text{knee}}$
- Maximum gate-emitter voltage $V_{GE,\text{max}}$
- Short-circuit pulse energy, $E_{SC}$
- Collector current rise time, $t_r$
- Gradient of the collector current rise, $di/dt_{\text{rise}}$
- Collector current fall time, $t_f$
- Gradient of the collector current fall, $di/dt_{\text{fall}}$

$V_{CE,\text{max}}$ is the maximum collector-emitter voltage occurring at a short-circuit turn-off. In practical applications, this value should not exceed the maximum collector-emitter voltage defined in the component datasheet, as exceeding of this value may cause an avalanche breakdown of the component. In a comparison of simulation/experimental results, it measures how well the simulation model estimates the real inductance and current $di/dt$ at a turn-off.

$I_{C,\text{max}}$ describes the maximum collector current at the beginning of a short-circuit pulse. A high collector current may trigger a current filamentation process in the IGBT, which may cause a device failure; the phenomenon of current filamentation is discussed for example in (Basler, 2014). In a comparison of simulation/experimental results, this measures how well the simulation model output characteristics correspond to the DUT.

$I_{C,\text{knee}}$ is the collector current at the moment when a short-circuit turn-off is initiated. In real applications there are no destructive phenomena caused only by current at a turn-off; nevertheless, in a comparison of simulation/experimental results, it gives an estimate of how well the model describes the self-heating effect during a short-circuit pulse.

$V_{GE,\text{max}}$ is the maximum gate-emitter voltage, and in the short-circuit Type I, it is normally located close to $I_{C,\text{max}}$. If $V_{GE,\text{max}}$ exceeds the maximum gate-emitter voltage defined in the component datasheet, it may cause a gate oxide breakdown and a device failure; however, it is not normally the reason for device failures in the short-circuit Type I (if there are e.g. no gate voltage oscillations). In a comparison of simulation/experimental results, it describes how well the collector-gate capacitance $C_{CG}$ and circuit inductances are modelled in a simulation model, as the gate-side and main current path are coupled through $C_{CG}$.

$E_{SC}$ is the total short-circuit pulse energy. A device failure may occur if $E_{SC}$ exceeds the device-specific critical energy as presented in (Lefebvre et al., 2005). In the short-circuit Type I, $V_{CE}$ stays relatively constant during a short-circuit pulse, and thus, in this case $E_{SC}$ is mainly affected by the collector current waveform. Therefore, in a comparison of simulation/experimental results, it provides a measure for the overall accuracy of the collector current modelling. $E_{SC}$ is calculated by determining the instantaneous power
4.4 Analysis of the simulation and measurement results

loss for every time step of the short-circuit pulse and integrating it over the pulse time $t_{SC}$. Calculation is started when $I_C$ exceeds 5% of $I_{C,max}$ and ended when $I_C$ goes below 5% of $I_{C,max}$.

The last four parameters describe the DUT and model behaviour in transient states. The current rise time $t_r$ measures the time to reach the maximum short-circuit current. In this study, the rise time is determined as the time from 10% of $I_{C,max}$ to 90% of $I_{C,max}$. The slope of the current rise $dI/dt_{rise}$ is determined between the same collector current points as in the determination of the rise time.

The corresponding parameters for the short-circuit turn-off are the current fall time $t_f$ and the current gradient of the turn-off $dI/dt_{fall}$. The turn-off parameters are determined from 90% of $I_{C,knee}$ to 10% of $I_{C,knee}$.

In a comparison of simulation/experimental results, $t_r, dI/dt_{rise}, t_f,$ and $dI/dt_{fall}$ describe how well the simulation model input capacitances $C_{CG}$ and $C_{GE}$ correspond to the capacitances of the DUT.

The following colour coding is used in the figures if other information is not given:

- Orange: Simulation result from Model1
- Purple: Simulation result from Model2 (Ansys model)
- Green: Measurement

In the following sections, the measured waveforms in the figures are filtered with a 5-point moving average filter to reduce measurement noise. However, the short-circuit parameters presented above are calculated from the waveforms that are filtered with a larger number of points in the moving average filter to ensure that the automatic calculation of parameters is reliable, and it is not affected by measurement noise. The number of points used for the moving average filtering $K_f$ for the measured waveforms from where the short-circuit parameters are calculated is as follows:

- $V_{CE}$: $K_f = 50$
- $I_C$: $K_f = 30$
- $V_{GE}$: $K_f = 30$

Because of the strong filtering, the presented parameter values may differ slightly from the values that can be read directly from the waveform figures.

4.4.1 Operation in the normal collector-emitter voltage range

The purpose of this section is to give an overview of the behaviour of the simulation models and their results close to the nominal operation voltage. The simulation results are then compared with the measurements, and differences are analysed. The operating point
voltage $V_{\text{DC}}$ is varied in a limited range (from 650 V to 750 V) to give an idea of how the voltage changes the behaviour of the models and how it affects the measurement results. A wider voltage range will be investigated in the next section. The results are shown for two values of $R_{\text{g,off}}$ (4.7 $\Omega$ and 10 $\Omega$) and for a short-circuit pulse length $t_{\text{SC}} = 5 \mu$s. The simulations and measurements are performed at room temperature.

The simulated and measured $V_{\text{CE}}$ waveforms are presented in Figure 4-9 and Figure 4-10. The DC voltage level $V_{\text{DC}}$ is 750 V, the pulse length $t_{\text{SC}}$ is 5 $\mu$s, and the gate turn-off resistor $R_{\text{g,off}}$ is 10 $\Omega$. A short-circuit pulse is triggered at 2.8 $\mu$s when $V_{\text{GE}}$ starts to rise as presented in Figure 4-13 and Figure 4-14. After $V_{\text{GE}}$ has reached the threshold voltage $V_{\text{TH}}$, $I_C$ starts to rise, and as a result of finite inductances in the circuit, $V_{\text{CE}}$ starts to decrease. In Figure 4-9, the simulated $V_{\text{CE}}$ starts to decrease at the same time instant as the measured value, and thus, it can be assumed that the delay in Model1 corresponds well with the real test setup. However, the amplitude of the drop in the simulated $V_{\text{CE}}$ is not as steep as in the measured $V_{\text{CE}}$. The voltage drop can be calculated by Eq. (4.1).

$$\Delta V = L_\sigma \cdot \frac{dI_C}{dt},$$

where $L_\sigma$ is the parasitic commutation inductance and $dI_C/dt$ is the current gradient.

An erroneous voltage drop can be caused for two reasons. First, the circuit inductance is not modelled correctly, or second, the current gradient is not as high as in the real setup. The collector current waveform is presented in Figure 4-11, which shows that the current gradient at the beginning of the current rise is lower in the simulation than in the experimental result. Consequently, the $V_{\text{CE}}$ voltage drop in the simulation is lower than in the experimental result.
Another obvious difference between the simulated and measured $V_{CE}$ waveforms is the amplitude of the voltage spike at the turn-off. The measured voltage spike has a higher amplitude and the voltage rise is faster compared with the simulated ones. Based on Eq. (4.1), the reason for an increase in $V_{CE}$ at the turn-off in the measurement (or simulation) circuit is the parasitic inductance with the collector current gradient. Figure 4-11 shows that $\frac{di_C}{dt}$ at the turn-off is lower in the simulation than in the measurement, which causes a difference in the $V_{CE}$ voltage spikes in Figure 4-9.

The $V_{CE}$ oscillation after the turn-off in Figure 4-9 is a consequence of the resonance of the snubber capacitor and busbar inductances. The amplitude and frequency of the resonance in the simulation corresponds quite well with the measurement, but as a result of the slower turn-off there is a phase shift between the results.
When comparing the simulated $V_{CE}$ waveforms in Figure 4-9 and Figure 4-10, it can be seen that the delay in Model2 is not modelled as accurately as in Model1. Furthermore, as a result of the slower current rise in Model2, the amplitude of the $V_{CE}$ voltage drop is lower than with Model1.

Collector current waveforms during a short-circuit are presented in Figure 4-11 and Figure 4-12. The pulse shape in the simulation of Model1 (Figure 4-11) is very similar to the measurement, but there are slight differences in the current rise and fall and in the maximum amplitude of the current. The Model1 capacitances are not exactly the same as in a real IGBT, which causes a difference in the current gradients. Model1 executes $I_C$ according to the $I_C$–$V_{GE}$ output characteristics, and thus, the reason for an incorrect $I_{C,max}$ is inaccurate output characteristics or inaccurate modelling of $V_{GE}$.

At the end of the short-circuit pulse, the current gradient of the measured $I_C$ decreases drastically because of the charge stored in the component, and it is called the IGBT tail current. This charge can decrease only by a recombination in the semiconductor; the reduction rate is determined by the carrier lifetime of the semiconductor. Owing to the simplicity of the models, the behavioural IGBT models are not directly based on semiconductor physics, and usually all the phenomena originating from specific physical semiconductor properties are excluded from the models. Because the tail current does not have a significant effect on the IGBT short-circuit operation, this phenomenon is excluded also from Model1.
From the short-circuit current pulse simulated with Model2 (Figure 4-12), it can be seen that the shape of the pulse does not follow the measured pulse shape. As mentioned above, the collector current starts to rise earlier than in the measurement, but also the maximum amplitude of the current pulse $I_{C,max}$ differs from the measurement. In addition, the region around the maximum current is flatter than in the measurement. Another difference is the slower current gradient at the turn-off. One very interesting phenomenon in the Model2 simulations is the current oscillation after the IGBT has turned off. Because Model2 was made by Ansys and there is no comprehensive information available about its internal structure, it is difficult to say why the current behaves like this. However, a similar oscillation is visible in the $V_{GE}$ waveform in Figure 4-14. In principle, $I_C$ follows $V_{GE}$ according to the transfer characteristics, and thus, current oscillation may be caused by $V_{GE}$ oscillation. A similar oscillation cannot be seen in the measured current waveform or the waveform simulated with Model1. The measured $V_{GE}$ has an oscillatory phenomenon after turn-off, but the amplitude of the oscillation is much lower than in the results with Model2.
When comparing the $V_{GE}$ waveforms from Model1 and Model2 with the measurements, it can be observed that $V_{GE}$ in Model1 decreases slower than in Model2 or in the experimental results. On the other hand, $V_{GE}$ in the Model2 simulation decreases faster than in the measurement. Furthermore, the maximum gate-emitter voltage $V_{GE,max}$ is highest in Model1 simulation, but also Model2 has a higher $V_{GE,max}$ compared with the measurement. In Model1, the gate side is modelled in a very simple way as the gate driver effects are outside the scope of this doctoral dissertation. The IGBT gate side is modelled with two capacitors; $C_{CG}$ and $C_{GE}$ as presented in Section 3.1 and Figure 3-2, and the gate driver with a gate voltage source and $R_{g,on}$ and $R_{g,off}$ separated by diodes (Section 3.1).
4.4 Analysis of the simulation and measurement results

Figure 4-13 Measured and simulated (Model1) $V_{GE}$ waveforms, $V_{DC} = 750 \, V$, $R_{g,off} = 10 \, \Omega$.

Figure 4-14 Measured and simulated (Model2) $V_{GE}$ waveforms, $V_{DC} = 750 \, V$, $R_{g,off} = 10 \, \Omega$.

Overall, the shape of the $V_{GE}$ waveform in Model2 is closer to the measurement than in Model1. The situation is very different when compared with the $V_{CE}$ and $I_C$ waveforms, because in that case Model1 gives better results.
A comparison of the results with $V_{\text{DC}} = 650$ V is presented in Figure 4-15–Figure 4-20. The general observations of the waveform shapes discussed above are valid also here, only the values of the compared parameters are changed because of the different $V_{\text{DC}}$.

**Figure 4-15** Measured and simulated (Model1) $V_{\text{CE}}$ waveforms, $V_{\text{DC}} = 650$ V, $R_{g,\text{off}} = 10$ Ω.

**Figure 4-16** Measured and simulated (Model2) $V_{\text{CE}}$ waveforms, $V_{\text{DC}} = 650$ V, $R_{g,\text{off}} = 10$ Ω.
4.4 Analysis of the simulation and measurement results

Figure 4-17 Measured and simulated (Model1) $I_C$ waveforms, $V_{DC} = 650$ V, $R_{g,off} = 10$ Ω.

Figure 4-18 Measured and simulated (Model2) $I_C$ waveforms, $V_{DC} = 650$ V, $R_{g,off} = 10$ Ω.
The compared short-circuit parameters introduced in Section 4.4 are presented in Figure 4-21 for $V_{DC} = 650 \text{ V} - 750 \text{ V}$ and $R_{g,off} = 10 \Omega$, and for the pulse length $t_{SC} = 5 \mu s$. As can be seen, $V_{CE,max}$ behaves very linearly as a function of DC voltage, that is, when $V_{DC}$ is increased by 100 V, the amplitude of the voltage spike at the turn-off increases by 100 V. Both simulation models, Model1 and Model2, show a similar linear behaviour even
4.4 Analysis of the simulation and measurement results

though the difference between Model2 and the measurement is slightly larger than between Model1 and the measurement, as shown in Figure 4-21a.

The measurement of $I_{C, \text{max}}$ in Figure 4-21b has also an increasing trend as $V_{DC}$ increases. This is due to an increase in the IGBT bipolar current gain as discussed in Section 2.2.3. The results of Model1 show a similar behaviour, but the increase rate is slower compared with the measurement, whereas Model2 has a slightly decreasing behaviour when $V_{DC}$ is increased. The absolute difference in $I_{C, \text{max}}$ between Model1 and the experimental result is greater than between Model2 and the measurement at $V_{DC} = 650$ V, but the situation changes at higher DC voltages.

A comparison of $I_{C, \text{knee}}$ (in Figure 4-21c) shows quite good results for both simulation models, but there is a difference in the $I_{C, \text{knee}}$ behaviour as a function of DC voltage. The measured value of $I_{C, \text{knee}}$ increases with increasing voltages, but decreases slightly in the Model1 simulations. With short short-circuit pulse lengths ($t_{SC}$ is $5 \mu s$), the current decrease after $I_{C, \text{max}}$ is mainly caused by a decrease in $V_{GE}$, which is due to the main and gate-side circuit coupling through $C_{CG}$. Therefore, it seems that the effect of $C_{CG}$ as a function of voltage is not exactly modelled in Model1. However, the value of $I_{C, \text{knee}}$ is manually recorded from the results, because it is difficult to automatically determine the collector current knee point as the shape of the knee point changes when the operating point is changed, and the overall collector current knee point is very smooth. Manual determination causes some variation to the point where $I_{C, \text{knee}}$ is recorded, and therefore, it is better to compare the change in the trends of $I_{C, \text{knee}}$ and its difference compared with the measurement than single results in a specific operating point. The $I_{C, \text{knee}}$ behaviour in Model2 simulations is similar to the measurement, but the increase rate as a function of voltage is slightly lower.

The behaviour of $V_{GE, \text{max}}$ is illustrated in Figure 4-21d. $V_{GE, \text{max}}$ in the figure seems to be fairly constant in the measurement and simulations, but in reality, the measured $V_{GE, \text{max}}$ increases with an increasing $V_{DC}$ as presented in Table 4-1, where the exact numerical values of the compared parameters are given. In this case, both the simulation models show a distinct behaviour compared with the experiments.

The simulated and measured short-circuit pulse energies $E_{SC}$ increase when $V_{DC}$ is changed from 650 V to 750 V as presented in Figure 4-21e. This is an obvious phenomenon as $E_{SC}$ is calculated by using the pulse length and the instantaneous power $P_{SC}$ according to Eq. (4.2).

$$E_{SC} = \int P_{SC} dt = \int i_c \cdot V_{CE} dt$$ (4.2)

In the short-circuit Type I, $V_{CE}$ is mainly defined by $V_{DC}$ (excluding the $V_{CE}$ variation caused by voltage drops across parasitic inductances), and thus, an increase in $V_{DC}$ causes an increase in $V_{CE}$ and consequently, an increase in $E_{SC}$. The increase rate of $E_{SC}$ in both simulation models is smaller than in the measurement, and thereby, the absolute
difference between the simulations and the measurement is smaller when the voltage is increased. Furthermore, the difference between the results of Model1 and the measurement is smaller than the difference with Model2. This is mainly due to the collector current modelling (Figure 4-11, Figure 4-12, Figure 4-17, and Figure 4-18), where Model1 shows a better accuracy.

The collector current rise and fall states are compared in Figure 4-21f–i. As could be seen in the $I_C$ waveform figures above, the turn-on phase is much faster and the turn-off phase much slower in the results of Model2 compared with Model1 or the measurements. The trend in $t_{rise}$ is similar in all the results; the rise time decreases when $V_{DC}$ is increased, as can be seen in Figure 4-21f. Furthermore, $\frac{di}{drise}$ in Figure 4-21g increases, but the rate in the Model2 results is much lower than in Model1 or in the measurement.

In a comparison of the fall time $t_{fall}$, in Figure 4-21h, the trends of all the results behave differently. When $V_{DC}$ is increased, $t_{fall}$ from Model1 decreases, $t_{fall}$ from Model2 stays relatively constant, and $t_{fall}$ in the measurements increases. A similar behaviour of trends can be observed with $\frac{di}{dfall}$ in Figure 4-21i.
4.4 Analysis of the simulation and measurement results

Figure 4-21 Parameter comparison for $V_{DC} = 650\text{ V} - 750\text{ V}$ and $R_{g,\text{off}} = 10\ \Omega$. Orange: Model1, purple: Model2, and green: measurement.
Data used for \( V_{\text{DC}} = 750 \, \text{V} \) and 650 V in Figure 4-21 are presented in numerical form in Table 4-1. The difference percentage is calculated by dividing the absolute difference by the measured value. To keep the comparison of the simulation models straightforward, certain limits for the difference percentages have to be selected. In this study, the difference percentage is considered ‘accurate’ if it is below 5 %, ‘acceptable’ if it is below 10 %, ‘neutral’ if it is below 50 %, and ‘not acceptable’ if it is above 50 %.

Table 4-1 Comparison of the short-circuit parameters for \( V_{\text{DC}} = 750 \, \text{V} \) and 650 V with \( R_{\text{off}} = 10 \, \Omega \).

<table>
<thead>
<tr>
<th>( V_{\text{DC}} )</th>
<th>( V_{\text{CE,max}} )</th>
<th>( I_{C,max} )</th>
<th>( V_{GE,max} )</th>
<th>( E_{SC} )</th>
<th>( t_{\text{rise}} )</th>
<th>( d_i/dt_{\text{rise}} )</th>
<th>( t_{\text{fall}} )</th>
<th>( d_i/dt_{\text{fall}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>750 V</td>
<td>894.80</td>
<td>9054.30</td>
<td>18.01</td>
<td>23.18</td>
<td>1.76</td>
<td>4.14E+09</td>
<td>0.57</td>
<td>1.02E+10</td>
</tr>
<tr>
<td>Model1</td>
<td>879.02</td>
<td>8240.90</td>
<td>17.17</td>
<td>24.90</td>
<td>1.37</td>
<td>4.79E+09</td>
<td>0.92</td>
<td>6.35E+09</td>
</tr>
<tr>
<td>Meas.</td>
<td>910.93</td>
<td>8811.90</td>
<td>16.19</td>
<td>22.25</td>
<td>1.89</td>
<td>3.72E+09</td>
<td>0.50</td>
<td>1.18E+10</td>
</tr>
<tr>
<td>Model2</td>
<td>795.46</td>
<td>8994.50</td>
<td>18.12</td>
<td>19.91</td>
<td>0.53</td>
<td>4.01E+09</td>
<td>0.59</td>
<td>1.07E+09</td>
</tr>
<tr>
<td>Meas.</td>
<td>777.84</td>
<td>8273.10</td>
<td>17.24</td>
<td>21.53</td>
<td>0.13</td>
<td>4.77E+09</td>
<td>0.91</td>
<td>1.01E+10</td>
</tr>
<tr>
<td>650 V</td>
<td>811.20</td>
<td>8549.50</td>
<td>16.10</td>
<td>18.42</td>
<td>1.19</td>
<td>3.54E+09</td>
<td>0.48</td>
<td>5.97E+09</td>
</tr>
<tr>
<td>Model1</td>
<td>811.20</td>
<td>8549.50</td>
<td>16.10</td>
<td>18.42</td>
<td>1.19</td>
<td>3.54E+09</td>
<td>0.48</td>
<td>5.97E+09</td>
</tr>
<tr>
<td>Meas.</td>
<td>811.20</td>
<td>8549.50</td>
<td>16.10</td>
<td>18.42</td>
<td>1.19</td>
<td>3.54E+09</td>
<td>0.48</td>
<td>5.97E+09</td>
</tr>
</tbody>
</table>
The difference percentages for Model1 are quite low in $V_{\text{CE,max}}$, $I_{\text{C,max}}$, and $I_{\text{C,knee}}$, and therefore, in general, the voltage across the component and the current through it are modelled with a good accuracy. However, $V_{\text{GE,max}}$ has a two-digit difference percentage at both voltages (11.24 % and 12.55 %, respectively), which is much worse than with the previous parameters.

The percentages for Model2 are mainly somewhat higher in $V_{\text{CE,max}}$, $I_{\text{C,max}}$, and $I_{\text{C,knee}}$ compared with Model1, but still within acceptable limits when considering the model used as a design tool. The $V_{\text{GE,max}}$ difference percentage for Model2 is lower than for Model1, which was already seen above in the $V_{\text{GE,max}}$ waveforms (Figure 4-14 and Figure 4-20).

If the critical energy $E_c$ for a certain device is known, the simulation model can be used to estimate whether the short-circuit pulse energy of a certain design is below $E_c$ or whether it is possibly exceeded. In this kind of investigation, the accuracy of $E_{\text{SC}}$ is highly relevant. The $E_{\text{SC}}$ difference percentages for Model1 are 4.18 % at 750 V and 8.10 % at 650 V, which are not as accurate as for $V_{\text{CE}}$ and $I_{\text{C}}$ but better than for Model2. For Model2, the percentages are 11.91 % and 16.93 %. Here, the difference between the models is mainly due to the more accurate $I_{\text{C}}$ modelling in Model1.

Probably the most difficult part of IGBT modelling with the behavioural models is modelling of the transient state as it requires accurate modelling of the IGBT capacitances, which have a very non-linear dependence of several operating point variables. The difference percentages of the transient state parameters ($t_{\text{rise}}$, $di/dt_{\text{rise}}$, $t_{\text{fall}}$, and $di/dt_{\text{fall}}$) are larger compared with the previous parameters for both the simulation models, which proves that simple capacitance modelling methods are difficult to use if a very high transient state accuracy is required.

The only transient state parameter whose accuracy in this operating point range is in the category of acceptable is $t_{\text{rise}}$ modelled with Model1. All the other transient state parameters (excluding $t_{\text{fall}}$ of Model2) for both the simulation models are in the neutral category, meaning that the difference percentage is from 10 % to 50 %. The highest transient state difference percentage for Model1 is 22.08 % ($t_{\text{fall}}$ at 650 V). The largest percentages for Model2 can be found from $t_{\text{fall}}$, where it is 81.37 % at 750 V and 90.10 % at 650 V. These values fall into the category of not acceptable.

**Results with $R_{\text{g,off}} = 4.7 \ \Omega$**

Even though the comparison of the simulation and measurement results as a function of $R_{\text{g,off}}$ will be discussed in a section of its own later in this study (Section 4.4.3), some results with $R_{\text{g,off}} = 4.7 \ \Omega$ in a limited $V_{\text{DC}}$ range are given below. Figure 4-22 presents the measured and simulated $V_{\text{CE}}$ waveforms for Model1 with $R_{\text{g,off}} = 4.7 \ \Omega$ at $V_{\text{DC}} = 750$ V. If the figure is compared with Figure 4-9, where $R_{\text{g,off}} = 10 \ \Omega$, it can be seen that the amplitude of the voltage spike is now closer to the measurement. In addition, the increase
rate of $V_{CE}$ at the turn-off is faster than with a higher $R_{g,off}$. The same applies to Model2 (Figure 4-23), even though the turn-off is still slower than in the Model1 results.

Figure 4-22 Measured and simulated (Model1) $V_{CE}$ waveforms, $V_{DC} = 750$ V, $R_{g,off} = 4.7$ Ω.

Figure 4-23 Measured and simulated (Model2) $V_{CE}$ waveforms, $V_{DC} = 750$ V, $R_{g,off} = 4.7$ Ω.

Figure 4-24 and Figure 4-25 show the measured and simulated waveforms of $I_C$ with $R_{g,off} = 4.7$ Ω. In general, the shape of the current pulse is similar to the results where
4.4 Analysis of the simulation and measurement results

$R_{g,\text{off}} = 10 \ \Omega$, but the difference between the simulation and the measurement in $I_{C,\text{max}}$ is now larger than in Figure 4-11. The increased collector current at the beginning of the short-circuit pulse in the Type I short-circuit is caused by $dV_{CE}/dt$, which produces a current through $C_{CG}$, which then increases $V_{GE}$. Consequently, a larger difference in $I_{C,\text{max}}$ with a lower $R_{g,\text{off}}$ indicates that this $C_{CG}$–$V_{GE}$ interaction is not precisely modelled.

![Figure 4-24 Measured and simulated (Model1) $I_C$ waveforms, $V_{DC} = 750$ V, $R_{g,\text{off}} = 4.7 \ \Omega$.](image)

A similar behaviour can also be seen for Model2, because $I_{C,\text{max}}$ in Figure 4-25 is greater than in Figure 4-12.

Compared with the case where $R_{g,\text{off}} = 10 \ \Omega$, $t_{\text{fall}}$ is now more accurately modelled with Model1 (the difference percentage is 0.00 % at 750 V and 6.35 % at 650 V), whereas Model2 gives more inaccurate results (the difference percentage is 185.07 % at 750 V and 197.10 % at 650 V). Commonly, behavioural models can be optimized to a specific operating point, where the model gives very precise results, but the accuracy decreases when the operating point is changed. In this study, the coefficient $K_{CCG}$ (Eq. (2.39)), which modifies $C_{CG}$ as a function of $I_C$, is optimized to give accurate results with $R_{g,\text{off}} = 4.7 \ \Omega$ at $V_{DC} = 750$ V. This is the reason why the percentage of error of $t_{\text{fall}}$ is 0 in this operating point.
Simulated and measured $V_{GE}$ waveforms with $R_{g,\text{off}} = 4.7$ Ω are presented in Figure 4-26 and Figure 4-27. Both Model1 and Model2 show a faster $V_{GE}$ rise and fall compared with Figure 4-13 and Figure 4-14, as can be expected based on theory. The gate-emitter waveforms are not analysed in detail (e.g. $t_{\text{rise}}$, $t_{\text{fall}}$, percentages of error) because the gate driver and gate-side operation are excluded from this doctoral dissertation. However, $V_{GE}$ waveforms are analysed at a general level to get some idea of the accuracy of the gate-side modelling.

$V_{GE,\text{max}}$ of Model1 and Model2 is still above the measured value, even though the difference is not as high as with the 10 Ω gate turn-off resistor. The difference percentages at 750 V are 7.63 % for Model1 and 4.59 % for Model2, which means that the modelling accuracy of $V_{GE}$ with Model2 is very good from the perspective of the maximum voltage amplitude. Nevertheless, when looking at the $V_{GE}$ waveform after the turn-off, the voltage level goes very low, even below -12 V, which is defined as the gate driver turn-off voltage.
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Figure 4-26 Measured and simulated (Model1) $V_{GE}$ waveforms, $V_{DC} = 750$ V, $R_{g,off} = 4.7$ Ω.

Figure 4-27 Measured and simulated (Model2) $V_{GE}$ waveforms, $V_{DC} = 750$ V, $R_{g,off} = 4.7$ Ω.

Figure 4-28 presents the short-circuit parameters for $R_{g,off} = 4.7$ Ω and $V_{DC}$ is 650 V–750 V. In general, the trends in the parameters remain the same as in the case with $R_{g,off}$ of 10 Ω (Figure 4-21), but the behaviour at $I_{C,\text{max}}$ and $I_{C,knee}$ is changed. With $R_{g,off} = 10$ Ω in Figure 4-21b and c, Model1 gives better results, but with $R_{g,off} = 4.7$ Ω in Figure 4-28b and c, Model2 is more accurate.
The information given in Figure 4-28 is presented in numerical form in Table 4-2. When comparing the percentages of error of $E_{SC}$ with Table 4-1, Model 1 is now more accurate, whereas the difference percentages of Model 2 increase. The results of the transient state parameters $t_{rise}$, $di/dt_{rise}$, $t_{fall}$ and $di/dt_{fall}$ show a similar behaviour to the larger gate resistor, that is, Model 1 is more accurate than Model 2, yet the percentages are as small as for $V_{CE,max}$, $I_{C,max}$, $I_{C,knee}$, and $E_{SC}$. 
Figure 4.28 Parameter comparison for $V_{\text{DC}} = 650 \text{ V}–750 \text{ V}$ and $R_{g,\text{off}} = 4.7 \ \Omega$. Orange: Model1, purple: Model2, and green: measurement.
4 Experimental results and simulation model verification

Table 4.2 Comparison of the short-circuit parameters for $V_{DC} = 750$ V and 650 V with $R_{g,off} = 4.7$ Ω.

<table>
<thead>
<tr>
<th>$V_{DC}$</th>
<th>750 V</th>
<th>650 V</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Model1</td>
<td>Model2</td>
</tr>
<tr>
<td>$V_{CE,max}$ [V]</td>
<td>930.05</td>
<td>898.75</td>
</tr>
<tr>
<td>Abs. diff. [V]</td>
<td>14.45</td>
<td>45.75</td>
</tr>
<tr>
<td>Diff. %</td>
<td>1.53 %</td>
<td>4.84 %</td>
</tr>
<tr>
<td>$I_{C,max}$ [A]</td>
<td>8493.70</td>
<td>7983.30</td>
</tr>
<tr>
<td>Abs. diff. [A]</td>
<td>581.40</td>
<td>71.00</td>
</tr>
<tr>
<td>Diff. %</td>
<td>7.35 %</td>
<td>0.90 %</td>
</tr>
<tr>
<td>$V_{GE,max}$ [V]</td>
<td>17.30</td>
<td>16.81</td>
</tr>
<tr>
<td>Abs. diff. [V]</td>
<td>1.23</td>
<td>0.74</td>
</tr>
<tr>
<td>Diff. %</td>
<td>7.63 %</td>
<td>4.59 %</td>
</tr>
<tr>
<td>$E_{SC}$ [J]</td>
<td>20.36</td>
<td>22.44</td>
</tr>
<tr>
<td>Abs. diff. [J]</td>
<td>0.71</td>
<td>0.74</td>
</tr>
<tr>
<td>Diff. %</td>
<td>3.62 %</td>
<td>4.59 %</td>
</tr>
<tr>
<td>$t_{rise}$ [µs]</td>
<td>1.61</td>
<td>1.33</td>
</tr>
<tr>
<td>Abs. diff. [µs]</td>
<td>0.12</td>
<td>0.40</td>
</tr>
<tr>
<td>Diff. %</td>
<td>6.78 %</td>
<td>22.91 %</td>
</tr>
<tr>
<td>$d_i/dt_{rise}$ [A/s]</td>
<td>4.26E+09</td>
<td>4.81E+09</td>
</tr>
<tr>
<td>Abs. diff. [A/s]</td>
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<td>1.14E+09</td>
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<tr>
<td>Diff. %</td>
<td>16.18 %</td>
<td>31.07 %</td>
</tr>
<tr>
<td>$t_{fall}$ [µs]</td>
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<td>0.82</td>
</tr>
<tr>
<td>Abs. diff. [µs]</td>
<td>0.00</td>
<td>0.53</td>
</tr>
<tr>
<td>Diff. %</td>
<td>0.00 %</td>
<td>185.07 %</td>
</tr>
<tr>
<td>$d_i/dt_{fall}$ [A/s]</td>
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<td>6.28E+09</td>
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<tr>
<td>Abs. diff. [A/s]</td>
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<td>1.14E+10</td>
</tr>
<tr>
<td>Diff. %</td>
<td>2.26 %</td>
<td>64.40 %</td>
</tr>
</tbody>
</table>

4.4.2 Operation in a wide collector-emitter voltage range

In this section, the behaviour of the simulation and measurement results is investigated as a function of $V_{DC}$ variation. The objective is to show how the simulation models behave when the operating point voltage is far from the nominal and to show what phenomena a low voltage can produce to the operation of a real IGBT. The theory behind low-voltage operation of the IGBT was discussed in Section 2.2.7. The results are shown for two $R_{g,off}$ values (10 Ω and 4.7 Ω), and the voltage range for $R_{g,off} = 10$ Ω is from 150 V to 750 V and for $R_{g,off} = 4.7$ Ω from 350 V to 750 V. Different voltage ranges are chosen because
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in the very low voltage range (< 350 V) DUT starts to oscillate, and because of their simple structure, the simulation models cannot describe the oscillation. Thus, it is not reasonable to compare all the results in that voltage range. The ambient temperature $T_a$ is 25 °C in the results with $R_{g,off} = 10 \, \Omega$, and in the results with $R_{g,off} = 4.7 \, \Omega$, $T_a = 30 \, ^\circ C$.

As discussed in Sections 2.2.3 and 2.2.7, the operation voltage has a significant effect on the IGBT short-circuit behaviour. Some of the phenomena arising from a change in $V_{CE}$ are very difficult or impossible to model without complex device models relying on semiconductor physics. One example is the $V_{GE}$ oscillation observed in (Wu et al., 2015) and (Treek et al., 2018). It originates from the physical properties of the IGBT chip as presented in (Reigosa et al., 2019) and (Kikuchi et al., 2018), and therefore, modelling of this effect requires more complex and detailed models than is achievable within the scope of this study. In the experimental tests of this doctoral dissertation, oscillation is observed in the voltage range $V_{DC} = 200 \, V – 300 \, V$. The oscillation is triggered at 200 V, and the phenomenon is amplified towards higher voltages until it disappears at 350 V. A strong oscillation in $V_{GE}$ also affects for example $I_C$, and consequently, the effect of oscillation can be seen in the short-circuit parameters in addition to $V_{GE,max}$.

According to (Reigosa et al., 2018), the origin of oscillation is the time-varying $C_{CG}$. Modelling of this variation requires an IGBT chip model that includes information of its physical structure and the semiconductor material properties. In simplified behavioural models, such a chip model is not used, and thus, it cannot be assumed that behavioural models can model the $V_{GE}$ oscillation depending on the applied voltage.

However, it is important that simulation results are compared with experiments also in the full voltage range to understand the limitations of the model. Moreover, the results of this section can be used to compare Model1 and Model2. The detailed structure of Model2 is not known, and therefore, a comparison of results between Model1 and Model2 can give information of how well the structure of Model1 corresponds to the structure of Model2.

As an oscillation that occurs between 200 V and 300 V cannot be described without complex simulation models, the full voltage range from 150 V to 750 V is analysed only for one gate turn-off resistor value ($R_{g,off} = 10 \, \Omega$). The voltage range from 350 V to 750 V (where a $V_{GE}$ oscillation does not occur) is also analysed with a lower turn-off resistor value ($R_{g,off} = 4.7 \, \Omega$) to allow investigation of the effect of the applied voltage as a function of $R_{g,off}$.

Results with $R_{g,off} = 10 \, \Omega$ at $V_{DC} = 150 \, V – 750 \, V$

The measurement and simulation waveforms at $V_{DC} = 200 \, V$ are presented in Figure 4-29–Figure 4-34. In the measured $V_{CE}$ waveform (e.g. in Figure 4-29), the first obvious difference compared with the voltage range $V_{DC} = 650 \, V – 750 \, V$ is that $V_{CE}$ starts to oscillate at the end of the short-circuit pulse. The $V_{CE}$ oscillation is triggered by a strong $V_{GE}$ oscillation, shown in Figure 4-33. The maximum $V_{GE}$ value read from Figure 4-33
exceeds 35 V, whereas the automatically calculated $V_{GE,\text{max}} = 32.54$ V. The reason for the difference is the different filtering of the waveform in the figure and in the parameter calculation as discussed in Section 4.4. At the beginning of the short-circuit pulse, the simulated $V_{CE}$ starts to decrease earlier than the measured one. At lower voltages this holds true for both the simulation models; see Figure 4-29 for Model1 and Figure 4-30 for Model2. In the voltage range $V_{DC} = 650$ V–750 V, only Model2 shows a similar behaviour, whereas there is no significant delay error in the Model1 simulations. The reason for an error in the delay can be found from the $V_{GE}$ waveforms (Figure 4-33 and Figure 4-34), where the simulated $V_{GE}$ reaches the threshold value $V_{GE,\text{th}}$ earlier than the measurement. As soon as $V_{GE}$ reaches $V_{GE,\text{th}}$, $I_C$ starts to rise and $V_{CE}$ starts to decrease. There is also a significant difference in the saturation behaviour in the lower voltage range compared with the operation close to the normal operating voltage. During 5 µs, the short-circuit pulse $I_C$ that is simulated with Model1 does not saturate but is turned off directly from $I_{C,\text{max}}$ as presented in Figure 4-31. The same phenomenon is visible in the $V_{CE}$ waveform in Figure 4-29, where $V_{CE}$ does not reach $V_{DC}$ before the turn-off point.

![Image](image.png)

Figure 4-29 Measured and simulated (Model1) $V_{CE}$ waveforms, $V_{DC} = 200$ V, $R_{\text{off}} = 10$ Ω.

As was discussed in Section 4.4.1, the turn-off state of Model1 and Model2 is slower compared with the measurement. For Model1, this phenomenon is significantly amplified when the $V_{DC}$ is lowered further from 750 V, to which the model is optimized. Thus, it seems that the voltage dependence of the capacitance $C_{CG}$ is not exactly correct. When considering Figure 4-30, where the $V_{CE}$ waveform is simulated with Model2, a similar behaviour with Model1 can be observed, but the effect of $V_{DC}$ is not as significant as for Model1.
However, a straightforward answer cannot be given as to why the turn-off state becomes more inaccurate when $V_{DC}$ is decreased. The turn-off state is also affected by $I_C$, where the simulations show more inaccurate results for $V_{DC} = 200$ V than for $V_{DC} = 750$ V. As shown by the theoretical background presented in Sections 2.2.3 and 2.2.6, the short-circuit current behaviour as a function of voltage applied across an IGBT is a very complex phenomenon requiring in-depth information of semiconductor physics, and it is impossible to derive the required parameters from the information commonly given in commercially available datasheets. Furthermore, Model2 is more or less a black box for the user because its manual does not give comprehensive information about the model, and thus, it is extremely difficult to analyse the reasons why $V_{DC}$ affects its behaviour. Because the information required for the voltage dependence and calculation of the ambipolar current gain $\alpha_{PNP}$ is not available for Model1 either, the $I_C$ dependence of $V_{CE}$ is derived from the measurements. As presented in (Basler, 2014), this dependence is quite linear for the current saturation region as shown in Section 2.2.3. By applying this information, a single coefficient for the voltage dependence $K_{VCE}$ can be extracted from the measurement. For Model1, $K_{VCE}$ is 1.22. The short-circuit current voltage dependence is applied to the model as follows:

1. $I_C-V_{GE}$ curve from the datasheet is used to determine $I_C$ as a function of $V_{GE}$ at $V_{CE} = 20$ V
2. A linear coefficient for the voltage dependence is extracted from measurements where $V_{DC}$ is from 350 V to 750 V (measurements from lower voltages are excluded because of the $V_{GE}$ oscillation)
3. The coefficient is used to estimate how much $I_C$ changes when $V_{CE}$ is changed from 20 V to 750 V with the following result: $I_C$ at 750 V is 1.22 times $I_C$ at 20 V $\rightarrow K_{VCE} = 1.22$
4. $I_C$ values from point 1 are multiplied by $K_{VCE}$ to get $I_C-V_{GE}$ curves for $V_{CE} = 750$ V
5. $I_C-V_{GE}$ curves for $V_{CE} = 20$ V and $V_{CE} = 750$ V are inserted in the look-up table in Model1
6. $I_C-V_{GE}$ curves for $V_{CE} = 20$–750 V are assumed to behave linearly between the points $V_{CE} = 20$ V and $V_{CE} = 750$ V
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Figure 4-30 Measured and simulated (Model2) $V_{CE}$ waveforms, $V_{DC} = 200$ V, $R_{g,off} = 10$ Ω.

$I_{C,max}$ simulated with Model1 in Figure 4-31 is much higher than the measured value. Even though the target is to keep the model simple, there are several parameters that affect $I_C$. Therefore, it is very challenging to distinguish which parameter causes the difference in a current. A list of possible reasons for the error are given below:

1. Linear estimation of the transfer characteristics for values $V_{GE} > 12$ V is not correct, and thus, $I_{C,sat}$ at $V_{CE} = 20$ V is not correct
2. Linear voltage dependence of $I_{C,sat}$, that is estimated from the measurements is not correct
3. Estimation of the $C_{CG}$ voltage/current dependence is not correct, which causes an erroneous $V_{GE}$

The most probable reasons for the $I_C$ error in the lower voltage range are the second and third points on the list. First, the second point is considered. The theoretical background for $I_{C,sat}$ was discussed in Sections 2.2.3, where it was found that $I_{C,sat}$ does not change linearly as a function of voltage but there are two different gradients for $I_{C,sat}$ in the output characteristics. This is also clearly visible in Figure 2-10. Therefore, more erroneous $I_C$ waveforms can be expected for lower voltages if the current gradient in the output characteristics changes below a certain voltage.

Secondly, $C_{CG}$ in the third point on the list has a very strong non-linear behaviour depending on the operating point and the IGBT chip properties. In Model1, the $C_{CG}$ voltage dependence is modelled by Eq. (2.39), where $C_{CG}$ is assumed to change as a function of the square root of $V_{CE}$. This method is suitable for a rough estimate of the $C_{CG}$
4.4 Analysis of the simulation and measurement results

provided by the manufacturer, but it is likely that it cannot describe the $C_{CG}$ voltage dependence accurately in all operating points. Furthermore, as discussed in Section 2.2.6, $C_{CG}$ has also a current dependence, which is also applied in Model1. The idea of the $C_{CG}$ current dependence is presented in (Yang et al., 2015) and (Tominaga et al., 2011), where it is within the normal operating range of the IGBT. To the author’s knowledge, so far, the $C_{CG}$ current dependence in the IGBT short-circuit operation has not been investigated in the literature.

![Figure 4-31 Measured and simulated (Model1) $I_C$ waveforms, $V_{DC} = 200$ V, $R_{g,off} = 10$ Ω.](image)

The difference between the simulated and measured $I_C$ at low voltages increases also for Model2; see Figure 4-32. In addition to $I_{C,\text{max}}$, the current rise in the simulation starts much earlier and the rise/fall times differ greatly when compared with the measurement. Moreover, a similar oscillation phenomenon in $I_C$ can be seen at $V_{DC} = 200$ V as in the case of $V_{DC} = 650$ V–750 V.

The above-discussed $V_{GE}$ oscillation can be clearly seen also in the measured $I_C$ waveform. After $I_{C,\text{max}}$ at around 7 µs in Figure 4-32, $I_C$ starts to decrease, but because of the $V_{GE}$ oscillation it starts to rise again. In the measurements, the amplitude of the $V_{GE}$ oscillation is amplified when $V_{DC}$ is increased from 200 V, and consequently, also the rise in $I_C$ caused by oscillation is amplified. This can be seen in Figure 4-35 and Figure 4-36, where the short-circuit parameters $V_{GE,\text{max}}$, $I_{C,\text{max}}$, $I_{C,knee}$, $V_{GE,\text{max}}$, and $E_{SC}$ are presented for the voltage range $V_{DC} = 150$ V–750 V.
The oscillation disappears completely when $V_{DC}$ is increased to 350 V, which corresponds well with the theory and the experiments and numerical simulations for example in (Treek et al., 2018). A strong oscillation in $V_{GE}$ can be critical from the perspective of the short-circuit ruggedness of the IGBT, because the component can fail even when the destructive current/voltage limits or the critical short-circuit pulse energy are not exceeded. If the amplitude of the oscillation is high enough, it can break the IGBT gate oxidation, as a result of which the controllability of the component will be lost.

A comparison of the $V_{GE}$ waveforms in Figure 4-33 and Figure 4-34 shows that also at lower $V_{DC}$ voltages, Model2 describes the gate-side behaviour better than Model1 excluding the turn-on state, where Model2 reaches the threshold voltage $V_{TH}$ earlier than Model1. In addition, $V_{GE}$ simulated with Model1 does not reach $V_{GE,max}$ or steady state until the point where the short-circuit is turned off. As already observed in Figure 4-31, $I_C$ is not saturated during a 5 µs short-circuit pulse, which is a natural consequence of the non-steady state $V_{GE}$.
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Figure 4-33 Measured and simulated (Model1) $V_{GE}$ waveforms, $V_{DC} = 200$ V, $R_{g,off} = 10$ Ω.

![Graph showing $V_{GE}$ waveforms for Model1](image1)

Figure 4-34 Measured and simulated (Model2) $V_{GE}$ waveforms, $V_{DC} = 200$ V, $R_{g,off} = 10$ Ω.

![Graph showing $V_{GE}$ waveforms for Model2](image2)

In Figure 4-35, the short-circuit parameters of $V_{CE,max}$, $I_{C,max}$, and $I_{C,knee}$ are presented for a $V_{DC}$ voltage range from 150 V to 750 V with $R_{g,off} = 10$ Ω. The effect of the $V_{GE}$ oscillation can be observed from all the parameters in the figure at voltages $V_{DC} = 250$ V and 300 V. The oscillation occurs in $V_{GE}$ already at $V_{DC} = 200$ V (see Figure 4-36a), but its effect is not clearly seen in $V_{CE,max}$, $I_{C,max}$ or $I_{C,knee}$ at this voltage.
$V_{CE,max}$ in Figure 4-35a behaves very linearly as a function of voltage (excluding voltages where the $V_{GE}$ oscillation occurs) as was also observed in the case of $V_{DC} = 650 \text{ V} - 750 \text{ V}$. The difference between the simulated and measured $V_{CE,max}$ is smaller for Model1 than for Model2. Thus, according to the results, the modelled $V_{CE,max}$ behaviour as a function of voltage is similar to the measured one, but there is an offset error in the simulation.

According to the theory, the short-circuit current of the IGBT should increase as a function of voltage. This was discussed in Section 2.2.3, which deals with the IGBT output characteristics. However, when looking at $I_{C,max}$ and $I_{C,knee}$ in Figure 4-35b and c, the results from the simulation models behave differently from the theory because the $I_{C}$ values are mainly decreasing when the $V_{DC}$ voltage goes higher. The results with Model2 decrease continuously through the whole voltage range, whereas the trend of $I_{C,max}$ turns into an increase after $V_{DC} = 550 \text{ V}$. The transfer characteristics of Model1 are composed to give a higher $I_{C}$ if the voltage is increased, but as discussed above, $I_{C}$ is determined also by $C_{CG}$ through $V_{GE}$. Because $I_{C,max}$ is higher for lower voltages, it seems that the effect of $C_{CG}$ is so strong that it overcomes the effect of the voltage dependence in the transfer characteristics.

The way in which the $I_{C,sat}$ voltage dependence is executed in Model2 is not known, but the trend in $I_{C,max}$ and $I_{C,knee}$ is equivalent to Model1, and thus, it can be assumed that the basic structure of the models is similar.

The results of the measured $V_{GE,max}$ in Figure 4-36a clearly show the voltage range where the oscillation occurs. The measured $V_{GE,max}$ is 16.79 V at $V_{DC} = 150 \text{ V}$, and it increases significantly for voltages $V_{DC} = 200 \text{ V} - 300 \text{ V}$ until at $V_{DC} = 350 \text{ V}$ $V_{GE,max}$ is 15.85 V, being thus rather nominal again. After that, the measured $V_{GE,max}$ slightly increases as a function of voltage. As can be assumed, owing to the simple structure of the simulation models, the effect of oscillation cannot be seen in the $V_{GE,max}$ values determined from the simulations. After $V_{DC} = 350 \text{ V}$, the simulated $V_{GE,max}$ values decrease slightly as a function of voltage, and thus, the behaviour is different from the measurement.

Because the increase in $V_{GE}$ is caused by the $i_{CCG}$ and $dV_{CE}/dt$ interaction, it is obvious that in the experiments, $V_{GE,max}$ increases continuously at higher voltages where the value of $C_{CG}$ is small and relatively constant. In the measurement, $I_{C}$ increases as a function of increasing voltage. This leads to a higher $dV_{CE}/dt$, and thereby a higher $i_{CCG}$ causing a higher increase in $V_{GE}$. If $C_{CG}$ is not modelled correctly as a function of voltage and current $i_{CCG}$, consequently, the trend in $V_{GE,max}$ is not modelled correctly in simulations either, even though the trend in the simulated $dV_{CE}/dt$ behaves as in the measurements.
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Figure 4-35 $V_{CE,max}$, $I_{C,max}$ and $I_{C,knee}$ with $R_{g,off} = 10 \, \Omega$ in the DC voltage range from 150 v to 750 V.

A linear behaviour as a function of voltage is seen also in the short-circuit pulse energy $E_{SC}$ in Figure 4-36b. The difference between $E_{SC}$ from Model2 and the measurement stays relatively constant through the whole voltage range, whereas the difference between
Model1 and the measurement decreases when the voltage increases. This is a consequence of the $I_C$ modelling, where Model1 gives more accurate results for higher voltages.

![Graph of $V_{GE,max}$ and $E_{SC}$ at $R_{g,off} = 10 \, \Omega$](image)

Figure 4-36 $V_{GE,max}$ and $E_{SC}$ at $R_{g,off} = 10 \, \Omega$ in the DC voltage range from 150 V to 750 V.

For the trends in the short-circuit rise time $t_{rise}$ and the current gradient $\frac{di}{dt_{rise}}$, both the simulation models show a somewhat similar behaviour to the measurement as presented in Figure 4-37. After the $V_{GE}$ oscillation has disappeared at $V_{DC} = 350 \, \text{V}$, the measured $t_{rise}$ remains constant or slightly increases when the voltage is increased. Both the simulation models show a gradually increasing trend in the same voltage range. In contrast, $\frac{di}{dt_{rise}}$ is continuously increasing as a function of increasing voltage in the measurements and in the results simulated with both the models. The results of Model1 in $t_{rise}$ and $\frac{di}{dt_{rise}}$ are closer to the measured value compared with the results of Model2, excluding very low voltage values below $V_{DC} = 200 \, \text{V}$. 

![Graph of $t_{rise}$ and $\frac{di}{dt_{rise}}$](image)
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In the fall time and current gradient in the turn-off comparison in Figure 4-38, more differences between the models and the measurement can be observed. The fall time $t_{\text{fall}}$ simulated with Model2 behaves much like the measurement as there is no significant variation as a function of voltage, whereas $t_{\text{fall}}$ from Model1 simulations decreases strongly, especially in the low-voltage range ($V_{\text{DC}} < 400$ V). However, the absolute value of $t_{\text{fall}}$ is closer to the measurement in Model1 simulations than in the Model2 simulations.

When looking at the collector current fall gradient $\frac{di}{dt_{\text{fall}}}$ in Figure 4-38b, the results of the Model2 simulation and the measurement show a decreasing trend with an increasing voltage, whereas the results from Model1 simulations have an opposite trend.

The fall time $t_{\text{fall}}$ and the current gradient $\frac{di}{dt_{\text{fall}}}$ are calculated from 90 % of $I_{C,knee}$ to 10 % of $I_{C,knee}$, and thus, the $t_{\text{fall}}$ and $\frac{di}{dt_{\text{fall}}}$ values are affected by the ability of the model to describe a decrease in $I_C$ after $I_{C,max}$. Because the short-circuit pulse is relatively short in these simulations, a decrease in $I_C$ after $I_{C,max}$ is primarily caused by a decrease in $V_{GE}$, whereas the IGBT chip self-heating is not so significant.

Figure 4-37 $t_{\text{rise}}$ and $\frac{di}{dt_{\text{rise}}}$ with $R_{g,\text{off}} = 10$ Ω in the DC voltage range from 150 V to 750 V.
In this section, a comparison of the short-circuit parameters with $R_{\text{g,off}} = 4.7 \, \Omega$ as a function of voltage is presented. In contrast to the previous results, the voltages where the $V_{\text{GE}}$ oscillation occurs in the measurements are excluded from the analysis because the models used in the simulations are not capable of describing such an oscillation. Therefore, the voltage range in the analysis reported below is from 350 V to 750 V. $V_{\text{CE,max}}$, $I_{\text{C,max}}$, and $I_{\text{C,knee}}$ are presented in Figure 4-39. Figure 4-40 shows the results of $V_{\text{GE,max}}$ and $E_{\text{SC}}$, and the transient state parameters $t_{\text{rise}}$, $\frac{di}{dt_{\text{rise}}}$, $t_{\text{fall}}$ and $\frac{di}{dt_{\text{fall}}}$ are shown in Figure 4-41 and Figure 4-42. The numerical values and error percentages of the results are given in Appendix E.

Almost all the observations from the previous analysis are valid also for the results with $R_{\text{g,off}} = 4.7 \, \Omega$, but there are some differences compared with the case where the value of the turn-off resistor is higher. In the previous section, the trend of $I_{\text{C,knee}}$ in the simulations
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did not turn positive before $V_{DC} = 700$ V, but with $R_{g,off} = 4.7$ Ω the same trend shows an increase already after $V_{DC} = 650$ V for Model2 and $V_{DC} = 600$ V for Model1.

Figure 4-39 $V_{CE,max}$, $I_{C,max}$ and $I_{C,knee}$ with $R_{g,off} = 4.7$ Ω in the DC voltage range from 350 V to 750 V.
In general, the simulation results are closer to the ones measured with $R_{g,\text{off}} = 4.7$ Ω than with $R_{g,\text{off}} = 10$ Ω. When the turn-off resistor gets a smaller value, the effect of $i_{CCG}$ on $V_{GE}$ decreases because the current through $C_{CG}$ does not cause as large a voltage drop across the turn-off resistor. The short-circuit operation as a function of $R_{g,\text{off}}$ is analysed in more detail in the following section.

Figure 4-40 $V_{GE,\text{max}}$ and $E_{SC}$ at $R_{g,\text{off}} = 4.7$ Ω in the DC voltage range from 350 V to 750 V.
Figure 4-41 $t_{\text{rise}}$ and $\frac{d}{d$t_{\text{rise}}}$ with $R_{\text{g,off}} = 4.7 \, \Omega$ in the DC voltage range from 350 V to 750 V.
4 Experimental results and simulation model verification

Discussion of the short-circuit behaviour as a function of voltage

The results in the previous two sections show that the IGBT short-circuit behaviour is difficult to describe precisely throughout a wide DC voltage range with the behavioural models used in this study, and furthermore, certain phenomena, such as the $V_{GE}$ oscillation, cannot be modelled at all. In principle, the difficulties in the modelling of the voltage dependence are due to two reasons. First, modelling of $I_{C,sat}$ as a function of $V_{CE}$ is a complex phenomenon, as discussed in Section 2.2.3. The IGBT output characteristics are typically only given for low voltages ($V_{CE}$ is up to a few volts) and the transfer characteristics are often determined at approx. $V_{CE} = 20$ V in datasheets. Thus, some approximation method without a basis of physical parameters has to be used to compose the full IGBT output characteristics. Secondly, $C_{CG}$ has a very non-linear voltage-dependent behaviour, and again, the datasheet information about the $C_{CG}$ behaviour is usually very limited. Furthermore, determination of the $C_{CG}$ value in different operating points often requires very detailed numerical simulation models, as the measurement of $C_{CG}$ is not an easy task. These two issues are the main reasons for the error in the

Figure 4-42 $t_{fall}$ and $di/dt_{fall}$ with $R_{g,off} = 4.7 \, \Omega$ in the DC voltage range from 350 V to 750 V.

![Graph of $t_{fall}$ and $di/dt_{fall}$](image)

![Graph of $C_{CG}$](image)
modelling of the IGBT short-circuit behaviour as a function of $V_{CE}$ with the behavioural simulation models.

At a general level, Model1 gives somewhat more accurate results than Model2 with some exceptions. For example $V_{CE,max}$, $E_{SC}$, and transient state parameters $t_{rise}$, $di/dt_{rise}$, $t_{fall}$, and $di/dt_{fall}$ are better modelled with Model1, whereas Model2 yields better results for collector current parameters and for $V_{GE,max}$. In the previous analysis, the short-circuit pulse length $t_{sc}$ was 5 µs, which causes that $I_C$ is mainly determined by $V_{GE}$ and its behaviour. As presented in the previous $V_{GE}$ waveform figures and in Figure 4-36a and Figure 4-40a, Model2 describes $V_{GE}$ more accurately than Model1. Consequently, also the modelling of $I_C$ is more accurate for short pulse durations.

For longer pulses, $I_C$ is also determined by the self-heating of the IGBT chip, where the effect of the chip thermal model becomes important. Long short-circuit pulses are investigated later in this dissertation.

The accuracy of the transient state parameters is strictly linked to the $V_{CE,max}$ and $E_{SC}$ parameters, and thus, when $t_{rise}$, $di/dt_{rise}$, $t_{fall}$, and $di/dt_{fall}$ are accurate, it is more likely to get accurate results also for $V_{CE,max}$ and $E_{SC}$. For example, when $t_{fall}$ modelled with Model1 in Figure 4-42a shows a good agreement with the measurement, also $V_{CE,max}$ in Figure 4-39a is accurate.

Furthermore, the value of the gate turn-off resistor affects the accuracy of the modelling as shown in the comparison of the results with $R_{g,off} = 4.7 \, \Omega$ and $R_{g,off} = 10 \, \Omega$. When $R_{g,off}$ is changed, it affects especially the accuracy of the transient state parameters, and $I_{C,\text{max}}$ and $I_{C,knee}$. However, the effect of $R_{g,off}$ is analysed in more detail in the next section.

Even though the short-circuit at lower voltages may be critical for the IGBT, for example because of the $V_{GE}$ oscillation, the low-voltage range is not so interesting from the perspective of the power electronic design. At voltages close to the normal operation, the energy of the short-circuit pulse increases, and thus, the device is heated more, and the risk of the destruction of the device increases. There are some special applications and topologies where the switching component may operate in a wide voltage range, but typically, the most critical operating points are found at higher voltages. Therefore, it is more important to achieve good simulation results at voltages close to the normal operation if the IGBT model is used as a design tool.

### 4.4.3 Short-circuit operation as a function of $R_{g,off}$

In this section, the IGBT short-circuit Type I operation is analysed as a function of the gate turn-off resistance $R_{g,off}$, and the simulation results of Model1 and Model2 are compared with the measurement results. The value of $R_{g,off}$ is varied from 3.3 Ω to 22 Ω, including resistances 3.3 Ω, 4.7 Ω, 6.8 Ω, 8.2 Ω, 10 Ω, and 22 Ω. The gate turn-on resistance value $R_{g,on}$ is kept at 3.3 Ω in all cases. Compared with the previous sections, the duration of the short-circuit pulse $t_{sc}$ is increased from 5 µs to 8.33 µs to ensure that
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$V_{GE}$ has reached a steady state before turn-off. When considering the use of a simulation model as a design tool, the most interesting voltage range is close to the nominal, and thus, the voltage selected for this analysis is $V_{DC} = 750$ V. A comparison of the short-circuit parameters is made similarly to the previous section, but the variable that is changed between the operating points is $R_{g,off}$ instead of $V_{DC}$.

The measurements with different $R_{g,off}$ values are performed in a calorimetric chamber where temperature of the chamber can be controlled. The results in this section are recorded/simulated at an ambient temperature $T_a = 40 \degree C$.

A comparison of the short-circuit parameters as a function of $R_{g,off}$ is presented in Figure 4-43, Figure 4-44, Figure 4-45, and Figure 4-46. Overall, the trends of the simulated parameter values correspond well with the measurements, excluding $I_{C,knee}$ in Figure 4-43c, where the measured $I_{C,knee}$ decreases with an increasing $R_{g,off}$, whereas the simulation results show an opposite behaviour.

$V_{CE,max}$ simulated with Model1 is very close and a slightly above the measured value throughout the whole investigated $R_{g,off}$ range, see Figure 4-43a. The results of $V_{CE,max}$ with Model2 are also close to the experiments, but with lower $R_{g,off}$ values Model2 gives underestimated values and with higher values of $R_{g,off}$ the simulated $V_{CE,max}$ value is above the measurement.

A similar behaviour with Model2 can also be observed in the $I_{C,max}$ parameter as presented in Figure 4-43b. For Model1, there is a relatively constant offset error between the simulated and measured $I_{C,max}$, although the offset decreases at $R_{g,off} = 22 \Omega$.

Figure 4-43c shows the results of the short-circuit turn-off current $I_{C,knee}$. Here, the behaviour of the simulation models differs significantly from the measurement as the simulation results increase towards higher $R_{g,off}$ values, whereas the measurements show a decreasing behaviour. The difference between Model1 and the measurement results is smaller compared with the difference between Model2 results and the measurements. As the short-circuit pulse duration $t_{SC}$ is 8.33 µs in this analysis, the component self-heating affects the $I_C$ waveforms slightly, which can be seen also in $I_{C,knee}$. Information about the Model2 structure does not show any sign that the model would include a self-heating effect, whereas a chip thermal model is included in Model1 as presented in Section 3.1. The possible reason for more accurate $I_{C,knee}$ results with Model1 is that it also models the self-heating of the IGBT chip.

The maximum gate-emitter voltage $V_{GE,max}$ and the short-circuit pulse energy $E_{SC}$ are presented in Figure 4-44a and Figure 4-44b, respectively. As was also observed in the case where the DC voltage was varied, both the simulation models give overestimated $V_{GE,max}$ values compared with the measurement, and furthermore, the Model1 $V_{GE,max}$ values are higher than the ones simulated with Model2. However, the effect of $R_{g,off}$ on $V_{GE,max}$ is not as strong for Model2 as it is for Model1 or detected in the measurements.
Figure 4-43 $V_{CE,max}$, $I_{C,max}$ and $I_{C,knee}$ at $V_{DC} = 750$ V while $R_{g,off}$ is varied from 3.3 Ω to 22 Ω.

When comparing the $E_{SC}$ values in Figure 4-44b, it is clear that Model1 gives more accurate results than Model2 even though the difference between Model1 and the measurement becomes larger with an increasing $R_{g,off}$. One reason for the inaccuracy in $E_{SC}$ with Model2 is that the $I_C$ waveform between $I_{C,max}$ and the turn-off point stays...
constantly higher than the measurement. This is also seen as a difference between Model2 and the measurement in $I_{C,knee}$ in Figure 4-43b. Another error source in $E_{SC}$ is the more erroneous modelling of $t_{fall}$, see Figure 4-46a.

![Graph a)](image1)

**Figure 4-44** $V_{GE,max}$ and $E_{SC}$ at $V_{DC} = 750$ V while $R_{g,off}$ is varied from 3.3 Ω to 22 Ω.

In principle, a change in $R_{g,off}$ does not considerably affect the short-circuit turn-on if other operating point parameters remain the same. However, the short-circuit parameters $t_{rise}$ and $di/dt_{rise}$ change as a function of $R_{g,off}$ as presented in Figure 4-45. The reason for the observed phenomenon is that $R_{g,off}$ affects $V_{GE,max}$ and thereby also $I_{C,max}$. The parameters $t_{rise}$ and $di/dt_{rise}$ are calculated from the collector current points that are relative to $I_{C,max}$, and thus, these parameters change as a function of $R_{g,off}$. The results of $t_{rise}$ and $di/dt_{rise}$ with Model1 are, in general, closer to the measured values than the results with Model2 when the value of $R_{g,off}$ is varied.

![Graph b)](image2)
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Figure 4-45 \(t_{\text{rise}}\) and \(d_i/dt_{\text{rise}}\) at \(V_{\text{DC}} = 750\) V while \(R_{g,\text{off}}\) is varied from 3.3 Ω to 22 Ω.

In a comparison of the turn-off state parameters \(t_{\text{fall}}\) and \(d_i/dt_{\text{fall}}\) in Figure 4-46, Model1 shows a very good agreement with the measurements in both the absolute value of the parameter and the trend in behaviour as a function of \(R_{g,\text{off}}\). However, at \(R_{g,\text{off}} = 22\), the difference in the absolute values between Model2 and the measurement is smaller than between Model1 and the measurement. Increasing the value of \(R_{g,\text{off}}\) has a significant influence on the IGBT turn-off behaviour by increasing the turn-off time \(t_{\text{fall}}\) and decreasing the turn-off current gradient \(d_i/dt_{\text{fall}}\); this is generally used to reduce for example \(V_{\text{CE,max}}\) at the short-circuit turn-off. Nevertheless, \(t_{\text{fall}}\) and \(d_i/dt_{\text{fall}}\) in Model2 results do not change significantly as a function of \(R_{g,\text{off}}\). This is especially true for \(d_i/dt_{\text{fall}}\), which shows almost a constant value even when \(R_{g,\text{off}}\) is changed. \(I_{C,knee}\) in the Model2 simulations changes as a function of \(R_{g,\text{off}}\), which causes different change rates of \(t_{\text{fall}}\) and \(d_i/dt_{\text{fall}}\).
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Figure 4-46: $t_{\text{fall}}$ and $\frac{d}{d\text{fall}}$ at $V_{\text{DC}} = 750 \text{ V}$ while $R_{g,\text{off}}$ is varied from 3.3 $\Omega$ to 22 $\Omega$.

The following figures present simulated/measured $V_{\text{CE}}$ waveforms when the value of $R_{g,\text{off}}$ is changed. Figure 4-47 shows the results simulated with Model1, Figure 4-48 illustrates the results simulated with Model2, and the measurement results are depicted in Figure 4-49. In all the figures, the effect of $R_{g,\text{off}}$ on the turn-off behaviour is clearly seen when observing for example the amplitude of the voltage spike at the short-circuit turn-off starting at $t = 9.73 \mu\text{s}$.

The $V_{\text{CE}}$ behaviour in the short-circuit Type I is determined particularly by $\frac{dI_{\text{C}}}{dt}$. At the beginning of the short-circuit turn-on, the $V_{\text{CE}}$ waveforms with different $R_{g,\text{off}}$ values are identical as $\frac{dI_{\text{C}}}{dt}$ does not change as a function of $R_{g,\text{off}}$ during this period. However, when reaching the point where $I_{\text{C}}$ becomes closer to $I_{\text{C, max}}$ ($t$ is around 5 $\mu\text{s}$), variation in the $V_{\text{CE}}$ waveform can be noticed, because $I_{\text{C, max}}$ and the behaviour of the $I_{\text{C}}$ waveform after it change when $R_{g,\text{off}}$ is varied. $I_{\text{C}}$ waveforms as a function of $R_{g,\text{off}}$ for Model1, Model2, and measurement are presented in Figure 4-50, Figure 4-51, and Figure 4-52, respectively. In the $V_{\text{CE}}$ waveforms, $R_{g,\text{off}}$ clearly affects the amplitude of the voltage spike.
at the turn-off, and the location of $V_{CE,max}$. Further, the phase and amplitude of the $V_{CE}$ oscillation after the turn-off are affected.

Figure 4-47 $V_{CE}$ waveforms simulated with Model1 as a function of $R_{g,off}$.

When comparing Figure 4-47 and Figure 4-48, it can be seen that the effect of $R_{g,off}$ is not as strong for the Model2 $V_{CE}$ waveform as for Model1. This is a consequence of the more stable $I_C$ waveform close to $I_{C,max}$ and after it, as can be seen in Figure 4-50 and Figure 4-51.
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The measured $V_{CE}$ waveform in Figure 4-49 is somewhere between the $V_{CE}$ waveforms simulated with Model1 and Model2. However, the voltage drop at the beginning of the short-circuit pulse in the measurement is steeper than in the simulations, even though $di/dt_{rise}$, calculated from the measurement, is smaller than in the simulations. The reason for this is most likely that the instantaneous $di/C_{d}dt$ at the beginning of the SC pulse is higher in the measurement than in the simulation (see e.g. Figure 4-24 and Figure 4-25). Another reason may be that the circuit inductance is modelled too low in the simulations as it does not consider for example the connections and all details inside the IGBT module.

There is also a difference in $V_{CE,max}$ between the simulations and the measurements. As presented in Figure 4-46b, $di/dt_{fall}$ of Model2 is much lower than in the measurement, and therefore, the voltage spikes in Figure 4-48 are lower than in Figure 4-49. The voltage spikes in Model1 simulations compared with the measurement are higher at lower $R_{g,off}$ values and lower at higher $R_{g,off}$ values as presented in Figure 4-43a. This corresponds well with the $di/dt_{fall}$ behaviour, where Model1 also shows higher values at lower $R_{g,off}$ and lower values at higher $R_{g,off}$ when compared with the measurement.
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Figure 4-49 Measured $V_{CE}$ waveforms as a function of $R_{g,off}$.

In the comparison of the $I_C$ waveforms in Figure 4-50, Figure 4-51, and Figure 4-52, both the simulation models differ from the measurement after $I_{C,max}$. In the measurement in Figure 4-52, $I_C$ decreases toward a single point where the turn-off starts, which means that $I_{C,knee}$ is relatively independent of $R_{g,off}$. Actually, $I_{C,knee}$ is slightly reduced, whereas $R_{g,off}$ is increased. This is due to the higher $I_C$ between $I_{C,max}$ and $I_{C,knee}$ with a larger $R_{g,off}$, which causes a higher $E_{SC}$, which increases the chip temperature.

In the Model1 simulations, $I_{C,knee}$ increases marginally as a function of increasing $R_{g,off}$ (excluding $R_{g,off} = 22 \, \Omega$). In the range $R_{g,off} = 4.7 \, \Omega$–10 $\Omega$, the $I_C$ waveform in Figure 4-50 decreases towards a single point as in the measurement. A comparison with the results of Model2 shows that here $I_{C,knee}$ increases continuously with an increasing $R_{g,off}$, which is different behaviour than in the measurement. This offset error in $I_{C,knee}$ is caused by an error in the $V_{GE}$ modelling as presented in Figure 4-53–Figure 4-55. The error in $V_{GE}$ modelling is probably due to the imprecise $C_{CG}$ modelling and the simplified gate driver model.
Another difference between the simulations and the measurement is the \( I_C \) behaviour during the turn-off. Model1 and the measurement clearly indicate that \( \frac{di}{df_{\text{fall}}} \) is affected by \( R_{\text{g,off}} \), whereas in the Model2 simulations \( \frac{di}{df_{\text{fall}}} \) remains almost constant even though \( R_{\text{g,off}} \) is varied.

As can be seen in all the results, \( R_{\text{g,off}} \) affects the IGBT short-circuit behaviour by increasing \( i_{\text{C,max}} \) and shifting its occurrence later in time. This is due to the current through a Miller capacitance \( i_{\text{CCG}} \) that flows also through \( R_{\text{g,off}} \), which increases \( V_{\text{GE}} \).
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Figure 4-51 $I_C$ waveforms simulated with Model2 as a function of $R_{g,off}$.

Figure 4-52 Measured $I_C$ waveforms as a function of $R_{g,off}$.

The simulated and measured $V_{GE}$ waveforms as a function of $R_{g,off}$ are presented in Figure 4-53–Figure 4-55. All the results show a similar general behaviour when $R_{g,off}$ is changed, that is, $V_{GE,max}$ increases and the gradient of $V_{GE}$ decreases with an increasing $R_{g,off}$. The main differences are that the $V_{GE}$ gradient at the turn-off in Model1 simulations is much smaller than in the measurement, and this phenomenon is amplified whereas $R_{g,off}$ is
increased, and that there is an oscillation in $V_{GE}$ at the end of the turn-off phase in the Model2 simulations. Some discontinuity in the model capacitances probably causes the latter one. As $V_{GE}$ at the turn-off is only determined by the discharging of the component capacitances in Model1, the error in the $V_{GE}$ gradient comes from the capacitance modelling. Because a higher $R_{g,off}$ causes a slightly higher $I_{C,knee}$ in the Model1 simulations and because $C_{CG}$ is modelled as current dependent, it seems that $C_{CG}$ gets too large a value at higher $R_{g,off}$ values. Too large a $C_{CG}$ value, in turn, causes a slower discharging rate, which can be seen as a lower $V_{GE}$ gradient in Figure 4-53.

Figure 4-53 $V_{GE}$ waveforms simulated with Model1 as a function of $R_{g,off}$. 
4.4 Analysis of the simulation and measurement results

Figure 4-54 $V_{GE}$ waveforms simulated with Model2 as a function of $R_{g,off}$.

Figure 4-55 Measured $V_{GE}$ waveforms as a function of $R_{g,off}$.

Discussion of the short-circuit behaviour as a function of $R_{g,off}$

The numerical values of short-circuit parameters for $R_{g,off} = 3.3 \, \Omega$ and $22 \, \Omega$ are presented and compared in Appendix F. As the percentages of difference show, Model1 describes the short-circuit behaviour as a function of $R_{g,off}$ better in $V_{CE,max}$, $I_{C,knee}$, $E_{SC}$, and the
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Transient state parameters $t_{\text{rise}}$ and $\frac{di}{dt_{\text{rise}}}$. For $t_{\text{fall}}$ and $\frac{di}{dt_{\text{fall}}}$, Model1 gives more accurate results than Model2 with a small $R_{\text{g,off}}$, but the accuracy deteriorates with $R_{\text{g,off}} = 22 \, \Omega$.

In general, Model1 shows an appropriate accuracy as apart from one exception, the percentages of difference are below 20 %, and for many parameters the error is below 5 %. For Model2, there are a couple of parameters that show an error below 5 %, but there are also many parameters for which the error percentage is above 20 % when the maximum error percentage is 244.96 % in $t_{\text{fall}}$ with $R_{\text{g,off}} = 3.3 \, \Omega$.

If the simulation model is used as a design tool, for example in a motor drive design, the model behaviour as a function of $R_{\text{g,off}}$ is probably more important than its behaviour as a function of voltage, because the voltage across the IGBT is more or less fixed by the DC link voltage, whereas the value of $R_{\text{g,off}}$ can be selected more freely. As discussed above, most of the errors in the simulations come from erroneous modelling of $V_{\text{GE}}$, which is affected by $C_{\text{CG}}$. This is critical because an inaccuracy in $V_{\text{GE}}$ leads to an inaccuracy in $I_{\text{C,max}}$, $I_{\text{C,knee}}$, and $\frac{di}{dt_{\text{fall}}}$ (which causes an inaccurate $V_{\text{CE,max}}$), whereas errors in the $I_{\text{C}}$ and $V_{\text{CE}}$ waveforms lead to an error in $E_{\text{SC}}$. $I_{\text{C,max}}$, $V_{\text{CE,max}}$, and an excessive $E_{\text{SC}}$ can all cause IGBT destruction during or right after a short-circuit pulse, and therefore, accurate modelling of these parameters is important. However, the results presented above show sufficient accuracy to model for example an effect of different design selections at early stages of the design process. Yet, if the modelling accuracy as a function of $R_{\text{g,off}}$ is wanted to be improved, the most effective way is to improve the accuracy of the $C_{\text{CG}}$ modelling.

4.4.4 Short-circuit operation as a function of $t_{\text{SC}}$

In this section, the IGBT short-circuit operation is analysed as a function of short-circuit pulse length. Manufacturers typically determine the maximum short-circuit pulse length $t_{\text{SC,max}}$ in a certain operating point ($V_{\text{DC}}$, $T_{\text{j}}$ etc.) in the component datasheet. The reason for this is that with longer pulses, the power losses inside the component increase, which may cause excessive heating of the component and eventually, thermal runaway and component destruction. According to some references, for instance (Arab et al., 2008), the component-specific critical energy $E_{\text{c}}$ defines the limit for component destruction. If the short-circuit pulse energy $E_{\text{SC}}$ is below $E_{\text{c}}$, the component tolerates a large number of short-circuits, whereas when $E_{\text{SC}} > E_{\text{c}}$, the component is destroyed by a single SC incident. $E_{\text{SC}}$ is determined by the $I_{\text{C}}$ and $V_{\text{CE}}$ waveforms during a short-circuit pulse, and if these waveforms are accurately modelled, also $E_{\text{SC}}$ can be calculated with a good accuracy. Because $V_{\text{CE}}$ is relatively constant in the short-circuit Type I, the accuracy of the $I_{\text{C}}$ waveform has a significant impact on the accuracy of $E_{\text{SC}}$. In addition to $V_{\text{GE}}$, the effect of which on $I_{\text{C}}$ was discussed in previous sections, the self-heating of the IGBT chip is very relevant when the $I_{\text{C}}$ waveform is investigated with longer pulses. In Model1, the chip temperature is modelled by using the thermal capacity of the chip, whereas in Model2 a traditional thermal network from the IGBT chip junction to the IGBT module case is applied. The results are compared with the on gate turn-off resistor value ($R_{\text{g,off}} = 4.7 \, \Omega$) at two voltages $V_{\text{DC}} = 400 \, \text{V}$ and $750 \, \text{V}$. The short-circuit pulse length $t_{\text{SC}}$ is varied from 5 µs to 12.5 µs.
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The IGBT chip self-heating has a direct effect on the carrier mobility and thereby $I_{C,sat}$ as discussed in Section 2.2.4. The effect is more clearly seen in the $I_C$ waveform after the point where $V_{GE}$ has reached a steady-state value, because there $I_{C,sat}$ is no longer affected by the $V_{GE}$ variation. Obviously, the short-circuit pulse length and self-heating do not affect the short-circuit parameters that are determined in the turn-on phase or before $V_{GE}$ reaches its maximum value; such parameters are $I_{C,max}$, $V_{GE,max}$, $t_{rise}$, and $d_{i/dt_{rise}}$. The short-circuit parameters most affected by self-heating are $V_{CE,max}$, $I_{C,knee}$, and $E_{SC}$. Furthermore, based on the theory presented in Section 2.2.4, the turn-off phase parameters $t_{fall}$ and $d_{i/dt_{fall}}$ should be changed as a function of temperature, and thus, as a function of $t_{SC}$ because of the reduction in the carrier mobility.

Figure 4-56 Measured and simulated (Model1) $V_{CE}$ waveform, $R_{g,off} = 4.7 \, \Omega$, $V_{DC} = 750 \, \text{V}$, and $t_{SC} = 8.33 \, \mu\text{s}$.
Figure 4-57 Measured and simulated (Model2) $V_{CE}$ waveform; $R_{g,off} = 4.7 \, \Omega$, $V_{DC} = 750 \, V$, and $t_{SC} = 8.33 \, \mu s$.

Figure 4-58 Measured and simulated (Model1) $I_C$ waveform; $R_{g,off} = 4.7 \, \Omega$, $V_{DC} = 750 \, V$, and $t_{SC} = 8.33 \, \mu s$. 
Figure 4-59 Measured and simulated (Model2) $I_C$ waveform; $R_{\text{g,off}} = 4.7 \, \Omega$, $V_{\text{DC}} = 750 \, \text{V}$, and $t_{\text{SC}} = 8.33 \, \mu\text{s}$.

Figure 4-60 Measured and simulated (Model1) $V_{GE}$ waveform; $R_{\text{g,off}} = 4.7 \, \Omega$, $V_{\text{DC}} = 750 \, \text{V}$, and $t_{\text{SC}} = 8.33 \, \mu\text{s}$. 
4 Experimental results and simulation model verification

Figure 4-61 Measured and simulated (Model2) $V_{GE}$ waveform; $R_{g,off} = 4.7 \, \Omega$, $V_{DC} = 750 \, V$, and $t_{SC} = 8.33 \, \mu s$.

Figure 4-62 and Figure 4-63 present the measured and simulated $V_{CE}$ waveforms with the 12.5 \, \mu s short-circuit pulse length. The $V_{CE}$ waveform from Model1 follows quite well the measured one, but because of the limited energy source of the test setup, the measured $V_{CE}$ does not stay constant during the pulse. The voltage spikes of the measurement and the simulation at the end of the pulse in Figure 4-62 are also very close to each other, indicating that also $I_{C,knee}$ and $di/dt_{fall}$ are modelled with a good accuracy.
4.4 Analysis of the simulation and measurement results

Figure 4-62 Measured and simulated (Model1) $V_{CE}$ waveform; $R_{\text{off}} = 4.7 \, \Omega$, $V_{DC} = 750 \, V$, and $t_{SC} = 12.5 \, \mu s$.

The most interesting waveform from the perspective of self-heating is the collector current waveform, because it is also determined by the IGBT chip temperature. The $I_C$ waveforms simulated with Model1 and Model2 with $t_{SC} = 12.5 \, \mu s$ are presented in Figure 4-64 and Figure 4-65, respectively. The measured $I_C$ waveform is also shown in the figures. First, when observing the behaviour of the measured $I_C$, it can be seen that after $I_{C,\text{max}}$ at around $t = 5 \, \mu s$, the collector current decreases rapidly, and after around $t = 10 \, \mu s$, the rate of decrease is slower and rather linear. Between these points there is some fluctuation in the $I_C$ curve. The fluctuation is caused by a change in $V_{CE}$, which is also seen in the $V_{GE}$ waveform in Figure 4-66 and Figure 4-67. Therefore, between $t = 5 \, \mu s$ and $t = 10 \, \mu s$ the decrease in $I_C$ is not caused only by self-heating, but the variation in $V_{GE}$ affects also the $I_C$ waveform. After $t = 10 \, \mu s$, the measured $V_{GE}$ is constant, and thus, from this point on, the decrease in the $I_C$ can be assumed to be caused by self-heating only. Hence, the effect of pure self-heating seems to be linear.
The effect of self-heating is also clearly visible in the Model1 simulations in Figure 4-64, and the decrease rate of $I_C$ is very similar to the measurement. However, the behaviour between $t = 5 \mu s$ and $t = 10 \mu s$ is slightly different, because the simulated $V_{CE}$ and $V_{GE}$ reach a steady state already at $t = 7 \mu s$. After $t = 10 \mu s$, the measured and simulated $I_C$ waveforms behave very similarly, even though the decrease rate is slightly different.

The difference in the decrease rate is probably caused by two simplifications in the chip temperature estimation in Model1. First, the temperature of the chip is assumed to be uniform, which is not the case in a real IGBT. As presented in Section 2.2.4, the top of the chip is usually much hotter than the bottom, because there is no efficient heat transfer path on the top of the chip, and because the bottom of the chip stays at a base plate temperature if the thermal time constant of the base plate is much higher than the duration of the short-circuit. The second simplification is that the chip temperature in Model1 is simulated only for one chip, the current of which is 1/12 of the total current through the module. This is correct if all the 12 parallel-connected chips are equally stressed during the short-circuit, but this is not exactly correct in a real IGBT module. According to (Wu et al., 2014), the chips in the middle of the module are much more stressed by the short-circuit current than the chips on the edges. The module layout in (Wu et al., 2014) is the same as the one used in this study. Consequently, the decrease in the $I_C$ waveform caused by self-heating, and measured from the main connections, is an average of the decreases in the unequally heated chips inside the module. Detailed investigation of the chip temperature during a short-circuit requires numerical simulations, because it is difficult to measure the chip junction temperature under dynamic conditions of the short-circuit.
Figure 4-64 Measured and simulated (Model1) \( I_C \) waveform; \( R_{g,off} = 4.7 \, \Omega \), \( V_{DC} = 750 \, \text{V} \), and \( t_{SC} = 12.5 \, \mu\text{s} \).

When comparing the simulation results with Model1 in Figure 4-64 and with Model2 in Figure 4-65, it is clear that the self-heating effect is not accurately modelled in Model2. The documentation of Model2 does not report the temperature dependence of the model parameters or whether the parameters are constantly updated during a conduction pulse, and therefore, it is difficult to find a clear reason for the Model2 behaviour. However, the chip dimensions, its material properties, or the IGBT module internal layout (e.g. the number of parallel chips) is not required in the characterization tool of Model2, and thus, it seems likely that the chip temperature is not determined by using the chip properties in Model2, whereas the thermal network parameters from the chip junction to the case can be given in the characterization tool. The component datasheet usually gives thermal network data for a Foster-type network. The difficulty of the Foster-type network is that the thermal parameters do not correspond with the actual layers of the component, meaning that it cannot be used to define the specific temperature from the inside of the thermal network, only the temperature difference between the junction and the case. The time constants of the whole thermal network chain determine how fast transients can be investigated with a Foster-type network. In this study, the thermal network data of the IGBT module are given by four time constants, the smallest of which is 0.8 ms (Infineon, 2016). If the time scale of the short-circuit is under 20 \( \mu\text{s} \), the chip temperature cannot be determined with this type of thermal model.
4 Experimental results and simulation model verification

Figure 4-65 Measured and simulated (Model2) $I_C$ waveform; $R_{\text{g,off}} = 4.7\ \Omega$, $V_{\text{DC}} = 750\ \text{V}$, and $t_{\text{SC}} = 12.5\ \mu\text{s}$.

Figure 4-66 Measured and simulated (Model1) $V_{\text{GE}}$ waveform; $R_{\text{g,off}} = 4.7\ \Omega$, $V_{\text{DC}} = 750\ \text{V}$, and $t_{\text{SC}} = 12.5\ \mu\text{s}$. 
4.4 Analysis of the simulation and measurement results

Figure 4-67 Measured and simulated (Model2) $V_{GE}$ waveform; $R_{g,off} = 4.7 \ \Omega$, $V_{DC} = 750 \ \text{V}$, and $t_{SC} = 12.5 \ \mu\text{s}$.

Figure 4-68 shows the short-circuit parameters $V_{CE,max}$ and $I_{C,knee}$ as a function $t_{SC}$. As Model1 includes modelling of the self-heating effect, both the parameters simulated with the model correspond well with the measurement. $V_{CE,max}$ is decreased as a function of $t_{SC}$ because of the lower $I_{C,knee}$ and $di/dt_{fall}$. In the Model2 simulations, $V_{CE,max}$ remains quite constant.
Figure 4-68 $V_{CE,max}$ and $I_{C,knee}$ at $V_{DC} = 750$ V while $t_{SC}$ is varied from 5 $\mu$s to 12.5 $\mu$s.

Figure 4-69 presents values for $E_{SC}$, $t_{fall}$, and $di/dt_{fall}$. Naturally, $E_{SC}$ increases when $t_{SC}$ becomes longer, and the measurements and the results with both the simulation models show all similar trends. However, the difference between the measurement and Model2 results is much larger than the difference between the Model1 simulations and the measurements. This is because of the self-heating modelling included in Model1 and thereby a more accurate $I_C$ waveform.
4.4 Analysis of the simulation and measurement results

The current fall time $t_{\text{fall}}$ stays relatively constant as a function of $t_{\text{SC}}$, but in the measurement and Model1 simulations $d/dt_{\text{fall}}$ shows a slightly decreasing trend. The component with a higher temperature behaves generally slower in transients than the component with a lower temperature, and thus, $d/dt_{\text{fall}}$ decreases with longer SC pulses.

Figure 4-69 $E_{\text{SC}}$, $t_{\text{fall}}$ and $di/dt_{\text{fall}}$ at $V_{\text{DC}} = 750$ V while $t_{\text{SC}}$ is varied from 5 µs to 12.5 µs.
When \( \frac{di}{dt_{\text{fall}}} \) decreases, \( t_{\text{fall}} \) has to stay relatively constant, because \( I_{C,\text{knee}} \) is also decreasing as a function of increasing \( t_{SC} \).

The percentages of difference between the results of Model1/Model2 and the measurements with \( t_{SC} = 12.5 \) µs are listed in Appendix G. The parameter values are given with two voltages, \( V_{DC} = 750 \) V and \( V_{DC} = 400 \) V. The results show that the proposed method to include the self-heating effect in Model1 is reasonable, because the results with Model1 are more accurate than with Model2, excluding \( V_{GE,\text{max}} \). However, when the voltage is decreased, the accuracy of Model1 deteriorates, but the effect of voltage is not so strong on the accuracy of Model2. In fact, the accuracy of Model2 is even improved in some parameters when the voltage is decreased. The origin of error in the Model1 voltage dependence is the imprecisely modelled \( I_{C,\text{sat}} \) voltage dependence and \( C_{CG} \) voltage dependence.

**Discussion of the short-circuit behaviour as a function of \( t_{SC} \)**

The results presented above show that the IGBT self-heating effect during a short-circuit can be modelled with a reasonable accuracy by using the IGBT chip thermal capacity to estimate the chip temperature. However, as it does not describe the temperature distribution inside the chip, it cannot be used to determine the maximum temperature within the chip. For example, numerical or simplified analytical methods have to be used for a detailed temperature modelling. Model1 with the self-heating modelling included gives more accurate results with a longer \( t_{SC} \) compared with Model2. This is shown especially in the accuracy of the parameter \( E_{SC} \).

As already observed in Section 4.4.2, the accuracy of the simulation models deteriorates when the voltage across the component is decreased. A similar behaviour is also seen in the results with longer short-circuit pulses. However, if the models are used to determine for example exceeding of \( E_{c} \) or the maximum allowed \( V_{CE} \), an inaccurate voltage dependence is not so critical because the component is stressed the most when the voltage is high.

**4.4.5 Short-circuit operation as a function of \( T_{a} \)**

The IGBT behaviour as a function of the chip junction temperature \( T_{j} \) is widely investigated and reported in the literature; nevertheless, to the author’s knowledge, there are few publications that deal with the IGBT short-circuit behaviour as a function of the ambient temperature \( T_{a} \). The objective of this section is to investigate whether there are some visible indications of an increased \( T_{a} \) in the IGBT short-circuit waveforms \( (V_{CE}, I_{C}, V_{GE}) \), and if there are such indications, whether they can come from some other component in the circuit than the IGBT itself. The results show that the effect of \( T_{a} \) can only be seen in the \( I_{C} \) waveform, and \( V_{CE} \) are \( V_{GE} \) remain the same even though the temperature is increased. The results of the simulation models as a function of ambient temperature are also presented in this section.
Because of the limitations of the calorimetric chamber used as a test chamber in the experiments with a variable $T_a$, the ambient temperature is only studied at two temperatures $T_a = 30 \, ^\circ\text{C}$ and $T_a = 40 \, ^\circ\text{C}$. In real applications $T_a$ can be much higher. The effect of $T_a$ is analysed in the operating point where $V_{\text{DC}} = 750 \, \text{V}$, $R_{g,\text{off}} = 4.7 \, \Omega$ and $t_{SC} = 8.33 \mu\text{s}$.

The $V_{\text{CE}}$ waveforms as a function of ambient temperature from the measurement and the simulations are presented in Figure 4-70. In all the results, the waveforms with $T_a = 30 \, ^\circ\text{C}$ and $T_a = 40 \, ^\circ\text{C}$ overlap each other, and thus, the temperature change of 10 \, ^\circ\text{C} does not cause any visible variation to the collector-emitter voltage.
The situation is the same in the $V_{GE}$ waveforms as in $V_{CE}$ as presented in Figure 4-71.
4.4 Analysis of the simulation and measurement results

Figure 4-71 $V_{GE}$ waveforms a) from the measurement, b) from the Model1 simulation, and c) from the Model2 simulation as a function of temperature; $V_{DC} = 750$ V, $R_{G,off} = 4.7 \, \Omega$, and $t_{SC} = 8.33 \, \mu$s.

When investigating the measured collector current waveform in Figure 4-72, the effect of the ambient temperature is visible. When $I_C$ approaches $I_{C,\text{max}}$, the waveforms at
The transient states in Figure 4-72 are the very same at both temperatures, and thus, it can be assumed that a 10-degree temperature change does not significantly affect the component capacitances.

![Figure 4-72 IC waveforms from the measurement as a function of ambient temperature; \( V_{DC} = 750 \, \text{V}, R_{g,off} = 4.7 \, \Omega, \) and \( t_{SC} = 8.33 \, \mu\text{s}. \)](image)

When considering the effect of ambient temperature on \( I_C \) in the Model1 simulations in Figure 4-73, a very similar behaviour to the measurements can be found. The difference between \( I_C \) at \( T_a = 30 \, ^\circ\text{C} \) and at \( T_a = 40 \, ^\circ\text{C} \) is largest at \( I_{C,Cmax} \), and the difference decreases towards the turn-off point. However, a small difference in \( I_{C,knee} \) in the turn-off point can be observed in the simulated waveforms, whereas no difference can be seen in the measurements.
4.4 Analysis of the simulation and measurement results

Figure 4-73 $I_C$ waveforms from the Model1 simulations as a function of ambient temperature; $V_{DC} = 750$ V, $R_{g,off} = 4.7 \, \Omega$, and $t_{SC} = 8.33 \, \mu$s.

In the Model2 simulations, the effect of ambient temperature on the collector current waveform is very small as presented in Figure 4-74. A marginal difference can be observed at $I_{C,\text{max}}$, when $I_C$ waveforms at $T_a = 30 ^\circ \text{C}$ and $T_a = 40 ^\circ \text{C}$ are compared. The difference in the $I_C$ waveforms is much smaller compared with the measurement and the Model1 simulations, and the reason for this is very likely the thermal modelling method used in Model2. By using a thermal network from the junction to the case to estimate the junction temperature, the temperature response is so slow that the junction temperature does not change much during the short-circuit pulse. Even though $I_{C,\text{sat}}$ as a function of temperature is modelled correctly, its effect cannot be seen in the Model2 simulations if the chip temperature is not modelled accurately.
IGBT chip temperature during a short-circuit

It is very difficult to measure the IGBT chip temperature from a real IGBT module, even though some studies have shown that for example a thermal imaging camera can be used to determine the chip temperature during a short-circuit pulse from an opened IGBT module. Determining the chip temperature from measurements is outside the scope of this study; nevertheless, the accuracy of the Model1 chip temperature calculation can be investigated based on some assumptions.

By assuming that the short-circuit data given in the component datasheet are valid for the maximum short-circuit stress that the component can tolerate, the following information can be derived from the datasheet. The short-circuit current $I_{SC}$ for the component is 5600 A at $V_{DC} = 800$ V, $V_{GE} = 15$ V, $t_{SC} = 10$ µs, and $T_j = 150$ °C, and thus, $T_{j,max}$ should be close to 426.85 °C (700 K), which is the critical temperature for silicon at the end of the pulse if the conditions in the datasheet represent the maximum short-circuit pulse. However, when using Model1 to simulate a short-circuit pulse with the parameters $V_{DC} = 800$ V, $V_{GE} = 15$ V, $t_{SC} = 10$ µs, and $T_j = 150$ °C, the chip temperature at the end of the pulse is only $T_j = 236.7$ °C (509.85 K). As discussed in Section 2.2.4, the chip maximum temperature is incorrect if a uniform temperature distribution in the chip is assumed, and this causes an error between the simulated $T_{j,max}$ and critical temperature of silicon.

By determining the short-circuit current from the simulated $I_C$ waveform in the same way as in the datasheet, Eq. (2.24) can be applied to estimate the maximum temperature on
the top of the chip and compare it with the temperature calculated with the datasheet values. The simulated short-circuit current $I_{SC} = 5097.20 \text{ A}$ for the operating point $V_{DC} = 800 \text{ V}$, $V_{GE} = 15 \text{ V}$, $t_{SC} = 10 \text{ µs}$, and $T_j = 150 \text{ °C}$ when Model1 is used. By applying Eq. (2.24), the maximum chip temperature $T_{j,max} = 385.41 \text{ °C}$ (658.56 K), which is higher than $T_{j,max}$ determined from the simulation where a uniform chip temperature is assumed, but still below $T_{j,max} = 420.96 \text{ °C}$ (694.11 K), which can be calculated by using datasheet information. A lower $T_{j,max}$ from the simulation is a natural consequence of the lower $I_{SC}$ compared with the datasheet value. $I_{SC}$ is determined also from the $I_C$ waveform simulated with Model2. Because Model2 does not model the self-heating effect, $I_{SC}$ is almost the same as the turn-off point current $I_{C,knee}$. In this case, $I_{SC} = 5887.25 \text{ A}$, which leads to $T_{j,max} = 441.27 \text{ °C}$ (714.42 K), which is already above the critical temperature of silicon.

The calculated chip temperatures as a function of chip thickness for $t_{SC} = 10 \text{ µs}$ are presented in Figure 4-75.

The $I_{SC}$ value in the datasheet is not for example an average value of the collector current during a short-circuit but determined by applying the turn-off point current and the $I_C$ decrease rate during the pulse, as presented in Figure 4-76. The method applied to the $I_{SC}$ determination leads to an (almost) equal $I_{C,knee}$ and $I_{SC}$ if the IGBT self-heating during the SC pulse is modelled too weak or if it is not modelled at all.
Possible reasons for the different $I_{SC,ave}$ in the datasheet and the Model1 simulation are inaccurate $I_C$ modelling as a function of $T_j$ and/or inaccurate $I_C$ modelling as a function of $V_{DC}$. In Model1, $I_C$ is defined as a function of $T_j$ or $V_{DC}$ by using the transfer characteristics from the datasheet and extrapolating points for values $T_j > 150 \, ^\circ C$ to determine the $T_j$ dependence or applying measurement data to determine the $V_{DC}$ dependence. Both of these can lead to imprecision in the $I_C$ estimation as complete $I_C$ data as a function of $T_j$ and $V_{DC}$ are not available. Because there are no measurement data for this operating point available, a detailed analysis of the error sources in the $T_{j,max}$ calculation is not possible.

**Discussion of the short-circuit behaviour as a function of $T_a$**

The results of this section show that a minor change in the ambient temperature does not significantly affect the IGBT short-circuit behaviour. Considering the measured/simulated quantities, the collector current waveform is the only one that shows a visible change as a function of temperature. However, even though the change in the measured waveform is small, it can be compared with the change in the simulation waveforms. The behaviour of the results of Model1 is very similar to the measurement, which shows that the proposed method where the IGBT chip thermal capacity is used for the chip temperature estimation is feasible. In contrast, the results of Model2 do not show significant variation as a function of ambient temperature.

Because measurement results are not available for the operating point where the short-circuit data in the datasheet are determined, a comparison of the measurement and the simulation cannot be made in this operating point, but the simulation results can be
compared directly with the datasheet values. Both the simulation models give reasonable
short-circuit current results when compared with $I_{SC}$ from the datasheet. $I_{SC}$ from Model1
is slightly below $I_{SC}$ from the datasheet, whereas the result from Model2 is slightly above
the datasheet value. With some assumptions, $I_{SC}$ can be used to calculate the maximum
chip temperature $T_{j,max}$ for a certain short-circuit pulse length. In this comparison, the
results are similar to the $I_{SC}$ comparison. $T_{j,max}$ calculated from Model1 $I_{SC}$ is slightly
below $T_{j,max}$ calculated from the datasheet $I_{SC}$, whereas $T_{j,max}$ calculated from Model2 $I_{SC}$
is slightly above it. However, the short-circuit data in the datasheet are very limited, and
thus, far-reaching conclusions from the comparison of the simulations and the datasheet
information should not be made.

Overall, Model1 behaves very similarly to the measurements when the temperature is
changed. Model2 can describe the effect of $T_j$ on $I_C$, but a drawback in Model2 is that it
does not update its junction temperature continuously or the power loss/junction
temperature calculation gives inaccurate results. Thus, the self-heating effect does not
occur correctly in the $I_C$ waveforms as was also observed in Section 4.4.4.
5 Conclusions and Discussion

From the modelling perspective, the IGBT short-circuit operation is a complex problem. The IGBT chip itself has a very non-linear behaviour in different operating points, and the behaviour is strongly affected by the auxiliary circuit parameters in the commutation circuit. This causes a coupling between the main current and gate circuitry, which has to be taken into account when analysing the short-circuit behaviour. Furthermore, during a short-circuit, the IGBT chip is in a very dynamic thermal state, which also affects the currents and voltages at the IGBT main connectors. In many cases, these aspects are modelled by numerical or analytical models, the characterization of which requires detailed information about the IGBT chip structure and the semiconductor material parameters. However, as presented in this study, also simplified behavioural models can be used to describe the IGBT short-circuit behaviour. Naturally, when the model complexity is reduced, the accuracy of the model may decrease, which should be kept in mind when considering the possible use of simple models.

The objective of the study was to investigate the usability of behavioural IGBT models for modelling of short-circuit operation. Moreover, a new behavioural model, with a special focus on short-circuit operation modelling, was developed in the study. This aim is particularly important, because as shown in the literature survey in Section 2.5, models of this kind have not been used for short-circuit modelling so far. The initial objective was to achieve a model that can be characterized only with datasheet information, but this objective was not accomplished to the full. Certain phenomena or parameter variation, such as $I_{C,sat}$ as a function of $V_{DC}$ or $C_{GG}$ voltage dependence, are so complex that they cannot be solved without detailed information of the IGBT chip structure and more complex models. To overcome this problem, some model parameters were adjusted with the help of measurement results to achieve a satisfactory modelling accuracy. The simulation results of the developed model (Model1) were compared with the measurement results and also with results obtained with the IGBT model included in the commercially available circuit simulation software (Model2). With this comparison, the applicability of the models could be analysed. At a general level, the simulation results show good agreement with the measurements, even though there are some limitations in the usability of the models. The main observations of the limitations are presented in Section 3.4.

The comparison of the simulation results and measurements was made as a function of the DC voltage $V_{DC}$, the gate turn-off resistor $R_{g,off}$, the short-circuit pulse length $t_{SC}$, and the ambient temperature $T_{a}$. Furthermore, a comparison was conducted between the $V_{CE}$, $I_{C}$, and $V_{GE}$ waveforms and the parameters that can be determined from previous waveforms. Owing to the structure of the behavioural models, the model optimization has to be carried out for some specific operating point, and the results in other operating points are determined based on estimation of the operating-point-dependent parameters. Therefore, a common feature of behavioural models is that the modelling accuracy may be reduced when the operating point is changed from the operating point where the model is optimized. In this study, Model1 was tuned for $V_{DC} = 750 \text{ V}$, $R_{g,off} = 4.7 \Omega$, $t_{SC} = 12.5 \mu$s,
and $T_a = 25\, ^\circ C$. The selection of $V_{DC}$ was based on the voltage that can be in effect across the investigated component when it is assembled to a two-level inverter connected to a 400 V grid. The optimization point for $t_{SC}$ was selected to be 12.5 µs, because the self-heating effect, which is very significant in short-circuit current modelling, is not clearly seen if the pulse length is too short. Moreover, the datasheet information is commonly given at room temperature, and thus, the optimization point for $T_a$ was selected to be 25 °C. The datasheet does not give information about the gate turn-off resistor for short-circuit operation, and therefore, it is not clear which value should be used as the optimization point for $R_{g,off}$. Thus, the optimization point $R_{g,off} = 4.7 \, \Omega$ was only a selection from the $R_{g,off}$ range used in the measurements. The optimization of Model2 was done automatically by the characterization tool as described in Section 3.2.1. Because Model2 is a black box for the user and the simulation software manual does not give detailed information about the optimization process, the operating point for optimization was not known. Nevertheless, Model2 was used as the reference model in this study, and therefore, it is not necessary to know all its details here.

As presented in Section 4.4.1, Model1 gives sufficient results for $V_{CE}$ and $I_C$ when $V_{DC}$ is close to the nominal voltage. However, the $V_{GE}$ waveform simulated with Model2 is closer to the measured one than the waveform simulated with Model1. Thus, it seems that the IGBT gate-side modelling was more successful in Model2 than in Model1. The main focus in the development of Model1 was on $V_{CE}$ and $I_C$ waveforms to limit the scope of the study, but of course, if the accuracy of $V_{GE}$ is improved, a better overall accuracy can be achieved.

When $V_{DC}$ is reduced further from the nominal voltage, the accuracy of both models decreases as presented in Section 4.4.2. Even though it is not common that an IGBT has to operate at very low $V_{DC}$ levels, for example when considering two-level inverters there are some topologies in which the voltage across the component is much lower than the nominal value. Thus, it is important to also analyse the short-circuit behaviour with a low $V_{DC}$. Furthermore, as presented in Sections 2.2.7 and 2.3, there is a specific IGBT failure mode that is more likely to occur at low voltage levels. At low $V_{DC}$ levels, the IGBT can be destroyed during a short-circuit by a high-frequency $V_{GE}$ oscillation, which can cause gate oxide breakdown and consequently, a loss of component controllability. The reason for oscillation is the time-varying collector-gate capacitance (discussed in Section 2.2.7). However, owing to the complexity of this phenomenon, behavioural models applied in this study cannot be used to describe high-frequency $V_{GE}$ oscillation. Short-circuit modelling at low $V_{DC}$ levels is difficult for two reasons. First, $I_{C,sat}$ is voltage dependent according to Eq. (2.13), where the voltage dependence is determined by $\alpha_{PNP}$ as presented in Section 2.2.3. Furthermore, accurate definition of $\alpha_{PNP}$ requires detailed information of the IGBT structure. Secondly, the transient states of a short-circuit event are essentially determined by the terminal capacitance $C_{CG}$, which is also voltage dependent. The value of $C_{CG}$ depends on the depletion layer width inside the IGBT chip, and it has very non-linear behaviour as a function of voltage. Furthermore, according to (Yang et al., 2015) and (Tominaga et al., 2011), $C_{CG}$ also depends on current, which makes the $C_{CG}$ estimation even more complicated. To sum up, accurate determination of $\alpha_{PNP}$ and $C_{CG}$
5.1 Concluding remarks

as a function of voltage and current is not possible only with datasheet information, and the estimation methods for the short-circuit behaviour voltage dependence applied in this study can reach only a limited accuracy.

When comparing the simulation results with the measured values as a function of $R_{g,\text{off}}$, Model1 behaves quite similarly to the case where the simulation results are compared as a function of $V_{DC}$. At low $R_{g,\text{off}}$ values the simulation results with Model1 are very close to the measurements, but with a high resistance value ($R_{g,\text{off}} = 22 \, \Omega$) the accuracy of the model decreases. However, the results with Model1 as a function of $R_{g,\text{off}}$ are, in general, better than the results of Model2. The value of $R_{g,\text{off}}$ has an effect on the maximum value of $V_{GE}$ at the beginning of a short-circuit pulse as a result of the displacement current through $C_{CG}$. Thus, modelling of $C_{CG}$ has a significant effect on the modelling accuracy when $R_{g,\text{off}}$ is varied. Therefore, according to the results presented in Section 4.4.3, the methods used to model $C_{CG}$ in Model1 are more accurate than the methods used in Model2. Because this study is focused only on investigating short-circuit operation, the above conclusions hold only for this particular case.

The IGBT short-circuit current is also determined by the chip temperature, which changes significantly during a short-circuit pulse as a result of the high power losses generated in the IGBT chip. Because of the short time range, traditional thermal network parameters commonly given in the component datasheet are not useful to determine the chip temperature in short-circuit operation. Model1 includes a chip thermal model, which is used to simulate the chip temperature during a short-circuit. This temperature is then used to modify the IGBT transfer characteristics to take the self-heating effect into account. The results presented in Section 4.4.4 and 4.4.5 show that this method can be applied to describe the self-heating effect. Model2 applies traditional thermal network parameters to estimate the IGBT temperature, and the accuracy of the results is not as good as with the method used in Model1. Moreover, in Model1, all parallel-connected IGBT chips are assumed to be equally heated, which is not true in an actual IGBT module. Owing to the unequal current sharing between the parallel-connected chips in the IGBT module, the temperatures of the chips are not equal in short-circuit operation. This causes an inaccuracy in the simulation results of Model1, but the accuracy is still better than when using thermal network parameters from the component datasheet.

Various challenges arise when attempting to achieve a simple simulation model for the IGBT short-circuit behaviour. First and foremost, an IGBT is a very complex component, which includes features from the MOSFET and the BJT. Accurate simulation of the IGBT short-circuit behaviour requires solving of electron and hole currents that are flowing through the MOSFET and BJT parts of the component. In the behavioural models used in this study, the short-circuit current is not separated into electron and hole currents, but the total short-circuit current is used to describe the current flowing through the
Conclusions and Discussion

Component. Hence, it is not possible to achieve accurate modelling for all phenomena occurring in the short-circuit.

Furthermore, various parameters, such as temperature, external circuit parameters, and gate drive conditions, influence the IGBT short-circuit behaviour. The effect of chip temperature was discussed in the previous chapter and in Section 2.2.4. During a short-circuit, the temperature distribution in the IGBT is not uniform but the top of the chip is heated more than the bottom part, which is usually connected to the base plate of the IGBT module. Usually, some numerical modelling method is required if the temperature distribution has to be modelled accurately. According to the results of this study, the accuracy of behavioural models can be increased even with a simple chip thermal model used in Model1.

Considering the external circuit parameters, the inductance of the busbars has the major contribution to the modelling accuracy in short-circuit conditions. In the short-circuit Type I, the voltage across the IGBT is always high, but because of the changing current in the transient state and the inductance of the busbars, the voltage changes significantly at the short-circuit turn-on and turn-off. This voltage variation also affects $V_{GE}$, which, again, has an effect on $I_{C,sat}$. Moreover, at the short-circuit turn-off, a very high voltage spike occurs across the IGBT, which can cause IGBT destruction if the critical voltage level is exceeded. Thus, modelling of the busbar inductance has to be performed with a sufficient accuracy when using the presented IGBT models for short-circuit modelling. However, it does not suffice to model the inductance correctly, but also the transient state $\frac{di}{dt}$ has to be modelled accurately. The inductance modelling method itself is not in the scope of the study; nevertheless, the method applied provides a reasonable accuracy in the inductance modelling as presented in Section 3.3.

The gate drive conditions also affect the IGBT short-circuit behaviour, but the gate driver is excluded from the study. For example the $V_{GE}$ turn-on and turn-off voltage levels should be considered if the effect of the gate driver has to be analysed in detail. Furthermore, the IGBT gate driver usually includes some protection features, which contribute to the $V_{GE}$ waveform and thereby to $I_C$ and $V_{CE}$ in a short-circuit. In this study, only a simple gate driver without any protection features was used to ensure that the effect of the gate driver on the IGBT short-circuit behaviour was as small as possible.

Even though the short-circuit operation of the IGBT is a very complex case, also simple methods examined and presented in this study can be used to model this operation. The accuracy of Model1 and Model2 is not, and cannot be, as high as with more complex models, but the usability of the presented models is better because basically all the required data for model characterization are publicly available. Furthermore, the characterization process is fast and simple. The models can be used for example in the preliminary design phase of a power electronic device, such as a frequency converter, and to examine the effects of a short-circuit event in larger electric systems. In many cases, the short-circuit operation of power electronic devices is investigated with prototypes. However, by simulations, the number of required prototype cycles can be reduced. In
larger electric systems, prototypes cannot be used to investigate the effects of a short-circuit, and thus, simulations are the only option. If the applied simulation models are complex, it may be necessary to reduce the size of the investigated system to achieve a reasonable simulation time. Thus, simple simulation models enable simulation of larger units. Furthermore, simple models can be implemented into HIL systems, where hardware is used in combination with simulation models to investigate the operation of hardware by replacing a part of the prototype with a simulation model.

Not-so-complex IGBT models are not commonly used for short-circuit modelling, and therefore, it is necessary to demonstrate the usability of such models for this type of modelling in detail, as it is done in this study. Moreover, the presented models and methods can be further improved and investigated. To this end, future work outside the scope of the present study will be discussed in the following chapter.
6 Future Work

Some interesting questions and topics of possible future work have arisen in the course of the study. For example, within the scope of the study it was not possible to investigate the behaviour of the modelling accuracy when the circuit inductance is varied. This is an important topic if IGBT models are used for instance in the design process of a power electronic device. As presented above, external circuit parameters have an effect on the IGBT short-circuit behaviour, and it is common that during a design process the busbar structure (i.e., the circuit inductance) is one of the design parameters that is varied.

Furthermore, both the presented IGBT models use transfer characteristics from the datasheet in the model characterization. However, the characteristics represent only a limited $V_{GE}$ range, which does not include the $V_{GE}$ level (+15 V) that is used commonly in the IGBT on-state. As a topic of future work, it would be interesting to investigate how the models behave if the whole transfer characteristics up to $V_{GE} = +15$ V can be determined for example with measurements or numerical simulations, and this characteristic is then used for the characterization of behavioural models.

Moreover, an interesting topic of future work could be improvement of the chip thermal model. In Model1, a simple thermal model, which assumes uniform temperature distribution, was used. As presented in Section 2.2.4, the temperature distribution is not uniform during a short-circuit, but the top of the chip is heated more than the bottom part. By improving the chip thermal model for example by using numerical modelling methods, it could be possible to achieve a better accuracy to describe the self-heating effect. This naturally requires that the IGBT transfer characteristics as a function of temperature are known with a sufficient accuracy.

As the $C_{CG}$ variation as a function of voltage and current has a significant effect on the short-circuit transient states, also further investigation of this variation might improve the overall accuracy of the IGBT models. One possible way is to model $C_{CG}$ as a function of voltage and current with the TCAD software and use these data for the IGBT circuit simulation model. In this case, detailed information of the IGBT structure is needed, but if these data are available, more accurate data of the $C_{CG}$ operating point dependence can be extracted.

One wider topic of future work can be experimental investigation of a large number of IGBT samples to determine the statistical distribution of the IGBT short-circuit parameters. Because only a few IGBT modules were tested in this doctoral dissertation, the statistical distribution of the parameters could not be determined. However, knowledge of the statistical distribution of the IGBT short-circuit parameters is important when defining the IGBT model accuracy.
References


References


Appendix A: Model1 characterization parameters

The numbers from 1 to 3 in Table A-1 represent electrical characterization parameters for Model1, whereas the numbers 4–7 are used for the thermal model.

\( K_{VCE} \) is the parameter that describes the \( I_{C,\text{sat}} \) voltage dependence. This parameter is used to determine transfer characteristics for the \( V_{CE} \) levels that are not presented in the component datasheet.

\( K_{CCG} \) is used to describe \( C_{CG} \) as a function of \( I_C \) (Eq. 2.39).

\( K_{CGE} \) is an experimentally determined coefficient for \( C_{GE} \) to adjust the \( V_{GE} \) delay in simulations to correspond with the measurements.

The thermal parameters for the IGBT chip are as follows:

\( d \)  
IGBT chip thickness

\( A \)  
Surface area of the IGBT chip

\( \rho \)  
Density of silicon

\( c_{th} \)  
Specific heat capacity of silicon

Table A-1 Model1 characterization parameters

<table>
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<th>Number</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
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<tr>
<td>1</td>
<td>( K_{VCE} )</td>
<td>1.22</td>
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<tr>
<td>2</td>
<td>( K_{CCG} )</td>
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<td>3</td>
<td>( K_{CGE} )</td>
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<tr>
<td>4</td>
<td>( d )</td>
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<td>m</td>
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<tr>
<td>5</td>
<td>( A )</td>
<td>142e-6</td>
<td>m²</td>
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<tr>
<td>6</td>
<td>( \rho )</td>
<td>2329</td>
<td>kg/m³</td>
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<tr>
<td>7</td>
<td>( c_{th} )</td>
<td>713</td>
<td>Ws/(kg*K)</td>
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Table A-2 Description of components in Figure 3-2

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<tr>
<th>Symbol</th>
<th>Description</th>
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<tr>
<td>( V_{dc} )</td>
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<td>( L_{DClink} )</td>
<td>Inductance of the DC capacitor</td>
</tr>
<tr>
<td>( C_{DClink} )</td>
<td>Capacitance of the DC capacitor</td>
</tr>
<tr>
<td>( R_{DClink} )</td>
<td>Resistance of the DC capacitor</td>
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<tr>
<td>( L_{clamp} )</td>
<td>Inductance of the snubber capacitor</td>
</tr>
<tr>
<td>( C_{clamp} )</td>
<td>Capacitance of the snubber capacitor</td>
</tr>
<tr>
<td>( R_{clamp} )</td>
<td>Resistance of the snubber capacitor</td>
</tr>
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<td>PlusPlate:T_P_Cap</td>
<td>DC busbar connection for the DC capacitor plus terminal</td>
</tr>
<tr>
<td>MinusPlate:T_M_Cap</td>
<td>DC busbar connection for the DC capacitor minus terminal</td>
</tr>
<tr>
<td>PlusPlate:T_P_IGBT</td>
<td>DC busbar connection for IGBT module terminals 9 and 11</td>
</tr>
<tr>
<td>MinusPlate:T_M_IGBT</td>
<td>DC busbar connection for IGBT module terminals 10 and 12</td>
</tr>
<tr>
<td>T911:T_911_M</td>
<td>IGBT module terminals 9 and 11</td>
</tr>
<tr>
<td>T1012:T_1012_M</td>
<td>IGBT module terminals 10 and 12</td>
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<tr>
<td>T8:T_8</td>
<td>IGBT module terminal 8</td>
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<tr>
<td>T911:T_911_chip</td>
<td>Internal busbar of the IGBT module, collector of the top IGBT</td>
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## Appendix A: Model1 characterization parameters

<table>
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<tr>
<th>Parameter</th>
<th>Description</th>
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<tr>
<td>T1012:T_1012_chip</td>
<td>Internal busbar of IGBT module, emitter of the bottom IGBT</td>
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<td>Resistance of the load</td>
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<tr>
<td>Lload</td>
<td>Inductance of the load</td>
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<td>FWD</td>
<td>Freewheeling diode</td>
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<tr>
<td>Vce</td>
<td>Current-controlled voltage source (output characteristics)</td>
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<tr>
<td>Ic</td>
<td>Controlled current source (transfer characteristics)</td>
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<td>Transchar</td>
<td>Transfer characteristics (function of $V_{GE}$, $V_{CE}$, and $T_j$)</td>
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<td>Non-linear capacitance $C_{CG}$</td>
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<td>Ccg_char</td>
<td>$C_{CG}$ characteristics (function of $V_{CE}$ and $I_C$)</td>
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<td>Capacitance $C_{GE}$</td>
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<tr>
<td>Rgon</td>
<td>External gate turn-on resistance</td>
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<tr>
<td>Rgoff</td>
<td>External gate turn-off resistance</td>
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<tr>
<td>Vge</td>
<td>Gate-emitter voltage</td>
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<td>Short-circuit power loss source for the chip thermal model</td>
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<td>IGBT chip thermal capacity</td>
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<td>Tj</td>
<td>IGBT chip temperature</td>
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<td>Turn-on transition (state machine of the IGBT control)</td>
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<tr>
<td>TRANS2</td>
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### Measurements

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Appendix B: Model2 parameter list

Table B-1 Model2 IGBT parameters

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### Appendix B: Model2 parameter list

#### Table B-2 Model2 thermal parameters

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#### Table B-3 Model2 diode parameters

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#### Table B-4 Model2 IGBT module parameters

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Appendix C: Gate driver schematics
Appendix D: Components of the short-circuit test setup

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<td>IGBT module</td>
<td>1</td>
<td>Infineon</td>
<td>FF1400R12IP4</td>
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<tr>
<td>DC capacitors</td>
<td>2</td>
<td>Electronicon</td>
<td>E50.S34-135N10</td>
</tr>
<tr>
<td>Gate driver</td>
<td>4</td>
<td>Custom-made</td>
<td></td>
</tr>
<tr>
<td>Clamp capacitors</td>
<td>5</td>
<td>Vishay</td>
<td>386M MKP F1351</td>
</tr>
<tr>
<td>Current probes</td>
<td>6</td>
<td>PEM</td>
<td>CWT30</td>
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<tr>
<td>Voltage probe (V_{\text{CH}})</td>
<td>7</td>
<td>Tektronix</td>
<td>P5202A</td>
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<tr>
<td>Voltage probe (V_{\text{CE}})</td>
<td>8</td>
<td>Tektronix</td>
<td>P5205A</td>
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<tr>
<td>Oscilloscope</td>
<td>9</td>
<td>Agilent Technologies</td>
<td>MSO-X 3054A</td>
</tr>
<tr>
<td>Signal generator</td>
<td>10</td>
<td>Agilent Technologies</td>
<td>33120A</td>
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</table>
**Appendix E: Error percentages of $V_{DC} = 350$ V and 750 V**

<table>
<thead>
<tr>
<th>$V_{DC}$</th>
<th>Model1</th>
<th>Model2</th>
<th>Meas.</th>
<th>Model1</th>
<th>Model2</th>
<th>Meas.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CE,max}$ [V]</td>
<td>533.26</td>
<td>500.33</td>
<td>544.32</td>
<td>679.31</td>
<td>649.95</td>
<td>693.89</td>
</tr>
<tr>
<td>Abs. diff. [V]</td>
<td>11.06</td>
<td>43.99</td>
<td>-</td>
<td>14.58</td>
<td>43.94</td>
<td>-</td>
</tr>
<tr>
<td>Diff. %</td>
<td>2.03 %</td>
<td>8.08 %</td>
<td>-</td>
<td>2.10 %</td>
<td>6.33 %</td>
<td>-</td>
</tr>
<tr>
<td>$I_{C,max}$ [A]</td>
<td>8449.90</td>
<td>8159.10</td>
<td>7141.40</td>
<td>8364.40</td>
<td>8062.60</td>
<td>7386.50</td>
</tr>
<tr>
<td>Abs. diff. [A]</td>
<td>1308.50</td>
<td>1017.70</td>
<td>-</td>
<td>977.90</td>
<td>676.10</td>
<td>-</td>
</tr>
<tr>
<td>Diff. %</td>
<td>18.32 %</td>
<td>14.25 %</td>
<td>-</td>
<td>13.24 %</td>
<td>9.15 %</td>
<td>-</td>
</tr>
<tr>
<td>Abs. diff. [J]</td>
<td>1.44</td>
<td>2.79</td>
<td>-</td>
<td>1.39</td>
<td>3.20</td>
<td>-</td>
</tr>
<tr>
<td>Diff. %</td>
<td>11.08 %</td>
<td>16.26 %</td>
<td>-</td>
<td>15.87 %</td>
<td>19.67 %</td>
<td>-</td>
</tr>
<tr>
<td>$t_{rise}$ [μs]</td>
<td>1.90</td>
<td>1.43</td>
<td>1.71</td>
<td>1.74</td>
<td>1.38</td>
<td>1.71</td>
</tr>
<tr>
<td>Abs. diff. [μs]</td>
<td>0.19</td>
<td>0.28</td>
<td>-</td>
<td>0.03</td>
<td>0.34</td>
<td>-</td>
</tr>
<tr>
<td>Diff. %</td>
<td>18.94 %</td>
<td>36.60 %</td>
<td>-</td>
<td>11.80 %</td>
<td>27.29 %</td>
<td>-</td>
</tr>
<tr>
<td>$d\Delta/dt_{rise}$ [A/s]</td>
<td>3.64E+09</td>
<td>4.64E+09</td>
<td>3.35E+09</td>
<td>3.90E+09</td>
<td>4.73E+09</td>
<td>3.45E+09</td>
</tr>
<tr>
<td>Abs. diff. [A/s]</td>
<td>2.88E+08</td>
<td>1.29E+09</td>
<td>-</td>
<td>4.51E+08</td>
<td>1.28E+09</td>
<td>-</td>
</tr>
<tr>
<td>Diff. %</td>
<td>8.59 %</td>
<td>38.56 %</td>
<td>-</td>
<td>13.07 %</td>
<td>37.23 %</td>
<td>-</td>
</tr>
<tr>
<td>$\tau_{on}$ [μs]</td>
<td>0.33</td>
<td>0.82</td>
<td>0.25</td>
<td>0.31</td>
<td>0.82</td>
<td>0.27</td>
</tr>
<tr>
<td>Abs. diff. [μs]</td>
<td>0.07</td>
<td>0.57</td>
<td>-</td>
<td>0.04</td>
<td>0.56</td>
<td>-</td>
</tr>
<tr>
<td>Diff. %</td>
<td>29.05 %</td>
<td>122.90 %</td>
<td>-</td>
<td>14.88 %</td>
<td>210.17 %</td>
<td>-</td>
</tr>
<tr>
<td>$d\Delta/ dt_{fall}$ [A/s]</td>
<td>1.57E+10</td>
<td>6.24E+09</td>
<td>1.88E+10</td>
<td>1.63E+10</td>
<td>6.24E+09</td>
<td>1.86E+10</td>
</tr>
<tr>
<td>Abs. diff. [A/s]</td>
<td>3.16E+09</td>
<td>1.26E+10</td>
<td>-</td>
<td>2.29E+09</td>
<td>1.23E+10</td>
<td>-</td>
</tr>
<tr>
<td>Diff. %</td>
<td>16.80 %</td>
<td>66.86 %</td>
<td>-</td>
<td>12.35 %</td>
<td>66.37 %</td>
<td>-</td>
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</table>
## Appendix F: Error percentages of $R_{g,\text{off}} = 3.3\ \Omega$ and $22\ \Omega$

<table>
<thead>
<tr>
<th>$R_{g,\text{off}}$</th>
<th>3.3 $\Omega$</th>
<th>22 $\Omega$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CE,\text{max}}$ [V]</td>
<td>949.54</td>
<td>1005.40</td>
</tr>
<tr>
<td>Abs. diff. [V]</td>
<td>17.57</td>
<td>73.43</td>
</tr>
<tr>
<td>Diff. %</td>
<td>1.89 %</td>
<td>7.88 %</td>
</tr>
<tr>
<td>$I_{C,\text{max}}$ [A]</td>
<td>8072.50</td>
<td>7921.10</td>
</tr>
<tr>
<td>Abs. diff. [A]</td>
<td>509.80</td>
<td>358.40</td>
</tr>
<tr>
<td>Diff. %</td>
<td>6.74 %</td>
<td>4.74 %</td>
</tr>
<tr>
<td>$V_{CE,\text{max}}$ [V]</td>
<td>16.92</td>
<td>16.65</td>
</tr>
<tr>
<td>Abs. diff. [V]</td>
<td>1.22</td>
<td>0.95</td>
</tr>
<tr>
<td>Diff. %</td>
<td>7.77 %</td>
<td>6.07 %</td>
</tr>
<tr>
<td>$E_{SC}$ [J]</td>
<td>33.00</td>
<td>36.37</td>
</tr>
<tr>
<td>Abs. diff. [J]</td>
<td>0.48</td>
<td>3.85</td>
</tr>
<tr>
<td>Diff. %</td>
<td>1.46 %</td>
<td>11.83 %</td>
</tr>
<tr>
<td>$t_{\text{rise}}$ [µs]</td>
<td>1.51</td>
<td>1.31</td>
</tr>
<tr>
<td>Abs. diff. [µs]</td>
<td>0.12</td>
<td>0.32</td>
</tr>
<tr>
<td>Diff. %</td>
<td>7.12 %</td>
<td>19.83 %</td>
</tr>
<tr>
<td>$d/dt_{\text{rise}}$ [A/s]</td>
<td>4.27E+09</td>
<td>4.85E+09</td>
</tr>
<tr>
<td>Abs. diff. [A/s]</td>
<td>5.55E+08</td>
<td>1.14E+09</td>
</tr>
<tr>
<td>Diff. %</td>
<td>14.93 %</td>
<td>30.68 %</td>
</tr>
<tr>
<td>$t_{\text{fall}}$ [µs]</td>
<td>0.22</td>
<td>0.79</td>
</tr>
<tr>
<td>Abs. diff. [µs]</td>
<td>0.01</td>
<td>0.56</td>
</tr>
<tr>
<td>Diff. %</td>
<td>4.39 %</td>
<td>244.96 %</td>
</tr>
<tr>
<td>$d/dt_{\text{fall}}$ [A/s]</td>
<td>1.99E+10</td>
<td>5.93E+09</td>
</tr>
<tr>
<td>Abs. diff. [A/s]</td>
<td>8.65E+08</td>
<td>1.31E+10</td>
</tr>
<tr>
<td>Diff. %</td>
<td>4.54 %</td>
<td>68.90 %</td>
</tr>
</tbody>
</table>
Appendix G: Error percentages of $t_{SC} = 12.5 \, \mu s$ and $V_{DC} = 750 \, V / 400 \, V$

<table>
<thead>
<tr>
<th>$V_{bc}$</th>
<th>750 V</th>
<th>400 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abs. diff. [V]</td>
<td>13.50</td>
<td>18.75</td>
</tr>
<tr>
<td>Diff. %</td>
<td>1.49 %</td>
<td>2.07 %</td>
</tr>
<tr>
<td>$I_{C,max}$ [A]</td>
<td>8594.30</td>
<td>8080.10</td>
</tr>
<tr>
<td>Abs. diff. [A]</td>
<td>246.00</td>
<td>268.20</td>
</tr>
<tr>
<td>Diff. %</td>
<td>2.95 %</td>
<td>3.21 %</td>
</tr>
<tr>
<td>$V_{GE,max}$ [V]</td>
<td>17.33</td>
<td>16.83</td>
</tr>
<tr>
<td>Abs. diff. [V]</td>
<td>1.45</td>
<td>0.96</td>
</tr>
<tr>
<td>Diff. %</td>
<td>9.15 %</td>
<td>6.04 %</td>
</tr>
<tr>
<td>$E_{SC}$ [J]</td>
<td>51.87</td>
<td>55.90</td>
</tr>
<tr>
<td>Abs. diff. [J]</td>
<td>0.93</td>
<td>3.10</td>
</tr>
<tr>
<td>Diff. %</td>
<td>1.75 %</td>
<td>5.88 %</td>
</tr>
<tr>
<td>$t_{rise}$ [µs]</td>
<td>1.60</td>
<td>1.33</td>
</tr>
<tr>
<td>Abs. diff. [µs]</td>
<td>0.18</td>
<td>0.45</td>
</tr>
<tr>
<td>Diff. %</td>
<td>9.94 %</td>
<td>25.48 %</td>
</tr>
<tr>
<td>$d/d_{t_{rise}}$ [A/s]</td>
<td>4.29E+09</td>
<td>4.87E+09</td>
</tr>
<tr>
<td>Abs. diff. [A/s]</td>
<td>5.36E+08</td>
<td>1.12E+09</td>
</tr>
<tr>
<td>Diff. %</td>
<td>14.29 %</td>
<td>29.86 %</td>
</tr>
<tr>
<td>$t_{fall}$ [µs]</td>
<td>0.27</td>
<td>0.81</td>
</tr>
<tr>
<td>Abs. diff. [µs]</td>
<td>0.01</td>
<td>0.53</td>
</tr>
<tr>
<td>Diff. %</td>
<td>3.70 %</td>
<td>184.86 %</td>
</tr>
<tr>
<td>$d/d_{t_{fall}}$ [A/s]</td>
<td>1.53E+10</td>
<td>5.84E+09</td>
</tr>
<tr>
<td>Abs. diff. [A/s]</td>
<td>3.00E+06</td>
<td>9.43E+09</td>
</tr>
<tr>
<td>Diff. %</td>
<td>0.02 %</td>
<td>61.76 %</td>
</tr>
</tbody>
</table>
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