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SIMULATION AND CHARACTERIZATION OF A FRONT-END ASIC FOR GASEOUS MUON DETECTORS

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Abstract

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The Large hadron collider at CERN will get a luminosity upgrade in 2027. To cope with the increased particle rates, the compact muon solenoid (CMS) experiment will be upgraded with new gaseous muon detectors known as GEMs. These GEMs are large area, high density detectors which will face a high particle rate. A new-front end ASIC needed to be designed for them. The chip is known as VFAT3 and it is a crucial part of the new detector, converting the analog signal from the detector into a processable digital data. In this thesis, we study the operation and properties of the VFAT3 chip.

Mixed signal simulation methods were used during the design of the chip. With these methods the digital and analog parts of the chip could be designed alongside each other. This allowed the chip to be simulated as a whole throughout the design phase, which reduces the possibility of interface problems between different design blocks. The full chip simulation model was used to study the operation and usability of the chip and it allowed the co-development of the chip design and the physical verification platform.

A dedicated verification platform was designed for the full verification and characterization of the VFAT3. The platform is based around a Kintex-7 FPGA development kit, which is controlled by software running on a PC. The chip is connected to the kit with a series of custom-designed printed circuit boards, which provide the chip with powering and communication lines.

The results of the simulation, physical verification and characterization of the VFAT3 are presented and discussed.

The VFAT3 chip was found to be a reasonable solution for the use in the large area GEM readout. The chip showed good performance under the requirements set by the higher particle rate.

Keywords: Mixed-signal simulation, Gaseous muon detectors, ASIC, front-end ASIC, Verification

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Henri Petrow
May 2021
Lappeenranta, Finland

Contents

List of publications

Publication I

Petrow, H., Aspell P., Robertis, G.D., Licciulli F., Loddo, F., Tuuva, T. (2021). High Level Verification of the VFAT3 ASIC for CMS GEM Detectors. *The Journal of Instrumentation, JINST 16 P02005*

Publication II

Petrow, H., Aspell P., Bravo, C., Dabrowski, M., Lentdecker, G.D., Leroux, P., Robertis, G.D., Irshad, A., Lenzi, T., Licciulli F., Loddo, F., Robert, F., Tavernier, F., Rosa, J., Tuuva, T. (2017). A Verification Platform to provide the Functional, Characterization and Production testing for the VFAT3 ASIC. *2017 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*

Publication III

Licciulli, F., Aspell P., Dabrowski, M., Lentdecker, G.D., Robertis, G.D., Idzik, M., Irshad, A., Loddo, **Petrow, H.**, F., Robert, F., Rosa, J., Tuuva, T. (2017). Calibration, bias and monitoring system for the VFAT3 ASIC of the CMS GEM detector. *2017 7th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)*, pp. 81-84.

Publication IV

Aspell P., Bravo, C., Dabrowski, M., Lentdecker, G.D., Robertis, G.D., Firlej, M., Fiutowski, T., Hakkarainen, T., Idzik, M., Irshad, A., Leroux, P., Licciulli F., Loddo, F., Muhammad, A., Moron, J., **Petrow, H.**, Swientek, K., Tavernier, Tuuva, T. (2018). VFAT3: A Trigger and Tracking Front-end ASIC for the Binary Readout of Gaseous and Silicon Sensors. *2018 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*

Author's contribution

Henri Petrow is the principal author and investigator in papers I and II. Dr Francesco Licciulli is the main author and investigator in paper III and Petrow took part in the simulation, test setup preparation and data taking. Dr. Paul Aspell is the main author of the paper IV and Petrow took part in the simulations, test setup preparation and conducting the experiments.

Nomenclature

ADC	Analog to digital converter
ASIC	Application-Specific Integrated Circuit
BC	Bunch crossing counter
CBM	Calibration bias and monitoring
CERN	The European Organization for Nuclear Research
CFD	Constant fraction discriminator
CMS	Compact Muon Solenoid
CSC	Cathode strip chamber
DAC	Digital to analog converter
DAQ	Data acquisition
DC	Direct current
DDR	Double data rate
DT	Drift tube
EC	Event counter
ENC	Equivalent noise charge
ESD	Electrostatic discharge
FIFO	First in, first out
FPGA	Field programmable gate array
GBT	GigaBit transceiver
GE1/1	First Triple-GEM installation slot
GE2/1	Second Triple-GEM installation slot
GEB	GEM electronics board
GEM	Gas electron multiplier
HDL	Hardware description language
HDLC	High-level data link control
HG	High gain
HL-LHC	High luminosity - large hadron collider
HV	High voltage
LHC	Large Hadron Collider
LV1A	Level 1A CMS trigger
ME0	Third Triple-GEM installation slot
MG	Medium gain
OH	Opto hybrid
PC	Personal computer
PCB	Printed circuit board
PMOS	P-type metal-oxide-semiconductor
RPC	Resistive plate chamber
RTL	Register transfer logic
SLVS	Scalable-low-voltage-signaling

SRAM	Static random-access memory
SRAM1	Buffer SRAM of the VFAT3
SRAM2	Storage SRAM of the VFAT3
VFAT2	Front-end binary very forward ATLAS and TOTEM 2
VFAT3	Front-end binary very forward ATLAS and TOTEM 3
ZCC	Zero crossing comparator

1 Introduction

The Large Hadron Collider (LHC) at CERN is to get a luminosity upgrade by 2027. The upgrade is known as the High Luminosity LHC (HL-LHC) and it is supposed to increase the luminosity of the collider from $1.6 * 10^{34} cm^{-2} s^{-1}$ to $5 * 10^{34} cm^{-2} s^{-1}$ (Bejar Alonso I., 2020). This luminosity improvement will increase the rate of collisions and due to the statistical nature of particle physics, help confirm current results and bring more rare collisions within reach of the collider. The upgrade of the collider also brings higher requirements for the detectors used in the experiment (Contardo et al., 2015). To meet these requirements, a decision was taken to upgrade the muon subsystem of the Compact Muon Solenoid (CMS) experiment with additional gas electron multiplier (GEM) detectors (Abbaneo et al., 2014a,b, 2015a,b). The CMS muon system was originally made up of three complementary gaseous muon detection technologies. Drift tubes (DT), which are installed to the CMS chamber, cover the pseudorapidity of $|\eta| < 1.2$. Cathode strip chambers (CSC), installed in the CMS endcap, cover $|\eta| > 1.2$. Resistive plate chambers (RPC), installed both in the barrel and the endcap, cover the $|\eta| < 1.6$. So originally the high eta region of $1.6 < |\eta| < 2.6$ is covered by the CSC detectors. The new GEM detectors would be installed to the high eta region of $1.6 < |\eta| < 2.2$ to complement the existing CSC detectors. This will help to reduce the muon trigger rate and improve the tracking performance in the new high luminosity environment. In the high eta region low-pT (pT$\sim$5 GeV/c) muons are misinterpreted as high-pT muons (pT $>$20 GeV/c), when only the CSC detectors are in use. By installing the additional GEM detectors, the muon angles can be measured more accurately, which makes it possible to differentiate between the low-pT and the high-pT muons (Abbaneo et al., 2014; Radogna, 2016). The GEM detectors will be placed in three locations in the CMS endcaps. The locations are shown in Figure 1.1 as GE1/1, GE2/1 and ME0 (Colaleo et al., 2015; Abbaneo et al., 2018; Simone et al., 2019). The research and development of the GEM detectors started in 2009 with the RD51 collaboration(Tytgat et al., 2018).

An existing front-end readout chip, known as VFAT2 (Aspell et al., 2007), was considered for the GEM detector. However, it is unable to cope with the increased particle rate and is not compatible with CMS requirements for high luminosity phase. Furthermore, it was not designed for gaseous detectors, and thus its shaping time is too short to collect the whole charge produced by passing particles. Consequently, a new FE-chip had to be designed. The new chip had to have a fast communication channel and a large internal memory to cope with the increased trigger rate from the CMS. To be suitable for the gaseous detectors, the shaping time of the chip should be longer than in VFAT2 (Colaleo et al., 2015).

A decision was taken to design a new front-end readout chip, to be known as VFAT3.

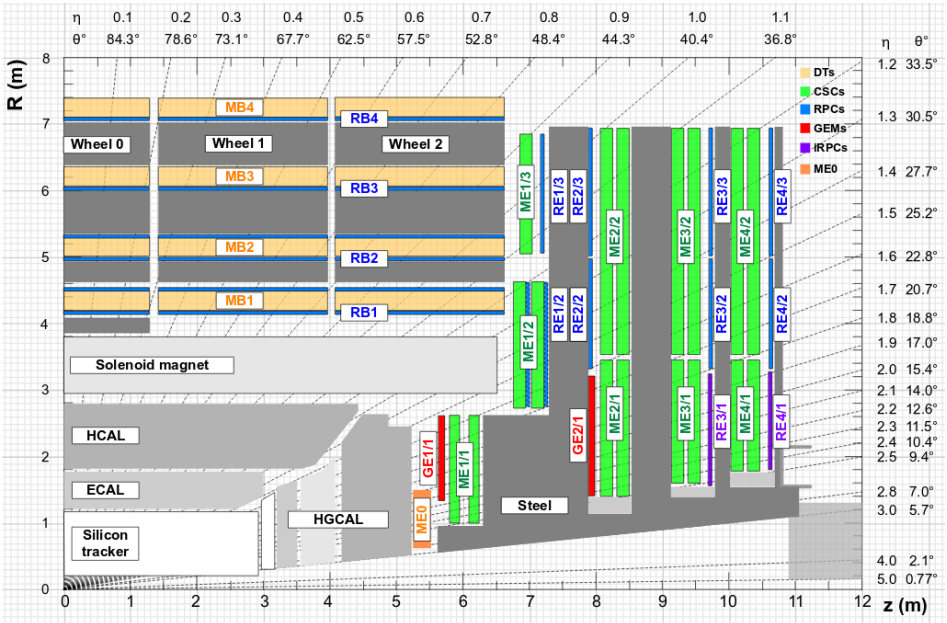

Figure 1.1: GEM positions in the CMS experiment are shown in the picture in red (GE1/1 and GE2/1) and in orange (ME0). (Collaboration, 2017).

The chip had to have 128 analog input channels and configurable components, including internal biasing DACs, ADCs, a front-end with different peaking times and gains, a constant fraction discriminator, monitoring possibilities and data packet options (Aspell et al., 2018). To implement all of the functionality desired for the chip, a large number of both analog and digital design blocks were used. These blocks are closely integrated with each other.

1.1 Gas electron multiplier technology

A gas electron multiplier (GEM) detector is made of metal-clad polymer foils which have a high density of microscopic holes in them (Sauli, 1997). A closeup of the foil can be seen in Figure 1.2. The holes are shaped as truncated double cones, with an inner diameter of $50\,\mu\mathrm{m}$ and outer diameter of $70\,\mu\mathrm{m}$. The metal foil towards the readout board is a continuous conductor, but the side facing the drift board is segmented into several high voltage sectors. This structure helps to reduce the charge that can flow from one foil and thus protects the foils against damage from discharges. Discharges are observed in GEMs and they can be damaging to the readout electronics (Utrobicic

et al., 2019; Bachmann et al., 2002). During the operation a voltage is applied between the upper and lower metal layers. This creates an electric field as high as 80 kV/cm inside the microscopic holes.

A triple-GEM chamber is made up of a stack of three GEM foils, which are spaced by a few millimeters and immersed in a gas mixture. When a charged particle passes through the gas volume it can ionize some of the gas molecules. These ionized particles then drift towards the high electric field in the holes. Once the ionized particles pass through the holes, they acquire enough kinetic energy to create secondary ionization in the next gas volume. This creates an avalanche of charged particles towards the bottom of the detector, where a readout PCB collects the charge and gives out a signal. This process is shown in Figure 1.3.

The triple-GEM technology is a popular choice for particle detectors since it has uniformity over it surface for gain, energy resolution and efficiency (Patra et al., 2017).

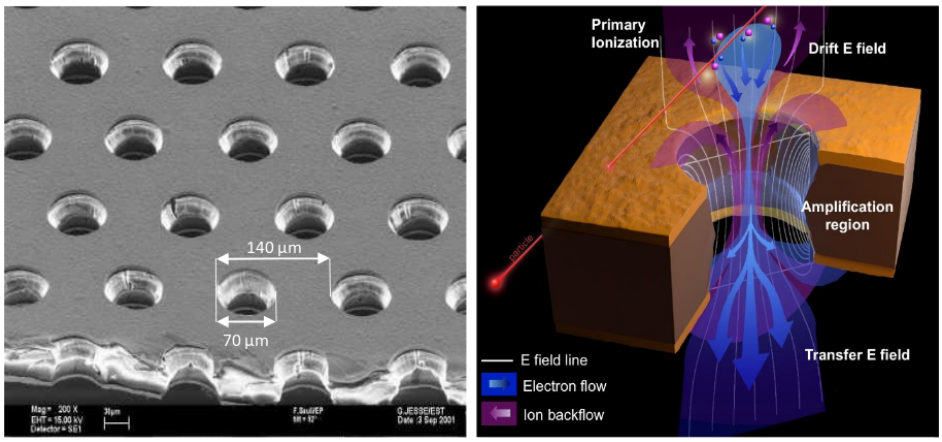

Figure 1.2: GEM structure and electric field (Collaboration, 2017).

1.2 VFAT3 front-end ASIC

This chapter presents the details of the VFAT3 front-end chip based on the **Publication III** and **Publication IV**. The VFAT3 is a front-end ASIC designed and optimized for gaseous detectors and in particular GEM detectors. With its programmable input channels, it can also be adjusted for use with silicon detectors. The design parameters come from the needs of the GEM project and the main parameters required are the following:

- 128 input channels.

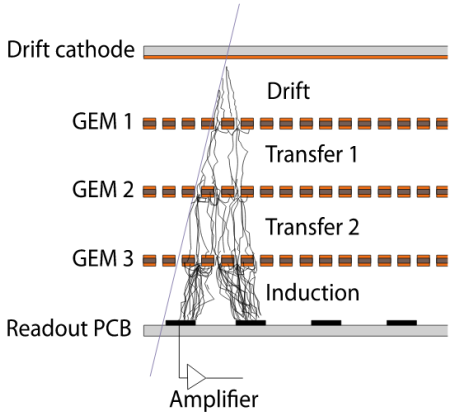

Figure 1.3: GEM operation principle (Collaboration, 2017).

- Possibility to read both positive and negative signals.
- Provide both tracking and trigger information.
- Return full granularity tracking information after LV1A trigger.
- LV1A trigger latency beyond $12.5\,\mu s$.
- Time resolution of less than 7.5 ns (with detector).
- Integrated calibration and monitoring for the input channels.
- GBT compatible interface with 320 Mbs.
- Radiation tolerant up to 100 MRads.
- Robust against single event effects.

The VFAT3 can be roughly divided into three parts, namely the analog block, the digital block and the internal ADC block. The analog block hosts the 128 input channels with constant fraction discriminators (CFD) at the end of each one and the calibration, biasing and monitoring unit (CBM). The digital block hosts the communication channels, internal SRAMs, Slow Control registers and control logic. The main functional blocks of the VFAT3 are shown in Figure 1.4.

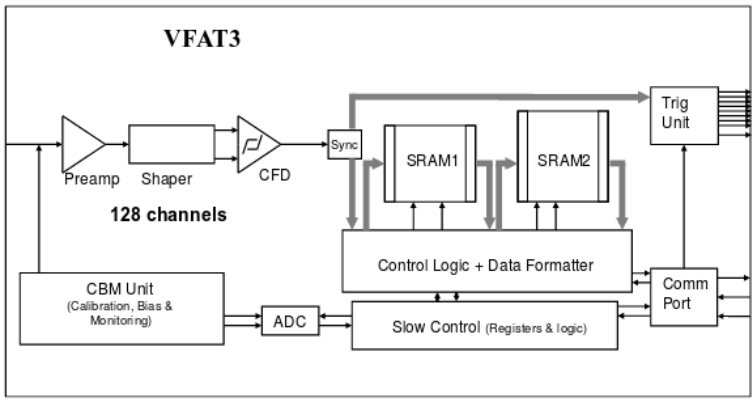

Figure 1.4: VFAT3 functional blocks: 128 input channels, CBM block, ADCs and the digital functionality (Aspell et al., 2018).

1.2.1 Analog block

As mentioned previously, the analog block includes the analog functionality of the chip. The analog functions are the input channels with the analog front end and CFD, the calibration unit, for the calibration of the chip; the biasing unit to provide adjustable biasing for the input channels; and the monitoring unit for monitoring the internal voltages and currents.

The input channels consist of an analog front-end and a CFD. The analog front-end design has four main parts: input protection, preamplifier, shaper and a single to differential amplifier. The construction of the front-end is shown in Figure 1.5.

The preamplifier's function is to convert the current caused by the input charge into a voltage. The preamplifier is implemented with a high gain amplifier and a programmable feedback capacitor and resistor, that can be changed to control the gain of the preamplifier. The shaper is a second order low pass filter comprising of two OTA-C based integrators. The shaper's function is to give the voltage output of the preamplifier a predefined peaking time. The peaking time adjustment is realized by programmable parallel capacitors at the end of each integrator. The single to differential amplifier acts as an interface between the analog front end and the CFD. It is based on a PMOS differential folded-cascode architecture and it provides further gain for the signal (Dabrowski et al., 2017).

The CFD at the end of the input channels acts as a comparator, digitizing the arrival time of the incoming signal. The constant fraction discrimination technique is used to

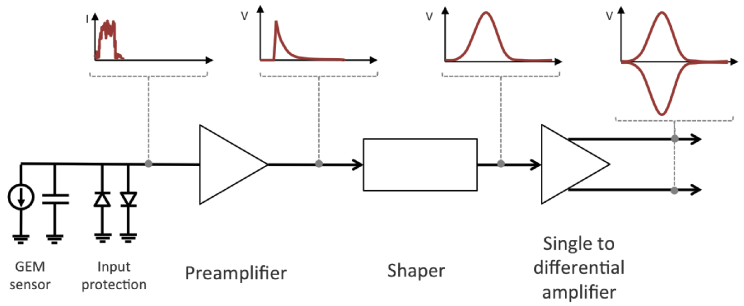

Figure 1.5: Analog part of the input channel is composed of preamplifier, shaper and the single to differential amplifier. (Dabrowski et al., 2017).

reduce the time-walk introduced in the timing information. The operation principle of it is based on detecting the zero-crossing of the bipolar pulse obtained by subtracting a fraction of the input uni-polar signal to its delayed copy. The principle is shown in Figure 1.6.

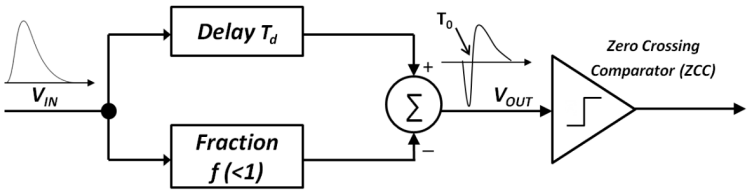

Figure 1.6: The operation principle of the zero crossing comparator (Abbaneo et al., 2016).

In VFAT3, the proposed implementation of CFD is based on a fully differential architecture for better noise rejection. The differential input signals are sent to a passive shaping network that converts them into bipolar pulses with amplitude-independent zero-crossing time. The post-amplifier then amplifies the bipolar pulses and compensates for the offset. A zero-crossing comparator (ZCC) produces a digital pulse when the signal crosses the baseline. In parallel the signal is also fed to an arming circuitry. This allows the CFD to only output a signal when a certain programmable threshold has been passed. This threshold is controlled by a global 8-bit DAC. Both the arming comparator and the ZCC also have a local DAC which allows the correction of mismatches between channels. Finally, a multiplexer allows the selection of the comparator output. For instance, it is possible to bypass the CFD and use the arming comparator output without

the time-walk correction. The principle is shown in Figure 1.7.

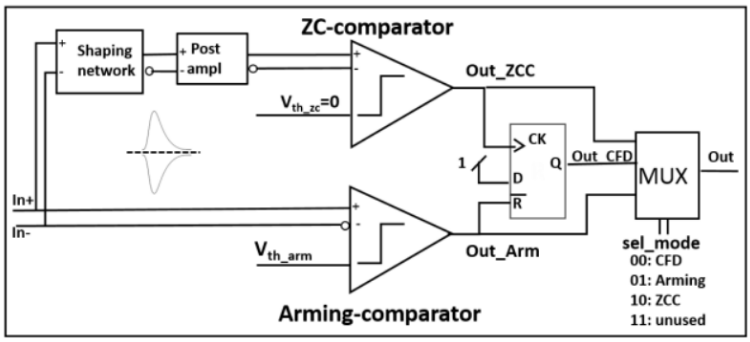

Figure 1.7: Block diagram of the constant fraction discriminator (Abbaneo et al., 2016).

A large part of the analog block is the calibration, bias and monitoring unit (CBM). It handles the calibration and biasing of the analog front-end and CFD and monitoring of the internal voltages and currents. The CBM unit is controlled and interfaced from the digital section's registers.

The VFAT3 chip's analog part is dependent on process variations and radiation damage during its lifetime. To compensate for the variations, the CBM unit provides each sensible circuit with a programmable bias. All the biases are controlled by current DACs, with 6 or 8 bits of resolution. The DACs get a current and voltage reference from a bandgap reference which is stable against the temperature and power supply variations (Kuczynska et al., 2015). The structure of the biasing system is shown in Figure 1.8

The CBM unit also provides the calibration circuitry needed for the characterization and equalization of the input channels. The circuitry can provide either voltage or current pulse to the input channels. It allows the polarity, duration and amplitude of the pulse to be determined. The pulse parameters can be changed by the slow control registers in the digital part of the chip. The amplitude for both voltage and current pulse is determined by an 8-bit DAC and the duration and polarity of the pulses can be changed by switching internal switches in a different order. The structure of the calibration system is shown in Figure 1.9

All of the reference currents and voltages can be monitored through the CBM. The monitoring system incorporates a multiplexing system to select which DAC to monitor and whether to monitor the current or the voltage. The values can then be read either by using one of the two internal ADCs or an external ADC located outside of the chip. The

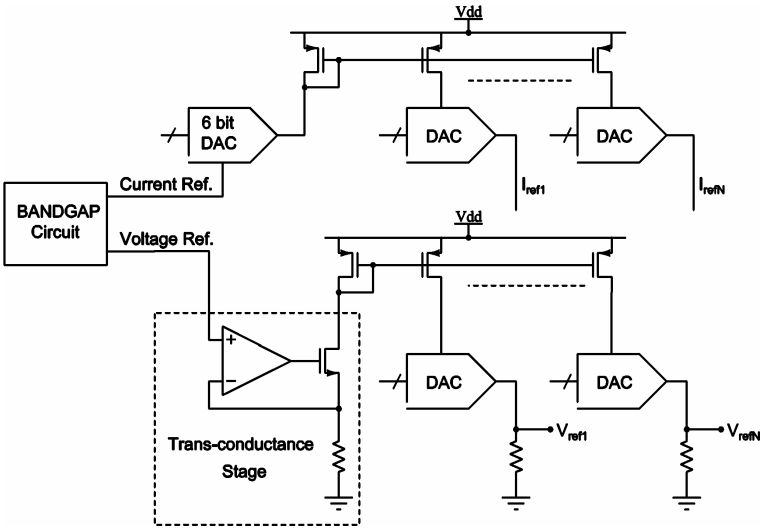

Figure 1.8: Diagram of the operation of the biasing network of the CBM.

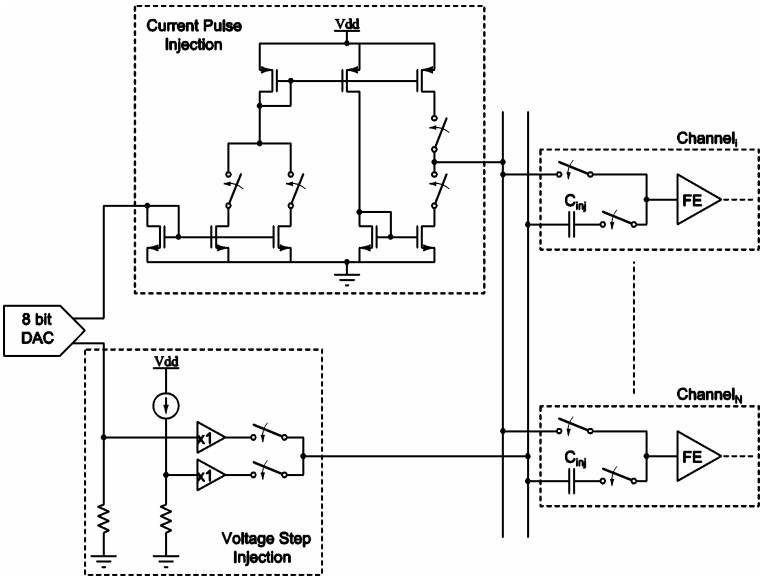

Figure 1.9: Diagram of the calibration circuit of the CBM.

internal ADCs are 10-bit SAR differential converters (Firlej et al., 2015), with one of them having internal reference derived from the bandgap and the other an external refer-

ence. The monitored currents are transformed into a voltage signal for the ADCs with an external high precision resistor. The monitoring voltage multiplexer can be controlled, and the ADCs can be read by using the digital slow control registers. The structure of the monitoring system is shown in Figure 1.10

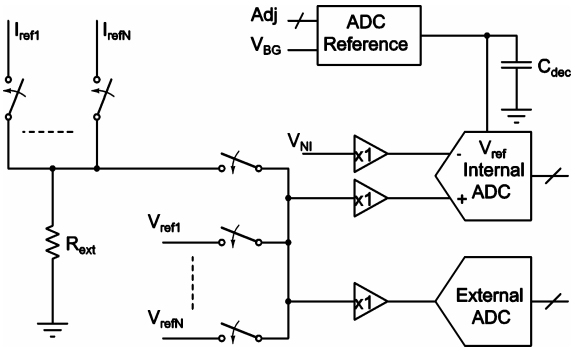

Figure 1.10: Diagram of the monitoring operation of the CBM.

1.2.2 Digital part

The digital part of the chip includes all of the digital functionality including the data synchronization and a pulse stretching unit, internal SRAM memories, communication ports, control logic, data formatting and slow control registers. The structure of the digital part is shown in Figure 1.11

The data synchronization and pulse stretching unit is used to interface between the asynchronous analog front-end and the synchronous digital part of the chip. The unit samples the output of the CFDs at the end of each of the 128 channels in every clock cycle. The output of the unit is connected to the internal SRAM1 and to the trigger output unit. The output of the unit to the SRAM1 can be stretched in the digital domain, the pulse stretch can be adjusted to be from one to eight clock cycles.

The internal SRAM memories are divided into two blocks, namely SRAM1 and SRAM2. SRAM1 is a circular buffer which samples the output of the synchronization and a pulse stretching unit every clock cycle. The size of the SRAM1 is 128 x 1024 bits, which means it can save the data from 128 channels for 1024 clock cycles before it starts to overwrite previous values. This allows the data to be read from the buffer with a certain latency, which is programmable in VFAT3. In the case of a 40 MHz clock, the maximum latency that can be set is $25.6\,\mu s$. The SRAM2 acts as a FIFO, receiving data

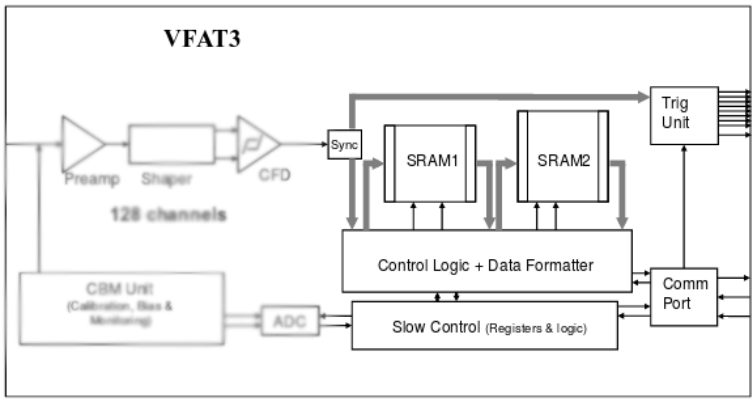

Figure 1.11: VFAT3 digital part: synchronization unit, SRAMS, Control logic and data formatter, slow control, comm port and the triggering unit.

from a certain time slot from the SRAM1, when a trigger LV1A is received. From the SRAM2, the data is fed through the communication port outside of the chip to the DAQ. The size of the SRAM2 is 176 x 512 bits, which means it can queue 512 data packets for the transfer before it starts to overflow.

The communication port is the main communication channel for the control of the chip and the data transfer in and out of the chip. The main feature of the port is the compatibility with the GBTX communication chip developed for the HL-LHC experiments (Bonacini et al., 2009). The port works at 320 Mbs, which means it can transmit 8 bits for every 40 MHz clock cycle of the CMS. The port uses a defined set of 8-bit characters to transmit commands and register information in and out of the chip. The set of characters used is shown in Table 1.1. The data packets are sent out of the chip in 8-bit sections ((Dabrowski et al., 2015)).

The slow control uses an IPbus protocol, which is wrapped within a High-Level Data Link Control (HDLC) frame (RFC 1662, 1994). The IPbus protocol provides the needed internal addressing of the slow control registers and the HDLC provides chip addressing and error detection. The slow control is accessed through the comm port by sending two 8-bit characters, SC0 and SC1, which correspond to values 0 and 1 going to the slow control. The communication is also lower in priority when compared to triggered data packets synchronous controls. This means that the slow control communication can be stopped at any time and resumed later. The slow control has 147 general read-and-write

Table 1.1: List of characters that can be sent to comm port of the VFAT3.

FSCC	Character	Function
EC0	00001111	Reset of the Event Counter (EC)
BC0	00110011	Reset of the BCZ Counter (BC)
CalPulse	00111100	Injection of the Calibration Pulse
ReSync	01010101	Resets all VFAT3 state machines
SCOnly	010111010	Force ”Slow Control Only” Mode
RunMode	01100110	Return from ”Slow Control Only” Mode
LV1A	01101001	First Level Trigger
SC0	10010110	Sends ”0” to the Slow Control
SC1	10011001	Sends ”1” to the Slow Control
ReSC	10100101	Reset of Slow Control
LV1A+EC0	10101010	First Level Trigger and reset of the EC
LV1A+BC0	11000011	First Level Trigger and reset of the BC
LV1A+EC0+BC0	11001100	First Level Trigger and reset of the EC and the BC
Ec0+BC0	11110000	Reset of the EC and the BC

registers which can be used to control the internal functionality of the chip, 3 read-only registers which have identification values, two registers for accessing the internal ADC outputs, and one register for burning the internal chip ID. The registers are mapped internally into a wishbone bus structure, which can be controlled by two masters: the IPbus transactor and auxiliary SPI master.

Inside the digital part, two separate data paths are defined: the variable latency path and the fixed latency path. The variable latency path works through the internal SRAMs and the data is only transferred if a trigger is received. The fixed latency path goes straight from the synchronization unit to the trigger unit output with a fixed latency. The different data paths are shown in Figure 1.12

In the CMS data acquisition scheme, there are separate data lines for trigger data and the full data readout. The trigger data is used to discriminate interesting events from the mass of generated event in the collisions. A certain trigger fingerprint is defined for the events of interest. When this fingerprint is detected in the system, a full data readout of the system is performed through the full data path (collaboration CMS et al., 2016).

The trigger output unit has 8 Scalable Low Voltage Signaling (SLVS) (Bulbakov et al., 2016) pairs for transmitting the data at 320 MHz. The output can be configured to either use single data rate or double data rate. The single data rate is able to transmit 64 bits in one 40 MHz clock cycle, so the data granularity is reduced by taking a fast OR of every

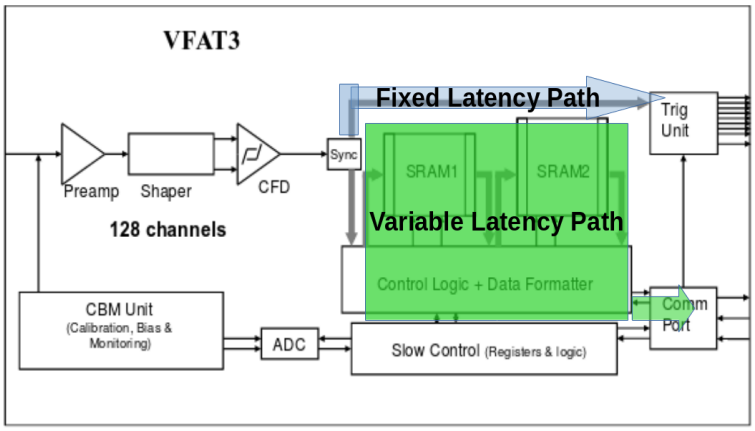

Figure 1.12: The two different data paths in the VFAT3 chip. The fixed latency path and the variable latency path.

second channel. With the double data rate, the unit can output 128 bits in one 40 MHz cycle, so full granularity of the channel data can be transmitted every clock cycle.

For the use in the GEM system, the VFAT3 is bonded into a hybrid PCB board. This hybrid hosts the external passive components, needed for the operation of the chip. The connections of the chip are fed through two connectors located on the hybrid; one for the connecting the input channels to the GEM detector and one for the communication lines that are used to control the chip and read out the data. A picture of the chip bonded on a hybrid board is shown in Figure 1.13.

1.3 Triple-GEM detector for GE1/1

A GE 1/1 triple-GEM chamber is based on a stack of three GEM foils. The chambers are trapezoidal in shape and have a detection area of 990 x (220-455)mm^2. The foils in the Triple-GEM detector are spaced a few millimeters apart from each other and placed in a gas volume. A drift PCB is located at the bottom of the foil stack. On top of the stack, there is a readout board and a GEM electronics board (GEB) (Talvitie, 2015). The VFAT3 hybrids are attached on top of the GEB and a cooling pipe circuitry is placed on top of the hybrids. The GEB also hosts one optical communication board. The whole stack is finally sealed with a protective aluminium cover. The structure of the chamber is shown in Figure 1.14 (Colaleo et al., 2015).

The stack of foils creates the different regions of the detector, as shown in Figure 1.3. The dimensions of the different regions are the drift region of 1 mm, 1 mm and 2 mm

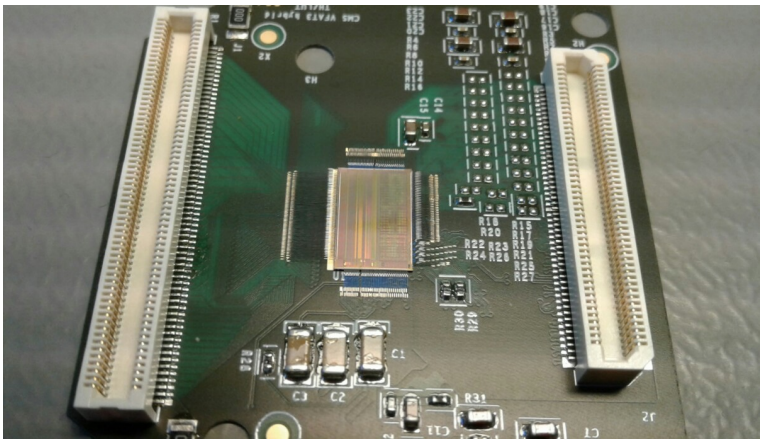

Figure 1.13: A VFAT3 bonded onto a hybrid PCB.

for the transfer regions 1 and 2, and 1 mm for the induction region. The foils are tensioned with pull-outs which are fixed to the drift and readout PBCs from the sides. By adjusting the screws on the side of the chamber, the foils can be adjusted to a desired tension (Colaleo et al., 2015) (Abbaneo et al., 2019).

The drift board has a single drift cathode on its inner surface and a solid ground plane on the outer side. The drift board routes the high voltage (HV) connections from the external supply to the various GEM electrodes. For this purpose it also hosts a noise filtering circuitry for the HV lines.

The readout board hosts high density connectors on its outer side. On the inner side it has the readout strips, which are connected to the connectors on the other side.

The electronics of the chamber consist of the GEB, 24 VFAT3 hybrids and an optohybrid (OH). The VFAT3 hybrids have a connector for the input channels, which is connected to the readout board, and a connector for the communication, which is connected to the GEB. The GEB provides the communication channels between the 24 hybrids and the optohybrid. The powering for VFAT3s and OH is also routed through the GEB. The structure of the GEM electronics system is shown in Figure 1.15

A super-chamber is created by installing two Triple-GEM detectors back to back. Each of these super chambers cover a sector of 10.15 °. To cover the full azimuthal ring, 36 super-chambers are needed. Instrumenting both CMS endcaps takes a total of 72 super-chambers. In the GE1/1 station two version of the detectors are used, a long and a short

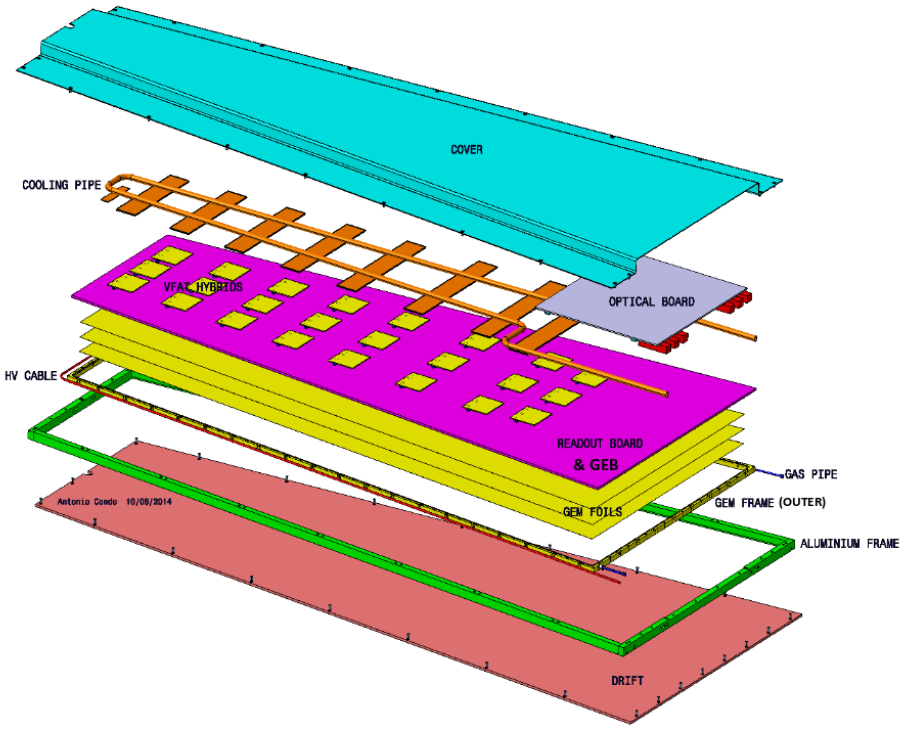

Figure 1.14: Structure of the GEM chamber (Colaleo et al., 2015).

version. Long chambers have a radial length of 128.5 cm, while short chambers have a radial length of 113.5 cm

1.4 Motivation and outline of the study

The motivation for this thesis is to study the VFAT3 chip before and after production. The VFAT3 is a rather complex chip with many analog and digital components which are closely integrated into each other. For this reason, it was decided that the mixed signal methods should be used during the design of the chip. This would ensure that all of the internal parts of the chip work together and there are no issues with the interfaces of the blocks. The high-level mixed signal simulations also work as a bridge from the simulation to the real-world verification. Many of the routines needed for the physical verification were already developed while running the high-level simulations of the chip. This ensured a seamless transition from the simulation to the study of the physical

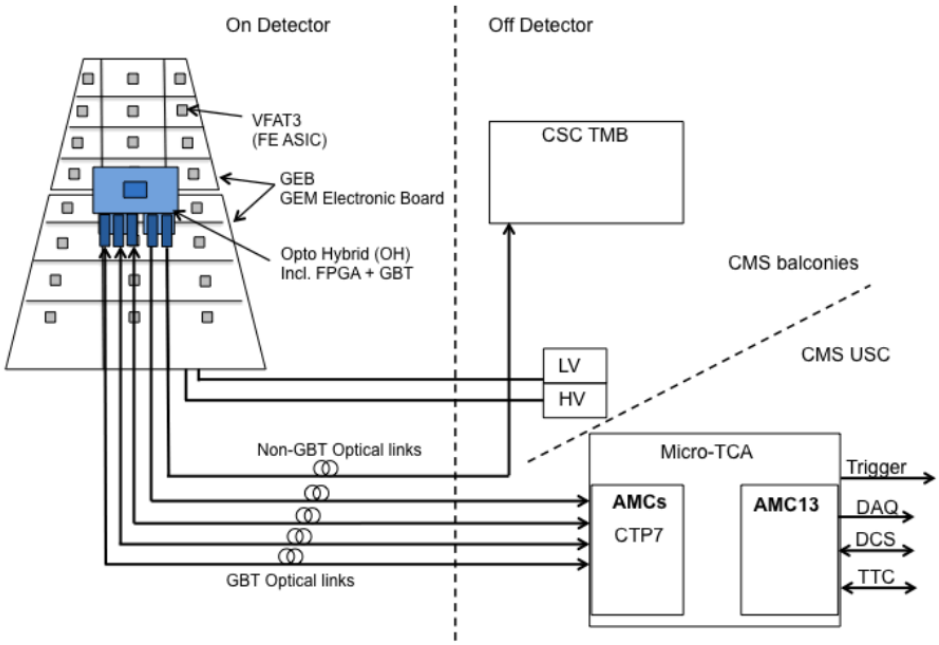

Figure 1.15: Electronic structure of the GEM chamber (Starling, 2019).

chip.

The VFAT3 has a wide range of physical test and probe pins, internal test scans and test routines. From early on it was noticed that a completely new verification and characterization platform is needed to fully study the chip - one that would be optimized for all of the test options that the VFAT3 has to offer. The platform would need to have hardware for the high-density connections of the chip, fast firmware for the connection, and test routines and software to control everything and run top-level routines.

Chapter 1 of the thesis introduces the background of the study. It presents the GEM project and the role and place of the VFAT3 chip inside the project. Chapter 2 explains the mixed simulation methods, which were used in the high level verification and study of the VFAT3 chip. Chapter 3 gives an overview of the physical verification platform designed for the VFAT3. Chapter 4 presents all of the verification and characterization results obtained from the VFAT3.

2 Simulation

The development of the integrated circuit design tools has enabled more advanced simulation methods to be performed on the design. The chips can be tested at a high level throughout the design phase. To ensure the correct high-level functionality of the VFAT3 chip, the chip was simulated with mixed signal simulation methods throughout the whole design phase of the chip. This chapter is based on **Publication I** and it describes mixed signal simulation methods in general and the simulation methods used with the VFAT3 design.

2.1 Mixed-signal simulation

A traditional way of simulating ASICs during their production was to simulate the digital and analog parts separately. Since the early 2000s, this has been slowly changing with the introduction of mixed signal hardware description languages (HDL) (Miller and Cassagnes, 2000; Mantooth et al., 2007). The two main mixed signal hardware description languages are Verilog-AMS (Accellera, 2014) and VHDL-AMS (vhd, 1999). In the mixed signal method, the digital and analog parts are simulated together. This offers the possibility test the high level functionality of the chip throughout the design phase (Kundert and Zinke, 2004; Frey and O'Riordan, 2000).

In the mixed signal methodology, models of different levels of abstraction are used during the design of a chip. As a starting point the different parts of the chip are modelled with rather crude models. The analog parts are often modelled with simple mathematical models and the digital parts as register-transfer level models. Modelling languages for this stage are often Verilog-AMS and SystemVerilog. As the different blocks of the chip are designed they are then replaced to the full chip model in the place of the functional models (Bhattacharya et al., 2012; Chen et al., 2012).

The mixed-signal-based approach gives possibilities for the simulation time optimization. Running the top-level simulations with transistor-level descriptions of the components can be very computationally demanding. With mixed signal methods it is possible to mix design blocks with different levels of abstraction, with transistor level descriptions being the most computationally demanding and real number models (RNM) the most lightweight. When simulating a certain part of the chip, the essential blocks should have as detailed a description as possible, while the blocks which are not essential for that part can be left as more high-level models. The basic concept of different abstraction levels and their simulation times are shown in Figure 2.1 (Montiel et al., 2012; Georgoulopoulos and Hatzopoulos, 2017).

The use of RNM models allows the analog blocks being simulated by the digital solvers, this improves the simulation speed significantly (CDS, 2013). Additional advantage of the simulation in the digital domain is the fact that for the digital domain there exists powerful verification methods, such as the universal verification methodology (UVM). Currently the UVM does not provide much support for MS-simulations. However, this will most like change in the future, since there is an ongoing effort on implementing MS-simulation tools on the UVM (Mehta, 2018) (Ramirez et al., 2019).

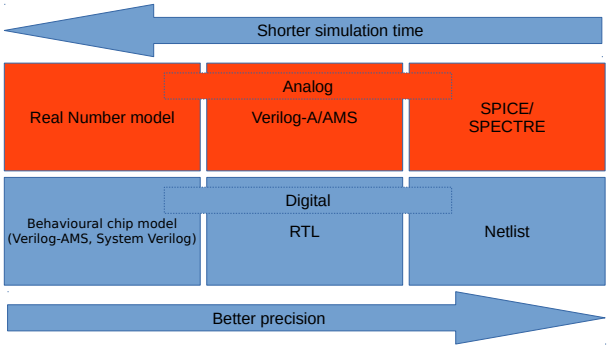

Figure 2.1: Different abstraction levels of mixed signal simulation. The top row options are for analog simulation models and the lower row options for digital models. By moving to the right on the diagram the precision of the simulation increases at the cost of increasing simulation time.

The simulation models allow the chip to be used as it was a physical chip. This allows the design of test routines and test setup to start already during the design phase (You and Song, 2009).

2.2 VFAT3 simulation

During the design of the VFAT3, mixed simulations methods were used extensively. Originally a functional high-level model of the chip was created. Later, when the design started to take shape, the model was refined to smaller and more detailed blocks. These blocks were then replaced with the transistor models as they became available. For all of the analog blocks, at least two models were used: the Verilog-AMS model and the transistor model. Many of the blocks also had a real number model (Petrow, 2015).
In the beginning, the digital part was simulated by using RTL models. After a netlist model was available, it was used for all the simulations. It was found that the simulation times between the two different models were insignificant. An example simulation

setup is shown in Figure 2.2.

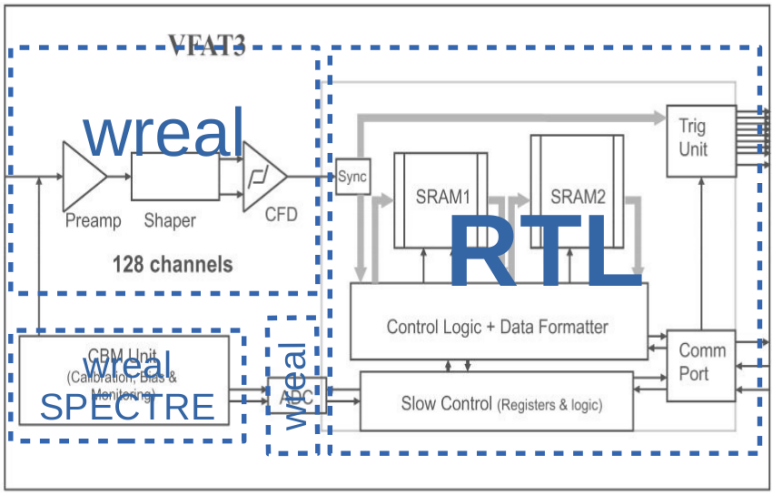

Figure 2.2: Example setup for use in simulation. Digital parts are described at RTL level and analog parts in wreal or SPECTRE models.

The use of the mixed signal models allowed the co-development of the chip design and test setup software. A custom communication protocol was implemented for the communication of the software to the environment where the chip simulation model was run. The protocol was based on temporary files shared between the simulation environment and the test setup software. One file is for control commands between the environments and two files are used to implement the communication between the software and the chip model. The protocol is described in more detail in Figure 2.3.

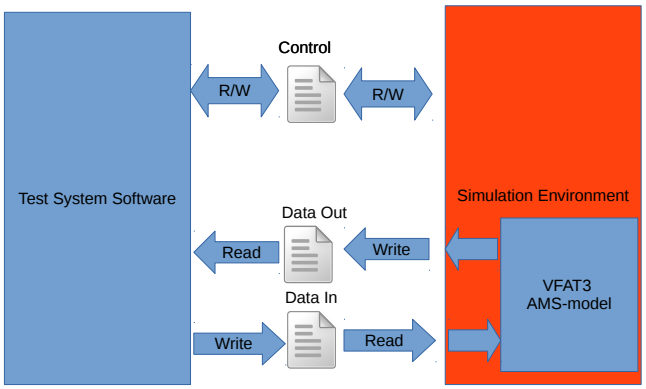

Figure 2.3: Protocol used in co-development of the test system software and the simulation model. Three temporary files are used for the communication: *Control*, which is used to control the simulation environment; *Data out*, which passes the data coming out from the chip model to the software; and *Data in*, which passes the data from the software to the model of the chip.

3 Verification Platform

In this chapter, the VFAT3 verification system is presented based on **Publication II**. A verification platform was needed throughout the testing, characterisation and possible debugging of the VFAT3. A similar system had been designed for the verification of the VFAT2 chip (Aspell et al., 2008). With the help of the mixed signal simulation model of the VFAT3, it was possible to start the design of the verification platform before the chip was back from the foundry. This allowed the testing and characterization to start soon after the chip was received. The platform was designed to be used in three different testing schemes: functional testing, characterization and production testing. The first functional testing is a crude testing phase, which aims to verify the basic functionality of the chip. The characterization phase characterizes many of the internal blocks by analyzing their performance. At this stage most of the built-in test functionality of the chip needs to be used. The last testing scheme is production testing, during which a large number of the chips are tested for production. For this stage, only essential tests are performed to ensure the functionality of the chip. The production testing is required to run the desired set of tests in the shortest time possible.

3.1 Platform

The verification platform is made up of three different components, namely the PC running the testing software, the firmware designed for a Kintex-7 FPGA development board, and several custom PCB hardware boards, optimized for different stages of the testing. The principal structure of the verification platform is shown in Figure 3.1.

3.1.1 Software

The software is the main interface between the user and the verification platform. It is used to communicate with the chip's internal functionality and run routines needed in the characterization of the chip. The software is written with Python (Rossum, 1995) and the graphical user interface is implemented by using the TkInter graphical library (Hughes, 2000). Python is a cross-platform programming language which allows the verification platform to be easily adapted between different operating systems.

3.1.2 Firmware

The firmware is designed for the Kintex-7 development board and it is based on the IP-bus architecture presented by (Larrea et al., 2015). The firmware acts as an intermediate

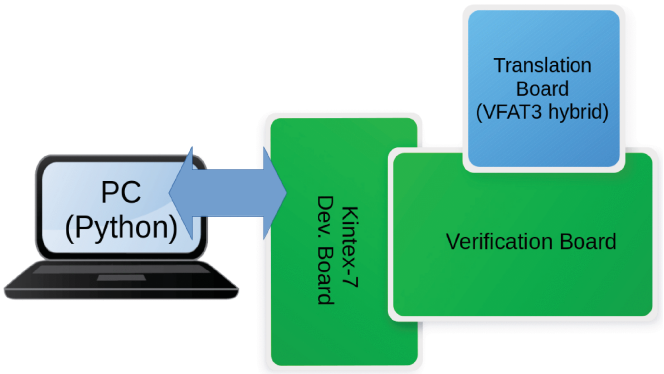

Figure 3.1: Diagram of the verification platform parts. Namely the PC, Kintex-7 and the custom PCBs.

step between the software and the physical signal lines going to the chip. The software sends the lists of commands which the firmware then sends to the chip synchronized to the communication line clock. In addition to the communication lines, the firmware also controls the external ADC located on the verification board.

3.1.3 Custom hardware

The custom hardware of the verification platform consists of two types of boards. The first type is the hybrid boards, which have the VFAT3 chip bonded on them, and the second type is the verification boards, which host the powering and the communication lines between the FPGA and the VFAT3 hybrids. The VFAT3 hybrids come in three different flavors; a translation board lite for functional tests, a translation board with all pins bonded for the characterization, and the final production hybrid. An example of the translation board lite is shown in Figure 3.2. The verification board provides three different options for powering the hybrids, including also the powering from the Feast DC-DC converters presented by (Allongue et al., 2010), which are intended to be used for the powering of the final system. An example of the hardware setup is shown in Figure 3.3.

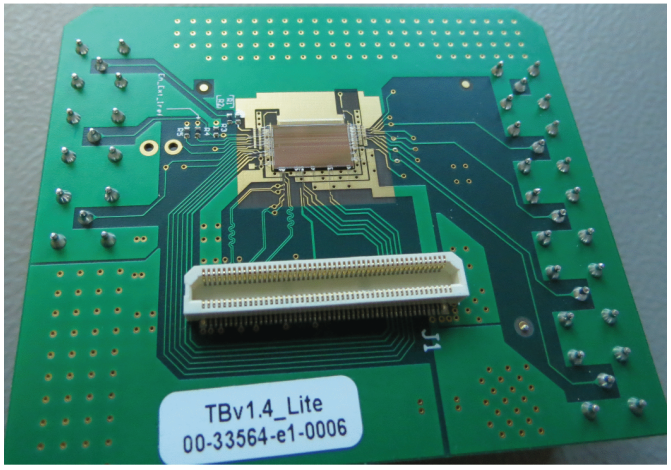

Figure 3.2: A close-up picture of the translation board lite, with the VFAT3 bonded on it.

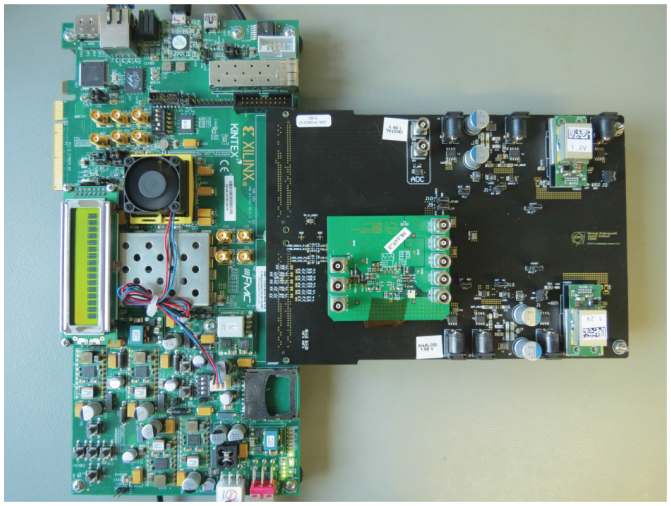

Figure 3.3: The verification platform consists of three hardware boards. The first one on the left is the Kintex-7 development board. The next one is the black verification board, which is connected to the development board. On top of it is the small green translation lite board.

3.2 Tests

The platform was designed to be used for three different testing schemes: functional testing, which only needs simple communication with the chip; characterization, which needs advanced predefined routines to be run on the chip, and the large-scale production testing of the chip, where concatenated routines need to be run effectively and fast.

3.2.1 Functional test

The functional tests are used to confirm the proper operation of the chip when it is received from the foundry. In this mode, the software allows a real time operation of the chip. In this interactive mode, the user can for example synchronize the chip, read and write slow control registers, change internal biases, send calibration pulses to the channels, and receive triggered data packets. The software displays everything that the chip responds to in real time on the software terminal.

3.2.2 Characterization

The verification platform has a routine mode, which is intended to be used for the characterization of the chip. The routine mode offers the possibility to run more comprehensive test sequences and scans to be performed on the chip. A dedicated script language was developed for the use of this mode. The script language allows the routines and scans to be defined with clear syntax. The instructions created with the language are decoded by the software into a list of timing and command pairs. The list is then uploaded to the memory of the FPGA board. Since the FPGA runs synchronously with the chip, it can send the commands to the chip with a well-defined timing between them. This allows the elimination of the possible delays and time variations in the communication between the software and the firmware. The timing in the command lists is defined as time difference between consecutive commands. This allows the routines to be of infinite length, restricted only by the internal memory of the FPGA kit. The operation principle and the syntax of the routines are shown in Figure 3.4. In characterization mode, the software collects the data from the chip. The data is then later be analyzed and displayed. For characterization purposes, the hardware has options for probing the test and debug pins in the chip. Some of the characterization results have been presented by (Dabrowski et al., 2017).

3.2.3 Production tests

For the production tests, the platform offers the possibility to run a set of predefined test routines. In the production mode, the routine execution speed is a key parameter and it

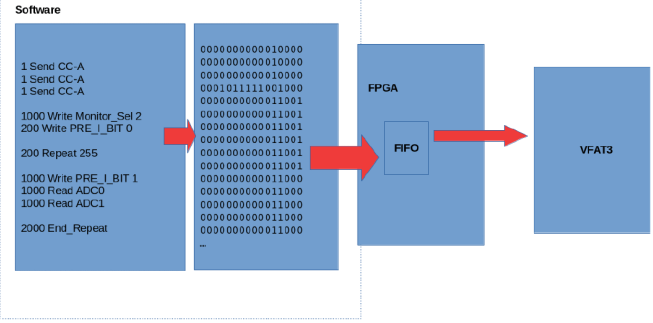

Figure 3.4: An example syntax of the custom routines and the operation principle.

can be optimized by modifications to the software or the firmware. Both of them have been designed to be easily modified. For production testing, only a subset of the VFAT3 pins are connected, namely the ones needed for the normal operation of the chip and some extra pins needed for production testing.

4 Results

In this chapter the results from the simulations and the characterization measurements are presented. The presented results are based on **Publications I, III and IV**.

4.1 Simulation results

VFAT3 high-level functionality was tested before the design was submitted to the foundry, i.e. throughout the design phase. The simulations were run in the Cadence Virtuoso Analog Design environment, which has many integrated mixed-signal simulation functionalities. The functional tests included checks for the digital part, front-end channels, biasing and monitoring. The tests that were run using the simulation model to verify the functionality of the chip are introduced in the next sub-sections.

4.1.1 Digital functions

The first step is to test the communication to the chip. The comm-ports synchronization procedure was tested and was found to be working as expected. When the three consecutive synchronization characters were sent, the chip responded with a ”synchronization ok” character. When the synchronization verification character was sent, the chip replied with the correct response character. The proper operation was also verified from the communication line wave forms, which are shown in Figure 4.1. The chip has also 147 internal slow control registers, which have read and write functionality. Each of these registers were tested and found to be working as expected.

4.1.2 Variable latency data path

In the variable latency data path, the data packet consists of a header, bunch crossing counter value (BC), an event counter value (EC), channel hit data and a crc-value for the data packet. There are multiple options for formatting the data packet in different configurations, such as reducing data packets, which have zero hits and reduce the sent data by dividing the data into partitions. The data packet triggering is completely operated from the digital side. This allowed the simulation to be run with only simple wreal models for the analog parts of the chip. All of the datapacket configurations were found to be working in the simulations. Two example cases are shown in Figure 4.2.

The variable latency data path has an internal buffer memory where the triggered data packets are stored while they are in the queue to be sent out of the chip. When the trigger rate is greater than the rate that the data packets are sent out at, the buffer memory starts

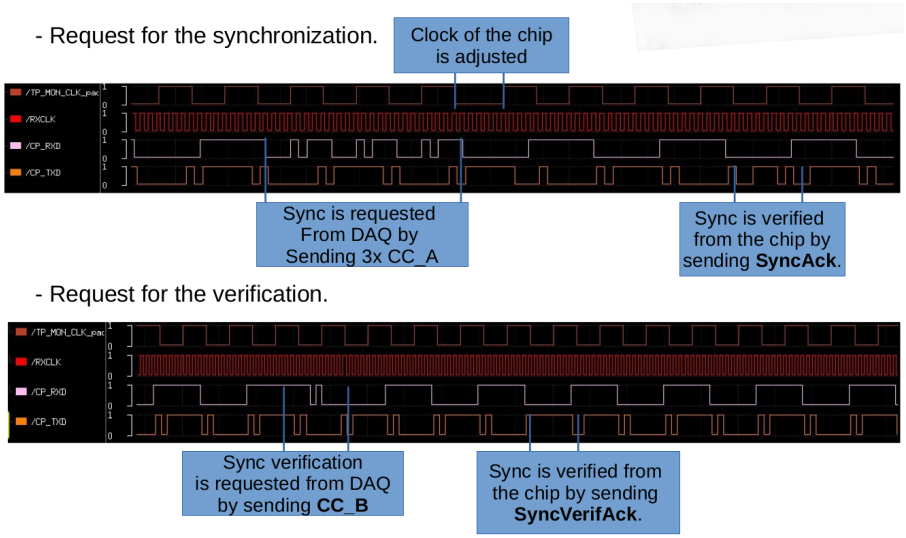

Figure 4.1: Example case of comm-port synchronization and synchronization verification functionality.

to fill up. When the buffer is full, the system starts to lose data packets. The point of overflow can be formulated as follows:

$$x = \frac{W}{1 - \frac{i}{N+1}}, \tag{4.1}$$

where W is the FIFO depth, i is the trigger interval in BCs and N is the size of the data packet in bytes. The simulation was run with several different data packet formats, and the point of overflow seemed to follow the theory rather well. The theoretical curve is shown with the measured data points in Figure 4.3.

The default VFAT3 data packet size is 22 bytes. According to the equation (4.1) the overflow goes to infinity when the trigger interval is 23 BC. This equals to a trigger rate of 1.7 MHz. Trigger rates higher than that can be maintained only for a certain period of time. Trigger rates of 1.7 MHz and lower than can be used indefinitely. This result was verified by using the simulation model.

4.1.3 Fixed latency data path

The fixed latency path sends out the data through eight trigger output signals lines. Through the signal lines, full channel data is sent out at every bunch crossing. The data

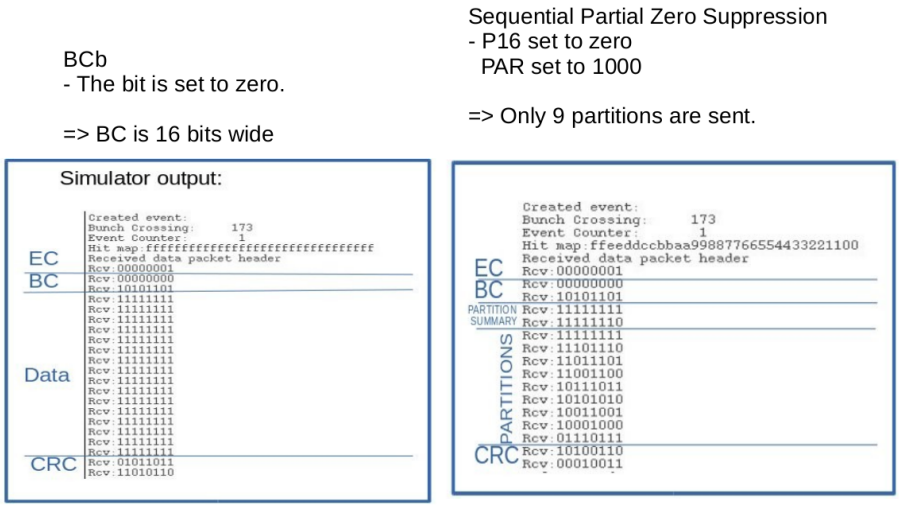

Figure 4.2: Examples of different data packet formatting options. On the left side, the packet has the default formatting. On the right side, a zero-suppression mode is activated. In this mode, the chip sends a partition table of the bytes which have hits. The partitions have also been limited to 9, which causes some data to be lost since 15 partitions have data.

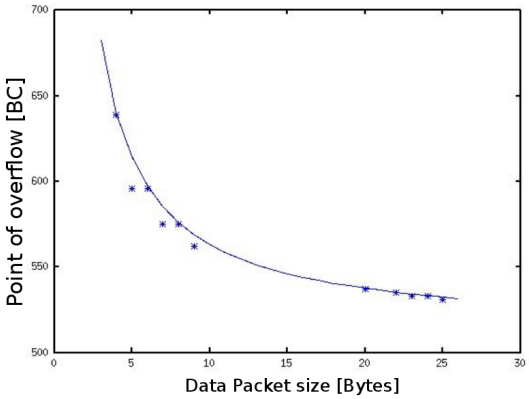

Figure 4.3: Theoretical FIFO overflow versus data packet size plotted as a smooth line and the measured data points shown as blue stars.

can be sent out with full granularity in *Double Data Rate* (DDR) mode or fastOR of every two channels in *Normal* mode. In DDR mode, the output frequency is 640 MHz and each signal line sends out 16 bits for each bunch crossing, and in Normal mode the output frequency is 320 MHz and each signal line send out 8 bits for each bunch crossing. The fixed latency path was found to be working as expected and two example cases are shown in Figure 4.4 and Figure 4.5.

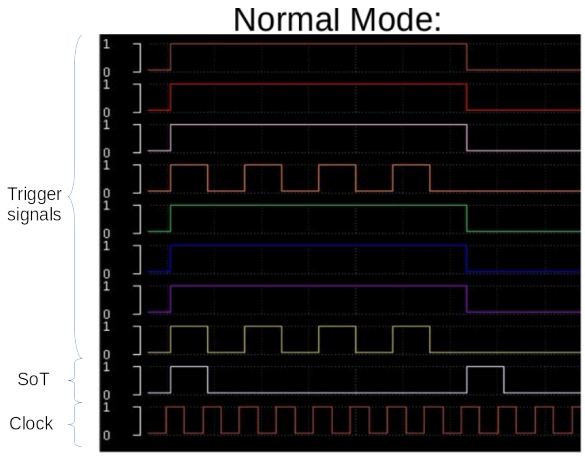

Figure 4.4: Fixed latency trigger path output in the *Normal* mode. The 8 signals on top are the trigger outputs. Under the trigger signals, there is a start of transmission signal, and the bottom signal is a 320 MHz clock signal to the chip.

An important parameter for the fixed latency data path is the time between the moment when a signal is received by analog front-end input and the moment when the trigger signal is sent from the chip. This latency can be studied when having a full analog and digital chain in the simulation. For the digital functionality of the chip, a netlist level model was used to achieve more accuracy. To optimize the accuracy and simulation time, the verilog-AMS model was chosen for the input channels. Since the CBM in this case mainly provides static biasing signals, a wreal model could be used for it. The latencies were verified by setting a certain peaking time for the input channel and injecting a calibration pulse to one of the channels. By observing the time between the input injection and the following trigger signal, the latency could be verified. During the simulation, several internal signals could also be monitored for better understanding of the internal timing. An example simulation case is presented in Figure 4.6.

The latency changes with different front-end peaking times. Using the simulation, all different peaking time settings could be studied and the latencies in bunch crossings (BC) were:

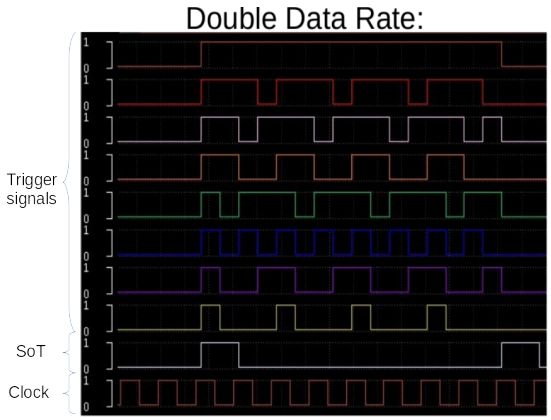

Figure 4.5: Fixed latency trigger path output in the *Double Data Rate* mode. The 8 signals on top are the trigger outputs. Under the trigger signals, there is a start of transmission signal and the bottom signal is a 320 MHz clock signal to the chip.

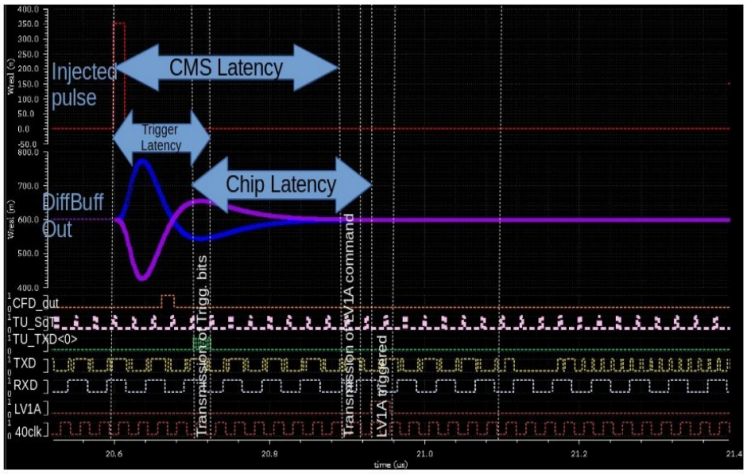

Figure 4.6: Example case of simulation of chip latency. The peaking time of the front-end is set to 25 ns. The trigger latency and the programmable chip latency are shown in the figure.

- 5 BC for peaking time of 25 ns.
- 6 BC for peaking time of 50 ns.
- 7 BC for peaking time of 75 ns.
- 9 BC for peaking time of 100 ns.

4.2 Characterization results

The characterization of the chip started as soon as it was received from the foundry. The verification platform presented in Chapter 3 was used for the characterization of the chip. The characterization focuses mainly on the analog side of the chip. The functional testing of the chip was performed before the characterization, since all of the functionality is required to be working for the characterization testing to be possible.

4.2.1 Calibration, bias and monitoring unit

The first component tested from the calibration bias and monitoring unit (CBM) was the internal ADC. The first operation is to calibrate the internal ADCs to find conversion constants, which can be used to convert the ADC counts to voltage values. An internal DAC was scanned by its full range and the value of the monitoring signal was read out by both internal ADCs and an external ADC. By comparing the values from the two ADCs, calibration constants can be calculated for the internal ADC. By applying the calculated constants, the values of the internal ADC can be converted to voltages. The results from the internal and external ADCs are shown in Figure 4.7.

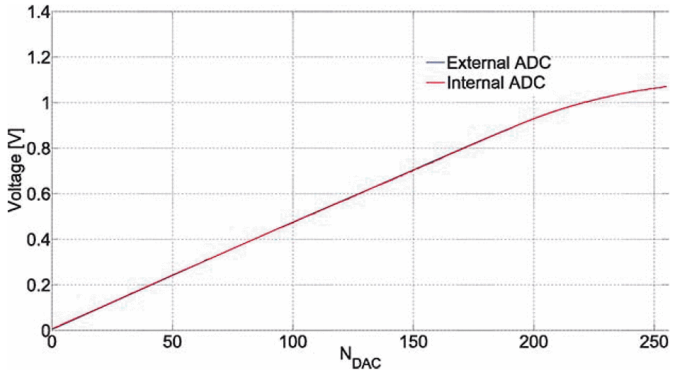

Figure 4.7: Internal and external ADC conversions after the calibration phase.

After the internal ADC was calibrated, it could be used to monitor the internal biasing voltages and currents. All of the internal biasing DACs were scanned to find their behavior throughout their full range. One case of a DAC scan is shown in Figure 4.8, where the results have been plotted with the simulated value of the DAC.

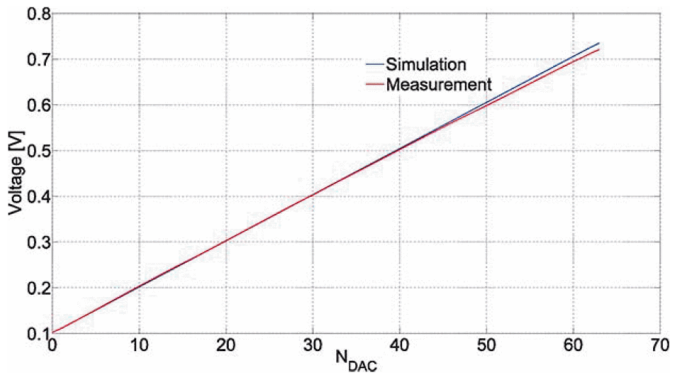

Figure 4.8: Comparison between simulation and measurements for a scan of voltage reference DAC.

The verification of the internal calibration pulsing system could be done with the help of the built-in test channel in the VFAT3. The test channel has the possibility to probe the signal between the different blocks of the analog front end. The basic structure of the test channel is shown in Figure 4.9. By probing the signal coming out of the test channel preamplifier, it was possible to measure the injected calibration pulse. Figure 4.10 shows two injected calibration pulses with the same charge. The blue curve has a pulse width of a 100 ns. The red curve has double of the pulse width, but half of the amplitude of the blue curve.

4.2.2 Input channels

The VFAT3 has a 129 th channel, which is not connected to the digital circuitry and is only used for characterization and debugging of the analog front end. The channel allows the probing of the signal between the pre-amplifier, shaper and the single to differential amplifier. The construction of the test channel is shown in Figure 4.9.

By using the analog test channel, the front end could be characterized. The measured wave forms can be seen in Figure 4.11. From the measurements, it can be seen that the shaping times after the shaper are: 15 ns, 25 ns, 36 ns and 45 ns. This is about half of the shaping times given in the specifications. It can also be seen that the analog pulse returns to zero level within 500 ns; this shows that the VFAT3 is able to operate with a

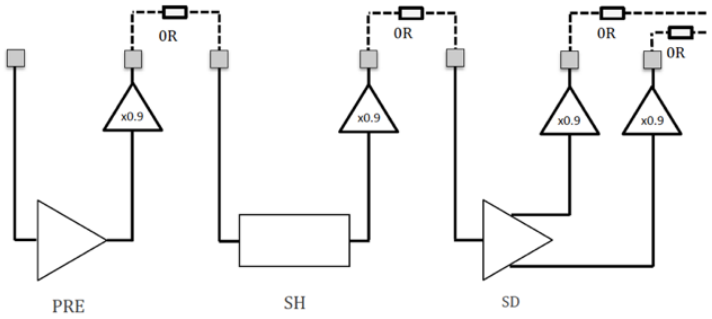

Figure 4.9: The structure of the analog test channel. Preamplifier (PRE), shaper (SH) and the single to differential amplifier (SD).

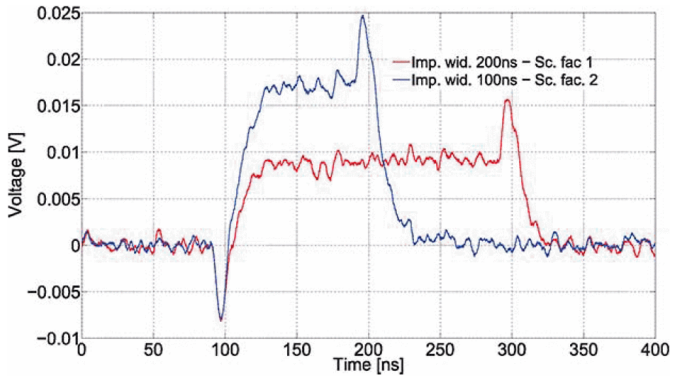

Figure 4.10: Response of the charge sensitive amplifier for two different pulses. Both pulses have the same charge, but different duration. Red curve: impulse duration 200 ns, with scale factor 1. Blue curve: impulse duration 100 ns and scale factor 2.

hit rate of 2 MHz before baseline restoration becomes an issue.

The S-curve measurements for the front-ends could be done with the help of the internal calibration pulse functionality. The S-curves for the 128 channels are shown in the top plot of Figure 4.12. By fitting an error function to the S-curves it is possible to extract the mean of the curve (threshold of the channel) and the sigma of the fit (noise of the channel). The lower plot of Figure 4.12 shows the S-curves after a threshold trimming routine. By the routine, the spread of the channel threshold can be reduced by up to a factor of 29.3.

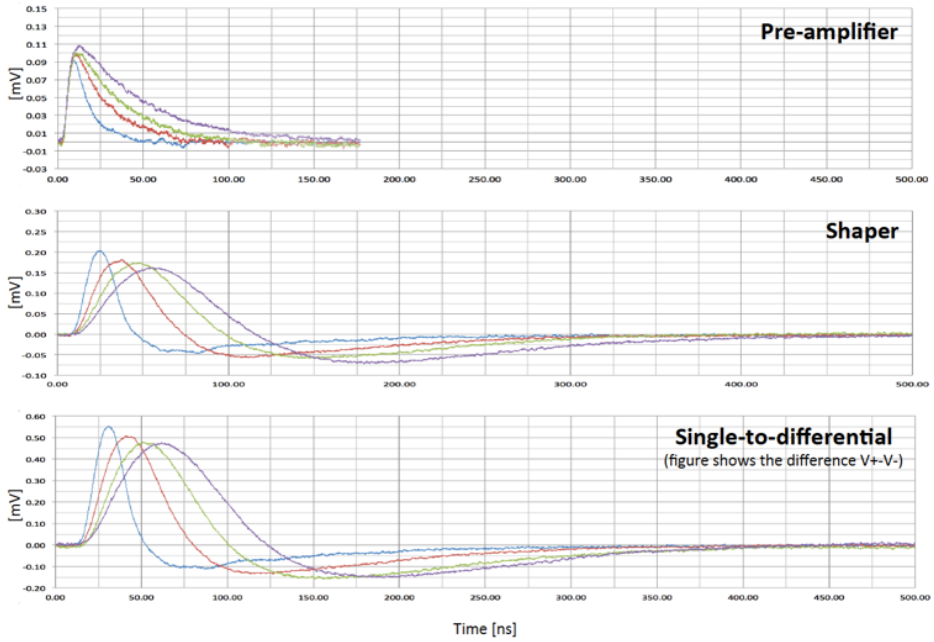

Figure 4.11: The analog pulse as measured on the analog test channel.

The noise of the channels was measured with varying the capacitance in the input of the channels. The results obtained for the medium gain setting can be seen in Figure 4.13. The measured noise slopes for the high and medium gain are:

- ENC(HG 45ns) = 650 e + 33 e/pF
- ENC(MG 45ns) = 1072 e + 28 e/pF

4.2.3 Constant fraction discriminator

The performance time walk compensation in the CFD was studied. The CFD can be used in two modes: Arming mode, in which the comparator acts only on the leading edge of the signal, and CFD mode, where the whole charge is integrated. The results are shown in Figure 4.14, which show the arming mode, and in Figure 4.15, which show the CFD mode.

By using arming mode, the time walk is about 8.5 ns for the input charges from 3 fC to 30 fC. By using CFD mode, the time walk can be reduced to about 400 ps for the same

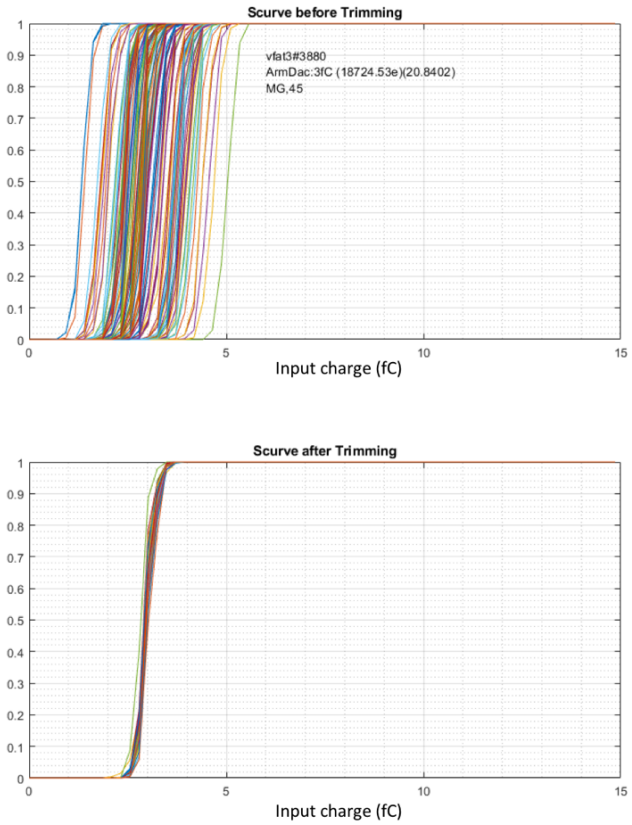

Figure 4.12: S-curve histograms for all 128 channels before and after threshold trimming. The threshold spread is reduced from 4537e to 155e.

range of input charges.

4.2.4 Characterization Summary

The characterization of the chip's CBM is in a good agreement with the simulated values. This is of great importance since it is a crucial part of the chip. Testing of the input channels would be impossible if the CBM had non-operating units. The input channels had noise performance as expected from the simulations, but the programmable peaking times were found to be about half of the designed values. The CFD showed a significant improvement in the time walk, when compared to the mode with using only the arming comparator. With the arming comparator, the time walk was in the order of 8.5 ns, but

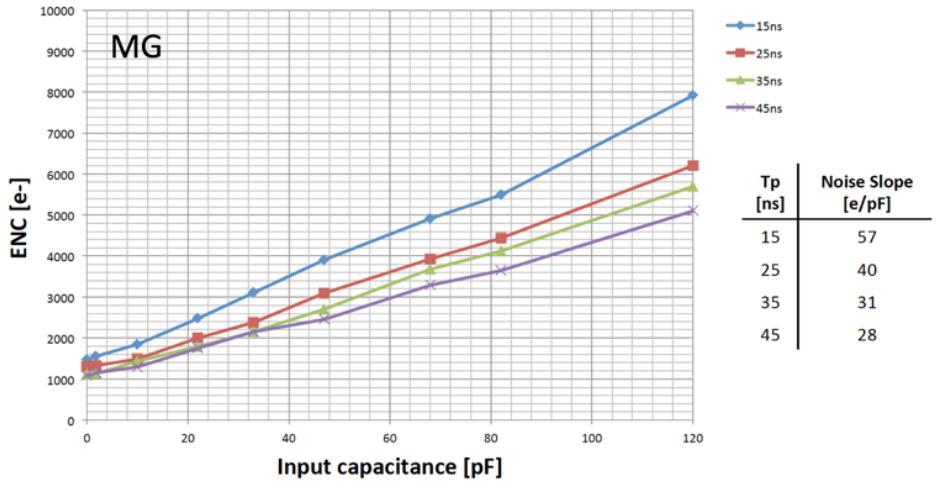

Figure 4.13: VFAT3 noise: ENC vs input capacitance for Medium Gain, mean results of all 128 channels.

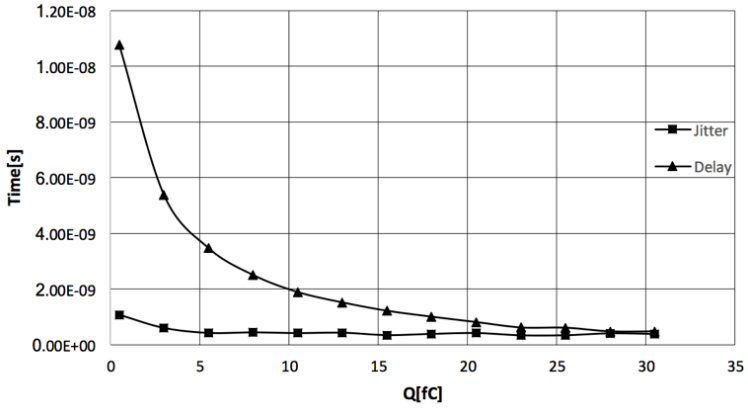

Figure 4.14: Discriminator performance in Leading Edge mode. The arming comparator peaking time is set to Tp=15 ns and a current pulse of 25 ns with charge in the range of 3 to 30 fC. The time walk (delay) is approximately 8.5 ns.

when using the CFD, the time walk could be reduced to approximately 400 ps. The characterization measurement results are listed in Table 4.1.

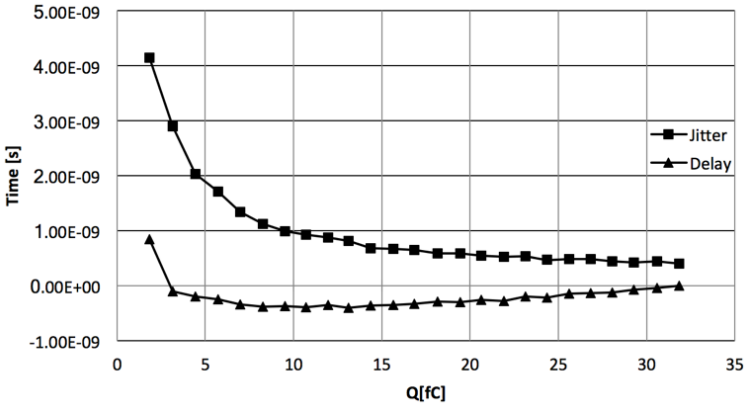

Figure 4.15: Discriminator performance in Full Charge Integration mode. The CFD is set to Tp=45 ns and a current pulse of 25 ns with charge in the range of 3 to 30 fC. The time walk (delay) is approximately 400 ps.

Table 4.1: Summary of most important parameter values measured from the VFAT3.

Parameter	Measured Performance
Peaking times	15 ns, 25 ns, 36 ns, 45 ns
Gain & Linear Range	HG: 48 mV/fC, 9.5 fC MG: 16 mV/fC, 28 fC LG: 8 mV/fC, 55 fC
ENC	HG: 620 e + 33 e/pF MG : 1072 e + 28 e/pF
Time Walk (CFD mode)	less than 0.4 ns (signal range 3 fC to 30 fC)
Input capacitance range	0 - 80 pF
Int. temp. measurement	20 - 110 °C with sensitivity 3.83 mV/°C
Maximum particle rate	2 MHz/channel
Maximum LV1A rate	1.7 MHz (more if using zero suppression)
Power consumption, Vdd=1.2V	Sleep: An.= 89 mW, Dig.=60 mW Run: An.=167 mW, Dig.=80 mW

5 Summary of publications

5.1 Publication I - High Level Verification of the VFAT3 ASIC for CMS GEM Detectors

Research objectives

During the design of an ASIC, it is important to test that all of the designed blocks fit together and that the chip design works as a whole. For a long time, the designs of the digital and analog parts of the chip have been done in isolation, with both sides having their own tools and design methodologies. When the parts are finally integrated on the same chip design, there is a possibility of having mismatches on the interface between the analog and digital side. Advances in the design tools have brought the possibility to design the digital and analog parts of the chip in the same environment. This process is known as mixed signal design. This allows the different parts to be run in the same simulation. When simulating all of the parts together, the interface problems between the blocks can be detected early on during the design phase.
A new front-end ASIC, known as VFAT3, was designed for GEM detectors. From early on, it was decided that the mixed signal methods should be used during the design of the chip. This would ensure that there are no problems in the interfaces. It also gave the possibility to simulate the chip as a whole and test that all of the high level functionality is working as expected.

Main contributions

The used mixed signal simulation model was used extensively during the design of the VFAT3. With the help of the model it could be ensured that the designed blocks worked together without any interface issues. The model could also be used for the co-development of the physical verification platform.

5.2 Publication II - A Verification Platform to provide the Functional, Characterization and Production testing for the VFAT3 ASIC

Research objectives

The newly designed VFAT3 ASIC needed a platform which could be used to verify the operation of the ASIC and to characterize its main features. The platform would be needed in three different testing scenarios: functional testing, characterization and production testing. During the functional testing, only simple communication with the

chip is needed for ensuring that the basic functions of the chip are operational. During the characterization, the internal blocks are characterized, and operational limits and characteristics are investigated. For production testing it is necessary to run a set of concatenated tests. For production testing, the speed at which the test can be run is a main optimization parameter.

Main contributions

The required verification platform was designed around a Kintex-7 development board. The platform is operated with software running on a PC connected to the FPGA. On the FPGA, several custom PCBs can be attached. The custom PCBs include different hybrid boards, which host the VFAT3 chip, and intermediate boards between the hybrids and the FPGA, which provide the communication and the powering for the hybrids.

5.3 Publication III - Calibration, bias and monitoring system for the VFAT3 ASIC of the CMS GEM detector

Research objectives

The VFAT3 ASIC has 128 input channels, which need several accurate biasing currents and voltages. Due to process variations during the manufacturing and operating the chip in a harsh radiation environment, these bias currents are deemed for variation between chips and during their lifetime. For this reason, the biasing currents and voltages should have the possibility to be adjusted. This allows the variations to be compensated, to ensure the proper operation of the input channels. Also, because of the same process variations and radiation environment, the operation of the input channels themselves can differentiate in one chip. To compensate for the differences, there should be a possibility to calibrate the input channels.

Main contributions

For this purpose, a calibration, bias and monitoring block (CBM) was designed. The block offers adjustable internal DACs for each biasing current and voltage. Since the variations also affect the adjustable DACs, the CBM provides a possibility to monitor the internal biasing voltages and currents. For the calibration of the input channels, the CBM provides the possibility to inject accurately controllable calibration pulses to the input channels. The calibration can be done with current or voltage pulses. The calibration, bias and monitoring options of the VFAT3 were tested and found to be working as expected.

5.4 Publication IV - VFAT3: A Trigger and Tracking Front-end ASIC for the Binary Readout of Gaseous and Silicon Sensors

Research objectives

A suitable front-end ASIC needed to be designed for the new triple-GEM muon detectors. The chip needed to work with the signal obtained from the GEM detectors, but also be programmable to be used with silicon detectors. The ASIC should have 128 input channels with the possibility to adjust the gain and peaking time of the channels. The chip should also include the possibility to compensate for the time walk caused by the incoming signal. For communication, the chip should have one main communication channel for both data and slow control, and the channel should be compatible with the GBT standard developed at CERN.

Main contributions

A VFAT3 front end ASIC was designed. The ASIC fulfills all the requirements set by the GEM project. The main characteristics of the chip were measured and presented.

6 Conclusions

The Large Hadron Collider at Cern will get a luminosity upgrade in the near future. In the compact muon solenoid experiment of the collider, it was decided that a detector upgrade is needed to improve the muon tracking capabilities. A plan was made to upgrade the endcap of the experiment with additional gaseous muon detectors. In 2009, research started in order to develop these new detectors. A new front-end readout chip was needed for the detector - one that would suit its specific needs for time resolution, latency and configurability. The new chip would be known as VFAT3, which is an indispensable part of the detectors since it is responsible for converting the analog signal of the particle into digital data that can be processed and analyzed. The main objectives of this thesis are the simulation of the chip during its design, and the study and characterization of the physical chip.

Mixed-signal simulation methods were used during the chip design, since the chip has many digital and analog blocks which have complex interconnections between them. These mixed signal methods were presented in this thesis. They also proved to be a valuable tool for studying the chip before submission to the foundry. The simulations made it possible to study the compatibility of the high-level components and the communication to the external data acquisition systems. Due to the chip simulation model working as a complete chip, it could be used to start the development of the physical verification platform.

The second objective of this study was to design the verification platform that is used to study the operation of the VFAT3 chip. For this purpose, the physical verification platform was developed. The platform is built around a Kintex-7 FPGA development board. The FPGA board is controlled from software running on a PC and the chip is connected to the FPGA by a set of custom printed circuit boards. This proved to be a very versatile system and the platform could be easily adapted according to the needs of the system.

The simulation, verification and characterization results were presented and discussed in this thesis. The chip was found to mostly operate as expected from the simulations. One major difference was found from the peaking times of the front end, which has faster peaking times than what had been simulated.

This thesis only covered results of the functional testing and the characterization of the VFAT3 chip. The production tests started in 2019 and were finished in 2020, with 3000 hybrid modules tested. Preliminary results have been published by Irshad et al. (2020). Last GEM detectors were installed into the CMS experiment in the end of 2020, and they have been collecting data since the beginning of 2021.

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Publication I

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High Level Verification of the VFAT3 ASIC for CMS GEM Detectors

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High Level Verification of the VFAT3 ASIC for CMS GEM Detectors

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Abstract: A front-end readout chip VFAT3 was designed for the muon detector gas electron multipliers (GEM). GEMs were installed at the Compact Muon Solenoid (CMS) experiment of the Large Hadron Collider (LHC) at CERN for the high luminosity upgrade. The design of the VFAT3 uses 790 analog and 172 digital blocks which are highly integrated, thus it is crucial to ensure that the different blocks work together and the chip works as a whole. Mixed signal simulation methods were used to verify the high level functionality. Trigger latencies of 125, 150, 175 and 225 ns were found for front-end peaking times of 25, 50, 75 and 100 ns, respectively. The maximum trigger rate for reading out standard data packets was found to be 1.7 MHz. Results of the VFAT3 high level verification are presented and the simulation methods described.

Keywords: Front-end electronics for detector readout

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Contents

1 Introduction

The Large Hadron Collider (LHC) at CERN is planned to get a luminosity upgrade by 2027. The upgrade is known as the High Luminosity LHC (HL-LHC) and it is supposed to increase the instantaneous luminosity of the collider from $2*10^{34}cm^{-2}s^{-1}$ to $5*10^{34}cm^{-2}s^{-1}$. This improvement will increase the rate of collisions and, due to the statistical nature of particle physics, help confirm current results and bring rarer and rared interactions within reach of the collider. The upgrade of the collider brings also higher requirements for the detectors used in the experiment [1]. To meet these requirements, a decision was taken to upgrade the muon subsystem of the Compact Muon Solenoid (CMS) experiment with additional gas electron multiplier (GEM) detectors [2].

An existing front-end readout chip VFAT2 (Very Forward ATLAS and TOTEM), which has been used for the GEM telescope of TOTEM experiment, was considered for the new CMS GEM detector [3]. The chip design was optimized to be used for silicon, GEM and CSC detectors at TOTEM. Although the VFAT2 was used in GEM detectors at TOTEM, its shaping time is too short to collect the whole charge produced by particles crossing the new GEM detectors. Additionally, the chip is unable to cope with the increased particle rate and is not compatible with CMS requirements. Consequently, a new FE-chip had to be designed. The chip had to have a fast communication channel and a large internal memory to cope with the expected trigger rate from the CMS. To be suitable for the GEM detectors, the chip shaping time had to be longer than in VFAT2 [2]. Due to placement in

the forward region of CMS, radiation hardness was required. No commercial component with such specifications was found.

A decision was taken to design a front-end readout chip VFAT3. The chip had to have 128 analog input channels and a vast amount of configurable components, including internal biasing DACs, ADCs, a front-end with different peaking times and gains, a constant fraction discriminator, monitoring possibilities and data packet options [4]. To implement all of the functionality desired for the chip, a large number of both analog and digital design blocks were used. These blocks are closely integrated with each other, so mixed signal simulation methods were needed during the design of the chip. This allowed high level functional verification of the chip throughout the whole design phase.

1.1 VFAT3

As mentioned in the previous section, the VFAT3 chip has both analog and digital functional blocks. The blocks can be divided into four parts, namely: The analog front-end, which has 128 input channels and a constant fraction discriminator (CFD) for each channel [5] [6]; the calibration, bias and monitoring (CBM) block, which handles the chip biasing and calibration [7]; the digital part, which has the communication port, internal SRAM memories, internal registry and control blocks [8]; the ADC-block, which has two ADCs used for chip monitoring.

The analog input channels have four peaking time settings: 25 ns, 50 ns, 75 ns and 100 ns and three gain levels: low, medium and high. The CBM unit provides the needed biasing for the input channels and the possibility to monitor these signals externally via the onboard ADC blocks. The digital block provides the slow control functionality of the chip and furnishes a 320 MHz GBT communication channel. The main functional blocks of the VFAT3 are shown in Figure 1.

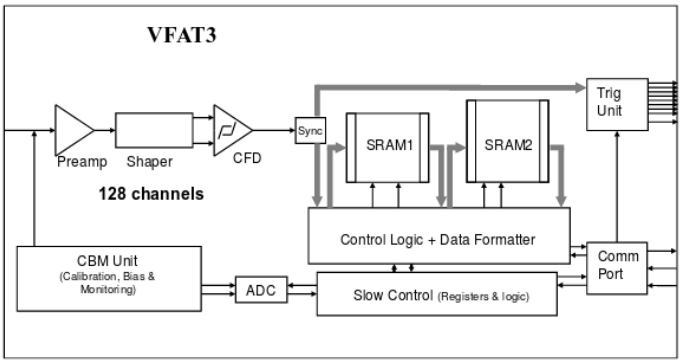

Figure 1. VFAT3 functional blocks: 128 input channels, CBM block, ADCs and the digital functionality[4].

The aim of this paper is to present the high-level simulation results of the VFAT3 front-end chip. Chapter 2 starts with an introduction to mixed-signal simulation methods and then goes on to present details about the methods used in the VFAT3 high-level simulations. Chapter 3 presents the main results obtained from the simulations. These results include measuring the trigger latencies at different peaking times and overflow of the internal FIFO at different data packet sizes. The

advantages of using mixed-simulation methods are discussed in chapter 4. Chapter 5 gives an overview of the used methods and obtained results.

2 Mixed-signal simulation

Mixed signal verification is a method used to verify the high-level functionality of an ASIC throughout the whole design phase. The method started first appearing around the turn of the century when the industry started slowly adopting it to their workflows. The high energy physics community continued to rely on the traditional verification method. However in recent years, the community has started to include this method as it has become more mature and standardized.

At the beginning of a typical top-down mixed signal design process, a chip is composed of a set of analog and digital mixed-signal (AMS) and register-transfer level (RTL) models which describe the desired high level functionality of the final ASIC. These models are described using mathematical and functional models written in modeling languages such as Verilog-AMS and SystemVerilog. The models are later replaced by components which are described at transistor level or netlist level as the component designs are finalized. Using models on different abstraction levels allows the newly designed components to be verified as part of the whole system already in the early stages of the chip design [9] [10][11][12].

The mixed-signal based approach comes also with drawbacks. Running the top-level simulations with transistor level descriptions of the components is computationally very demanding and requires a lot of computational power. To avoid long simulation times, the components can have descriptions with different levels of complexity: for instance, a computationally intensive transistor-level model for accurate and detailed simulations and a lightweight real number model (RNM, wreal) for simulations that are more functional in nature. Thus, when simulating a certain part of the chip in more detail, parts that are not strictly bound to that part can be replaced by functional models. The functional RNM models are designed to be run by using digital simulation engines. Typically, signals in a digital domain can only have the values of high or low, but the RNM extensions allow the signals to have a real number value. The RNM models do not require the use of analog solvers during the simulations, which improves the speed of the simulations significantly. The downside is the fact that it is difficult to create models which accurately describe the operation of the analog blocks. This is why the RNM-models are typically used when verifying high-level connections inside the mixed signal models [13]. The use of RNM brings the verification to the digital domain, where powerful verification methods have been developed, such as the universal verification methodology (UVM). The UVM is a standardized verification methodology which offers testing libraries and easy reuse of developed verification blocks. However, the UVM is typically used for the testing of the digital domain and currently does not provide many features for the use in high-level verification which is better suited for the analog and mixed-signal performance of the chip. For future work with MS-simulations, the UVM could be considered since there is an ongoing effort to include more mixed-signal features into the UVM [14] [15]. The basic concept of different abstraction levels and their simulation times is shown in Figure 2[16].

Since the chip can be simulated as a whole, mixed-signal high-level models allow the development of test routines and procedures for use in the verification of the physical chip. The routines

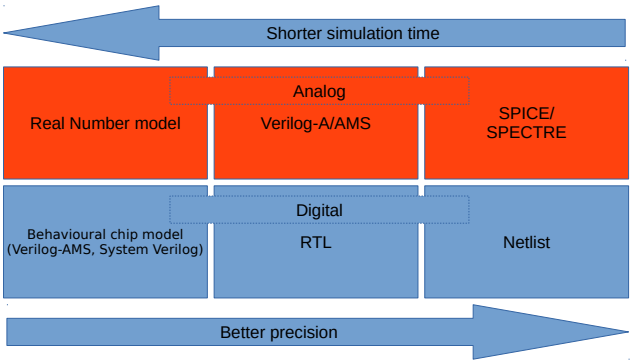

Figure 2. Different abstraction levels of mixed signal simulation. The top row options are for analog simulation models and the lower row options for digital models. By moving to the right on the diagram the precision of the simulation increases at the cost of increasing simulation time.

can be designed before the physical chip arrives from the foundry and testing can start immediately after the arrival of the chip [17].

Mixed-signal simulation methods were used during the design of VFAT3. The high-level simulations were run in addition to the analog and digital designers' own design block verification. The high-level models allowed the testing of cross domain functions, such as the readout chains, which require the use of the whole analog front-end and the digital readout features. The mixed-signal model was used to test some of the purely digital features of the chip, although in addition the digital domain had been tested thoroughly by the designers during the development.

For different sections of the chip, models of different levels of abstraction were used. For the analog blocks, three models were typically developed: a Verilog-AMS model to be used in place of the transistor level model while it is designed, a real number model to be used in high-level functional simulations, and the final transistor level model itself [18]. The different level models were provided by the designers, who also verified their designs more accurately on the transistor level. RTL models were used for the digital part of the chip until the netlist level description was available. After that, only the netlist was used for the simulation, since the simulation time difference between the RTL model and netlist level simulation is small.

The communication between the test bench and the model is mostly done through the VFAT3 main communication channel, the comm-port, which provides the clock signal and the two-way communication with the model. The test bench is also reading out the signals from the eight outputs of the trigger unit, which are essential for the operation of the chip. For the 128 input channels of the chip, the test bench offers a possibility to inject desired charge to any number of the channels.

For the simulation setup used for the VFAT3 register verification, an RTL-model was used for the digital section. Since the operation of the analog blocks is not critical for this verification, RNM models were used. These models are described at higher level, which allows faster simulation times. One simulation setup is shown in Figure 3.

The model of the chip can also be used in the development of the test setup for the physical

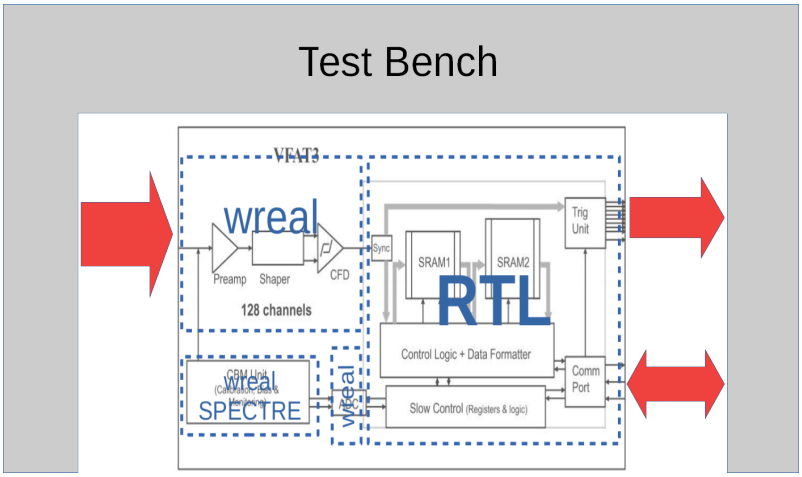

Figure 3. A setup used in simulation. Digital parts are described at RTL level and analog parts in wreal or SPECTRE models. The test bench mainly communicates through the VFAT3's comm-port, but it also reads the trigger output from the chip and can inject pulses into the input channels.

chip. By running the simulation environment and the developed test software alongside each other, the communication and test routines could be verified before the chip was submitted to the foundry.

For the co-development of the chip design and the physical test setup software, a custom communication protocol was implemented to allow the software to communicate with the environment where the chip simulation model was run. Interprocess communication (IPC) methods such as pipes and sockets are often used for the communication between the software and the simulation environment [19]. A plain text communication protocol had been earlier proposed for the use of the communication to the physical testbench [17]. To ease the co-development for both systems, the same protocol was used also for the simulations. The protocol is based on temporary files shared between the simulation environment and the test setup software. One file is for control commands between the environments and two files are used to implement the communication between the software and the chip model. The protocol is described in more detail in Figure 4.

3 VFAT3 high level verification results

VFAT3 high-level functionality was tested throughout the design phase. The simulations were run in the Cadence Virtuoso Analog Design environment, which has many integrated mixed-signal simulation functionalities. The high-level verification is mostly aimed at functions which include both analog and digital domains, such as calibration pulses, data packets, latency and monitoring. In addition, some of the essential digital features were verified with the model, such as synchronization, slow control registers and FIFO overflow. In depth simulations and verification for the pure analog and digital domains were performed by the designers: different gate delays were used for the digital domain, and corner and Monte Carlo simulations for the analog domain. Test runs using the mixed-signal simulation model to verify the functionality of the chip are introduced in the next sub sections.

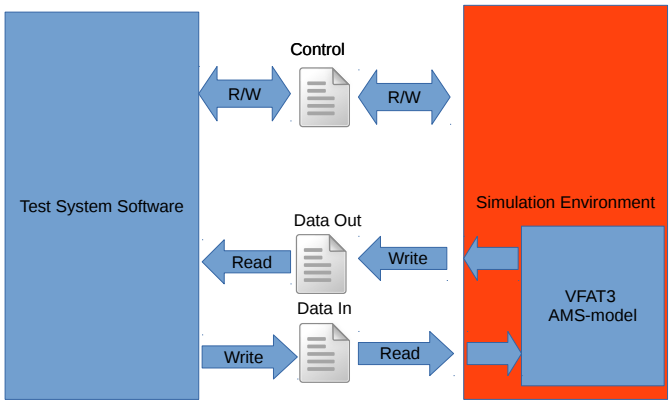

Figure 4. Protocol used in the co-development of the test system software and the simulation model. Three temporary files are used for the communication: *Control*, which is used to control the simulation environment; *Data out*, which passes the data coming out from the chip model to the software; and *Data in*, which passes the data from the software to the model of the chip.

3.1 Synchronization

As a first test, the synchronization functionality of the communication channel was tested. The aim of the procedure is to synchronize the chip with the LHC 40 MHz clock. When the communication line is synchronized with the LHC clock, the chip is able to read the incoming information bits correctly and reliably. The synchronization can be achieved by sending a unique synchronization character to the chip. When the chip receives three consecutive synchronization characters (CC_A), the chip communication channel adjusts its internal clock to match the phase of the synchronization characters. When the internal clock has been adjusted, the chip sends back a response character (SyncAck). To ensure that the chip is correctly synchronized, a synchronization verification character (CC_B) can be sent to the comm-port. When the chip receives the character, it triggers a response character (SyncVerifAck) after reception if the line is synchronized. Since the synchronization of the internal clocks is a purely digital feature, the accurate performance of the analog parts of the chip is not critical. This allowed the use of wreal models for the analog blocks, which in turn provided fast simulation times. Thus, the functionality of the communication channels was verified. The synchronization procedure is presented in Figure 5.

3.2 Slow control registers

There are 147 16-bit slow control registers in the VFAT3 chip which have read and write functionality. These registers are the interface through which the chip can be configured and operated. The registers control things such as the values of the internal bias DACs, the structure of the out coming data packets, setting of the internal calibration pulse and the reading of the value of the two internal ADCs. The register control inside the chip is based on a wishbone structure. The value of the registers is read and written by sending IPbus packets to the chip through the communication port. The functionality of these registers can be verified by writing bit patterns to the registers and then reading back and verifying that the bit patterns are equal. All 147 slow control registers of VFAT3

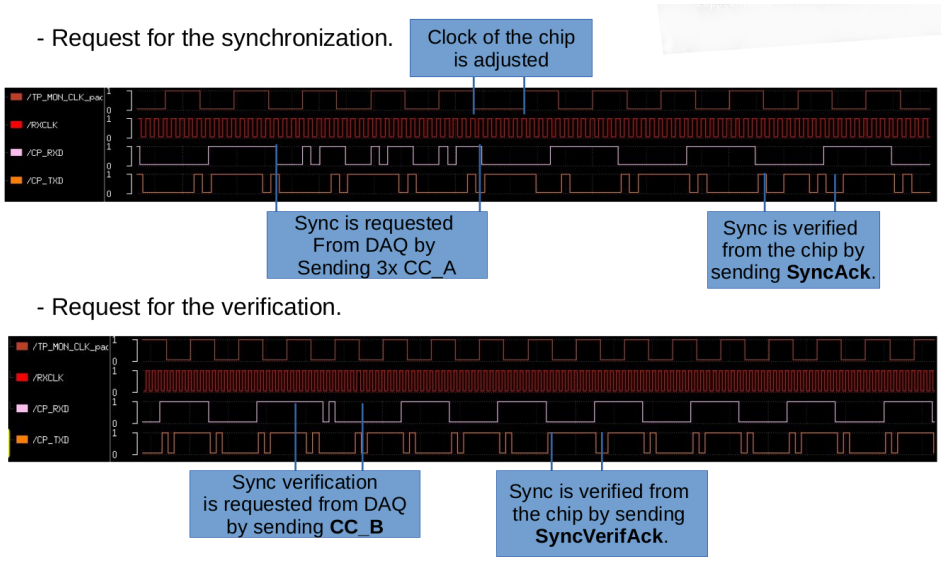

Figure 5. The comm-port synchronization and the synchronization verification functionality.

were verified to be functional. The verification of the registers requires only the digital blocks of the chip. So in this case it was also possible to use the wreal-models for the analog blocks and gain faster simulation times.

3.3 Triggering and calibration

The VFAT3 chip has a triggering function which allows data packets to be triggered by sending a trigger character to the chip. VFAT3 also has an internal calibration functionality which allows the calibration pulses of a certain charge to be injected into channels under investigation. The pulse can be a voltage pulse, which is sent to the preamplifier through a series of capacitors, creating a delta-like pulse. This type of pulse is similar to a signal from a silicon detector. In this mode the polarity, amplitude and the phase of the pulse can be controlled. The other type of pulse is a current pulse, which is fed straight to the preamplifier. This type of input is more similar to a signal obtained from a GEM-detector. In this mode, the amplitude and the polarity of the pulse can be controlled. Testing this functionality requires the use of mixed-signal methods, since both analog and digital domain are in use. The calibration pulse is set up through the digital registers, the pulse is injected to the analog front-end and the output of the front end is read through the digital domain. In this case, depending on the required accuracy of the analog front-end, a wreal or Verilog-AMS model could be considered. Since the timing of the input signal was not critical, a wreal-model was used. The analog blocks in the CBM needed only to provide static signals to the front end, so they could be modelled with wreal-models. To test the internal calibration and triggering of the chip, the internal calibration pulse was set up for different channels and a data packet corresponding to the pulse was triggered from the chip. The triggering and calibration functions were found to function as expected.

3.4 Data packets

The default data packet from the chip includes a header, a bunch crossing counter value (BC), an event counter value (EC), the hit data from each of the 128 channels and a CRC-value for the packet. VFAT3 has a vast array of options for modifying the size of the data packet. The size of the counters can be changed, the data zero-suppressed and whole data packets can be suppressed into just the header byte if no hits are received. The chip offers also a more advanced zero suppression mode, the sequential partial zero suppression (SPZS). In the SPZS mode the channel hit data is divided into 16 partitions. The data section of the packet starts with a partition table, indicating which partitions have hits. The partition table is then followed by the data from the partitions which have hits. The registers controlling the data packet formatting are the following: P16, forcing the data to include only the partition summary (SPZS mode); PAR, defining the maximum number of sent partitions (SPZS mode); DT, for toggling on and off the SPZS mode; SZP, suppressing zero data packets; SZD, suppressing zero data fields; TT, time tag formatting; ECb, setting EC size from one byte to three bytes; BCb, setting BC size to two or three bytes.

This verification procedure uses the full analog and digital readout chain, so mixed-signal methods were needed. Data packets are created and triggered inside the digital part of the chip, so a netlist level model was used for the digital part. Calibration pulses were sent to the analog input channels to obtain hits for the data packets, but the accuracy in their performance is not that critical. This allowed the input channels and CBM to be modeled with wreal models. A verification of the data packet formatting functionality was done by going through every combination of the data packet formatting options and checking whether the structure of the packet was as expected. Two different situations are shown in Figure 6. Using the testing routine, all data packet formatting options were verified to be functional.

3.5 FIFO overflow

VFAT3 is able to accept triggers at the rate of 40 MHz. It has an internal buffer memory that stores the triggered data packets before they are sent out of the chip. When triggers are received more often than data packets can be sent out, the FIFO buffer starts to fill up. When the buffer is full, it is unable to store more data until some of the data is sent out of the chip and new data is rejected. This situation is referred as an overflow of the buffer memory. The rate at which the FIFO buffer fills is a function of the trigger rate and the size of the data packet, which defines the time it takes to send out data. The point of overflow is defined as the amount of triggers needed before the internal buffer fills up and start to rejects new data. Theoretically the point of overflow x can be formulated as follows:

$$x = \frac{W}{1 - \frac{i}{N+1}}, \tag{3.1}$$

where W is the FIFO depth, i is the trigger interval in BC's and N is the size of the data packet in bytes. The trigger interval is defined as the interval between LHC bunch crossings (BC), which is 25 ns for one BC. The overflow point was simulated with several different values of data packet size, with FIFO depth being 512 and the interval 1 BC (25 ns). It was not possible to simulate all different data-packet sizes since some of the formats need incoming data from the channels

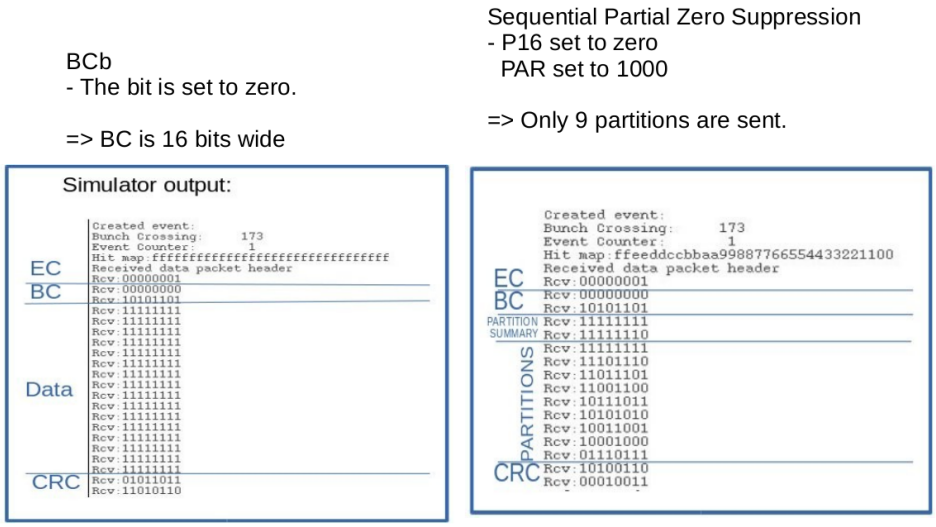

Figure 6. Two different data packet formatting options. On the left side, the packet has the default formatting. On the right side, a zero-suppression mode is activated. In this mode, the chip sends a table of the partitions which have hits. The partitions have also been limited to 9, which causes some data to be lost since 15 partitions have data. If a mismatch is found between the received data and the sent hits, the system raises an error.

to be triggered. Results of the simulated point of overflow for different data packet sizes and the theoretical prediction are presented in Figure 7. The simulated overflow points closely follow the expected value.

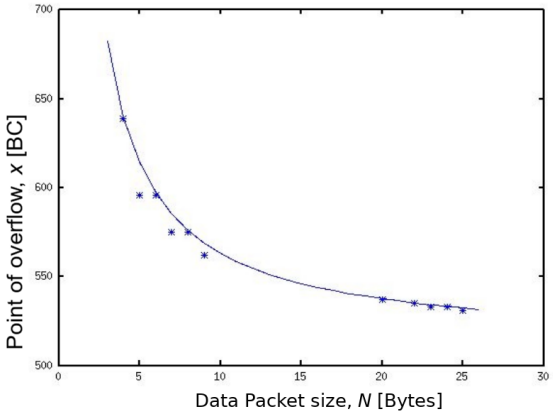

Figure 7. Theoretical FIFO overflow versus data packet size plotted as a smooth line. The data points measured from the simulation are marked with star symbol.

An interesting parameter is the maximum trigger rate which the chip can maintain indefinitely

without the FIFO overflowing. The default VFAT3 data packet size N is 22 bytes. According to the equation (3.1) the point of overflow goes to infinity when the trigger interval i is 23 BC (575 ns). This equals to a trigger rate of 1.7 MHz. Trigger rates higher than that can be maintained only for a certain period of time. Trigger rates of 1.7 MHz and lower can be used indefinitely. This result was verified by using the simulation model. The model requires mostly the digital blocks of the chip, so all of the analog input channels and the blocks inside the CBM could be modeled using the wreal-models.

3.6 Latency

An important parameter of the chip is the latency between the moment when a signal is received at the analog front-end input and the moment when the trigger signal is sent from the chip. This is defined as the chips "trigger latency", which is an important parameter when pairing incoming data with the correct bunch crossing. The latency can be studied when having a full analog and digital chain in the simulation. For the digital functionality of the chip, a netlist level model was used to achieve more accuracy. The netlist was run by using typical delay values and checked by using maximum and minimum delays. Choosing the right model for the analog front-end was crucial. The model needed to represent the front-and as accurately as possible, but still be light weight enough to be simulated along the digital domain. To optimize the accuracy and simulation time, the verilog-AMS model was chosen for the input channels. Since CBM in this case mainly provides static biasing signals, a wreal model was used. Latencies were verified by setting a certain peaking time for the input channel and injecting an input pulse to one of the channels. By observing the time between the input injection and the following trigger signal, the trigger latency was verified. During the simulation, several internal signals were also monitored for a better understanding of the internal timing. One simulation case is presented in Figure 8. In the figure, two additional latencies are shown. The first one is the CMS latency, which describes the time between the injected signal and the transmission of the level one accept trigger-signal (LV1A) to the chip. Here an arbitrary value was used. The second latency is the chip latency, which is defined as the used depth of the internal FIFO memory. The depth can be controlled by an internal slow control register. During operation, the chip latency should be set to such a value that the CMS LV1A-trigger points to a correct event.

The trigger latency changes with different front-end peaking times. Using the simulation, all different peaking time settings were studied and the trigger latencies in bunch crossings (BC) were: 5 BC for peaking time of 25 ns. 6 BC for peaking time of 50 ns. 7 BC for peaking time of 75 ns. 9 BC for peaking time of 100 ns.

3.7 Fixed latency trigger path

VFAT3 has eight trigger output signals, which send out the data from the input channels. The full trigger data is sent out every 25 ns. The channel data has two modes: *Normal* mode where the data is sent as a fastOR of every two channels in 320 MHz; and *Double Data Rate* mode (DDR), which sends full granularity data at 640 MHz by sending data on the rising and falling edge of the 320 MHz clock. In verification of the fixed latency trigger path, the full analog and digital chain is again needed. The digital part of the chip was modeled at the netlist level since it holds most of the functionality for the path. To reduce the simulation time, wreal-models were used for the input

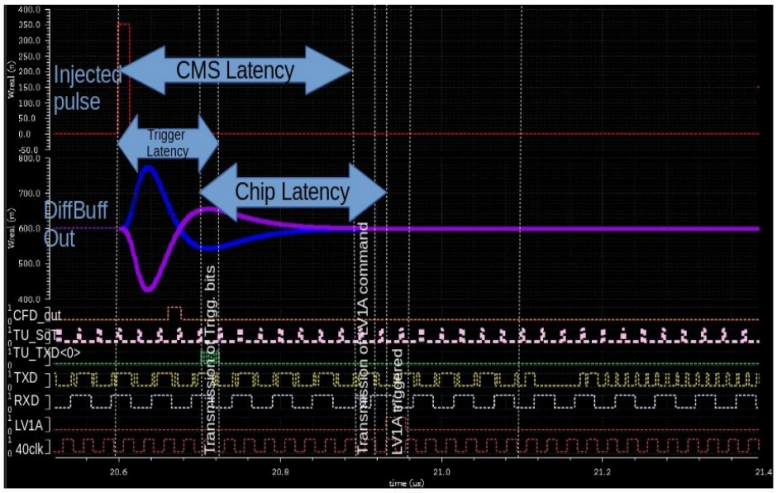

Figure 8. A simulation case of the chip latency. The peaking time of the front-end is set to 25 ns. The trigger latency and the programmable chip latency are shown in the figure. The monitored signals are: injected pulse, output of the differential buffer (DiffBuffOut), asynchronous output of the constant fraction discriminator (CFD_out), Start of transmission from the trigger unit (TU_SoT), first trigger unit output line (TU_TXD<0>), comm-port communication lines (TXD and RXD), internal LV1A signal (LV1A) and internal 40 MHz clock (40clk).

channels and CBM. This can be justified since the timing accuracy of the analog components is not crucial in this simulation. The simulation outputs of the two different output modes are presented in Figure 9 and Figure 10. By simulating the trigger signals with different input patterns, the fixed latency path was verified to be performing as expected.

3.8 Monitoring

There are multiple current and voltage DACs inside the VFAT3 chip which allow the internal biasing of the analog blocks to be adjusted. The chip has an internal monitoring functionality which allows monitoring of several internal currents and voltages using the on-chip ADCs. There are two internal 10-bit successive-approximation-register (SAR) ADCs. One of them has a reference voltage derived from the internal VFAT3 bandgap, and one has a reference voltage tied to VDD through an external high precision resistor. The internal currents and voltages can be chosen for monitoring with the internal slow control registers. The value can then be read out through the internal ADC's. By running this monitoring procedure combined with changing the internal DAC values, the functionality of the internal DACs and the monitoring block were verified.

Mixed-signal methods were essential in the verification of the monitoring feature. The DACs, the monitoring multiplexer and the ADCs are analog components, which are controlled through the digital registers. In this case, the blocks inside the CBM and the monitoring ADC's needed to be simulated by using Verilog-AMS models. Since there was no need to send signals through the analog inputs, they could be modeled by using the wreal-models.

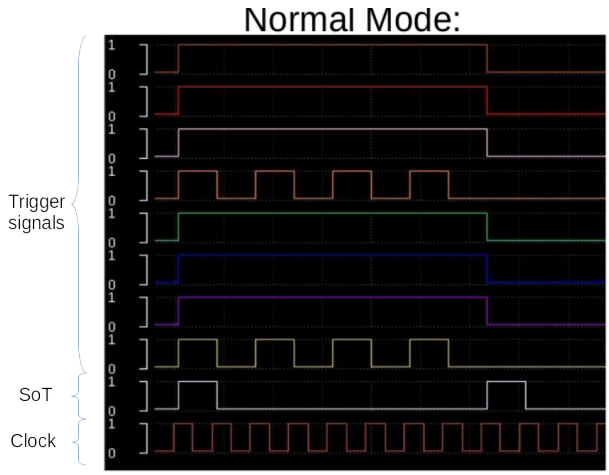

Figure 9. Fixed latency trigger path output in the *Normal* mode. 8 signals on top are the trigger outputs. Under the trigger signals, there is a start of transmission signal (SoT), and the bottom signal is a 320 MHz clock signal to the chip.

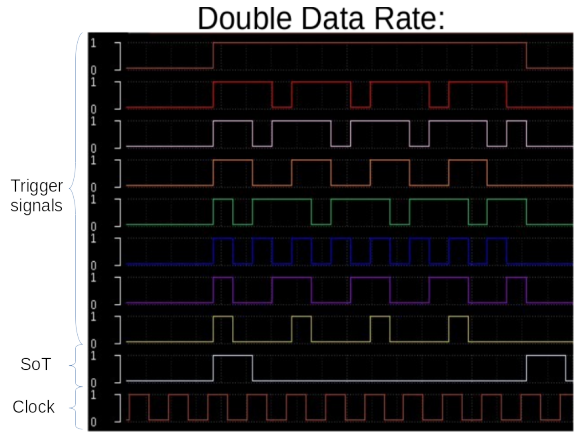

Figure 10. Fixed latency trigger path output in the *Double Data Rate* mode. 8 signals on top are the trigger outputs. Under the trigger signals, there is a start of transmission signal (SoT), and the bottom signal is a 320 MHz clock signal to the chip, on which the data is sent on the rising and falling edge.

4 Discussion

The use of mixed signal simulation methods proved to be a valuable tool in development of the VFAT3 chip. It allowed the high-level functionality of the VFAT3 to be verified throughout the design phase. The analog and digital domains in the chip have a complex array of interconnects between them. Verifying these connections has been a common source of errors in a typical chip design. However, by using the ms-simulation methods, all of these connections could be verified by using both domains in the same simulation model. Many of the presented simulation cases required

the use of the whole readout chain from the analog input to digital outputs. The simulations wouldn't have been possible using the old method of simulating analog and digital blocks in their respective domains.

The biggest challenge in the use of mixed-signal methods was the number of different models that needed to be handled and constantly updated. Creating Verilog-AMS and RNM model, which accurately describes an analog block, can be a time consuming and tedious task. The models need to be constantly updated as the chip design progresses, and this can take time away from the actual chip design process. Minimum, maximum and typical delays were used when the digital netlist was used in time critical simulations. The analog models didn't take into account corners and Monte Carlo simulations. This is something that could be improved in future work and models could be defined for analog blocks with possibility to use different scenarios. When the mixed-signal UVM methods become more mature, they will offer more possibilities for the automation of the verification tasks. In this work, some manual setup changes were still required between tests.

In addition, the use of mixed-signal methods enabled estimation of the user experience already during the design of the chip. This in turn allowed the design team to decide whether changes were needed to improve the compatibility of the chip with the external DAQ systems. Significantly, the main functionality of the VFAT3 chip was verified before the submission to the foundry.

The use of the simulation models made it possible to start developing test systems and routines for the physical chip during the design and manufacturing phase. The design of the test software was already started before submission by running the software along with the simulation models to test the communication and test routines developed for the software.

Due to the co-development of the mixed-signal simulations and the physical test bench, a working test environment was ready to be used for the characterization and verification of the physical chip [17]. The physical chip was fully verified and characterized, and was found to be working as predicted by the simulations [7] [20].

5 Conclusions

A front-end ASIC VFAT3 was designed for a future detector upgrade of CMS. The VFAT3 design has 790 analog and 172 digital design blocks which have complex interconnections between them. Due to this complexity, it was decided to use mixed signal simulation methods to ensure the high-level functionality of the chip before the submission to the foundry. With the high-level simulations, the major functionalities of the chip were verified to be working. The latencies for different front-end peaking times are: 5 BC for 25 ns, 6 BC for 50 ns, 7 BC for 75 ns and 9 BC for 100 ns. The maximum trigger rate for reading out standard data packets was confirmed to be 1.7 MHz, which matches the theory. The simulation models were used to start the design of the test environment used for physical chip, before it was received from the foundry.

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Publication II

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A Verification Platform to provide the Functional, Characterization and Production testing for the VFAT3 ASIC

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A Verification Platform to provide the Functional, Characterization and Production testing for the VFAT3 ASIC

H. Petrow, P. Aspell, C. Bravo, M. Dabrowski, G. De Lentdecker, P. Leroux, G. De Robertis, A. Irshad, T. Lenzi, F. Licciulli, F. Loddo, F. Robert, F. Tavernier, J. Rosa, and T. Tuuva,

***Abstract*—VFAT3 is a front-end ASIC designed for the readout of GEM detectors in the CMS Muon system. The strategy for the chip design was to design the full chip at once but provide extensive test and debug facilities for individual characterization of each internal chip module. The verification platform consists of three parts; namely the software (running on a PC), the firmware (designed for a Kintex-7 FPGA development board) and a selection of VFAT3 dedicated hardware boards for the different stages of verification. The system was designed to accommodate all of the steps needed to fully test the chip. The first step is the functional testing for which only rather simple functions are needed. For the functional testing. the software has an interactive interface to communicate with the chip through the FPGA. The requirements for the hardware are mostly the possibility for the use of the main communication channels. For the characterization of the chip, the software offers a possibility to easily generate lists of routine instructions that can be uploaded to the FPGA and run as synchronous commands. This allows for example the scanning of the chip's internal calibration DACs and creation of S-curves for all of the front-end channels. The hardware boards of the system allows access to the vast amount of test pads needed for the characterization and debug of the chip. The production tests require concatenated test routines where speed and execution efficiency are crucial. The software and the firmware of the system were designed to allow flexible evolution to increase the efficiency of complicated test routines.**

I. Introduction

A Verification platform has been designed to provide the Functional, Characterization and Production testing for the VFAT3 ASIC. Both the VFAT3 chip and the verification system have been designed within the framework of the GEM development for the CMS Muon system at the LHC[1][2]. The strategy in the chip design was to design the full chip at once and then provide test and debug facilities for each internal chip module [3]. The first functional" test is a crude verification of the main functionality of the chip modules. The second stage of testing is the performance characterization of the individual modules working in isolation and together, This stage requires access to most of the internal and external testing options of the chip. The third testing stage is the production test. This involves lengthy concatenated test routines which need to execute in a fast and efficient manner to minimize the volume production test time.

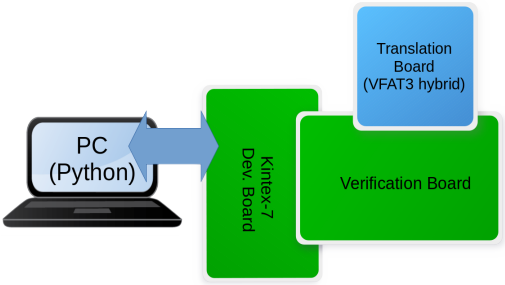

Fig. 1. Parts of the verification platform. A PC running the software, Kintex-7 FPGA development board running the firmware and the custom hardware boards: the verification board and the translation board.

II. Platform

The verification platform consists of three parts; namely the software (running on a PC), the firmware (designed for a Kintex-7 FPGA development board) and a selection of VFAT3 dedicated hardware boards for the different stages of verification. The parts of the system are shown in the Fig 1.

A. Software

The software of the platform is used to control the test. It was written in Python and the graphical user interface has been implemented with TkInter, which is built into the Python environment. This was done to allow the verification platform to be easily adaptable across different operating systems. The

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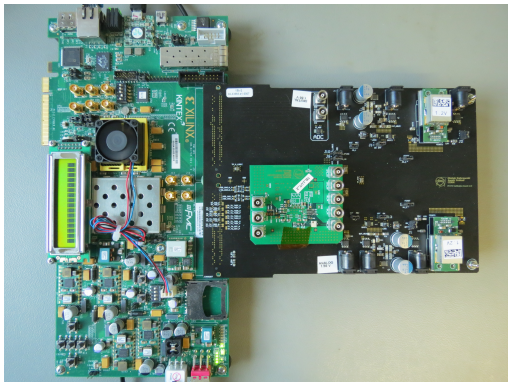

Fig. 2. The hardware boards of the verification platform. In the left side of the picture is the Kintex-7 development board. Connected to the development board is the verification board (black board). The translation board lite (green board) is mounted on top of the Verification board.

software hosts different modes of operation for different steps of the verification.

B. Firmware

Firmware of the platform is based on the IPbus architecture [4]. The main functionality of the firmware is to send command lists to the chip generated by the software and receive out coming communication from the chip. In addition the firmware also controls trigger and debug lines of the chip and also the external ADC located on the verification board.

C. Custom hardware

The hardware of the platform is based on two types of custom designed PCBs. The first is the verification board which provides powering and the interface control and data line between the FPGA board and the custom VFAT3 board. The custom VFAT3 boards come in 3 versions for the 3 different types of test. A translation board light for functional tests (Fig 3), and a translation board which include test and debug facilities for the characterization and debug stage, and the VFAT3 hybrid which contains only the signals required for final use in the system. The verification board provides 3 different powering options including using the Feast DC-DC converters as intended for the powering of the final system[5]. An example of the hardware setup is shown in the Fig 2.

III. Tests

The system was designed to accommodate all of the steps needed to fully test the chip. Namely the functional testing for which only rather simple functions are needed, the characterization of the chip where long routines and scans are needed and the production tests which require concatenated test routines where speed and execution efficiency are crucial.

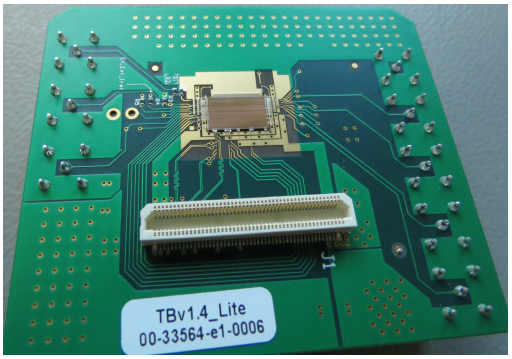

Fig. 3. A detail of the translation board lite. VFAT3 chip bonded on the pcb

A. Functional tests

For the functional tests, the software has an interactive mode which allows real time online operation with the chip. In interactive mode, the user can send instructions one by one to activate the different functions of the chip. Functions such as synchronizing the CommPort, write/read from internal registers, setting up bias conditions, pulsing the front-end and reading data packets. The data received from the chip is displayed in real time. With these basic controls the functionality could be tested.

B. Characterization

For the characterization of the chip the software offers a routine-mode which allows more comprehensive tests sequences and scans to be performed to the chip. In the characterization-mode the tests are defined with a special script language, which allows long scans and routines to be easily defined with a clear syntax. The software decodes these scripts into lists of timing and command pairs which are uploaded to the FPGA. The FPGA is then able to execute the commands in a synchronous fashion with well defined timing. This approach was chosen to remove the possible variations in timing that could have existed in the communication between the software and the firmware. The timing used in the lists is defined as the time difference between two consecutive commands, this technique allows the scans to be of infinite length restricted only by the size of the memories in the FPGA. The operation principle and the syntax of the routines is shown in the Fig 4. In the characterization mode the data coming out of the chip is collected by the software for later manipulation and display purposes. For the characterization the hardware also offers the possibility to probe all of the test and debug pins of the chip. The characterization is on going and some results have been presented[6].

C. Production tests

The production tests are intended for the volume testing of VFAT3 hybrids. These hybrids have only the pads bonded that

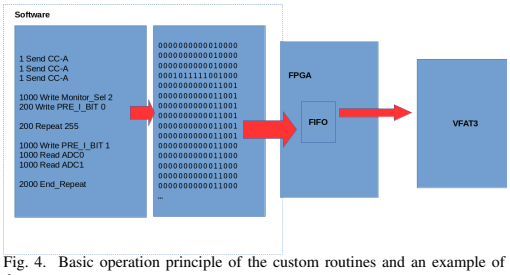

Fig. 4. Basic operation principle of the custom routines and an example of the syntax.

are needed for final operation of the chip in the system plus some pads intended to aid the production tests. The software has a production-mode, which allows the concatenated runs of routines and scans. The software and firmware were created to be flexible to speed up the run of the production tests if needed.

IV. Conclusion

A verification platform for the VFAT3 front end ASIC was developed. The platform allowed the chip to be functionally tested and characterized. The platform will be developed further to allow radiation testing of the chip and also to accommodate the large scale production tests of the final VFAT3 hybrid board.

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Publication III

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Calibration, Bias and Monitoring System for the VFAT3 ASIC of the CMS GEM Detector

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***Abstract*—VFAT3 is the last version of a family of multichannel trigger and tracking ASICs designed for the upgrade of the CMS experiment in the LHC. The chip has been developed to provide fast trigger information from the readout of gas particle detectors improving the resolution of the time measurement. The VFAT3 architecture comprises 128 analog channels, each one composed by a low noise and low power charge sensitive amplifier, shaper and constant fraction discriminator. The comparator output is synchronized with the LHC clock and sent both to a fixed latency path for trigger signal generation and to memories for storage and readout. The front-end amplifier is programmable in terms of gain and pulse shaping time, in order to adapt it to a wide range of gaseous detectors and also silicon detectors. The chip also comprises a programmable calibration system that can provide both voltage and current pulses. There are also two internal 10 bit ADCs for the monitoring of the internal bias references. The digital logic provides trigger generation, digital data tagging and storage, data formatting and data packet transmission with error protection on 320Mbps e-link. The digital design is triplicated in order to improve the radiation hardness of the system. A first run of the chip of $9.1x6.1mm^2$ in 130nm technology node has been submitted and produced. Chip architecture, measurements and characterization of the calibration, bias and monitoring system will be shown.**

I. Introduction

VFAT3 is a front-end ASIC designed for the readout of Gas Electron Multiplier (GEM) detectors for the upgrade of the CMS experiment at LHC at CERN. The architecture comprises 128 analog channels each one composed by a charge sensitive amplifier, a shaper and a constant fraction discriminator. A digital logic allows to control the chip and to exchange data with an external controller. A dedicated analog block has been designed to bias, calibrate and monitor (CBM) the analog front-ends.

VFAT3 is produced in two different versions in a 130nm technology: one with standard input ESD protections provided by the foundry and the other one with a custom scheme to improve the protection from discharge events that may occur in GEM detectors. First samples of the ASIC are currently under test and the first results about the CBM block will be shown.

II. CBM Architecture

A. Bias

VFAT3 is a mixed signal analog-digital ASIC where the analog part is strongly dependent from process variations and radiation damage due to the environment where the chip will be used (up to $100Mrad$). In order to compensate variations each sensible circuit has a programmable bias. All the references are controlled by means of current DACs whose resolutions (8 or 6 bits) and full scale ranges are chosen according on how much the circuit is affected by process variation. The reference network has a hierarchical structure (fig. 1): a bandgap reference [1] provides a voltage and a current stable both in temperature and against the power supply voltage variations. Temperature simulation of the bandgap reference, fig. 2, shows that in a range between $-20°C$ and $80°C$ the maximum variation of both references is lower that 0.7% respect to the nominal value at $27°C$.

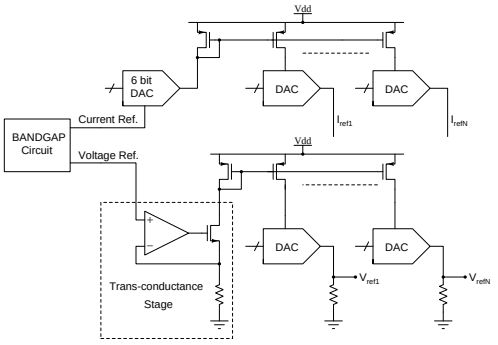

Fig. 1. Architecture of the Bias block.

The reference voltages are generate starting from the bandgap voltage output V_{BG}, that is about $350mV$ in the nominal corner and is converted into a current using a trans-

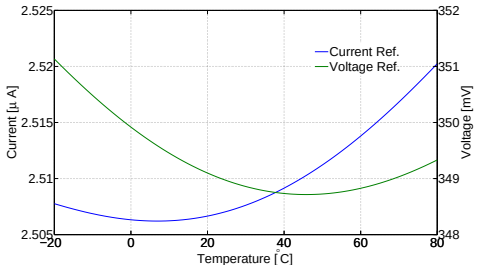

Fig. 2. Temperature simulation for the output voltage and current of the bandgap circuit.

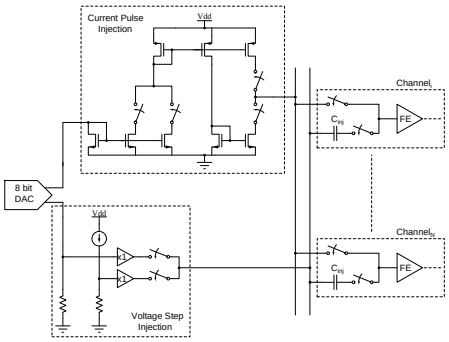

Fig. 3. Architecture of the calibration circuit.

conductance amplifier. Different scaled copies of this current are used as reference current for the DACs whose output are again converted into voltages. Exploiting the same kind of resistor from the technology library both for the trans-conductance amplifier and for the final voltage conversion at the output of the DACs it is possible to compensate temperature variations and also to reduce the resistor mismatch dependence of the reference.

All current references, instead, are generated by the bandgap current output. Since this quantity is strongly dependent from the process, it can be finely tuned using a 6-bit DAC to achieve a precise and controllable reference current stable with temperature and power supply. The mirrored and scaled copies of the current are used as reference current for the DACs that generate the bias of the analog blocks.

B. Calibration

The calibration circuit (fig. 3), necessary for the channel characterization and equalization, is designed to generate both voltage steps and current pulses. For the first setting the voltage step is realized switching one terminal of the injection capacitance C_{inj} (one for each channel) between two voltages: one is a fixed value while the other can be controlled by means of an 8-bit DAC. Adjusting the DAC output and the switching sequence it is possible to choose the polarity of the pulse and the amount of the charge injected that ranges from $0C$ to $63.75fC$ with an LSB of $0.25fC$.

The current pulse, useful to investigate about the ballistic deficit of the charge preamplifier, generates current pulses whose amplitude can be controlled through a DAC and whose duration is programmable and proportional to a $25ns$ clock cycles. A programmable mirror allows to control the polarity of the pulse and provides a further scaling factor to the current amplitude. The smallest current pulse injects $62.5aC$ of charge that can be scaled, changing the pulse amplitude, up to a factor 4 with a unity step and changing the pulse width up to 511 clock cycles.

C. Monitoring

All internal reference currents and voltages con be monitored using either and internal or an external ADC, according to the scheme shown in figure 4. The currents are mirrored and multiplexed toward an external high precision resistor (R_{ext}) to make the I/V conversion. The correspondent voltage is then multiplexed with the other voltage at the ADC input through a voltage follower. The internal ADC is a 10-bit SAR differential converter developed using a switching capacitor architecture achieving, in such a way, a high speed ultra-low power component [2]. The ADC reference (V_{ref}) derives from the bandgap voltage V_{BG} and it is provided by a dedicated circuit that, using two bits (Adj), can tune the reference with a resolution of $50mV/LSB$. This further control is necessary to compensate the process variation of the bandgap in order to achieve an ADC reference of $1V$ that corresponds to an LSB of about $2mV$. During the conversion phase the impulsive switching current is absorbed from reference, in order to avoid voltage drifts the reference node is connected to pad and loaded with a huge decoupling capacitance C_{dec}. The whole capacitance is divided into two parallel components: a smaller one of few hundred of pF made by MOS capacitors that is placed inside the chip as close as possible to the ADC reference input and an external one of $10\mu F$ connected to the pad. Several simulations have been done to verify the behaviour of the reference voltage during the conversion, especially taking care to model the LC parasitic resonator due to the decoupling capacitance and the parasitic inductance of the bonding.

The two differential inputs of the ADC are driven by two buffers: the first one, connected to the positive input, is used to decoupled the analog multiplexer from the ADC input capacitance (few pF), while the negative input is connected to a fixed potential, V_{NI}, derived from the bandgap voltage. The input buffer is realized using a precision amplifier designed to achieve an offset lower than a quarter of LSB (less than $500\mu V$) and for the inputs the same component is used so

that, exploiting the differential conversion, the measurements are not affected by the buffer thermal drift.

A third buffer, whose output is connected to a pad, provides a replica of internal ADC positive input to the outside. Monitoring this voltage by means of an external high precision ADC it is possible to calibrate the internal ADC.

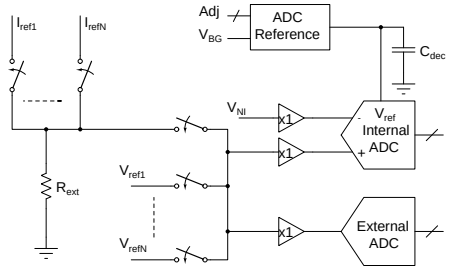

Fig. 4. Monitoring circuit scheme.

III. Experimental Results

A. Setup

Figure 5 shows the equipment used to test the VFAT3 chip: the ASIC is bonded on a dedicated small printed circuit board (6) that is connected on a bigger pcb that houses the voltage regulators used to power the chip, a 16-bit ADC necessary for the calibration discussed in the previous section and an FMC connector that provides the digital interconnection between the VFAT3 and the MOSAIC board. The MOSAIC ("MOdular System for Acquisition, Interface and Control") is a board initially designed for the readout and test of the pixel module for the silicon tracker upgrade of the ALICE experiment.

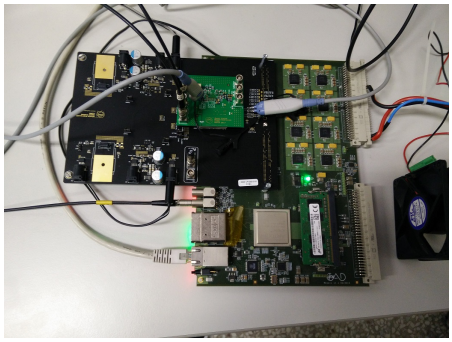

Fig. 5. Equipment used to test the VFAT3 chip.

The board is equipped with an Artix7 FPGA by Xilinx, a SODIMM 1GB DDR3 memory module and several

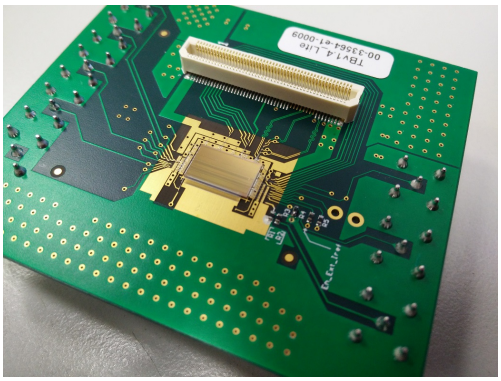

Fig. 6. VFAT3 chip bonded on its carrier board.

communication interfaces. All the communications with the board for data readout, setup and status monitoring are performed through an Ethernet interface capable of running up to 1 Gbps, high speed devices can be connected to 6.6 Gbps LVDS transceivers, two FMC connectors expand the communication lines with 68 single ended lines each that can be configured as 34 differential pairs. The MOSAIC board is compliant with the six unit Versa Modular Eurocard standard (6U-VME) for an easy housing in a standard VMEbus crate from which it takes only power supplies and cooling.

The test equipment is completed by a dedicated software with several routines developed to test all the functionalities and to perform measurements from a pc where data can be collected through the Ethernet interface for an immediate elaboration and evaluation.

B. CBM experimental results

The first component of the CBM block that has been tested is the internal ADC: scanning an internal reference DAC, the corresponding monitoring output is read by both internal and external ADCs and it is possible to create a calibration curve. The linear fitting of the calibration curve allows the extraction of the coefficients used for the conversion from the ADC digital output to the converted analog voltage. Figure 7 shows the comparison between the conversions of the external and internal ADCs for the same input after the calibration.

The bias and monitoring blocks have been tested by means of a scan of all the internal voltage and current references for all the DAC configuration values. The collected data have been compared,as shown in figure 8, with the simulation results and used to set the correct bias point of all the components of the front-end channel.

VFAT3 has been equipped with and additional test channel that allows to observe, by means of the oscilloscope, the internal voltages at the output of the main blocks of the analog

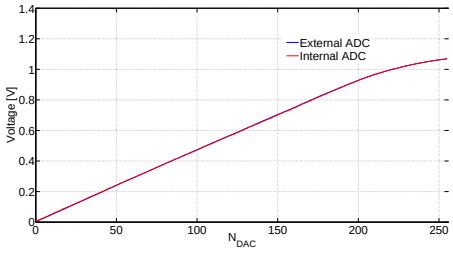

Fig. 7. Internal and external ADC conversions after the calibration phase.

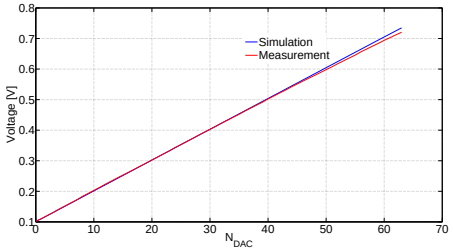

Fig. 8. Comparison between simulation and measurements for a scan of voltage reference DAC.

front-end. Exploiting this feature it has been possible, through the output of the charge sensitive amplifier (CSA), to verify the current impulse injection circuit. Figure 9 shows the CSA output for two different input current pulses where one has a width of 200ns (red curve) that is the double of the other one (blue curve) but with half amplitude. The total charge injected in both cases is the same but with a different time distribution that results really useful to evaluate the ballistic deficit of the analog front-end.

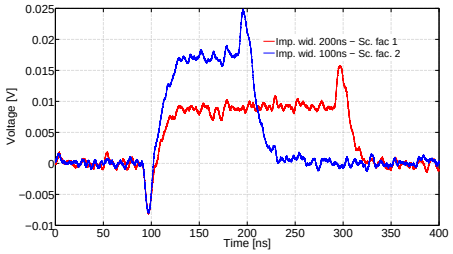

Fig. 9. Charge preamplifier output for two different injected current pulses, the amount of the injected charge is the same but with a different time distribution (red curve: impulse width 200ns and scale factor 1, blue curve: impulse width 100ns and scale factor 2).

IV. Conclusion

VFAT3 is an analog-mixed signal system that needs an accurate control and calibration of its main components. In this paper the architecture and the first measurements of the calibration, bias and monitoring block of the VFAT3 chip have been presented. The bias block has been designed in order to generate both current and voltage references temperature and power supply independent and controllable by means oft DACs. The monitoring block has an internal ADC with a dedicated reference and also provides the opportunity to fulfil the measurements by means of an external ADC. The calibration circuit generates both programmable voltage steps and current pulses that results really useful for the calibration of the inside thresholds of each analog channel.
The measurements of experimental tests are in good agreement with simulations results, thus proving that the CBM block fulfils the design specifications. A good knowledge of the bias references is a mandatory requirement for a reliable test of the analog front-end.

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[2] S. Bugiel, R. Dasgupta, M. Firlej, T. Fiutowski, M. Idzik, M. Kopec, J. Moron, and K. Swientek, "Ultra-low power fast multi-channel 10-bit adc asic for readout of particle physics detectors," *IEEE Transactions On Nuclear Science*, vol. 63, no. 5, pp. 2622–2631, 2016.

Publication IV

P. Aspell, C. Bravo, M. Dabrowski, G. De Lentdecker, G. De Robertis, M. Firlej, T. Fiutowski, T. Hakkarainen, M. Idzik, A. Irshad, P. Leroux, F. Licciulli, F. Loddo, A. Muhammad, J. Moron, H. Petrow, K. Swientek, F. Tavernier and T. Tuuva

VFAT3: A Trigger and Tracking Front-end ASIC for the Binary Readout of Gaseous and Silicon Sensors

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VFAT3: A Trigger and Tracking Front-end ASIC for the Binary Readout of Gaseous and Silicon Sensors.

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***Abstract*– VFAT3 is the front-end ASIC designed specifically for the readout of GEM detectors within the CMS experiment during the high luminosity phase of the LHC at CERN. This paper presents the analog and digital design plus the measured functional and characterization results. Key design goals were optimization to GEM charge characteristics maximizing signal to noise, timing resolution and operation at high particle rate. There are 128 front-end channels comprising preamplifier, shaper and constant fraction discriminator (CFD). Features include programmable polarity (for use with gaseous MPGD or silicon detectors), programmable gain (for linearity 9.5 fC, 28 fC and 55 fC) and programmable shaping times (15 ns, 25 ns, 36 ns and 45 ns), plus the CFD reducing time walk to less than 0.4 ns within 3 fC to 30 fC of input charge, optimizing timing resolution. An internal calibration circuit allows calibration of each channel with "GEM like" or "Silicon like" input pulses, each having programmable amplitude, polarity and phase. The ENC measures 620 e + 33 e/pF in high gain. The hit rate capability is demonstrated to 2 MHz per channel. VFAT3 has 2 output paths; the first (Trigger Path) provides hit information for every LHC clock cycle. The second (Data Path) provides data packets upon receipt of a trigger, each data packet contains hit information and time stamps. The chip can operate with trigger latencies up to 25.6 µs and is capable of receiving consecutive triggers. VFAT3 can operate with up to 2 MHz trigger rate in default mode and has data packet zero suppression capabilities to go beyond this rate. An internal dedicated Comm-Port allows communication to and from the chip. Additional features include channel input protection, internal/external temperature measurement and design for a radiation environment. The design and measurements presented demonstrate the VFAT3 capability as a complete binary front-end readout ASIC optimized for GEM detectors in the high luminosity LHC.**

I. Introduction

VFAT3 is a custom ASIC designed specifically for the front-end readout of GEM detectors. It has been designed to perform the front-end readout of GEM chambers within the CMS experiment at CERN foreseeing operation during the high luminosity phase of the LHC **Error! Reference source not found.**].

VFAT3 is a Trigger and Tracking ASIC designed in 130 nm CMOS technology. A photograph of the chip is shown in **Error! Reference source not found.**. There are 128 analog front-end channels which result in binary "hit" information per channel. There are two output paths for the trigger and tracking functions. The trigger path provides binary "hit" information in real time. The tracking path provides data packets following receipt of a trigger. Each data packet contains full granularity "hit" information plus time stamps and status flags.

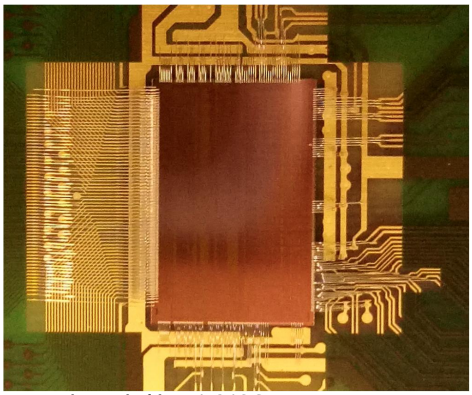

Figure 1: Photograph of the VFAT3 ASIC.

II. VFAT3 Architecture and design

The architecture of VFAT3 in block diagram format is shown in Figure 2.

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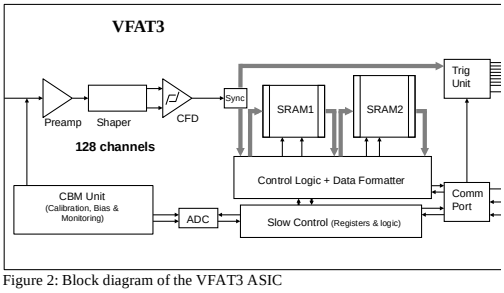


Figure 2: Block diagram of the VFAT3 ASIC

A. *The Analog Channel*

1) *Design for the GEM signal charge*

The signal charge (Figure 3) from a GEM detector is long in time (when compared to a silicon detector) and has statistical randomness in its form. The duration of the signal is derived from a knowledge of the physical dimensions of the different GEM regions and the drift velocity. Signal duration can extend up to 60 ns [2]. The randomness of the signal shape is due to clusters of ionization occurring along the particle track.

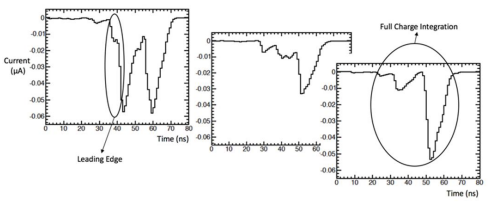


Figure 3: Three Garfield simulations of the triple GEM signal charge [2]. Plotted is the induced anode current against time. Note the signal duration and the randomness of the signal shape.

Each front-end channel consists of a preamplifier, shaper, single to differential stage [3] plus a constant fraction discriminator (CFD) [4] as shown in Figure 4. The channel has programmable gain, shaping time and a comparator with normal (Arming) or CFD mode.

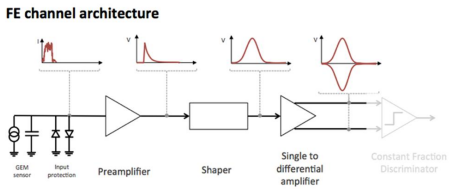


Figure 4: The analog signal channel

VFAT3 is designed to have two options for reacting to the GEM charge. The first is *Leading Edge* which reacts mainly to the leading edge of the signal charge (refer to Figure 3). In this mode the fastest shaping time is set, and the standard Arming comparator is used. Leading Edge mode is optimal for timing resolution but ignores a large fraction of the GEM signal charge due to ballistic deficit. The second option is *Full Charge Integration*. In this mode a longer shaping time is chosen such that the full (or majority) of the GEM charge is integrated hence avoiding ballistic deficit. The comparator can be switched to CFD mode which compensates time walk and results in optimized timing resolution whilst maximizing the signal to noise ratio. This is essential for optimizing GEM performance in trigger applications and is a unique feature of VFAT3.

2) *The analog front-end*

The analog front-end is shown in Figure 5 and the design detail reported in [3]. The preamplifier is based on a cascode design with an NMOS input transistor operating in weak inversion. The shaper is a second order low pass filter comprised of two OTA-C based integrators. The shaper time constant is defined by the load capacitance and the voltage gain by the OTA transconductances. Programmable gain and shaping times are achieved by switchable resistors and capacitors in the feedback of the preamplifier and the load capacitances of the shaper. Following the shaper is a single to differential amplifier to prepare the signal for the discriminator.

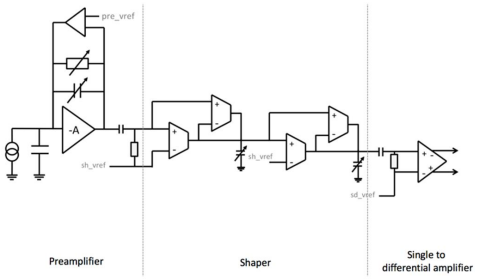


Figure 5: The front-end design

3) *The Constant Fraction Discriminator (CFD)*

Each channel has the choice of 2 comparator modes (Arming Comparator only and CFD mode).

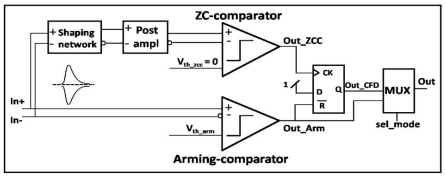


Figure 6: Block diagram of the comparator circuit

Figure **6** shows the comparator circuit. The differential input signal is first split into 2 branches; Zero Crossing (ZC) and Arming. Operation as a standard comparator uses just the Arming comparator path. Operation as a CFD uses both paths. A passive shaping network converts the inputs to a bipolar pulse with amplitude independent zero crossing (as shown in Figure **7**).

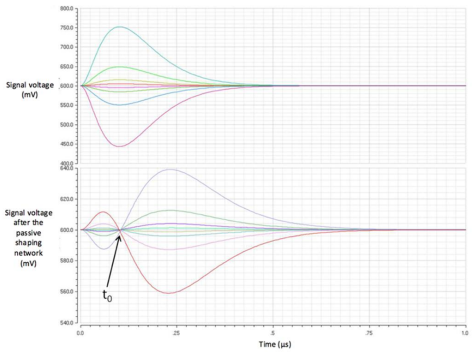


Figure 7: Simulation of the shaping network response to different signal amplitudes. T0 shows that the zero crossing is amplitude independent.

A post amplifier is then used to recover signal attenuation of the passive network. Following this a Zero Crossing Comparator (ZCC) produces a pulse when the differential input crosses the baseline. Fine adjustments are programmable via 6 bit DACs for both ZCC and Arming thresholds.

Following the comparator is a synchronisation stage which synchronises the signal pulse to the 40 MHz clock. The signal then divides into 2 paths for the Trigger Path and Data Path.

B. *The Trigger Path*

The trigger path leads to the Trigger Unit which has 9 SLVS outputs operating at 320 MHz. Eight of these are for transmitting *hit* information in real time to allow trigger building and the 9th is for a *Start Of Frame* pulse. The 8 trigger outputs can be configured to carry 64 or 128 bits of information for every 40 MHz LHC clock cycle. This is either a fast OR of every two channels at 320 Mbps or full granularity information using double data rate (DDR) at 640 Mbps.

Data Rate	Type	No. of bits	Granularity
SDR	Fast-OR	8 b/bx 64 b/bx (for 128 ch)	2
DDR	Full Channel	16 b/bx 128 b/bx (for 128 ch)	1

The DDR uses both edges of 320 MHz to transmit data.

C. *The Data Path*

The data path creates data packets corresponding to a triggered event occurring at a programmable time period in the past. Referring to Figure 2; the data path first passes through the Sync block which includes a Pulse Stretcher (PS).

1) *Synchronisation & Pulse Stretching*

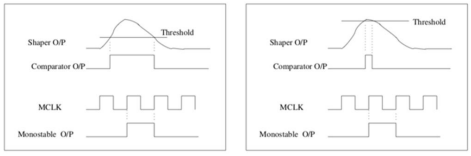


Figure 8: Synchronisation & Pulse stretching of the comparator pulse.

The synchronisation stage quantizes the comparator output to a single 40MHz clock period (Figure 8). A programmable Pulse Stretcher circuit allows the synchronised pulse to be extended from 1 to 8 clock periods in the data path.

2) *SRAMs and Control Logic*

The data path has two large SRAM blocks, Control Logic and a Data Formatter block. SRAM1 operates as a circular buffer storing binary information for all 128 channels for every 40 MHz LHC clock cycle. The depth of the memory is 1024 allowing up to 25.6 µs of history to be simultaneously stored in the memory before being over written. Receipt of a first level trigger (LV1A) identifies events to be saved into a second memory, the SRAM2. The LV1A has a constant time latency to its corresponding event of interest. This is called the LV1A latency and is programmable in VFAT3 from 1 to 1024 clock periods (25 ns to 25.6 µs). SRAM2 acts as a FIFO and is used to store triggered events with associated time tags from an internal bunch crossing counter (BC) and an event counter (EC). The SRAM2 depth is 512 corresponding to the maximum number of timeslots of triggered data that can be simultaneously stored. The control logic manages the data in and out of the two SRAMs. Consecutive triggers are permitted. This allows multiple time slots to be recorded per event if controlled externally by trigger management.

VFAT3 also has a "self trigger" option making it independent from an external trigger. The chip then becomes data driven and useful for stand alone experimental systems.

3) *Data Formatter*

The Data Formatter creates data packets to be read out in a sequential manner as soon as the chip contains triggered events. The general data packet structure is shown in Figure 9.

- Header
- Time Tags
- Data Field
- CRC

Figure 9: General Data Packet Structure

The data packet contains a Header, BC and EC counter time tags, a data field and a CRC code to ensure packet integrity. The data packet content is highly configurable to be able to deal with very high trigger rates. In its uncompressed state, the data packet contains 184 bits transmitted at 320 Mbps which corresponds to 575 ns. In this uncompressed *lossless* state; the

maximum trigger rate is 1.7 MHz. Zero suppression and other programmable options can be used to reduce the data packet size and hence allow trigger rates to go much higher.

D. Communication

1) The Comm-Port

The Comm-Port [5] is an SLVS bi-directional port operating at 320 MHz. It is designed to be compatible with the CERN GBT and lpGBT ASIC developments. Control characters are used and decoded by the Comm-Port for specific VFAT3 functions. Slow control communication to and from the chip also passes through the same Comm-Port. Encoding and a priority system avoid clashes between fast control commands and slow control data. A list of DataIn Control Characters and DataOut Characters are shown in Table 1 and Table 2.

TABLE 1: VFAT3 DATAIN CONTROL CHARACTERS & COMMANDS

Name	8b Command Character	Command
A	00000000	-
B	00001111	EC0
C	00110011	BC0
D	00111100	CalPulse
E	01010101	ReSync
F	01011010	SC Only
G	01100110	Run Mode
H	01101001	LV1A
I	10010110	SC0
J	10011001	SC1
K	10100101	ReSC
L	10101010	LV1A+EC0
M	11000011	LV1A+BC0
N	11001100	LV1A+EC0+BC0
O	11110000	EC0+BC0
P	11111111	-
CC-A	00010111	Synchronisation
CC-B	11101000	Verification of sync

TABLE 2: VFAT3 DATAOUT CHARACTERS

Name	8b Character
F1	01111110
F2	10000001
SC0	10010110
SC1	10011001
SyncAck	00111010
SyncVeriAck	11111110

2) The Slow Control

VFAT3 is highly configurable via slow control commands to write and read from a vast array of internal registers. These registers have default start-up conditions to ensure safe controlled conditions when applying power to the chip. Also included is E-fuse programmability to allow each chip to have an individual "chip ID".

E. Calibration, Bias & Monitoring (CBM)

A CBM block contains multiple DACs used for biasing the front-end analog channel. There is a calibration circuit that can generate "GEM like" or "Silicon like" charge pulses of programmable polarity, magnitude and phase. These pulses are used to calibrate each channel individually.

1) Monitoring

The Monitoring circuit is shown in block diagram format in Figure 10. An internal multiplexing circuit allows individual selection of internal voltage nodes to be sampled by an internal ADC and read back via the slow control communication. This allows calibration of an internal band-gap reference, all DACs and internal and external temperature sensors.

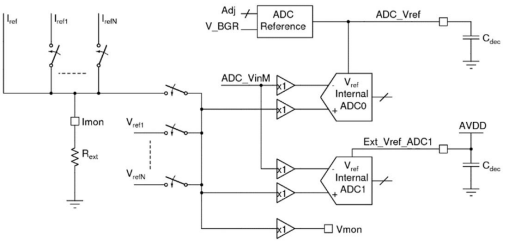


Figure 10: Block diagram of the circuit for monitoring bias DACs and calibration constants.

Two ADCs are available for this purpose, one with an internal reference and one with an external reference. The internal current DACs have their current converted to voltage by an external precision resistor. The inputs to the ADCs are also accessible to allow calibration of the internal ADCs during production test procedures.

The ADCs themselves are 10b SAR ADCs [6]. The effective resolution of which has been measured and given in Table 3.

TABLE 3: INTERNAL ADC MEASURED PERFORMANCE

Measured value	**ADC0 (1 V int. ref)**	**ADC1 (1.2 V ext. ref)**
LSB (mean)	1.9 mV	2.2 mV
Error (max) (INL)	3 mV	1.59 LSB
Error (stdev)	0.9 mV	0.47 LSB
Operational ENOB (over 1.2V SE range)	~9	~9

2) Calibration

A "silicon like" calibration pulse is generated by switching between 2 pre-charged nodes (V_{High} and V_{low}). This generates a voltage step applied to a capacitor in series with the input of a channel. The block diagram is shown in Figure 11. The magnitude of the step is controlled by a DAC controlling the V_{High} node. The polarity is control by inverting the order of switching between the two nodes. The phase of the switching is also programmable.

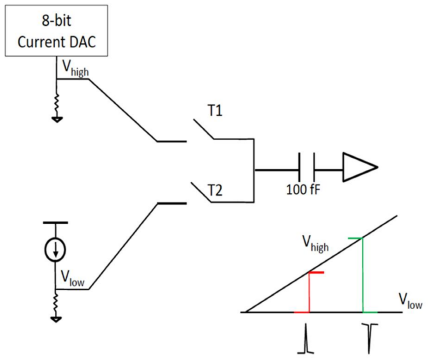


Figure 11: “Silicon like” Calibration Pulse Principle

Calibrating the magnitude of the voltage step is done by monitoring the DC values of V_{High} and V_{low} nodes. Hence the charge delivered to the input channel is :

Q_{inj} = 100 fF . ($V_{High} - V_{low}$)

The full programmable range of the injected charge is shown in Figure 12.

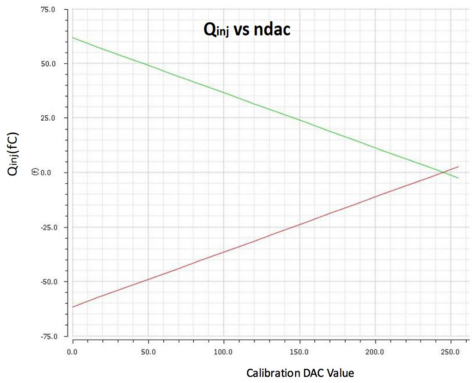


Figure 12: "Silicon like" Calibration Charge Range (both polarities). The range is from 0 fC to +- 60 fC.

A “GEM like” charge pulse is generated by the creation of a current pulse that feeds to the input of the preamplifier. The block diagram of this circuit is shown in Figure 13.

The magnitude of the current is controlled by an 8b DAC and the duration of the current pulse is programmable within the range 25 ns to 100 ns in 25 ns steps. The polarity is also programmable. Figure 14 shows the measured programmable range of the current pulse.

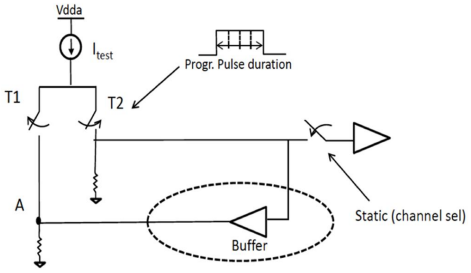


Figure 13: "GEM like" Calibration Pulse Principle

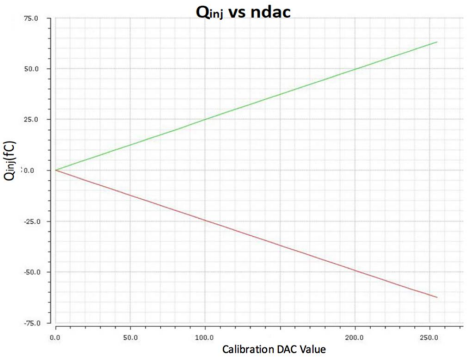


Figure 14: "GEM like" Calibration Charge Range (both polarities). The range is from 0 fC to +- 60 fC

F. Floorplan

The layout and chip dimensions are shown in Figure 15. Two versions of VFAT3 were designed, VFAT3 and VFAT3_prot. The VFAT3_prot has additional input protection resulting in a slightly wider chip. Apart from this the two versions are identical.

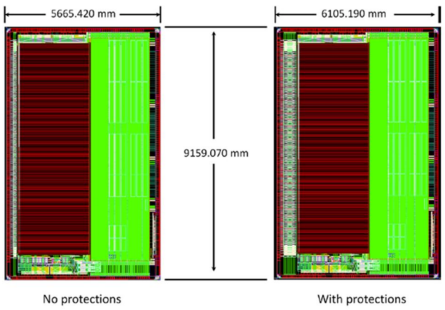


Figure 15: Full layout view of the VFAT3b and VFAT3b_prot chips

The west side of the VFAT3 contains the analog inputs. The north and south side have the power supply pads plus biasing and testability pads. The East side has the digital I/Os. The chip itself is bisected down the middle into analog and digital power domains. VFAT3 has 3 power domains in total; analog 1.2 V, digital 1.2 V and a 3rd I/O-Efuse power domain intended to operate at 2.5V.

III. Operational Flow

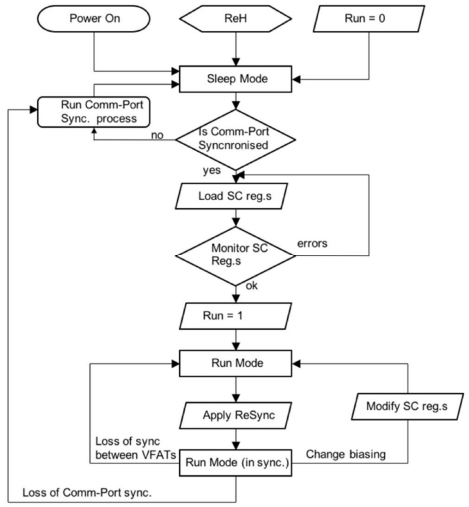


Figure 16: The VFAT3 Operational Flow

Figure 16 shows the operational flow when using VFAT3. After power is applied; VFAT3 enters *Sleep Mode* which is a safe and stable state consuming minimal power. Only the Comm-Port is active during *Sleep Mode*. An internal 40 MHz sampling clock is then synchronised by sending 3 consecutive CCA characters to the chip. VFAT3 acknowledges when synchronised. This process is used to adjust the phase of the internal 40 MHz sampling clock, adjustable in steps of 3.125 ns. The programmable settings can then be loaded and checked before applying *Run Mode*. In *Run Mode*, the programmed contents of the registers are applied and the chip becomes fully operational with is operating power consumption. Calibration routines and data taking can then follow.

IV. Measured Results

A. Analog signal chain

VFAT3 has one additional analog channel whose sole purpose is to allow buffered access to the outputs of the preamplifier, shaper and single to differential amplifier (Figure 17). The waveforms observed at these nodes are shown in Figure 18.

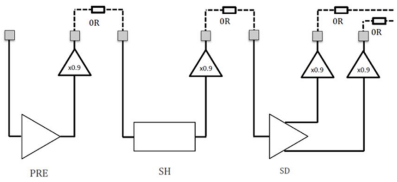


Figure 17: The Analog Test Channel

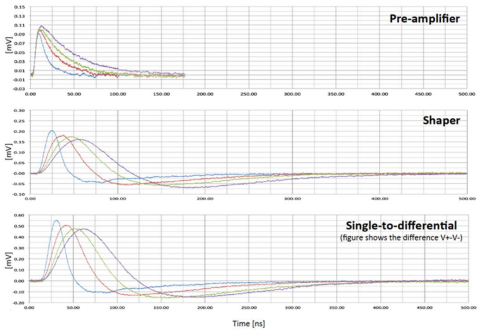


Figure 18: The analog pulse as measured on the analog test channel.

The programmable shaping times have been measured to be (15 ns, 25 ns, 36 ns and 45 ns).

Important to note is that the “return to zero” of the analog pulse is complete within 500 ns. This means that VFAT3 can operate with a hit rate of up to 2 MHz per channel before any analog baseline shift becomes evident.

B. Discriminator performance in both Leading Edge and Full Charge Integration modes.

Measurements have been performed to examine the effectiveness of time walk compensation when using the CFD technique for full charge integration compared to the Arming comparator when reacting just to the leading edge.

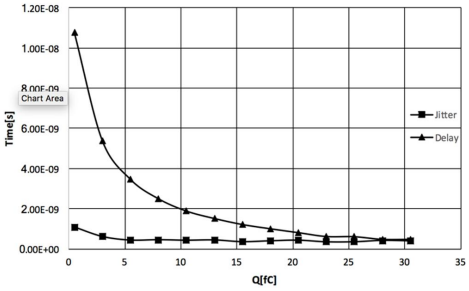


Figure 19: Discriminator performance in *Leading Edge* mode. The arming comparator is used with Tp=15 ns. Response to an IPluse of 25 ns with different magnitudes of charge. The time walk (delay) is approximately 8.5 ns.

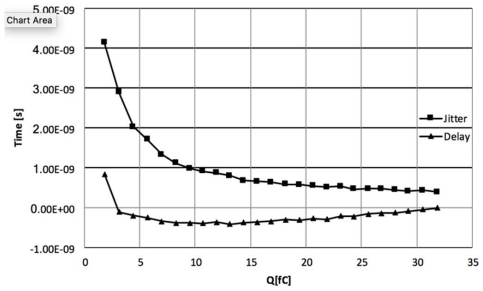


Figure 20: Discriminator performance in *Full Charge Integration* mode. The CFD comparator is used with Tp=45 ns. Response to an IPluse of 25 ns with different magnitudes of charge. . The time walk (delay) is approximately 400 ps.

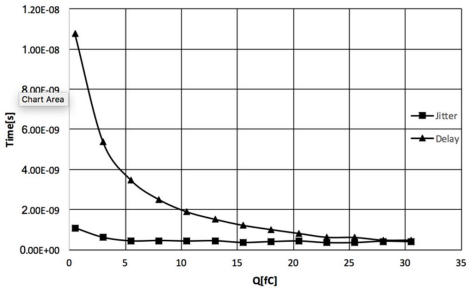


Figure **19** shows the discriminator performance in Leading Edge mode and Figure 20 in Full Integration mode. The two plots illustrate the time walk improvement when using the CFD compared to the arming comparator. With just the arming comparator the time walk is considerable at ~8.5 ns for input charge between 3 fC and 30 fC. The CFD technique reduces this to approximately 400 ps for the same input charge range. This is a very powerful option for reading charge from GEM detectors in that it allows optimization of the signal to noise ratio by integrating the full signal charge whilst maintaining optimal timing resolution.

C. S-curve measurements

The CBM circuit is used to generate internal test pulses such that S-curves can be generated for parameter measurement.

The top plot of Figure 21 shows a histogram of s-curves generated for all 128 channels of a VFAT3 chip. An *error function* fit allows the extraction of the threshold (the mean of the fit) and the noise (the sigma of the fit) for each channel. Each channel is equipped with individual threshold trim DACs that allow fine tuning of the threshold. The lower plot of Figure 21 shows all 128 channels of s-curves after threshold trimming. Threshold trimming for each channel allows the threshold spread to be reduced by up to a factor 29.3.

The measured noise performance is shown in Figure 22 for MG operation. The ENC in terms of electrons is plotted against increasing values of additional input capacitance.

The resulting noise performance and noise slope with respect to detector capacitance has been measured at:

$ENC_{(HG\ 45ns)}$ = ~650 e + 33 e/pF

$ENC_{(MG\ 45ns)}$ = ~1072 e + 28 e/pF

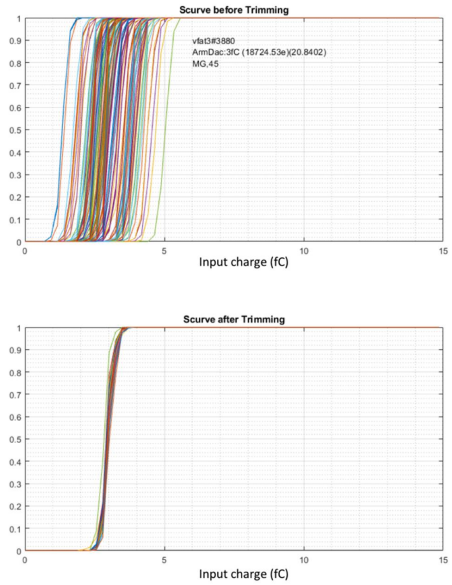
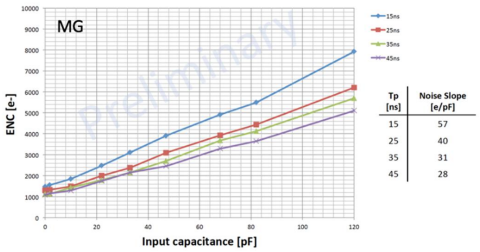


Figure 21: S-curve histograms for all 128 channels before and after threshold trimming. The threshold spread is reduced from 4537e to 155e.



Tp [ns]	Noise Slope [e/pF]
15	57
25	40
35	31
45	28

Figure 22: VFAT3 noise : ENC vs input capacitance for Medium Gain, mean results of all 128 channels.

A summary for the key measured results from VFAT3 are shown in Table 4. The gain, linearity and ENC expressed as mean results from 128 channels generated from S-curves. The

HG, MG and LG relate to High, Medium and Low gain front-end options.

TABLE 4: MAIN MEASURED PERFORMANCE RESULTS.

Parameter	**Measured performance**
Peaking times	15 ns, 25 ns, 36 ns, 45 ns
Gain & Linear Range (linear range to 10% amplitude reduction)	HG 48 mV/fC 9.5 fC MG 16 mV/fC 28 fC LG 8 mV/fC 55 fC
ENC	HG: 620 e + 33 e/pF MG : 1072 e + 28 e/pF
Time Walk (CFD mode)	< 0.4 ns (signal range 3 fC to 30 fC)
Input capacitance range	0 – 80 pF
Int. temp. measurement	20 – 110 ^{o}C with sensitivity 3.83 mV/ ^{o}C
Maximum particle rate	2 MHz/channel
Maximum LV1A rate	1.7 MHz (more if using zero suppression)
Power consumption, Vdd=1.2V (Sleep & Run Modes)	Sleep: An.= 89 mW, Dig.=60 mW Run: An.=167 mW, Dig.=80 mW

V. CONCLUSION

VFAT3 has been designed, fabricated and characterized. It is a complete trigger/tracking 128 channel binary readout chip for use with silicon or especially MPGD detectors such as GEMs. The main features of VFAT3 are summarised in Table 5. The measured performance goes well beyond the requirements for operation during the high luminosity phase of the LHC.

TABLE 5: TABLE OF KEY VFAT3 FEATURES

Key VFAT3 Features	**Note**
No of channels	128
Signal charge polarity	Positive & Negative (suitable for both silicon and gaseous MPGD detectors)
Programmable gain and shaping time	Yes
Comparator Options	Arming and CFD to optimize S/N and time walk.
Individual Channel Threshold Trimming	Yes
Internal Calibration, Bias and Monitoring	Yes, calibration possible with “silicon like” or “GEM like” charge pulses.
Trigger Path granularity	Fast OR of 2 channels 320 Mbps Full granularity, DDR 640 Mbps
Data Path : LV1A Latency Options	Programmable from 25ns to 25.6us
Consecutive Triggers supported	Yes
Self Trigger Option	Yes
Data Packet Zero suppression	Yes (numerous programmable options)
Temperature sensing	Yes, Both Internal and External (via external PT1000) temperature sensing read via VFAT3 slow control.
Comm Port compatibility	GBTx, LpGBT,

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