AVALANCHE ROBUSTNESS OF SILICON CARBIDE MOSFETS

Lappeenranta–Lahti University of Technology LUT

Electrical engineering, Master's Thesis

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Examiner(s): Prof. Pertti Silventoinen

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ABSTRACT

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Keywords: Avalanche breakdown, avalanche ruggedness, silicon carbide, power MOSFET, unclamped inductive switching.

This thesis presents a test setup and procedure to investigate the avalanche ruggedness (AR) of silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFET). This test is also known as the unclamped inductive switching (UIS) test.

The avalanche phenomenon affects the doped body of the MOSFET and its ability to block current in the reverse direction. Whenever a current through an inductance is interrupted fast, an electromagnetic counter force is induced, which consequently builds up high potentials across the switching device. Especially in snubber-less designs where inductive switching is present, the power semiconductor can be exposed to an avalanche event, which may result in device failure. Traditionally, conventional silicon device manufacturers express the single pulse avalanche energy in their datasheets, but for newer SiC MOSFETs, this information is often missing. Therefore, single pulse avalanche energies were determined for the tested devices as part of this work.

The aging aspect of AR testing involves exposing the device under test (DUT) to avalanche energies below the point of irreversible breakdown. In this study, SiC MOSFETs from two different manufacturers were stressed by repeated single-pulse avalanche exposure at a frequency of one hertz and energies slightly below their determined maximum values. The DUTs were electrically characterized and imaged with X-ray and scanning acoustic microscopy throughout the tests to assess the inflicted degradation. Failure analysis of the failed DUTs from the first manufacturer revealed three distinct failure modes, whereas no definite conclusions could be drawn for the DUTs from the second manufacturer. Finally, a complete AR testing and workflow procedure were presented for carrying out the AR test successfully.

The AR test setup and the developed process proved to be valuable in determining the avalanche ruggedness of SiC MOSFETs, as well as a valuable test for supporting the overall reliability evaluation of a power semiconductor device.

TIIVISTELMÄ

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Sähkötekniikka

Jimmy Ingman

Vyöryläpilyöntikestävyys SiC-MOSFET komponentissa

Sähkötekniikan diplomi tutkielma
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Tämä diplomityö käsittelee piikarbidi-MOS-transistorin (SiC MOSFET) vyöryläpilyöntikestävyyden testausta, eli AR-testausta (avalanche ruggedness), ja sitä varten rakennettua testilaitteistoa. Kyseinen testimenetelmä tunnetaan myös nimellä UIS-testi (unclamped indutctive switching).

Vyöryläpilyönti koettelee MOS-transistorin virran estokykyä sähkötermisesti. Virtapiirin äkillinen avaus saa aikaan voimakkaan sähkömagneettisen vastavoiman, joka aiheuttaa korkean potentiaa-lieron piikarbidisirun yli. Tämän nopean jännitepiikin energia saattaa johtaa komponentin hajoami-seen. Perinteisesti valmistajat ilmoittavat kuinka suurienergiaisen piikin eli läpilyöntienergian kom-ponentti kestää, mutta uudemmille piikarbidi-MOS-transistoreille tätä tietoa harvemmin annetaan. Tämän vuoksi maksimaaliset läpilyöntienergiat selvitettiin testattaville komponenteille työn osana.

Eritoten diplomityössä haluttiin tutkia testattavien komponenttien kestävyyttä useamman peräkkäisen vyöryläpilyönnin tapauksessa; tätäkään tietoa ei piikarbidi-MOS-transistoreille ole saatavilla. Työssä tähän tarkoitukseen kehitetyssä testissä läpilyöntienergia asetettiin hieman alle selvitetyn maksimaalisen arvon, jotta testattavia komponentteja rasitettaisiin mahdollisimman paljon, mutta kuitenkin siten että ne kestäisivät useamman sadan pulssin sarjan yhden hertsin taajuudella. Ennen testiä ja sen jälkeen komponentit karakterisoitiin sähköisesti sekä kuvattiin röntgenillä ja ultraäänellä, jotta rasituksen mahdollisia vaikutuksia voitaisiin arvioida.

Yllä käsitellyt toimenpiteet kostettiin prosessiksi, jonka mukaisesti testattiin kahta eri valmistajan kaupallisesti saatavilla olevaa piikarbidi-MOS-transistoria. Toisen valmistajan komponenttien havaittiin vikaantuvan kolmella eri tavalla, kun taas toisesta oli vaikeampi tehdä johtopäätöksiä. Testilaitteisto ja kehitetty prosessi osoittautuivat toimiviksi vyöryläpilyöntikestävyyden selvittämiseksi.

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Thank you, thank you, thank you.

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Jimmy Ingman

Greek characters

ϵ_S	relative dielectric constant

Roman characters

C	capacitance	[F]
i, I	current	[A]
f	frenquency	[Hz]
R	resistance	[Ohm]
T	temperature	[^{o}C, K]
t	time	[s]
u, U	voltage	[V]
L	inductance	[H]
P	power	[W]
q	elementary charge	[C]

Symbols

D	drain of MOSFET
E	electric field
E_{AV}	avalanche energy
E_C	critical electric field
G	gate of MOSFET
I_D	drain current
I_{DS}	drain to source current
I_{DSS}	drain to source leakage current
I_{GS}	gate to source current

I_{GSS}	gate to source leakage current
N_{D}	doping concentration in the drift region
R_{A}	MOSFET accumulation region resistance
R_{D}	MOSFET drift region resistance
R_{DSon}	MOSFET drain source on-state resistance
R_{S}	MOSFET source resistance
R_{sub}	MOSFET substrate resistance
S	source of MOSFET
T_{J}	junction temperature
t_{AV}	time in avalanche
t_{off}	signal off-time
t_{on}	signal on time
$V_{\mathrm{BR(eff)}}$	effective avalanche breakdown voltage
V_{DB}	breakdown voltage
V_{DC}	DC-Voltage
V_{DD}	supply voltage
V_{DS}	drain-source voltage
V_{GS}	gate-source voltage
V_{GSth}	gate-source threshold voltage
V_{in}	input voltage
V_{out}	output voltage
V_{th}	MOSFET threshold voltage

Abbreviations

ABB	Asea Brown Boveri
AC	Alternating Current
AR	Avalanche Ruggedness
EMF	Electromagnetic force
DC	Direct Current

DUT	Device Under Test
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
RMS	Root-Mean-Square
SAM	Scanning Acoustic Microscopy
SC	Short Circuit
Si	Silicon
SiC	Silicon Carbide
SOA	Safe Operating Area
TO	Transistor Outline
UIS	Unclamped Inductive Switching
VD	Vertically Diffused
WBG	Wide bandgap

Contents

1 Introduction

Over the past decade, silicon carbide (SiC) power Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) manufacturing technology has experienced rapid technological development and is nowadays a commercial reality and available from numerous manufacturers with various ratings. SiC power MOSFETs are nowadays in the spotlight and are one of the most typical SiC devices available in the market.Compared to conventional silicon-based MOSFETs, silicon carbide MOSFETs delivers a higher switching frequency capability, lower on-state resistance, and better off-state performance due to a small leakage current (Elasser & Chow, 2002; Hull et al., 2011).

Before SiC power MOSFETs can be implemented in power systems on a larger scale to acquire the advantages previously mentioned, it is essential to characterize these devices in terms of their robustness and reliability. Unclamped inductive switching (UIS) and short circuit (SC) tests are widely used in the power electronics industry to determine the limits of the device's safe operating area (SOA) (Fayyaz et al., 2017). This thesis will focus on the first testing methodology, unclamped inductive switching, also known as avalanche ruggedness (AR).

Power MOSFETs are widely used in high switching frequency applications where inductive loads are present, for example, motor drive applications and flyback converters. These applications require the device to withstand a particular duration of avalanche breakdown. Power MOSFET encounters an avalanche breakdown between the drain and source at the cut-off transient. This fast current interruption of an unclamped inductive load produces a back electromagnetic force dissipating into the device and the harsh switching transient could damage the device or cause it to fail. AR is an essential feature for a power device which defines its capability to dissipate avalanche energy E_{AV} without catastrophic device failure. This also enables the design to be snubber less, thus reducing the cost by a smaller number of components and decreasing the converter size. (Fayyaz et al., 2017)

The goal of this thesis is to provide a test setup to compare the repetitive AR of SiC power MOSFETs. A testing procedure to investigate the effects of the AR test as well as how to evaluate the aging parameters are also proposed in this thesis. Finally,

SiC MOSFETs of two different suppliers are tested and benchmarked in an effort to verify the proposed testing scheme as well as to investigate usefulness of the AR test in terms of component reliability testing. The usefulness of the AR test is further address through failure analysis of a few selected failed samples. However, determination of the true root cause of the failure is beyond the scope of this thesis.

In Chapter 2, the general aspects of SiC semiconductors are discussed, and a brief comparison between the SiC and the silicon-based power MOSFET is presented. An introduction to different SiC power MOSFET structures is also provided followed by an overview of the switching characteristics of the SiC MOSFET related to the AR test. Chapter 3 presents the designed AR test setup and the measurements obtained during an avalanche event. In Chapter 4, the implemented testing procedure is presented as well as how the aging parameter values for the device under test (DUT) are discovered. In Chapter 5, the analysis of the measurement results of two different suppliers tested in the AR test are examined in detail and the final findings are presented and discussed in Chapter 6. Finally, the conclusions of this thesis are presented in Chapter 7 as well as some future work. The block diagram of the AR test setup designed for this thesis is given in the Appendix.

2 Silicon carbide power MOSFET

The power MOSFET is a semiconductor device widely used for high power conversion in electronic devices. MOSFETs are used in various applications such as power supplies, consumer electronics, automotive electronics, and electric power converters (Witczak et al., 2021). Power MOSFET devices have long been critical components in power converters due to their high switching frequency characteristics (Elasser & Chow, 2002). The leading semiconductor manufacturing material for the past two decades has been silicon (Si). Si-based power devices have approached their physical performance limitations, leading to new materials being investigated (She et al., 2017). Lately, new semiconductor counterpart materials such as silicon carbide (SiC) have been introduced to the power device markets.

The SiC technology enables manufacturing of power semiconductor devices with significantly increased voltage capabilities ($\geq 0.6 - 3.3\ kV$) compared to the conventional silicon-based technology ($\leq 1\ kV$) (ROHM, 2020*b*, p. 11). The essential properties of SiC-based power devices originate from their wide band gap (WBG) semiconductor materials and allows for low-on resistance, which reduces switching losses and permits higher switching frequencies than with Si-based power devices (She et al., 2017). SiC offers ten times higher electric-field breakdown capability and three times higher thermal conductivity, allowing the SiC devices to operate at higher power densities and temperatures than the counterpart Si devices (Elasser & Chow, 2002; She et al., 2017). The essential characteristics of silicon compared to silicon carbide are summarized in Figure 1. The benefits provided by SiC properties can be translated into system-level advantages by reducing the system size, weight, and cost over systems using Si devices (Elasser & Chow, 2002; She et al., 2017).

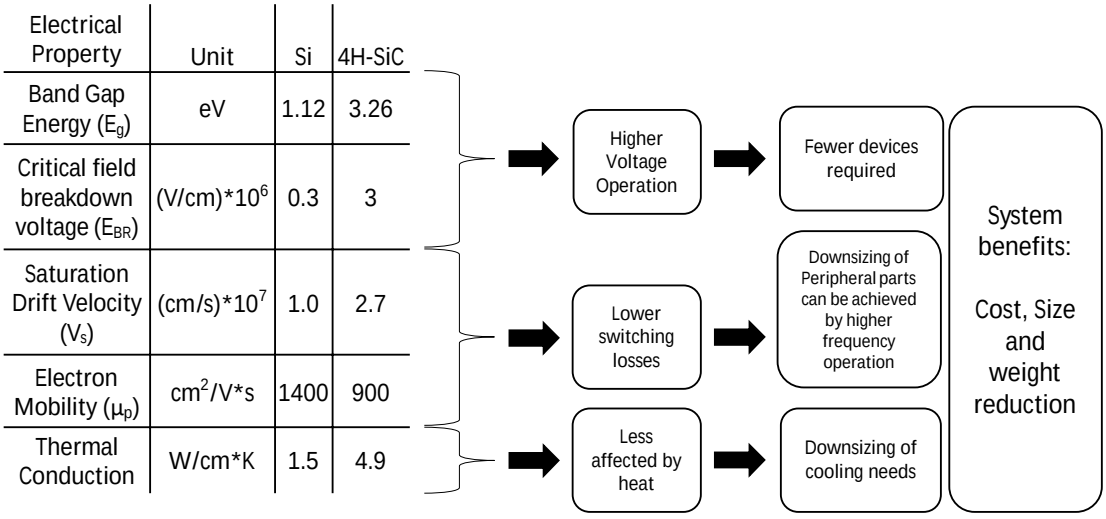

Figure 1: Semiconductor material properties (ROHM, 2020*a*, p. 5).

The following chapters examine the structure and operation principle of the SiC-based power MOSFET.

2.1 Structure

A silicon carbide MOSFET structure is very similar to its counterpart Si MOSFET. Power MOSFETs are typically packaged discretely, meaning that only one semiconductor chip is assembled inside a package. The most dominating packaging method for power MOSFETs has been the transistor outline (TO) family, of which the most typical standardized transistor packages are the TO-220 and TO-247. These packages consist of three leads, also called legs or pins. Two of the leads are attached to different areas of the power silicon chip via bond wires, commonly made of aluminum or copper. The MOSFET chip is soldered straight to a solid mounting surface of copper, which is a part of the last lead. All the pieces are fixed by a transfer mold, leaving only the legs and, for some devices, the backplate bare. In applications, the MOSFET legs are soldered to the printed circuit board (PCB), where the backplate of copper is typically attached to an external heat sink for greater cooling performance. A simplified drawing of a TO-247 packaged MOSFET is shown in Figure 2. (Lutz et al., 2018, p. 433)

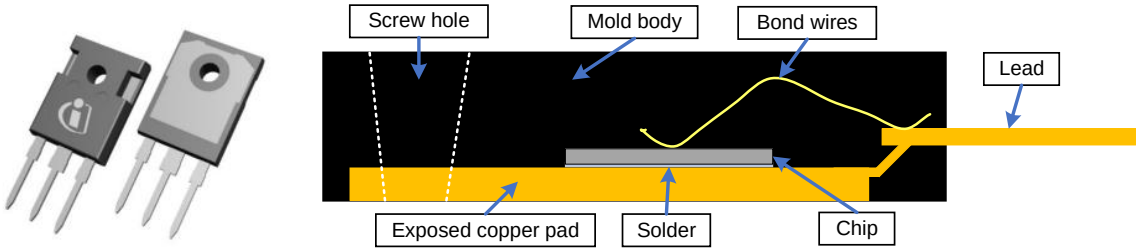

Figure 2: Power MOSFET packing principle. TO-247 package on the left-hand side (Lutz et al., 2018, p. 433).

One of the typical die structures of a power MOSFET is the Vertical Diffused (VD) MOSFET, also known as the planar structure. The device consists of three different terminals: Gate (G), Drain (D), and Source (S). The gate and source terminals are located on the structure's top side. The two terminals are connected to the legs of the package via the internal bonding wires. The drain terminal is found on the bottom side of the structure and is attached to the device's backplate. The word "Vertical" represents the current flowing vertically from the drain terminal to the source terminal when a positive voltage is applied to the gate. The "Diffused" refers to the manufacturing process called diffusing. With this technique, individual cells are formed consisting of p-wells and diffused n+ areas of the semiconductor, which allows the functionality of the device channel (Lutz et al., 2018, pp. 344-345).

Another typical die structure of a power MOSFET is the U-MOSFET, also known as the trench-gate structure. The main difference in the structure comes from how the gate in the cells is constructed, also termed gate build-up. The gate trench stretches from the upper surface of the structure through the n+ source and p base regions into the n- drift region (Baliga, 2018, p. 289). Both structures are illustrated in Figure 3, where (A) represents the planar structure, and (B) the trench-gate structure.

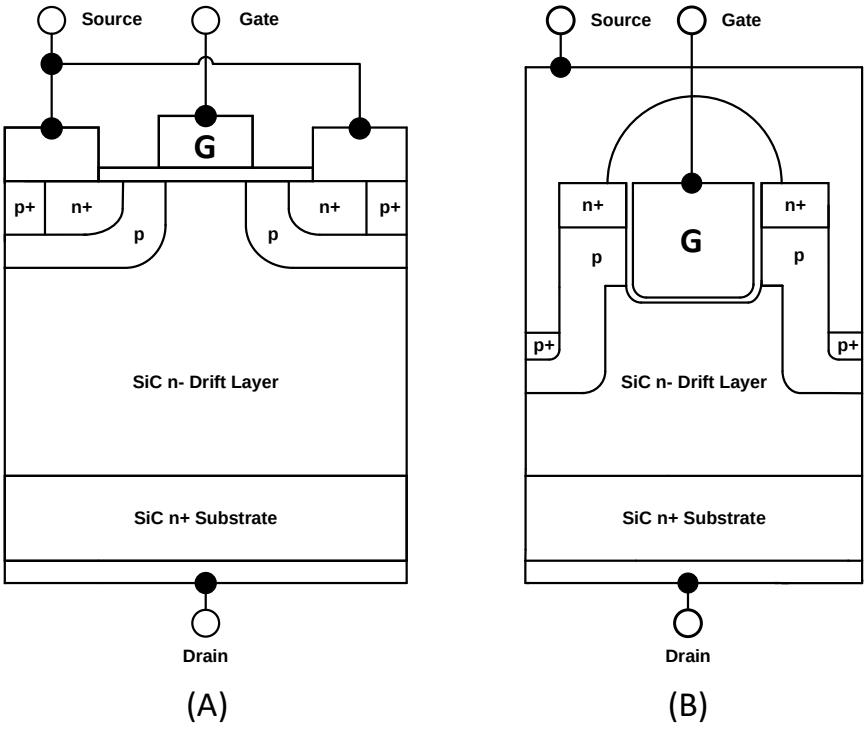

Figure 3: Regular SiC MOSFET structures (A) planar and (B) trench.

As seen in Figure 3 above, the difference between these two structures comes mainly from the gate build-up. The essential difference is the amount of on-resistance during forward conduction. The on-resistances affect the structures' different current flow paths and will be discussed in the next section.

2.2 Operation

2.2.1 On-state

The power MOSFET is turned conductive with a positive gate-source voltage V_{GS}. As the voltage is applied between the gate and the source, an inversion layer channel at the surface of the p base region under the gate electrode starts to form. When the applied gate voltage V_{GS} surpasses the gate threshold voltage V_{GSth}, the inversion layer channel extends from the n+ source region to the n- drift region. It forms a conduction path between the drain and the source terminals, and if a positive drain-source voltage V_{DS} is applied, the current flows vertically between the drain and source via this inversion layer channel. If the gate-source voltage V_{GS} drops below the gate threshold voltage V_{GSth}, the channel is closed, and the current flow is shut. (Baliga, 2010, pp. 23-24)

At the start of the conduction, the current passes several resistive components collectively called on-state resistance R_{DSon} (Baliga, 2011, p. 239). The planar structure's on-state resistance is divided into seven different resistances. Six of them are related to the chip: the n+ source diffusion resistance R_{Source}, channel resistance R_{ch}, accumulation-layer resistance R_{A}, "JFET" component-resistance R_{J}, drift-resistance R_{D}, and the n+ substrate resistance R_{sub}. The seventh resistance R_{wcml} is related to the packing factors. This resistance R_{wcml} combines the sum of bond wire resistance R_{BW}, the die attach solder resistance R_{Die}, and the contact resistance R_{C} between the metallization-to-chip (Dusmez et al., 2016). The total on-state resistance for a planar type MOSFET is the sum of the individual resistances of each layer and region and can be calculated as (Dusmez et al., 2016):

$$R_{\mathrm{DSon}} = R_{\mathrm{wcml}} + R_{\mathrm{Source}} + R_{\mathrm{ch}} + R_{\mathrm{A}} + R_{\mathrm{J}} + R_{\mathrm{D}} + R_{\mathrm{sub}}. \tag{1}$$

It is also worth mentioning that for high power MOSFETs and typically for high voltage devices, the significant contribution of the on-state resistance is the parasitically formed JFET region resistance R_{J} and the drift region resistance R_{D}. The rest of the layer and channel resistance are relatively small, and the R_{wcml} is generally negligible for such high voltage devices (Dusmez et al., 2016).

A cross-section of both structures is illustrated in Figure 4, where (A) represents the planar structure, and (B) the trench-gate structure.

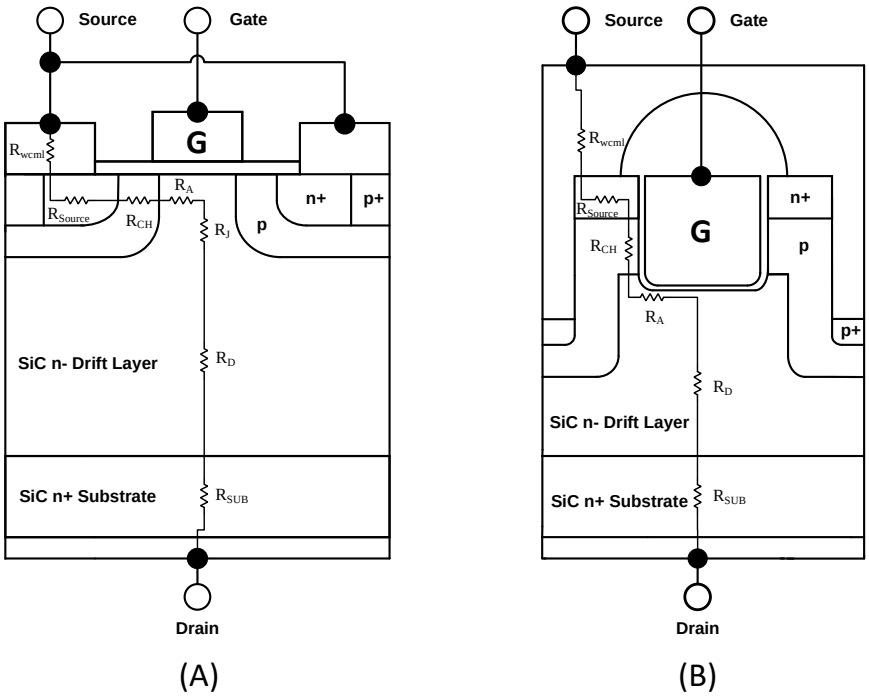

Figure 4: Regular SiC MOSFET structures (A) planar and (B) trench.

As seen in Figure 4 above, almost the same internal resistances apply to both structures. The major difference is that the JFET region is eliminated for the trench structure. The trench extends from the upper surface of the n+ source beyond the bottom of the p base region into the n- drift layer and forms a shorter channel between these two layers. Thus, the total on-state resistance is lower for a trench-gate structured MOSFET (Baliga, 2010, p. 66). The total on-state resistance for trench type MOSFET is calculated as:

$$R_{\mathrm{DSon}} = R_{\mathrm{wcml}} + R_{\mathrm{Source}} + R_{\mathrm{ch}} + R_{\mathrm{A}} + R_{\mathrm{D}} + R_{\mathrm{sub}}. \tag{2}$$

2.2.2 Switching characteristics

In order to study the switching characteristics of a power MOSFET, it is necessary to know the parasitic elements of the device. One of the parasitic elements are the parasitic capacitances that originate from the electric conductors with different potentials close to each other. This potential difference causes a charge between them and forms unwanted capacitors. For the power MOSFET structure, three different capacitances exist between the terminals and are commonly divided into the following capacitances:

Input capacitance C_{GS} between the gate and the source terminals, output capacitance C_{DS} between the drain and the source terminals, and the Miller capacitance C_{GD} between the gate and the drain terminals (Baliga, 2018, pp. 413-414).

The parasitic inductances are the other parasitic elements that affect the switching of a power MOSFET. The parasitic inductances originate from the internal electrical conductors of the device and are divided according to the device terminals: Gate inductance L_{G}, drain inductance L_{D}, and the source inductance L_{S}. (Qin et al., 2018)

These parasitic elements affect the switching behavior of the power MOSFET ether in their own way or combined with each other. The gate inductance L_{G} combined with the input capacitor C_{GS} can induce spurious oscillations in the gate voltage V_{GS} (Locorotondo et al., 2019). This again affects the device turn-on operation and can cause oscillations in the drain to the source voltage V_{DS}. This oscillation can be avoided by placing the device close to the gate drive circuit and minimizing the drive loop inductance of the circuit. The effect of this parameter is usually limited and is the least severe of the three primary sources of parasitic inductances. The drain inductance L_{D} resonating with the output capacitance C_{DS} generates a more significant effect on the switching transient of the device. This causes the oscillation to be coupled into the Miller capacitance C_{GD}, which generates oscillation in the gate loop and causes ringing in the device drain voltage V_{DS}, gate voltage V_{GS}, and drain current I_{D}. The most significant component impacting the switching transients of the MOSFET is the parasitic inductance of the source L_{S}. During the switching transient of the device, the inductance L_{S} work as negative feedback from the switching loop to the gate driver loop. As the drain current changes during switching, the voltage over L_{S} counteracts the gate voltage and, at the same instant, slows down the current flow of the device and yields higher switching losses during turn-on and turn-off of the device. (Chen et al., 2010)

The switching behavior of a SiC MOSFET can be examined with the help of a clamped inductive circuit, as shown in Figure 5. The circuit consists of two voltage sources. One of them is the supply voltage V_{DC} which provides a constant voltage to the main circuit. The other is the voltage source V_{GG} for the gate circuit and provides a step voltage via the external gate resistor R_{G} to the device gate pin. The

circuit also includes a free-wheeling diode D_{FW} connected in parallel with the load inductor L_{load}. When the MOSFET is not conducting, the load current is clamped via this free-wheeling diode. The Q represents the SiC MOSFET. L_{G}, L_{D}, and L_{S} are the parasitic inductances. These inductances originate from contact leads between the device and the circuit, where the L_{G} is the inductance between the gate pin and the gate drive circuit. L_{D} is the inductance between the main circuit and the drain pin. L_{S} is the inductance between the common ground and the source pin. The C_{GD}, C_{GS}, and C_{DS} are the gate-drain, gate-source, and drain-source parasitic capacitances originating from the MOSFET structure.

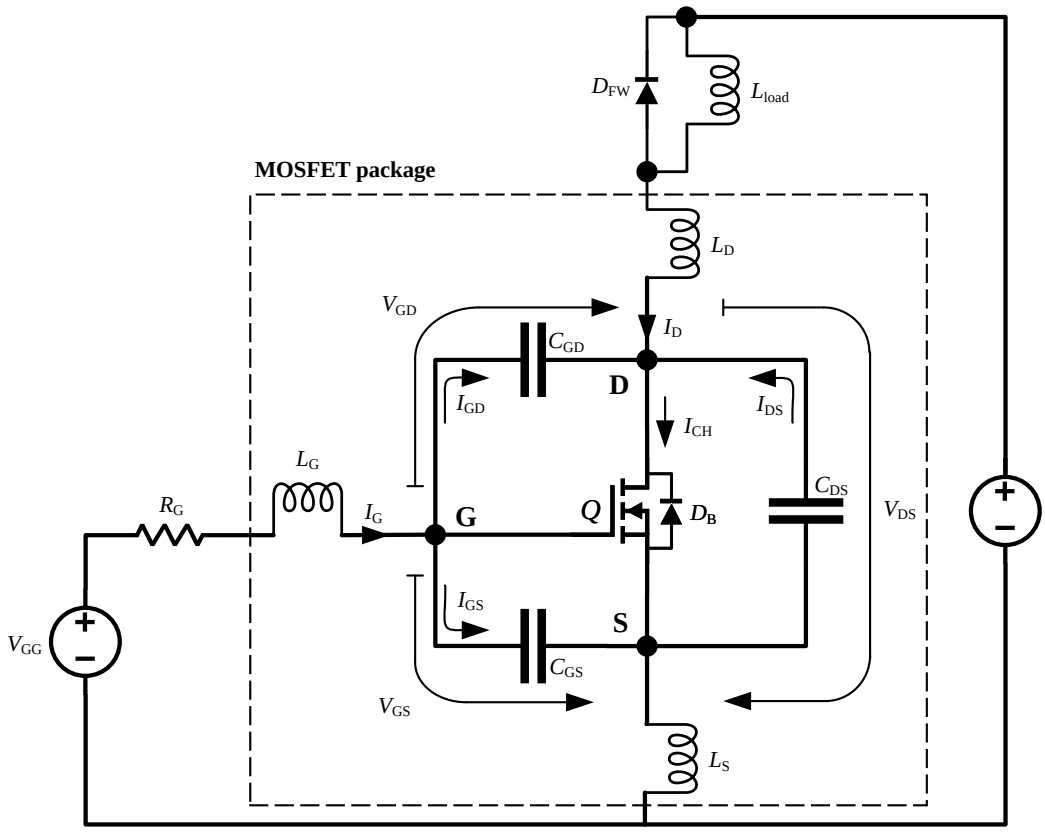

Figure 5: Power MOSFET in an ideal clamped inductive circuit.

The turn-on period can be divided into five stages, as shown in Figure 6. The first stage is the turn-on delay for the MOSFET (t_1-t_2). At time t_1, the gate signal V_{GG} increases from a negative to a positive voltage, and the gate-source voltage V_{GS} rises from a negative to a positive threshold voltage V_{GSth}. A gate current I_{G} starts to flow and charges up the input capacitance $C_{\mathrm{iss}} = C_{\mathrm{GD}} + C_{\mathrm{GS}}$ via the resistance R_{G}. During

this stage, V_{GS} raises according to the following exponential function:

$$V_{\mathrm{GS}} = V_{\mathrm{GG}}(1 - e^{\frac{t}{t_{\mathrm{iss}}}}), \tag{3}$$

where the time constant $t_{\mathrm{iss}} = R_{\mathrm{G}} C_{\mathrm{iss}}$. Under this turn-on delay stage (t_1-t_2), the MOSFET is still in off-state, zero drain current is conducted through the device's channel, and the drain to source voltage V_{DS} remains unchanged and is equal to the supply voltage V_{DC}. (Cittanti et al., 2017; Zhang et al., 2018)

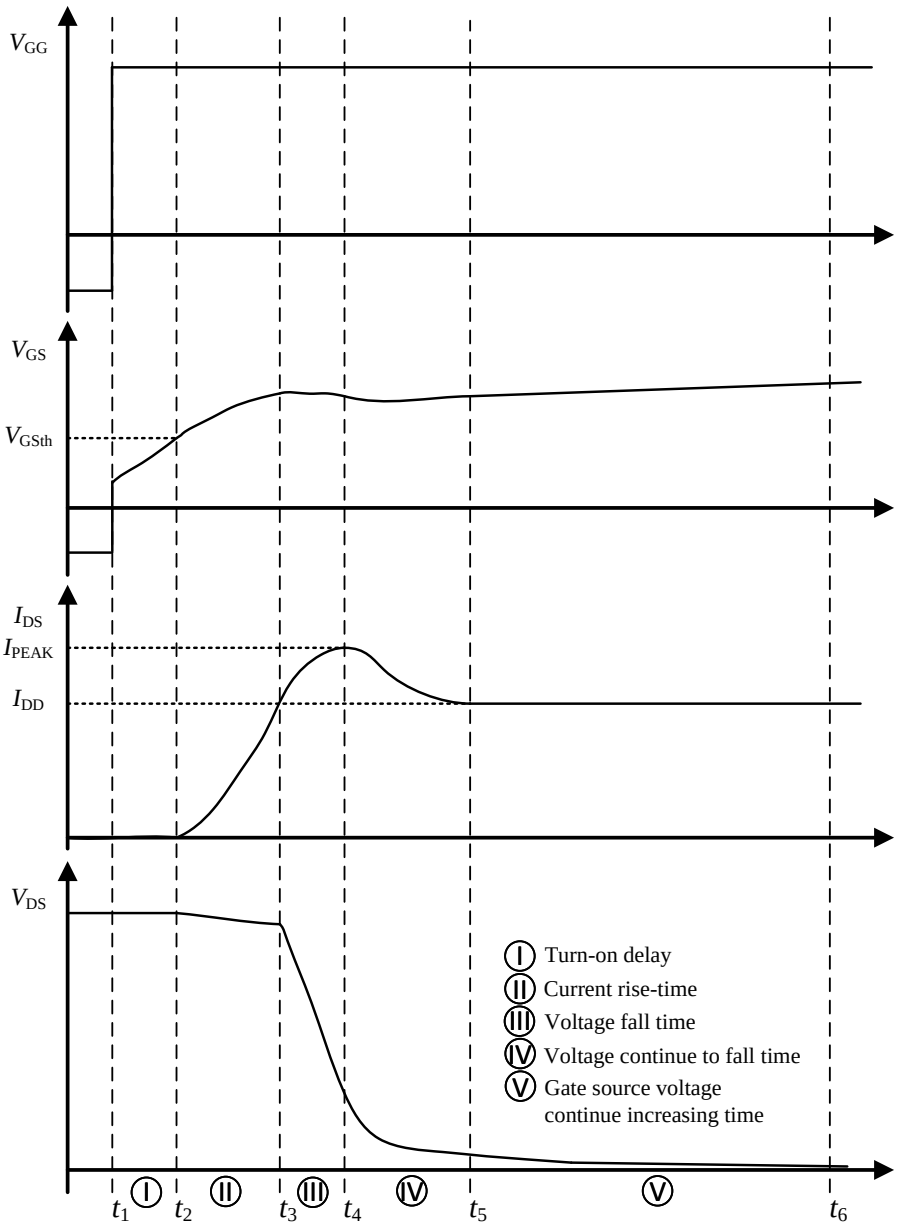

Figure 6: Waveforms of a SiC MOSFET during turn-on transient. Adapted from (Zhang et al., 2018).

The second stage is the current rise-time (t_2-t_3). At time t_2, the V_{GS} exceed the V_{GSth} level, and the current from the load starts to flow through the MOSFETs channel. During this stage, the MOSFET works as a voltage-controlled current source, and the current rises according to the following equation (Cittanti et al., 2017; Zhang et al., 2018):

$$I_{\mathrm{D}} = g_{\mathrm{fs}}(V_{\mathrm{GS}}(t) - V_{\mathrm{GSth}}), \tag{4}$$

whereby the g_{fs} is the transconductance of the MOSFET (Zhang et al., 2018; Cittanti et al., 2017).

From Figure 6, it can be obtained that a slight fluctuation occurs in both the V_{GS} and V_{DS}. This is due to the parasitic elements in the MOSFET. The fluctuation in the V_{GS} is caused mainly by the injected charge into the miller capacitance C_{GD}, but the two other parasitic capacitances C_{GS} and C_{DS}, also change in value. The decline in the V_{DS} is due to the parasitic inductance in the MOSFET and can be obtained by the following equation (Zhang et al., 2018):

$$V_{\mathrm{DS}}(t) = V_{\mathrm{DC}} - (L_{\mathrm{S}} + L_{\mathrm{D}})^{\frac{dI_{\mathrm{D}}(t)}{dt}}, \tag{5}$$

whereby the current rate of change is given by:

$$\frac{dI_{\mathrm{D}}(t)}{dt} = g_{\mathrm{fs}}\frac{V_{\mathrm{GS}}(t) - V_{\mathrm{GSth}}}{t_{\mathrm{iss}}}. \tag{6}$$

The third stage is the voltage fall time (t_3-t_4). At time t_3, the load current has been fully transferred from the free-wheeling diode, D_{FW}, to the MOSFET. The energy storage in the parasitic capacitance C_{DS} of the MOSFET starts to discharge itself via the MOSFET channel as in the following equation (Cittanti et al., 2017):

$$I_{\mathrm{DS}}(t) = -C_{\mathrm{DS}} - \frac{dV_{\mathrm{DS}}(t)}{dt}, \tag{7}$$

and the peak current I_{PEAK} conducted through the device channel is the sum of the three different currents (Cittanti et al., 2017):

$$I_{\mathrm{PEAK}} = I_{\mathrm{DD}} + I_{\mathrm{GD}} + I_{\mathrm{DS}}, \tag{8}$$

when the current surpasses the steady-state current I_{DD} level and continues to rise, the V_{DS} start to decline with a slope according to the following equation:

$$\frac{dV_{\mathrm{DS}}}{dt} = -\frac{dV_{\mathrm{GD}}}{dt} = -\frac{I_{\mathrm{G}}(t)}{C_{\mathrm{GD}}}, \tag{9}$$

where the gate to drain voltage V_{GD} is the voltage of the capacitance C_{GD}. During this voltage fall time stage (t_3-t_4), the MOSFET operates in the active region, and the peak current I_{PEAK} flowing through the device is reached at the end of this stage (t_4).

During the fourth stage, (t_4-t_5), the voltage continues to fall. At time t_4, the peak current I_{PEAK} is reached and starts to level off to the steady-state current level I_{DD}. The V_{DS} continue to decrease, and when V_{DS} is lower than V_{GS}, the operation of the MOSFET shifts from active to the ohmic region driving the device to function as a resistor rather than a voltage-controlled current source (Zhang et al., 2018). The V_{DS} decline with a slope according to Equation 9, where the gate driving current I_{G} is defined as in the following equation (Zhang et al., 2018):

$$I_G = \frac{V_{\mathrm{GG}} - V_{\mathrm{GS}}}{R_{\mathrm{G}}}. \tag{10}$$

In the fifth and final stage of the turn-on process of the MOSFET (t_5-t_6) the V_{GS} continue to increase according to Equation 3. The rate of change in the slop is driven by the time constant $t_{\mathrm{iss}} = R_{\mathrm{G}} C_{\mathrm{iss}}$, and at the end of this stage (t_6), the parasitic capacitance C_{GD} has been completely charged, the gate to source voltage V_{GS} is leveled to gate driver voltage V_{GG}, and the MOSFET is now turned on and works in a steady state. (Zhang et al., 2018)

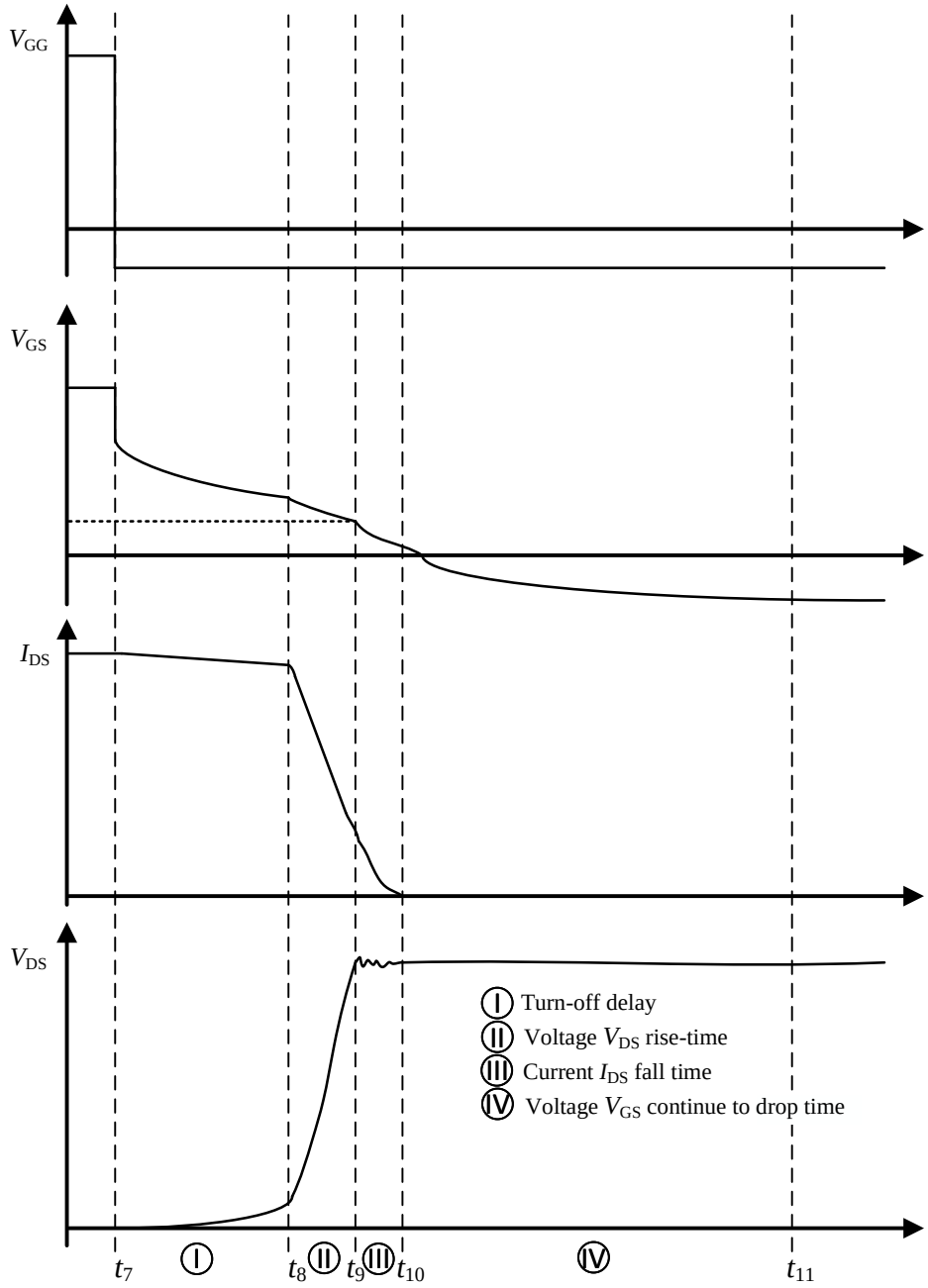

Figure 7: Waveforms of a SiC MOSFET during turn-off transient. Adapted from (Zhang et al., 2018).

The MOSFET turn-off process is similar to the turn-on process and can be divided into four stages, as shown in Figure 7. The first stage is the turn-off delay time (t_7-t_8). At time t_7, the gate signal V_{GG} is shifted instantaneously from positive to a negative voltage. The driving loop discharges the input capacitance C_{iss} through the gate resistor R_G and L_S, and the gate voltage V_{GS} drops slightly and starts to decline exponentially, according to Equation 3. During this stage, the gate current I_G can be

defined as follows (Zhang et al., 2018):

$$I_{\mathrm{G}} = (C_{\mathrm{GS}} - (C_{\mathrm{GD}})\frac{dV_{\mathrm{GS}}}{dt}. \tag{11}$$

From Figure 7, it can be noticed that the drain to source voltage V_{DS} starts to increase and is mainly driven by the increasing resistance in the device channel. During this stage (t_7-t_8), the MOSFET works in the ohmic region.

In the second stage, (t_8-t_9), termed voltage rise time stage, the V_{DS} voltage rises and at time t_8, the MOSFET transfers from the ohmic region to the active region. The V_{GS} continues to decrease, and at the end of this stage, the V_{GS} hits the threshold level V_{GSth}. The decline of the V_{GS} relies on the Miller effect and is mainly driven by the discharge of the Miller capacitance C_{GD}. The drain current I_{DS} fall rapidly, whereas the drain to source voltage V_{DS} rises sharply and levels off to the supply voltage V_{DC}. (Zhang et al., 2018)

In the third stage, (t_9-t_{10}), is the drain current fall time stage. At time t_9, the V_{GS} continue to decline and surpass the threshold voltage V_{GSth} level, whereby the input capacitance C_{iss} has been fully discharged. A slight overshoot is noticed in the V_{DS} due to the free-wheeling diode becoming forward-biased, whereby the load current starts to transfer from the MOSFETs channel to the diode. At the end of this stage (t_{10}), the drain current reaches zero, and the V_{DS} continue to be equal to the supply voltage V_{DC}. (Zhang et al., 2018)

In the fourth and last stage, (t_{10}-t_{11}), of the turn-off process, the V_{GS} continue to drop and at time t_{10}, the V_{GS} decrease to the negative voltage applied to the MOSFETs gate. The load current is conducted through the free-wheeling diode, and the drain current I_{D} is equal to zero. The V_{DS} equals to the supply voltage V_{DC}, and the MOSFET operates in the cutoff region. (Zhang et al., 2018)

2.3 Avalanche breakdown

Power semiconductor devices such as SiC MOSFETs are designed to withstand high voltages and low drain leakage current during the OFF state of the device. The avalanche breakdown (AR) phenomenon relies on the distribution of the electric field

(E) inside the structure of the device. During the development of the desired device, doping of the n- drift layer is carefully selected to acquire the preferred breakdown voltage class. The equations defining the breakdown voltage V_{BD} for non-fully n depleted region structures can be defined as the following Equation (Baliga, 2010, p. 7):

$$V_{\mathrm{BD}} = \frac{\varepsilon_{\mathrm{S}} E_{\mathrm{C}}^2}{2qN_{\mathrm{D}}}, \tag{12}$$

where ε_{S} is the dielectric constant for the semiconductor material, E_{C} is the critical electric field for the breakdown of the semiconductor material, q is the charge of an electron, and N_{D} is the doping of the n type drift region.

The risk of an avalanche phenomenon occurs, for instance, when a current through an inductance is interrupted. This reserved energy in the inductance will build up a counter electromagnetic force (EMF) which induces a high potential across the switching device. The induced potential difference occasionally exceeds the device's rated breakdown voltage V_{DSmax}, which produces a high electric field across the reversed biased p-n junction. The strong electric field causes mobile carriers with sufficient energy to collide with lattice atoms, resulting in the generation of electron-hole pairs. This is correspondingly known as impact ionization. The electron-hole pairs induced due to impact ionization result in the generation of additional electrons and hole pairs. Practically the impact ionization is a multiplicative phenomenon producing a continuous flow of electrons via the depletion region, which results in a significant flow of current through the device drain and source. Since the device cannot withstand the use of higher voltages due to the rapid increase in current, the device is considered to be subjected to an avalanche breakdown. Therefore, the avalanche breakdown limits the maximum operating voltage of the semiconductor device. (Baliga, 2018, p. 90)

During the breakdown event, as the voltage is high and the current increases, the power increases beyond the power dissipation capability of the device, eventually leading to thermal runaway in the active area of the chip. (Kelley et al., 2016)

The occurrence of avalanche breakdown has been met in the Flyback converter (i.e., typical example for avalanche mode of operation), where during the turn-off of the transistor, a high overvoltage can be induced by the magnetizing inductance of the

transformer (McDonald et al., 2011, p. 4).

3 Avalanche ruggedness test

This chapter describes the test bench designed and built to study the avalanche ruggedness phenomenon of SiC power MOSFET. In addition, the procedure of how the investigated device is triggered into an avalanche event is discussed, as well as the electrical measurements performed during the event. Finally, the measurement equipment and the parts used in the test setup are presented.

3.1 Test system

A test setup was designed and built to investigate the reliability of power MOSFETs AR. The purpose of the test setup is to enable robustness assessments of different MOSFET suppliers. The test focuses mainly on device-level reliability. Typically, these tests are performed by the MOSFET suppliers to give the datasheet an energy value that the device can withstand during an avalanche event. However, the suppliers' datasheets reveal a considerably diverse amount of information on the avalanche robustness, and often are not mentioned at all. Especially when datasheets of SiC MOSFETs are considered the AR information is most often lacking. The main goal with the proposed AR test and testing scheme in this thesis is to get a unified overview of various suppliers' avalanche capabilities by comparing the maximum energy dissipation that the different devices can withstand in the avalanche mode.

The test setup built and used in this study is comparable with common AR tests. The device is in series with an inductor. The inductor has an inductance value L able to store up to ten times the MOSFETs datasheet rated avalanche energy E_{AV} for a given drain to source current I_{DS} and selected supply voltage V_{DC}. The supply voltage V_{DC} value shouldn't exceed the maximum rated drain to source voltage V_{DSmax} of the MOSFET. The gate voltage V_{GS} and gate resistance R_{G} used under the test are the ones recommended in the MOSFETs datasheet.

3.2 Test description

By combining a power MOSFET in series with an inductive load, the AR of the device can be investigated. The combination of the device's high-speed switching and the

inductive load causes a high surge voltage between the drain and source at the turn-off phase. This induced high voltage often exceeds the rated breakdown voltage $V_{\mathrm{BR(DSS)}}$, which will trigger the device into avalanche mode. By the repetitive occurrence of the avalanche events, the qualification of the semiconductor device needs to be able to suppress (or survive) its datasheet specified avalanche energy E_{AV}, while keeping its characteristics after the test within datasheet specifications.

A standard test circuit for performing an AR test and its avalanche curves is shown in Figure 8. The device is mounted onto a TO-247-3 socket holder located on the test board. A clip-on heating sink is attached to the MOSFET. The device is series-connected with an inductor L, and the circuit branch is arranged in parallel with a DC capacitor C charged by a DC power supply V_{DC}. A waveform generator controls the gate driver of the MOSFET. The avalanche energy E_{AV} for the MOSFET in the circuit can be calculated as (Ionita et al., 2017):

$$E_{\mathrm{AV}} = \frac{1}{2} L I_{\mathrm{AV}}^2 \frac{V_{\mathrm{BR(eff)}}}{V_{\mathrm{BR(eff)}} - V_{\mathrm{DC}}}, \tag{13}$$

where L is the inductance of the series inductor, I_{AS} is the peak avalanche current when the gate is turned off, $V_{\mathrm{BR(eff)}}$ is the effective avalanche breakdown voltage at peak discharge current, and V_{DC} is the supply voltage.

It is worth mentioning that $V_{\mathrm{BR(eff)}}$ must be higher than the MOSFETs breakdown voltage given in the device datasheet. Typically, the manufacturers implement a safety margin in their design. And as a rule of thumb, the effective breakdown voltage can be considered by the Equation (Renesas, 2015, p. 3; Berry et al., 2020, p. 105):

$$V_{\mathrm{BR(eff)}} \cong 1.3 * V_{\mathrm{BR(DSS)}}, \tag{14}$$

where $V_{\mathrm{BR(eff)}}$ is the effective drain to source breakdown voltage at peak discharge current, and $V_{\mathrm{BR(DSS)}}$ is the rated drain to source breakdown voltage of the MOSFET.

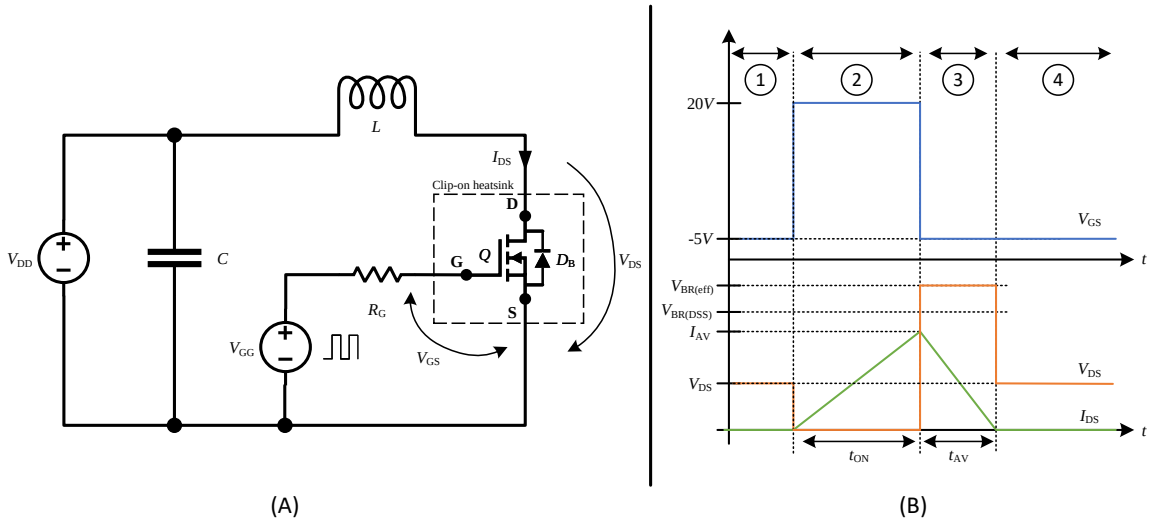

Figure 8: Simplified circuit of an avalanche ruggedness test setup; (B) voltage and current waveforms during an avalanche breakdown event.

However, a more precise calculation for the avalanche energy E_{AV} can be obtained using the current and voltage measurements of the device by (McDonald et al., 2011, p. 9):

$$E_{\mathrm{AV}} = \int_{t_1}^{t_2} V_{\mathrm{BR(eff)}}(t) \times I_{\mathrm{AS}}(t) \times dt. \tag{15}$$

3.3 Performing an avalanche event

As shown in Figure 8, performing a single avalanche event can be divided into four intervals. During the first interval, the MOSFET is OFF, no current or voltage flows through the device, and only the static supply voltage V_{DC} is seen. The second interval starts as the gate driver is turned ON for a predefined on-time t_{ON}. The current across the MOSFET starts to increase linearly to the desired test current according to the inductor L in series value and the supply voltage V_{DC} at the rate defined by (Ionita et al., 2017):

$$\frac{di}{dt} = \frac{V_{\mathrm{DC}}}{L}, \tag{16}$$

where V_{DC} is the supply voltage, and L is the series inductor inductance.

The third interval starts as the gate driver is switched-off, which abruptly turns off the MOSFET. The turn-off of the MOSFET opens the circuit, and the energy built up in the inductor L will dissipate its stored energy into the device. This inductive current

continues to flow, causing a high voltage across the drain to the source. This voltage passes the breakdown voltage $V_{\mathrm{BR(DSS)}}$ and is clamped to the effective breakdown voltage $V_{\mathrm{BR(eff)}}$ until the load current reaches zero. If the device passes the avalanche phase, the last and fourth interval begins. The effective breakdown voltage $V_{\mathrm{BR(eff)}}$ falls to the static level equivalent to the supply voltage V_{DC}, and the drain to source current I_{DS} falls to zero. This value I_{AV} should stay under or equal to the max rated continuous drain current I_{D} of the device.

3.4 Measurements during an avalanche event

During the test, three quantities are measured with the help of an oscilloscope, as shown in Figure 9.

1. The first monitored parameter is the gate voltage V_{GS} (blue waveform) measured between the MOSFETs gate and source. When switching the device ON, the voltage between V_{GS} goes from -5 V to 20 V (interval 1) and then back to OFF state -5 V (interval 2 and 3).

2. The second monitored parameter is the drain to source voltage V_{DS} (red waveform). When the MOSFET changes the state from blocking to conducting, the drain to source voltage changes from V_{DD} to zero (interval 1). When the t_{ON} time has passed, and the device is switched-off, the voltage rises sharply above the breakdown voltage $V_{\mathrm{BR(DSS)}}$ for a t_{AV} time (interval 2). If the device survives the avalanche phase, the voltage reverts to the supply voltage V_{DC} level (interval 3).

3. The third and last monitored parameter is the drain-source current I_{DS} passing through the device (green waveform). The current increases linearly when the MOSFET is ON, and the maximum current I_{AV} is reached when the MOSFET is switched off (interval 1). The drain to source current I_{DS} decrease linearly back to zero (interval 2 and 3).

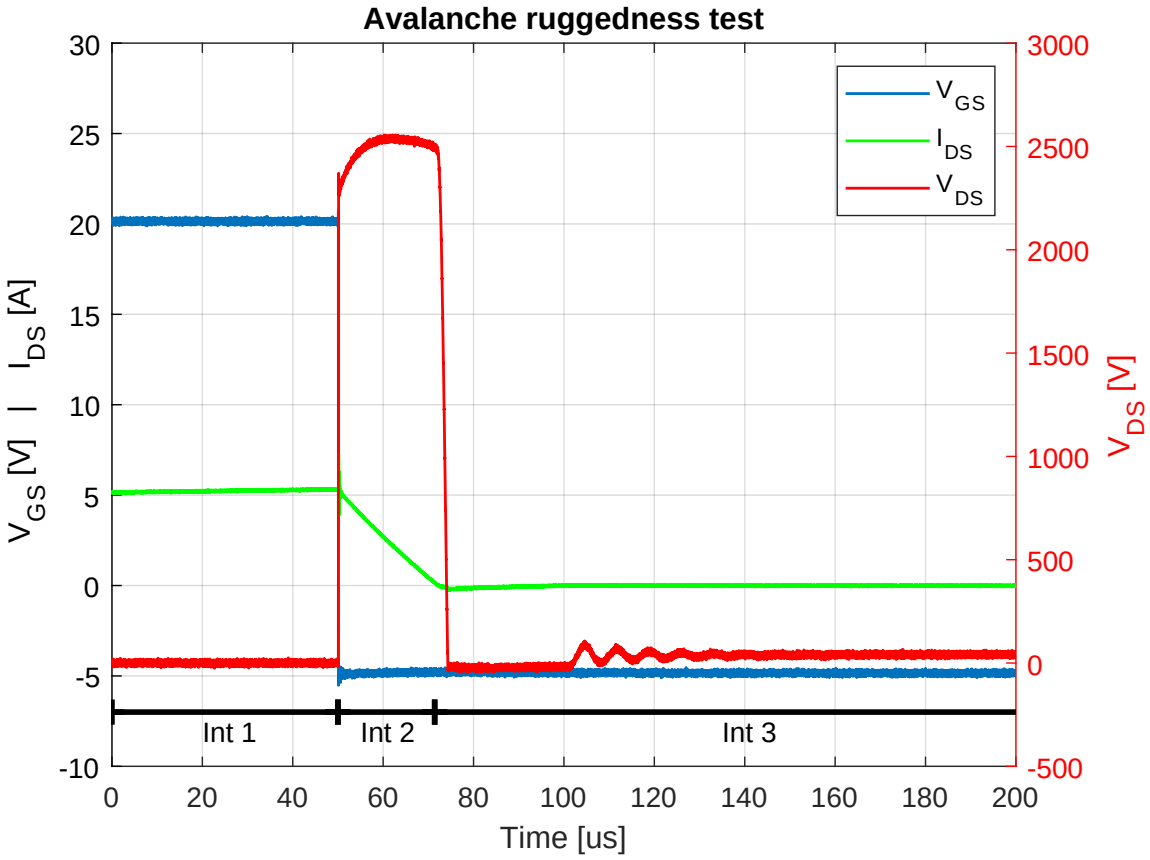

Figure 9: Waveforms of a SiC C2M1000170 MOSFET during avalanche. Drain to source voltage V_{DS} (red), drain to source current I_{DS} (green), and gate to source voltage V_{GS} (blue).

3.5 Test bench

The test bench designed and built for the purpose of studying the avalanche ruggedness phenomenon of power MOSFETs in this thesis is shown in Figure 10.

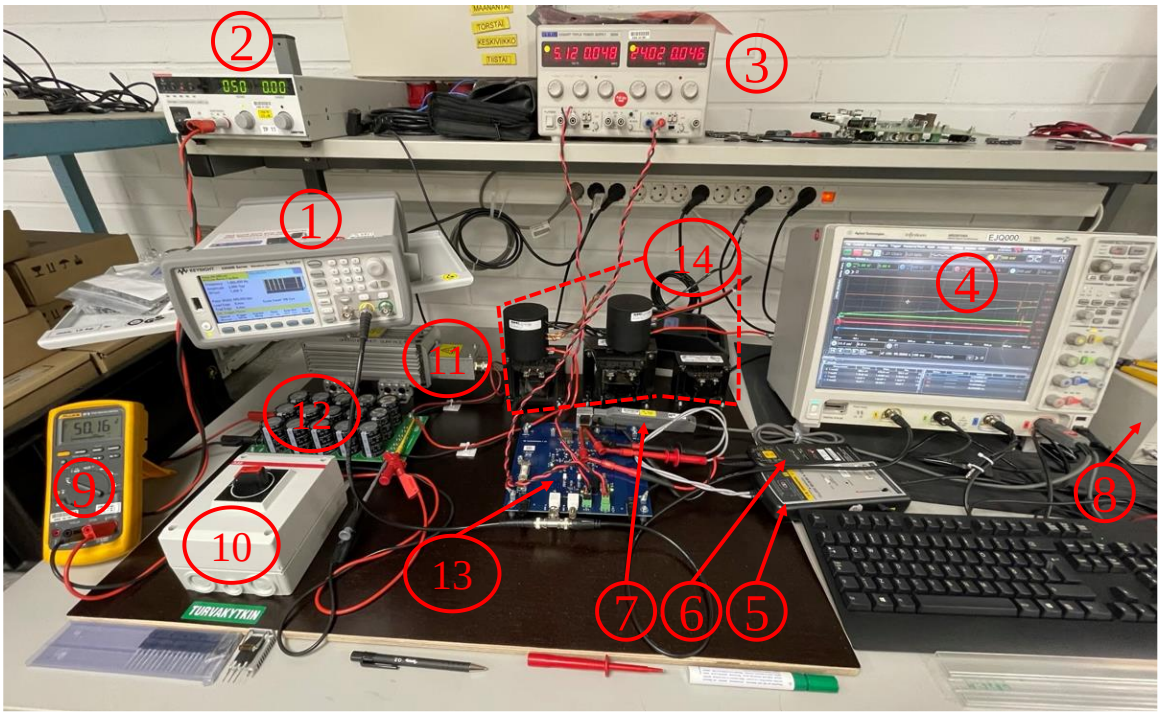

Figure 10: Test bench for investigation of avalanche ruggedness in SiC MOSFETs.

The test bench consists of several components and measurement devices which are all listed in Table 1. The waveform generator is used to control the gate drive of the MOSFET. The waveform generator allows control of the device conduction time and the repetition rate of the pulses. The DC power supply is used as the main power supply for the test and is connected in parallel with a capacitor bank. The capacitor bank's main task is to store electrical energy and to provide a stable flow of this energy to the device under test. The triple power supply generates the different voltage levels for the main electronics on the AR test board. The oscilloscope is used to display and capture the current and voltage waveforms with the help of current and voltage probes attached to various terminals of the device. The test bench is also equipped with a safety circuit. The safety circuit consists of a manual switch, and a discharge resistor arranged parallel with the capacitor bank. When the switch is closed, the capacitor bank is discharged through the discharge resistor. The multimeter is also a part of the safety circuit. The multimeter is used for the voltage measurement between the capacitor bank's potentials and indicates if the voltage has decreased.

Table 1: Equipment used for the AR test bench.

ID	Device	Brand	Model	Function
1	Waveform Generator	Keysight	33500B Series	Control the gate drive of the DUT
2	DC Power Supply	Sorensen	XHR 600-1.7	Main power supply for the test
3	Triple Power Supply	Aim-TTi	EX345RT	$5\,V$ and $24\,V$ for the main electronics
4	Mixed Signal Oscilloscope	Agilent	MSO9104A	Capture the waveforms during an AR event
5	Differential Probe	Yokogawa	701926	Measure the drain to source V_{DS} voltage
6	Differential Probe	Tektronix	P5200A	Measure the gate to source V_{GS} voltage
7	Current Probe	Yokogawa	701933	Measure the drain to source I_{DS} current
8	Power Supply	Yokogawa	701934	Power supply to the current probe
9	Multimeter	Fluke	87V TRMS	Measure the voltage across the capacitor bank
10	Safety Switch	ABB		Switch to discharge the capacitor bank
11	Discharge resistor			Resistor to discharge the capacitor bank
12	Capacitor bank	Self-design		Capacitor bank for AR tests
13	AR Test board	Self-design		Avalanche ruggedness test board
14	Inductors			Different size inductors used in the test

The test board designed to examine the AR of the SiC MOSFETs is shown in Figure 11. The test board is designed to test the TO-247-3 and TO-247-4 package devices. The primary voltages are derived on the edges of the PCB, and the gate driver circuit and its auxiliary voltages are found in the center of the PCB. A more detailed block diagram of the AR test bench can be found in the Appendix 1.

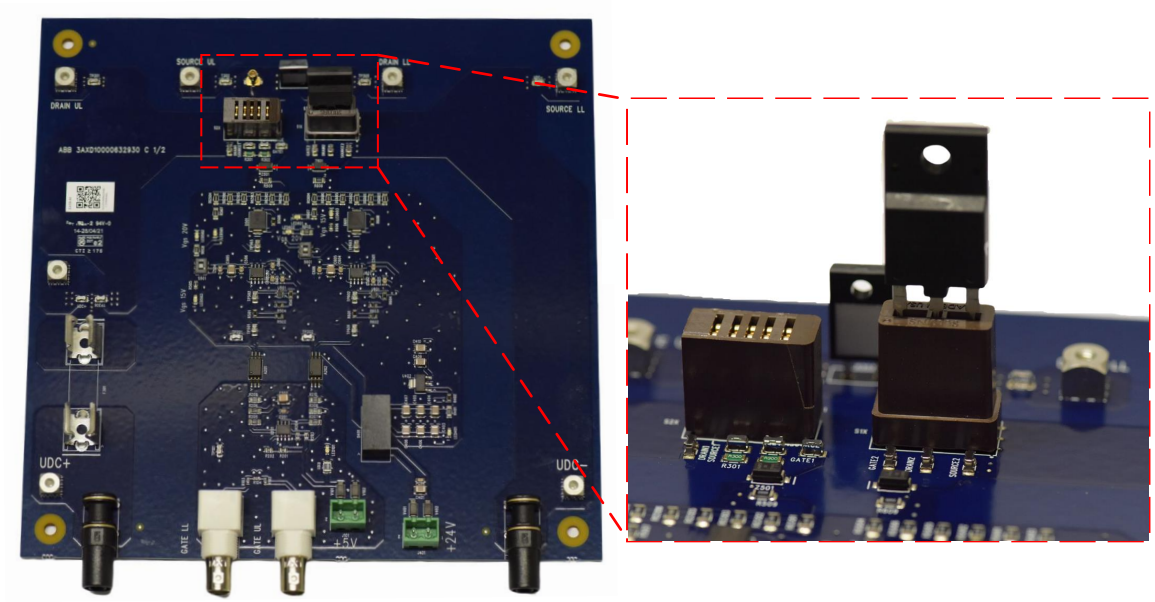

Figure 11: The designed test bench with the gate driver circuit for investigation of avalanche ruggedness in SiC MOSFETs.

4 Avalanche ruggedness test procedure

This chapter describes the implemented avalanche ruggedness test procedure for SiC MOSFETs. The measurement equipment used to investigate the aging effect on the devices, as well as how to set the aging parameters for the DUTs, is also described.

4.1 Implemented test procedure

Figure 12 illustrates the test procedure implemented to investigate the avalanche ruggedness of SiC MOSFETs. The test procedure consists of four main steps: X-ray image of the DUTs, Scanning Acoustic Microscopy (SAM) of the DUTs, electrical characterization of the DUTs, and the AR test for the DUTs.

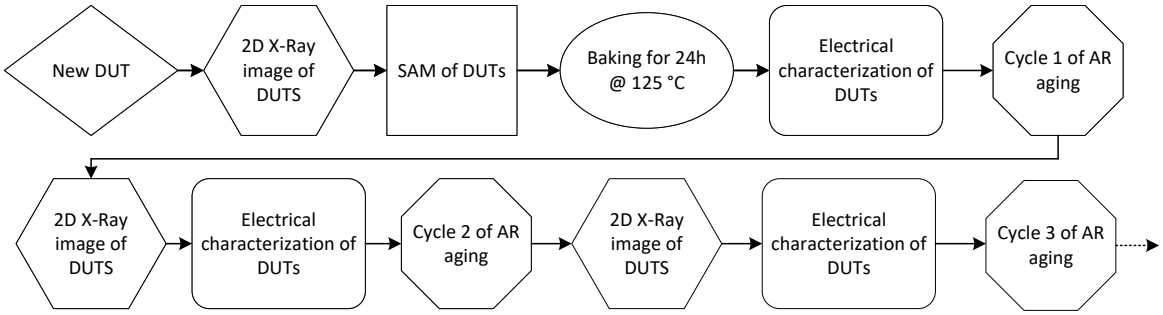

Figure 12: Implemented test procedure for investigation of the avalanche ruggedness of SiC MOSFETs.

Before the first cycle of the AR test, the initial conditions of the DUTs needs to be determined. The determination of the initial condition of the DUTs is performed by the imaging and electrical characterization of the DUTs, as shown in Figure 12. The first step of the characterization for the DUTs is done with a 2D X-ray machine. An example of an X-ray image of a SiC MOSFET chip is shown in Figure 13.

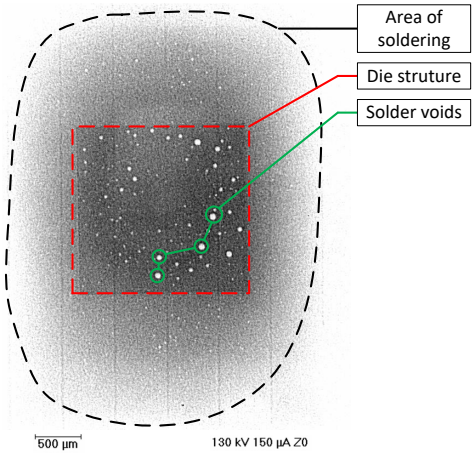

Figure 13: X-ray image of a C2M1000170D SiC MOSFET.

The X-ray image is taken from the top side of the DUT. The X-ray image is used to evaluate the soldering area, the die structure, and solder voids in the structure, as shown in Figure 13. The bond wires between the chip and the leeds absorb too few X-rays to create noticeable contrast, and they can not be observed in the X-ray image.

In the second step, the DUTs are imagined using a SAM. The SAM image of the DUT can efficiently reveal physical defects such as cracks, voids, and delamination in between the different attached layers. The SAM images of the DUTs are taken before the first cycle of the AR test and after the breakdown of the DUT. Figure 14 shows a SAM image of three layers: System solder of die-attach, chip die structure, and bond wire attached to the top of the chip die.

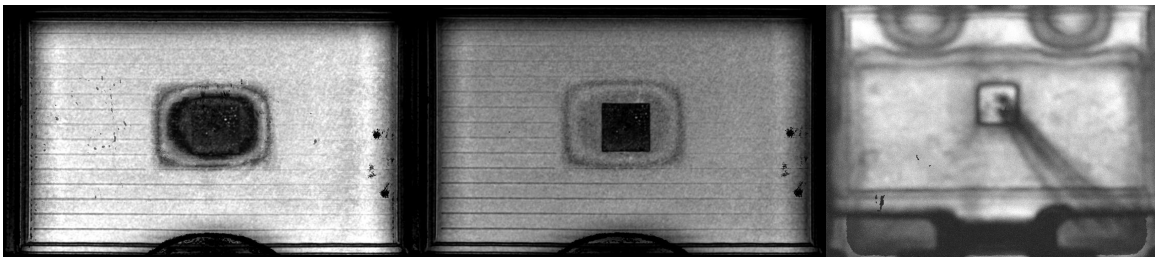

Figure 14: SAM images of a C2M1000170D SiC MOSFET. From left to right: System solder of die-attach, chip die structure, and bond wires attached to the top of the chip die.

The third and last step of the initial condition characterization is the electrical characterization of the DUTs. Before the electrical characterization can be performed, the DUTs are baked for 24 hours in a thermal chamber at 125 degrees Celsius accor-

ing to JEDEC standard 22-A113D, to drive out any leftover moisture from the SAM process from the samples before any electrical stress is applied to the DUTs. The electrical characterization is performed with a power device analyzer. This device allows the measurement of five key electrical characteristic measurements to reveal potential degradation of the DUT. The electrical characterization measurements are as follows: Output characteristics I_{D}-V_{DS}, transfer characteristics I_{D}-V_{GS}, forward characteristics of the body diode I_{S}-I_{SD}, drain-source leakage current I_{DSS}, and the gate-source leakage current I_{GSS}. The five electrical characterizations measurements are shown in Figure 15.

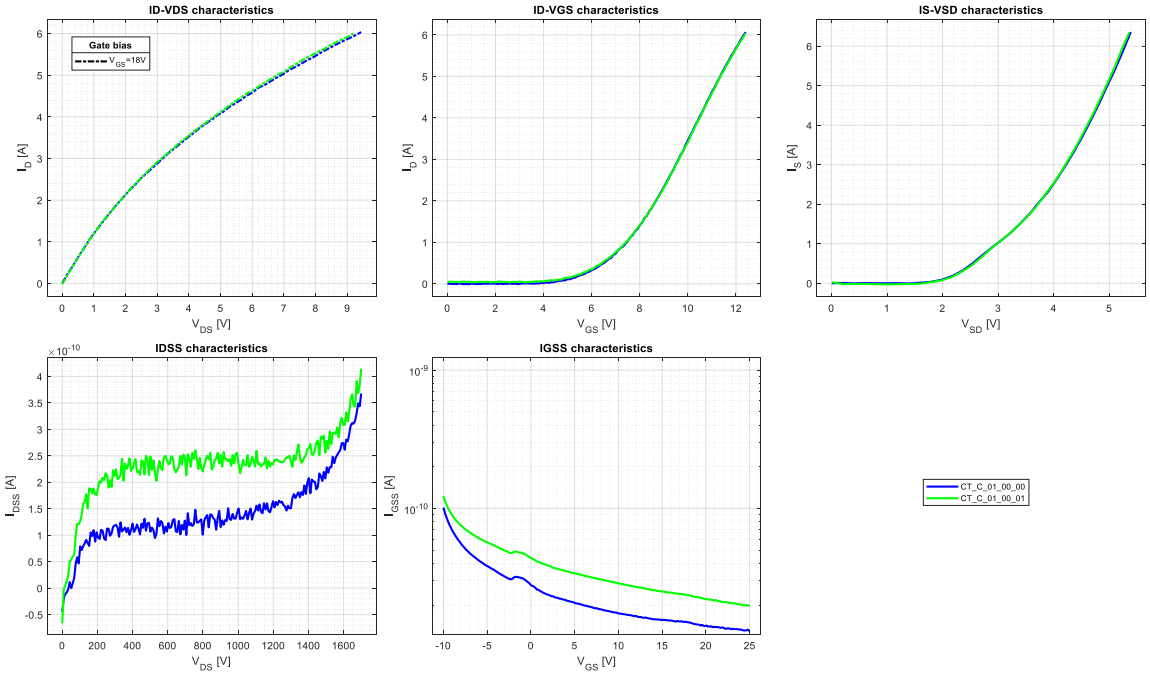

Figure 15: Five electrical characterization measurements were performed with a Keysight power device analyzer model B1506A. The blue-colored lines are measurements performed before any AR test, and the green-colored lines are measurements performed after 100 aging pulses of AR for the same DUT.

The imaging and electrical characterization devices used in the test procedure are listed in Table 2.

Table 2: Measurement equipment used for investigation of the aging effect in SiC MOSFETs.

Device	**Brand**	**Model**
X-ray Machine	General Electric	Nanomex 180 DXR
Scanning Acoustic Microscope	Sonoscan	GEN6 C-SAM Acoustic Microscope
Thermal Chamber	Espec	SH-642
Power Device Analyzer	Keysight	B1506A

4.2 Setting the aging parameter values

For the AR test performed in this thesis, one device from each supplier was selected to find the End-of-Life (EoL) avalanche energy. For each supplier, the maximum dissipated avalanche energy for the device was discovered by increasing the t_{ON} while the V_{DC} for the test was held constant. The t_{ON} was increased with 100 μs steps until avalanche failure of the device was reached. Two avalanche pulses with a repetition rate of 1 Hz were given for each step. Once the failure occurred, the parameters used prior to the device's destruction were considered the avalanche energy the device could withstand. These parameter values were then used for the aging of the DUTs selected for the AR tests. Figure 16 shows the procedure to find the aging parameter values for Cree C2M1000170 SiC MOSFET.

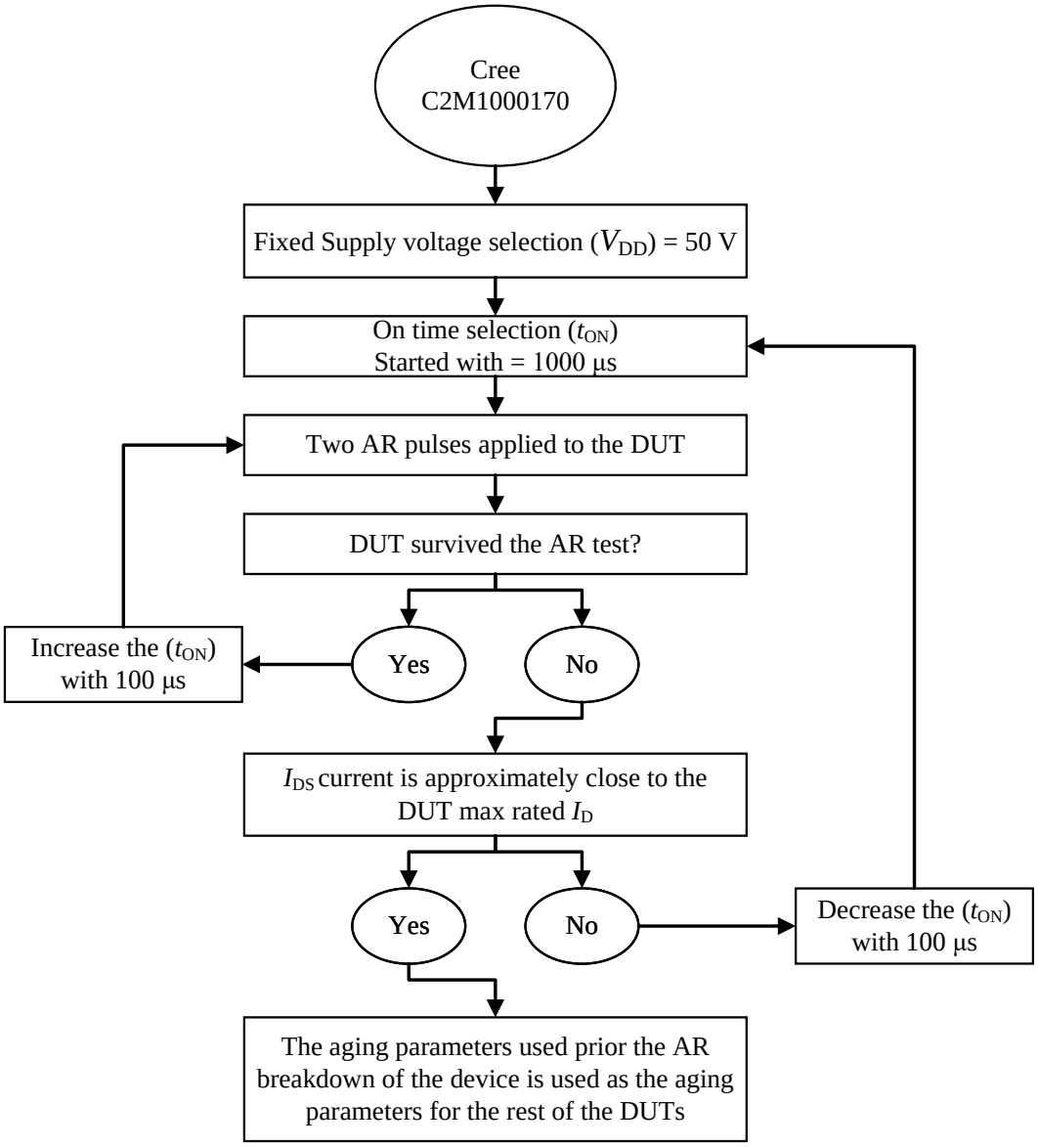

Figure 16: The method to find the aging parameter values for Cree C2M1000170 SiC MOSFET

5 Analysis and results

The analysis and results of the AR test conducted on two TO-247-3 packaged SiC power MOSFET suppliers is presented in this chapter. Both suppliers' devices benchmarked are 1700V rated SiC planar MOSFETs. For the respective supplier, ten DUTs were selected for AR testing. The datasheet values for the devices of each supplier are presented in the Table 3.

Table 3: Datasheet values for the tested DUTs. (Cree, 2021; ROHM, 2017)

Supplier	Cree	Rohm
Part Number	C2M1000170D	SCT2H12NZ
Generation	2nd Gen	2nd Gen
V_{DS} (V)	1700	1700
I_{D} (A)	5	3.7
T_{jmax} $(^{\circ}C)$	150	175
$R_{\mathrm{DS(on)}}$ (Ω)	1	1.15

5.1 Cree C2M1000170

As described at the end of Section 4, the maximum dissipated avalanche energy for the Cree C2M1000170 devices was obtained using the parameters listed in Table 4.

Table 4: Values used to set the aging parameters for the Cree C2M1000170 devices.

Cree C2M1000170					
Measurement identification number (ID)	001	002	003	004	005
Supply voltage V_{DC}	50	50	50	50	50
t_{ON} time (μs)	1000	1100	1200	1300	1400
Avalanche energy (mJ)	86.7	102.9	119.7	137.2	-
Survived the AR test (PASS/FAIL)	PASS	PASS	PASS	PASS	FAIL

The DUT failed with parameter values: $V_{\mathrm{DC}} = 50\,V$, and $t_{\mathrm{ON}} = 1400$ μs. The last recorded step before avalanche breakdown of the DUT was with the following parameter values: $V_{\mathrm{DC}} = 50\,V$ and $t_{\mathrm{ON}} = 1300$ μs, which using Equation 15, corresponds to the avalanche energy of $E_{\mathrm{AV}} = 137$ mJ. Figure 17 shows the waveforms with these parameter values.

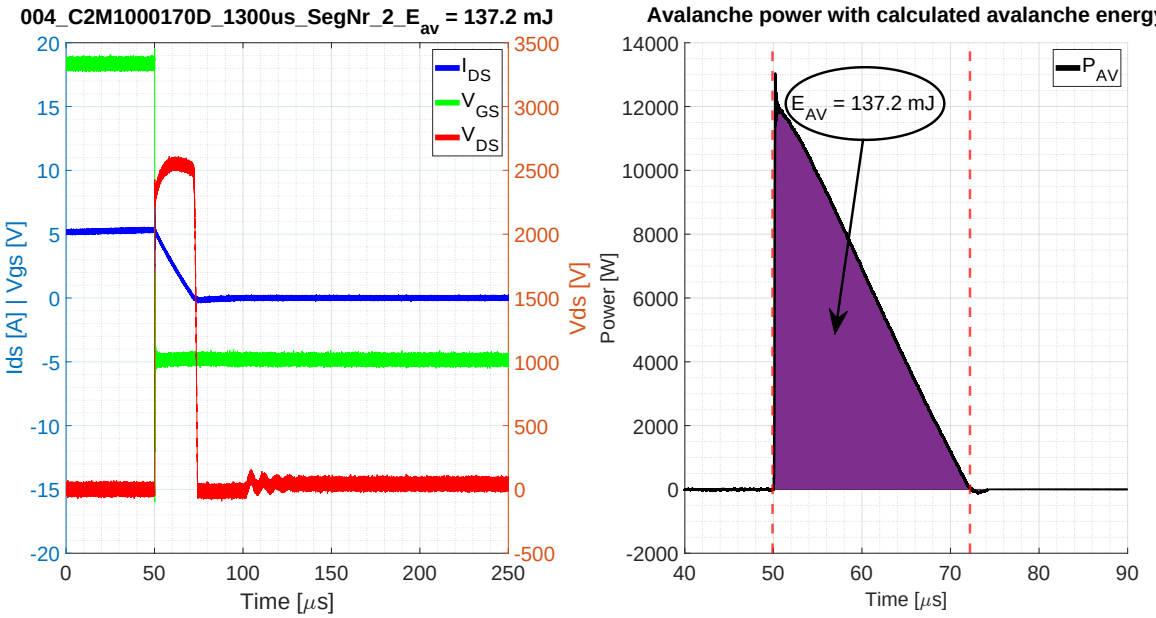

Figure 17: On the left-hand side is the last recorded AR pulse for the Cree C2M1000170 SiC MOSFET, and on the right-hand side, the avalanche power with calculated avalanche energy.

For the ten Cree C2M1000170 samples selected for the AR test, the final aging parameters used were with $V_{\mathrm{DC}} = 50\,V$ and $t_{\mathrm{ON}} = 1200\ \mu$s, corresponding to an avalanche energy of ∼120 mJ. Before the AR test with the final aging parameters were applied to the ten selected DUTs, it was decided to do a pre-conditioning test for all ten DUTs. This was done to ensure all devices were functional and to disclose any early failures of the DUTs. The pre-conditioning test were performed with $V_{\mathrm{DC}} = 50\,V$ and $t_{\mathrm{ON}} = 1100\ \mu$s corresponding to $E_{\mathrm{AV}} = 102.9$ mJ per pulse. The same repetition rate of 1 Hz was used for the pre-conditioning stage. All ten DUTs survived the pre-aging stage, and no device breakdown did occur. After the AR pre-conditioning, the electrical re-characterization for the DUTs was made.

The electrical characterization measurement results revealed that after the first 100 AR pre-conditioning pulses, the drain to source leakage current I_{DSS} increased approximately twice in value for the measurement range of $V_{\mathrm{DS}} = 250\,V$ to $800\,V$ compared to the I_{DSS} characterization measurement performed before the AR test. An increase in the gate to source leakage current I_{GSS} is seen for the full measurement range. No significant changes were seen in the rest of the electrical characterization measurements (I_{D}-V_{DS}, I_{D}-V_{GS}, and I_{S}-V_{SD}). Figure 18 shows the electrical characterization measure-

ment results for the ten DUTs. The blue line shows the measurement performed before the pre-conditioning test, and the green line indicates the measurement performed after the first 100 AR pre-conditioning pulses where the E_{AV} was $\approx$ 100 mJ per pulse.

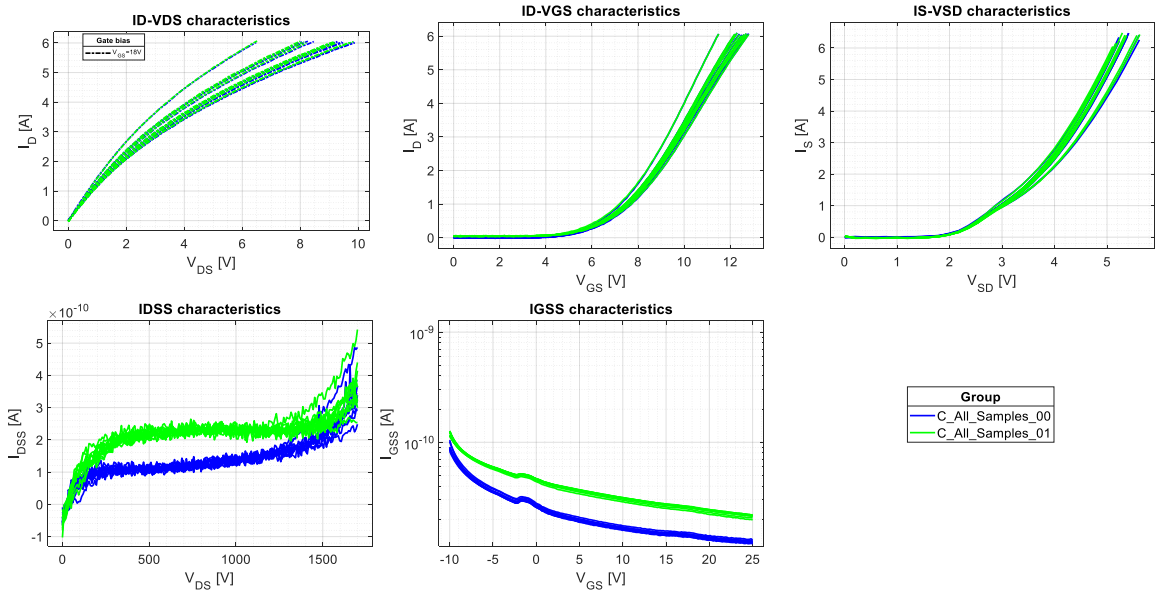

Figure 18: Electrical characterization measurement results before and after the 100 aging pulses. The E_{AV} was $\approx$ 100 mJ per pulse. Green-colored lines are before any AR aging pulses, and the blue-colored lines are after 100 AR aging pulses were applied to the DUTs.

After the electrical characterization, the 2D-Xray inspection of the ten Cree DUTs was performed. From the X-ray images, no changes in the construction could be observed after the 100 aging pulses. Figure 19 shows one X-ray image taken from the top side of the DUT.

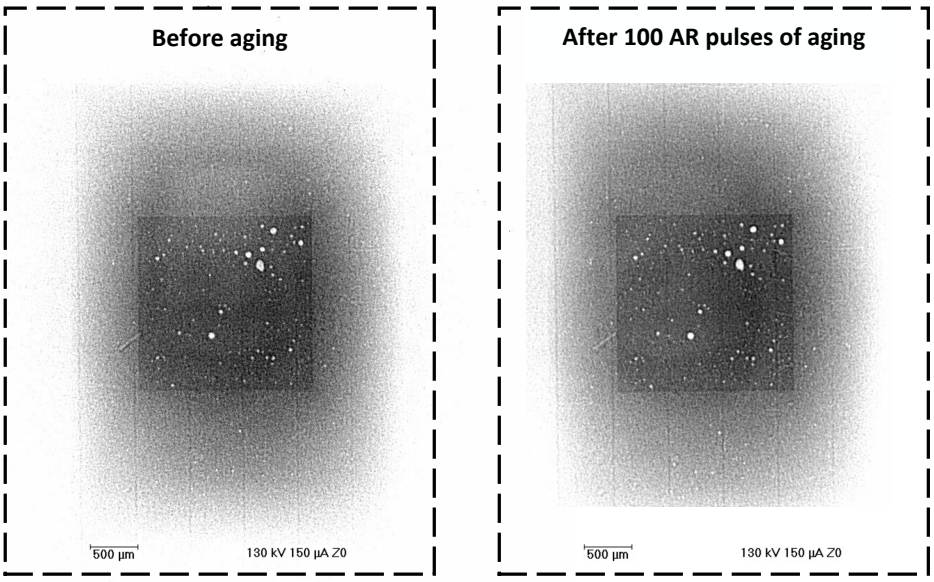

Figure 19: Cree C2M1000170 - DUT1 2D X-ray images after 100 aging pulses.

After the pre-conditioning stage, the AR test was continued with the aging parameters of $V_{\mathrm{DC}} = 50\,V$ and $t_{\mathrm{ON}} = 1200\ \mu$s, corresponding to the E_{AV} of ≈ 120 mJ. The total amount of survived aging pulses for all ten DUTs from Cree is shown in Figure 20. The figure shows that the DUTs from Cree have a notable variance in the robustness against AR aging pulses, where some of the DUTs survive 100, and some DUTs survive several thousand AR aging pulses. From the figure, three distinct groups can clearly be seen, indicating that the devices failed into three different types of failures.

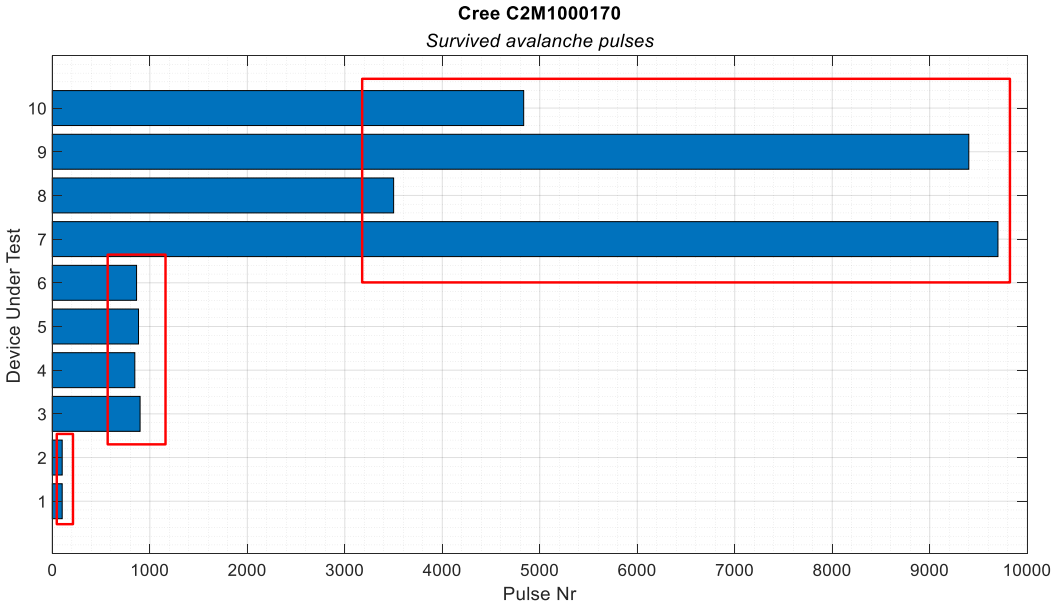

Figure 20: Total survived AR aging pulses for each DUT from Cree.

As seen in Figure 20, the first avalanche failures occurred for the DUTs with the identifier (ID) 1 and 2. Both devices failed on the first AR pulse of the first iteration and survived for a total of 100 pre-conditioning pulses. Figure 21 shows the oscilloscope waveforms during failure for DUT1, and Figure 22 for DUT2.

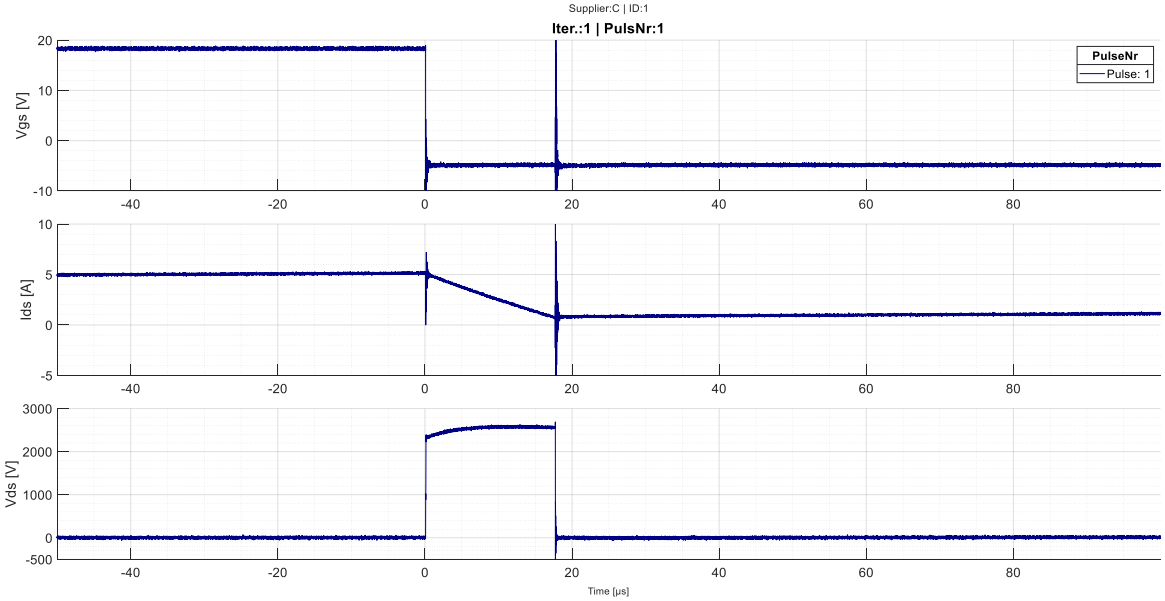

Figure 21: Oscilloscope waveforms of the failed Cree DUT1. From top to bottom: V_{GS}, I_{DS}, and V_{DS}.

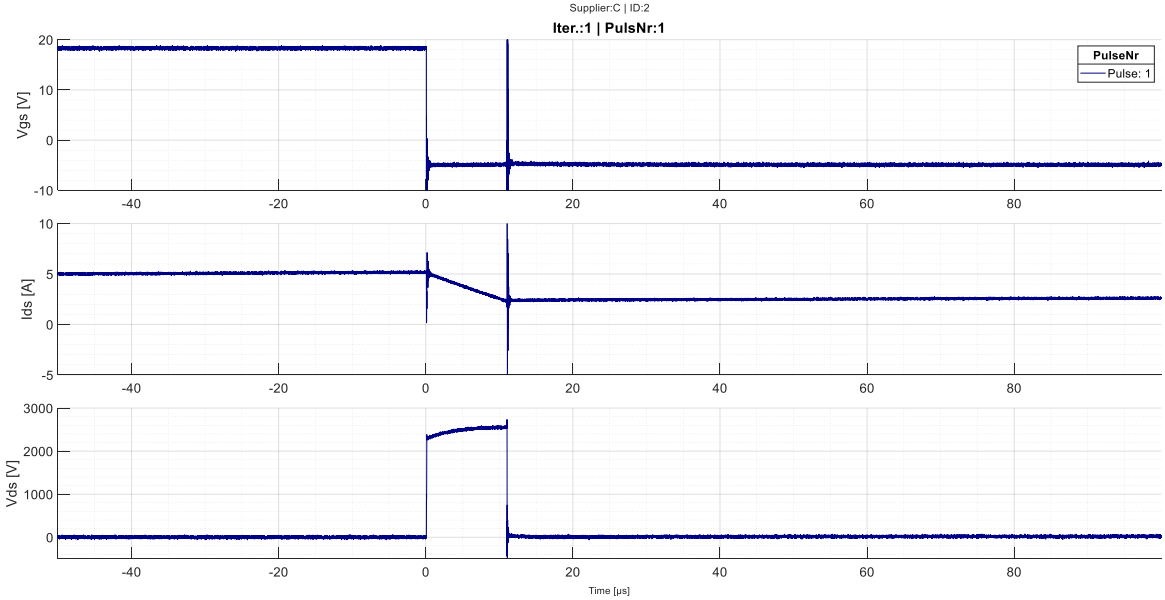

Figure 22: Oscilloscope waveforms of the failed Cree DUT2. From top to bottom: V_{GS}, I_{DS}, and V_{DS}.

From Figures 21 and 22, it is seen that both DUT1 and DUT2 have almost a similar breakdown phenomenon. For the DUT1, the drain to source current I_{DS} goes from $\sim 5.1\ A$ down to $\sim 0.7\ A$ until the failure occurs. The avalanche time t_{AV} before breakdown is $\approx 17.7\ \mu$s. When the DUT fails ($t_{\mathrm{AV}} \approx 17.7\ \mu$s), the I_{DS} current is not extinguished and does not reach zero as it should. Furthermore, a fluctuation in the V_{GS} voltage is seen even if the V_{GS} applied to the device is -5 V. From the V_{DS} waveform it is seen that the effective avalanche breakdown voltage $V_{(\mathrm{BR})\mathrm{eff}}$ stays at $\approx$ 2600 V for the time before the breakdown (t_{AV} 0 to 17.7 μs). When the failure occurs at $t_{\mathrm{AV}} = 17.7\ \mu$s, the $V_{(\mathrm{BR})\mathrm{eff}}$ rises to 2700 V and drops down to the input voltage level V_{DC} of 50 V.

The DUT2 behaves almost identical to the DUT1. The difference between the DUT2 compared to the DUT1 is that the avalanche time before device breakdown is shorter, $t_{\mathrm{AV}} = 11\ \mu$s. The device breakdown occurs at $\sim 2.3\ A$. The V_{GS} and V_{DS} profiles behave similarly for the DUT2 as for the DUT1. The resistance measured between the different terminals for both DUTs are almost identical as seen in Table 5.

Table 5: Resistances between the different terminals after the avalanche breakdown.

	Cree C2M1000170	
Measurement	DUT1	DUT2
Gate-source resistance (Ω)	229.2	224.5
Gate-drain resistance (Ω)	251.2	235.6
Drain-source resistance (Ω)	22.8	11.5

The 2D X-ray images of DUTs 1 and 2 do not show differences in the chip structure compared to the X-ray image taken before the AR testing. Figure 23 shows X-ray images taken before and after the avalanche breakdown of the DUT1. The red circle in the picture on the right-hand side shows a mechanical scratch from the fastening of the DUT to the heatsink.

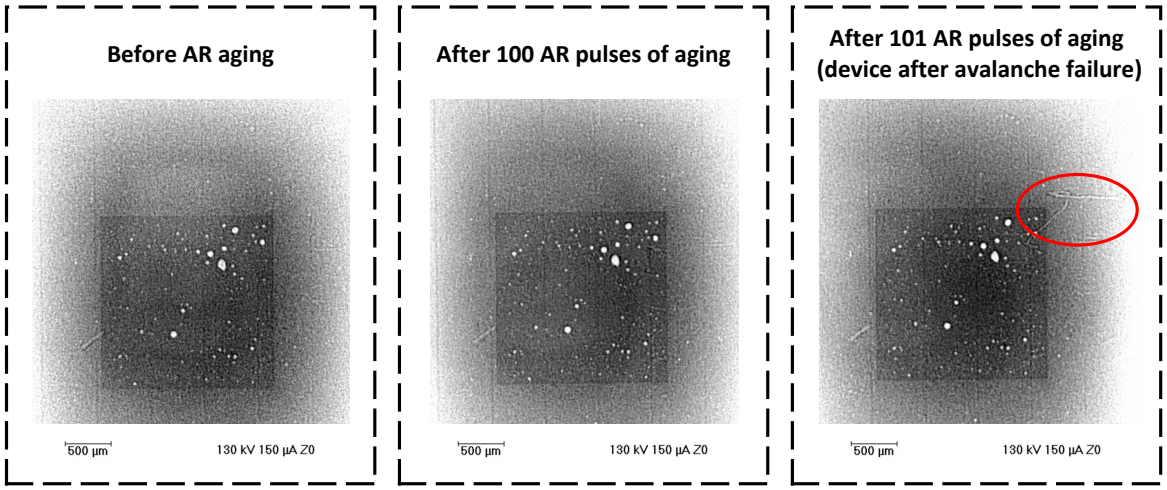

Figure 23: Cree C2M1000170 - DUT1 2D X-ray images. From left to right: X-ray image before any aging. X-ray image after the pre-conditioning stage and X-ray image after the avalanche breakdown.

After the X-ray examination, a SAM analysis of the DUTs was made. For the DUTs from Cree, the SAM images were taken from the top and bottom sides of the devices. Figure 24 shows the SAM images taken of the DUT1. The image on the upper left-hand side is a SAM image of the die-attach layer from the bottom side of the device, whereas the image below is from the top side of the device and shows the bond wires attached to the top of the chip. Both images are taken before any AR aging. The SAM images on the right-hand side are taken after the avalanche breakdown of the DUT1. From the upper image, any variance is not noticed in the SAM image, and it can be stated that for this DUT1, the AR has not affected the die-attach layer. From the bottom SAM image, a possible failure location on the chip can be detected, and the location is marked with red arrows. The removal of the mold compound reveals the failure location on the chip and is shown in Figure 25.

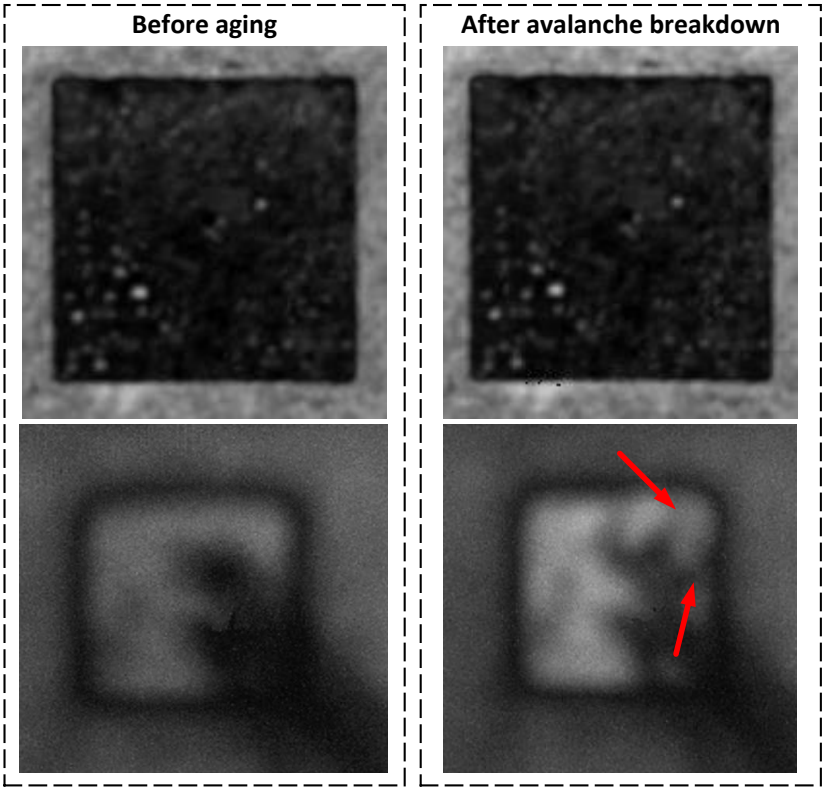

Figure 24: Figure 24 Cree C2M1000170 - DUT1 SAM images. On the left-hand side is the image taken before aging and on the right-hand side is the image taken after the avalanche breakdown. The red arrows indicate a possible failure location.

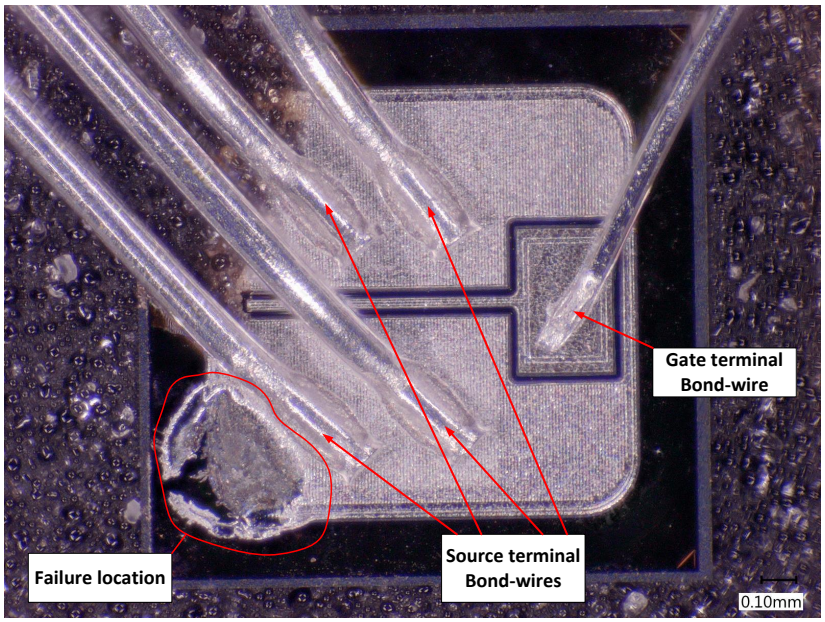

Figure 25: Failure location of the Cree DUT1 after the avalanche breakdown.

Regarding the second failure group identified in Figure 26, all four DUTs 3-6 sur-

vived for ≈ 900 aging pulses. The figure shows a scatter plot of I_{DSS} characterization measurement completed after every 100 AR aging pulses applied to the DUTs. The figure reveals that DUT3, DUT4, and DUT6 behave similarly. The I_{DSS} begins to increase before the failure of these DUTs occurs. For the DUT5, any significant change in the I_{GSS} is not seen before the breakdown of the device. The I_{GSS} characterization measurement was also performed for the DUTs and is shown in Figure 27. The figure shows that the I_{GSS} rises after the first 100 AR aging pulses but does not increase significantly for any of the pulses given to the DUTs after that. The DUT3 did not degrade completely after the 900 AR aging pulses, and it was possible to electrically re-characteristics. The DUT4 to 6 failed in the AR test, and they were not possible to be electrically re-characteristic. The I_{GSS} for DUT3 after 900 AR aging pulses was greater than 100 μA, which was set as the maximum limit for I_{GSS} measurement, and this DUT was chosen for further investigation.

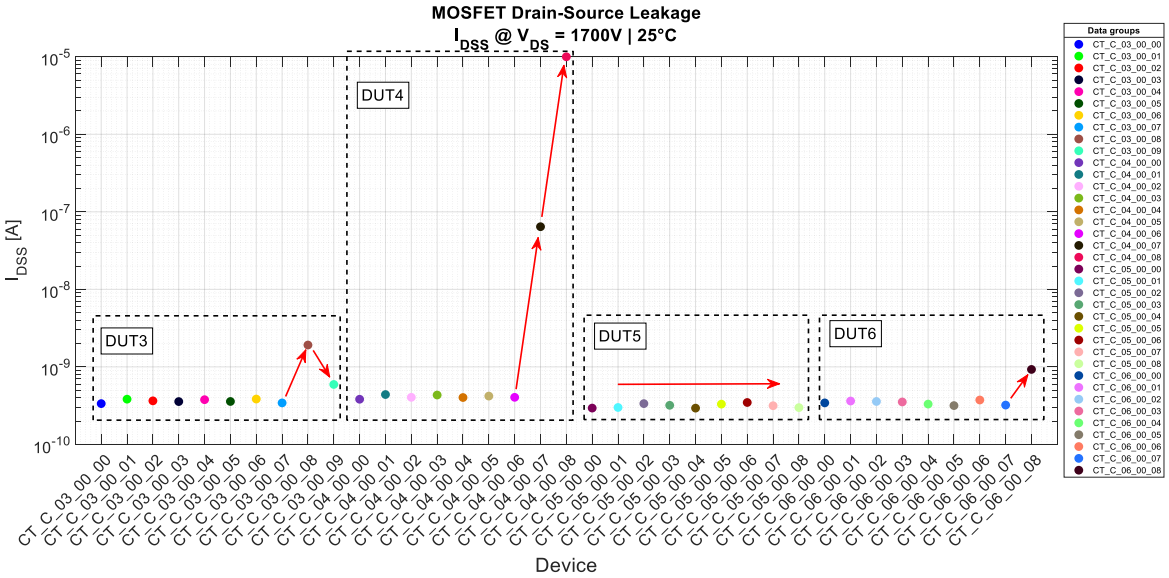

Figure 26: Drain to source leakage current plot for DUTs 3 to 6. The I_{DSS} measurement was performed after every 100 AR aging pulses. The 00 data point is before any aging pulses, and for example, the 05 data point is after 500 AR aging pulses. The I_{DSS} value is taken at $V_{DS} = 1700\ V$.

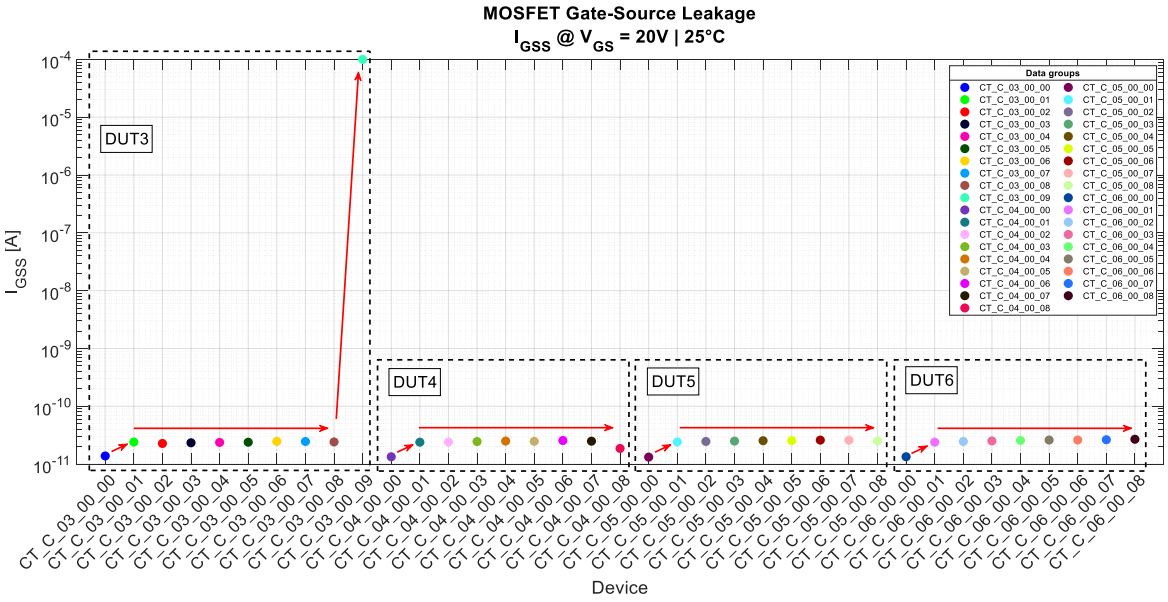

Figure 27: Drain to source leakage current plot for DUTs 3 to 6. The I_{GSS} measurement was performed after every 100 AR aging pulses. The 00 data point is before any aging pulses, and for example, the 05 data point is after 500 aging pulses. The I_{GSS} value is taken at $V_{\mathrm{GS}} = 20\ V$.

The oscilloscope measurements during the AR test did not reveal any significant difference for the DUTs 4-6. The t_{AV} varies for the DUTs as well as the number of pulses before the failure occurs. However, any notable difference in the voltage and current waveforms is not seen. Figure 28 shows the pulse where the avalanche breakdown occurs for the DUTs. This figure shows that the breakdown behaviour for these DUTs is similar to those of DUT1 and 2. The I_{DS} current is not extinguished and does not reach zero as it should. Furthermore, a fluctuation in the V_{GS} voltage is seen even if the V_{GS} applied to the device is -5 V.

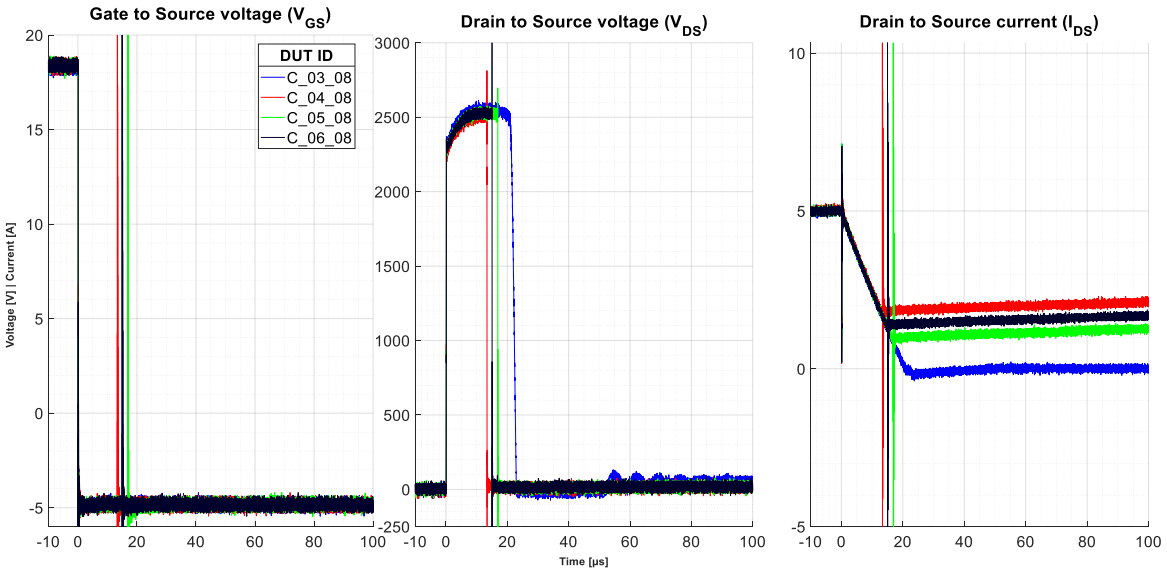

Figure 28: Oscilloscope waveforms of the failed Cree DUT3-6. From left to right: V_{GS}, V_{DS}, and I_{DS}. Blue colored lines are the waveforms for DUT3, red for DUT4, green for DUT5 and black for DUT6.

The X-ray investigation of the DUTs 3-6 did not reveal any abnormalities. Figure 29 shows X-ray images taken from the top side of the DUT5. Any notable change in the structure nor in the voids can be observed.

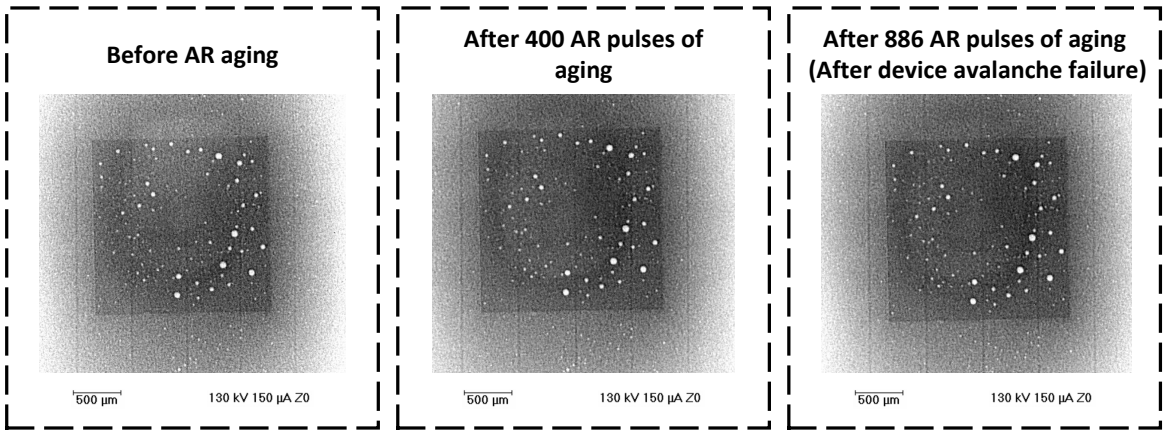

Figure 29: 2D X-ray image of the DUT5.

The SAM analysis of the DUT5 revealed similar results as the DUT1, although the DUT5 survived for almost ~ 8 times more AR aging pulses. The SAM images of DUT5 are shown in Figure 30, and from the image, it can be stated that the AR aging pulses do not affect the die-attach layer even if the number of aging pulses increases. The SAM image taken from the top side of the DUT5 shows a possible failure location close to

one of the source bond wires and is marked with a red arrow. The mold compound was removed from the DUT5, and the failure location of the DUT5 is shown in Figure 31. The failure location for the DUT5 is clearly in the device's active area and is most likely a different failure mode than for the DUT1. Furthermore, one of the four source bond wires has been cut off close to the end termination of the wire. However, it is noted that this could result from the mold compound removal process and needs further investigation.

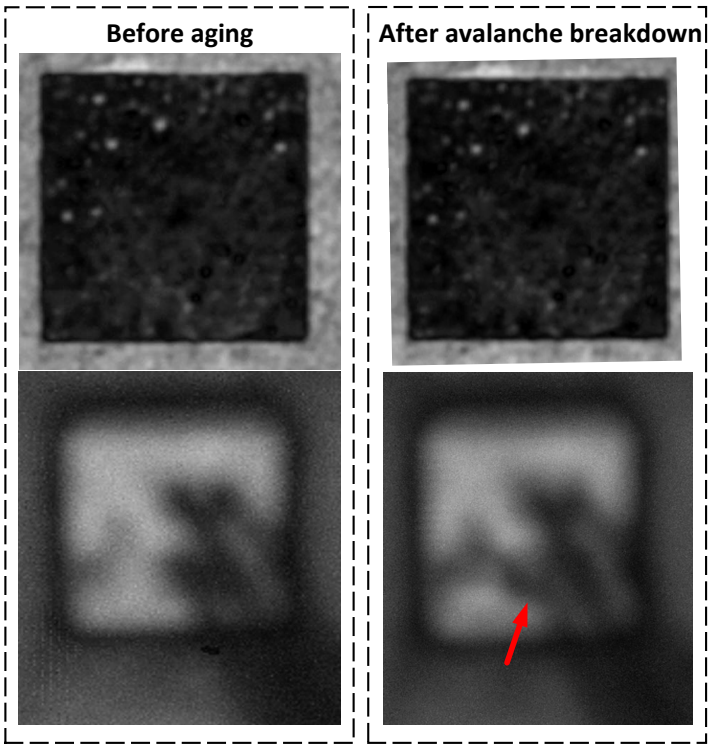

Figure 30: Cree C2M1000170 – DUT5 SAM images. On the left-hand side is the image taken before aging and on the right-hand side is the image taken after the avalanche breakdown. The red arrows indicate a possible failure location.

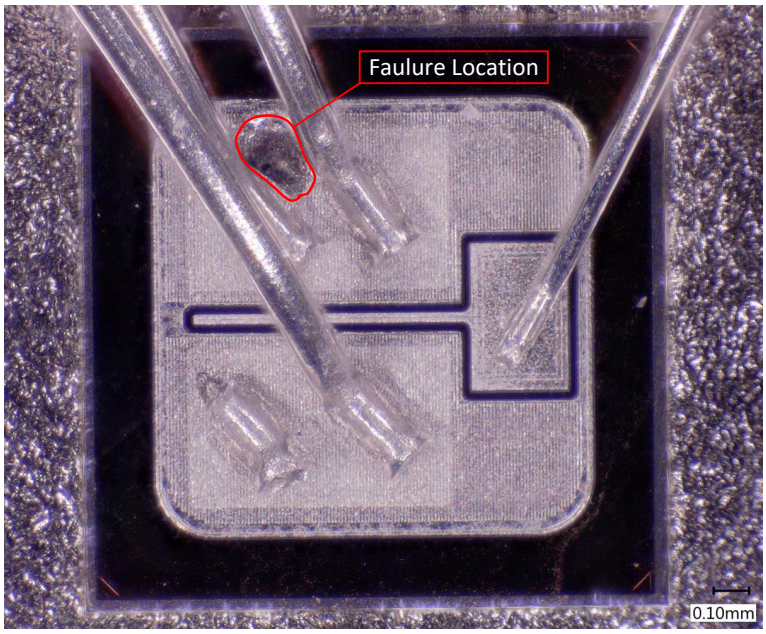

Figure 31: Failure location of the Cree DUT5 after the avalanche breakdown.

The subsequent AR breakdown occurred for DUT7, DUT8, DUT9, and DUT10. All four DUTs survived for several thousand AR aging pulses.

The electrical characteristics performed after every aging iteration reveals interesting behavior in the I_{DSS} and I_{GSS} measurements carried from the DUTs. The I_{DSS} results for DUTs 7 to 10 are shown in Figure 32 and the I_{GSS} in Figure 33. From the I_{DSS} figure, it can be noticed that all four DUTs behave similarly. The I_{DSS} stays at almost the same level for the first thousand AR aging pulses, after which the I_{DSS} starts to rise. The I_{GSS} also behaves identically to the previously analyzed DUTs 1-6. The I_{GSS} increases after the pre-conditioning stage, whereafter the I_{GSS} stays at the same level for approximately one thousand AR aging pulses, after which the I_{GSS} starts to decline. The I_{GSS} descends for about $\sim$ 400 pulses before the I_{GSS} rapidly increases above the 250 μA, which was set as the maximum limit for I_{GSS} measurement. Furthermore, the relation between the I_{DSS} and the I_{GSS} is clearly noticed when comparing Figures 32 and 33. When the I_{DSS} starts to increase, the I_{GSS} starts to decrease.

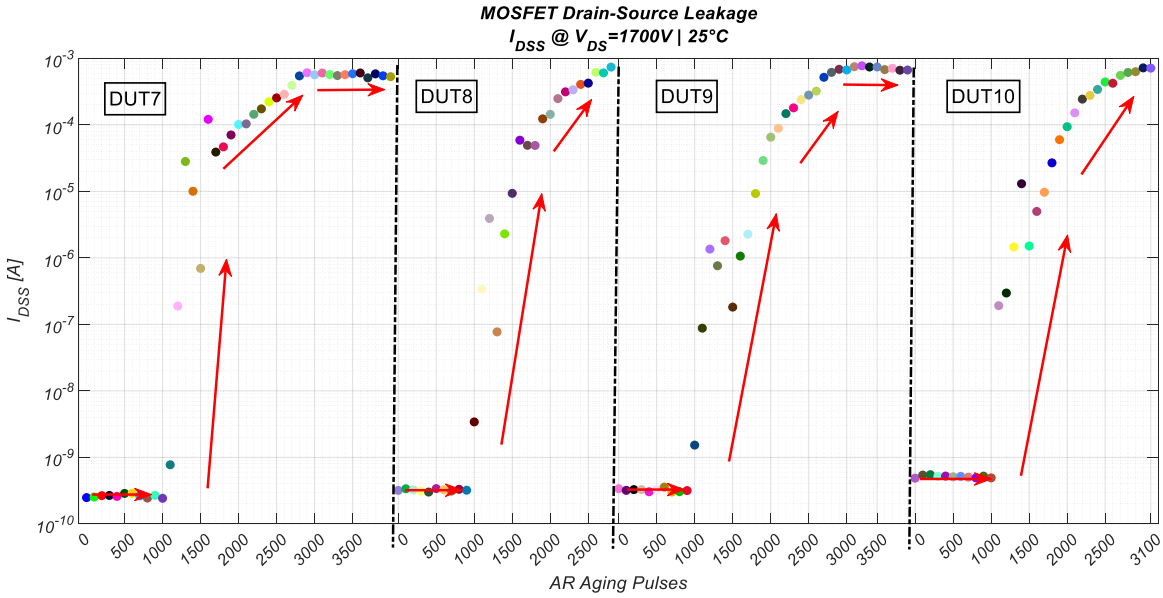

Figure 32: Drain to source leakage current plot for DUTs 7-10. The I_{DSS} measurement was performed after every 100 AR aging pulses. The I_{DSS} value is taken at $V_{\mathrm{DS}} = 1700$ V.

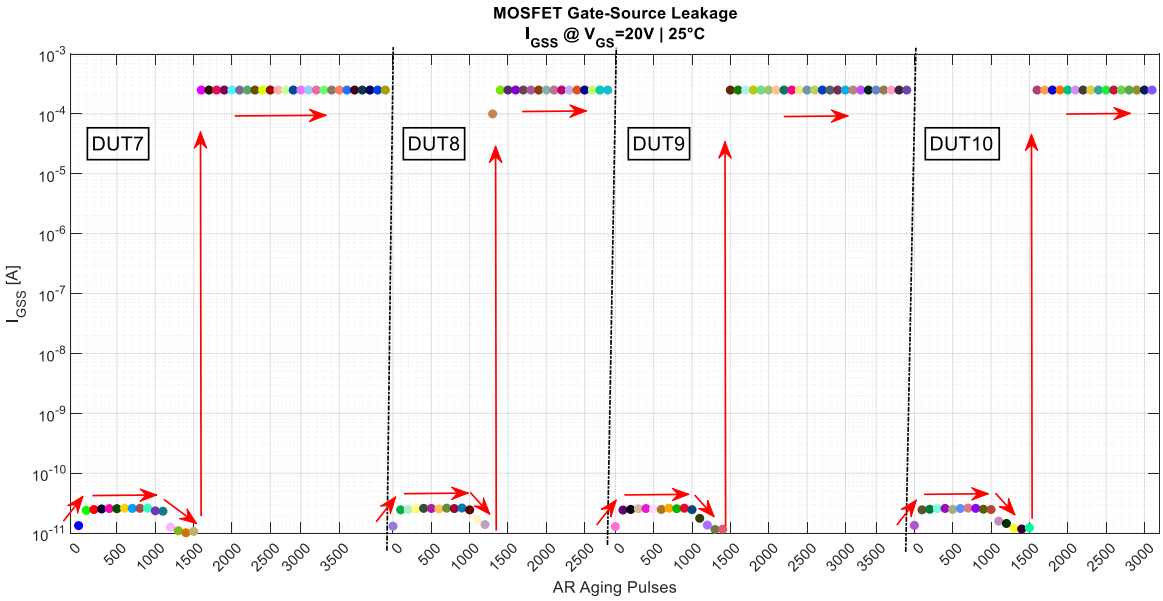

Figure 33: Gate to source leakage current plot for DUTs 7-10. The I_{GSS} measurement was performed after every 100 aging pulses. The I_{GSS} value is taken at $V_{\mathrm{GS}} = 20$ V.

The oscilloscope measurements during the AR test did show some differences for the DUTs 7 to 10 compared to the DUTs 1 to 6. The most notable difference for these DUTs that survived for several thousand AR aging pulses is that the V_{GS} declined as more AR aging pulses were applied to the DUTs.

Figure 33 shows that when the I_{GSS} starts to leak 250 μA at 1600 AR aging pulses for the DUT10, the impact is also seen in the AR tests. Figure 34 shows the oscilloscope waveforms during the AR tests to the DUT10. This figure shows every 100 AR aging pulse applied to the device. The blue-colored line is when 300 AR aging pulses are applied, and the green-colored line is when 1600 AR aging pulses were applied to the DUT. Any notable difference in the oscilloscope waveforms between the 300 to 1600 AR pulses is not seen, whereas when the device's gate starts to leak over 250 μA, the V_{GS} during the AR test starts to decline. When further AR aging pulses are applied to the DUT, the V_{GS} decline until the device breakdown occurs at $\sim$ 4800 AR aging pulses.

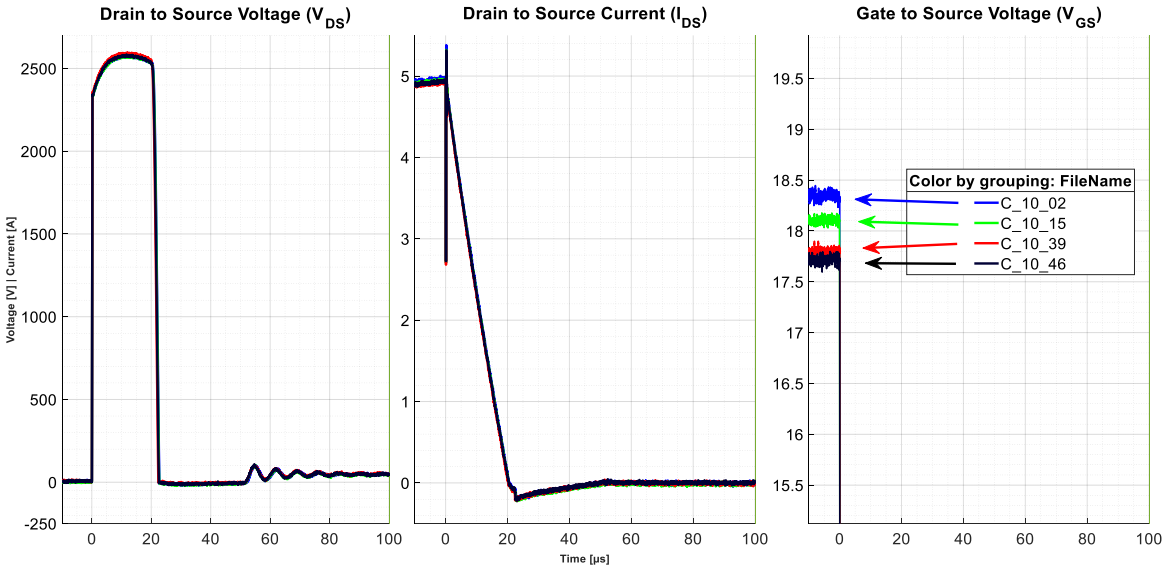

Figure 34: Oscilloscope waveforms of the Cree DUT10. From left to right: V_{DS}, I_{DS}, and V_{GS}. The blue line shows the 300 AR aging pulse, the green line shows the 1600 AR aging pulse, the red line shows the 4000 AR aging pulse, and the black line shows the 4700 AR aging pulse.

The X-ray investigation of the DUTs 7 to 10 did not show any abnormalities. Figure 35 shows X-ray images taken from the top side of the DUT10. From the figure, it can be concluded that the AR aging pulses do not affect the chip soldering, and any changes in the solder voids do not occur even if thousands of AR aging pulses are applied to the DUTs. Furthermore, the X-ray inspection of the Cree DUTs does not reveal any failure location on the DUTs, and therefore the X-ray is not an ideal technique for finding the damaged location in the CREE 1700 V rated MOSFETs.

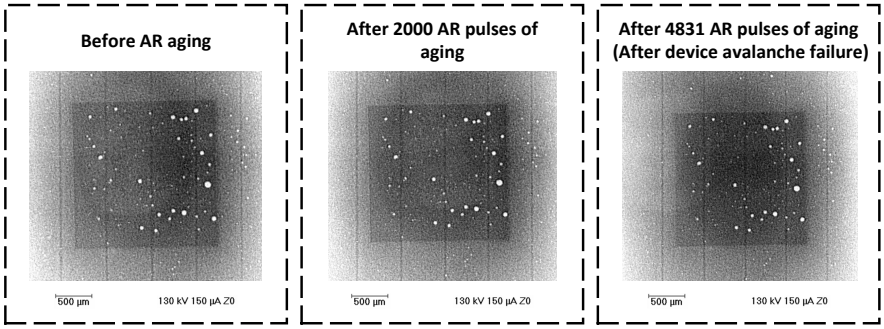

Figure 35: 2D X-ray image of the DUT10.

The SAM analysis of the DUT10 shows that the breakdown occurred close to the gate terminal of the device. The failure spot is shown in Figure 36, and the red arrow points to the breakdown location on the chip. After the SAM analysis of DUT10, the mold compound was removed, and an optical microscope image of DUT10 is shown in Figure 37. The mold compound removal proves that the breakdown of the device has occurred close to the gate terminal of the device chip and reveals a third failure mode for the Cree 1700 V devices.

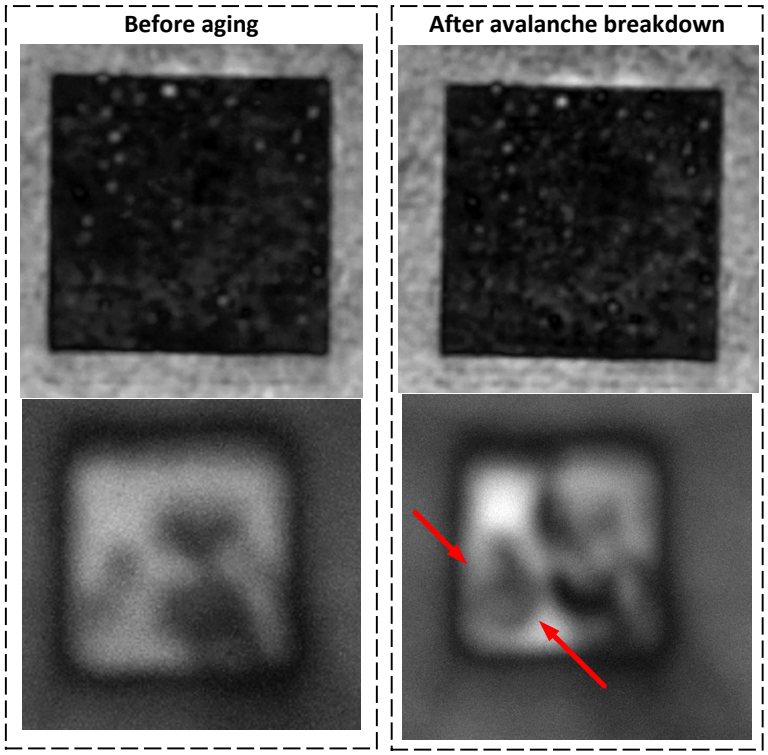

Figure 36: Cree C2M1000170 – DUT10 SAM images. On the left-hand side is the images taken before aging and on the right-hand side is the image taken after the avalanche breakdown. The red arrows indicate the failure location of the DUT.

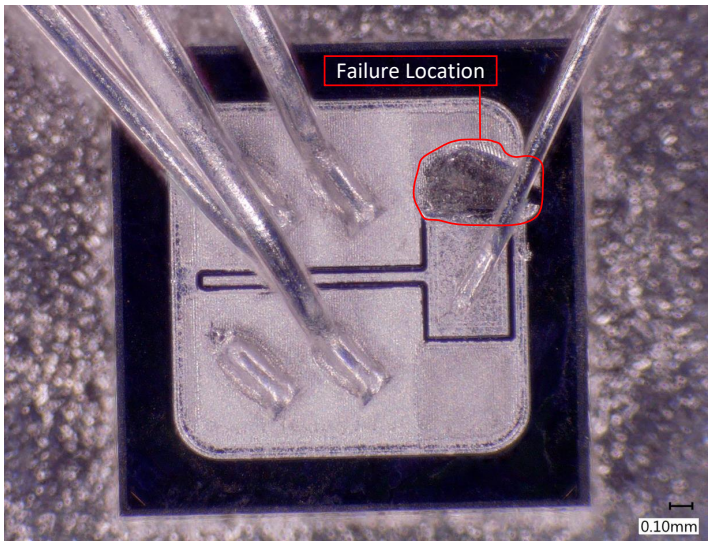

Figure 37: Failure location of the Cree DUT10 after the avalanche breakdown.

Figure 38 shows the AR aging pulse where the DUTs breakdown occures. From this figure, it can be noticed that for the DUTs 8 to 10, a slight voltage rise in the V_{GS} appears when the device failure occurs. This rise is not seen for the DUTs 1 to 6 and furthermore supports that these devices that last for several thousand AR aging pulses fail in a different way than the ones that last only hundreds of AR aging pulses. The I_{DS} and V_{DS} waveforms for the DUTs 7 to 10 are similar to the rest of the DUTs, and any notable difference are not seen.

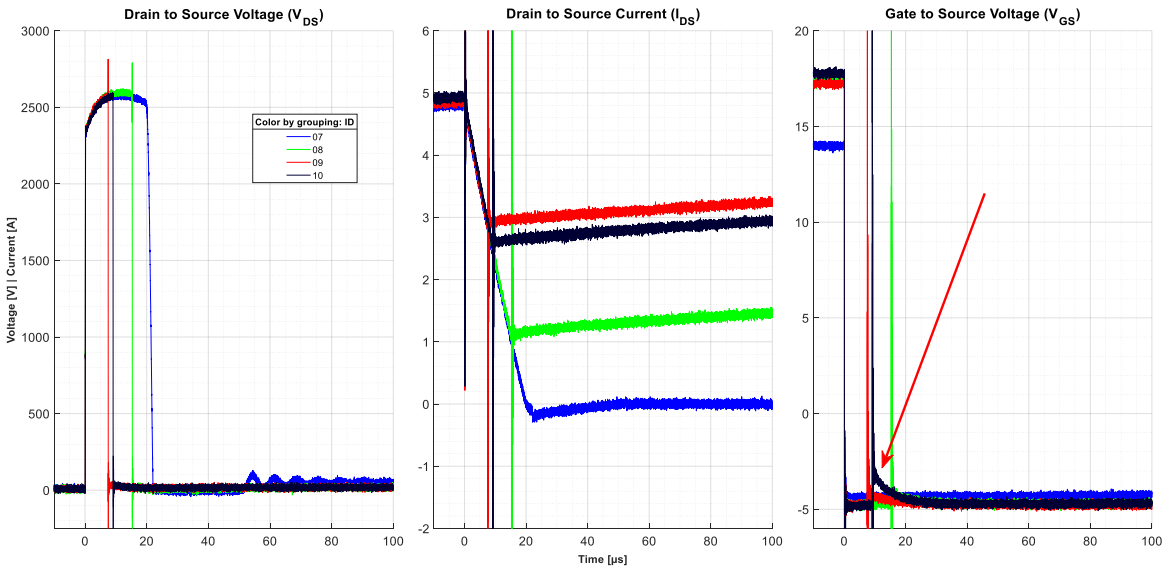

Figure 38: Oscilloscope waveforms during the AR aging of the failed Cree DUT10. From left to right: V_{DS}, I_{DS}, and V_{GS}. The red arrow indicates the rise in the V_{GS} waveform.

5.2 Summary of the Cree C2M1000170 devices

In the AR aging test performed in this thesis, three different failure modes could be observed for the Cree C2M1000170 MOSFETs. The first failure mode occurred for DUTs 1 to 2. The failure for these DUTs occurs in the chip's edge termination region (Figure 25). Since these devices failed at the first aging pulse, the likely hypothesis for the cause of failure seems to be defective edge termination structure, or possible contaminants. However, to disclose the true root cause of these failures, further failure analysis is required and is beyond the scope of this thesis.

For the second failure mode observed with the DUTs 4 to 6, the failure spot is located in the active area of the chip (Figure 31). Since the failure spot is in the active region, the likely hypothesis for the true failure root cause is thermal runaway due to chip degradation from repetitive exposure to high avalanche energies. Which is also the expected root cause of the failure in AR testing. (Kelley et al., 2016)

In the last one, seen with DUTs 7 to 10, the failure location is found close to the gate contact area (Figure 37). In this case it is speculated by the author, based on the I_{DSS} and I_{GSS} measurements shown in Figures 32 and 33, and the AR measurements shown in Figure 34, that the likely cause of failure is related to breakdown of the gate oxide. For all ten DUTs, the $V_{(\mathrm{BR})\mathrm{eff}}$ is around 2600 V, and the t_{AV} is around 22 μs with an E_{AV} of $\approx$ 120 mJ. It was possible with the SAM imaging technique to observe the failure location at the chips. The SAM also indicated that the AR aging does not impact the system solder of die-attach or the chip die structure. The X-ray taken from the top side of the DUT did not reveal any failure location on the DUTs, and therefore the X-ray is not an ideal technique for finding the damaged location for the C2M1000170 devices from Cree.

5.3 Rohm SCT2H12NZ

The same method was used for the Rohm SCT2H12NZ devices to find the AR aging parameters as was done with the Cree devices. The only difference was that t_{ON} time was started with 500 μs instead of 1000 μs that was used for the Cree devices. The same EoL test was performed where 2 AR pulses with a repetition rate of 1 Hz was given for each step. Furthermore, the same V_{DC} of 50 V was used for the Rohm devices. Table 6 shows the parameter values for each AR step.

Table 6: Parameter values used to set the aging parameters for the Rohm SCT2H12NZ devices.

Rohm SCT2H12NZ						
Measurement identification number (ID)	006	007	008	009	010	011
Supply voltage (V_{DC})	50	50	50	50	50	50
tON time (μs)	500	600	700	800	900	1000
Avalanche energy (mJ)	23.3	32.3	43.3	55.5	70.5	-
Survived the AR test (PASS/FAIL)	PASS	PASS	PASS	PASS	PASS	FAIL

The DUT for Rohm failed with parameters: $V_{\mathrm{DC}} = 50\ V$, and $t_{\mathrm{ON}} = 1000\ \mu$s. The last recorded step before the avalanche breakdown of the DUT was with the following parameter values: $V_{\mathrm{DC}} = 50\ V$ and $t_{\mathrm{ON}} = 900\ \mu$s, corresponding to an avalanche energy of $E_{\mathrm{AV}} = 70.5$ mJ. Figure 39 shows the waveforms with these parameter values.

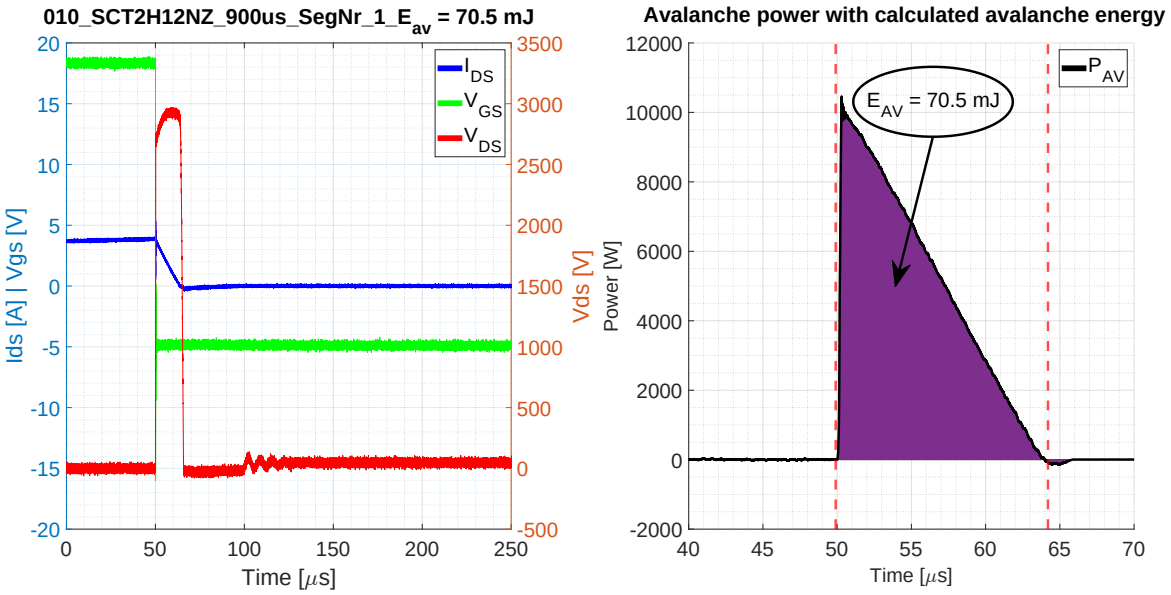

Figure 39: On the left-hand side is the last recorded AR pulse for the Rohm SCT2H12NZ SiC MOSFET, and on the right-hand side, the avalanche power with calculated E_{AV} of 70.5 mJ. The E_{AV} is calculated between the two red lines.

For the ten Rohm SCT2H12NZ samples selected for the AR test, the final aging parameters used were $V_{\mathrm{DC}} = 50\ V$ and $t_{\mathrm{ON}} = 900\ \mu$s, corresponding to an avalanche energy of $\sim$ 70.5 mJ. Contrary to the Cree devices, any pre-conditioning was not applied on the Rohm devices.

The first avalanche breakdown for Rohm devices occurred for the DUTs 1 and 2. Both DUTs failed on the first avalanche pulse and did not survive any AR aging pulses, and therefore could not be electrically re-characterized. The rest of the DUTs survived the first train of 100 AR aging pulses and were electrically re-characterized.

Figure 40 shows the first aging pulse applied to the DUTs 1 and 2. The waveforms for both DUTs are almost identical. For the DUT1, the drain to source current I_{DS} waveform goes from $\sim 3.8\ A$ down to $\sim 0.7\ A$ until the device fails. The t_{AV} for DUT1 before breakdown is $\approx 10.5\ \mu$s, and when the DUT fails ($t_{\mathrm{AV}} = 10.5\ \mu$s), the I_{DS} current is not extinguished and does not reach zero as it should. Furthermore, a fluctuation in the V_{GS} voltage is seen even if the V_{GS} applied to the device is -5 V. The V_{GS} voltage starts to increase as the I_{DS} current increases.

The DUT2 fails almost identically to the DUT1. The difference between these two devices is that the t_{AV} for DUT2 is shorter at $t_{\mathrm{AV}} \approx 8.3\ \mu$s, and therefore the I_{DS} and

V_{GS} waveform has a small variation. The failure behavior of the DUTs 1 to 2 from Rohm is almost equivalent to the Cree devices. The most notable difference between these two suppliers is that the Rohm SiC devices have a $V_{(BR)eff}$ of ≈ 2.9 kV, while again, the Cree SiC devices have $V_{(BR)eff}$ of ≈ 2.6 kV.

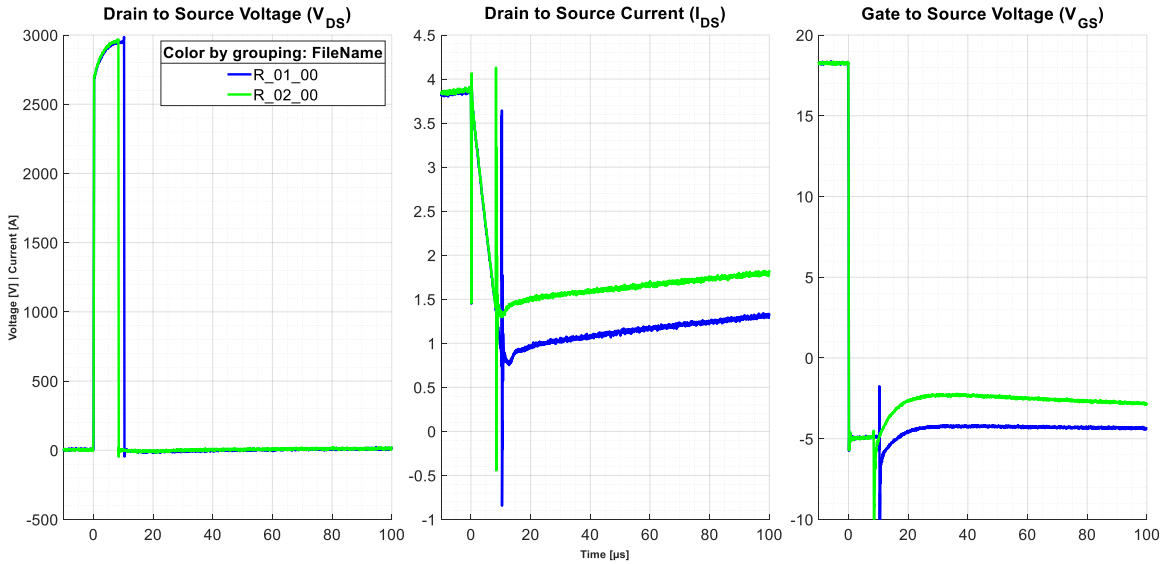

Figure 40: Oscilloscope waveforms of the failed Cree DUTs 1 and 2. From left to right: V_{DS}, I_{DS}, and V_{GS}.

Figure 41 shows the electrical characterization measurement results. The blue-colored line shows the measurement performed before any AR aging pulses are applied to the DUTs, and the green-colored line shows the measured values after the 100 AR aging pulses. The E_{AV} was ≈ 70 mJ per pulse. The figure reveals that after the 100 AR aging pulses, the drain to source leakage current I_{DSS} decreases in all eight DUTs in the range of 300 V to 1250 V, whereafter 1250 V, some of the DUTs I_{DSS} start to increase to the same value as the measurement performed before the AR aging pulses.

The gate-to-source leakage current I_{GSS} increases for all eight DUTs to 100 μA at $\sim$ 14 V. The datasheet specification for the I_{GSS} measurement for Rohm devices is that the device should not leak more than 100 nA at 22 V. After 100 AR aging pulses, the current leakage is 1000 times higher than in the datasheet specification. Furthermore, slight variation is seen in the rest of the electrical characterization measurements (I_D-V_{DS}, I_D-V_{GS}, and I_S-V_{DS}) before any AR aging pulses. The variation in the samples can cause deviation in the measurements for these DUTs.

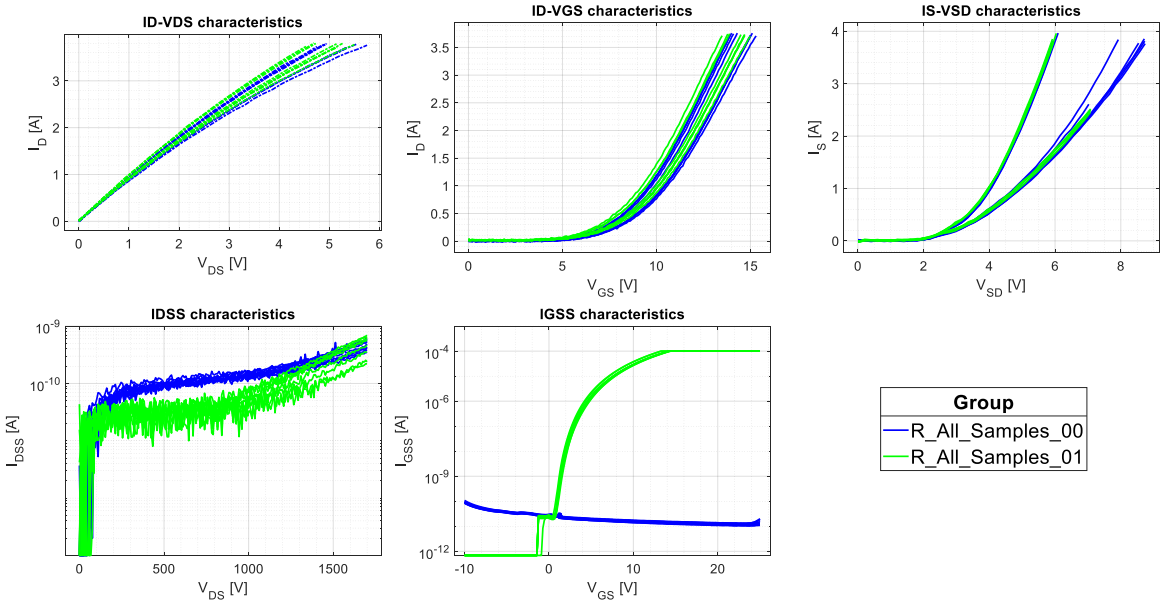

Figure 41: Electrical characterization measurement results before and after the 100 aging pulses. The E_{AV} was $\approx$ 70 mJ per pulse. Blue-colored lines are before any AR aging pulses, and the green-colored lines are after 100 AR aging pulses were applied to the DUTs.

After the electrical characterization, the 2D-Xray inspections of the ten Rohm DUTs were performed. The X-ray image taken from the top side of the DUT1 exposes the failure location on the DUT1 and is shown in Figure 42. The failure location is seen in the top left corner and is surrounded by a red circle. For the DUT2, any precise failure location cannot be seen in the X-ray image. After the X-ray examination, a SAM analysis of the DUTs was made. For the DUTs from Rohm, the SAM image was taken from the bottom side of the devices.

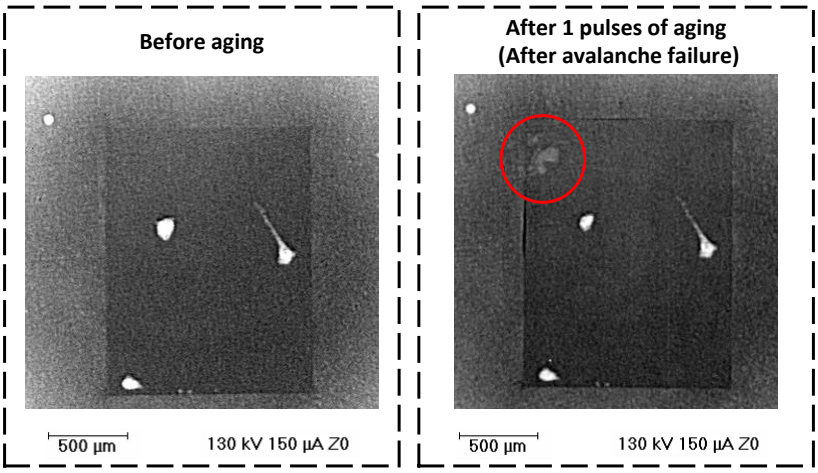

Figure 42: Rohm SCT2H12NZ - DUT1 2D X-ray images. On the left-hand side is the X-ray image taken from the top side of the device before any AR aging was applied to the DUT, and on the right-hand side is an X-ray image taken after the DUT has failed. The red circle indicates the failure location.

The SAM analysis of the DUT1 reveals the same failure location as seen in the X-ray image. The breakdown of the device occurred in the left top corner of the device. The failure spot is shown in Figure 43, and the red circle indicates the breakdown location on the chip. After the SAM analysis of DUT1, the mold compound was removed, and an optical microscope image of DUT1 is shown in Figure 44. From the figure, the failure location of the DUT1 can be precisely seen. One of the corners of the chip has completely melted, indicating that the chip's edge termination has failed. The DUTs 1 and 2 only survived for one AR aging pulse which could indicate that these two devices have had some variation in the structure of the device compared to the rest of the DUTs.

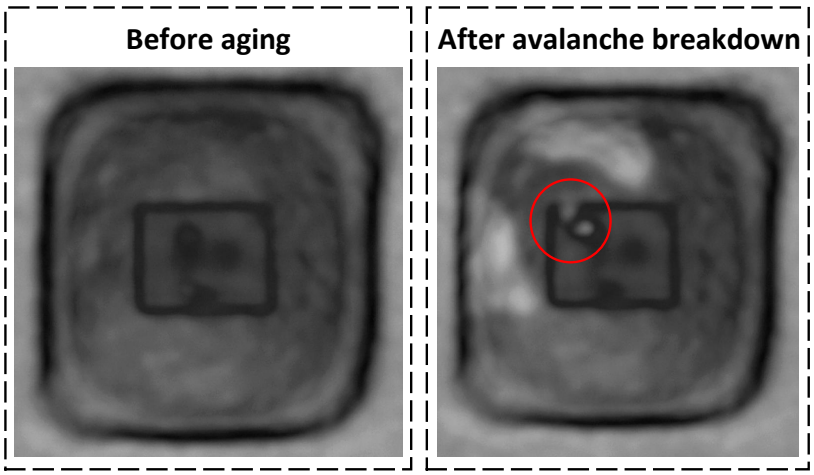

Figure 43: Rohm SCT2H12NZ – DUT1 SAM images. On the left-hand side is the image taken before AR aging and on the right-hand side is the image taken after the avalanche breakdown. The red circle indicates the failure location of the DUT.

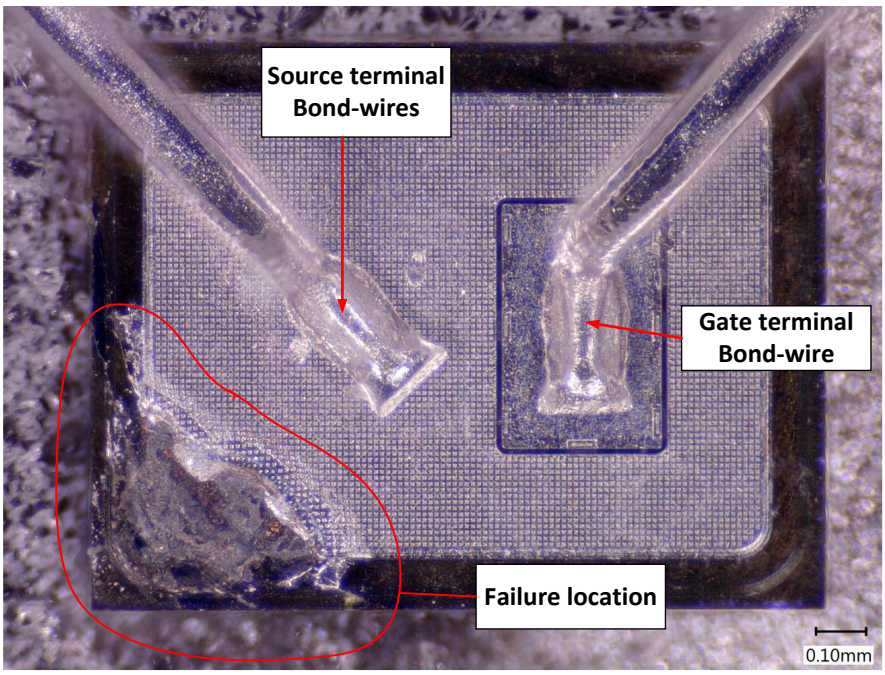

Figure 44: Failure location of the Rohm DUT1 after the avalanche breakdown.

For the rest of the DUTs 3 to 10 from Rohm, the AR aging was continued up to 3000 AR aging pulses. After every 100 AR aging pulses, electrically re-characterization and X-ray examination were performed. All the remaining DUTs 3 to 10 survived the AR tests, and any avalanche breakdown did not occur for these devices. Figure 45 displays a scatter plot of I_{GSS} characterization measurement completed after every 100 aging pulses. The DUTs from ROHM reached the maximum limit of 100 μA at V_{GS}

$\sim 14\ V$. Therefore, the I_{GSS} value is displayed at $V_{\mathrm{GS}} = 10\ V$ to show how the I_{GSS} increases after every AR iteration. The maximum measurement limit was not increased due to excessive current draw through the device's gate during the re-characterization process was not desirable as it could potentially damage or impact the device in an aging manner.

From Figure 45, it can be observed that DUTs 3 to 10 from Rohm behave similarly in the I_{GSS} measurements. For example, the IGSS measured before any AR aging applied to the DUT3 is $\sim 15\ nA$. After the first AR aging iteration, the I_{GSS} rises to 29 μA and continues to rise when additional AR aging pulses are applied. The same behavior is seen for all DUTs 3 to 10.

Figure 46 shows a similar scatter plot for I_{DSS} characterization measurement. The I_{DSS} values are displayed at $V_{\mathrm{DS}} = 1700\ V$. The figure shows that for two of the DUTs 3 and 7, the I_{DSS} decreases after the 100 first AR aging pulses. For DUT3, the I_{DSS} decreases slightly from $\sim 570\ pA$ to $\sim 470\ pA$. While more AR aging pulses are applied, the I_{DSS} increases.

For the DUTs 5 and 9, the I_{DSS} does not behave similarly after the 100 AR aging pulses. The I_{DSS} increases directly and rises when additional AR aging pulses are applied. For the I_{DSS} measurement, it should be noticed that the I_{DSS} value is ~ 500 pA. For example, after 3000 AR aging pulses, the I_{DSS} has increased to ~ 1 nA, which is still below the maximum I_{DSS} value of 10 μA stated by the Rohm device's datasheet.

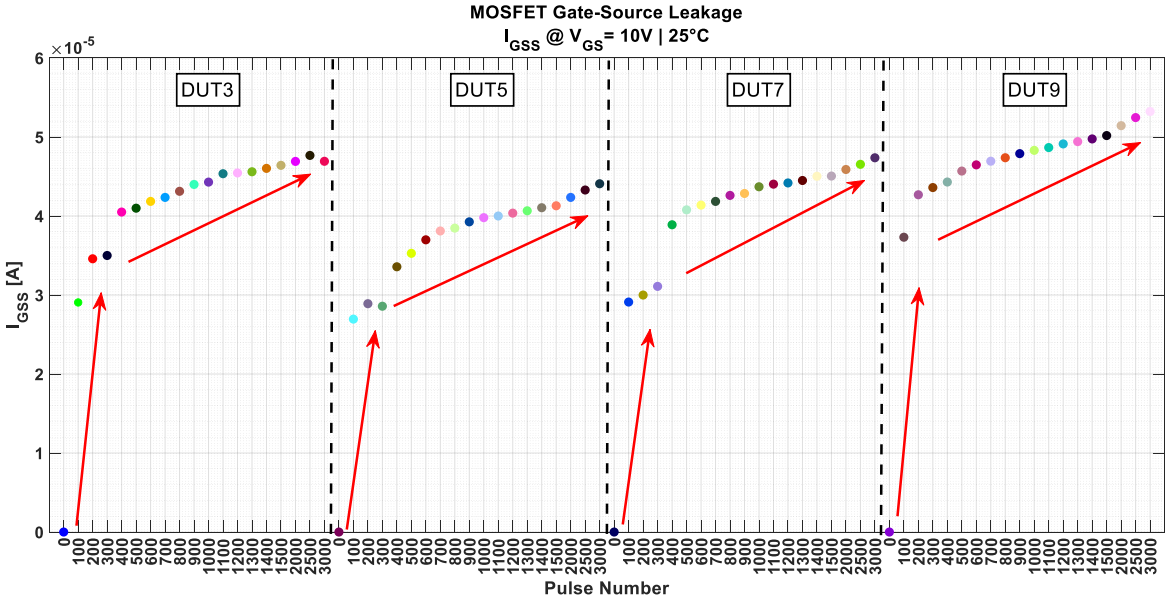

Figure 45: Gate to source leakage current plot for DUT3, DUT5, DUT7 and DUT9. The I_{GSS} measurement was performed after every 100 aging pulses. The I_{GSS} value is taken at $V_{\mathrm{GS}} = 10\ V$.

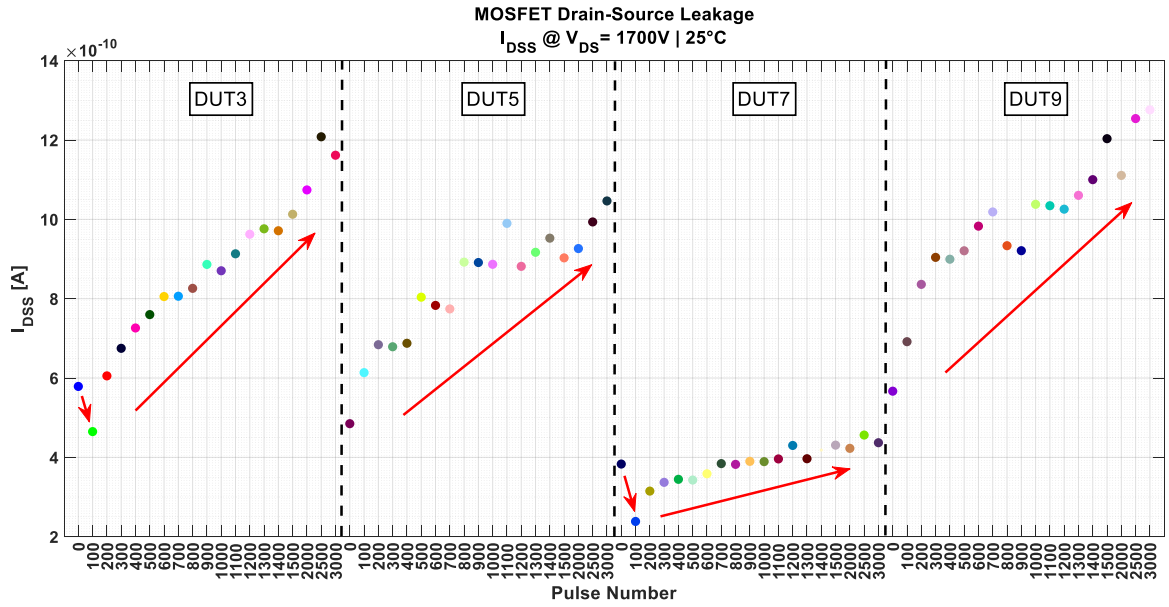

Figure 46: Drain to source leakage current plot for DUT3, DUT5, DUT7 and DUT9. The I_{DSS} measurement was performed after every 100 aging pulses. The I_{DSS} value is taken at $V_{\mathrm{DS}} = 1700\ V$.

The X-ray images taken from the top side of the DUTs after every AR iteration do not show any constructional change in the DUTS 3 to 10. Figure 47 displays the X-ray images taken from the DUT3, and from the figure, it can be concluded that the

AR aging of the Rohm devices does not affect the solder area or the solder voids in the DUT. The same appears for the DUTs 4 to 10, and any exceptions are not seen in these DUTs.

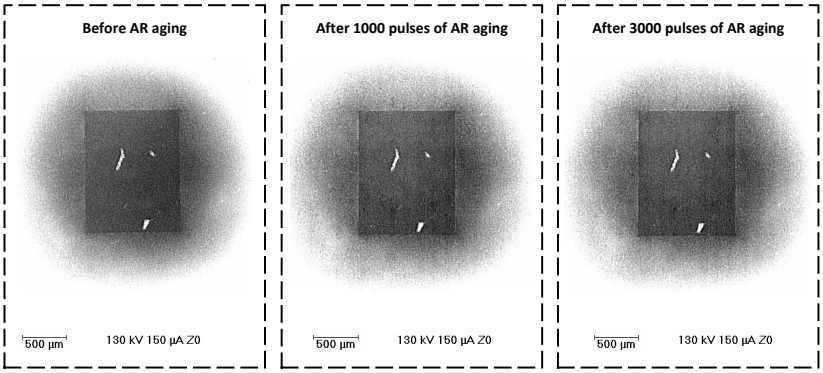

Figure 47: 2D X-ray image of the DUT3.

Figure 48 shows the SAM analysis completed on DUT3 before and after 3000 AR aging pulses. The SAM figure does not reveal any substantial difference between the before and after images.

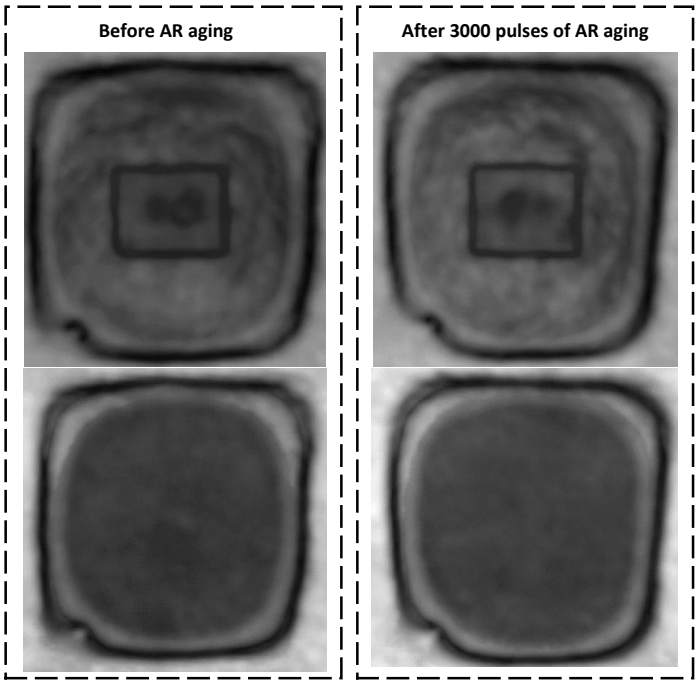

Figure 48: SAM images of the DUT3.

Additionally, for the DUTs 3 and 10, it was determined to remove the mold compound to check if any noteworthy changes could be observed with an optical microscope

of the DUTs. As shown in Figure 49, visual inspection of DUT10 reveals that one of the bond wires has been cut off. This was most likely caused by the demolding process. For the DUT3, any abnormality is not seen in the image.

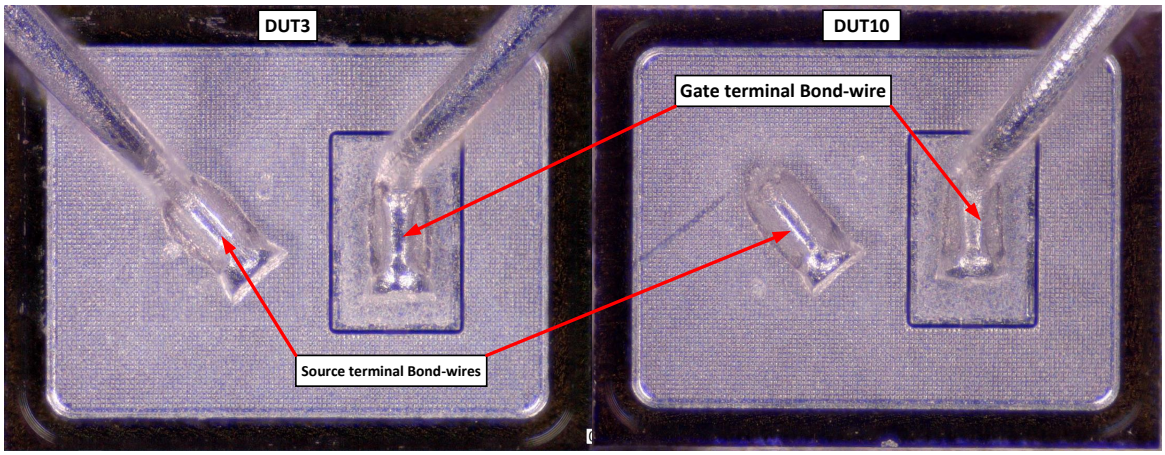

Figure 49: Optical microscope image of the DUT3 and DUT10.

The oscilloscope measurements during the AR test did not reveal any difference for the DUTs 3 to 10. Figure 50 shows every hundred AR pulses executed to the DUT3. Any variability in the waveforms of V_{DS}, I_{DS}, or V_{GS} cannot be observed between the AR aging iterations. The $t_{\mathrm{AV}} = 16$ μs stays the same during the full range of the AR aging.

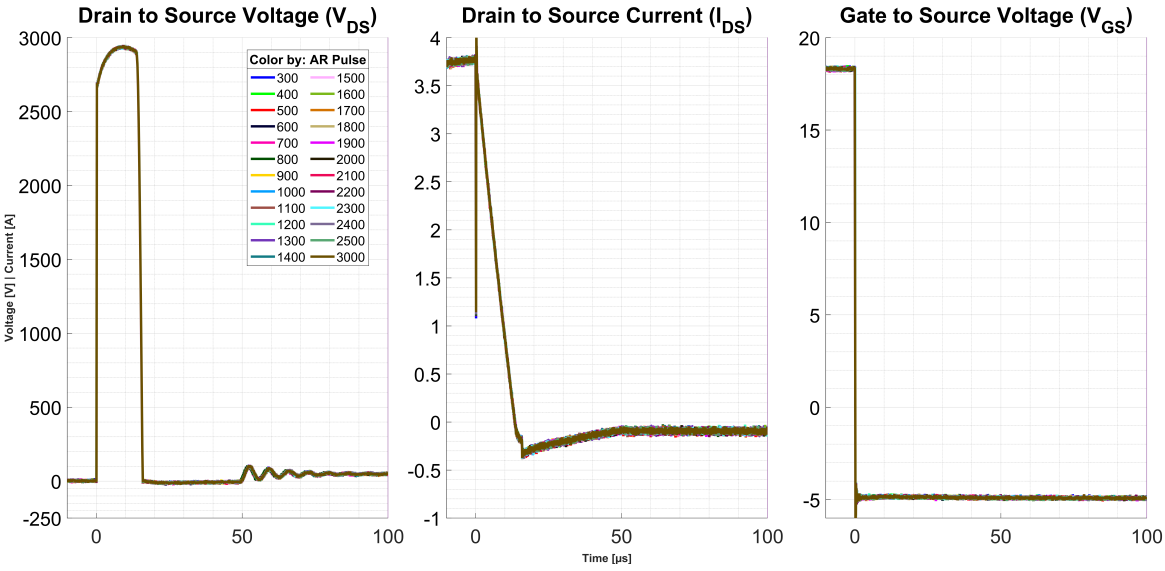

Figure 50: Oscilloscope waveforms of Rohm DUT3. From left to right: V_{DS}, I_{DS}, and V_{GS}.

5.4 Summary of the Rohm SCT2H12NZ devices

Figure 51 displays the number of applied avalanche pulses for the DUTs from Rohm. The DUTs 1 and 2 did not tolerate any AR aging pulses. The rest of the DUTs displayed a very homogeneous behavior in the AR test as well as in the electrical characterization measurements.

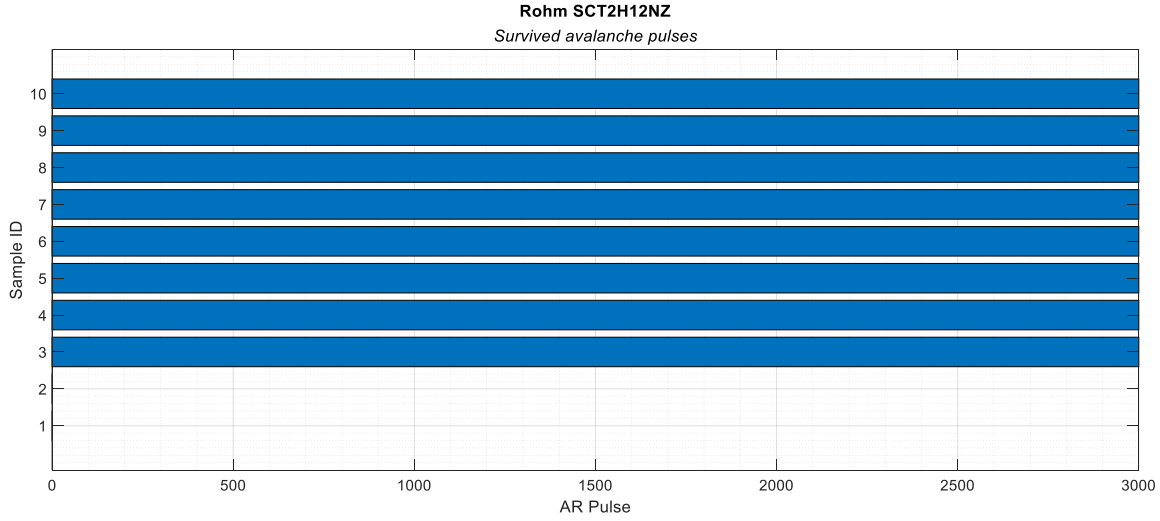

Figure 51: Total AR aging pulses applied for each DUT from Rohm.

The $V_{(\mathrm{BR})\mathrm{eff}}$ ($\sim 2900\ V$) for the Rohm devices was much higher than for the Cree devices, even if the t_{AV} ($\sim 11\ \mu$s) and dissipated E_{AV} were smaller (~ 70 mJ). The eight DUTs from Rohm did not completely fail in the AR test. However, the gate leakage of the devices was measured up to $\sim 500\ \mu A$ at $V_{\mathrm{GS}} = 10\,V$, an increase by a factor of 50k, after the 3000 AR aging pulses. The test was stopped after the 30^{th} iteration, as it was concluded that the initial aging parameter values should have been set higher. Nevertheless, eventually these devices would probably have failed due to the excessive current drawn through the gate of the devices.

As with the Cree devices, for the Rohm devices it was also possible to observe the failure location on the chips with SAM. The SAM images also indicated that the AR aging does not impact the system solder of die-attach nor the chip die structure. Contrary to the Cree devices, the X-ray images taken from the top side of the Rohm DUT1 did reveal the failure location. However, nothing could be seen for Rohm DUT2.

6 Discussion

The test setup proposed in this thesis was realized as device manufacturers of SiC MOSFETs still seems to provide inconstancy in their datasheet avalanche energy values. Often, especially regarding SiC devices, the avalanche ruggedness or UIS is not mentioned at all, not only in the test methodology nor test settings but also not in the maximum ratings where the maximum avalanche energy is usually reported. For instance the datasheets of the devices tested in this thesis do not state any information on UIS nor avalanche ruggedness capability. In Cree's datasheet, the clamped inductive switching is presented with schematic and energy waveforms, but the unclamped is not mentioned. The Rohm datasheet provides no information on clamped nor unclamped inductive switching.

Ten devices from Cree were tested. These devices showed a large variation in the avalanche ruggedness test results, from 100 to roughly 10000 AR aging pulses, from which three district groups could be observed. The measurement data from the AR tests also showed that the DUTs failed differently. In addition, aging effects were observed in the electrical characterization measurements for some of the DUTs before they reached complete failure. An interesting behavior of the relationship between the I_{DSS} and I_{GSS} was seen, and further investigation of this mechanism should be made. Based on the electrical measurements and AR test results, one device of each group was selected for demolding in the final analysis stage. The results clearly revealed three different failure modes with the Cree devices in the AR test.

On the contrary to the Cree devices, the ten Rohm devices tested showed a very homogeneous behavior. Most of the devices survived the same amount of repetitive AR pulses. The interesting behavior of the Rohm devices was that after the first 100 AR aging pulses, the I_{DSS} declined compared to the pre-characterization of the DUTs, whereas the I_{GSS} increased rapidly over the applied measurement compliance. In addition, the I_{DSS} increased when more AR aging pulses were applied to the DUTs.

When comparing the effective avalanche breakdown voltage for both suppliers, the effective avalanche breakdown voltage for Cree rose to $\sim 2.6\ \mathrm{k}V$ while again for the Rohm devices up to $\sim 2.9\ \mathrm{k}V$. The avalanche energy of the Rohm devices was roughly

half of the Cree devices, but the current rating is also much lower.

The obtained results are not directly comparable between the two devices since the MOSFETs are rated differently and therefore also different aging parameter settings were used, such as the applied pulse widths, resulting in dissimilar avalanche energies E_{AV} of the DUTs. However, the results for the supplier itself are comparable, and the work has shown that the test setup can reveal different failure modes for the tested DUTs.

Regarding future studies, it is worth noting that for a fair comparison between different supplier's devices, the performed avalanche test should be made with the same setup, inductor, and pre- and post-characterization procedures. Furthermore, the avalanche time t_{AV} for the various supplier DUTs should be the same, and the final avalanche energy E_{AV} should be obtained by keeping the pulse width identical and controlling the input voltage V_{DC} to the DUTs. Thus, the DUTs are kept in avalanche mode equally in terms of time. In addition, adding gate charge and gate capacitance characteristics to the electrical characterization measurements might be useful for observing degradation of the device and should be considered for future SiC MOSFETs avalanche ruggedness testing.

7 Conclusions

In this thesis, a test bench was designed and built for benchmarking the avalanche ruggedness of SiC MOSFETs. The test setup design is simple and does not require expensive or uncommon parts. However, for future use, the test setup should be further improved in terms of the safety aspect, for instance, by enclosing the whole setup or by covering the exposed voltage terminals.

In addition to the realized test bench, a test procedure for carrying out the AR test was also presented. Performing the whole AR testing procedure is not time consuming, since both the characterization measurements as well as obtaining the AR aging measurements from the DUTs can be acquired within a few hours. The steps involved in the testing procedure itself are not complicated. However, it requires expertise in using expensive equipment, such as the oscilloscope, voltage and current probes, and the power device analyzer. The proposed AR testing procedure was also shown to be especially suited for capturing the progress of the degradation in the DUTs. This enables an easier and more detailed comparison between the DUTs, which serves as a good basis for benchmarking and failure analysis purposes.

Failure analysis of the tested devices revealed different failure modes. For the tested Cree devices, three different failure modes were observed. The first failure mode was seen at the edge termination region, the second failure mode was found in the active area, and the third failure mode was located close to the gate contact area of the chips. Determining the true root cause for these failure modes is a topic for future work. However, the measurement data and failure analysis indicated that the observed failure modes relate to thermal runaway and gate oxide breakdown. Regardless, to fully utilize the presented testing method, further work on the physics of failure should be carried out.

Based on the AR measurement results and scanning acoustic microscopy images, three devices of each supplier were selected for further decapsulation and optical microscopy analysis. The optical imaging confirmed the same failure locations as seen in the SAM images of the failed devices. The SAM images also indicated that the AR aging does not impact the system solder of die-attach nor the chip die structure. On

the other hand, the X-ray imaging did not reveal any failure locations except in one case. Hence, for the AR test, the SAM imaging technique is better suited for failure location analysis than a more expensive X-ray technique.

The avalanche ruggedness test of SiC MOSFETs was revealed to be a useful test for assessing the component's general reliability. Depending on the application case, the AR test is recommended for benchmarking different MOSFET suppliers that are considered for the end product.

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Appendices

Appendix 1: Block diagram of the avalanche ruggedness test setup

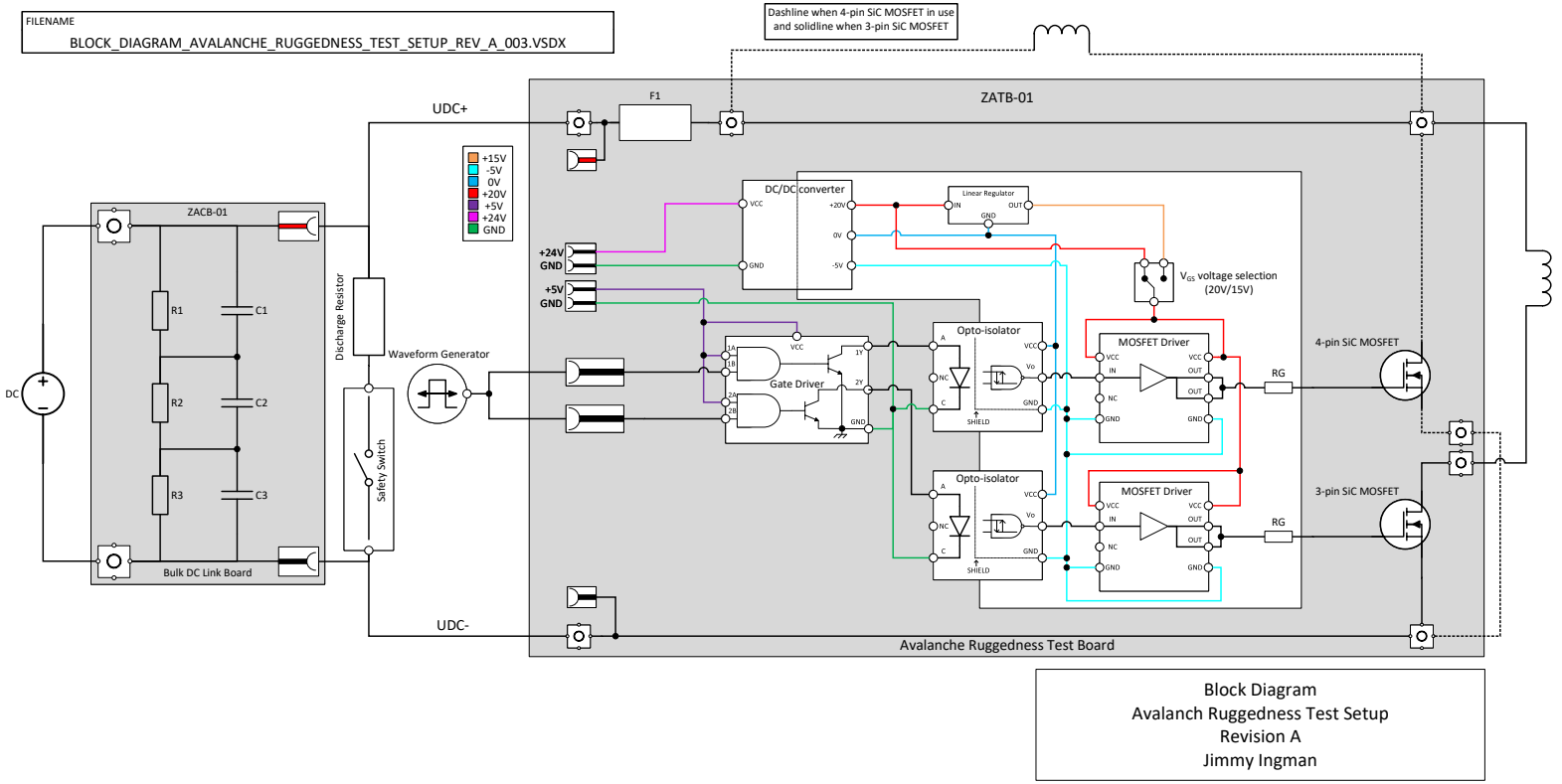

Figure A1: Block diagram of the AR test setup