Design of high switching frequency PFC totem-pole converter

Lappeenranta–Lahti University of Technology LUT

Master's thesis

2023

Väinö Kolho

Examiners: Professor, Pasi Peltoniemi

Doctor of Philosophy, David Meneses Herrera

ABSTRACT

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93 pages, 65 figures, 3 tables and 2 appendices

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Keywords: Power converter, Power Factor Correction, Totem-pole, Choke design, High switching frequency

With tightening regulations and demand for high electrical efficiency power converter designers are continuously looking for ways to improve efficiency. Another point of great interest in power converter design is high power density. Traditionally diode rectified converters have been the most proven topology. With advancements in semiconductor technology, new topologies have emerged. Currently totem-pole topology is attracting high interest.

In this work the main choke is designed and tested for a totem-pole converter. The background of the work is the need to test feasibility of XMC1400 microcontroller for high switching frequency operation, up to 1 MHz. The choke is designed for an existing prototype single phase totem-pole converter with 210 W 400 V output.

Several different chokes were built in the range of 26 to 52 µH. Initially, the 26 µH was taken for closer inspection, as it allowed for testing the highest switching frequency up to 1 MHz. The microcontroller proved to be too slow, however. A second choke with 99 µH was built for up to 300 kHz in 100 % load. With proper control the microcontroller was able to operate in such frequency. Due to time constraints further testing, such as efficiency and PF of the converter, were not measured in this work, which are they key performance parameters of any PFC converter.

TIIVISTELMÄ

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Korkeakytkentätaajuisen tehokerroinkorjatun toteemipaalumuuntimen suunnittelu

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Avainsanat: Teholähde, Tehokertoimen korjaus, Toteemipaalumuunnin, Kuristimen suunnittelu, Korkea kytkentätaajuus

Energiahyötysuhteen tiukentuvien vaatimuksien takia tehoelektroniikkasuunnittelijat etsivät jatkuvasti keinoja parantaa hyötysuhdetta. Hyötysuhteen lisäksi tehotiheys on usein suuren kiinnostuksen alla teholähteiden suunnittelussa. Dioditasasuunnatut teholähteet ovat pitkään olleet suosituin topologia AC/DC teholähteille, mutta puolijohdeteknologian kehityksen myötä uusia topologioita on noussut esiin. Toteemipaalu topologia herättää nykyisellään paljon kiinnostusta.

Tämän työn tarkoituksena on suunnitella ja testata kuristin toteemipaalu-teholähteelle. Työn taustana on tarve testata XMC1400 mikrokontrollerin toimintaa korkeilla kytkentätaajuuksilla, aina 1 MHz saakka. Kuristin suunniteltiin olemassa olevalla yksivaiheiselle prototyyppi toteemipaalu teholähteelle, jonka lähdössä on 210 W ja 400 V DC.

Muutama erilainen kuristin suunniteltiin ja rakennettiin välillä 26-52 µH. 26 µH otettiin aluksi lähempään tarkasteluun, koska sillä oli mahdollista testata korkeita kytkentätaajuuksia aina 1 MHz asti. Testauksessa tuli kuitenkin ilmi, että mikrokontrolleri oli yksinkertaisesti liian hidas. Uusi 99 µH kuristin suunniteltiin, jolla saavutettiin noin 300 kHz kytkentätaajuus täydellä kuormalla. Oikealla ohjauksella mikrokontrolleri pystyi operoimaan kyseisellä taajuudella. Aikarajoitteiden takia teholähteen hyötysuhdetta ja tehokerrointa ei ehditty mitata tässä työssä, jotka normaalisi ovat tehokerroinkorjatun teholähteen tärkeimpiä arviointiperusteita.

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The work for this thesis was done for Infineon Technologies, thank you for providing me with the opportunity to work on an interesting subject. From Infineon I would like to express my greatest gratitude to my supervisor Ph.D. David Meneses Herrera. From LUT University I would like to thank Professor Pasi Peltoniemi and Postdoctoral researcher Aleksi Mattsson for supervising my thesis.

Väinö Kolho

Helsinki, 17.5.2023

SYMBOLS AND ABBREVIATIONS

Symbols

A	Area	[m^2]
a	Steinmetz coefficient	
A_L	Inductance factor	[H]
$\hat{B}$	Flux density swing	[T]
B	Magnetic flux density	[T]
b	Steinmetz coefficient	
C	Capacitance	[F]
cos(φ)	Power factor	
d	Diameter	[m]
D	Diode	
D	Duty cycle	
E	Energy	[J]
f	Frequency	[Hz]
H	Magnetic field strength	[A/m]
I	Current	[A]
iL	Inductor current	[A]
K	Factor	
k	Steinmetz coefficient	
L	Inductance	[H]
l	Length	[m]
N	Number (of)	

n	Number (of)	
P	Power	[W]
Q	Charge	[C]
Q	Reactive power	[var]
R	Resistance	[Ω]
S	Apparent power	[VA]
S	Switch	
t	Time	[s]
V	Voltage	[V]
V	Volume	[m^3]

Greek characters

Δ	Change	
δ	Skin depth	[m]
μ_r	Relative permeability	
ρ	Resistivity	[Ω/m]

Constants

μ_0	Vacuum permeability, $1.25664 \cdot 10^{-6}$

Subscripts

avg	Average
avg_pk	Average peak value
cu	Copper

d	Distortion
e	Effective
g	Gap
g	Gate
in	Input
max	Maximum
negZVS	Negative valley
o	Output
oss	Output
out	Output
PD	Propagation delay
pk	Peak
ref	Reference
rms_n	Rms value of nth harmonic
rr	Reverse recovery
sw	Switching
w	Window

Abbreviations

APFC	Active Power Factor Correction
AWG	American Wire Gauge
CCM	Continuous Conduction Mode
CrCM	Critical Conduction Mode
DCM	Discontinuous Conduction Mode

DF	Dissipation Factor
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FEM	Finite Element Method
GaN	Gallium Nitride
HF	High Frequency
LP	Low Profile
MnZn	Manganese Zinc
MOSFET	Metal–Oxide–Semiconductor Feld-Effect Transistor
PF	Power Factor
PFC	Power Factor Correction
PLECS®	Piecewise Linear Electrical Circuit Simulation
PWM	Pulse Width Modulation
RMS	Root Mean Square
Si	Silicon
SiC	Silicon Carbide
SMPS	Switched-Mode Power Supply
SR	Set-Reset
TCM	Triangular Current Mode
THD	Total Harmonic Distortion
WBG	Wide-Bandgap Semiconductor
ZVS	Zero Voltage Switching

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1 Introduction

In the world of power electronics there is a constant trend towards higher electrical efficiency with ever tightening regulation from governments requiring higher efficiency. Another point of great interest is power density, as customers expect rapid charging of their devices, such as mobile phones, with devices taking a reasonable amount of space. Efficiency and power density often go together, as improved efficiency also means less dissipated heat, decreasing the size of cooling components.

With advancements in semiconductor technology new topologies have emerged. Traditionally a classic diode rectified converter has been the most proven technology, however other bridgeless topologies have emerged, thanks to the development of semiconductors. One of the most attracting topologies today is the totem-pole converter, which this work is focused on.

1.1 Objectives and background

This work is focused on design of soft switching high switching frequency totem-pole converter. The background for the project is the need to test feasibility of XMC1400 microcontroller for high switching frequency operation with Triangular Current Mode (TCM) and hysteresis control implementation. The initial goal was to see whether the microcontroller can handle switching frequencies up to 1 MHz.

The focus in the thesis is the design of the main choke for the converter, however all relevant aspects of totem-pole are covered in some detail. High ripple current of TCM operation sets a special environment for choke design. An existing single phase Continuous Conduction Mode (CCM) totem-pole converter with certain modifications is used as development and testing platform for the choke and microcontroller. The converter has 210 W 400 V DC output.

1.2 Structure of thesis

Chapter 2 is the literature part of the thesis, and it gives a brief overview on Power factor (PF) and Power Factor Correction (PFC), boost PFC topologies and PFC conduction modes. Operation of totem-pole converter control is presented in more detail in chapter 3. Chapter 4 includes the implementation part, with testing in chapter 5.

The actual design phase of the converter is after the literature part. As mentioned earlier, the main focus is on the magnetics design for the choke. The implemented choke is then measured. The feasibility of the XMC1400 microcontroller for high frequency is tested once the main choke is implemented.

2 Power factor correction

In electric systems, PF is defined by the ratio of which an AC system utilizes apparent power *S* fed to the system and converts it to useful real power *P*. PF is defined as

$$\mathrm{PF} = \frac{\text{Real power}}{\text{Apparent power}} = \frac{P}{S} \tag{1}$$

In a case of purely resistive load, where voltage and current are in same phase, PF is 1. In real life applications however, there are inductive and capacitive elements in the load, causing phase shift between current and voltage, and thus worsening PF. Power factor can be illustrated with power triangle alongside with voltage and current waveforms, as presented in Figure 1.

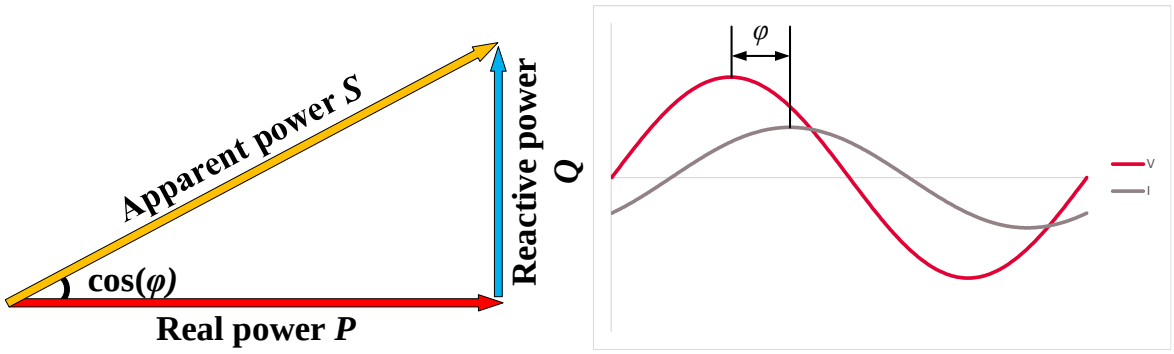

Figure 1 Power factor triangle (left) and lagging power factor (right).

For a linear load with purely sinusoidal voltage and current as in Figure 1 right, where PF only depends on phase difference between current and voltage, PF is

$$\mathrm{PF} = \cos(\varphi) \tag{2}$$

However, non-linear loads introduce non-sinusoidal components to the system. For practical purposes, electrical distribution grid can be considered as stiff system with ideal voltage waveform. PF for a system with sinusoidal voltage and non-sinusoidal current can be defined as

$$\mathrm{PF} = K_\mathrm{d} \cdot \cos(\varphi) \tag{3}$$

where K_d is the distortion power factor.

Distortion power factor is defined as the ratio of fundamental line current and total line current Root Mean Square (RMS) values.

$$K_d = \frac{I_{rms\_1}}{\sqrt{I_{rms_1}^2 + I_{rms_2}^2 + \cdots + I_{rms_n}^2}} = \frac{1}{\sqrt{1 + \frac{I_{rms_2}^2 + I_{rms_3}^2 + \cdots + I_{rms_n}^2}{I_{rms\_1}}}} \quad (4)$$

where I_{rms_n} is the RMS current of nth harmonic. For Total Harmonic Distortion (THD) of current

$$THD = \frac{\sqrt{I_{rms_2}^2 + I_{rms_3}^2 + \cdots + I_{rms_n}^2}}{I_{rms\_1}} \quad (5)$$

By combining equations (4) and (5) the distortion power factor equals to

$$K_d = \frac{1}{\sqrt{1 + THD^2}} \quad (6)$$

And by combining (3) and (6) the PF formula can be expressed as

$$PF = \frac{\cos(\varphi)}{\sqrt{1 + THD^2}} \quad (7)$$

The key takeaway from the power factor formula is that the reason for poor PF is either phase shift between input voltage and current together with harmonics in the line current. To improve PF of a system the line current should keep the same phase with the grid voltage and current harmonics should be dampened.

2.1 Power factor control

Power factor can be controlled passively with passive electrical filters or actively by incorporating active switch(es) with passive components. In figure 2 is an example of passive PFC circuit, a voltage doubler rectifier. Diodes and capacitors convert AC to DC, and inductor *L* improves PF.

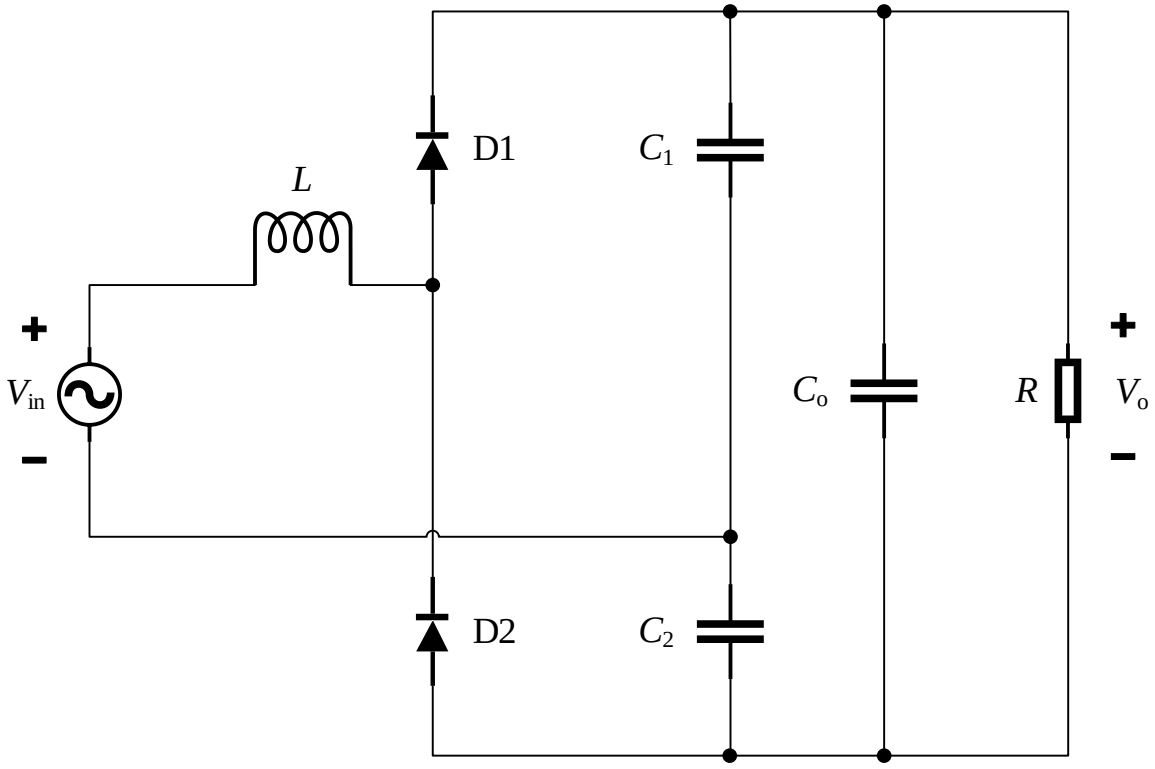

Figure 2 Voltage doubler rectifier passive PFC.

The passive power factor correction circuit includes only non-controlled passive components for power factor correction. Therefore, passive PFC is only suitable for applications, where active control is not required. Because the passive PFC converter operates at low (50 or 60 Hz) line frequency, the inductor and capacitors need to be large, making it only suitable for low power applications. (Toshiba, 2019, 6-7)

Active power factor correction (APFC) on the contrary actively senses and shapes the input current waveform to improve PF, as well as regulates the output voltage. Usually APFC is done with Switched-mode power supply (SMPS). SMPSs introduce actively controlled switches to regulate PF and output voltage. Whereas passive power factor correction is easy to implement and low in cost, APFC offers superior performance (McDonald Brent, Lough Ben, 2020, 4). One of the most common SMPS circuits is a boost, also known as step-up converter, presented in Figure 3.

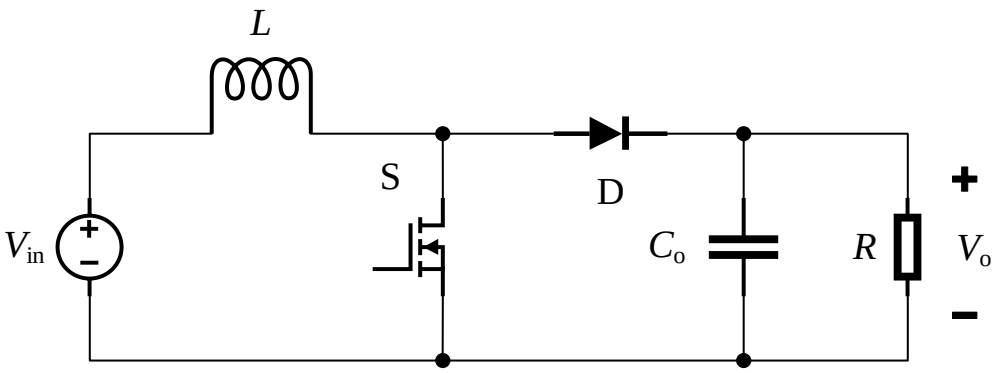

Figure 3 Boost converter.

A boost converter converts a DC voltage to a higher DC voltage. The active switch is regulated to achieve the desired output voltage. When S is closed, inductor L is being energized by the input source, while capacitor C_o is feeding the load R. Diode D is reverse biased, as its anode is connected to the same ground as S, and no current is passing through it. When S is open, the load R and C_o are being fed by the input and the energy stored in the magnetic field of the inductor through D, increasing the output voltage, as there are two sources in series. The key waveforms of boost converter in CCM operation mode are presented in Figure 4.

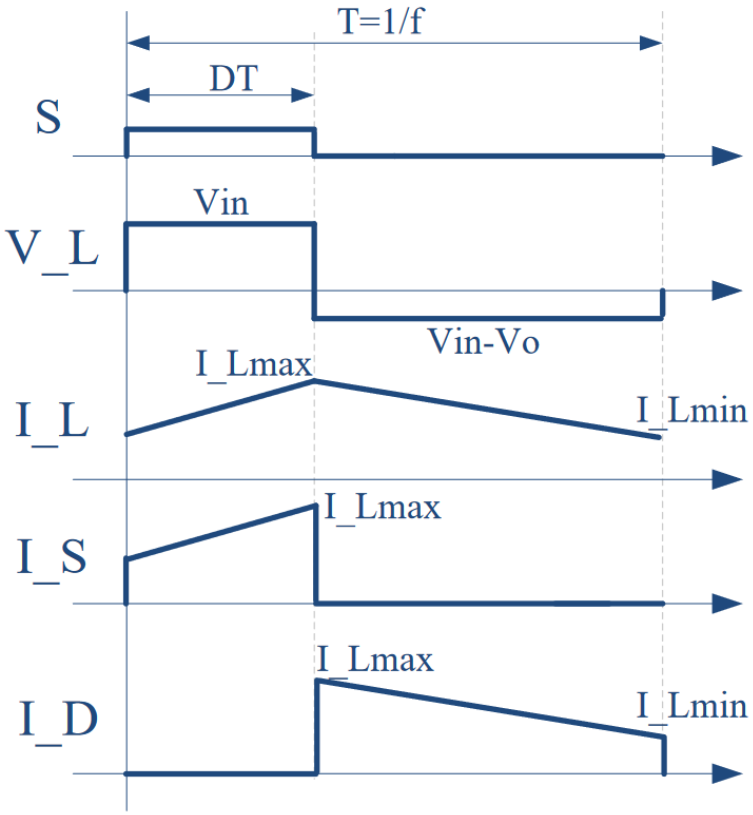

Figure 4 Key waveforms on boost converter in CCM operation. (Abdel-Rahman Sam, Stückler Franz, Siu Ken, 2016, 2)

The waveforms visualize the operation of boost converter by showcasing the important waveforms in relation to the switch position. As the operation of boost converter forms the basis of any type of boost PFC converter, understanding its working principle is essential.

2.2 Topologies for AC-DC boost PFC converters

An especially important category of SMPS are AC-DC converters used to convert energy from electrical grid to common user applications and devices. There is continuous pressure for higher energy efficiencies, and as such designers are always looking for ways to cut power losses wherever possible. In this chapter several boost PFC converter topologies are presented.

2.2.1 Traditional boost PFC converter

A traditional boost PFC converter, presented in Figure 5, consists of a diode bridge for line rectification and boost topology to step-up the output voltage. At any given time 3 semiconductors are conducting.

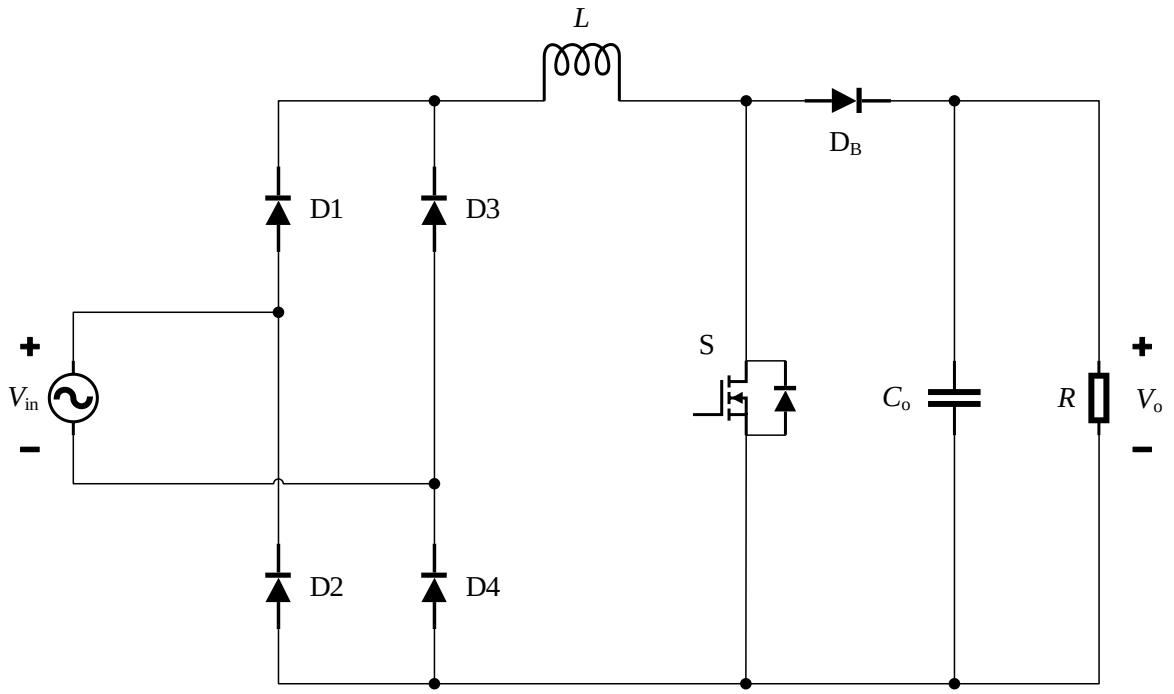

Figure 5 Traditional boost PFC converter.

Diodes 1-4 operate at line frequency. During positive AC half-cycle, current passes through D1 and returns through D4. During negative half cycle, current route is through D3 and D2. The rest of the circuitry consists of basic boost topology and operates in same way, as in figure 3. The states of traditional boost PFC are illustrated in Figure 6.

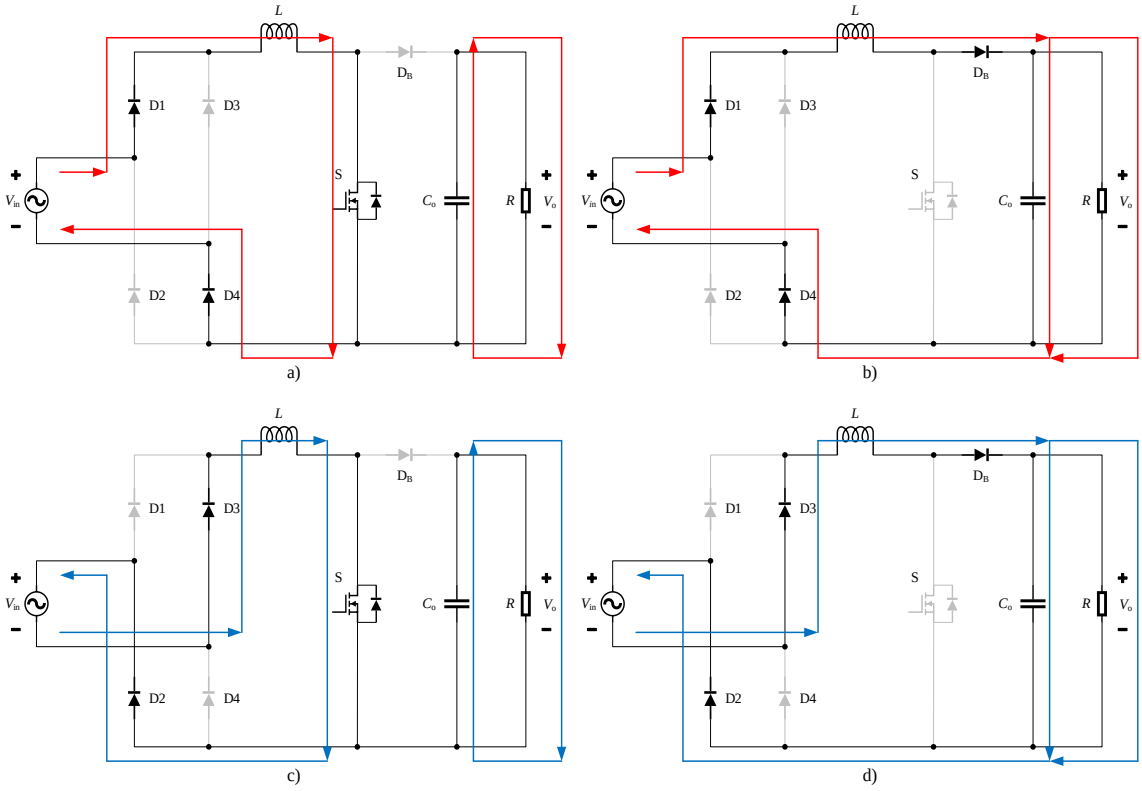

Figure 6 Operating modes of traditional boost PFC in positive half cycle (a, b) and negative half cycle (c, d).

Traditional boost PFC is a robust and proven design, but the main issue is the high conduction losses in the diodes. Bridgeless topologies have since emerged to address the diode bridge losses. (Chellappan Salil, 2018)

2.2.2 Bridgeless PFC boost converter

In bridgeless topologies the diode rectifier bridge is removed, hence the name bridgeless. Figure 7 presents a traditional bridgeless boost PFC converter.

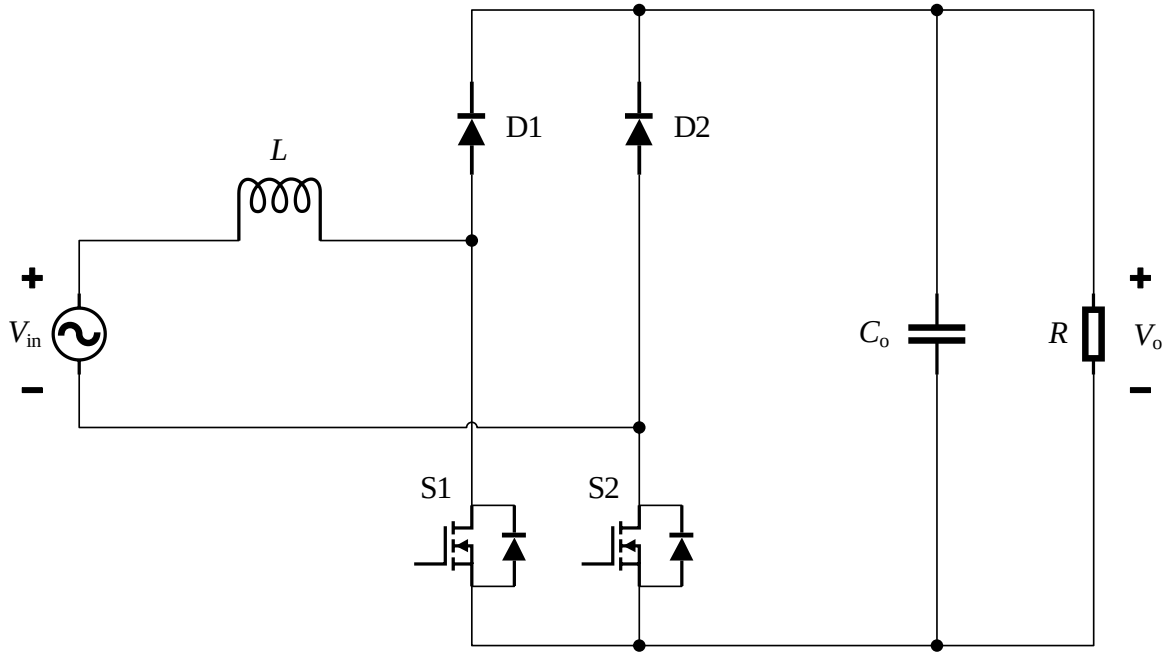

Figure 7 Bridgeless boost PFC converter.

In bridgeless PFC topology the boost inductor is moved to the AC input side and the bottom diodes of rectification bridge are replaced with active switches. During positive half cycle, D1 and S1 operate in boost mode, and the body diode of S2 acts as current return path. Consequently, during negative half cycle D2 and S2 operate in boost mode, and the body diode of S1 is the current return path.

Compared to traditional boost PFC topology, bridgeless PFC topology eliminates losses in the diode rectifier. The number of semiconductors in the current path is reduced from 3 to 2 compared to the traditional boost PFC. Another benefit of the bridgeless topology is the simple control. The operation of the bridgeless PFC in different states is presented in Figure 8. (Chellappan Salil, 2018)

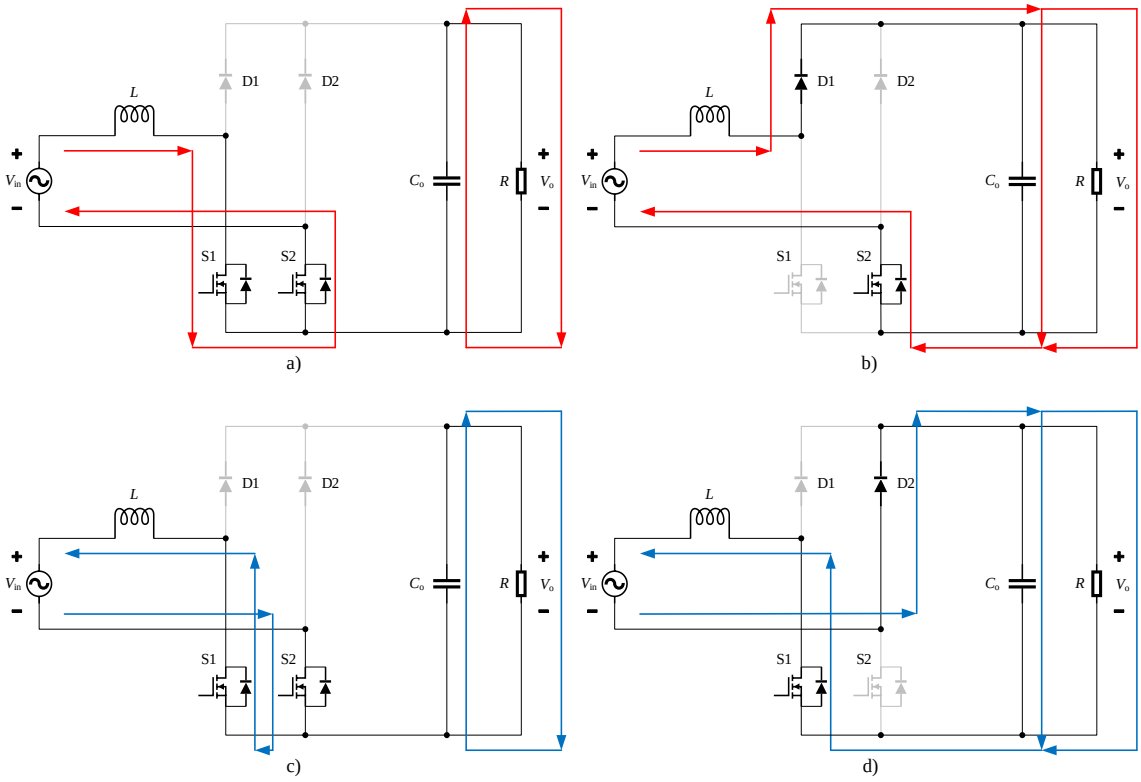

Figure 8 Operating modes of bridgeless boost PFC in positive half cycle (a, b) and negative half cycle (c, d).

In its attempt to address the diode bridge losses, bridgeless PFC topology introduces other problems, such as increased Electromagnetic Interference (EMI). The main drawback of the bridgeless PFC topology is the significant common mode noise, often offsetting any other benefits gained using the topology. Current sensing for control is also more difficult. (Brent et al. 2020, 15)

2.2.3 Semi-bridgeless PFC

To address the EMI and common mode noise problem in the previously presented bridgeless topology, two slow diodes are added to the input. However, this also requires adding an additional boost inductor to the circuit. Semi-bridgeless PFC, also known as dual boost PFC topology, is presented in Figure 9.

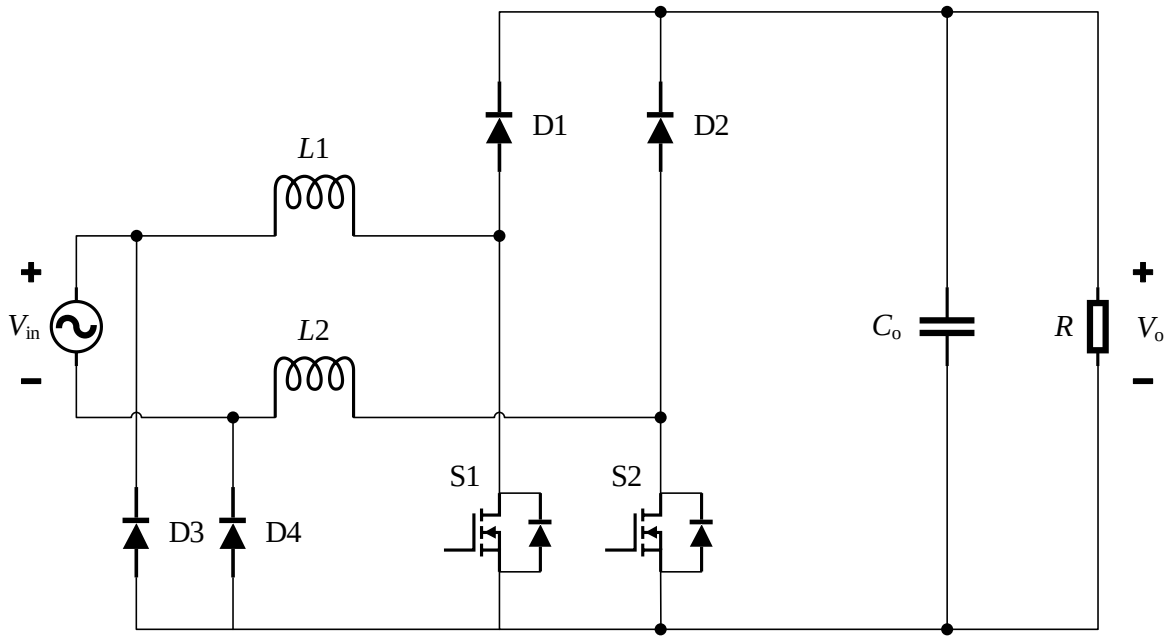

Figure 9 Semi-bridgeless boost PFC converter.

Instead of the body diodes of S1 and S2 diodes D3 and D4 are used for the current return path. The main inductor is split into two equal sized inductors, one for each half cycle. Both inductors need to be same size as a single inductor in the previously presented traditional or bridgeless topologies, doubling the amount of space inductors take. The operation of semi-bridgeless PFC is presented in Figure 10.

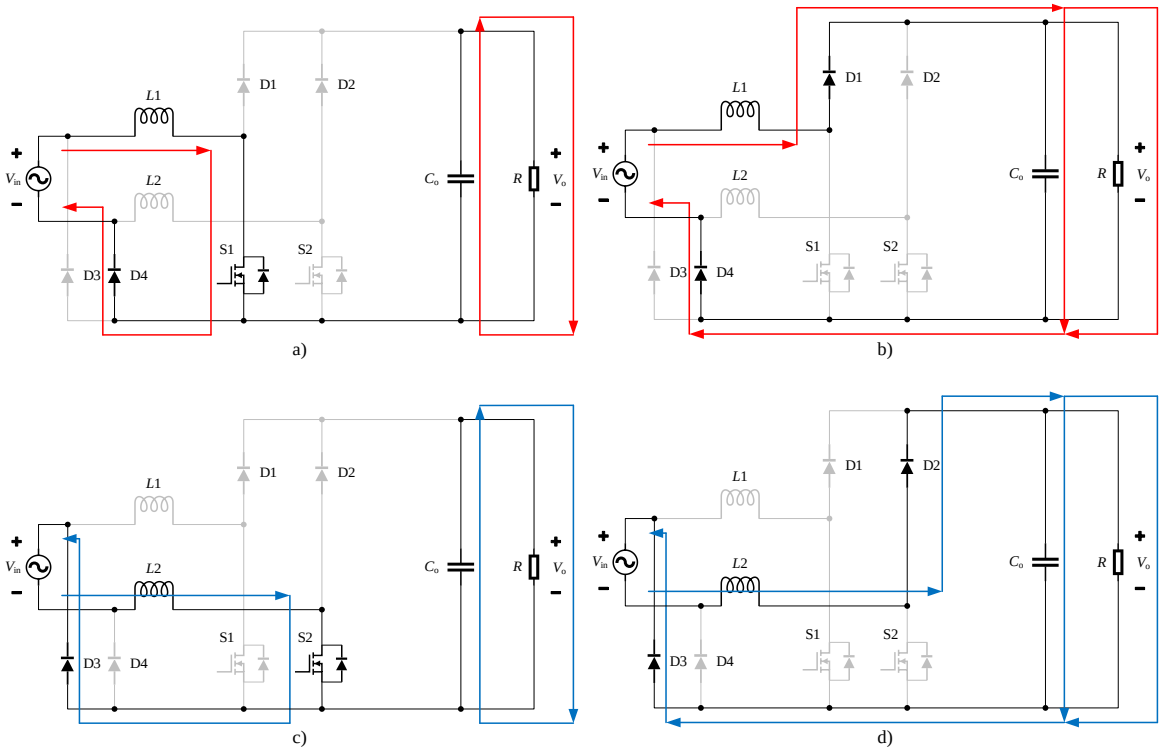

Figure 10 Operating modes of semi-bridgeless PFC in positive half cycle (a, b) and negative half cycle (c, d).

While eliminating the common mode noise and reducing EMI, the semi-bridgeless topology does a poor job of component utilization. While the number of components in the current path remain the same as with regular bridgeless topology, the total number of components increases, reducing power density and increasing price. (Chellappan Salil, 2018, 2)

2.2.4 Totem-pole PFC converter

A totem-pole converter is a modification of the basic bridgeless boost-PFC topology. In totem-pole topology D1 and S2 switch places, moving the switch on top of the other, hence the name totem-pole. A totem-pole PFC converter is presented in Figure 11.

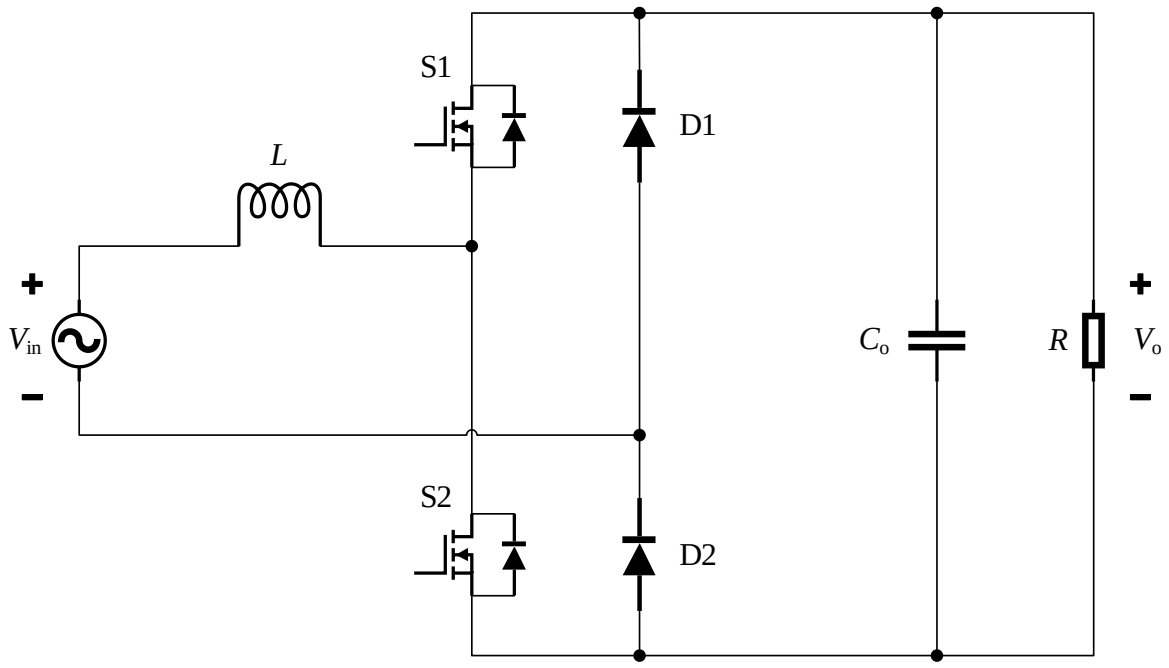

Figure 11 Totem-pole PFC converter with diode line rectification.

During positive half cycle, S2 is closed when charging inductor while S1 remains open. When supplying the load, S2 opens and S1 closes. D2 is the current return path during positive half cycle. During negative half cycle, the components work oppositely. S1 is closed and S2 is open when charging inductor, whereas S2 is closed and S1 open when supplying the load. D1 is the return path, as the current goes through it before the switches.

To further improve efficiency, the slow diodes D1 and D2 can be replaced with active switches such as Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFET). Such topology is presented in Figure 12.

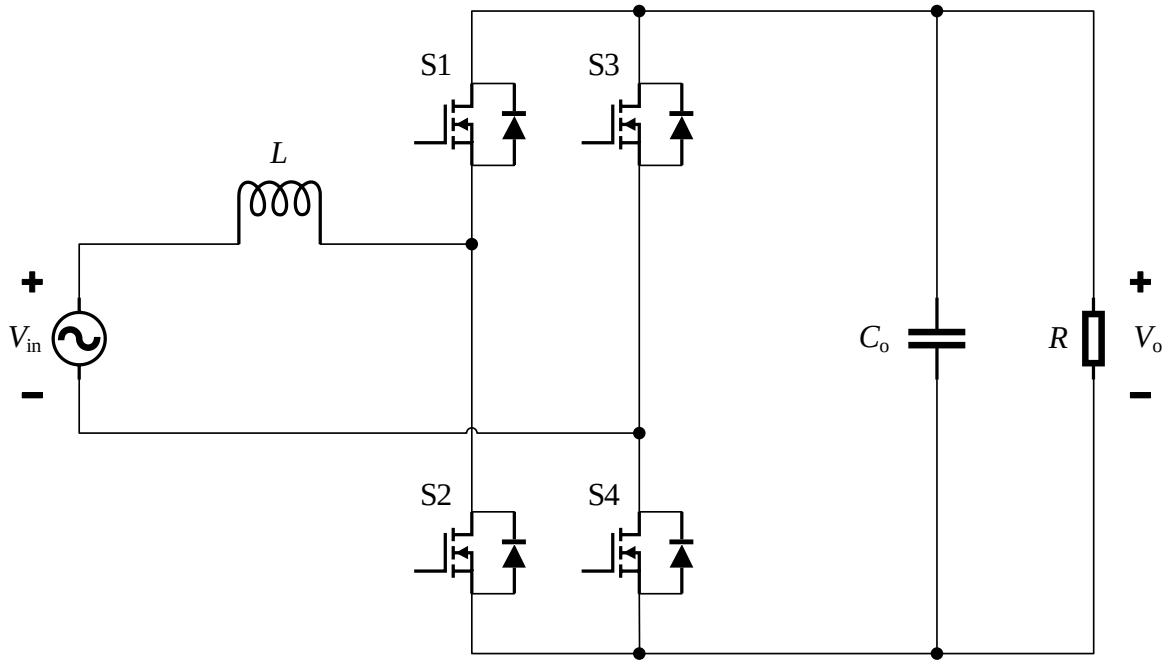

Figure 12 Totem-pole PFC with MOSFET line rectification.

The MOSFET line rectified totem-pole operates in same manner as diode rectified. S3 and S4 both operate in their respective AC half cycles, S4 during positive, and S3 during negative. The operation of totem-pole converter with MOSFET line rectification is illustrated in Figure 13.

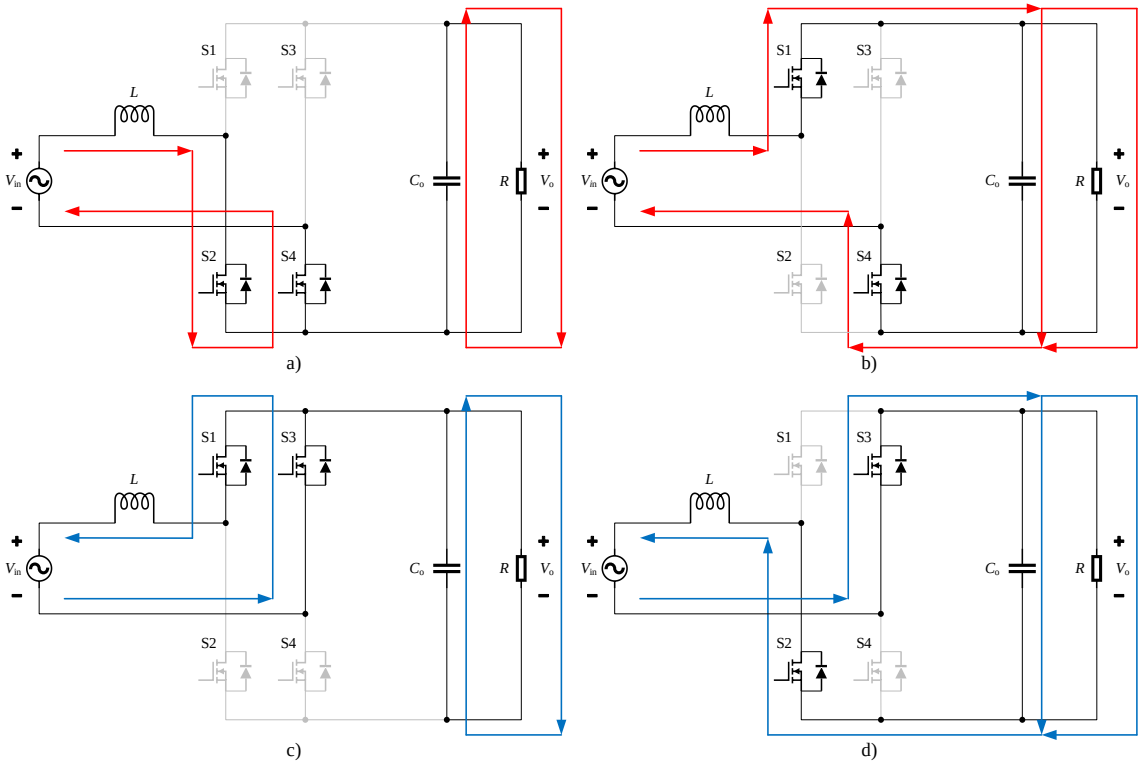

Figure 13 Operating modes of totem-pole PFC in positive half cycle (a, b) and negative half cycle (c, d).

To illustrate the operation of totem-pole further, gate signals of the switches are plotted in Figure 14 for one AC cycle, with duty cycle variations of S1 and S2 in red. The figure is only illustrative, as it portrays a case of extremely low switching frequency.

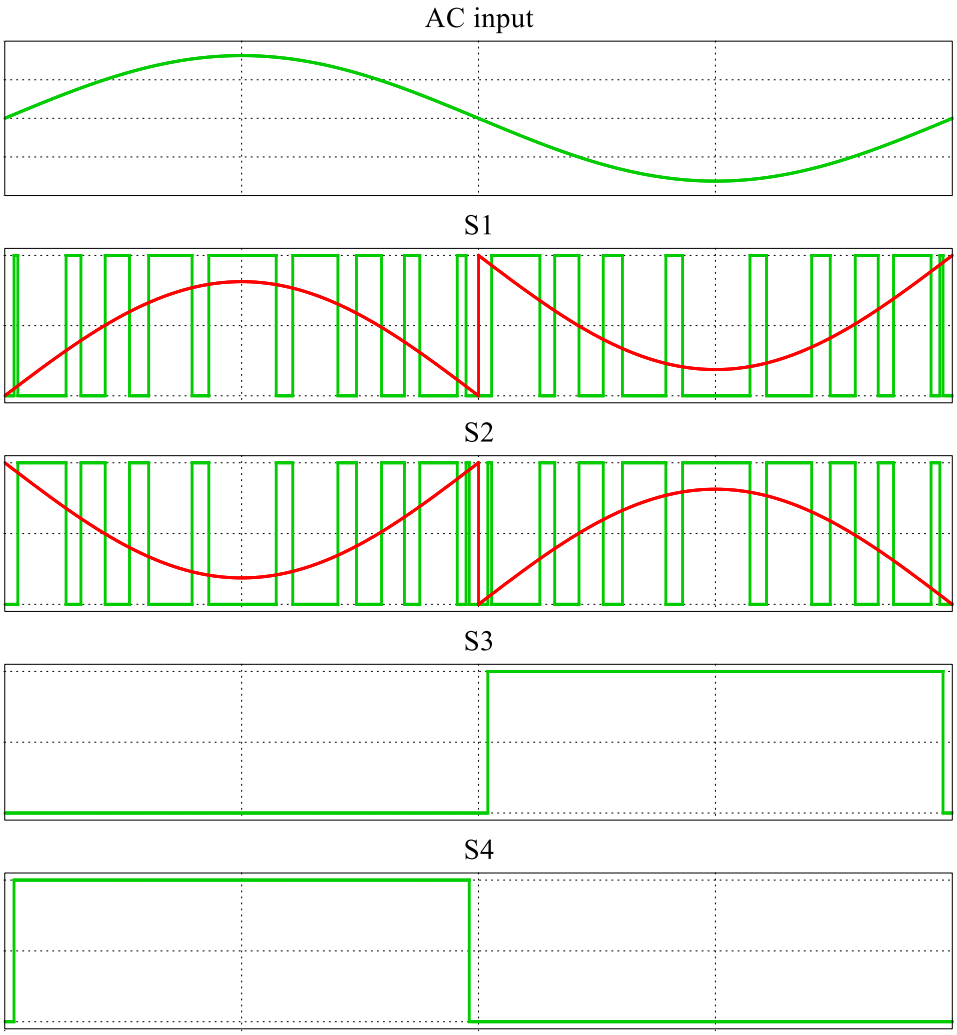

Figure 14 Illustrative picture of totem-pole PFC gate signals.

The totem-pole topology does an excellent job of component utilization, while eliminating the losses in the rectifier bridge. Despite its advantages the totem-pole topology has issues of its own that need addressing. Control for the totem-pole is relatively complex, and it is generally stricter on semiconductor selection due to the way the current flows. The reverse recovery of the fast switches body diodes causes excessive losses without proper attention. However, with advancements in semiconductor technology, namely the coming of Wide-Bandgap Semiconductors (WBG) and their zero reverse recovery charge, totem-pole has gained significant interested. (Chellappan Salil, 2018) (Brent et al. 2020)

2.3 Hard switching vs soft switching

A main part in a power converter design is the analysis of switching transition behaviour of transistors, as a significant amount of the losses occur during switching. The switching behaviour also influences the EMI behaviour of the device. (Edmunds Mark)

Hard switching occurs, when there is an overlap of current and voltage during the switching period of the transistor. When there is both current and voltage, power dissipation during switching occurs, decreasing the efficiency of the converter. A demonstrative figure of hard switching is presented in Figure 15. (Edmunds Mark)

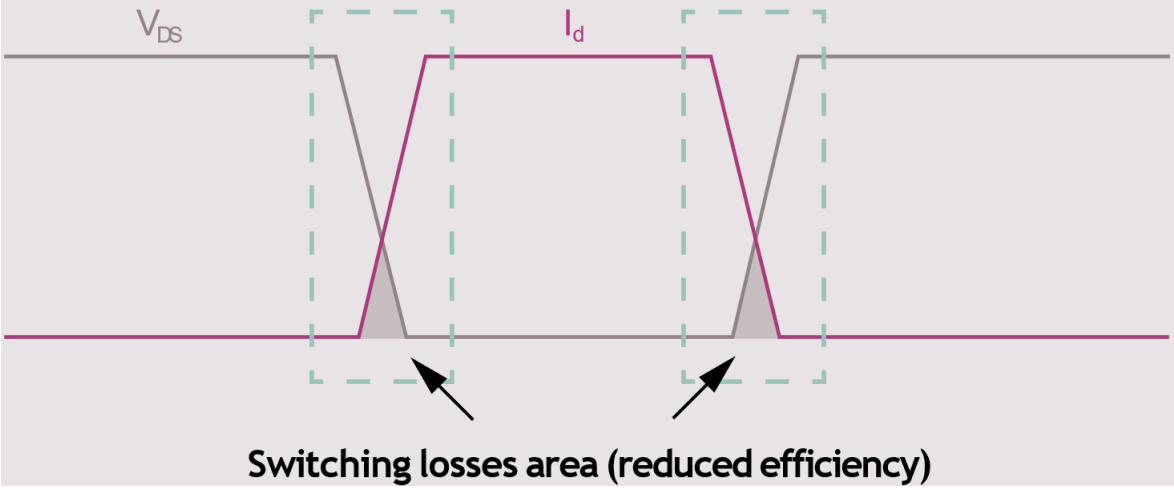

Figure 15 Hard switching MOSFET current and voltage waveform. (Infineon Technologies, 2019, 4)

Soft switching on the other hand occurs when there is no current or voltage when the switching starts. Soft switching greatly reduces the power losses in the main switching power transistor. A figure of soft switching is illustrated in Figure 16. (Edmunds Mark)

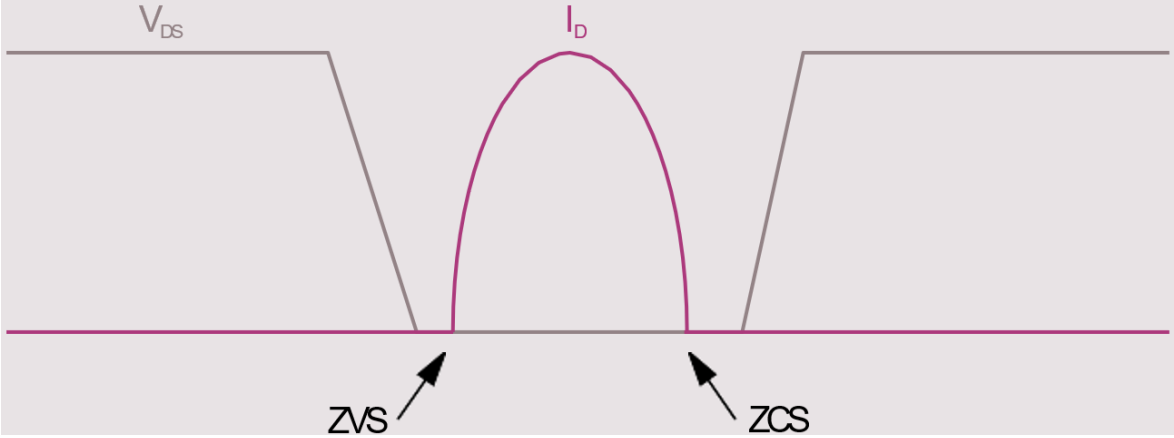

Figure 16 Soft switching MOSFET current and voltage waveform. (Infineon Technologies, 2019, 5)

Soft switching is generally desirable when possible. Not only is there an increase in energy efficiency, but also better EMI performance. The increased thermal performance can also increase the longevity of power components. (Edmunds Mark)

2.4 PFC conduction modes

Conduction modes of a PFC converter are usually divided into three main modes depending on the way the inductor current is controlled. The selection of the conduction strategy depends on the specific application, as each of the modes have their own advantages and disadvantages.

2.4.1 Continuous Conduction Mode

In CCM the inductor current doesn’t drop to zero, and current is continuously flowing through the inductor. In a PFC circuit the boosting switch turns on before the current reaches zero. CCM utilizes constant switching frequency, making control simpler. Figure 17 shows an example of CCM operation current waveform in blue and input line current in red.

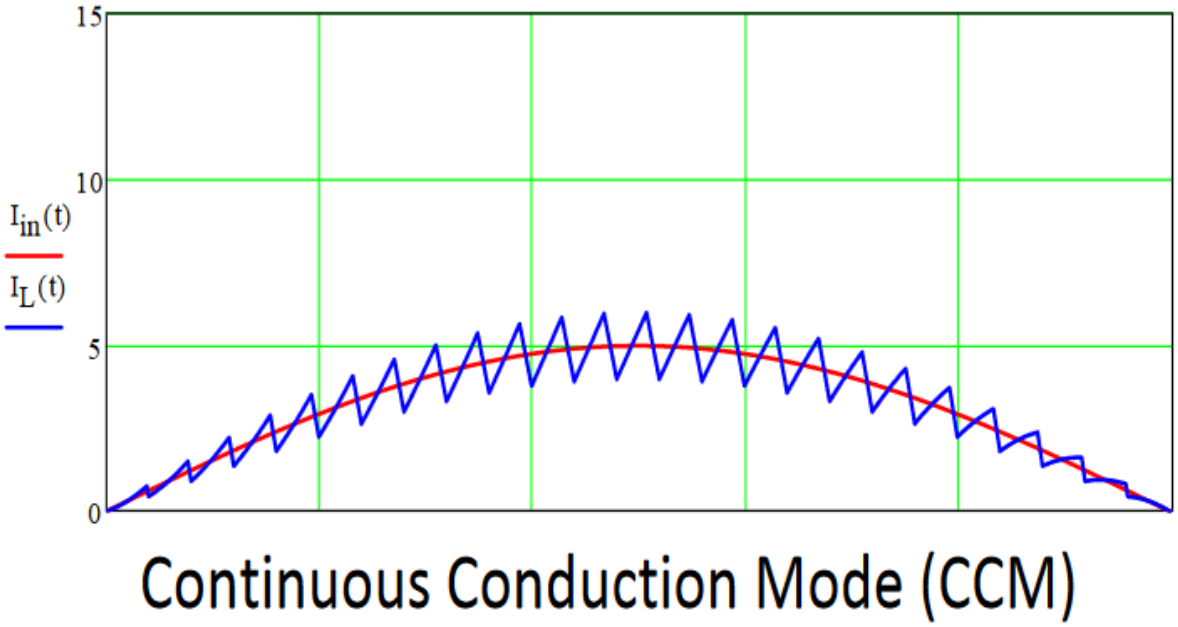

Figure 17 CCM waveform. (Abdel-Rahman Sam et al. 2016, 3)

Out of the conduction modes, CCM has the smallest peak and ripple current, meaning it has the smallest conduction losses. Turn-off losses are generally lower than on other conduction modes, as the inductor current during turn-off is lower. On the contrary, CCM has high turn-on losses, as current is conducting during turn-on. CCM operation is generally favourable and used in higher power applications. (Abdel-Rahman Sam et al. 2016, 2-3) (Toshiba, 2019, 8-11)

2.4.2 Discontinuous Conduction Mode

In Discontinuous Conduction Mode (DCM) the current in the inductor is allowed to drop to zero for some time during the switching cycle. In Figure 18 is presented the waveform of DCM with the exact same voltage and power conditions as in figure 17.

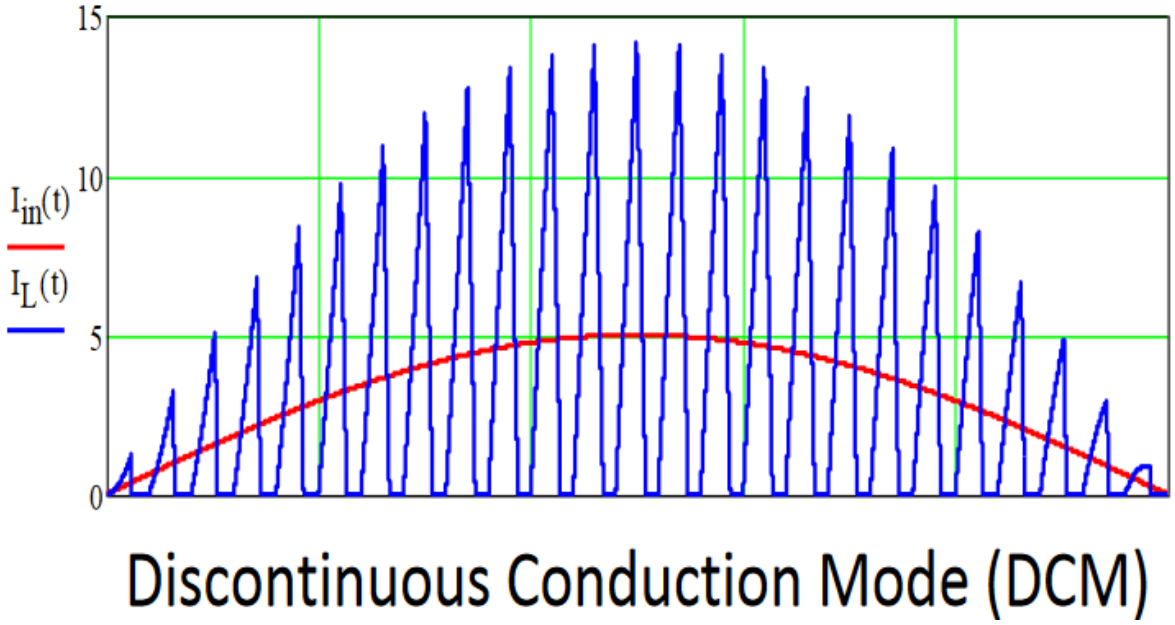

Figure 18 DCM waveform. (Abdel-Rahman Sam et al. 2016, 3)

DCM has the highest current peak and ripple. The advantage of the mode is that turn-on losses are reduced in respect to CCM. The control is also simple. DCM is generally favourable only for low (<100 W) power applications. (Abdel-Rahman Sam et al. 2016, 2) (Toshiba, 2019, 10-11)

2.4.3 Critical Conduction Mode

CrCM, also found in literature as boundary conduction mode or transition mode, is the boundary between CCM and DCM, where the current is controlled to stay between the upper boundary and zero, but never to stay on zero current. When the inductor current reaches zero, the boost switch is instantaneously turned on to energize the inductor. In Figure 18 is shown CrCM operation with the same voltage and power conditions as in figures 17 and 18.

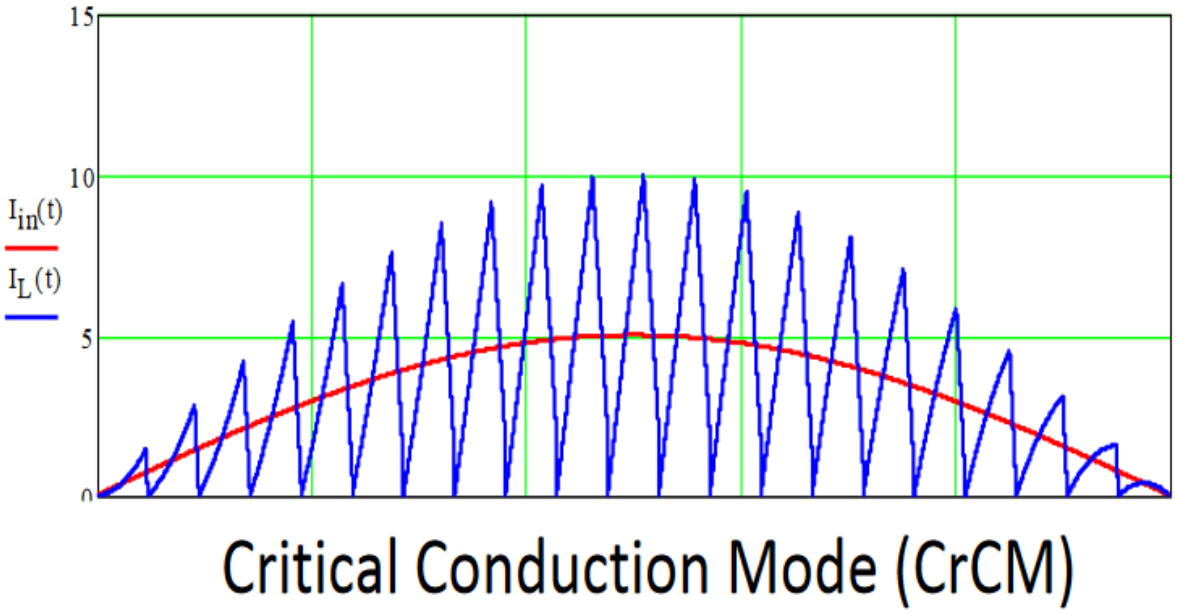

Figure 19 CrCM waveform. (Abdel-Rahman Sam et al. 2016, 3)

In CrCM operation the peak ripple current is always 2 times the average input current, meaning that the ripple is higher than in CCM operation but lower than in DCM operation. Compared to CCM operation, CrCM has higher RMS current and turn-off current. On the contrary, CrCM offers the possibility of Zero Voltage Switching (ZVS) and reduced switching losses when $V_{in} < V_o/2$ (H. Zhou, W. Liu and E. Persson, 2016). With CrCM switching frequency is variable.

At low to medium power levels CrCM is the desired mode of operation, as it offers potentional improvements in efficiency and power density. At higher power applications CCM is the preferred mode, however. (Abdel-Rahman Sam et al. 2016, 2-3) (Toshiba, 2019, 8-11)

2.4.4 Triangular Current Mode

TCM is very similar to CrCM. The difference is that in TCM, certain negative current is allowed through the inductor to overcome the limitation in CrCM and allow for ZVS

operation for the entire mains period (H. Zhou et al, 2016). TCM operation for a full AC cycle in presented in Figure 20.

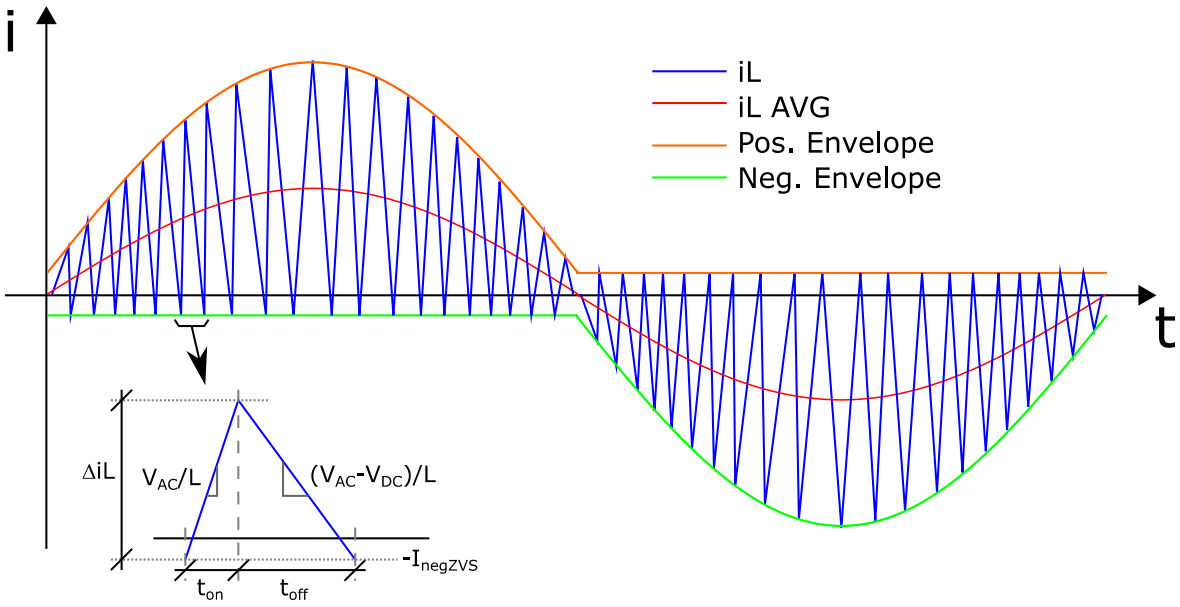

Figure 20 TCM waveform.

As with CrCM, TCM peak ripple needs to be twice the amplitude of average input current. In addition of that, the peak current amplitude also needs to compensate for the introduced negative current I_{negZVS}.

$$iL_{\text{pk}} = iL_{\text{avg}} \cdot 2 + \left|I_{\text{negZVS}}\right| \tag{8}$$

As in CrCM, when the boost switch is on inductor current rises linearly since the input voltage is applied, and the current ripple can be expressed as

$$\Delta iL = \frac{V_{\text{in}}}{L} \cdot t_{\text{on}} \tag{9}$$

When the switch turns off, inductor current decreases and current ripple can be expressed as

$$\Delta iL = \frac{V_{\text{in}} - V_{\text{o}}}{L} \cdot t_{\text{off}} \tag{10}$$

The same equations are also presented in Figure 19 on bottom left, which illustrates a single switching cycle inside the mains cycle. Like with CrCM, in TCM operation switching

frequency is variable. The switching frequency f_{sw} in both modes can be calculated using (9) and (10) and is given as

$$f_{sw} = \frac{V_{in} \cdot (V_o - V_{in})}{V_o \cdot L \cdot \Delta iL} \quad (11)$$

Figure 21 illustrates the f_{sw} waveforms of CrCM and TCM modes. Grey is TCM and red is CrCM.

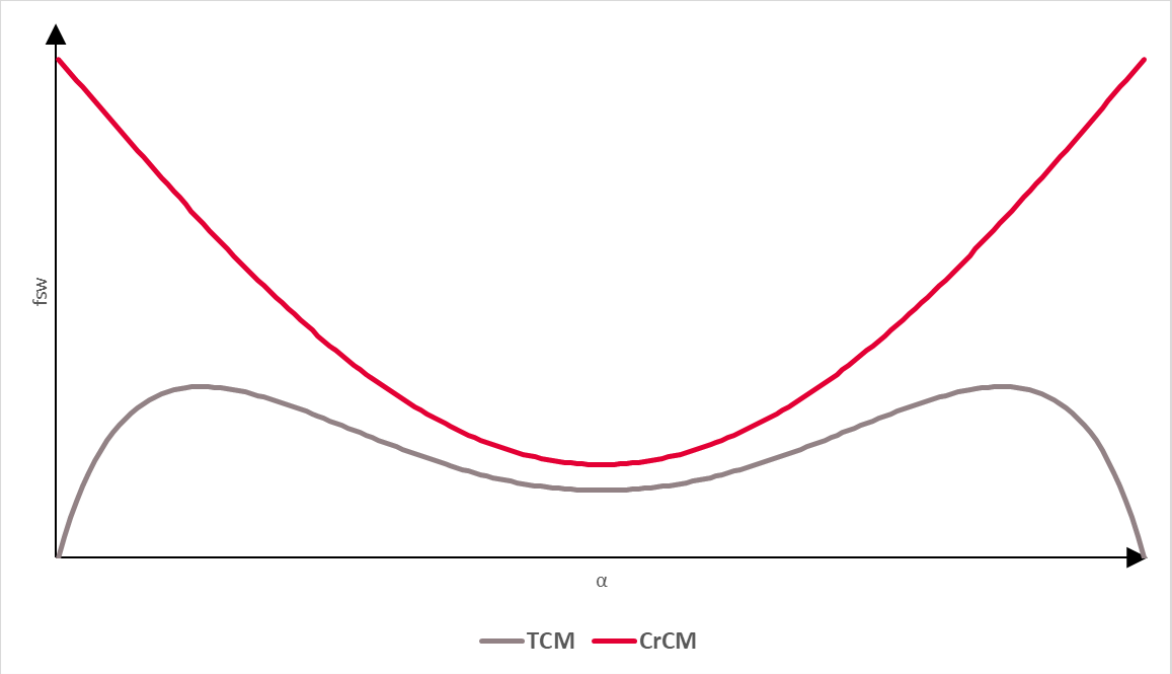

Figure 21 TCM vs. CrCM waveforms.

For the same conditions CrCM f_{sw} is higher, as with CrCM there is no added valley current to the total inductor ripple current. When input voltage is close to zero, CrCM has very high f_{sw}, as the inductor ripple current ΔiL is very small. With TCM operation this is not the case, as there will always be at least the ripple current associated with valley envelope.

3 PFC totem-pole operation and design

The main driving factor in power supply market is high electrical efficiency, however high power density is usually of great interest as well. The efficiency and power density of the device greatly depends on the topology, selected power devices and control strategy. Pursuit for higher power density may have trade off as lower electrical efficiency and vice versa, and the balancing of power density and energy efficiency is an eternal challenge for the designers.

With advancements in semiconductor technology the totem-pole topology has gained interest. Traditionally Silicon (Si) MOSFETs combined with the traditional boost PFC topology has been the most mature technology. With the emerging WBG like Silicon Carbide (SiC) and Gallium Nitride (GaN) transistors and their improved performance and characteristics over traditional Si transistors, designers can overcome the previous considerations and limitations concerning totem-pole topology. In Figure 22 is presented a comparison of the technologies in relation to their switching frequency and application output power. (Q. Huang, A. Q. Huang, 2017)

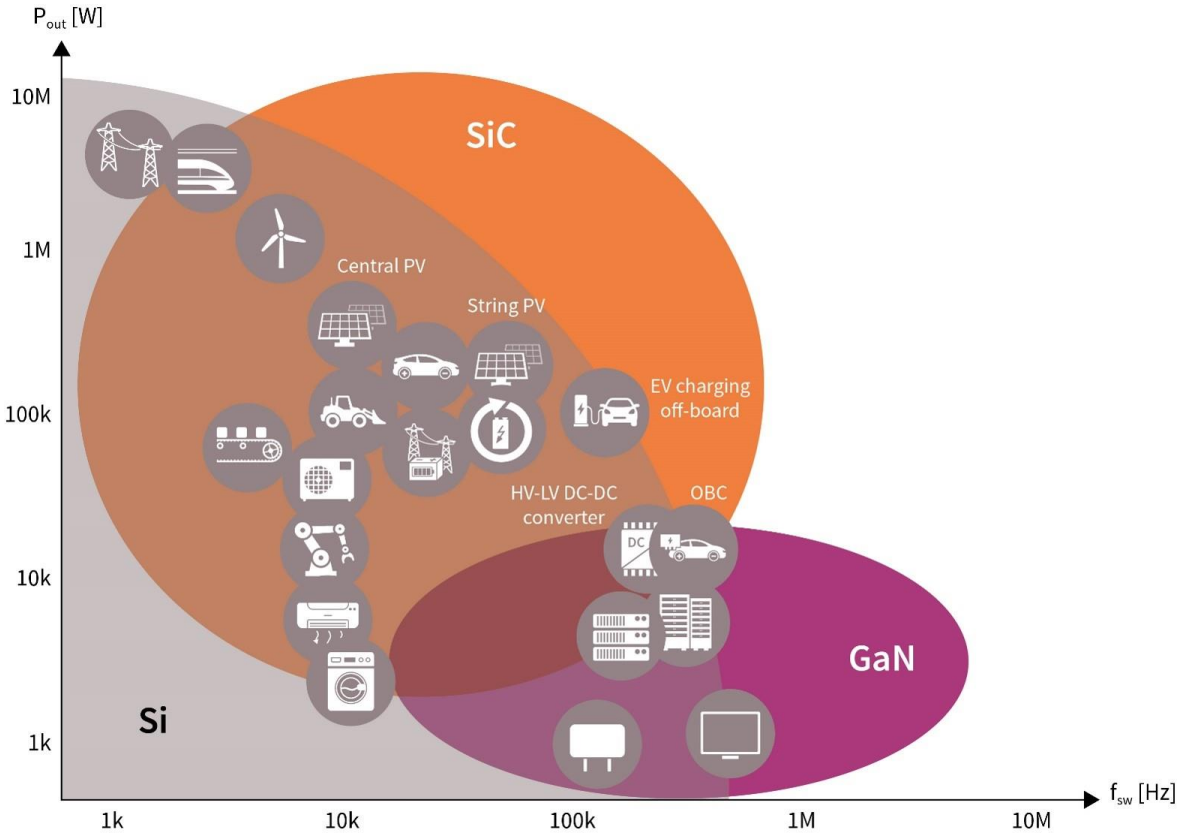

Figure 22 Comparison of Si, SiC and GaN technologies. (Infineon Technologies, b)

With traditional Si MOSFETs and CCM operation the reverse recovery Q_{rr} and output charge Q_{oss} that occur during switching transitions are a major issue for totem-pole topology. They are not only a major source of losses but entirely prevent the operation of totem-pole in CCM, as a single hard switching event could potentially destroy the transistor. If totem-pole topology is used with Si devices, soft switching operation is mandatory. (Q. Huang et al. 2017)

With GaN devices and their zero reverse recovery loss, the totem-pole can even be used under hard switching CCM operation. ZVS soft switching operating is still beneficial though, as turn-on losses related to energy stored in the output capacitance E_{oss} can be avoided. (Q. Huang et al. 2017)

As TCM operation allows for minimal switching losses, combined with the improved characteristics of GaN devices, higher switching frequencies can be pursued. Increasing switching frequency is one of the most straightforward ways to increase the power density of the converter. For example, consider the design equation for the inductance of boost converter.

$$L = \frac{V_{\text{in}} \cdot (V_{\text{o}} - V_{\text{in}})}{\Delta iL \cdot f_{\text{sw}} \cdot V_{\text{o}}} \quad (12)$$

The required inductance is inversely proportional to the switching frequency. Thus, increasing the switching frequency reduces the required inductance, which in turn allows for smaller inductor, potentially increasing the power density of the application.

3.1 TCM control implementation

A simple way to operate TCM totem-pole is hysteresis current control. In hysteresis current control, the inductor current is kept between the hysteresis references or envelopes. Switching frequency is variable, as that is the inherent behaviour of TCM.

In Figure 23 is presented a simplified control block diagram of the hysteresis current controlled TCM totem-pole. The reference for the average current of inductor is done by comparing the output voltage to the set reference voltage and feeding the error to the voltage regulator. The output of the voltage loop is combined with the AC voltage and RMS feedforward value of the input voltage to generate the average value of inductor current. By multiplying the average current by 2 and adding the set valley switching, the peak envelope for the hysteresis controller is generated, as indicated by (8).

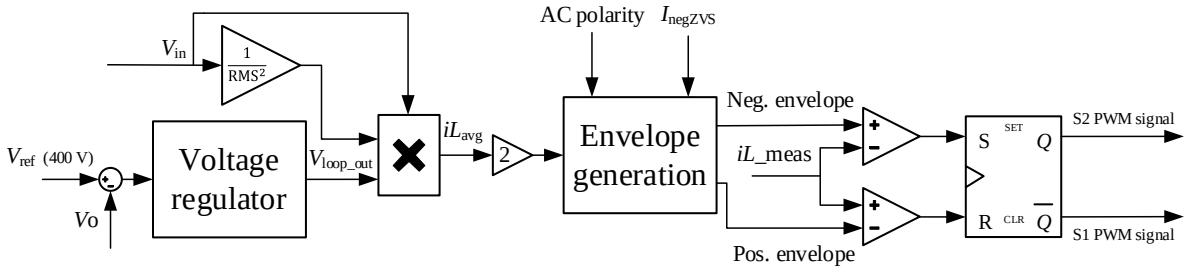

Figure 23 Simplified control block diagram of hysteresis current controlled TCM totem-pole.

As is presented in figure 23, the positive and negative envelope generation depends on the AC polarity, hence AC polarity information is needed for the envelope generation. Assuming a constant load, the envelopes are mirrored copies of each other. During positive half cycle, the positive envelope is the sinusoidal reference generated by the voltage loop output, feedforward input voltage and AC voltage and the negative envelope is the set valley value. The opposite is true for negative half cycle.

The measured inductor current *iL*_meas is compared to the generated envelopes with comparators. Finally, the PWM pulses for the switches are generated using Set-Reset (SR) flip-flop. During AC zero crossing, all switches are turned off for certain period for simplicity and robustness.

3.2 Simulation

To study the behaviour of PFC totem-pole with the selected control strategy a simplified simulation model of it was created in Piecewise Linear Electrical Circuit Simulation PLECS®. PLECS is software that is mainly focused on simulating power electronics (Plexim). The simulation model is presented in Figure 24.

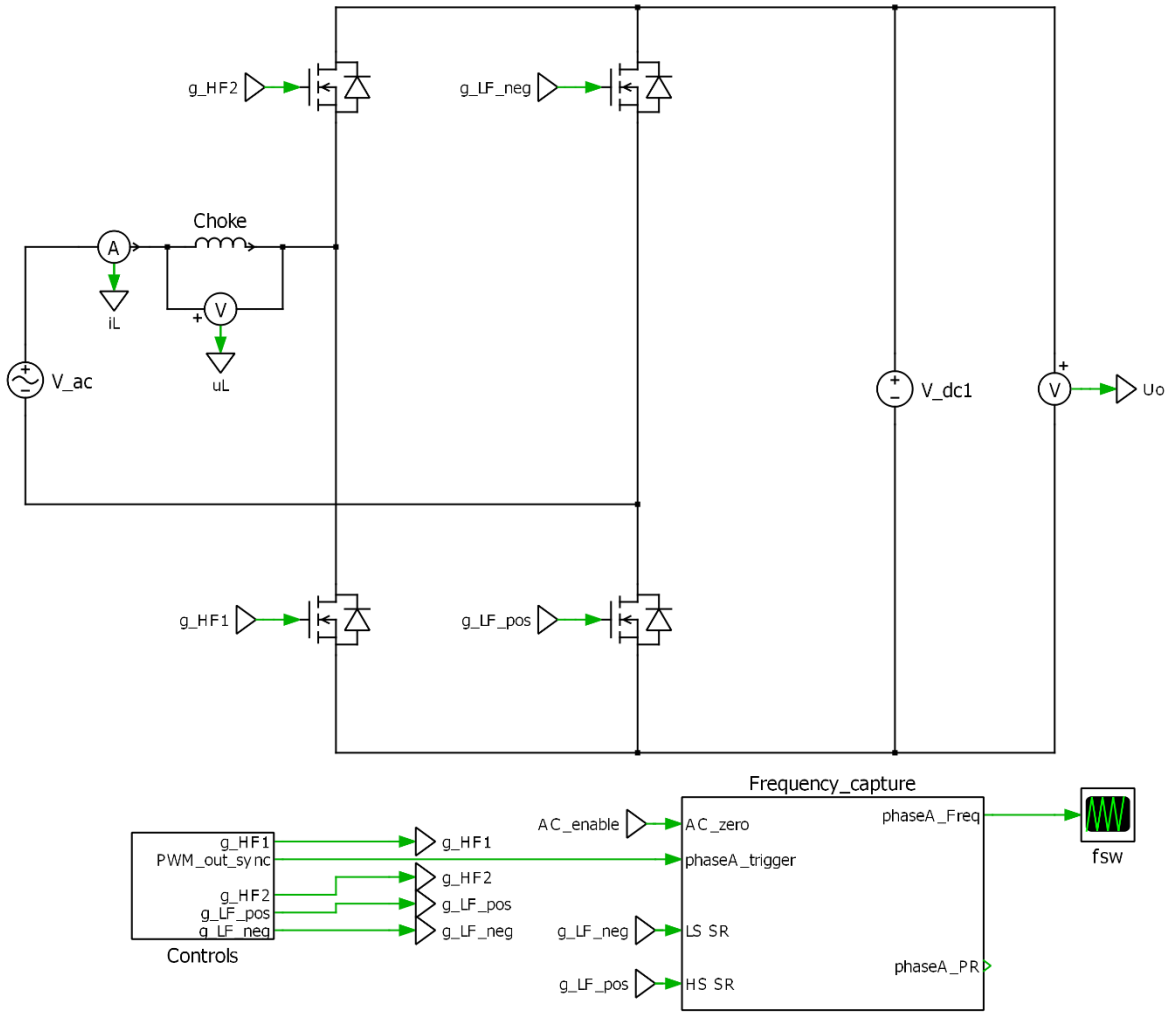

Figure 24 Simplified PLECS model of TCM PFC totem-pole.

The topology of the model is the same as presented in Figure 12, with the output capacitor and load replaced with DC voltage source for idealized voltage loop behaviour, as the goal of the simulation is to study the current control and effects of inductance in switching frequency. The frequency capture subsystem is used to measure the switching frequency of the system. More details of "Controls" block are introduced in Appendix 1, that work as explained in 3.1 and Figure 23. The difference is that since there is no voltage loop V_{loop_out}, a proportional value of the input AC voltage is used as current reference to generate desirable iL_{avg} value.

To demonstrate the operation of the simulation an unrealistically high value of 20 mH is used for the choke for low switching frequency. The rest of the simulation parameters are presented in Table 1, where L is the inductance of the choke and I_{negZVS} is the applied valley current, and $iL_{\mathrm{avg\_pk}}$ is the peak value of the average inductor current. The peak value for the average current is calculated as

$$iL_{\mathrm{avg\_pk}} = \sqrt{2} \cdot \frac{P_{\mathrm{o}}}{V_{\mathrm{in}}} \tag{13}$$

Table 1 Parameters of the simulation.

L (mH)	I_{negZVS} (A)	V_{in} (V)	V_{o} (V)	P_{o} (W)	$iL_{\mathrm{avg\_pk}}$ (A)
20	1	230	400	210	1.291

In Figure 25 is presented hysteresis envelopes and average current generated by the controls, and the inductor current, that resemble to already presented waveforms in Figure 20.

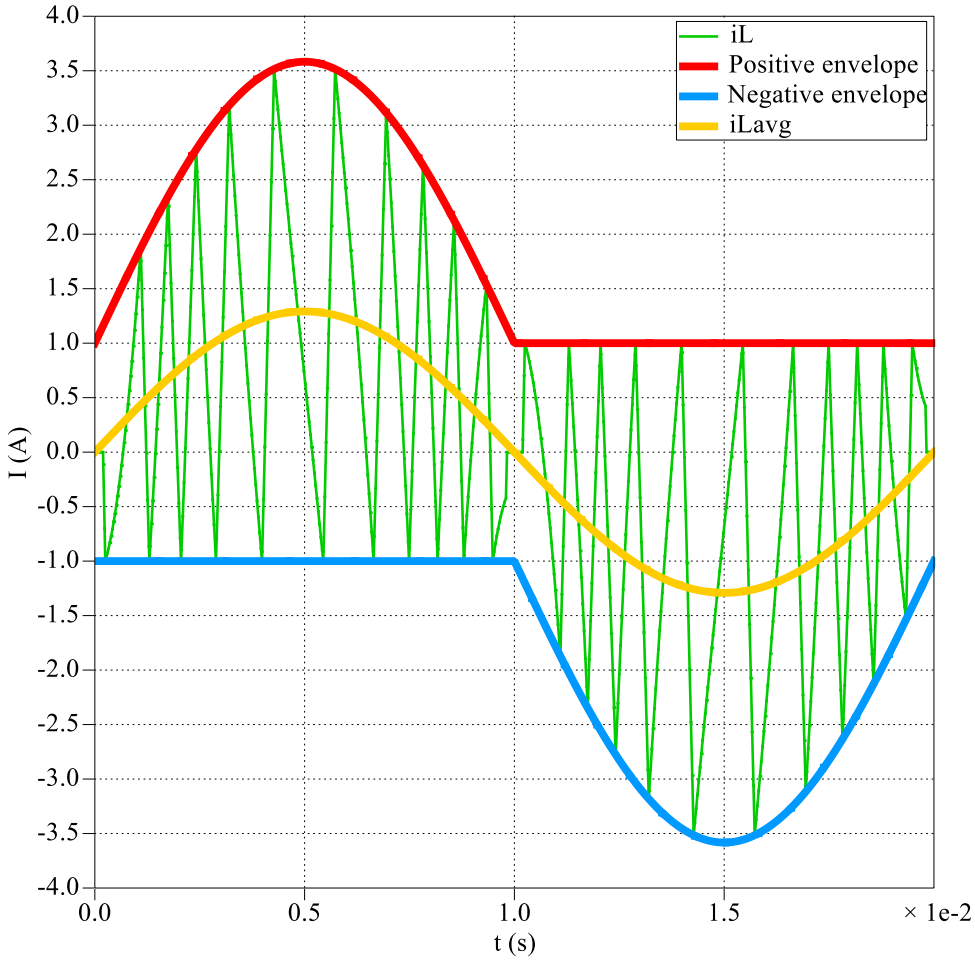

Figure 25 Simulated hysteresis current control of totem-pole.

As is evident from the simulation, the inductor current is kept between the hysteresis envelopes, and the peak inductor current is the same as calculated with (8). To further illustrate the operation of totem-pole, PWM signals and currents of High Frequency (HF) switches are shown in Figure 26 for the positive AC cycle.

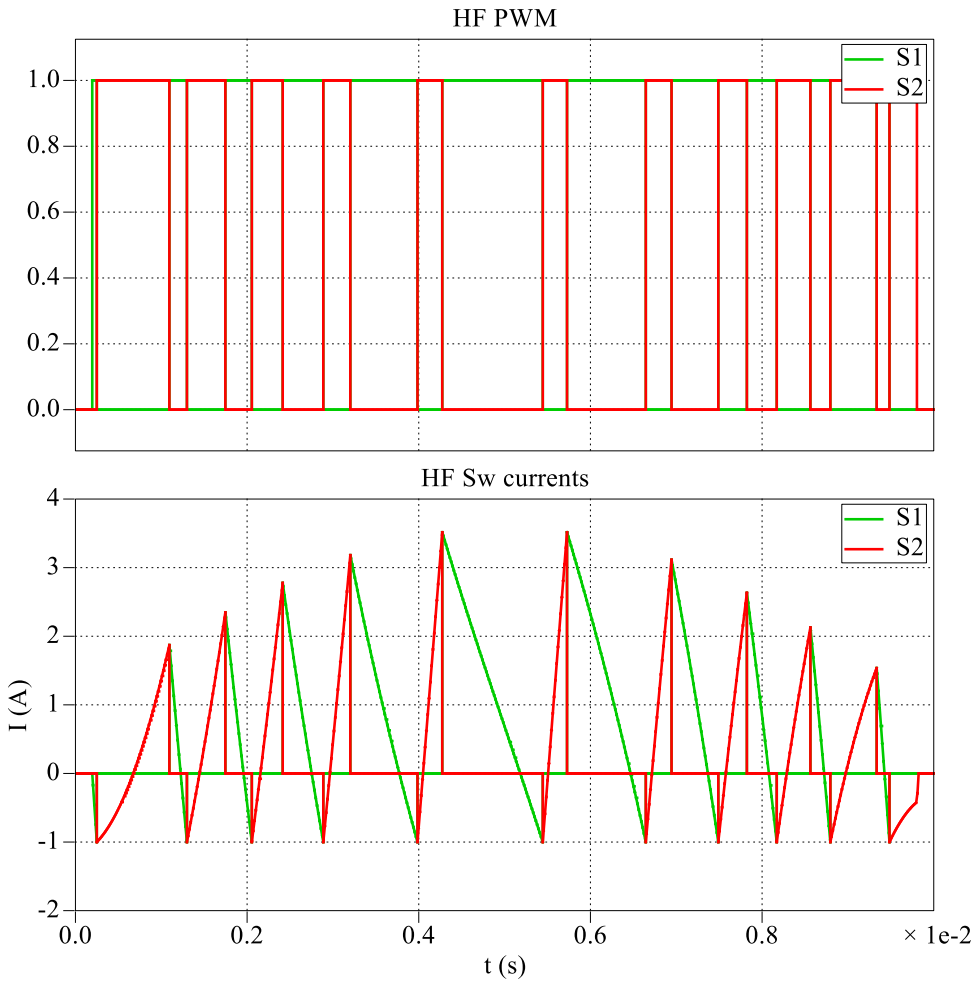

Figure 26 Simulated PWM signals and currents of HF switches for positive half cycle.

The behaviour is as explained in 2.2.4. When S1 is conducting, the inductor is being discharged to feed the load. When S2 is conducting, the inductor is being charged.

In the actual implementation, much higher switching frequency is required for high power density. The frequency capture unit is not readily available block from PLECS library, but instead a relatively complex user made measurement unit. For the simulation of the actual system, inductance value of 100 μH is used, with the rest of parameters same as in table 1. In Figure 27 is presented the hysteresis control and inductor current for positive AC half cycle.

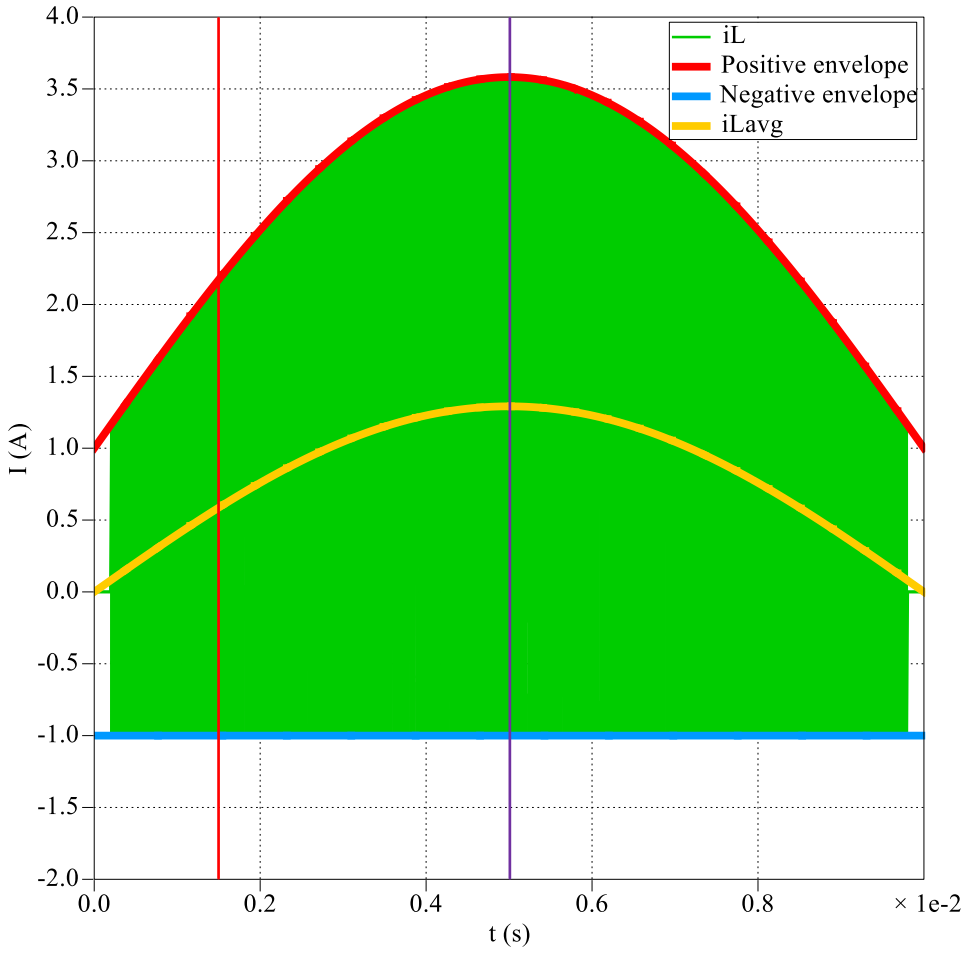

Figure 27 Simulated hysteresis current control of totem-pole with L of 100 µH.

As is visible from the simulation, the changes in inductor current are rapid due to the much lower inductance, which in turn leads to higher f_{sw}. To get a better view of the current change a zoomed view is presented in Figure 28 between time intervals 0.00148 s < t < 0.00152 s marked as vertical red line and 0.00498 s < t < 0.00502 s, marked as purple line in the previous figure. During the first time interval peak f_{sw} is expected with selected simulation parameters.

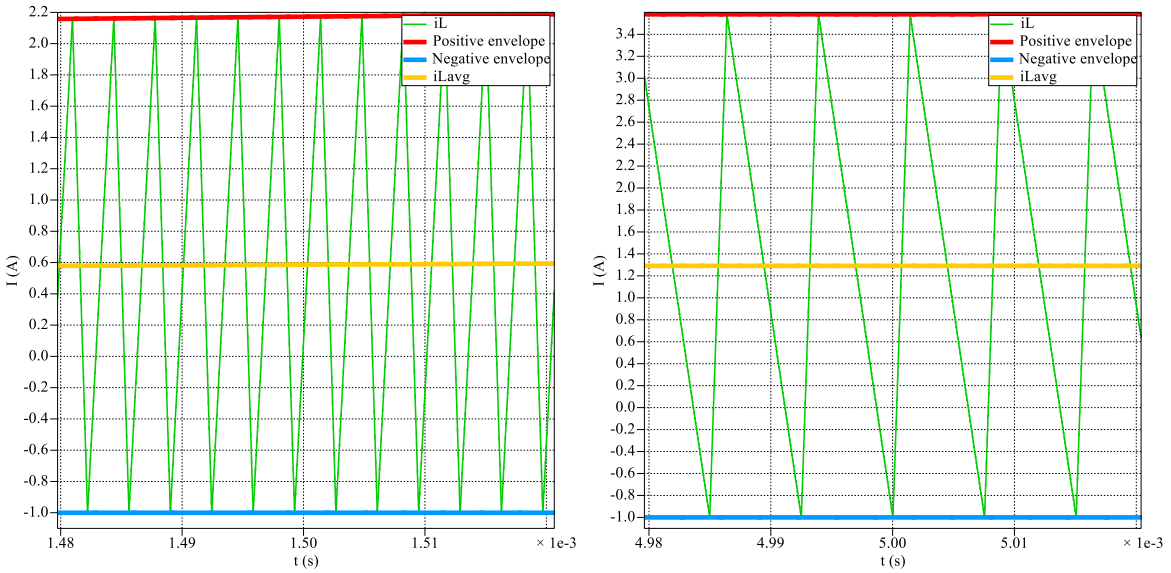

Figure 28 Simulated hysteresis current control of totem-pole with L of 100 µH between (left) 0.00148 s < t < 0.00152 s and (right) 0.00498 s < t < 0.00502 s.

As is visible from the simulation f_{sw} is much higher during the first interval. By taking the Δt between 2 switching occurrences for one switch, it is possible to calculate f_{sw}, which is done by the frequency capture unit in the simulation. Δt for the first interval is 3.4 µs and 7.52 µs for the second. By taking the reciprocal number of Δt, f_{sw} is obtained. F_{sw} during the first time interval is 294 kHz and 133 kHz during the second. In Figure 29 is presented switching frequency captured by the frequency capture unit for 100 µH, 1 A valley. A comparison with 30 µH and 1.5 negative valley is presented in the same figure.

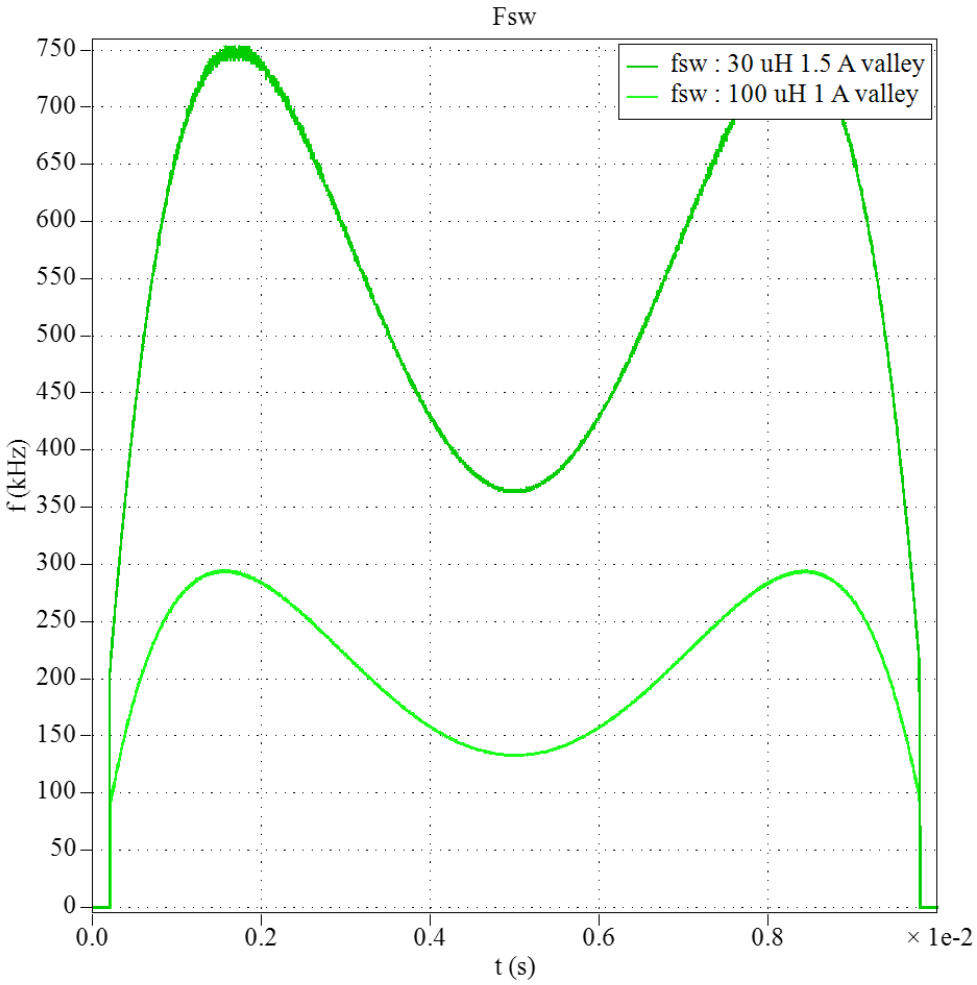

Figure 29 Simulated switching frequency of totem-pole with *L* of 100 µH 1 A valley and 30 µH and 1.5 A valley.

As is visible from the figure, the frequency capture unit outputs the same kind of values that were manually calculated using the detailed simulation data in Figure 28. F_{sw} is continuously variable, and with lower inductance f_{sw} is significantly higher, even with the increased valley current.

4 Implementation

The core goal of the work is to research the feasibility of high switching frequency with the XMC1400 microcontroller for TCM operation. The XMC1400 controller is used on an existing prototype totem-pole device with IGI60F140A1L GaN switches for HF bridge leg and IPL60R065P7 for line rectification. The pursuit for good energy efficiency and high power density were also points of great interest during the design. In this chapter the design for the inductor of the 210 W TCM totem-pole is presented.

Generally, it is desirable to design a power converter in a way that the same unit can work in universal range regardless of AC voltages and frequency. Even when totally ignoring control aspect, a power converter designed for 230 V 50 Hz grid voltage may not work at different line voltage or frequency. In this work the focus is on design for 230 V 50 Hz grid as nominal condition, referred as high line, with 85 V 60 Hz as a secondary consideration, referred as low line. The maximum output power is 210 W and output voltage 400 V.

4.1 Switching frequency

As discussed with TCM operation f_{sw} is variable according to (11). As the main grid voltage V_{in} is fixed and V_o is usually a given requirement for an application that the converter is feeding, that only leaves inductance L and inductor ripple current ΔiL as degrees of freedom to control the switching frequency range. As f_{sw} is inversely affected by L and ΔiL, decreasing either value will increase f_{sw} and vice versa. As known from (8), inductor ripple current can be controlled to an extent by changing the value of valley current.

With the goal of up to 1 MHz f_{sw} for nominal input voltage, initial specification for inductance was set at around 30-50 µH and 1-2 A valley. Figure 30 shows the expected switching frequency for 30 µH inductance with 1.5 A during high line positive half cycle

using (11). Unless otherwise specified, all figures are shown only for positive high line half cycle, however f_{sw} graphs are the same regardless of AC polarity.

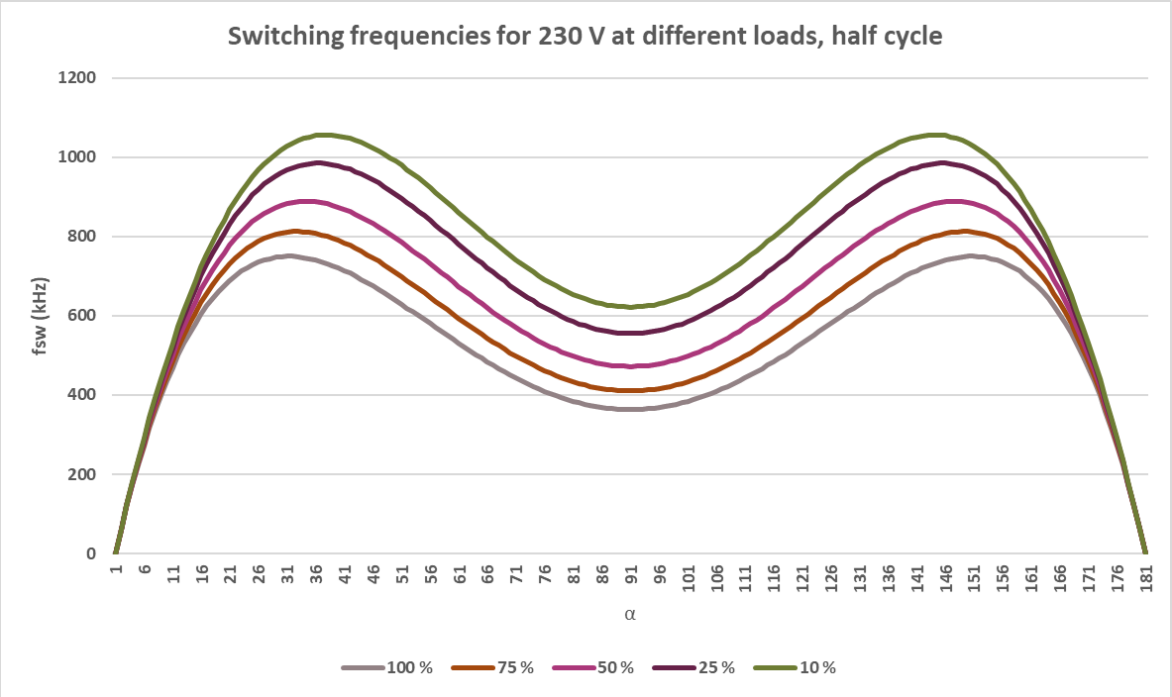

Figure 30 Switching frequency at different loads for 30 µH and 1.5 A valley.

The shape corresponds to that as simulated in Figure 29. Switching frequency increases as load decreases, as decreasing the load decreases current ripple which inversely increases f_{sw}. In Figure 31 is presented the excepted f_{sw} for 50 µH inductance and 1.5 valley.

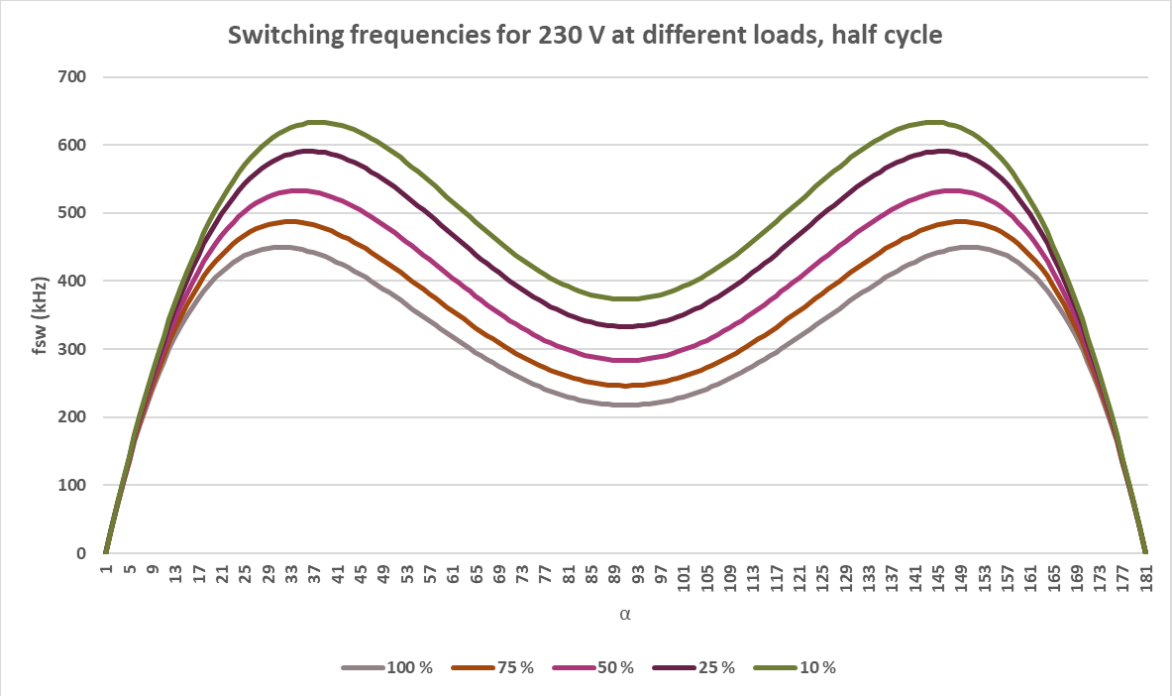

Figure 31 Switching frequency at different loads for 50 µH and 1.5 A valley.

As is visible from the figures, increasing inductance by 66 % has a significant effect on the expected f_{sw}. With the initial goal of up to 1 MHz f_{sw}, the first design was chosen for implementation.

With low line voltage the excepted f_{sw} is significantly different due to the increased ripple current. In Figure 32 is presented switching frequency for low line with 30 µH and 1.5 valley.

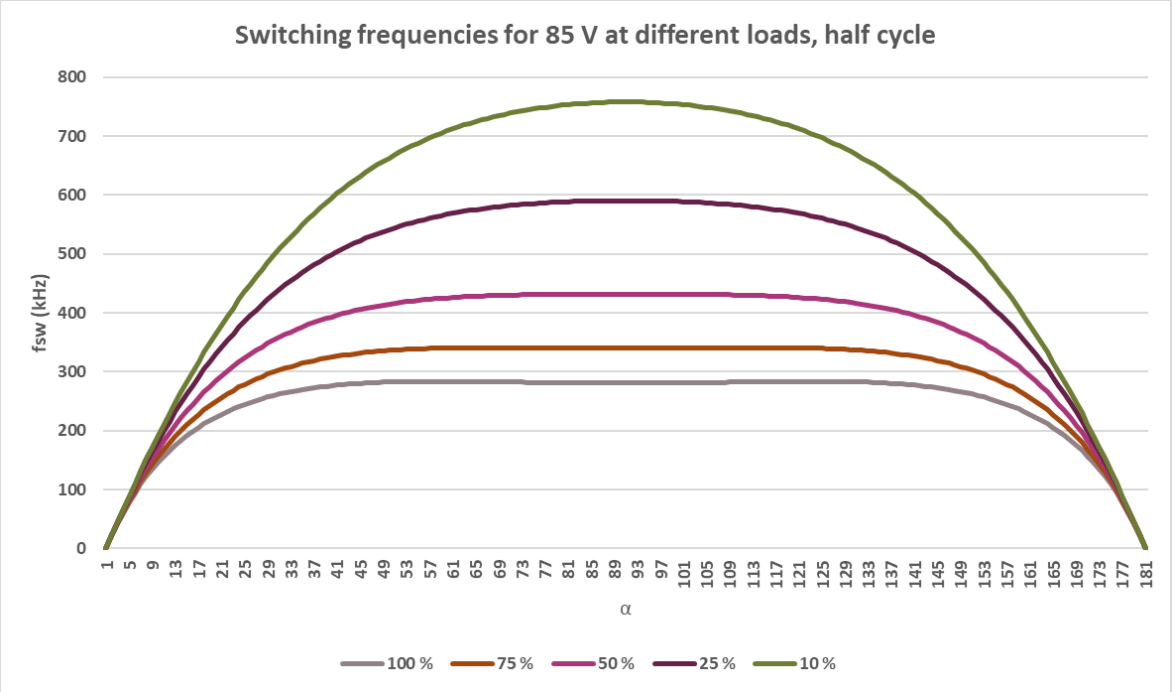

Figure 32 Switching frequency at different loads for 30 µH and 1.5 A valley for low line voltage.

The f_{sw} waveform shape is vastly different to that compared to high line. The overall switching frequency is also lower due to increased ripple current since the required average current is much higher. The reason to consider the low line voltage even when focusing on design for high line, is that it sets a different design constraint. In the high line the main concern is the higher f_{sw} and its effects. On the other hand, low line has increased total current running through the components, making thermal behaviour of the converter and its components as the main issue. In Figure 33 is depicted the difference between currents for high line and low line.

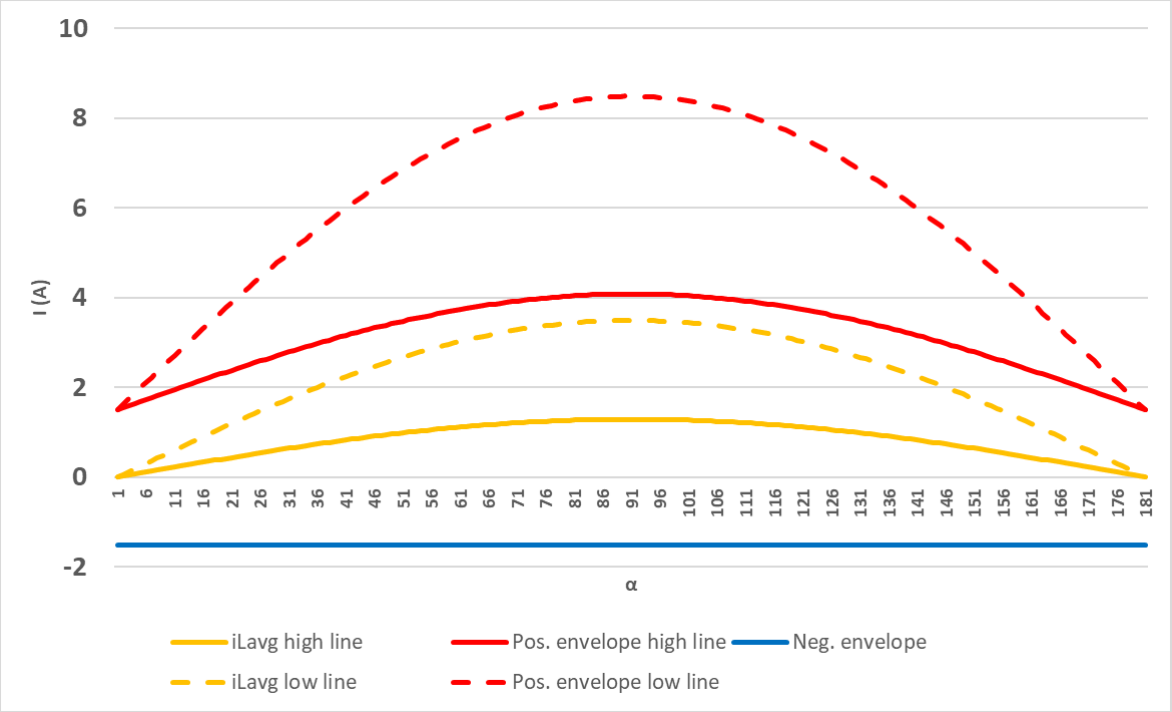

Figure 33 Inductor average current (orange), positive current envelope (red), and negative current envelope (blue) for high line (sold line) and low line (dashed line), 100 % load.

The difference in average and peak current is substantial. Using (13) the iL_{avg_pk} is 1.29 A for 230 V and 3.49 A for 85 V, nearly a threefold increase in average current. With 1.5 A valley the resulting peak current is 4.08 A and 8.49 A respectively. The increased current not only increases conduction losses, but also influences component design and selection.

4.2 Choke

The main choke design for a power converter is often balancing of different trade-offs. Having a bigger core may be more energy efficient but takes up more space worsening power density. In any case, the choke needs to meet the required inductance for the design specifications. Figure 34 illustrates the relation between core and winding losses as a function of turns in choke. The figure is only illustrative, and not representative of a real case.

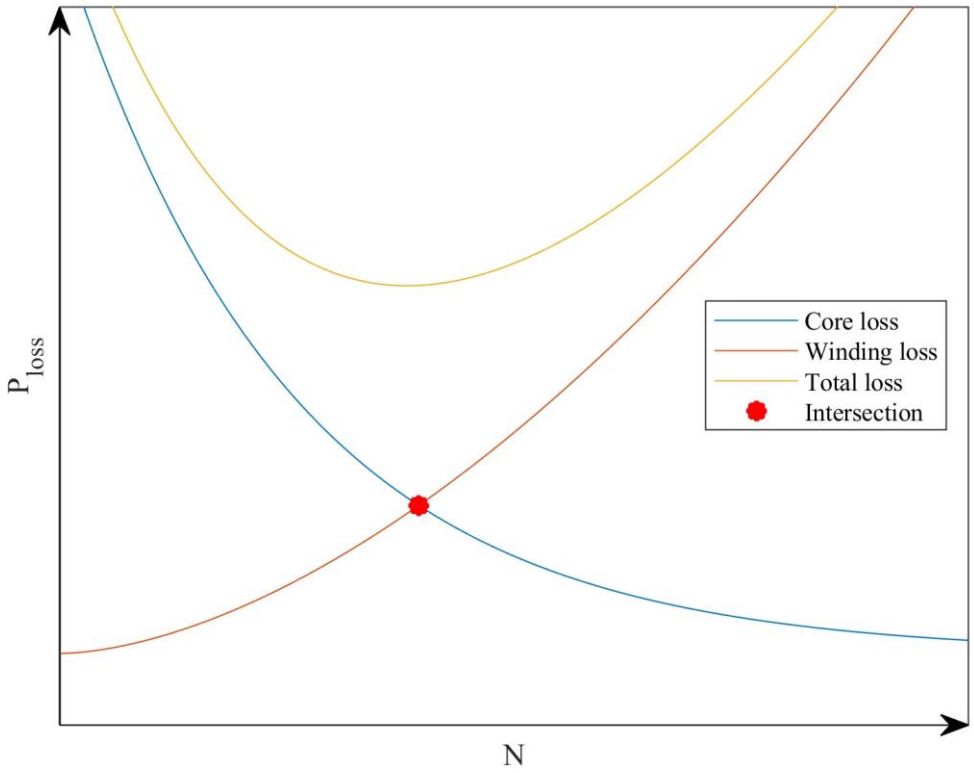

Figure 34 Illustrative figure of core loss vs. winding loss as a function of number of turns.

As the figure depicts, increasing the number of turns increases the losses in winding, but lowers them in the core material. In an ideal case, the intersecting point is the point of lowest total losses, which makes for the most optimal design from losses point of view.

Even though there are readily available chokes from retailers with rated inductance, there are many benefits to designing a choke yourself. Designing the choke gives more freedom of choice in the specific design and optimization.

4.2.1 Core

The high frequency of TCM together with the high ripple current, compared to CCM operation, poses a challenge for the choke design. For higher frequencies ferrite materials are more attractive option. For this application N49 Manganese Zinc (MnZn) material from TDK is used, as its optimum frequency range is between 300-1000 kHz (TDK, 2023).

The design equation for the minimum number of turns N in inductor is

$$N_{\min} = \frac{L \cdot iL_{\mathrm{pk}}}{A_{\mathrm{e}} \cdot B_{\max}} \tag{14}$$

where iL_{pk} is the peak current of inductor, A_e the effective magnetic cross section of the core, and $B_{\max}$ is the maximum allowed flux density. As calculated earlier with (8), iL_{pk} is 8.49 for the low line, which represent the worst-case scenario. A_{e} depends on the specific core size and geometry and $B_{\max}$ depends on the core material and desired safety margin. For N49 the saturation flux is a little less than 400 mT at 100 °C. The hysteresis BH loop of N49 is presented in Figure 35.

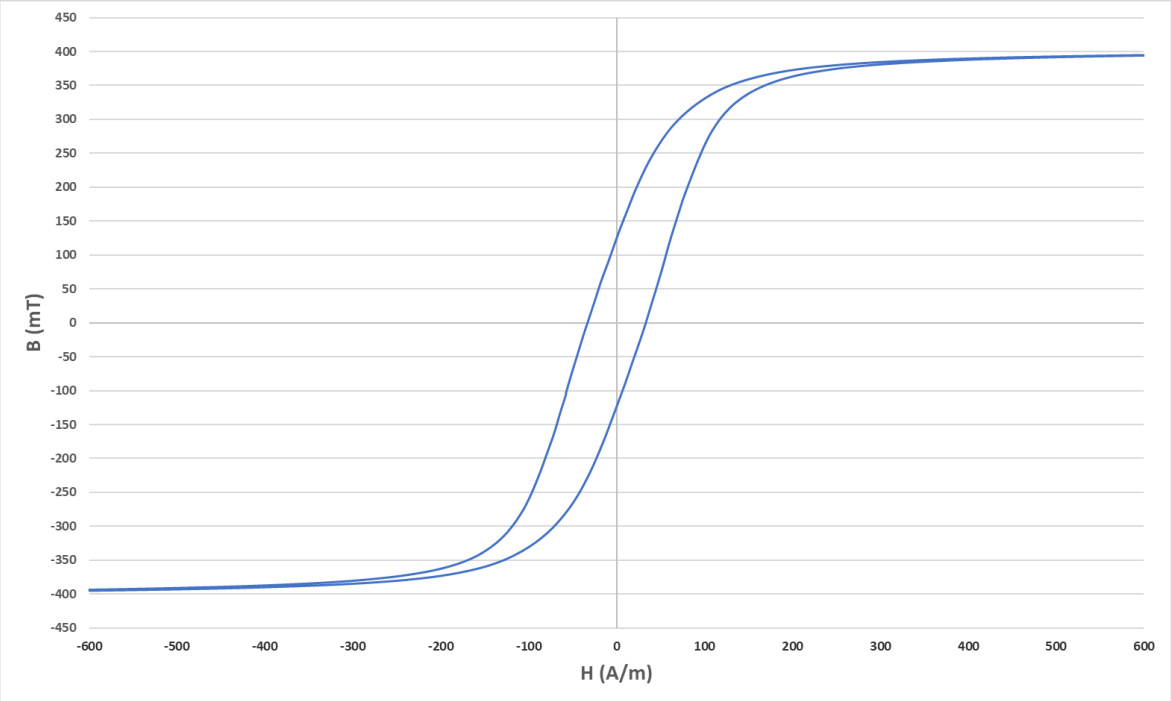

Figure 35 N49 BH loop at 100 °C. Data is acquired from TDK ferrite magnetic design tool.

When the magnetic flux density reaches its saturation point, it is not feasible to increase it further by increasing the magnetic field strength. When the saturation point is reached, the inductance of inductor drops, essentially making the inductor unable to operate as one. Therefore, it is important to make sure that the core never saturates in its intended operating range. As the peak current during low line is much higher, it is the value used when calculating turns for the choke. It is also wise to leave some safety margin in the design, so if the saturation point is 400 mT, the maximum flux should only be 65 % of it, or 260 mT, for some safety margin from the saturation point.

Inductance factor A_L, or inductance per turn is calculated as

$$A_L = \frac{L}{N^2} \tag{15}$$

With ferrite cores the specific inductance of core is achieved by adjusting the airgap of inductor. The required airgap l_g of inductor can be estimated with

$$l_g \approx \frac{\mu_0 \cdot A_e}{A_L} \tag{16}$$

where μ_0 is vacuum permeability. It is in the designers interests to keep the air gap at reasonable value to avoid problems such as fringing flux, where the magnetic flux flowing thorough the core spreads outside from the gap. The exact definition of reasonable value is very vague however, and depends from case to case. The effects of airgap on flux can be estimated or simulated with Finite Element Method (FEM) analysis for example.

Calculating the actual peak flux B_{pk} after the turns number N is decided can be done by solving B_{max} from (14).

$$B_{pk} = \frac{L \cdot iL_{pk}}{N \cdot A_e} \tag{17}$$

As discussed earlier, when designing the choke B_{max} value is chosen as input parameter for the minimum turns value determination. It is only after measuring the actual inductance of the built choke, checking for the B_{pk} has a meaning to it, especially if $N \neq N_{min}$.

For the converter a set of different PQ and RM N49 material cores from TDK were considered. The considered cores were PQ 16/11.6 to PQ 32/20 and RM 6 to RM 12. All the considered cores and their relevant dimensions are presented in Appendix 2.

By applying the equations presented in this section the design for different cores can be compared. The minimum number of turns for the different cores is presented in Figure 36.

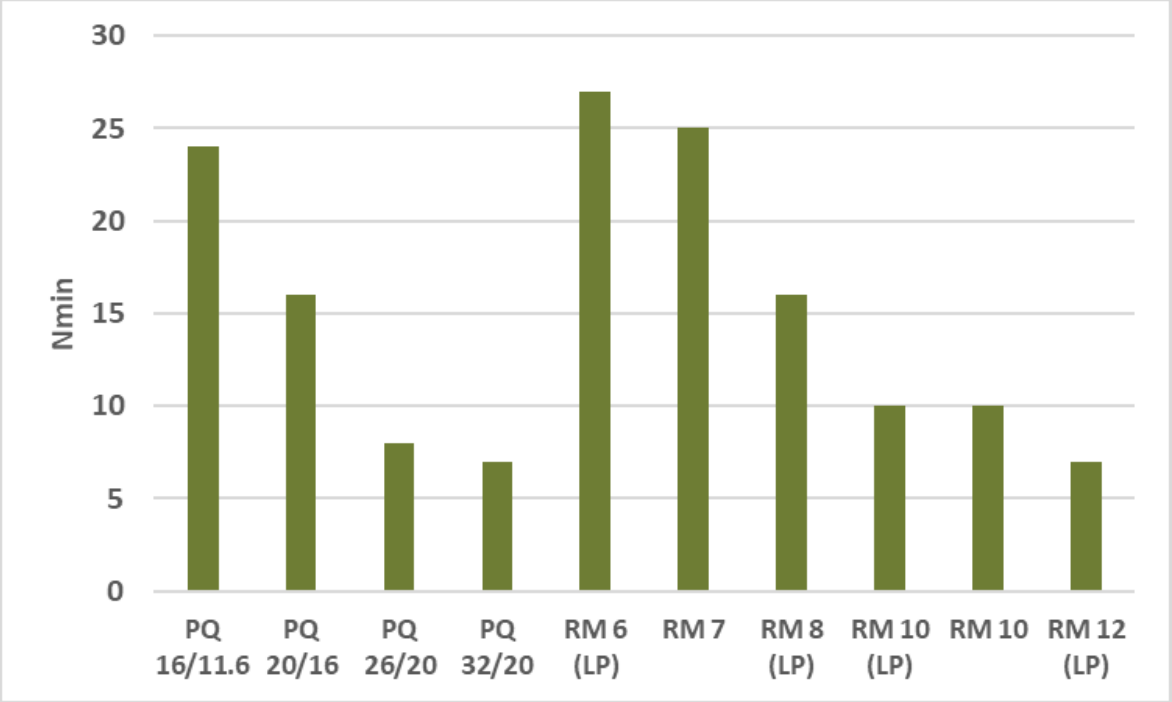

Figure 36 Minimum number of turns for different cores, rounded to the higher integer for 30 μH, 260 mT B_{pk} and 8.49 A iL_{pk}.

Since A_e is bigger for the larger cores, the number of turns for the designed inductance is lower. In Figure 37 is presented the estimated airgap values.

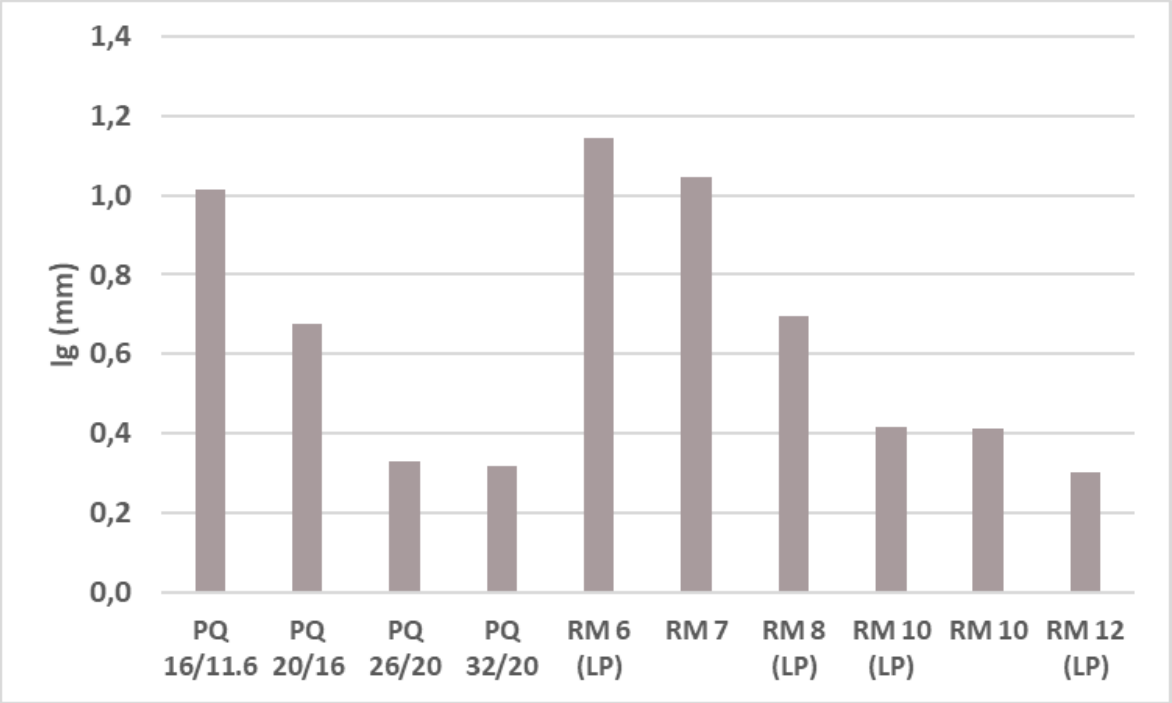

Figure 37 Estimated airgap of different cores for 30 μH, 260 mT B_{pk} and 8.49 A iL_{pk}.

The bigger cores required significantly shorter airgap due to increased effective area and inductance factor. Having a smaller core has the benefit of increased power density, however increasing turns has a significant effect on winding losses due to high currents of TCM operation. As discussed earlier, a bigger gap may also lead to fringing effect. By combining (15) and (16), the expression for gap is

$$l_g \approx \frac{\mu_0 \cdot N^2 \cdot A_e}{L} \tag{18}$$

As the value of L is required by the design, only turns N and A_e effective area can be changed. Usually, it is better to have less turns and bigger core, however the increase in core size also increases core losses, especially at higher frequencies, that will be discussed later. (Q. Huang et al. 2017)

For the implementation RM 7 and RM 10 Low Profile (LP) were chosen, as they were readily available from our own stocks. It also offers comparison for 2 different approaches: a smaller core with more turns and bigger gap, and a bigger core with less turns and smaller gap.

4.2.2 Winding

For winding litz wire was chosen, as at higher frequencies current has tendency to stack on the edges of wire, also called skin effect. Litz wire is formed from multiple finer strands that are twisted together to form a single bigger wire. Skin depth is calculated as

$$\delta = \sqrt{\frac{\rho}{\pi \cdot f \mu_r \cdot \mu_0}} \tag{19}$$

where ρ is resistivity of conductor, for copper $1.68 \cdot 10^{-8}$ Ω/m, and μ_r is the relative permeability of conductor, for copper 1. Skin effect is illustrated in Figure 38. The figure is only illustrative, as in real life skin effect is obviously more gradual.

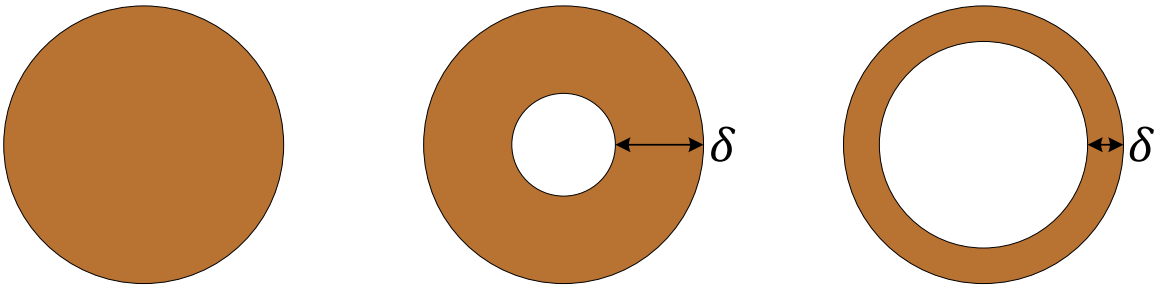

Figure 38 Skin effect in wire for DC current, low frequency AC current and high frequency AC current.

The higher the frequency is, the smaller the value of δ gets, forcing the current to flow through on a smaller area on the edges of the conductor. The increased current density on edges increases power dissipation and makes rest of the wire unutilized. By using a stranded litz, where d_{strand} is same or less than 2δ, the whole wire is utilized, and skin effect is significantly reduced.

For the chosen design with 30 µH, the minimum skin depth is reached on 10 % load during high line, and is 0.059 mm. That however represents the absolute worst-case scenario for minimal amount of time, and more realistic approach would be to look at the skin depth for average *fsw* (617 kHz) at 100 % load, which is 0.083. By using litz with subconductors less than 0.166 mm in diameter, skin effect is greatly reduced for the most part.

When selecting the wire, maximizing the copper area A_{cu} inside core window area A_w is beneficial, as winding resistance gets lower. In other words, fitting the biggest wire possible for the required turns N inside the core window. Figure 39 is a crosscut view of an E core illustrating the wires forming the copper area A_{cu} inside the core window A_w.

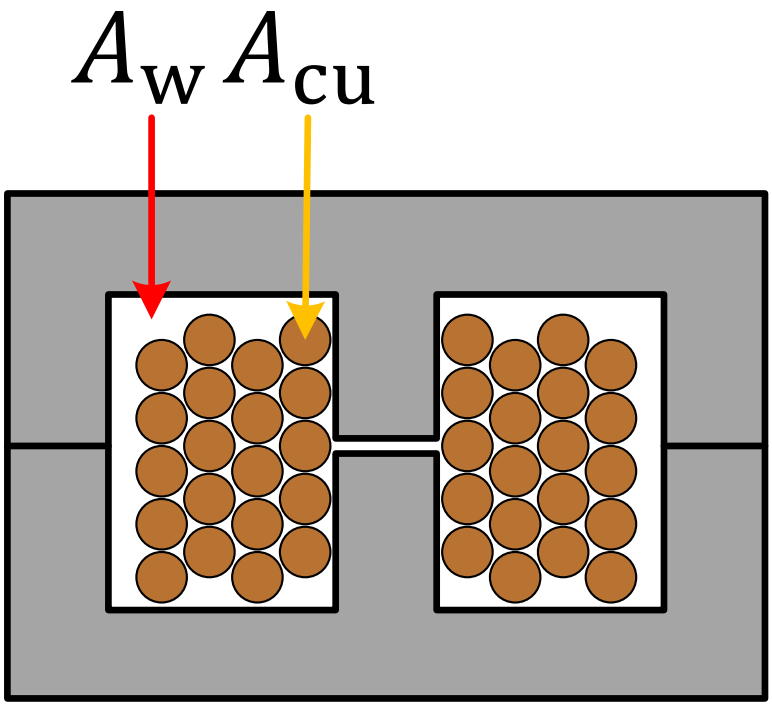

Figure 39 Crosscut view of an E core.

As higher copper content leads to lower losses, maximizing the filling factor f_w is desirable. In the figure above the window area is utilized to high extent. For gapped inductors positioning the wires away from the gap may be beneficial due to the fringing effect, however this work does not go to such detail in the design (C. R. Sullivan and R. Y. Zhang, 2014).

There are methods to choose the ideal or best type of litz for the design, however for our construction only wires readily available from our own stocks were considered. The wires are presented in Table 2.

Table 2 Available litz wires.

AWG sizes	*n* (Strands)	Strand diameter (mm)	Strand area (mm²)	iso (µm)	iso_layers	Cu area estimate (mm²)	Cu diameter (mm)	Total diameter (mm)	Total area (mm²)
AWG 38 - 45	45	0,1016	0,0081	63	3	0,36	0,68	1,06	0,88
AWG 38 - 75	75	0,1016	0,0081	63	3	0,61	0,88	1,26	1,24
AWG 38 - 120	120	0,1016	0,0081	63	3	0,97	1,11	1,49	1,75
AWG 44 - 128	128	0,0500	0,0020	52	1	0,26	0,58	0,68	0,36
AWG 44 - 512	512	0,0500	0,0020	63	3	1,04	1,15	1,53	1,83
AWG 46 - 25	25	0,0400	0,0013	52	1	0,03	0,20	0,30	0,07
AWG 46 - 75	75	0,0400	0,0013	52	1	0,09	0,35	0,45	0,16
AWG 46 - 135	135	0,0400	0,0013	52	1	0,17	0,46	0,57	0,25
AWG 46 - 270	270	0,0400	0,0013	52	1	0,34	0,66	0,76	0,45

The wires are reported in American Wire Gauge (AWG) system, with the number after dash implying the number of strands. For example, AWG 38 – 45 means 45 strands of AWG 38 twisted together. Iso refers to the coating of the wire, and the last four columns attempt to roughly estimate to total area and diameter of the litz wire, without and with coating.

Estimating AC resistance of conductor is quite difficult due to skin effect at high frequency, however there are methods developed to estimate the DC resistance of litz wire, giving a rough baseline for loss estimation. The DC resistance of litz may be estimated with

$$R_{\mathrm{DC}} = \frac{4 \cdot \rho \cdot N \cdot \mathrm{l}_N}{\pi \cdot n \cdot d^2} \tag{20}$$

where l_N is the length of a turn, n is the number of strands and d the diameter of strand (Xu Tang, C. R. Sullivan, 2003).

When the turns N, core window area A_{w} and total area of litz is known, it is a matter of selecting the wire for the build. To estimate whether a specific wire fits into the window area, the wire should take no more than 25 -30 % of the window area for handmade manually wounded design (C. R. Sullivan et al, 2014, 3). This estimate proved to be pretty good in practice as well. In Figure 40 is presented the estimated filling factors of litzes from table 2 for RM 7 with 25 turns and RM 10 (LP) with 10 turns.

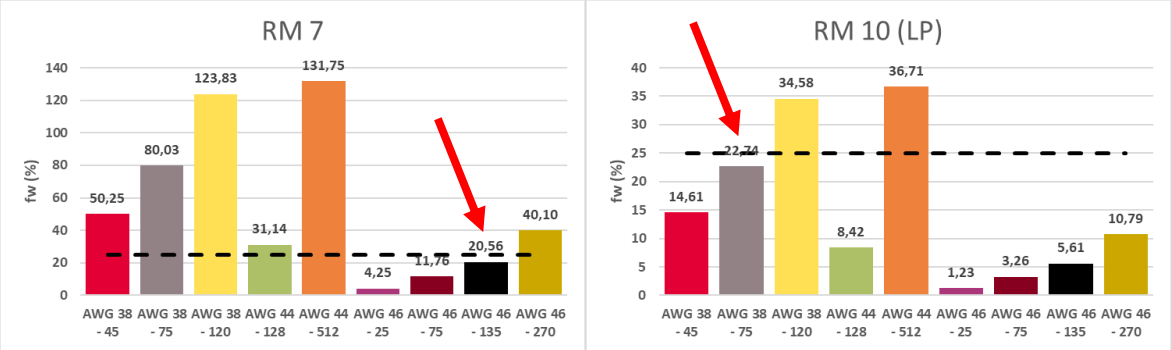

Figure 40 Filling factors for (left) RM 7 and (right) RM 10 (LP), with selected litz highlighted by red arrow.

The horizontal dashed line represents 25 % f_w mark, indicating that anything bigger would not fit in the window area. The same kind of comparison is made for resistances using (20) in Figure 41.

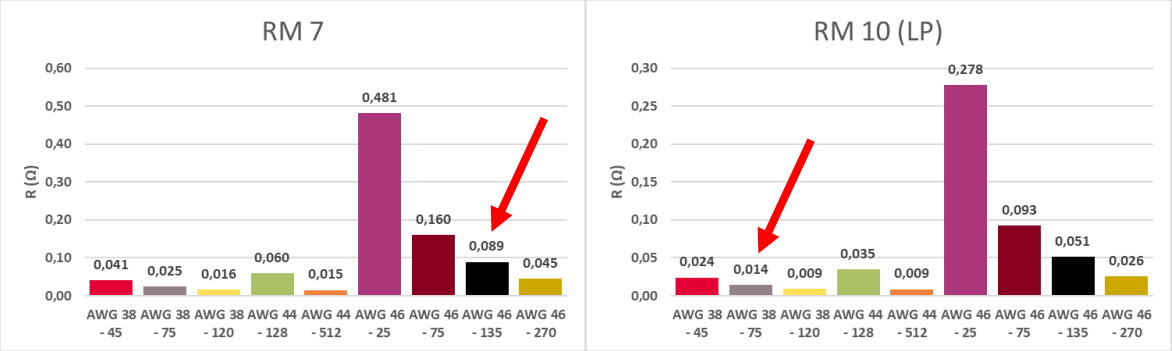

Figure 41 DC resistance estimates for (left) RM 7 and (right) RM 10 (LP), with selected litz highlighted by red arrow.

As is evident, the bigger the wire, the better estimated performance it offers. For the final construction AWG 46 – 135 for RM 7 and AWG 38 – 75 for RM 10 (LP) were selected, as they were the wires with the highest copper area that fit inside the cores.

4.3 Bulk capacitor

For the bulk capacitor two 56 µF capacitors are placed in parallel for 112 µF total capacitance. The Equivalent Series Resistance (ESR) of capacitor is calculated as

$$\mathrm{ESR} = \frac{\mathrm{DF}}{2 \cdot \pi \cdot f \cdot C} \tag{21}$$

where DF is Dissipation Factor of the capacitor, and f is the frequency where dissipation factor is given by the manufacturer, in this case 120 Hz. DF of the electrolytic capacitor used is 0.2. There were some concerns about durability and losses in the bulk capacitor, due to high ripple current of TCM operation, however due to time constraints a conclusive result was not obtained in this work.

4.4 Losses estimation

Estimating losses mathematically is a good way to get an initial estimate of the performance and difference between designs. In this work the main focus is on the losses in the magnetic parts.

4.4.1 Core and copper losses

Core losses may be estimated with Steinmetz equation

$$P_v = k \cdot f^{\mathrm{a}} \cdot \hat{B}^{\mathrm{b}} \tag{22}$$

where P_v is the losses referred to the volume of the core and k, a and b are Steinmetz coefficients. $\hat{B}$ is the total flux density swing, which is half of the flux variation at a given operating point. $\hat{B}$ is calculated as

$$\hat{B} = \frac{L \cdot \Delta iL}{2 \cdot N \cdot A_{\mathrm{e}}} \tag{23}$$

The coefficients a and b of the Steinmetz equation are frequency dependent and can be acquired empirically from the magnetics manufacturer data. For N49 ferrite the coefficients are acquired using the power losses as a function of flux density at different frequencies. The data is presented in Figure 42 in logarithmic scale, with the different lines presenting different frequencies.

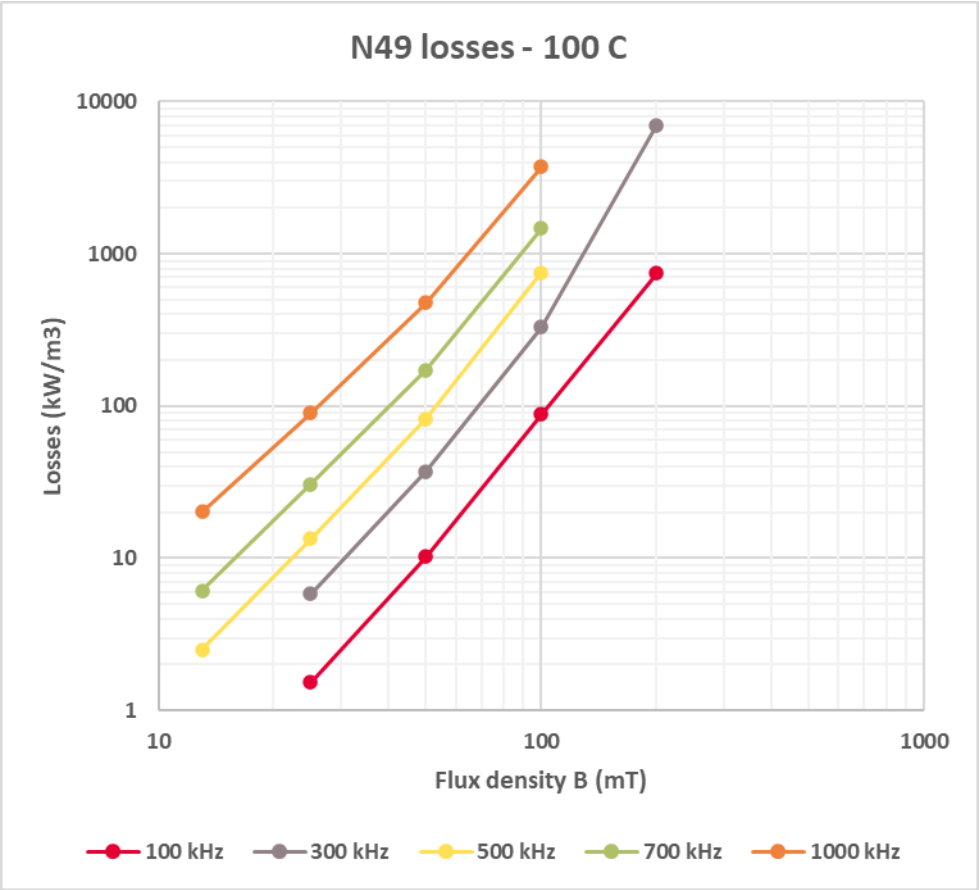

Figure 42 N49 losses against flux density at different frequencies. Data is acquired from TDK ferrite magnetic design tool.

As is evident, the losses increase with frequency and flux density. At 100 mT the losses are 88 kW/m^3 at 100 kHz, however at 1000 kHz the losses are 3730 kW/m^3. The loss properties set a boundary to the switching frequency for specific material, as at some point the losses become unsustainable. An example of how the core losses compare between the analysed designs during high line is presented in Figure 43.

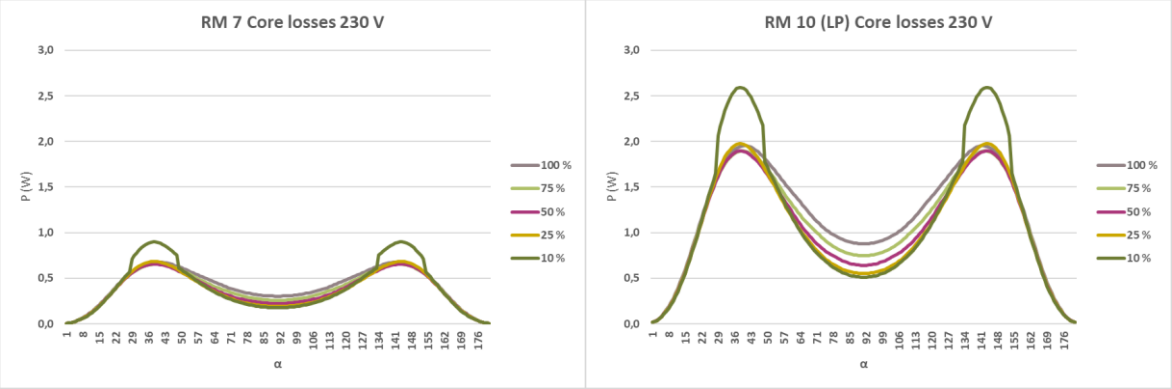

Figure 43 Core losses for (left) RM 7 and (right) RM 10 (LP).

As the comparison illustrates, RM 7 design has significantly less expected core losses. Since frequency, and thus losses, is continuously variable, the total core loss is the average loss through the mains cycle. The loss graph is a little bit skewed for the 10 % load due to the way the developed magnetics design program calculates core losses when f_{sw} surpasses 1 MHz. Since there is not data available from the manufacturer for higher frequencies, the losses are extrapolated beyond 1 MHz.

The conduction losses in the wire are calculated using RMS ripple current. Since the current in inductor is triangular waveform, the RMS ripple is calculated as

$$iL_{\mathrm{RMS}} = \frac{\Delta iL}{\sqrt{3}} \tag{24}$$

And conduction losses

$$P_{\mathrm{cu}} = iL_{\mathrm{RMS}}^2 \cdot R_{\mathrm{DC}} \tag{25}$$

where R_{DC} is the resistance estimate for litz using (20). With all the formulas for loss calculation in the choke known, the different design can be compared in a bar chart form. In Figure 44 is presented the estimated losses for the chokes during high line at different loads.

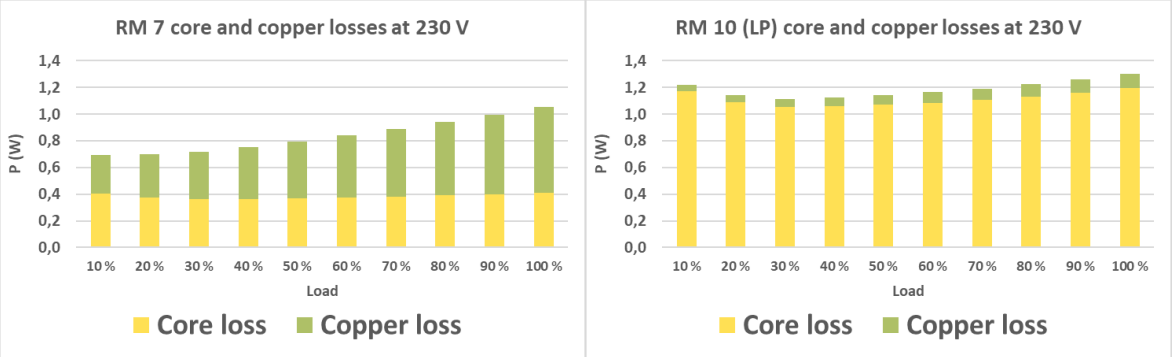

Figure 44 Core and copper losses during high line for (left) RM 7 and (right) RM 10 (LP).

With smaller core the estimated core losses are lower, however estimated copper losses are significantly higher. In Figure 45 the losses are presented for low line.

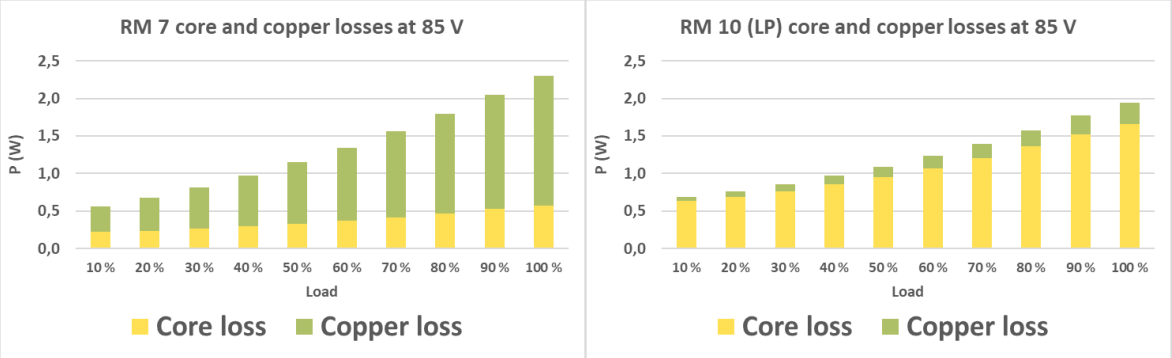

Figure 45 Core and copper losses during low line for (left) RM 7 and (right) RM 10 (LP).

During low line the copper losses are significantly higher due to the increased ripple current. Overall, the RM 7 seems to offer a little bit better estimated losses than RM 10 (LP) for high line, during low line RM 10 (LP) appears to be a little bit better. The losses are not the only consideration however, as the discrete gap that is significantly wider in RM 7 may come with other problems discussed earlier. It is noteworthy that all losses are affected by temperature variation, however this work does not go in such detail in loss estimation and only constant temperature is considered.

4.4.2 High frequency GaN losses

The losses in HF bridge are a combination of conduction and switching losses. Due to ZVS, only turn-on losses are minimal. There are several approaches to switching loss calculation, such as time, energy and output capacitance based. In this work switching losses P_{sw} are calculated as

$$P_{\mathrm{sw}} = \frac{1}{2} \cdot f_{\mathrm{sw}} \cdot C_{\mathrm{oss}} \cdot V_{\mathrm{o}}^2 \tag{26}$$

where C_{oss} is the output capacitance of IGI60F140A1L GaN, 28 pF (Infineon Technologies, a).

The total conduction losses are a sum of the switches operating as boost switch and boost rectifier. The duty cycle of boost switch is calculated as

$$D = 1 - \frac{V_{\mathrm{in}}}{V_{out}} \tag{27}$$

and the duty cycle of boost rectifier switch is 1-*D*. For both modes the RMS current is calculated as

$$I_{\mathrm{S,RMS}} = \Delta iL \cdot \sqrt{\frac{\mathrm{D}}{3}} \tag{28}$$

where *D* is the duty cycle associated to the switch. The conduction losses are finally calculated as

$$P_{\mathrm{cond,HF}} = I_{\mathrm{S,RMS}}^2 \cdot R_{\mathrm{DS(on)}} \tag{29}$$

where $R_{DS(on)}$ resistance for IGI60F140A1L is 0.19 Ω maximum (Infineon Technologies, a).

In addition to the switching and conduction losses there is a small loss associated with operating the switch, called gate loss. Gate loss is calculated as

$$P_{\mathrm{g}} = Q_{\mathrm{g}} \cdot V_{\mathrm{gs}} \cdot f_{\mathrm{sw}} \tag{30}$$

where Q_g is the gate charge and V_{gs} is gate drive voltage.

4.4.3 Low frequency rectifier losses

For the rectifier switches only conduction losses are considered, as the switching loss is minimal due to line frequency operation. The RMS ripple current of rectifier switch is the same inductor current, so (24) is used for current. The $R_{\mathrm{DS(on)}}$ resistance for IPL60R065P7 is 0.065 Ω maximum (Infineon Technologies, 2018).

$$P_{\mathrm{cond,LF}} = iL^2_{\mathrm{RMS}} \cdot R_{\mathrm{DS(on)}} \tag{31}$$

4.4.4 Bulk capacitor losses

Bulk capacitor RMS current is estimated with

$$I_{C,\mathrm{RMS}} = \frac{\Delta iL}{2 \cdot \sqrt{3}} \tag{32}$$

The losses associated with the capacitor are calculated using ESR as calculated in (21).

$$P_C = I^2_{C,\mathrm{RMS}} \cdot \mathrm{ESR} \tag{33}$$

An example of the RMS current waveforms used for loss calculation is shown in Figure 46. All the conduction losses are based on the RMS currents.

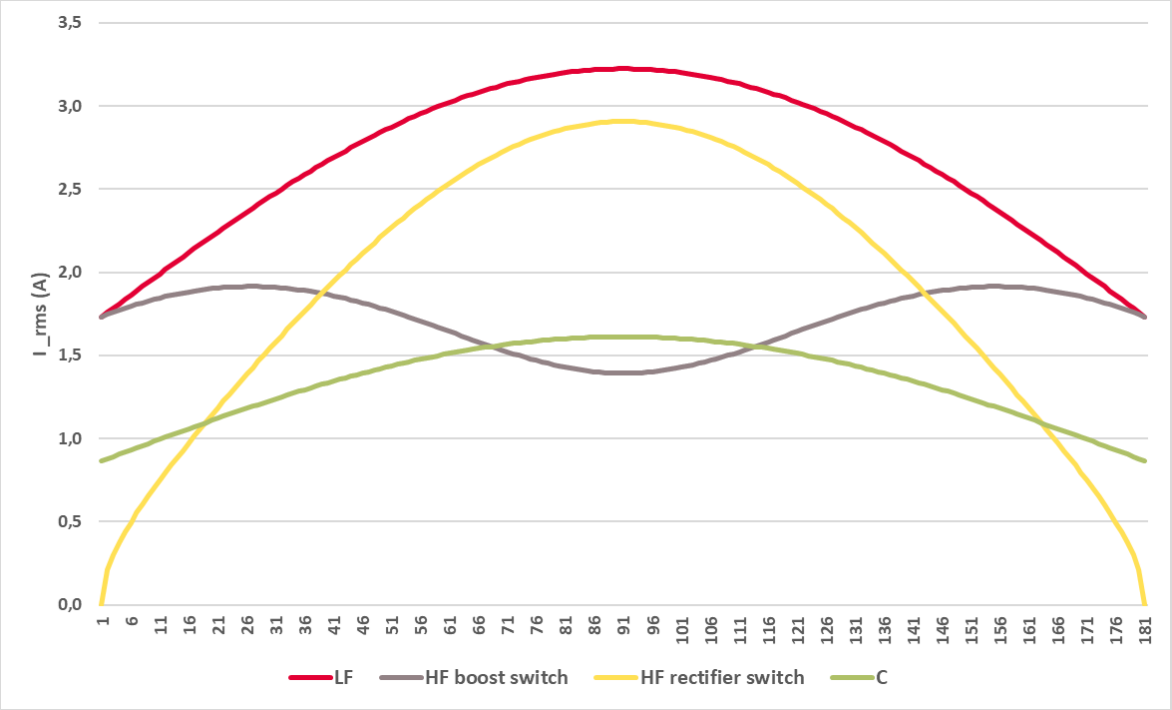

Figure 46 RMS currents for 100 % load during high line.

With all loss formulas presented the losses are presented in easily readable bar chart. Combination of all losses are only shown for RM 10 (LP) core, as other losses than core and winding remain the same regardless of the core. In Figure 47 is the loss estimate during high line.

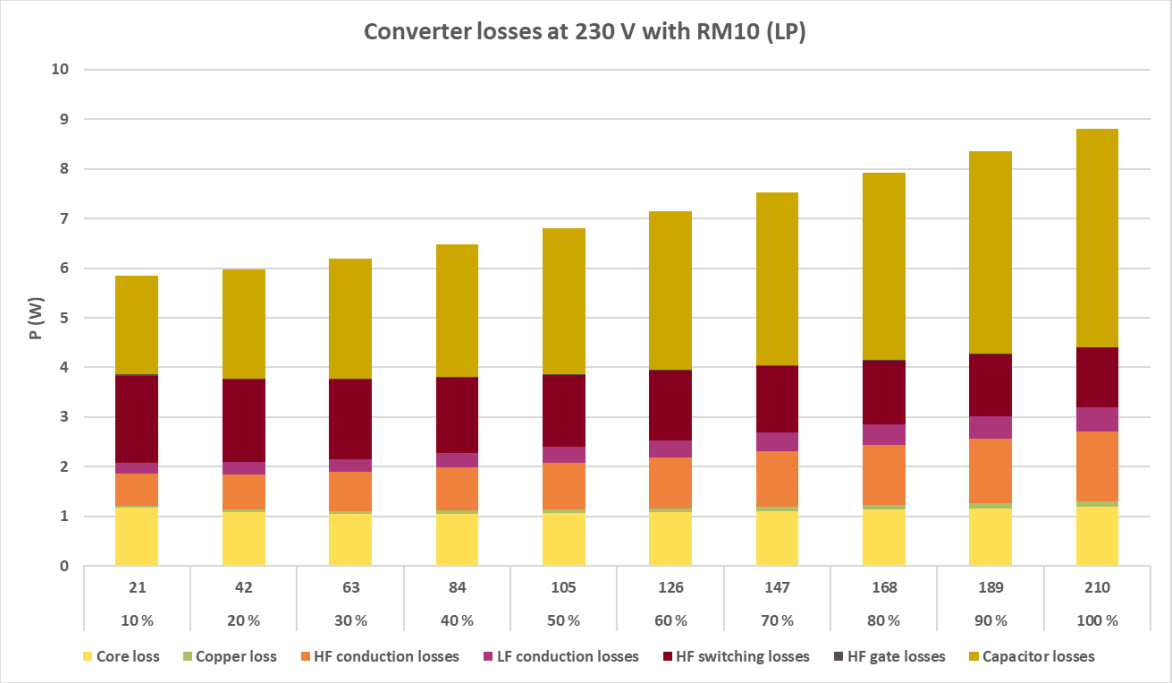

Figure 47 Loss estimates for high line at different loads.

The same data is presented for low line in Figure 48.

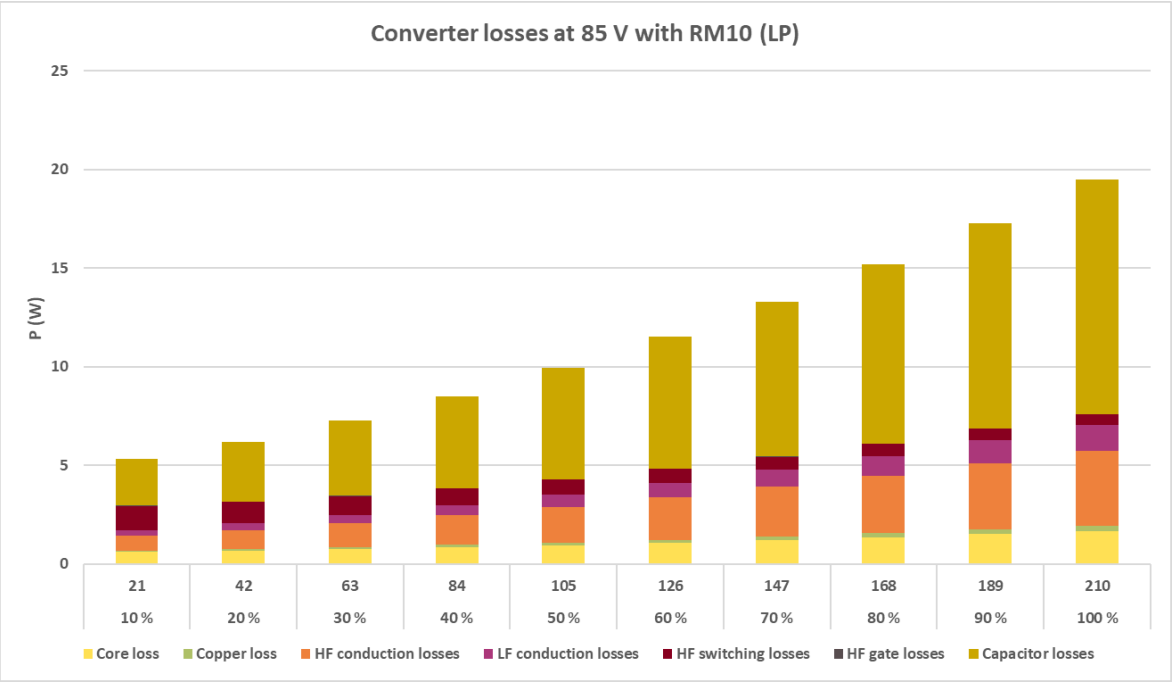

Figure 48 Loss estimates for low line at different loads.

As is evident, the estimated losses are excessive. Especially the high ripple current and low *C* in the output capacitor is causing very high loss estimates in the bulk capacitor. With power dissipation so high in such small capacitor even a catastrophic failure of the capacitor is possible. To reduce losses and increase the robustness of capacitors bigger capacitors may be used, that however comes with the cost of worse power density, as higher capacitance capacitors take up more space. The efficiency estimate of the converter is presented in Figure 49.

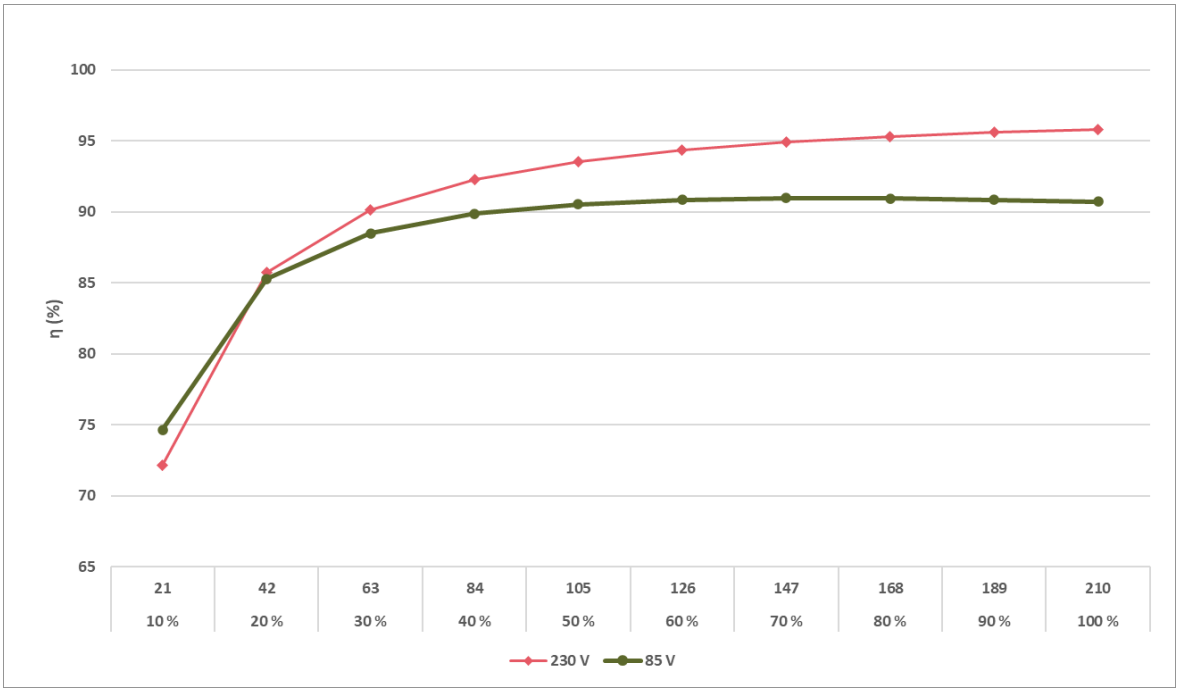

Figure 49 Efficiency estimates of converter.

The efficiency estimate indicates only 95.8 % efficiency at 100 % load for high line, which would be very poor. At least 97-98 % efficiency is excepted from modern PFC converters at their maximum output power. Hence it can be concluded that either the design is poor or unfeasible, or more likely the loss estimate is inaccurate. Since the focus of this work is on the magnetics design, more accurate analysis is not conducted, as for the core loss estimate the results can be excepted reasonably accurate compared to other losses.

4.5 Implementation of the choke

Usually, discrete gapped inductors have a single airgap in the centre leg, illustrated by Figure 50 on the left. This can be done by grinding the required gap by shaving material of the core or manufacturing the core with the gap already built. Since we lack the equipment to grind the material, the gap is implemented by including a spacer between the core halves instead, demonstrated by Figure 50 on the right.

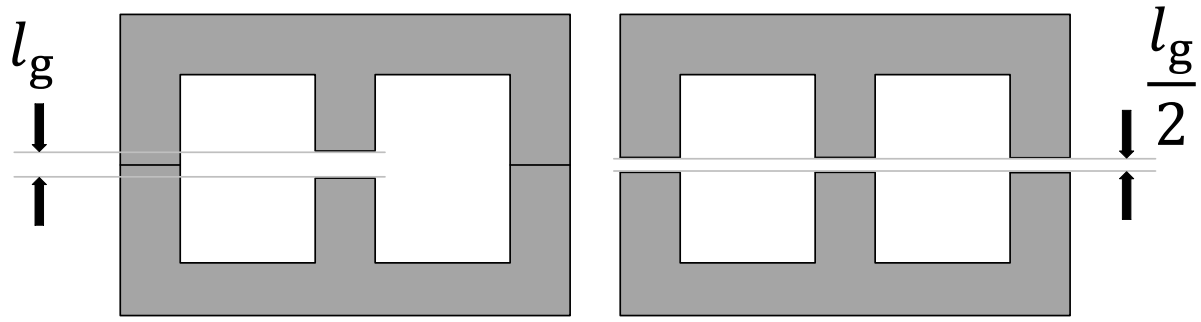

Figure 50 Airgap of an E core. The effective gap is the same in both examples.

By putting spacers between the outer legs of the core it is possible to implement the same effective gap, as with single gap in the middle. This is beneficial not only because it is easy to implement, but the ability to adjust to length of the gap to gain the desired *L* without cutting any material. However, it comes with the disadvantage of possibly generating fringing flux outside of the inductor. Gap implemented with spacers is unlikely to be seen in commercial applications.

The gap was implemented with copy paper sheets as spacers. If assuming that the thickness of paper is around 0.1 mm, then placing 2 sheets on each side would equal to 0.4 mm effective gap. In Figure 51 is shown the implemented cores.

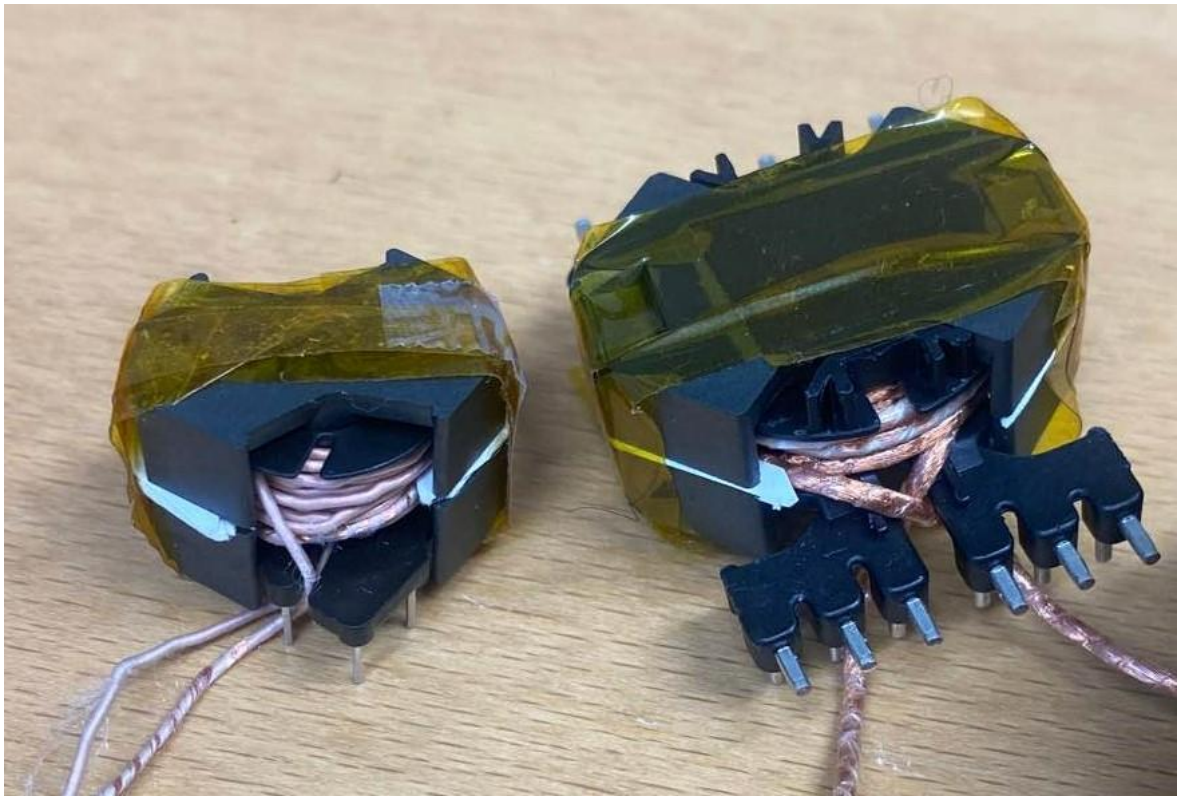

Figure 51 Built RM 7 (left) and RM 10 (LP) cores.

The cores are held together with thermal tape. Preferably clamps would be used, but those were not available. The winding is wounded around a plastic coil former.

4.6 Control delay

With power converter control there is always some control delay associated with switching of the transistors. This delay is a combination of delay in the analog comparator of the microcontroller and propagation delay of the driver t_{PD}, as well as some logic delay. In the case of IGI60F140A1L, it is the propagation delay t_{PD} of the driver of the GaN. The length of delay differs between different microcontrollers and transistors. In lower frequency applications the delay is less likely to be a cause of concern, however at higher frequencies it can be a limiting factor.

For the tested microcontroller XMC1400 the analog comparator delay is between 25-80 ns in high power mode according to the datasheet (Infineon Technologies, 2017, 57). For the GaN driver, the delay is 47 ns (Infineon Technologies, a). Even with infinitely fast controller at least the GaN driver delay is present.

Effects of control delay can also be simulated by adding propagation delay blocks to the generated PWM pulses shown in Figure 24. In the simulations 200 ns total delay is used. Figure 52 illustrates the effect of delay.

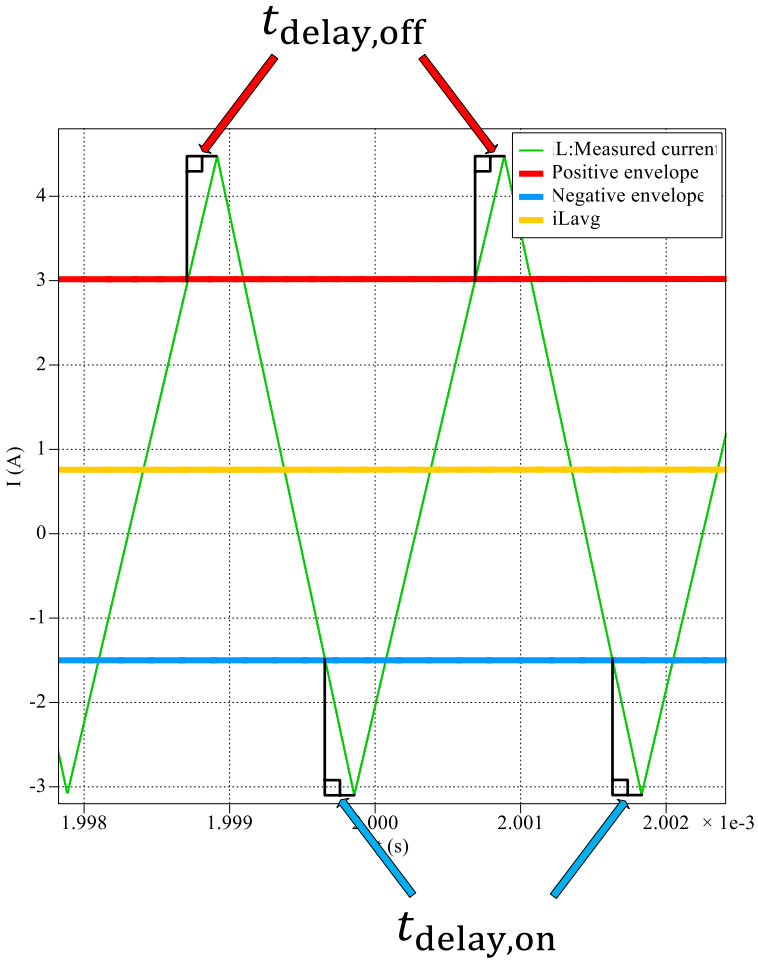

Figure 52 Effect of control delay in current overshoot.

When the inductor current hits the hysteresis reference, a trigger is activated to update the PWM pattern. With taking the delay into account, the current keeps rising according to (9) and decreasing with (10) for the duration of the delay. As the current slope is steeper with lower inductance (and hence higher f_{sw}), the phenomena becomes more apparent when lower inductance is used. If current overshoot is too high, higher inductance inductor may be required, however it will result in lower f_{sw}, putting a practical limit to the capability of the microcontroller and transistor. In Figure 53 is simulated how the 200 ns delay effects f_{sw} and hysteresis current behaviour for the analysed design with 30 µH and 1.5 A valley.

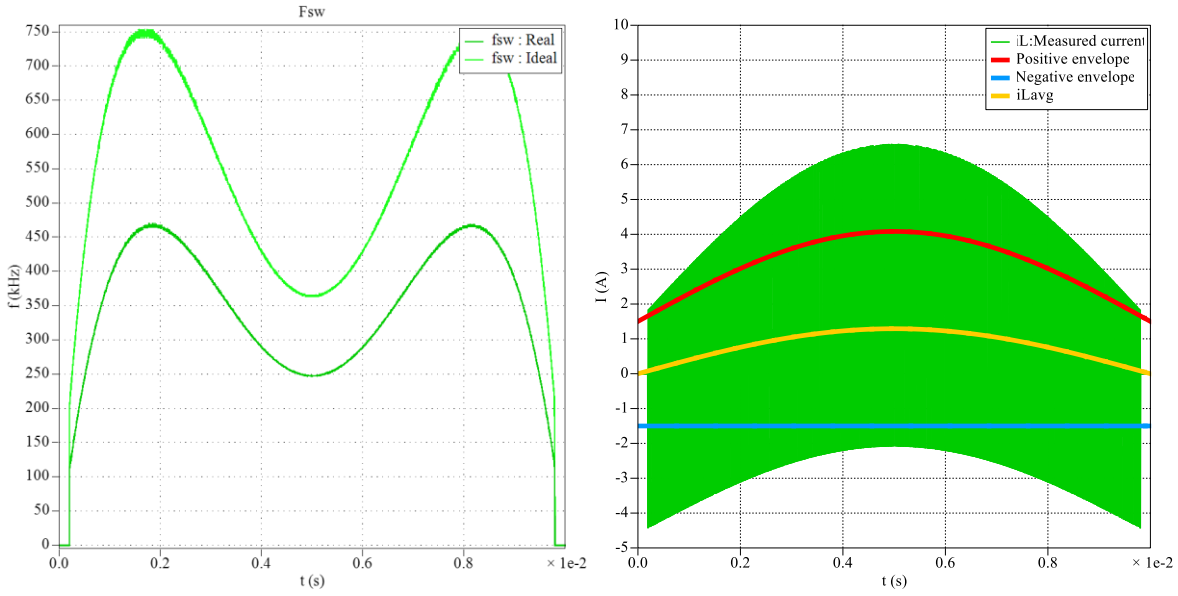

Figure 53 Simulated f_{sw} and hysteresis with 200 ns delay.

With 200 ns delay the current is way out of the envelopes and the *iL*avg would be negative towards both ends of the half cycle in reality. Switching frequency is reduced compared to the ideal case without delay, as current ripple *ΔiL* increases due to the delay. Figure 54 simulates how f_{sw} and hysteresis are affected with higher inductance of 80 µH with 1 A valley.

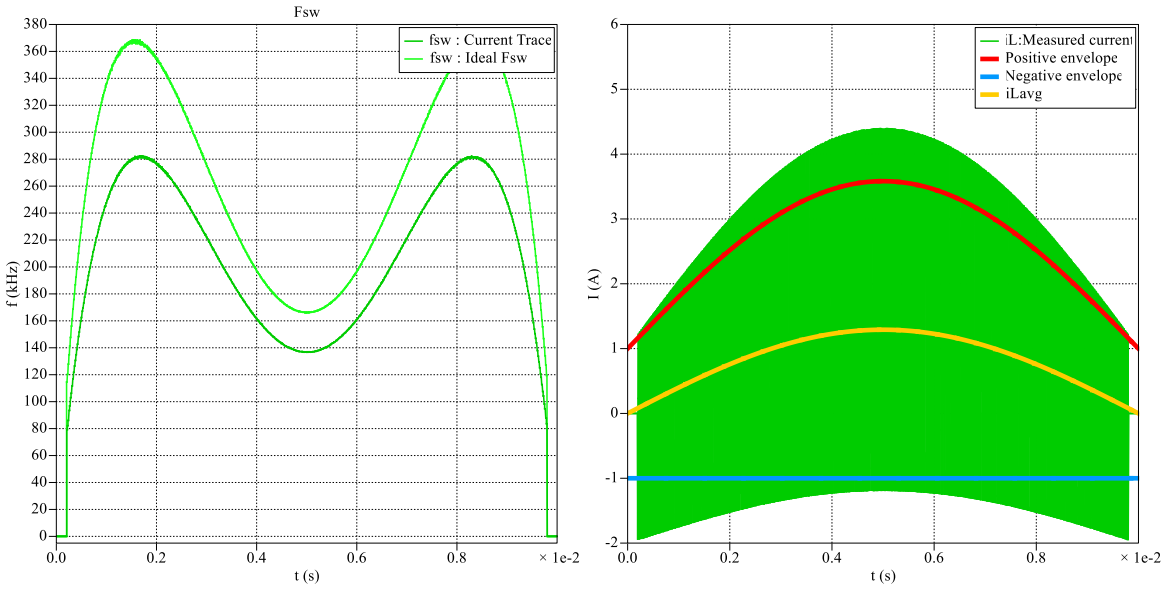

Figure 54 Simulated f_{sw} and hysteresis for 80 µH and 200 ns delay.

With higher inductance current overshoot is significantly reduced. Real f_{sw} is closer to the desired ideal value, however the overall f_{sw} would be much lower compared to the desired up to 1 MHz f_{sw} range.

It is possible to compensate for the delay to an extent by applying a sinusoidal reference to the valley envelope. Instead of being constant value, the valley moves to the opposite direction from the other envelope sinusoidally, attempting to counter the effects of delay. In Figure 55 is presented effects of compensation with the same parameters as in Figure 54.

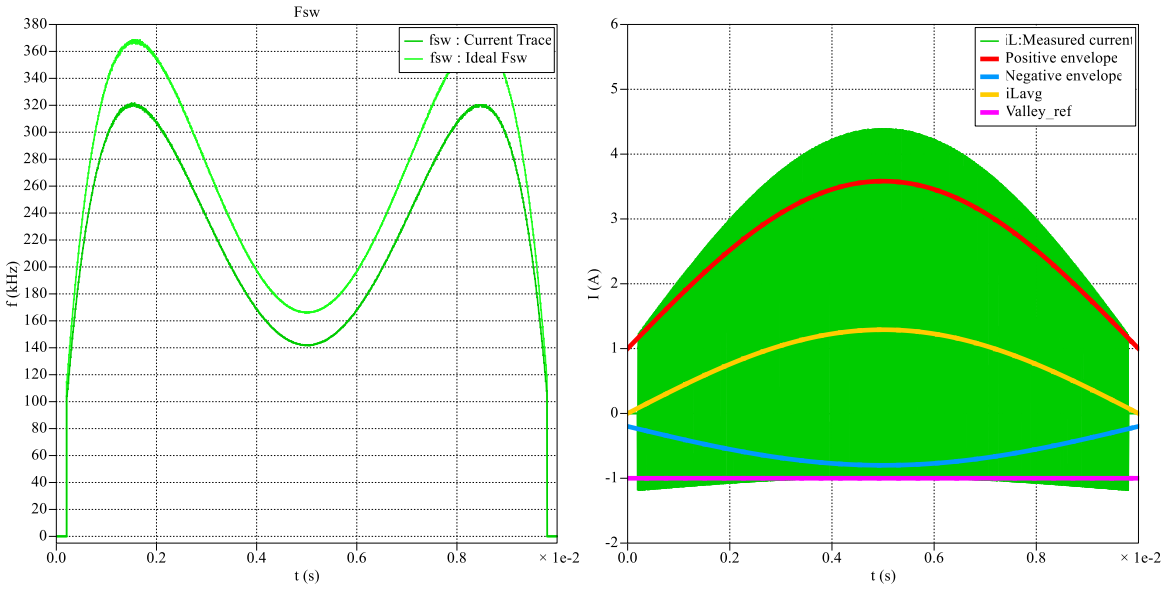

Figure 55 Effect of compensation on *f*sw and hysteresis.

The valley reference (blue) is now moving sinusoidally, compensating for the delay, and bringing the inductor ripple negative peak current closer to the desired valley of 1 A (purple). F_{sw} is increased and is closer to the ideal value, as ripple current decreases. Compensating for the delay comes with the expense of increased control complexity, however.

5 Testing and results

In this chapter the relevant tests and measurements performed to the converter are presented. The main goal of testing and control development is to test the feasibility of the XMC 1400 up to MHz range.

5.1 Choke measurements

The most accurate and probably the simplest method to measure the inductance of choke is to use impedance analyser. Impedance analyser can measure for example inductance and AC resistance of a choke over wide frequency range. For the choke measurements Wayne Kerr 6500B series impedance analyser was used. In Figure 56 is presented one of the measurements on 20 kHz - 2 MHz range for inductance and resistance for RM 10 (LP) with spacers for estimated 0.4 mm gap for targeted 30 μH inductance.

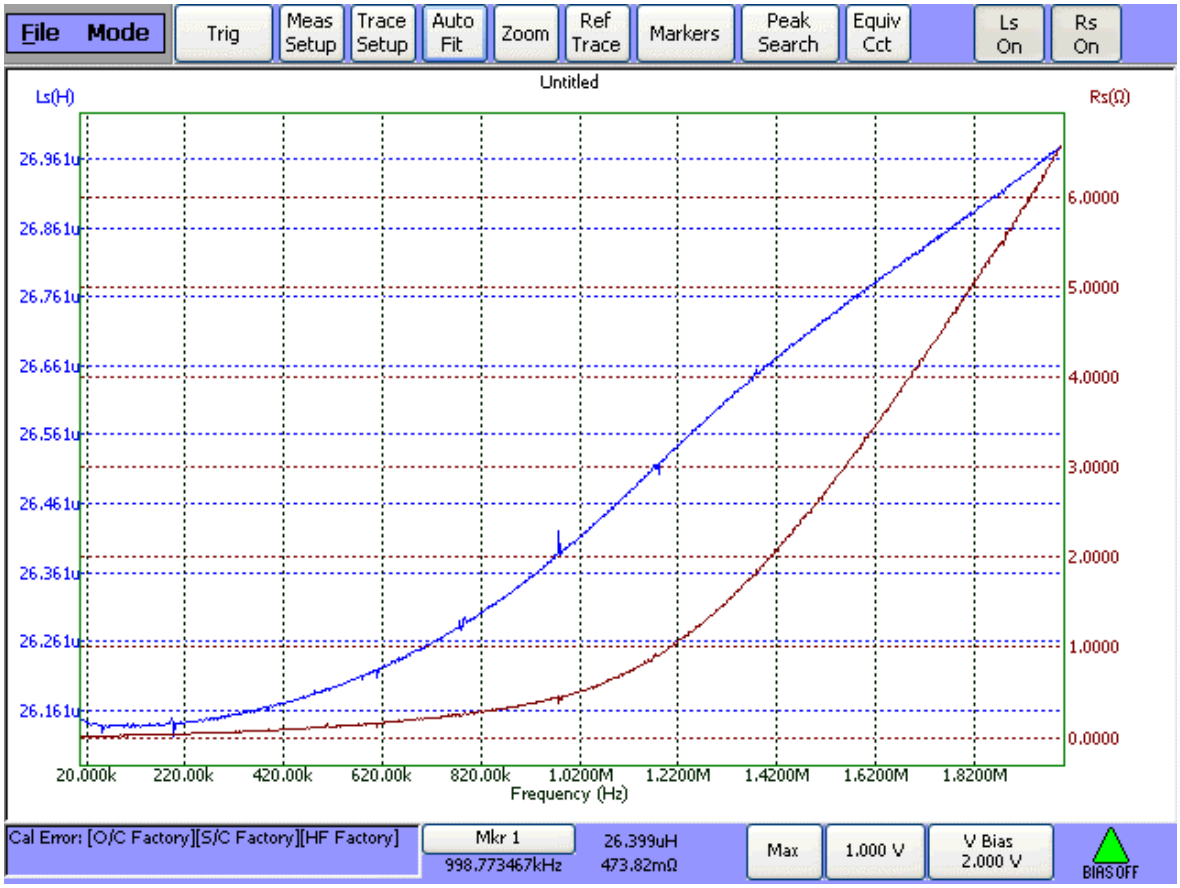

Figure 56 Measured inductance (blue) and AC resistance (brown) of choke with impedance analyser.

The measured inductance is close to the design value. The resistance increases significantly quicker beyond 1 MHz, however that is mostly out of the frequency operating range. All the measured chokes are presented in Table 3. Paper is used as spacer for gap implementation. L is the measured inductance, calculated gap refers to the gap calculated with (16) for the measured inductance. Actual gap refers to how wide the gap is in reality, and difference portrays the difference between the calculated gap and real gap.

Table 3 Measured chokes. *Assuming that paper thickness is 0.1 mm.

Core and *N*	*L* (µH)	Calculated gap (mm)	Actual gap* (mm)	Difference (mm)	Gap implementation
RM 7, *N* = 25	52	0.6	1.2	- 0.6	6 sheets per side
	44	0.71	1.6	- 0.89	8 sheets per side
RM 10 (LP), *N* = 10	45	0.28	0.2	+ 0.08	1 sheet per side
	26	0.48	0.4	+ 0.04	2 sheets per side

As there was limited availability and time to the test equipment and adjusting the chokes while testing, the RM 10 (LP) with 26 µH was settled for the final build, as it is closest to the desired 30 µH value. To further adjust the other chokes closer to 30 µH would require finetuning the gap or reducing the number of turns, which was not possible in the testing timeframe.

Interestingly, the gap estimate for the bigger core with lower turns seems be quite accurate, whereas for the smaller one it is quite a bit off. The actual implemented gap is only a rough estimate however, as the real gap varies due to the inconsistent nature of the spacers. In any case, another reason to pick the RM 10 (LP) with smaller gap is the presumably smaller fringing effect, which also helps improving AC resistance performance. The measured AC resistances are presented in Figure 57.

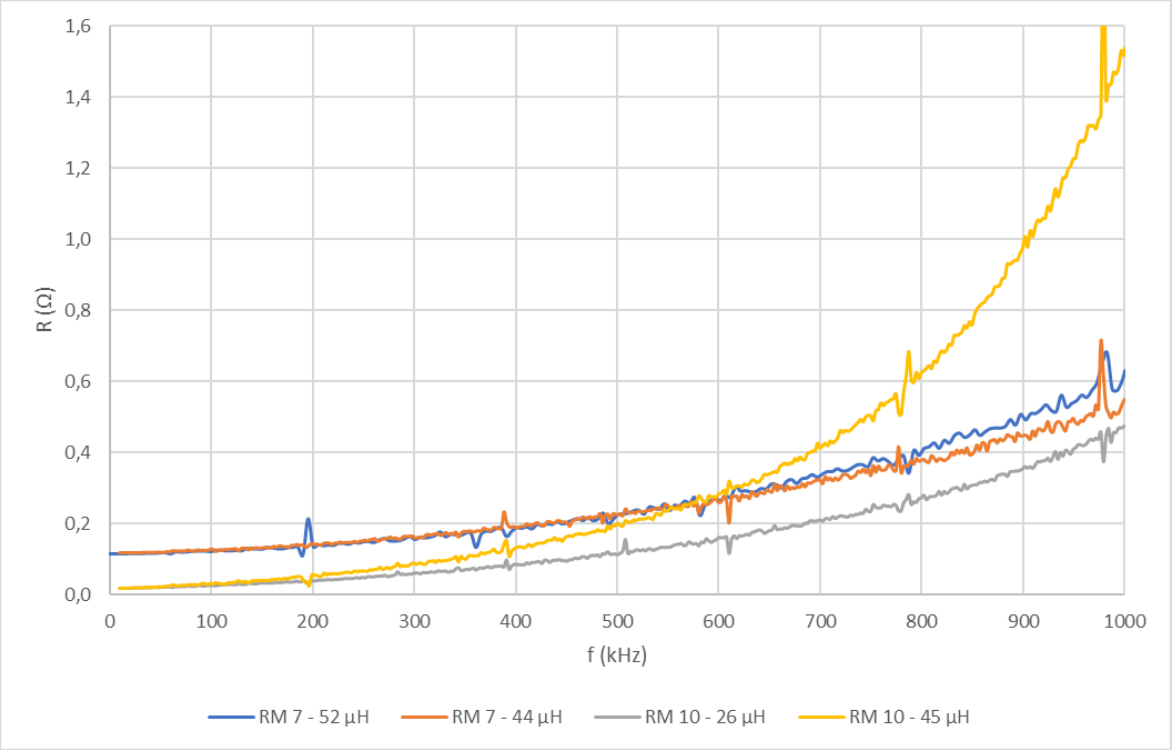

Figure 57 Measured resistances in 0-1 MHz range.

The selected choke offers the best performance across the frequency range, especially at lower frequencies the relative difference is rather advantageous against RM 7. The other RM 10 (LP) measurement could be misinterpreted due to bad contact or similar, as the resistance rises rapidly after 500 kHz, and is not in line with the other chokes.

Another measurement with the impedance analyser was determining the self-resonant frequency of the inductor. Self-resonance is the frequency where the parasitic capacitance of inductor resonates with the ideal inductance. At self-resonant frequency impedance of the choke rises rapidly and inductor loses its ability to function as one, as *L* drops. Figure 58 is the resonant frequency measurement for the 26 µH choke.

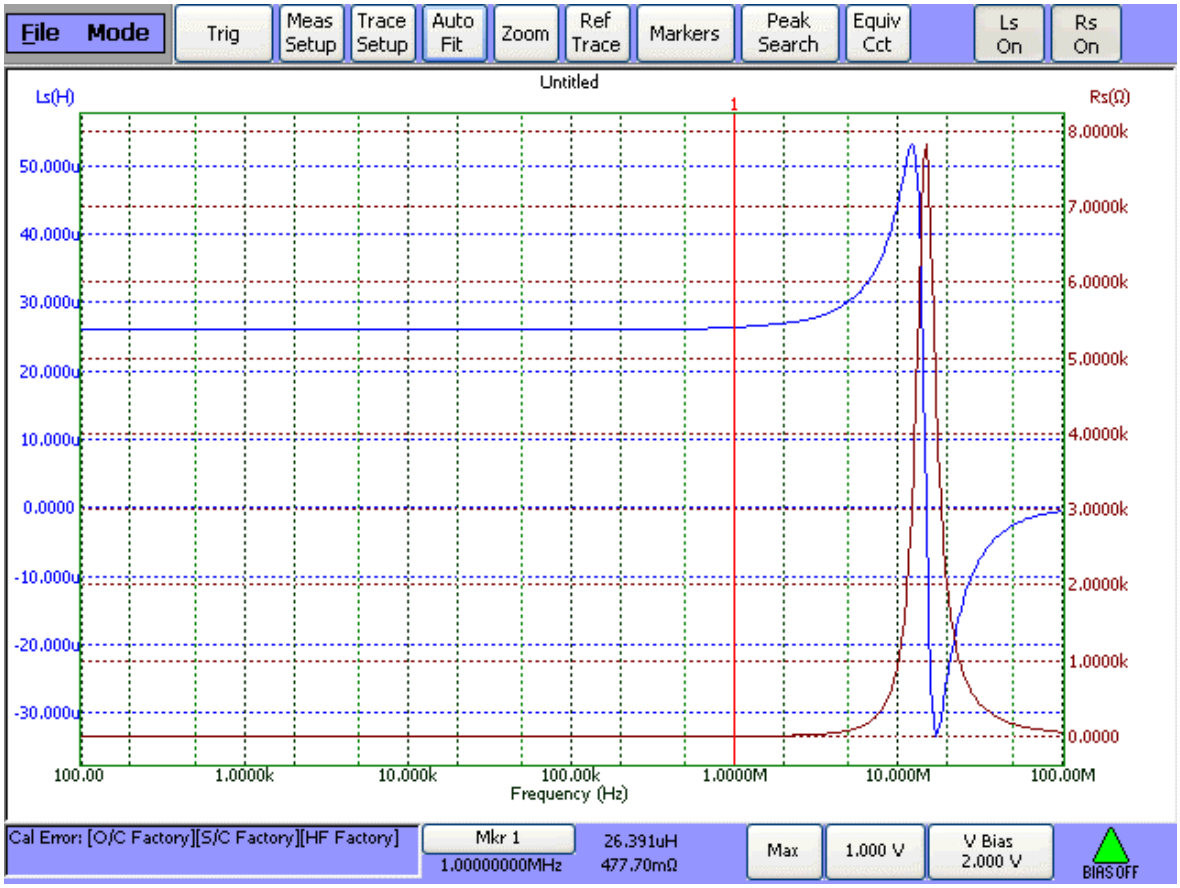

Figure 58 Self-resonant frequency measurement of choke.

The figure presents inductance and impedance of the choke in 100 Hz-100 MHz logarithmic scale. As is evident, close to and beyond 10 MHz and impedance and inductance rapidly rise then fall. The peak of impedance (brown curve in Figure 58) occurs at the self-resonant frequency of the choke. Since the resonance point is way beyond the designed operating range, it should not cause any issues. Similar results were observed for the other chokes.

5.2 Testing within the main board

The selected choke was hooked to the prototype board with control and specification explained in earlier parts. Digital control for the board is not perfected in the testing and was being developed and adjusted at the time. In Figure 59 is presented the board with choke attached.

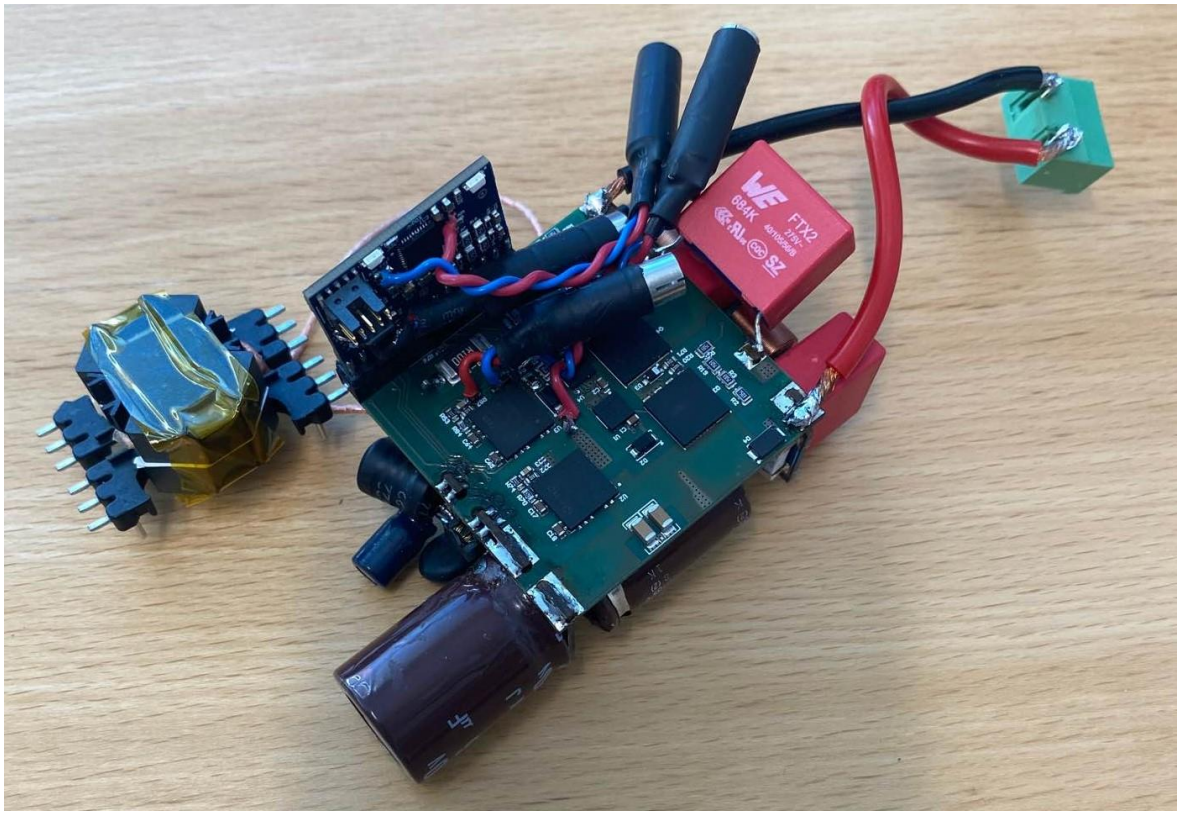

Figure 59 Totem-pole test board with inductor attached.

It was rapidly determined that the microcontroller is simply too slow for the up to 1 MHz f_{sw} range operation. Figure 60 presents oscilloscope view of full mains cycle. Purple and blue waveforms are the digitally generated hysteresis references, green is sensed current by the system and yellow is the actual inductor current.

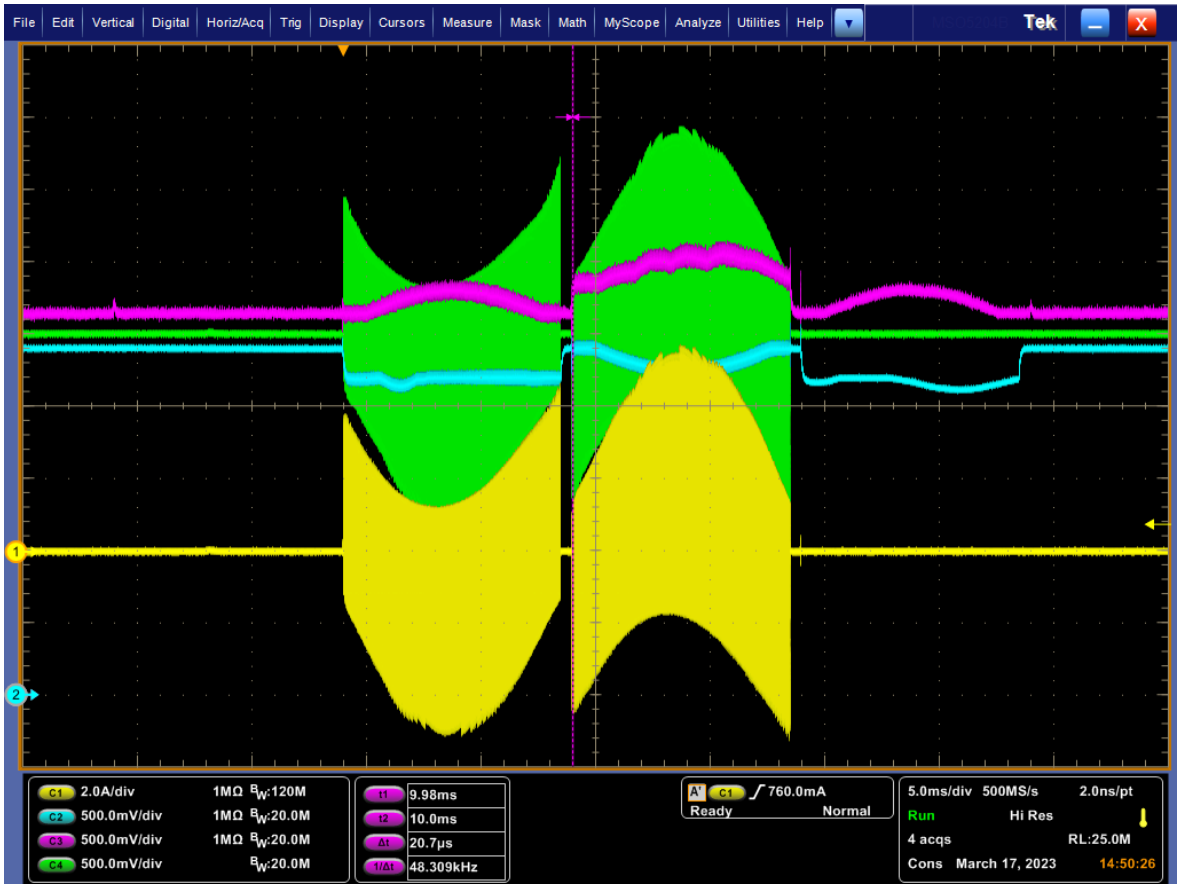

Figure 60 Full cycle oscilloscope view with 26 µH choke.

The current doesn't stay inside the envelopes at all and overshoots, as was also previously simulated in Figure 53. A detailed view is presented in Figure 61.

Figure 61 Detailed oscilloscope view of a switching cycle.

During the testing total delay of around 200 ns was observed, in the figure above Δt of 210 ns is measured. As it was determined that XMC1400 is too slow for the original desired frequency range, a new choke was designed for lower frequency range. The 80 µH inductance simulated in Figures 54 and 55 was determined to give acceptable results.

The new choke was built using the same RM 10 (LP) core, with 25 turns and l_g of 0.97 mm for estimated inductance of 80 µH. AWG 44 – 128 was used for winding. Since this time impedance analyser was not available, single-pulse test was used to determine the inductance of the new choke. By applying voltage pulse, it possible to determine the inductance from the current slope with

$$L = \frac{V_{\text{in}} \cdot \Delta t}{\Delta I} \tag{34}$$

Single-pulse test also give information about saturation of the core. When applying constant voltage, current increases linearly. When the core material begins to saturate, currents starts to behave nonlinearly. The core should not saturate, and current should behave linearly under the intended I_{pk} value, which in this design is 7.99 A. Figure 62 presents the performed single-pulse test.

Figure 62 Single-pulse test of the choke with targeted 80 µH.

With single-pulse test, the new choke was measured to 99 µH. F_{sw} will be lower, but there is expected less problems with propagation delay with higher inductance. The current (yellow) starts to behave nonlinearly at around 10 A, as the core starts to saturate. As the saturation point is beyond the intended I_{pk}, the core design should be good, and never saturate under normal operating conditions.

The effects of delay and compensation on f_{sw} can also be mathematically calculated instead of simulated. The effects and effectiveness of delay compensation is presented in Figure 63 for the new 99 µH choke for 100 % and 10 % loads.

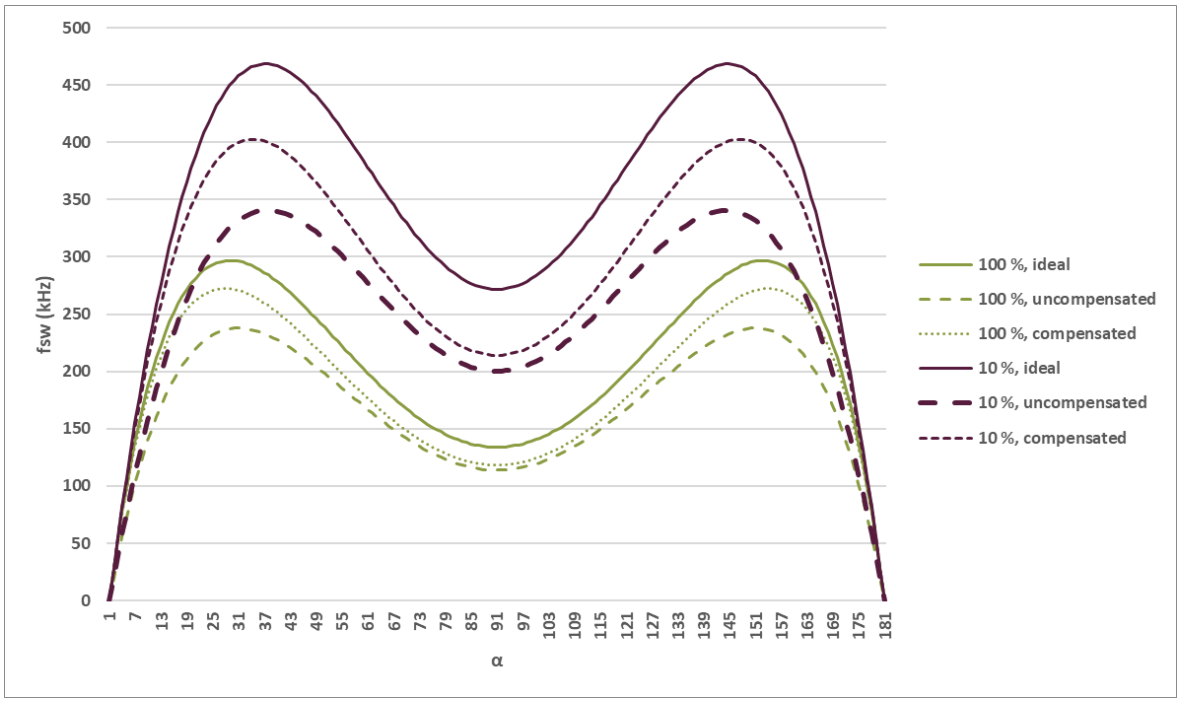

Figure 63 Effects of delay and compensation on f_{sw} with the new 99 µH choke.

Solid line represents ideal, dashed line uncompensated and dotted line compensated f_{sw}. With compensation, the real f_{sw} moves closer to the ideal design value. An ideally compensated waveform would be identical to the solid ideal line, however implementing such control in practice is difficult. Similar effect is presented in Figure 64 for hysteresis currents.

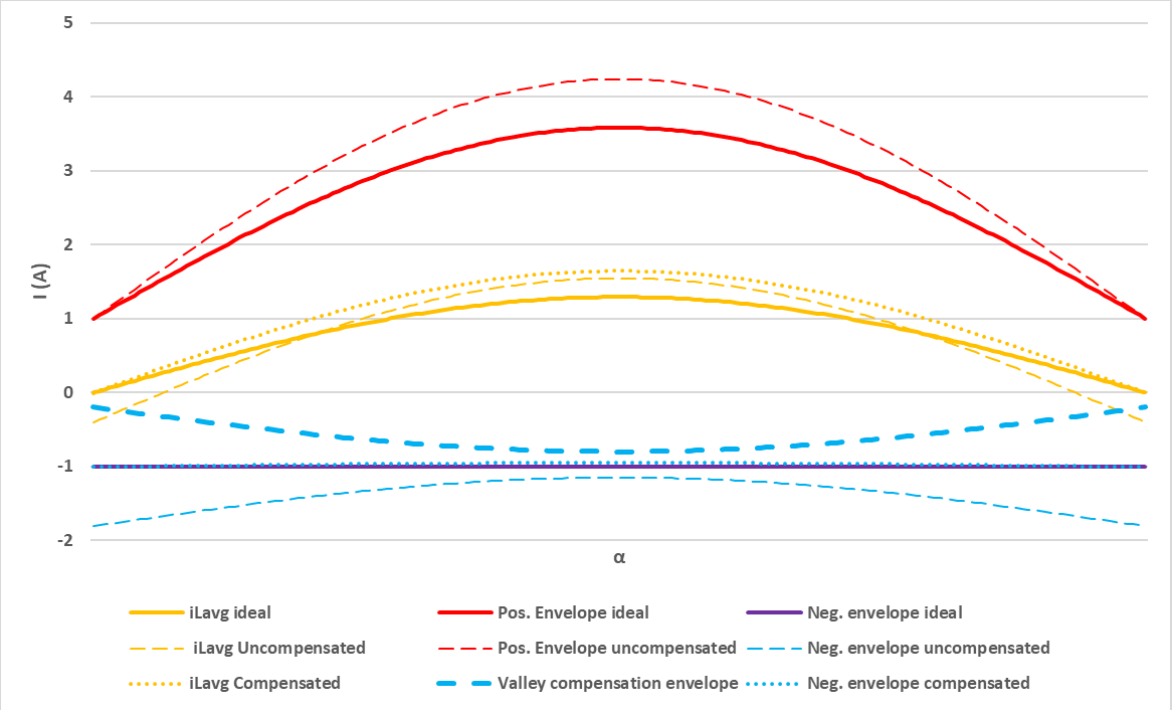

Figure 64 Effects of delay and compensation on 99 µH choke currents, 100 % load.

The figure is quite filled with data, but in addition of demonstrating the valley compensation shown in simulations, it also demonstrates the effects on the average current. The orange dashed line represents the uncompensated average current, which is negative on both ends. With compensation the resulting average current is always positive in this case, represented by the dotted orange line above it.

The new choke was attached to the board and tested. A full cycle view of hysteresis is presented in Figure 65, like in Figure 60.

Figure 65 Full cycle oscilloscope view with 99 µH choke.

Same as in Figure 60, purple and blue waveforms represent the digitally generated hysteresis references, green is sensed current and yellow is the real measured current. Compared to the 26 µH choke, the new choke performs much better as excepted, as there is less error in current and f_{sw}. The voltage loop of the control still needs work though, as the generated envelopes, and the resulting output current has quite a bit ripple content to it.

6 Conclusions

In this thesis the design of high switching frequency TCM operated totem-pole was demonstrated, with focus on the implementation of the main choke. By building correctly dimensioned choke it was possible to determine the feasibility of XMC1400 at high frequency, which ultimately led to the conclusion that the microcontroller is too slow. A new build with refined expectations for the microcontroller was tested, and it was determined that somewhere in the range of 300 kHz under nominal conditions the microcontroller can handle. For the original desired value of around 1 MHz a faster microcontroller would be needed. The work done in developing the design tools and knowledge is still not in vain though, as the developed tools could be used in future for further developing this design, or on other applications.

Due to time constraints the testing was very limited, only basic test of determining feasibility of XMC1400 for high f_{sw} was determined. No tests measuring the efficiency or PF were done, the key benchmarks of PFC converters. The thesis still gives a reasonable overview on the background of PFC converters and design phase of magnetics for a converter.

6.1 Future work

The immediate working point for future is to develop a working voltage loop. Without proper voltage loop operation other characteristics of the converter can’t be measured. When the voltage loop is properly implemented, it will be interesting to see how the losses compare to the estimated losses.

With a faster microcontroller it would be interesting to test how the converter and the magnetic parts perform in the original intended 1 MHz range, as high switching frequency is always a challenge for the inductor design. The smaller RM 7 choke was also left unused,

with proper control and faster microcontroller the difference in performance versus the bigger core would be interesting to measure.

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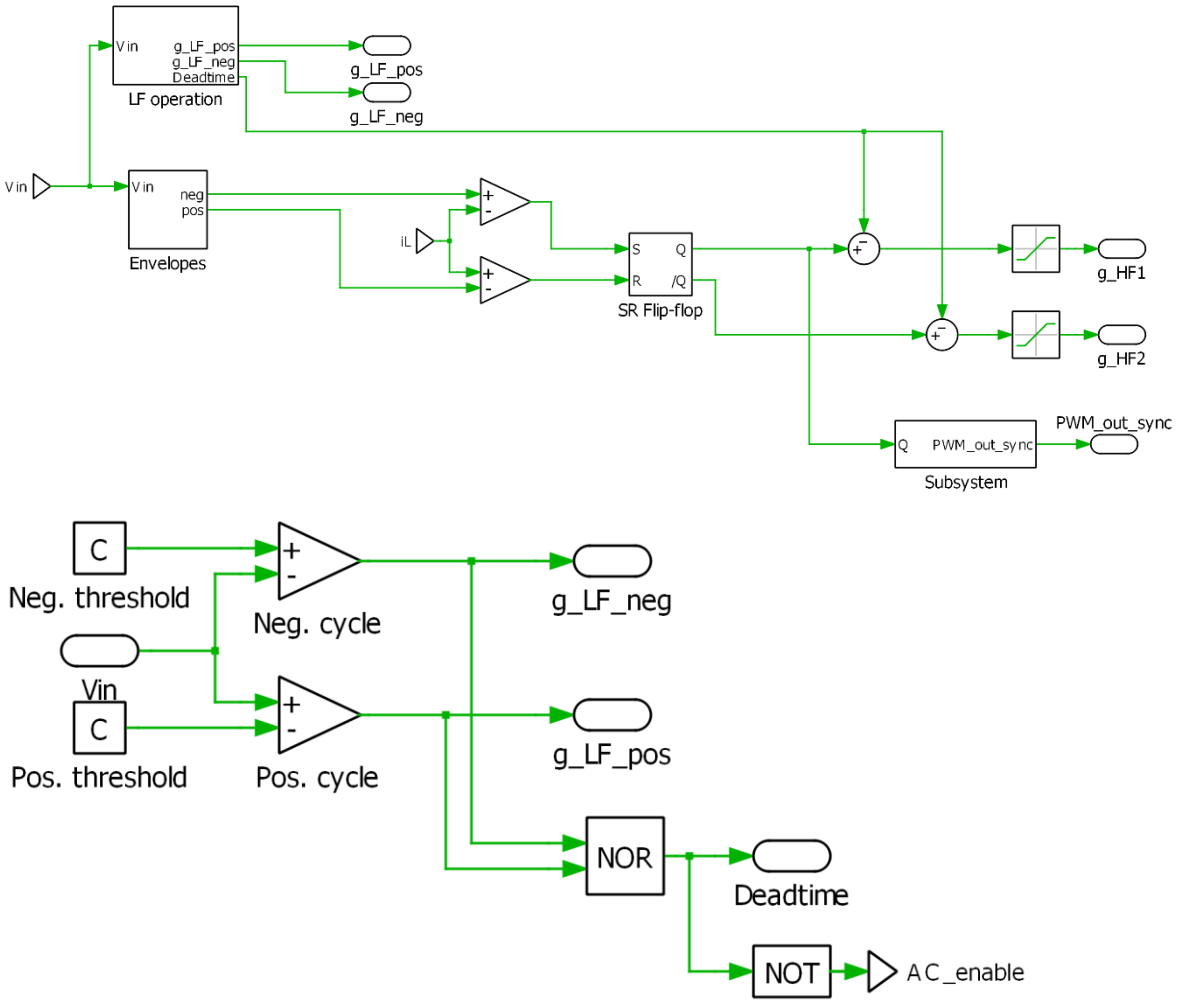
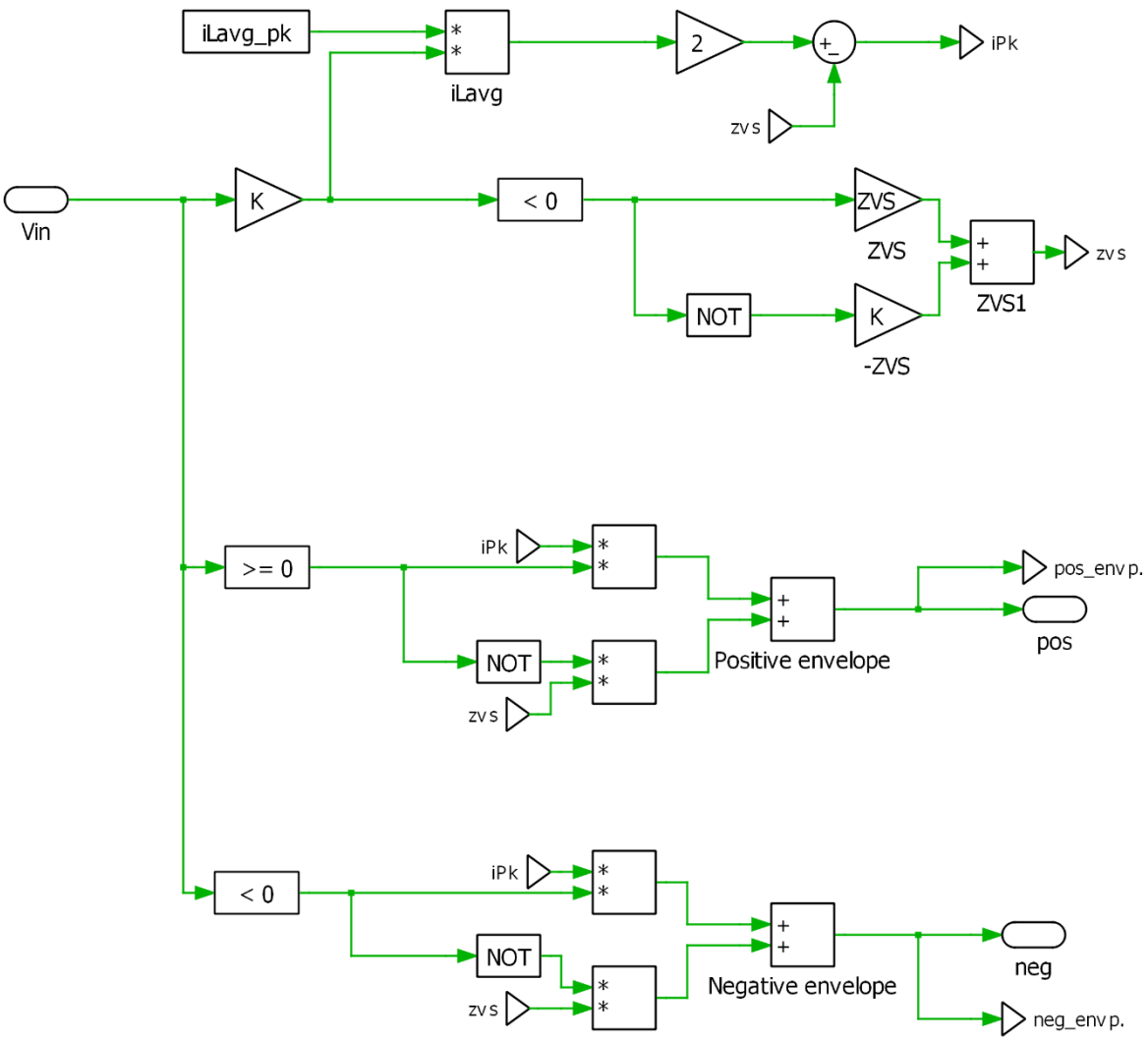
Appendix 1. Controls for the PLECS model of PFC totem-pole




iLavg_pk
iLavg
2
iPk
zvs
Vin
K
< 0
ZVS
ZVS
ZVS1
zvs
NOT
K
-ZVS
>= 0
iPk
NOT
zvs
Positive envelope
pos_envp.
pos
< 0
iPk
NOT
zvs
Negative envelope
neg
neg_envp.

Appendix 2. Parameters of considered cores.

Core	L_e (mm)	A_e (mm²)	V_e (mm³)	l_N (mm)	A_w (mm²)	b (mm)
PQ 16/11.6	27	42,1	1140	35	8,7	6,7
PQ 20/16	37,2	63,2	2360	44	21,0	10,3
PQ 26/20	44,4	122,6	5440	56	33,0	11,5
PQ 32/20	48,4	154,2	7460	66	47,0	11,5
RM 6 (LP)	21,8	37,5	820	30	13,5	4,5
RM 7	29,8	40,0	1190	36	22,4	8,4
RM 8 (LP)	28,7	64,9	1860	42	24,9	5,9
RM 10 (LP)	33,9	99,1	3360	52	34,5	6,7
RM 10	44	98,0	4310	52	41,5	12,4
RM 12 (LP)	42	147,5	6195	61	54,9	9