



Accelerated endurance testing of discrete SiC MOSFETs

Lappeenranta–Lahti University of Technology LUT

Degree Programme in Electrical Engineering, Master's Thesis

2023

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ABSTRACT

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Electrical Engineering

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Accelerated endurance testing of discrete SiC MOSFETs

Master's thesis

2023

43 pages, 17 figures, 5 tables and 3 appendices

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Keywords: SiC MOSFET, endurance test, loss calculations

The aim of this thesis was to study the temperature swing effect in an accelerated endurance test with SiC MOSFET. Due to a gate driver issue, the scope was changed to improving the test setup.

In the thesis SiC MOSFETs' common failure mechanisms, loss calculations, and device health monitoring was studied. A test setup for the experimental part was assembled during the thesis. A heat sink for the test setup was designed based on loss calculations. Also, the cycle times were estimated in the calculations.

Minor weaknesses of the setup were noted during assembling the test setup and in the initial tests. Weaknesses were analysed and improvement suggestions were presented. The initial test confirmed that the cycle time estimation was successful, the difference between calculated and measured heating time was 1 second and 16 seconds in cooling time. The cycle time was about 8 minutes.

Major improvements suggested in this thesis were drawing schematic for drain-source voltage online measurement and designing a test profile for DC-DC side. The test profile was simulated, and the results were promising.

TIIVISTELMÄ

Lappeenrannan–Lahden teknillinen yliopisto LUT

LUT Energiajärjestelmät

Sähkötekniikka

Anssi Lintunen

Diskreettien piikarbidikanavatransistorien kiihdytetty kestotestaus

Diplomityö

2023

43 sivua, 17 kuvaa, 5 taulukkoa ja 3 liitettä

Tarkastajat: Professori Pertti Silventoinen

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Avainsanat: Piikarbidikanavatransistori, kestotesti, häviöiden laskenta

Tämän diplomityön tavoitteena oli selvittää lämpötilamuutosten vaikutusta kiihdytetyssä kestotestissä piikarbidikanavatransistoreissa. Koeasetelman hilaohjaimen ongelmien myötä työn tulokset painottuivat koeasetelman kehitykseen.

Työssä pureuduttiin piikarbidikanavatransistoreiden vikaantumismekanismiin, häviöiden laskemiseen sekä komponentin kunnan seurantametteihin. Työn aikana myös rakennettiin kokeelliseen osuuteen vaadittava koeasetelma. Laskettujen tehohäviöiden perusteella työssä laskettiin sopiva jäähdytyslementti sekä arvioitiin sykli aika.

Koeasetelman rakentamisen aikana sekä kokeellisen osuuden alussa kerättiin kehityskohteita, jotka esitellään työn parannukset -kappaleessa. Kokeellisessa osiossa voitiin todeta, että sykli ajan arviointi onnistui. Ero lasketussa ja mitatussa lämpenemisajassa oli yksi sekunti ja viilennysajassa 16 sekuntia, koko sykli ajan ollessa noin kahdeksan minuuttia.

Työssä tarkoituksena oli myös etsiä sopiva kytkentä mittaamaan johtumistilan lähteen ja nielun välistä jännitettä. Kytkentä onnistuttiin löytämään sekä simuloinnilla tukemaan sen valintaa. Työssä muodostettiin myös ohjausprofiili DC-DC puolen komponenttien testaamiseen. Simuloinnin perusteella komponenttien johtumis- ja kytkentähäviöt olivat oikeaa suuruusluokkaa.

ALKUSANAT

Tämän työn kokeellinen osuus toteutettiin Kempower Oyj:n laboratorio tiloissa. Haluan kiittää tästä mahdollisuudesta sekä annetuista resursseista. Kiitokset kaikille mukana olleille. Erityiset kiitokset Heikki Järvisalolle ja Dai Trinhille raiteilla pitämisestä sekä eteenpäin työntämisestä. Mielenkiintoisen aiheen ehdottamisesta kiitän Petri Korhosta.

Yliopiston puolelta tarkastajina olivat Pertti Silventoinen ja Aleksi Mattsson. Suuri kiitos heille hyvistä kommentteista sekä antoisista keskusteluista. Kiitos LUT-yliopistolle mielenkiintoisen ja monipuolisen opetuksen tarjoamisesta. Paljon on tullut uusia ystäviä kursseilta sekä muusta opiskeluelämästä.

Kiitokset perheelleni, ystäväilleni ja puolisololleni Annalle vankkumattomasta tuesta ja kannustamisesta!

Anssi Lintunen

Lahdessa 4.12.2023

SYMBOLS AND ABBREVIATIONS

Symbols

α	Convection coefficient
D	Duty cycle
E_{cond}	Conduction energy
E_{on}	Turn-on energy
E_{off}	Turn-off energy
f_{sw}	Switching frequency
h	Fin height
I_{D}	Drain current
I_{peak}	Peak current
l	Heat sink length
λ	Thermal conductivity
ν	Kinematic viscosity
Nu	Nusselt number
P_{cond}	Conduction losses
$P_{\text{switching}}$	Switching losses
Pr	Prandtl number
$q_{\text{convection}}$	Convection heat flow
$R_{\text{DS,on}}$	Conduction state drain-source resistance
R_{θ}	Thermal resistance
Re	Reynolds number
s	Fin gap

T_{ambient}	Ambient temperature
T_j	Junction temperature
T_s	Heat sink surface temperature
$t_{\text{d(off)}}$	Turn-off delay time
$t_{\text{d(on)}}$	Turn-on delay time
t_f	Fall time
t_{on}	Turn-on time
t_r	Rise time
V_{DS}	Drain-source voltage
$V_{\text{DS,on}}$	Conduction state drain-source voltage
$V_{\text{DS,off}}$	Off-state drain-source voltage
V_{GS}	Gate-source voltage

Abbreviations

AC	Alternating Current
AFE	Active Front End
BTI	Bias Temperature Instability
DC	Direct Current
DUT	Device under test
DVCC	Drain-source Voltage Clamp Circuit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NBTI	Negative Bias Temperature Instability
PBTI	Positive Bias Temperature Instability
PWM	Pulse Width Modulation

Si	Silicon
SiC	Silicon Carbide
SMD	Surface Mount Device

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1 Introduction

The world of power electronics is very dynamic, which means decisions must be made quickly. One of those decisions can be component selection. The component validation process is a part of the component selection. Endurance testing is a vital part of the component validation process. The testing results show if the component is durable enough for the real system. If proper testing is not performed and wrong components are chosen, it can result in very early system failure. These kinds of malfunctions may cause bad reputation for the manufacturer. (NIST/SEMATECH, 2012)

The endurance test should be long enough to be reliable. Standard endurance tests have been traditionally quite time consuming. For example, Infineon performed a 3000 h test to check the robustness of the CoolSiC™ MOSFETs (Infineon, 2020). This means more than four months must be used purely for endurance testing.

This thesis studies the accelerated endurance testing of discrete silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFET). SiC as a power semiconductor material has some advantages compared to traditionally used silicon (Si), for example high-voltage operation and fast switching can be combined. SiC devices are also more radiation resistant and provide better high-temperature operation than Si devices. However, since SiC-based devices diverge from traditional Si devices, they require different tests. SiC MOSFETs' problem has been reliability issues. (Infineon, 2020)

1.1 Research problem

This thesis aimed to define a reliable method for a quicker endurance testing and the scope was on analysing relations of test parameters and results. Due to hardware issues, the schedule became too tight for the original plan, so the scope of the thesis was re-evaluated. The new investigation area is improving test setup, and the primary outcomes of the thesis are:

- The test profile used in the setup was designed for the active front end (AFE) side. In the future, a similar test could be performed using the DC-DC side. Since a similar profile for the DC-DC side does not exist, one will be carried out in this thesis.
- A schematic level design of an online drain-source voltage online measurement circuit.
- Calculations for MOSFET's switching and conduction losses, heat sink dimensioning, and cycle times.

Also, some more minor improvements to hardware and software will be presented. The general idea is to make the test setup more replicable, useful, and convenient.

1.2 Research framing

In this thesis, an endurance test setup for TO-247 packaged SiC MOSFETs will be built. The initial idea was to have three test batches with different minimum temperatures on the cycle and analyse the effect of the swing temperature on the lifetime. Due to the hardware issues, the schedule became too tight and new framing was needed. The new frame was to debug hardware issue and carry out hardware and testing improvements. Test setup will be replicated after this thesis, and relation of swing temperature will be analysed then.

1.3 Structure of the thesis

The thesis is divided into theory, testing, and improvements sections. In the theory chapter general information of SiC MOSFET, common failure mechanisms, accelerated endurance test, loss calculation, and device health monitoring are presented. The testing chapter describes the test setup components, thermal calculations, test strategy, and test software. The improvements chapter consists of solutions to issues which have appeared during the thesis work.

1.4 Research methods

In the theory chapter, literature was used for information acquisition. The heat sink dimensioning and cycle time estimation calculations were performed using MATLAB software. Values for the calculations were found from datasheets. The test setup assembly and debugging were both done in Kempower's laboratory. The DC-DC cycling profile was investigated using gecko simulation software. Schematics were drawn using Circuit LAB online tool.

2 Theory

Early SiC MOSFETs' problem was a high number of gate-oxide failures, which caused bad reputation for reliability for a long time (Infineon, 2020). However, SiC MOSFETs still are a promising option for traditional Si MOSFETs. SiC MOSFETs have the following features making them potential alternatives compared to traditional Si devices:

- Combined high breakdown voltage and fast switching.
- More cosmic radiation resistant.
- Better high-temperature operation.

2.1 Common failure mechanisms

Gate oxide degradation is the main reason for SiC MOSFET ageing (Pu et al., 2022). As Si devices accumulate charge in the oxide, SiC devices accumulate charges in the defects which can be found in the region near the SiC-SiO₂ interface. These are so-called near interface oxide traps. The accumulation of negative charges to this region will decrease the effective electric field across the gate oxide. Weaker effective electric field affects the forming of the inversion channel in MOSFET. (Karki and Peng, 2018)

Gate oxide degradation increases threshold voltage, gate plateau voltage and gate plateau time, which then increases the losses and switching times of the device (Karki and Peng, 2018). Gate oxide degradation also significantly affects the turn-on delay (t_{don}) and turn-off delay (t_{doff}) times (Kim, Kwak and Choi, 2022). Figure 1 shows a typical turn-on waveform of a power MOSFET.

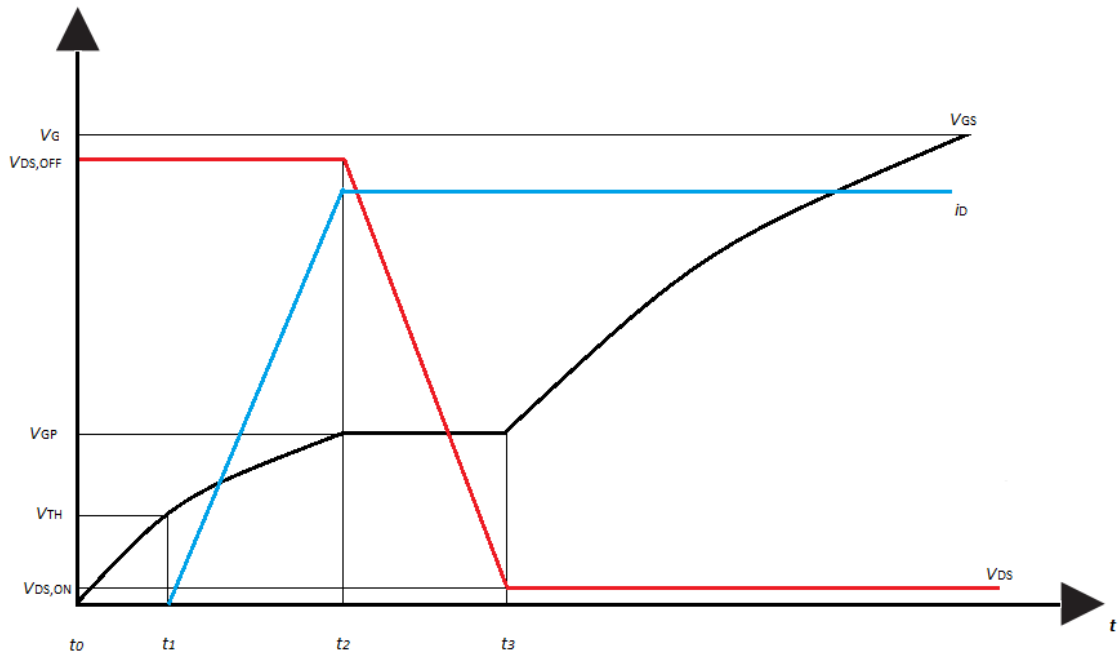


Figure 1. Turn-on waveforms of a MOSFET (Karki and Peng, 2018).

The black line is the gate-source voltage (V_{GS}), the blue line is the drain current (I_D), and the red line is the drain-source voltage (V_{DS}). The turn-on delay ($t_{d(on)}$) is time between t_1 and t_0 , the rise time (t_r) is time between time t_2 and t_1 , and the gate plateau time (t_{GP}) is the time difference between t_3 and t_2 . The increased t_{GP} decreases $\frac{V_{DS}}{dt}$ which is the reason for the longer switching time.

Bias temperature instability (BTI) is about threshold voltage drift. That means $R_{DS,on}$ varies while $V_{GS,on}$ stays constant. Due to increased channel resistance, losses increase which causes excess heat. Since the device becomes hotter, its lifetime can be degraded. (Infineon, 2020)

BTI occurs due to the oxide traps in the SiC-SiO₂ interface. There are two types of BTI: positive bias temperature instability (PBTI) and negative bias temperature instability (NBTI). In PBTI, threshold voltage increases, which causes more conduction losses and in NBTI, threshold voltage decreases, increasing the risk of undesirable switching behaviour as being in a conducting state when it should not (Kim, Kwak and Choi, 2022). After the voltage stress in the gate ends, traps are recovered and they release electrons or holes, depending on the case. Electrons are released after $V_{GS} > 0$ stress test and holes after $V_{GS} <$

0 stress test. Recovery can also be incomplete and cause permanent threshold voltage shift (Ortiz Gonzalez and Alatisse, 2019).

2.2 Accelerated endurance test

In accelerated life tests, components are generally operated at high stress levels. Also, observing the failure data is a crucial part of the test (NIST/SEMATECH, 2012). In this thesis, the high stress will be caused by high temperature swings.

The International Electrotechnical Commission (IEC) has defined standard cycling strategies for component testing. IEC 60749-34 defines a standard power cycling test and IEC 60749-25 defines a standard temperature cycling test. IEC 60749 series generally defines a standard for semiconductor mechanical and climatic tests. The schematic for the standard power cycling test is shown in Figure 2. (IEC, 2010) (IEC, 2003)

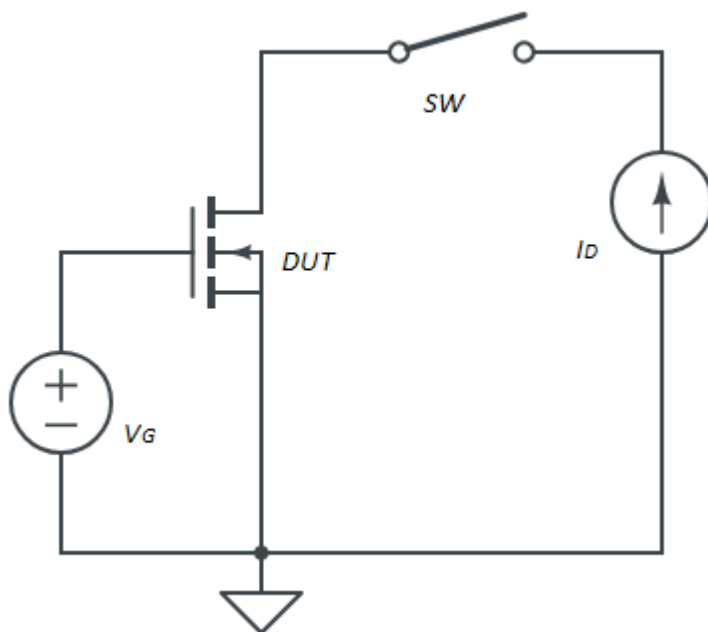


Figure 2. Standard power cycling test schematic (IEC, 2010).

In the standard power cycling test, the device under test (DUT) is in a conductive state throughout the test. This means the required gate voltage (V_G) must be supplied continuously from an external DC power supply. The power cycling is done by externally applied power

which will be switched on and off periodically. Thus, the flowing current causes periodical internal heating in DUT.

In the standard temperature cycling, heating is caused externally using a heat chamber. The typical cycle rate is 1-3 cycles per hour.

2.3 Loss calculations

Cooling is a vital thing in using power semiconductors. The cooling system should be optimised to be cost-effective. Also, the simplest possible solution is desirable, since it has fewer defective parts. For example, it would not be wise to use liquid cooling if air cooling would be enough for the application. Thermal resistance, junction temperature, and ambient temperature define power dissipation (Rode et al., 2021). For optimised cooling, losses must be known.

Semiconductor loss calculations can be divided into two parts: conduction and switching losses. Conduction losses can be defined by the conduction state channel resistance $R_{DS,on}$ and the drain current I_D . The idea is to calculate the conduction energy loss and multiply it by frequency. Equations in this section are based on Infineon (2002). Conduction losses can be calculated using the following equations:

$$E_{cond} = \int_0^{t_{on}} R_{DS,on} * I_D^2 dt, \quad (2.1)$$

$$P_{cond} = E_{cond} * f_{sw}, \quad (2.2)$$

where E_{cond} is the conduction energy in switching period, f_{sw} is the switching frequency. The switching losses can be separated into turn-on and turn-off losses. The exact mathematical expressions for turn-on and turn-off energies are shown in the following equations:

$$E_{\text{on}} = \int_0^{t_{d(\text{on})} + t_r} v_{\text{ds}}(t) i_{\text{d}}(t) dt, \quad (2.3)$$

$$E_{\text{off}} = \int_0^{t_{d(\text{off})} + t_f} v_{\text{ds}}(t) i_{\text{d}}(t) dt. \quad (2.4)$$

The graphical expression for the turn-on calculation is shown in Figure 3. Thus, the grey area in the graphical expression is calculated in equation 2.3.

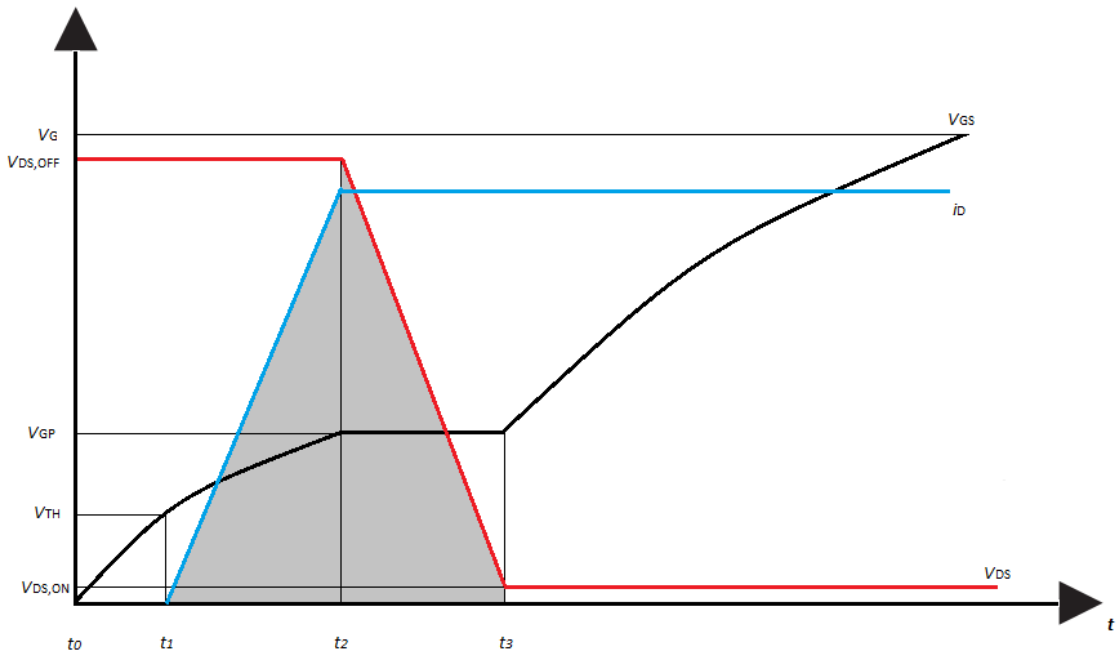


Figure 3. Graphical expression for the turn on energy calculations.

The expressions for $t_{d(\text{on})}$ and t_r are shown in Figure 3, $t_{d(\text{on})}$ is time between t_1 and t_0 and t_r is time between time t_2 and t_1 . When the switching energies are known, the switching power loss can be obtained by the following equation:

$$P_{\text{switching}} = (E_{\text{on}} + E_{\text{off}}) * f_{\text{sw}}. \quad (2.5)$$

2.4 Device health monitoring

Measuring $R_{DS,on}$ online is a fundamental part of device health monitoring. $V_{DS,on}$ and I_D must be measured for $R_{DS,on}$. Measuring I_D is relatively simple compared to $V_{DS,on}$, so this section discusses methods to measure $V_{DS,on}$. Since the measured differences are quite minimal, an accurate measurement circuit must be used. Also, a wide temperature spectrum causes difficulties. High temperatures may disturb measurements since component values are temperature dependent. Also, components in the circuit may be heated unevenly which makes the phenomenon unpredictable. The measurement circuit must be clamped, since the off-state drain-source voltage ($V_{DS,off}$) over the device can easily be over 600 V. Yu, Wang and Ahmed (2020) studied clamp circuits and their accuracies, and also presented a new drain-source voltage clamp circuit (DVCC) design.

Two common circuits for V_{DS} online measurement exist. DZD is a DVCC based on Zener diode and D2D is a DVCC based on two diodes. The basic idea of the DVCC is to show $V_{DS,on}$ to the processor during conduction and clamped voltage during $V_{DS,off}$. Schematic for the Zener-based DVCC can be seen in Figure 4.

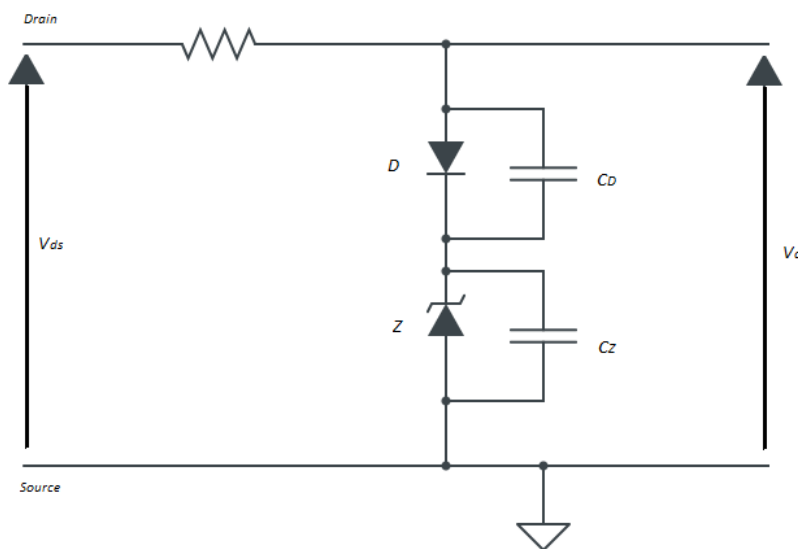


Figure 4. Schematic for Zener-based DVCC (Yu, Wang and Ahmed, 2020).

The Zener-based DVCC is shown in Figure 4. During off-state, the voltage is clamped to the same level as the sum voltage drop of both diodes. The main reason for using the diode in

series with the Zener is to reduce the total parasitic capacitance. The $V_{DS,on}$ must be smaller than the clamping voltage, otherwise $V_{DS,on}$ would be clamped and the DVCC will not show the correct value as output voltage (V_o). The RC circuit also causes a time constant, so there is a delay in the measurement. (Gelagaev, Jacqmaer and Driesen, 2015)

The output voltage of the Zener-based DVCC can be calculated using the following equation.

$$V_o = V_{DS,on} - R_1 i_{leak}, \quad (2.6)$$

where i_{leak} is reverse leakage current of the Zener diode and R_1 is the resistance of resistor. The difference between V_o and $V_{DS,on}$ is relatively small at lower temperatures and high $V_{DS,on}$. But when temperature increase, i_{leak} increases which grows the error voltage over R_1 . Also the value of R_1 is temperature dependent which affects the error voltage. The schematic for two diode based DVCC can be seen in Figure 5.

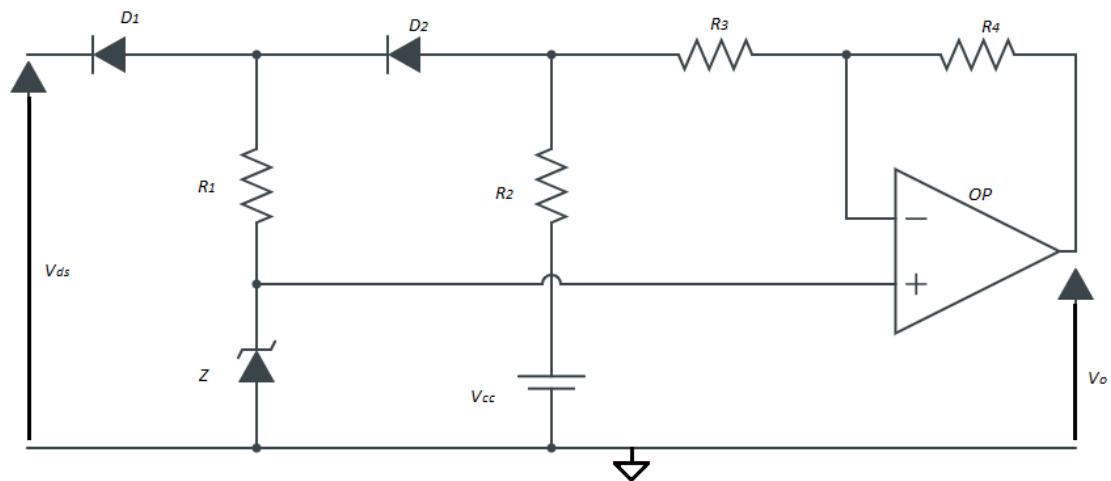


Figure 5. Schematic for two diode DVCC (Yu, Wang and Ahmed, 2020).

The DVCC based on two diodes is shown in Figure 5. The equation for V_o is shown in the following equation.

$$V_o = V_{DS,on} + V_{D1} - \frac{R_4}{R_3} * V_{D2}, \quad (2.7)$$

where V_{D1} and V_{D2} are the forward voltages of D_1 and D_2 . The forward current and temperature affect the forward voltage. The difference of forward voltages is relatively smaller at lower temperature than at higher temperatures. Different distances to the thermal source cause the difference between diode temperatures. Thus, forward voltages are different at higher temperatures, which grows the error.

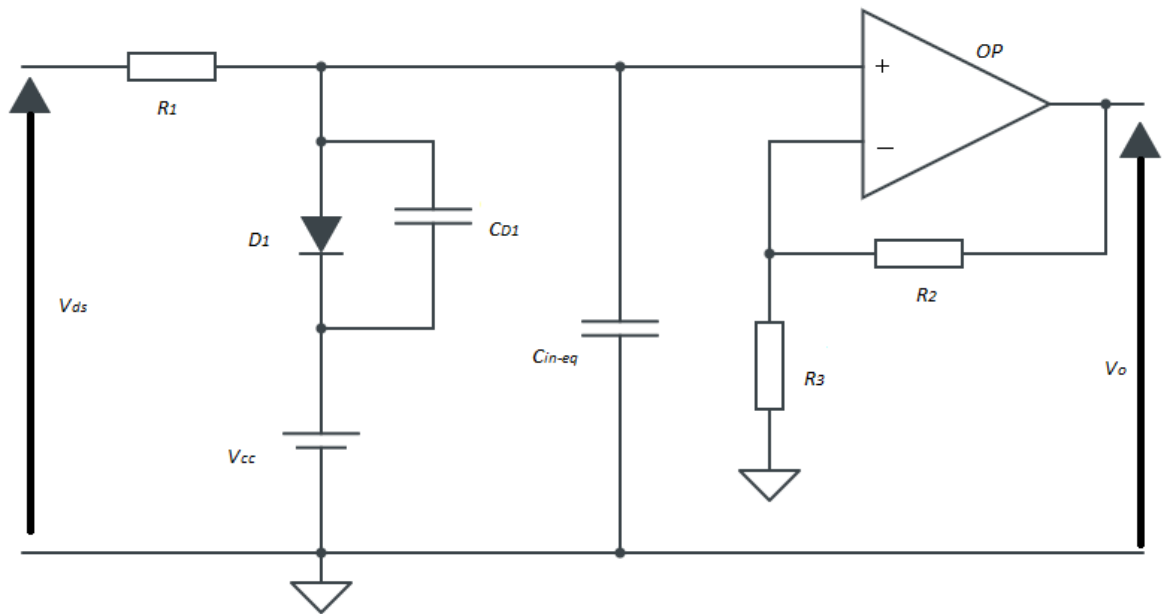


Figure 6. Schematic for proposed DVCC (Yu, Wang and Ahmed, 2020).

Compared to the DVCCs presented above, the proposed DVCC is more accurate throughout the temperature range, since no diodes affect the $V_{DS,on}$ measurement. D_1 is blocked by the voltage source V_{cc} , which makes the equation simpler compared to the other DVCCs. V_o for the proposed DVCC can be solved by following equation.

$$V_o = \left(1 + \frac{R_4}{R_3}\right) * V_{DS,on}, \quad (2.8)$$

Yu, Wang and Ahmed (2020) studied the accuracies of presented DVCCs. Table 1 shows the simulated measurement errors. The range of $V_{DS,on}$ in the simulations was from 36 mV

to 2.5 V. In the actual system measurements, the maximum error of the proposed DVCC appeared at 100 °C and 36 mV, with an error of 0.49 %.

Table 1. DVCCs' errors in the simulation (Yu, Wang and Ahmed, 2020)

Type	Total error at 25 °C, [%]	Total error at 75 °C, [%]	Total error at 100 °C, [%]
DZD	18.8	20.7	21.9
D2D	19.3	19.2	19.1
Proposed DVCC	0.13	0.19	0.39

DVCCs were also simulated in this thesis. The DVCC component values were picked from Yu, Wang and Ahmed (2020). However, all the values were not presented, so the following simulation results are just directional, and accuracies cannot be compared. The optimisation of the components will be a topic for further investigation.

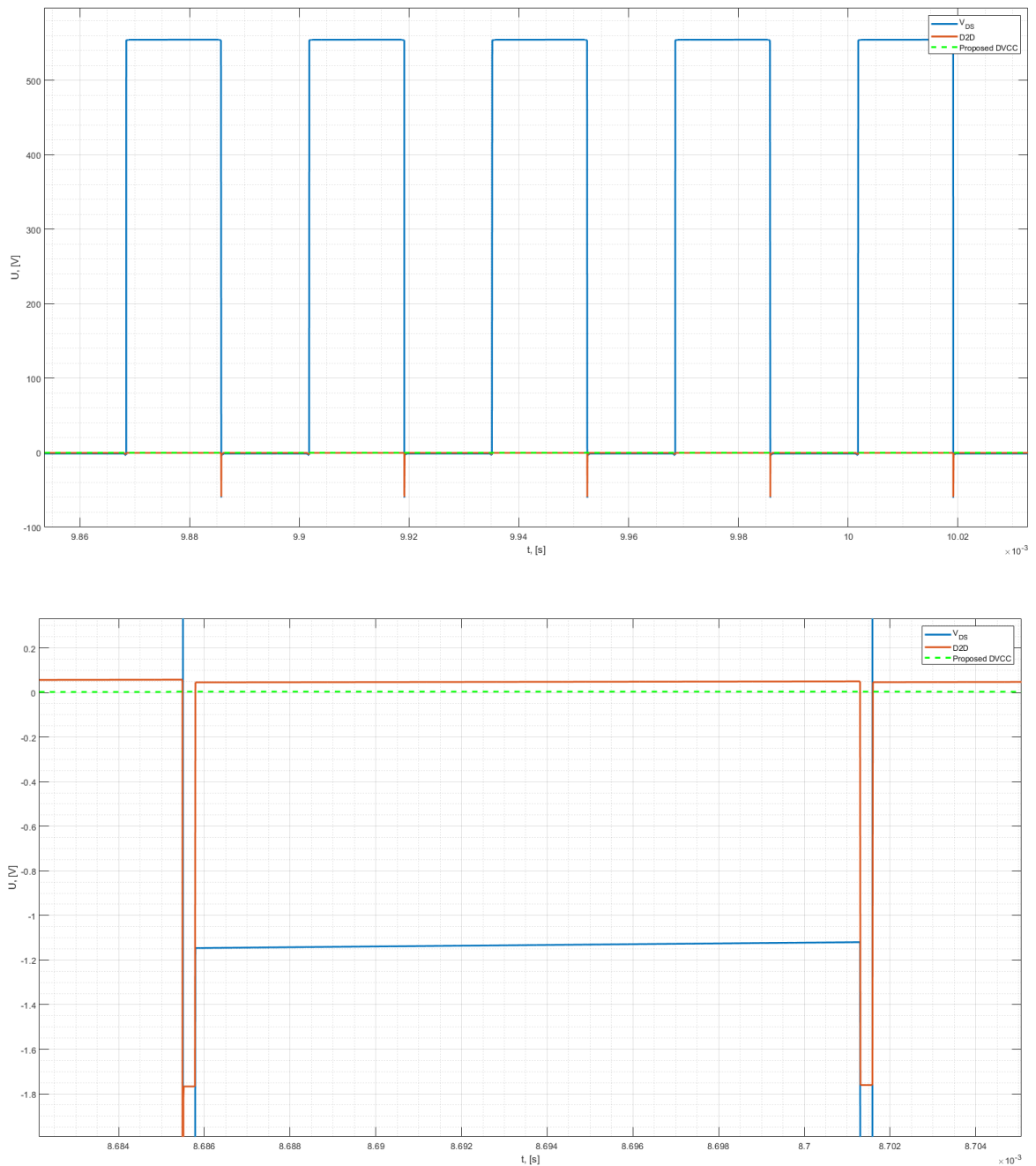


Figure 7. D2D and proposed DVCC compared, full scale (top) and zoomed in (bottom).

Figure 7 shows V_{DS} on blue line, voltage measured by the two-diode based DVCC on red line, and voltage measured by the proposed DVCC on dashed green line. The two-diode based DVCC have much higher negative overshoot than the proposed DVCC. Figure 8 shows the proposed DVCC behaviour.

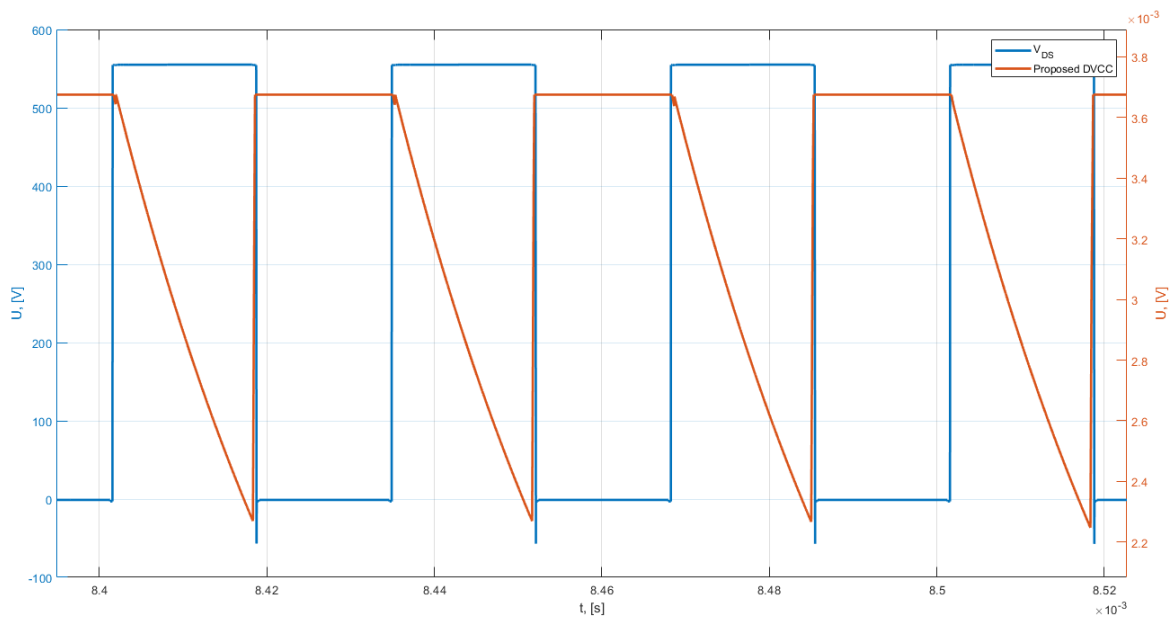


Figure 8. Behaviour of the proposed DVCC.

The blue line is V_{DS} and the left y-axis describes its value. The red line is V_O of the proposed DVCC and its value is in the right y-axis. The difference between minimum and maximum at that point is about 1.4 mV which is very minimal compared to two-diode based DVCC's 60 V negative overshoot. Maximum V_O must be sampled by the analog-to-digital converter at the flat area.

Before starting the endurance test, the limit for the $R_{DS,on}$ increase can be set. When the limit is achieved, one may want to stop the test and do some further investigations. One option for further investigation could be checking the DUT using radiography.

3 Endurance test

The initial idea was to build three setups and perform three endurance tests with different temperature swings. Due to hardware issues the schedule would have been very tight, so only one was eventually built and used in the test. Initial test parameters are shown in Table 2.

Table 2. Test parameters

Parameter	Value
DC Link voltage	510 V
Load current	38 A
Heat sink swing temperature	50 °C
Number of DUTs	6

In the standard temperature cycling strategy, heat comes from an external source. However, in this thesis a modified strategy will be used, where conduction and switching losses of the DUT will cause the heat. Because the switching losses are neglected in the standard power cycling, the modified strategy imitates a real system better. Since the power will not be switched off, the DUTs will be cooled with forced convection. Devices will be tested in the three-phase inverter mode. To minimize power consumption during the test, the switch control strategy will be modified to accommodate losses only in the semiconductor devices.

3.1 Setup

The setup consists of the following parts: platform card, gate driver card, power control card, cycle control unit, FET card, and load. The block diagram for the test setup is shown in Figure 9. Picture of the test setup can be found in Appendix I.

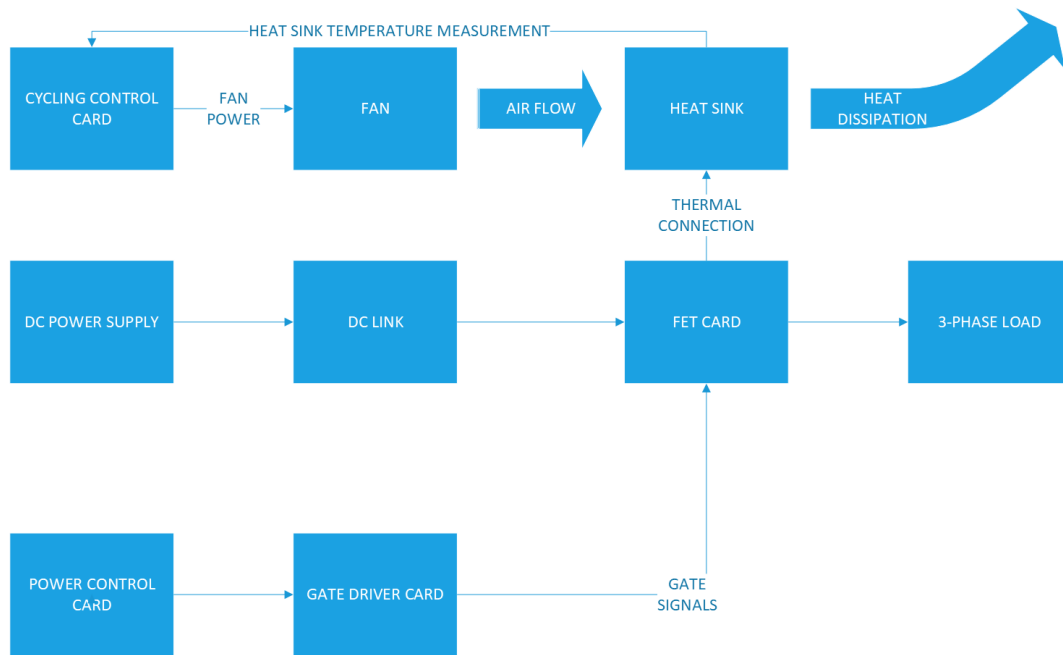


Figure 9. Test setup block diagram.

Platform card was the central part of the setup. It was developed for major topologies. For example, use as an active front end and produce high frequency AC. In this test, AFE was used in the inverter mode. The schematic for the test setup is shown in Figure 10.

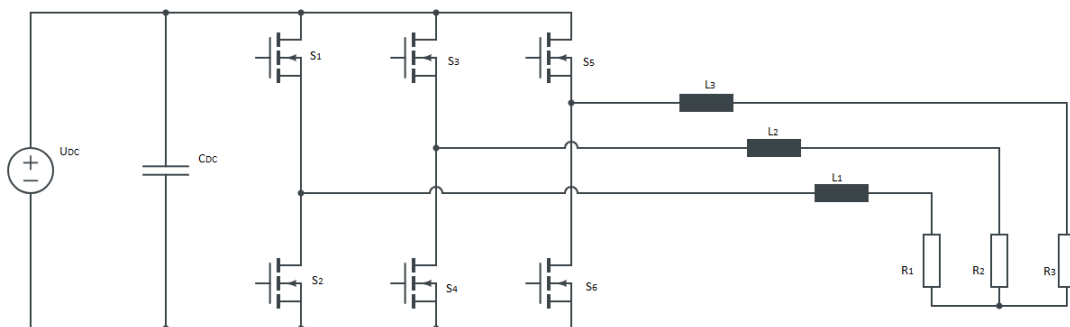


Figure 10. Schematic for the test setup.

DC was supplied from the external DC power supply to the platform card, converted to three-phase AC in the converter unit and supplied to the three-phase RL load. Main power side components can be seen in Figure 11; definitions are in the Table 3.

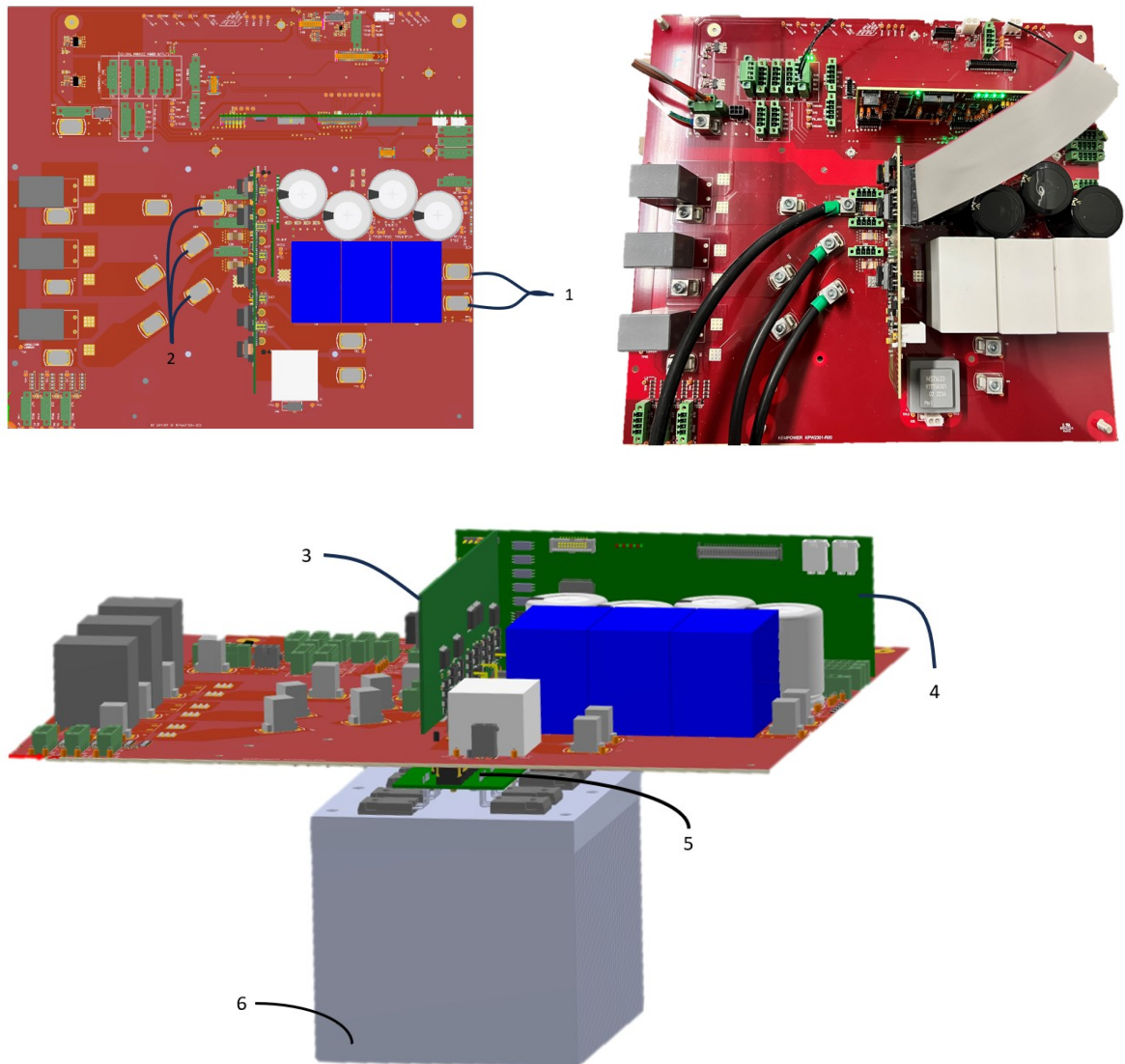


Figure 11. Test setup power side.

Table 3. Power side component definitions

Index	Definition
1	DC Link input
2	Connectors for 3-phase load
3	Gate driver card
4	Power control card
5	FET card
6	Heat sink

3.2 Control

The control signals of the switches were generated in the power control card. The setup includes an option for feedback signals from the power side, but this feature was not in use, so the control signal was constant. The signal was 50 % duty cycle Pulse Width Modulation (PWM) with small variation. PWMs, drive enable signal, gate power voltage, and +3.3V drive voltage were supplied to the gate driver card, generating gate-source voltages to MOSFETs and provided a basic isolation to control parts. The gate driver card is shown in Figure 12.

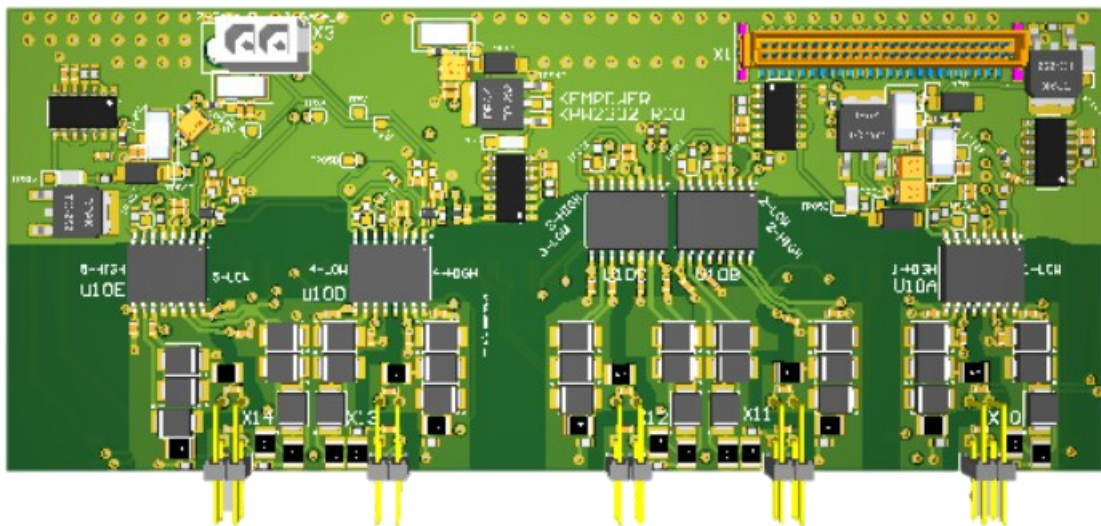


Figure 12. Gate driver card.

The converter unit includes the FET card and the heat sink. The FET card is connected to the platform card and the gate driver card. The DC link connection was performed using Würth PRESS-FIT couplers. The FET card was connected to platform card using Harting modulars, the gate driver card by pin headers.

The cycle control unit measures the heat sink temperature and controls it by fans. The cycle control card is shown in Figure 13.

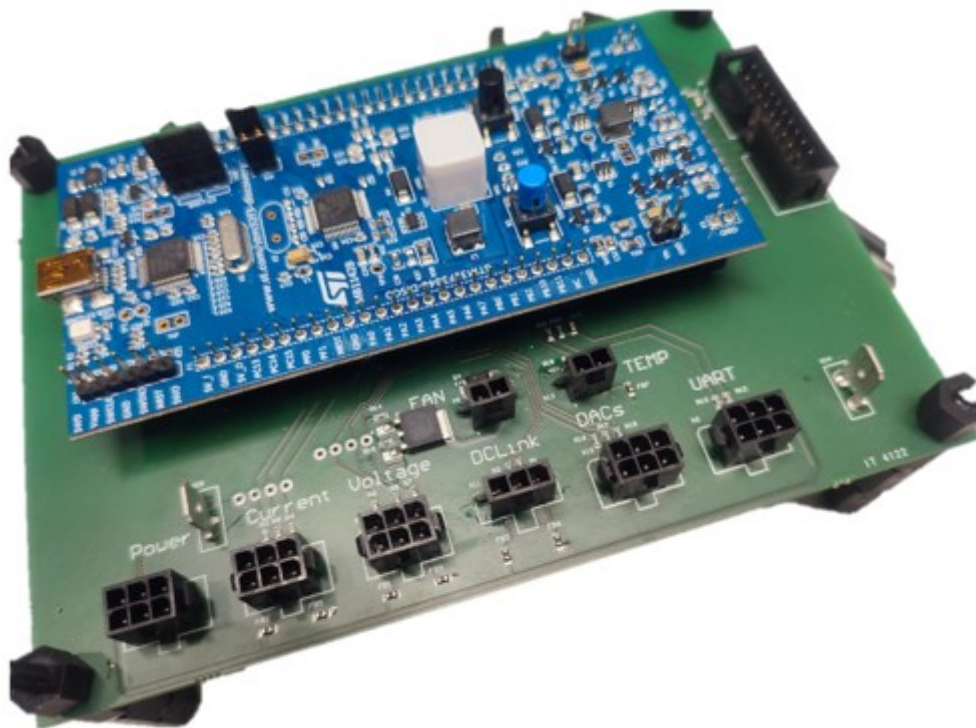


Figure 13. Cycle control card.

It also has a cycle time measurement feature for up to 26 000 cycles. Using that feature the cycle time variation can be analysed. The cycle control card measures the heat sink temperature and supplies power for fans to accordingly perform the desired thermal cycle. The maximum ambient temperature was considered to define the minimum temperature for the test, since the minimum temperature must be higher than the maximum ambient temperature with some margin. Otherwise, the cooling time would be very long, or the desired minimum temperature would be unattainable. The maximum ambient temperature was tested by driving a 9 kW thermal load in the test container. The outdoor maximum temperature was around 27 °C. The air conditioner in the test container was set to 20 °C. After 24 hours of testing, the indoor temperature was around 40 °C. Since the outdoor temperature will be considerably lower during the test and the maximum thermal load around 2 kW, 40 °C can be selected for the minimum swing temperature.

3.3 Thermal consideration

The heat sink is one thing that must be designed in this work. On dimensioning, three things must be considered. It must be small enough to achieve the desired maximum temperature, big enough to achieve the desired minimum temperature, and the cycle time must also be appropriate. The heat sink is made of an aluminium profile with a length of 10 cm, a fin gap 3.5 mm, and an original height 10 cm.

Heat dissipation calculations must be carried out to design the heat sink, so conduction and switching losses should be defined. Conduction losses can be defined by conduction state drain-source resistance ($R_{DS,on}$) and drain current. One way to measure $R_{DS,on}$ is to keep the channel constantly in a conduction state and drive known test current through the channel and then measure $V_{DS,on}$. When $V_{DS,on}$ is known, $R_{DS,on}$ can be solved using Ohm's law. $R_{DS,on}$ was measured for each MOSFET in the beginning and the average was 35.8 m Ω . For exact switching losses, a double pulse test should be performed. Due to the tight schedule, one was not organised. Instead, the switching losses were calculated based on manufacturer's datasheet values. Using the equations and values from the manufacturer's datasheet, losses can be calculated. According to previous investigations the power dissipation on the operation point will be around 42 W for one MOSFET. However, the device in the previous investigation was not the same; they were surface mount devices (SMD), but the chip was the same as in this test. Because of the different package-type, heat dissipation may vary. Since the chip was the same, this information can be used to evaluate loss calculations. Switching losses can be obtained by equation 2.5.

Since the conditions were specific in the datasheet, the correct values must be calculated using linear approximation. Linear approximation was also used to take into account different junction temperatures. First turn-on and turn-off energies on 25 °C junction temperature were defined on 600 V and 800 V. That way, values on 510 V at 25 °C junction temperature were able to be defined. Turn-on and turn-off energies at that condition were 221 μ J and 32 μ J, respectively. The variation on junction temperature was considered only on turn-on energy since the variation on turn-off energy was negligible. Equations 2.1 and 2.2 can be combined to have conduction losses. The current switching level waveform is square, so the following equation is the final form for the conduction losses.

$$P_{\text{cond}} = R_{\text{DS,on}} * I_{\text{D}}^2 * D, \quad (3.1)$$

where $R_{\text{DS,on}}$ is MOSFET On state drain-source resistance, I_{D} is the drain current, and D is duty cycle.

According to the datasheet, MOSFET's thermal resistance is 0.45 K/W. Insulator and thermal grease thermal resistances were 0.025 K/W and 0.05 K/W. Because the temperature difference from the heat sink surface to the junction varies as a function of losses, the junction temperature array endpoints were calculated using the following equation.

$$T_{\text{j}} = T_{\text{s}} + R_{\theta} * P_{\text{loss,@Tj}}, \quad (3.2)$$

where T_{s} is heat sink surface temperature, T_{j} is junction temperature, R_{θ} is thermal resistance, and $P_{\text{loss,@Tj}}$ is losses at junction temperature. The minimum and maximum were solved iteratively. The initial guess for junction temperature was the heat sink surface temperature, and the process was repeated until a difference was under 1 K.

Calculated losses for one MOSFET are now 36.4 W at 40 °C and 46.1 W at 90 °C. These values are pretty close to previously measured 42 W loss. Once losses are known, the heat sink size can be calculated. Equations are collected from Nerg (2019). In the calculations, some assumptions were made. In the heating period, only convection was considered and forced convection was taken into account during cooling period. The following equation was used to calculate convection heat flow.

$$q_{\text{convection}} = \alpha(2 * n * l * h)(T_{\text{s}} - T_{\text{ambient}}), \quad (3.3)$$

where α is the convection coefficient, n is the number of fins, l is the length of the fin, and h is the height of the fin. The convection coefficient can be obtained with equation:

$$\alpha = \frac{\lambda}{s}, \quad (3.4)$$

where s is the fin gap and λ is the thermal conductivity of air. Forced convection was also calculated using equation 3.4, but the convection coefficient was defined differently:

$$\alpha = \frac{Nu * \lambda}{l}, \quad (3.5)$$

where Nu is the Nusselt number and l is the length of the fin. Now flow type must be analysed, whether it is laminar or turbulent. Flow type must be known to have the correct equation for the Nusselt number. The Reynolds number (Re) describes the flow type and can be calculated:

$$Re = \frac{v * l}{\nu}, \quad (3.6)$$

where v is the air flow speed, l is the length of the fin, and ν is the kinematic viscosity of air. Since Reynolds number is below $5 * 10^5$ at every desired temperature, the flow is laminar and the Nusselt number is defined:

$$Nu = 0.664 * Re^{\frac{1}{2}} Pr^{\frac{1}{3}}, \quad (3.7)$$

where Pr is the Prandtl number.

When the losses and the heat dissipation are known, cycle times can be estimated with different heat sink sizes. The minimum fin number is 16, if it would be smaller some MOSFETs would not be in contact with the heat sink. Table 4 shows heating and cooling times based on the calculations and initial measurements of the actual test setup.

Table 4. Calculated and measured period times

Period	Time
Cooling (calculated)	2 min 26 sec
Cooling (measured)	2 min 10 sec
Heating (calculated)	5 min 49 sec
Heating (measured)	5 min 48 sec

The calculations were quite accurate, in the heating period the time difference is only one second. In the cooling period the time difference is 16 seconds. In the cooling period, forced convection was applied and its calculations are more complex compared to convection. The inaccuracy in the cooling period calculation may be caused by incorrect air flow speed. The air flow speed was only estimated based on the manufacturer's datasheet. It could have been measured for more accurate calculations. However, the accuracy of the calculated period times is good enough for this purpose. The calculations are shown in Appendix II and used air properties in Appendix III. In Figure 14 losses and convection are shown as a function of heat sink surface temperature.

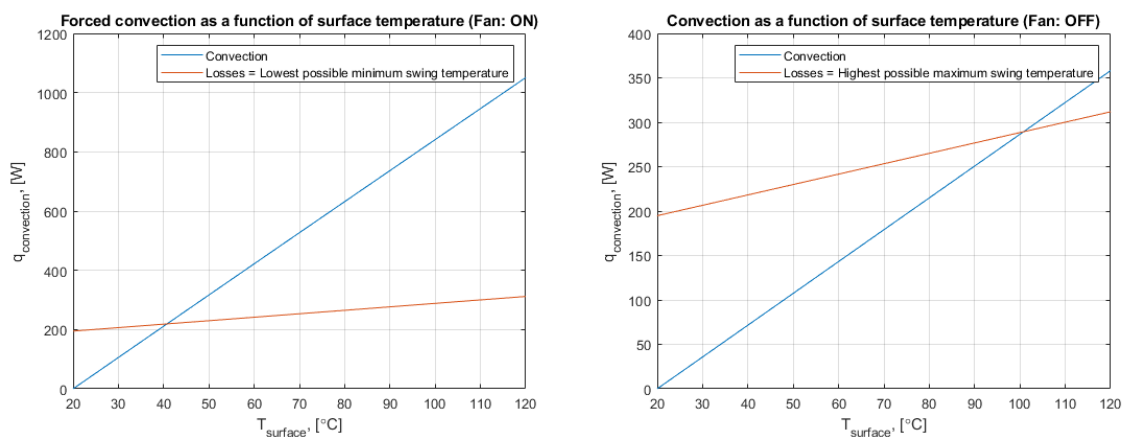


Figure 14. Losses and convection as a function of heat sink surface temperature.

The intersection points of losses and convection figures are the calculated highest and lowest possible swing temperatures.

3.4 Test software

This section will describe the cycling software used in the test setup. As mentioned in section 3.1, the test setup includes two control cards. A power control card is used to control the switches, and a cycle control card is used to control thermal cycling. Both control cards have STMicroelectronics processors, and the code was modified using STM32CubeIDE software.

The power control card creates PWM signals with a specific profile. Using this specific profile full switching and conduction losses can be roughly attained by low input current. The processor in the power control card was STM32G474. The cycle control card measures the heat sink temperature and switches the fans on and off according to the thermal cycle logic. The processor in the card was STM32F334.

3.5 Test strategy

As mentioned in the section 2.2, different cycling strategies exist. The strategy used in this work also contains switching losses, which will be missed if only DC current is driven through the specimen. Control signals are created complying with the test profile. To create PWM signals to the gate driver card, the process is following.

Table 5. Carrier and reference signal details

	Carrier signal	Reference signal
Maximum amplitude	0.5	1
Frequency	30 kHz	50 Hz
Offset	0.5	0
Phase	0°	0°
Maximum duty cycle	0.5	1

First, carrier signal (U_c) and reference signals (U_{ref}) are created. Table 5 shows the details of U_c and U_{ref} . The reference signal is used to create three different control signals with 120° phase difference. The carrier signal is multiplied by maximum PWM resolution. The

maximum PWM resolution can be solved by the following equation. The maximum PWM resolution describes steps for 100 % pulse width.

$$PWM_{\max,\text{resolution}} = \frac{f_{\text{processor}}}{f_{\text{sw}}} / 2, \quad (3.8)$$

where $f_{\text{processor}}$ is the processor clock frequency and f_{sw} is the switching frequency. The following equation defines the value of PWM signal:

$$PWM_{\max,\text{resolution}} * U_c < U_{\text{ref}} + \frac{PWM_{\max,\text{resolution}}}{2}, \quad (3.9)$$

The value of the PWM output signal is one if equation 3.9 is true. If equation 3.9 is false, PWM signal for the certain phase equals to zero. The previous tests have shown that using similar phase current on the real product, the heat sink temperature was 43 °C. In the real product fans are constantly blowing, so it is comparable to the lowest possible swing temperature shown in Figure 14 (left). In the calculations, the lowest possible swing temperature was around 40 °C. In the initial tests with test setup, 38 °C was the lowest possible temperature. In the initial tests, the ambient temperature may have been different, which could explain the difference between calculated and tested minimum temperatures. Of course, there are many variables which effect the lowest possible temperature such as the ambient temperature and the velocity of the air flow.

4 Improvements

As mentioned in the research framing, the analysis consists of test setup and condition improvements. Improvements in this chapter are further research suggestions and will not be realised in this thesis.

4.1 Hardware improvements

The main issue with the hardware was the unrobust gate power source. The issue was related to a mistake in the PCB layout. The weak points were vias, causing more loop inductance. That loop caused too high voltage spikes for the serial Schottky diode breaking it. The vias are circled by red in Figure 15.

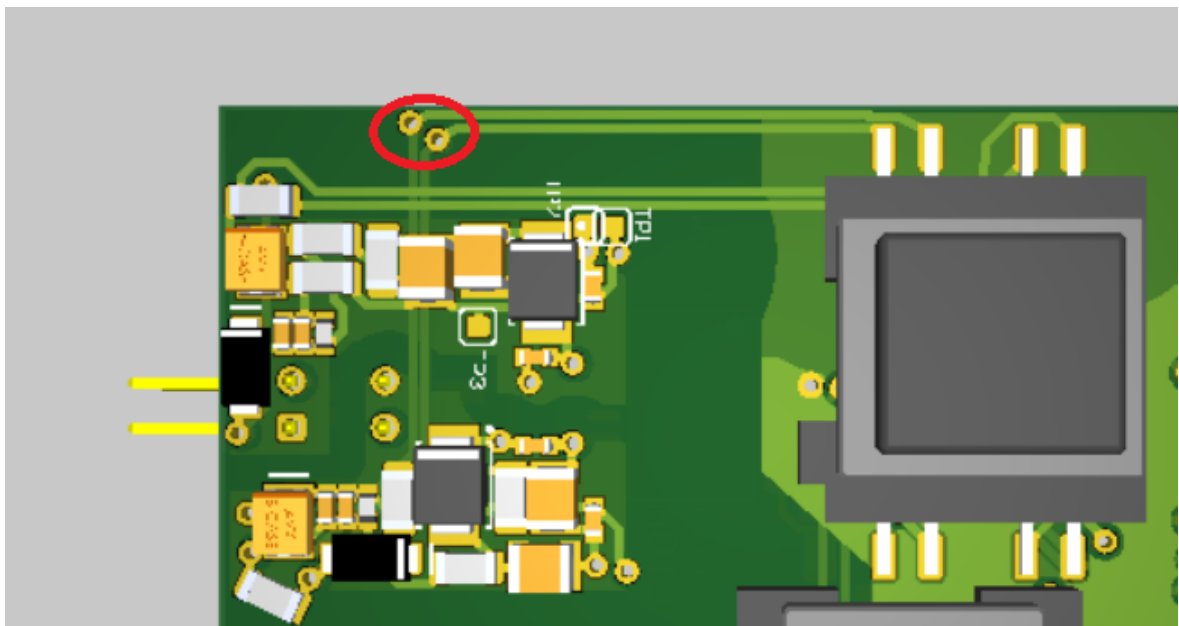


Figure 15. Gate driver secondary.

In the revised PCB, the signal will be rectified right after gate transformer. In the temporary solution, the maximum allowed voltage was increased by adding another Schottky in series.

The temporary solution was viable, and the setup started to perform as designed. The defect point test will be done in future investigations to see if earlier rectification helps.

During the debug process, it was noticed that more indicators and measuring points could be added to the PCB since this setup will be only used for test purposes. Adding indicators would make debugging much quicker if all the signals could be checked without measuring. For example, drive enable, PWMs, and gate voltage power are important signals, so they would need indicators. Also, V_{GS} was relatively difficult to measure without soldering wires to pin headers, adding test points would make it much easier and it would reduce the risk of short circuit.

A circuit to measure the conduction state drain source resistance ($R_{DS,on}$) would be a good addition to the revised setup. In the current setup, almost everything must be disassembled for the $R_{DS,on}$ measurement. $R_{DS,on}$ can be defined by measuring V_{DS} and I_D . So, these must be measured to calculate $R_{DS,on}$. The current measurement possibility already exists in the platform card. The current is measured using shunt resistors, the terminals to measure voltage over the shunt resistors also exist in the platform card. Only V_{DS} measuring circuit must be added to enable this feature. In section 2.4 three different DVCCs were introduced. The proposed DVCC was the most accurate and predictable, so it will also be proposed to be added to the improved test setup.

4.2 Test improvements

The test software did have a cycle time registration feature. However, cycle times will not be analysed in this thesis, since unstable ambient temperature distorted cycle times. Constant ambient temperature plays a crucial role if cycle times are analysed. The test setup was in an outdoor office container with a heat pump, but it looks like outdoor temperature still had a great effect on test setup ambient temperature. The future tests would be suggested to perform in the dedicated constant temperature container or at least in indoor conditions with more stable temperatures. That way, cycle times over the test period are comparable. Also, the test setup would have the measuring and logging for ambient temperature. That way the variation of ambient temperature could be checked and analysed after the endurance test.

Cycle time could be shorter to have a more aggressive and quicker test. One solution would be shutting down the control signal during the cooling period. That way, the heat sink can be designed to be smaller. Some initial tests can be done to verify this assumption by switching off the power supply manually during the cooling period. Then, the test strategy would be like modified power cycling. To achieve the power shutting feature, the power control card should measure the heat sink temperature, which can be done easily since the card already has terminals to the NTC resistor for temperature monitoring. Figure 16 shows improved and simplified version of the test setup in block diagram form. Adding pins for fan control to the platform or power control card is the minimum requirement for hardware modifications to achieve this more straightforward test setup. The feedback from the load is V_{DS} and I_D measurement signals for the device health monitoring.

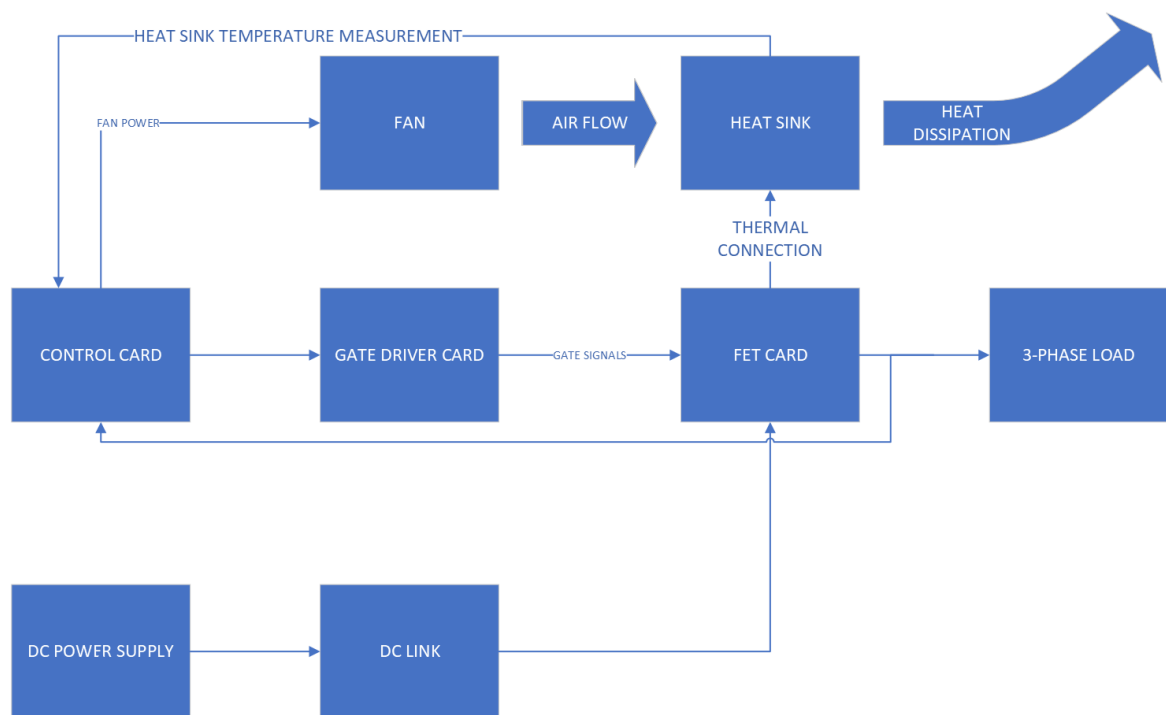


Figure 16. Block diagram of improved test setup.

At this point, only the AFE side can be used for thermal cycling in this control strategy. As mentioned in the framing, a test profile for DC-DC side will be suggested in this thesis. The test profile on the DC-DC side must be different than on the AFE side. On the AFE side, the load was a three-phase load, so it was used as a three-phase inverter but in the DC-DC side

the load will be single-phase. This thesis will investigate the test profile for the DC-DC side as a single-phase inverter. The load type will be a resistor and choke inductor. The schematic for the DC-DC side is shown in Figure 17.

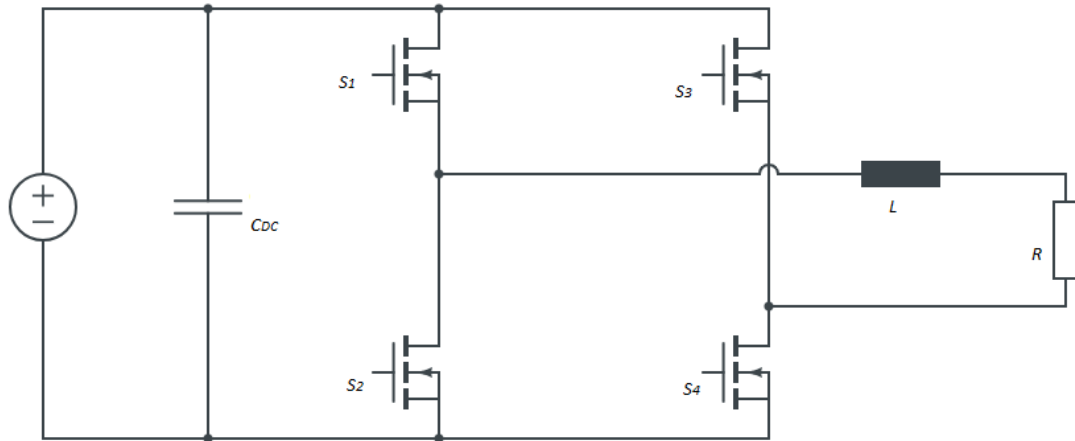


Figure 17. Schematic for DC-DC side.

For control signal developing, two sets of waveforms must be created. The first will be used as a carrier signal and the other one as a reference signal. The details of both signals are shown in Table 5. The control signal will be a PWM signal, and it will be on during the reference signal value is higher than the carrier signal value. Switches S_1 and S_4 will be controlled by identical signals. Switches S_2 and S_3 will also be controlled by identical signals which are just opposite to the first pair. In the simulation the relation between power supply current and load current was similar as it was in case of AFE side. Switching and conduction losses are a bit higher than in AFE, as they should be.

In the simulations, the values of load resistor and choke inductor were $200\text{ m}\Omega$ and $200\text{ }\mu\text{H}$, respectively. The load affects the semiconductor losses, so it is a crucial part of the test setup. The final values of the load resistor and choke inductor will not be defined in this thesis.

5 Conclusions

This thesis aimed to define a reliable method for a quicker endurance test process. However, due to hardware issues the scope was re-evaluated. The new scope was to carry out the cycling profile for the DC-DC side, design schematic for drain-source voltage online measuring, and calculations for losses, cooling, and cycle times. Common failure mechanisms, standard endurance tests, loss calculations, and device health monitoring were studied in the theory chapter. The re-evaluated scope's primary outcomes were completed with good results.

The test setup included a test profile only for the AFE side tests. A test profile for the DC-DC side was one of the primary outcomes in the research problems. The DC-DC test profile was introduced in the test improvements section. The test profile was tested in the simulation and the results were promising.

The schematic level design for the drain source voltage online measurement was also one of the primary outcomes in the research problems. DVCCs were studied in the device health monitoring section. Based on the literature review one design was suggested in the improvement chapter. Also, initial simulations were performed and the results of the proposed DVCC was promising.

The last primary outcome of this thesis was to carry out calculations for MOSFET's switching and conduction losses, heat sink dimensioning, and cycle times. The loss calculations were first studied in the theory chapter and in the thermal consideration losses were calculated. The heat sink fin number was minimised, since calculations show that the cycle time was appropriate.

The calculated period times were quite close to the measured real setup period times. Table 4 presents the calculated and measured times for cooling and heating periods. The time difference between calculated and measured heating period was one second. In the cooling period the difference was 16 seconds. This accuracy was more than enough for this work. The greater difference in the cooling period may be caused by inaccurate air flow speed. It can be said that the losses and the heat dissipation were successfully calculated since the differences in the cycle times were so small.

6 Future work

The things that must be done next are implementing the DVCC to the improved setup, DC-DC test profile tests and verifying the assumptions for the modified power cycling by calculations and measurements of the real system.

The DVCC components must be dimensioned properly, and then the PCB layout can be designed. Also, the software needs to be modified for this purpose. The DC-DC profile tests' only required hardware modification is changing the load. Also, the load values must be defined. The control code must be added, and then initial tests can be performed.

The unstable ambient temperature issue was also mentioned earlier. The next tests could be performed in a constant temperature area. That way the cycle time measuring could be tested. Of course, some other factors may also have effect on the cycle time, but they cannot be studied with unstable ambient temperature.

In the improvements chapter, modified power cycling was also suggested. The initial tests with modified power cycling could be performed easily by shutting down power manually for the cooling period. Before tests, the heat sink calculations must be done again. Based on the calculations, heat sink will be re-dimensioned.

After initial tests on the improved setup, the real tests can be performed, and test results analysed. This was the idea in the beginning of this thesis. Based on the test results a standard test procedure for the company can be constructed.

After implementing improvements, more data of the setup can be acquired. Based on the data, a more accurate component selection can be performed. Also, the product lifetime can be predicted better. The device health monitoring can be put into practice in the product by measuring $V_{DS,on}$ online. The device health monitoring system can collect valuable data of the product, and expensive failures could be avoided.

References

Engineers Edge. 2023. Viscosity of Air, Dynamic and Kinematic. Retrieved [Aug 27, 2023] Available:

https://www.engineersedge.com/physics/viscosity_of_air_dynamic_and_kinematic_14483.htm.

Gelagaev R., Jacqmaer P. and Driesen J. 2015. A Fast Voltage Clamp Circuit for the Accurate Measurement of the Dynamic ON-Resistance of Power Transistors. IEEE Transactions on Industrial Electronics 62(2): 1241-1250.

IEC. 2010. Semiconductor devices - Mechanical and climatic test methods - Part 34: Power cycling, International standard IEC 60749-34:2010, International Electrotechnical Commission.

IEC. 2003. Semiconductor devices - Mechanical and climatic test methods - Part 25: Temperature cycling IEC 60749-25:2003.

Infineon. 2020. How Infineon Controls and Assures the Reliability of SiC Based Power Semiconductors. Retrieved [May 5, 2023] Available at: https://www.infineon.com/dgdl/Infineon-Reliability_of_SiC_power_semiconductors-Whitepaper-v01_02-EN.pdf?fileId=5546d46272e49d2a01735723745d3f14&da=t.

Infineon. 2002. How to Select the Right CoolMOSTM and its Power Handling Capability. Retrieved [Oct 23, 2023] Available at: https://www.infineon.com/dgdl/Infineon-ApplicationNote_MOSFET_CoolMOS_How_to_select_the_right_CoolMOS-AN-v01_00-EN.pdf?fileId=db3a304412b407950112b40acf580693.

Kim J., Kwak S. and Choi S. 2022. Impacts of SiC-MOSFET Gate Oxide Degradation on Three-Phase Voltage and Current Source Inverters. Machines 10(12): 1194.

Nerg J. 2019. Terminen Laitesuunnittelu -Luennot.

NIST/SEMATECH. 2012. E-Handbook of Statistical Methods. Retrieved [Nov 7, 2023] Available: <http://www.itl.nist.gov/div898/handbook/>

Ortiz Gonzalez JA. and Alatisse O. 2019. A Novel Non-Intrusive Technique for BTI Characterization in SiC mosfets. IEEE Transactions on Power Electronics 34(6): 5737.

Pu S., Yang F., Vankayalapati BT. and Akin B. 2022. Aging Mechanisms and Accelerated Lifetime Tests for SiC MOSFETs: An Overview. IEEE Journal of Emerging and Selected Topics in Power Electronics 10(1): 1232-1254.

Rode S., Weis R., Schwingal N. and Bernet S. 2021. Thermal Design Comparison of various Natural Convection Cooling Concepts of Discrete SiC-MOSFETs. 2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe) P.1-P.9.

Karki U. and Peng F. Z. 2018. Precursors of Gate-Oxide Degradation in Silicon Carbide MOSFETs. - 2018 IEEE Energy Conversion Congress and Exposition (ECCE) 857-861.

Yu B., Wang L. and Ahmed D. 2020. Drain-Source Voltage Clamp Circuit for Online Accurate ON-State Resistance Measurement of SiC MOSFETs in DC Solid-State Power Controller. IEEE Journal of Emerging and Selected Topics in Power Electronics 8(1): 331-342.

Appendices

Appendix I: Picture of the test setup



Appendix II: MATLAB code to estimate cycle times

```

clc
close all

I_D = 38;
R_DSon_25 = 35.8e-3;
D = 0.5;
Eon600 = 300e-6;
Eoff600 = 50e-6;
Eon800 = 475e-6;
Eoff800 = 90e-6;

%Slope for Eon and Eoff voltage dependency
kon = (Eon800 - Eon600) ./ (800-600);
koff = (Eoff800 - Eoff600) ./ (800-600);

%Eon and Eoff at 510 V
Eon510 = Eon600 + kon .* (510 - 600);
Eoff510 = Eoff600 + koff .* (510 - 600);

%Slope for R_DSon
kR_DSon = (1.24.*R_DSon_25 - R_DSon_25.*0.95) ./ (100 - 25);
%R_DSon as a function junction temperature
R_DSont = @(T_j) R_DSon_25 + kR_DSon .* (T_j - 25);

%Slope for Eon temperature dependency
kont = (975e-6 - 500e-6) ./ (175 - 25);

%Eon as a function of junction temperature
Eont510 = @(T_j) Eon510 + kont .* (T_j - 25);

%Losses as a function of junction temperature
Pswitching = @(T_j) (Eoff510 + Eont510(T_j)) .* 30e3;
Pconduction = @(T_j) R_DSont(T_j) .* (I_D).^2 .* 0.5;
losses = @(T_j) (Pconduction(T_j) + Pswitching(T_j)).*6;

dt = 50;

%Heat sink dimensions
%n = 30 %original fin number
n = 16; %Fin number
L = 11.5e-2; %Fin length
H = 10e-2; %Fin height
cp_al = 900;
m = 1.49 * (16/30); %Heat sink mass

T_s = 20:10:120; %Heat sink surface temperatures
R_th = 0.05 + 0.025 + 0.45;
t1 = 20 + R_th .* 38.9885;
t2 = 120 + R_th .* 57.8889;
T_j = linspace(t1, t2, 11); %Junction temperatures
T_amb = 20; %Ambient temperature
T_f = (T_s + T_amb) ./ 2; %Film temperature
s = 3.5e-3; %cap length
lambda = 0.026;

```

```

alpha = 1.31 .* (lambda ./ s);

q_conv = @(T_s) alpha .* (2 .* n .* L .* H) .* (T_s - T_amb);

figure(1)
plot(T_s, q_conv(T_s))
grid on
ylabel 'q_{convection}, [W]'
xlabel 'T_{surface}, [C]'
title 'Convection as a function of surface temperature (Fan: OFF)'
hold on
plot(T_s, losses(T_s))
legend('Convection', 'Losses = Highest possible maximum swing temperature')
q_mean = mean(q_conv(T_s));
convection_max = max(q_conv(T_s));

heating = mean(losses(T_j) - q_conv(T_s));
time_perK = (m .* cp_al) ./ heating; %dT/dt
heating_time = time_perK .* dt;
heating_time_min = heating_time/60

A = H .* L;
volumeflow = 4.4; %m3/min
q_v = volumeflow / 60; %m3/s
V = q_v ./ A;

Pr = [0.7309 0.7296 0.7282 0.7268 0.7255 0.7241...
0.7228 (0.7228+0.7202)/2 0.7202 (0.7177+0.7202)/2 0.7177];
kinematic_viscosity = [1.516 1.562 1.608 1.655 1.702 1.750 1.798...
(1.798+1.896)/2 1.896 (1.995+1.896)/2 1.995] .* 10^-5;
thermal_conductivity = [0.02514 0.02551 0.02588 0.02625 0.02662 0.02699...
0.02735 (0.02735+0.02808)/2 0.02808 (0.02808+0.02881)/2 0.02881];
Re = V .* L ./ kinematic_viscosity; % under 5e5 -> laminar flow
Nu = 0.664 .* (Re.^ 0.5) .* Pr.^(1/3);
h = Nu .* thermal_conductivity/L;
q_forced = @(T_s) h .* (2 .* n .* L .* H) .* (T_s - T_amb);

figure(2)
plot(T_s, q_forced(T_s));
grid on
ylabel 'q_{convection}, [W]'
xlabel 'T_{surface}, [C]'
title 'Forced convection as a function of surface temperature (Fan: ON)'
hold on
plot(T_s, losses(T_s))
legend('Convection', 'Losses = Lowest possible minimum swing temperature')
cooling = mean(q_forced(T_s) - losses(T_j));
time_perK = (m .* cp_al) ./ cooling;
cooling_time = time_perK .* dt;
cooling_time_min = cooling_time/60
cycle_time = heating_time_min + cooling_time_min

```

Appendix III. Air properties as a function of temperature (Engineers Edge, 2023)

Film temperature, [°C]	Pr	Kinematic viscosity, [m ² /s]	Thermal conductivity, [W/mK]
20	0.7309	1.52E-05	0.02514
25	0.7296	1.56E-05	0.02551
30	0.7282	1.61E-05	0.02588
35	0.7268	1.66E-05	0.02625
40	0.7255	1.70E-05	0.02662
45	0.7241	1.75E-05	0.02699
50	0.7228	1.80E-05	0.02735
55	0.7215	1.85E-05	0.027715
60	0.7202	1.90E-05	0.02808
65	0.7190	1.95E-05	0.028445
70	0.7177	2.00E-05	0.02881