Lappeenranta
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Vesa Väisänen

PERFORMANCE AND SCALABILITY OF ISOLATED DC-DC CONVERTER TOPOLOGIES IN LOW VOLTAGE, HIGH CURRENT APPLICATIONS

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Abstract

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Fuel cells are a promising alternative for clean and efficient energy production. A fuel cell is probably the most demanding of all distributed generation power sources. It resembles a solar cell in many ways, but sets strict limits to current ripple, common mode voltages and load variations. The typically low output voltage from the fuel cell stack needs to be boosted to a higher voltage level for grid interfacing. Due to the high electrical efficiency of the fuel cell, there is a need for high efficiency power converters, and in the case of low voltage, high current and galvanic isolation, the implementation of such converters is not a trivial task.

This thesis presents galvanically isolated DC-DC converter topologies that have favorable characteristics for fuel cell usage and reviews the topologies from the viewpoint of electrical efficiency and cost efficiency. The focus is on evaluating the design issues when considering a single converter module having large current stresses.

The dominating loss mechanism in low voltage, high current applications is conduction losses. In the case of MOSFETs, the conduction losses can be efficiently reduced by paralleling, but in the case of diodes, the effectiveness of paralleling depends strongly on the semiconductor material, diode parameters and output configuration. The transformer winding losses can be a major source of losses if the windings are not optimized according to the topology and the operating conditions. Transformer prototyping can be expensive and time consuming, and thus it is preferable to utilize various calculation methods during the design process in order to evaluate the performance of the transformer. This thesis reviews calculation methods for solid wire, litz wire and copper foil winding losses, and in order to evaluate the applicability of the methods, the calculations are compared against measurements and FEM simulations. By selecting a proper calculation method for each winding type, the winding losses can be predicted quite accurately before actually constructing the transformer. The transformer leakage inductance, the amount of which can also be calculated with reasonable accuracy, has a significant impact on the semiconductor switching losses. Therefore, the leakage inductance effects should also be taken into account when considering the overall efficiency of the converter.

It is demonstrated in this thesis that although there are some distinctive differences in the loss distributions between the converter topologies, the differences in the overall efficiency can remain within a range of a few percentage points. However, the optimization effort required in order to achieve the high efficiencies is quite different in each topology. In the presence of

practical constraints such as manufacturing complexity or cost, the question of topology selection can become crucial.

Keywords: converter topologies, power conversion, semiconductors, magnetic components

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Lappeenranta, December 18th, 2012

Vesa Väisänen

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Nomenclature

In the present work, variables and constants are denoted in *italics*, vectors are denoted using **bold regular type**, and abbreviations are denoted using regular type.

Latin alphabet

A	area
A	multiplier in Equations (5.36) and (5.43)
B	flux density
B	multiplier in Equations (5.36) and (5.43)
C	capacitance
C	multiplier in Equations (5.36) and (5.43)
d	diameter
D	duty cycle
E	emissivity
E	energy
E	inductor core tongue width
f	frequency
F	fringing flux factor
g	transconductance
G	winding width
H	electric field
h	height
I	RMS current
J	current density
j	harmonic number
K	winding fill factor
K	constant depending on the inductor winding placement
k	waveform coefficient
L	inductance
l	length
M	total number of stacked transformer winding layers in a portion
m	MMF ratio in a winding layer
m	mass
n	transformer turns ratio
N	number of turns in a winding
p	litz packing factor
p	number of primary-secondary intersections
P	number of primary-secondary intersections
r	ripple
R	resistance
t	distance between adjacent conductors
t	time
T	period, time
T	temperature
V	RMS voltage

W	window
X	divider for the frequency in Equations (5.53) and (5.54)
X	multiplier depending on the litz wire insulation build

Greek alphabet

μ	permeability
γ	ratio of the single litz strand diameter to the diagonal of a square having a side length of one skin depth
δ	skin depth
η	porosity factor
θ	subscript in thermal resistivity
Λ	magnetic amplifier blocking time in volt-seconds
ρ	resistivity
Φ	magnetic flux
φ	relation factor between the conductor height and skin depth

Subscripts

0	vacuum
AC	alternative current
amb	ambient
avg	average
c	core
cld	core loss density
conv	convective
corr	corrected
Cr	resonance capacitor
cs	common-source
DC	direct current
d	delay
ds	drain-source
eff	effective
ext	external
g	gap
G	gate
gs	gate-source
init	initial
int	internal
leak	leakage
lk	leakage
max	maximum
opt	optimal
oss	MOSFET output capacitance
out	output
pk	peak
pri	primary
r	relative

r	reverse
rad	radiative
ref	reference
rm	datasheet test setup limited diode peak recovery current
rm(rec)	diode limited peak recovery current
rr	reverse recovery
sec	secondary
spec	specification
s	strand
th	threshold
tot	total
tr	transformer
vert	vertical
w	winding

Abbreviations

AC	alternative current
AWG	American wire gauge
DB	diode bridge
DC	direct current
ESL	equivalent series inductance
ESR	equivalent series resistance
FB	full-bridge
FEM	finite element method
Hz	Herz
kVA	kilovolt-ampere
LC	electrical circuit consisting of an inductive and capacitive component
LCR	electrical circuit consisting of an inductive, capacitive and resistive component
LITZ	Litzendraht, German for braided/stranded or woven wire
MATLAB	matrix laboratory
MLT	mean length of turn
MMF	magnetomotive force
MOSFET	metal oxide field effect transistor
PSFB	phase-shift full-bridge
PSFBVD	phase-shift full-bridge with a voltage doubler secondary
PWM	pulse-width modulation
RPP	resonant push-pull
SA	core surface area
SOFC	solid oxide fuel cell
TX	transformer
VD	voltage doubler
ZCS	zero current switching
ZVS	zero voltage switching

1 Introduction

This work was conducted under the SofcPower project, which was coordinated by the VTT Technical Research Centre of Finland. The main domestic contributors to the project along with VTT were companies and the universities of technology in Espoo, Lappeenranta and Tampere. The primary goal of the SofcPower was the demonstration and commercialization of SOFC systems. The project also aimed to support companies having emerging business in the field of SOFC systems, balance of plant components or fuel supply. Also the potential end users of the fuel cell systems gain benefits from the research conducted under the SofcPower project.

One task in the SofcPower project was to develop a suitable power conversion unit for a 10 kW SOFC stack. The goal of the work was to identify the requirements for power electronics in a solid oxide fuel cell application, where low DC voltage supplied by a fuel cell stack needed to be boosted to a suitable level for a three phase grid inverter (Riipinen et al., 2008). In this thesis, the isolated DC-DC converter topologies capable of meeting the stringent fuel cell requirements are analyzed in terms of electrical and cost efficiency as well as scalability. The high power prototype tests were conducted in co-operation with the VTT Technical Research Centre of Finland. At the time of writing, the resonant push-pull converter selected for the power conversion unit has been operating over 2500 hours with a high reliability.

1.1 Solid oxide fuel cells as a renewable power source

The political interests for pushing forward the development of renewable energy sources have generated a great deal of new research and innovations in the field of fuel cells and solar cells during the past decades. Among other fuel cell types the solid oxide fuel cells represent a nascent technology that could be used for clean and efficient stationary energy production. A single SOFC cell consists of a porous anode, a cathode and of a solid metal oxide electrolyte between them (Figure 1.1).

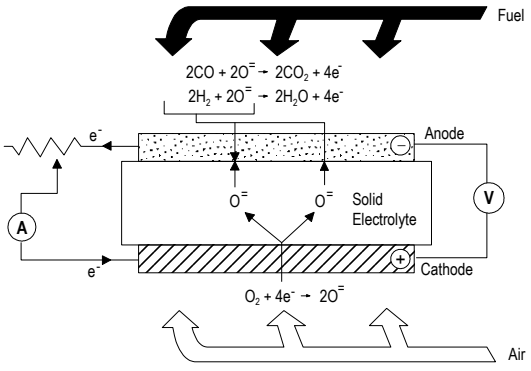


Figure 1.1: The simplified operation of a SOFC, reproduced from Brown (1998).

The fuel, which can be pure hydrogen or hydrocarbon based, is fed to the anode and air is fed to the cathode. Oxygen molecules enter the cathode/electrolyte interface and extract electrons from the cathode. The resulting oxygen ions react with the fuel at the anode-electrolyte boundary, which produces electric current and depending on the fuel also reaction by-products such as pure water, carbon dioxide and heat. The ideal standard potential, or H_2 oxidation potential, is

1.229 V. This ideal single cell voltage is reached when pure hydrogen and oxygen reacts at normal temperature and pressure. The total fuel cell stack voltage depends on how many single fuel cells are connected together and what the final reaction voltage is for each cell (Brown, 1998; Handbook, 2004).

The actual output voltage of the fuel cell varies from the ideal voltage due to three distinctive types of losses and operational areas, which can be seen in Figure 1.2 (Handbook, 2004; Riipinen et al., 2008). The normal operation area for a fuel cell is the region of ohmic losses.

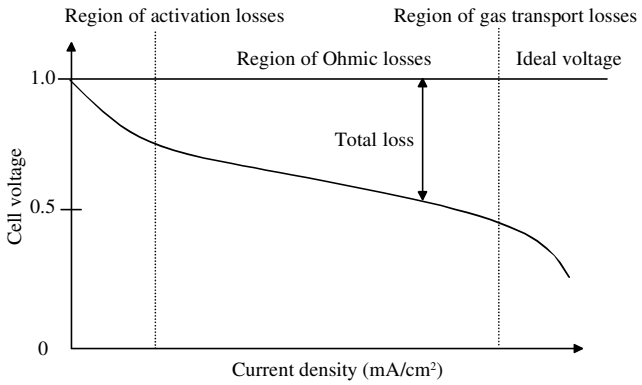


Figure 1.2: Actual fuel cell output characteristics compared to the ideal voltage output.

The activation losses are related to the activation energy of the electrochemical reactions at the electrodes and the amount of these losses depends mainly on the type of chemical reactions, cell materials and reactant utilization. The activation losses are often less significant in high temperature fuel cells such as SOFC. Therefore, the first knee point is not very easily distinguished (Handbook, 2004).

The ohmic losses are caused by ionic resistance in the electrolyte and electrodes, electronics resistance in the electrodes and all of the internal and external cabling including the contact resistances. The ohmic losses are mainly dependent on the current, conductor structure and materials, stack geometry and temperature. The resistivity of typical metal conductors increases together with the temperature, but in electronically and ionically conductive ceramics the resistivity decreases exponentially. The net effect of a temperature rise in high-temperature cells is a significant reduction in resistance, while in low-temperature cells the change in total resistance is small (Handbook, 2004).

The gas transport losses, or mass-transport related losses, result from the finite mass transport rate, which limits the supply of fresh reactants and the evacuation of reaction products. These losses are strongly dependent on the current density, reactant activity and electrode structure. In high temperature fuel cells the effect of gas transport losses is more significant and the second knee point in Figure 1.2 often extends further to the left (Handbook, 2004).

The achievable electrical efficiency of SOFC can range from 50% to 75% depending on the fuel and operating conditions (Demin and Panagiotis, 2001; Sidwell, 2005; Huayang and Kee, 2006). With combined heat and power production the total efficiency can be over 80% (Oates et al., 2002; Fontell et al., 2004). The output voltages of individual fuel cell stacks are usually below 100 V_{DC}, but higher stack voltages in the range of several hundred volts are also possible.

1.2 Need for DC-DC conversion in the field of renewable energy

What both fuel cells and solar cells have in common is that they produce unregulated DC voltage which in most cases needs to be boosted to a higher voltage level and regulated in order to interface a grid tie inverter. The grid interconnection with 400 V_{DC} requires inverter input voltages in the range of 410-1000 V_{DC} (Fontell et al., 2004; Sarén, 2005) depending on the inverter topology and modulation method. It is preferable to isolate the DC-source galvanically from the grid in order to break long ground loops and to meet the safety criteria in many applications. The galvanic isolation can be placed on the grid side or on the high frequency DC-converter. There is a substantial difference on the transformer size in these two cases. For example a commercial 50 Hz, 10 kVA one-phase transformer can weigh 72 kg, while a 50 kHz, 10 kVA transformer weighs approximately 2 kg.

The isolated DC-DC converters suitable for high power conversion can be divided into two main categories: voltage-fed converters and current-fed converters. The voltage-fed converters are buck derived topologies, while the current-fed ones apply the principle of the boost converter. Compared to voltage-fed converters the current-fed converters have inherently lower input current ripple due to an input inductor providing both voltage boosting and filtering. In addition, they have lower rectifier diode voltage stress resulting from reduced voltage ringing at the secondary and a smaller transformer turns ratio because of the boosting operating principle. The current-fed converter is also more tolerant for switching asymmetry induced DC offsets in the transformer magnetizing current; a quality which reduces the risk of transformer saturation and current overshoots (Väisänen et al., 2010).

1.3 The motivation for high power conversion efficiency

In order to benefit from the good electrical efficiency of the fuel cell, the total efficiency of the entire power plant including auxiliary systems and the power conversion unit should be high. Poor efficiency of the auxiliary systems will increase the operating costs in terms of lost energy and also investment costs if larger fuel cell stacks are needed in order to maintain a desired net power output. Halinen et al. (2011) have demonstrated a fuel cell system with net stack DC efficiency of 60% and power output of 9.8 kW, while the net AC efficiency was 43% and the AC power output 7.1 kW. The power loss in recycle and air blowers, stack current collection interfaces and cabling was 1.54 kW and DC-AC conversion losses were 1.1 kW. Thus the total auxiliary losses were over 27% of the total available stack power.

The impact of system efficiency on the total operating costs in terms of the lost net power output is increased together with the total power and feeding tariffs. Figure 1.3 illustrates the net cost of losses in a 100 kW system based on a feeding tariff of 83.5 €/MWh, which was accepted in 2011 as the renewable energy feeding tariff in Finland for a period of 12 years.

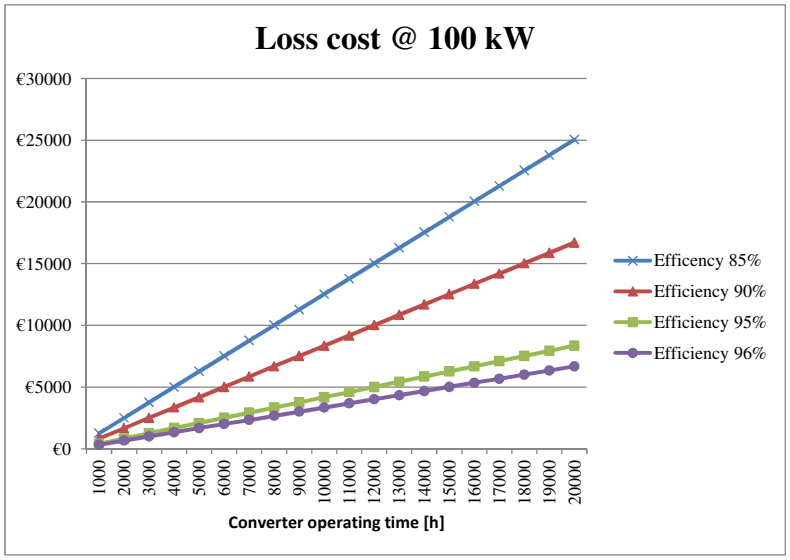


Figure 1.3: Cost of power losses in a 100 kW system based on a feeding tariff of 83.5 €/MWh.

Increasing the total efficiency from 85% to 95% would decrease the loss cost by 66.7% and increasing the efficiency from 95% to 96% would further reduce the cost by 20%.

1.4 Scope of the work

The scope of this work is to evaluate the performance and scalability of various DC-DC converter topologies in low voltage, high current applications. A low voltage is defined in this work to be in the range of 40-60 V, as in a SOFC stack described by Halinen et al. (2011). A high current is defined as 200 A and or higher. According to Ono et al. (2011) the typical output power of a residential SOFC cogeneration system in Japan has been in the range of 0.7-1 kW. If considering a small apartment with a yearly consumption of 2000 kWh, the average hourly consumption would be 228 W, which could be supplied with the 0.7 kW SOFC system. In a larger house with a yearly consumption of 20000 kWh the average hourly consumption would be 2.3 kW. If these consumptions are paralleled by the definitions medium and high power, respectively, a medium power system in this thesis would be in the range of 0.5-2 kW and a high power system from 2 kW upwards.

The physical phenomena behind the power losses are the same in every converter topology, but the differences in the loss distributions depend on the converter structure and operating principle. In this work these differences are introduced by analytical calculations and prototype measurements. The prototype measurements focus on current-fed converters, which are, at present, considered more suitable for applications requiring a large voltage step-up ratio due to reasons presented in the literature and also in this work. Past publications related to voltage-fed converters are usually based on step-down applications and do not consider the suitability to step-up applications. The simulations conducted in this work demonstrating the various converter phenomena are based on PSpice simulation models designed according to the general specifications in Table 1.1. The input and output specifications are based on the requirements set by the SOFC stack at the VTT Technical Research Centre of Finland.

The SOFC stack was operated so that the maximum output current was 200 A and the nominal stack voltage (with a non-degraded stack) was 50 V. During the stack test run, there was slight degradation in the stack voltage, and since the output current was kept at a maximum of 200 A, the stack output power decreased accordingly (Halinen et al., 2011). The 10 kW specification with 50 V and 200 A thus represents the practical worst case operating point for component dimensioning in this thesis.

The simulated figures in this thesis demonstrate the various switching phenomena in the topologies rather than compare the converter performances. However, attention is paid also to the modeling accuracy, as described in Appendix C.

Table 1.1. Operational parameters for the simulation models and calculations used in this work.

Nominal input voltage	50 V
Nominal input current	200 A
Nominal output voltage	660 V
Switching frequency	50 kHz
Input/output current ripple	Depends on the topology
Isolation transformer	Depends on the topology
Transistors	MOSFET, minimum available $R_{DS(on)}$ at minimum breakdown voltage of 1.2 x $V_{ds(max).}$
Diodes	Si or SiC, minimum breakdown voltage of 1.2 x $V_{out(max).}$

1.5 Outline of the thesis

Chapter 2 is a literature review of full-bridge-based galvanically isolated voltage-fed DC-DC converter topologies. Since the past publications have concentrated on step-down applications, the step-up characteristics have not been discussed. These characteristics and design trade-offs are evaluated and presented in this thesis.

Chapter 3 is a literature review of galvanically isolated current-fed converters. The topologies presented in the literature are reviewed from the viewpoint of a 10 kW low voltage, high current application. The design trade-offs related to the high current operation are presented and guidelines are given to increase the converter reliability under these conditions.

Chapter 4 presents the factors affecting the semiconductor device conduction and switching losses in the topologies compared. The advantages of semiconductor paralleling are also discussed in terms of efficiency and cost. Since some of the topologies employ a voltage doubler secondary instead of a diode bridge, a generalized loss comparison between these two output configurations is presented.

Chapter 5 presents the design trade-offs related to the design of inductors and transformers when considering a low voltage, high current step-up application. The calculation methods are presented and verified against measurements and FEM simulations. The advantages and

disadvantages of the litz wire are discussed and general guidelines are given by which to evaluate a suitable litz wire configuration for certain operating conditions.

Chapter 6 presents an overall efficiency and cost evaluation for the topologies compared when operating under the constraints presented in this thesis. The characteristics with the greatest impact on efficiency in each topology are summarized in this chapter. The chapter also presents suggestions for future work.

1.6 Scientific contributions

The main scientific contributions of this doctoral dissertation are the following:

- Presentation of a high efficiency, high power single unit DC-DC converter for low voltage applications (Väisänen et al., 2011).
- Presentation of the advantages provided by a voltage doubler secondary, such as a high voltage conversion ratio and tolerance for switching asymmetries (Väisänen et al., 2010). Also the disadvantages of a voltage-doubler secondary such as increased component stress and losses are discussed.
- Presentation of limiting factors for semiconductor component scaling in most common isolated topologies.
- Presentation of limiting factors for magnetic component scaling and litz wire applicability in the most common isolated topologies.
- Evaluation of the suitability of voltage-fed full-bridge topologies to high current step-up applications.

2 Isolated voltage-fed topologies for medium to high power applications

The field of voltage-fed converters is very wide and there is a considerable amount of publications each addressing various detailed problems, some of which may not even have significant practical value. This chapter focuses on the main design issues related to voltage-fed topologies and most of the cited publications include prototype measurements preferably with an input power of 1 kW or higher. The analysis on the scalability of the proposed topologies, especially the more complex ones, is often neglected, even though it would be crucial to evaluate converter performance with power levels higher than a few hundred watts. The low power applications often include consumer products, where extreme simplicity and low cost weigh more than ultimate efficiency.

Voltage-fed converters presented in this thesis operate with duty cycles below 50% (there is no switch overlapping in the switching leg) and the primary input energy storage component is a capacitor. The maximum voltage available at the transformer primary equals the input voltage.

2.1 Conventional full-bridge converter with hard switching

The basic full-bridge converter, in which the most commonly used output configurations are either a diode bridge, center-tapped transformer with two diodes or voltage doubler, is presented in Figure 2.1. In the hard switching method, transistors S_1 and S_2 are switched simultaneously as a pair, as are transistors S_3 and S_4. There is a small dead time between the conduction of the transistor pairs, meaning that all of the switches are off for a while. There is no utilization of the leakage inductance to achieve zero voltage switching, and thus the switching losses are increased at higher input voltages.

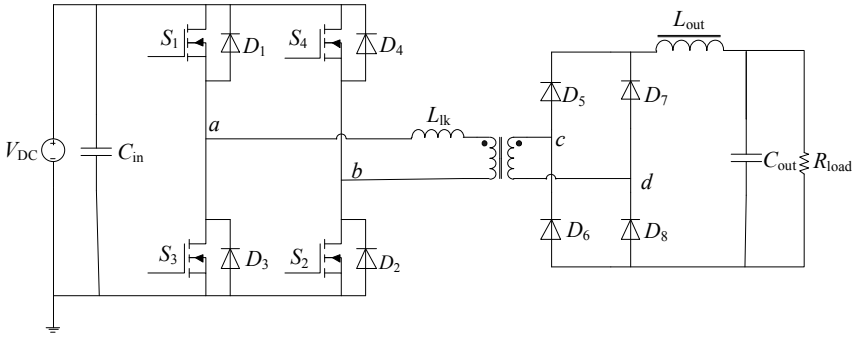


Figure 2.1: Basic voltage-fed full-bridge converter with a diode bridge output.

2.1.1 Dead time requirement and input current ripple

Due to the operating principle, there has to be a small dead time between the transistors in the same switching leg in order to avoid a short circuit. There is no external inductor to limit the current rate of rise, and consequently even a very short duration short circuit could destroy the transistors.

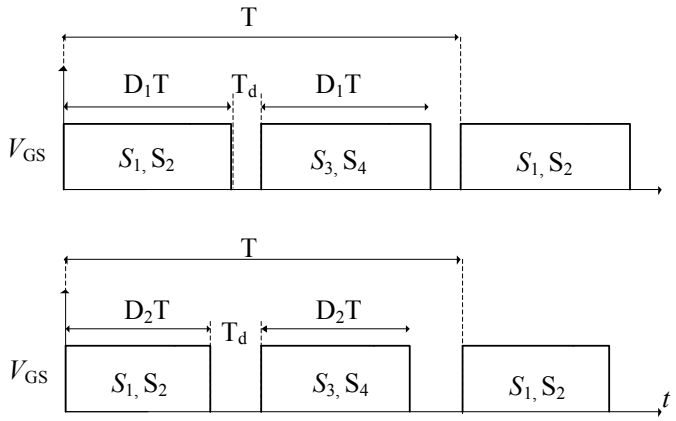


Figure 2.2: Gate drive principle of the hard switched voltage-fed full-bridge converter.

Figure 2.2 demonstrates that reducing the duty cycle increases the dead time. If the dead time was kept the same, the duty cycle D_2 would be much higher than D_1. This would cause a large transformer volt-second imbalance and most likely saturation. During the dead time the input current flows to charge the input capacitor and while the capacitor is charging the current declines towards zero. The impedance of the input source determines how fast the capacitor is charged and how much the input current can change during the dead time. An example of input current ripple caused by the dead time can be seen in Figure 2.3. There is a 230 µF capacitor and 100 nH parasitic inductance at the input, while the input power is 10 kW (50 V @ 200 A).

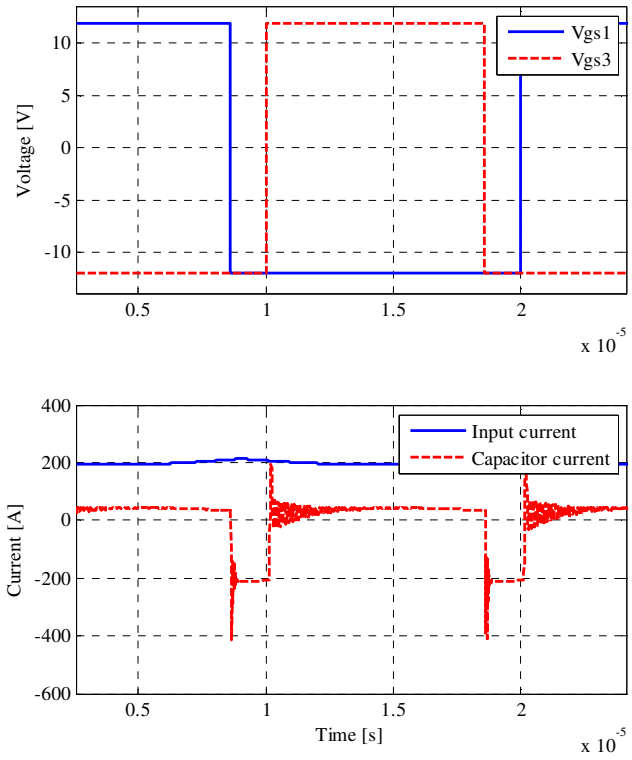


Figure 2.3: Simulated input current ripple during the dead time period with switching frequency of 50 kHz and duty cycle of 43%.

The peak-to-peak input current ripple in this case is 9% of the nominal current, while the input capacitor ripple is over 100%. To limit the input current ripple in this voltage-fed topology, the input LC circuit resonant frequency must be low enough (large inductance and/or capacitance) or the switching frequency must be high to keep the dead time period short enough.

2.1.2 Voltage overshoot and ringing at secondary rectifier

The secondary rectifiers suffer from leakage inductance related voltage ringing, which typically increases the required diode breakdown voltage rating at least by a factor of two meaning that in an unclamped 600 V application 1200 V diodes would be required. This voltage ringing phenomenon was simulated with a PSpice model according to specifications in Table 1.1, Figure 2.4. The maximum diode voltage amplitude is more than two times the nominal secondary voltage indicating that a diode snubber is a necessity in the hard switched topology.

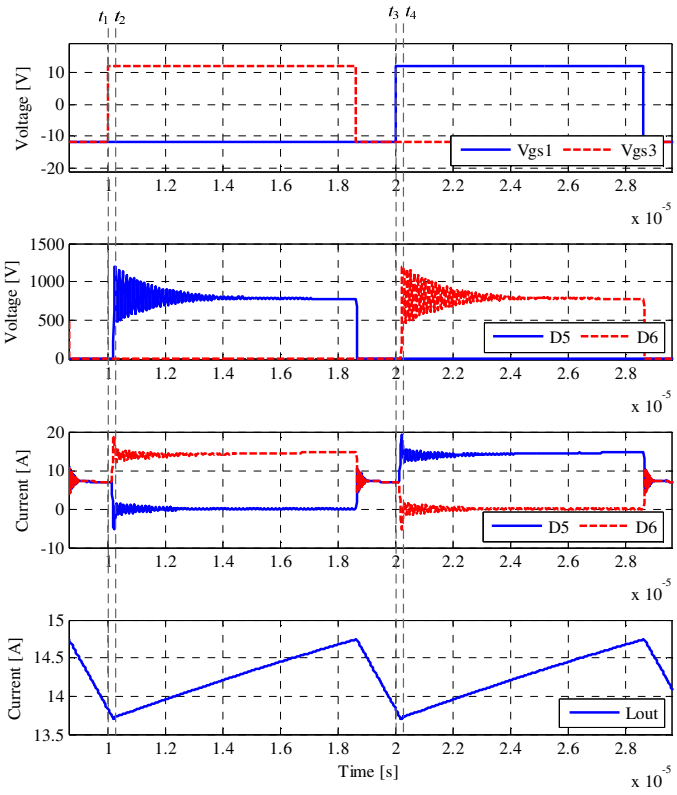


Figure 2.4: Simulated waveforms illustrating the secondary rectifier voltage overshoot. Waveforms from top: S_3 and S_1 control waveforms, diode D_5 and D_6 voltage, diode D_5 and D_6 current, output inductor current. The simulation model and a close-up view of the diode reverse recovery behavior are described in Appendix C.

Before t_1, all of the transistors are switched off, the secondary current is freewheeling through the diodes D_5-D_8 and the voltage across the transformer primary and secondary is zero. At t_1, transistors S_3 and S_4 are switched on and the current in diodes D_6 and D_7 start to increase with the rate $(V_{sec}\text{-}V_{out})/L_{lk}$, while diodes D_5 and D_8 undergo reverse recovery. During this reverse recovery period t_1-t_2, the voltage across the leakage inductance is limited to the transformer secondary voltage. At t_2, diodes D_5 and D_8 are able to support the reverse voltage thus allowing the leakage inductance voltage to overshoot and oscillate. At t_3 and t_4, the same process takes place with the opposite switching leg and diodes.

As the voltage-fed converter does not provide voltage boosting like current-fed converters, a large turns ratio is needed. Thus, more complex winding interleaving is required in order not to increase the transformer leakage inductance (Prieto et al., 1997; Vandelac and Ziogas, 1988). In high voltage applications additional snubber circuits are required to lower the diode breakdown ratings and voltage stress.

2.1.3 Primary current turn-on transient problem

As described in the previous section, the rectifier diode current commutation results in very low transformer secondary impedance, until the rectifier diodes corresponding to the non-conducting transistors have completely recovered. During this low impedance period the primary current increases by a rate determined by the leakage inductance in series with the reflected secondary impedance. After the diode reverse recovery period there is a damped oscillation of current and voltage, in which the maximum current amplitude is (Pressman, 1998)

$$I_{\mathrm{pk}} = \frac{V_{\mathrm{DC}} t_{\mathrm{rr}}}{L_{\mathrm{lk}}} \ , \tag{2.1}$$

where V_{DC} is the converter input voltage, t_{rr} is the specified reverse recovery time for the output rectifier diode and L_{lk} is the leakage inductance referred to the transformer primary. The oscillation frequency and amplitude are affected by the diode reverse recovery characteristics such as the recovery speed and softness factor. Figure 2.5 taken from a PSpice simulation demonstrates the primary current overshoot phenomena. The nominal input current is 200 A, but the maximum current peak reaches approximately 400 A. The current transient is drawn from the source having the lowest impedance, which is most likely the input capacitor.

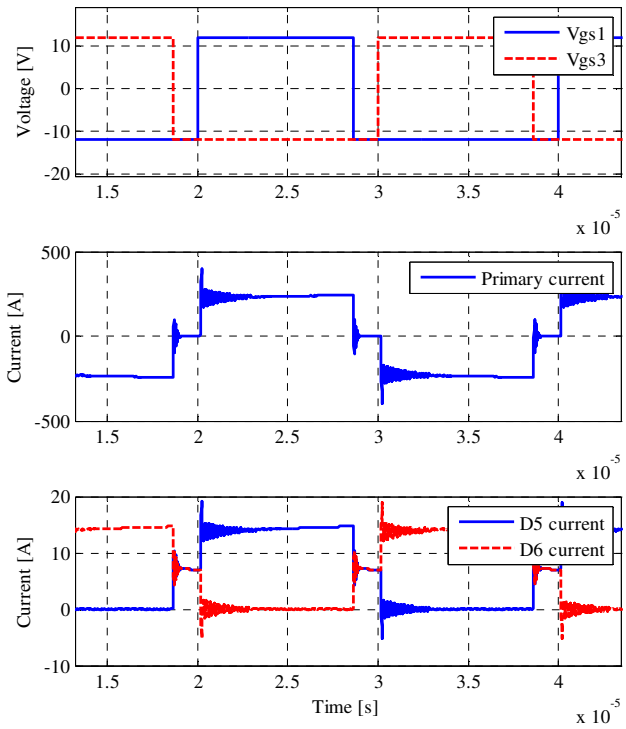


Figure 2.5: Primary current turn-on transient problem demonstrated by simulation.

2.1.4 Converter flux walking

Voltage-fed topologies utilizing diode bridge or center-tapped secondary configurations are particularly subject to transformer flux walking if there are differences in switching times between the switching legs. Due to component tolerances and the converter switching principle this is often the case. If the total transformer volt-seconds do not equal zero during the switching period, there will be an increasing DC flux in the transformer until the core walks into saturation. Creating headroom for unbalance by limiting the flux density is not a viable solution, as the flux walking process is cumulative over many cycles and in the case of a lack of inherent correction mechanisms the transformer will saturate. In current-fed converters the input inductor will limit the input current *di/dt* until the inductor saturates, thus decreasing the probability of total failure.

The voltage doubler output configuration helps to maintain the transformer volt-second balance, as was shown by Väisänen et al. (2010). The flux walking problem is balanced to some extent by positive temperature coefficients in switching elements (such as MOSFET) and the transformer. A common solution to prevent flux walking is to measure the transformer primary current in order to detect DC currents and to use current-mode control. The transformer primary current measurements are not so trivial in high current applications, as resistive sensing elements cause extra conduction losses and Hall effect sensors can experience high core losses due to large high frequency AC-currents. Placing a series capacitor at the transformer primary winding removes the DC-offsets, but in this case the capacitor has to be able to pass all of the power delivered to the transformer without experiencing excess losses and degrading.

2.1.5 Recent publications on the basic hard switched topology

In publications by Mohr and Fuchs (2006) and Mohr et al. (2010) voltage-fed full-bridge converter designed for 20 kW was compared to a current-fed full-bridge converter with the same specifications. The provided efficiency curves showed that the voltage-fed converter efficiency was 1-2% lower than the current-fed full-bridge efficiency over the whole load range. However, this comparison was based on calculations which were not verified with measurements. In the work by Nymand et al. (2009) a similar topology conversion with 1.5 kW converters was carried out. The measured efficiency of the voltage-fed converter was generally roughly 1-3.5% lower than the current-fed converter efficiency. Detailed loss budgets were not given, but the reasons mentioned for lower voltage-fed efficiency were higher switch currents and thus conduction losses, higher transformer winding losses and higher leakage inductance and ringing at the secondary (switching losses).

2.1.6 Advantages and disadvantages of the basic hard switched voltage-fed full-bridge converter

+ A low component count if snubbers are not needed in the secondary.

+ Low voltage stress on primary switches. This allows the usage of low voltage transistors, which generally have lower on-resistances than their higher voltage

counterparts. The need for snubbers on the high current primary side is eliminated if the input capacitor ESL is small enough.

- High switching stresses on primary switches. The switches are always switched with current and voltage overlapping with each other.
- Relatively high turn-off and RMS current on primary switches.
- The input current ripple can be high due to discontinuous operation. This requires large current handling capacity for the input capacitor.
- The duty cycle is limited between $0 < D < 0.5$ and in practice the dead time requirement reduces the maximum duty cycle even further.
- A large turns ratio is needed in boosting applications, which complicates transformer optimization.
- Large voltage spikes at the secondary rectifier diodes.
- Leakage inductance related duty cycle loss.
- A large output inductor is required to limit the output current ripple.
- Prone to transformer flux walking and saturation.
- There is no input inductor to limit current *di/dt* in case of a switching leg short circuit.

2.2 Phase-shifted PWM full-bridge ZVS converter

To overcome the high switching losses in a traditional voltage-fed full-bridge converter, a phase-shifted PWM modulation method is presented for example by Sabate et al. (1990) and Mweene et al. (1991). The basic topology is the same as in Figure 2.1. The gate control waveforms are presented in Figure 2.6.

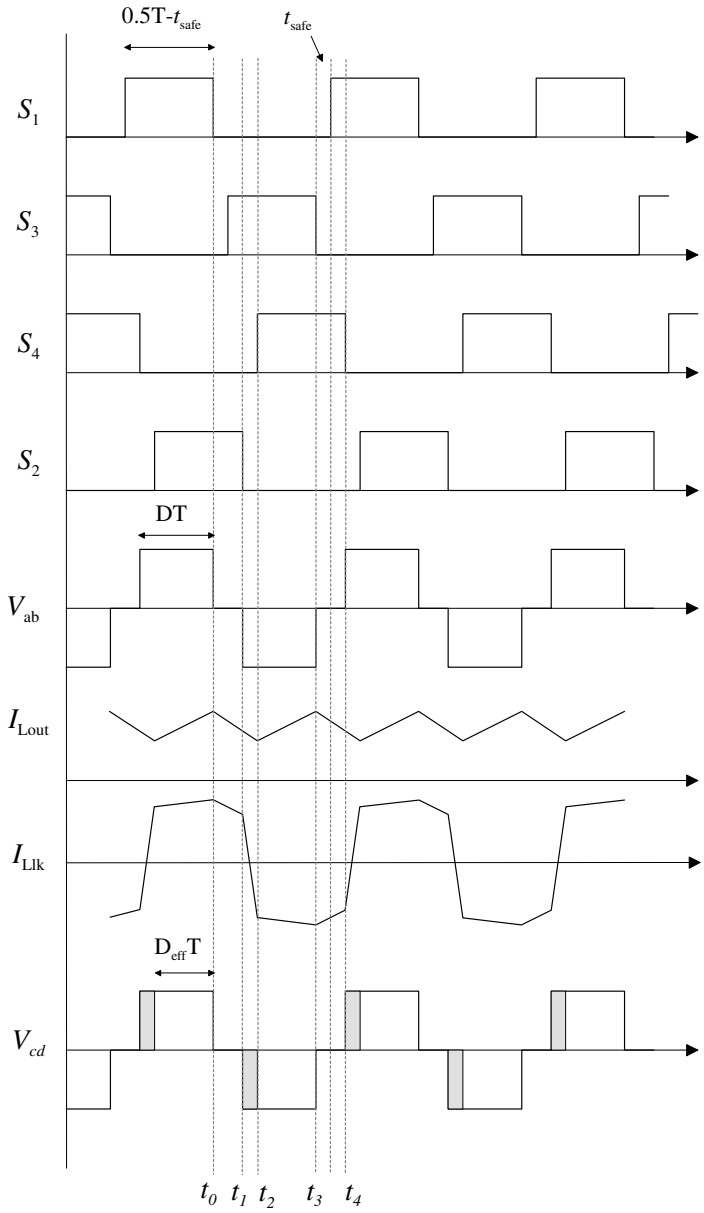


Figure 2.6: Phase-shift PWM converter gate control waveforms, transformer primary voltage, primary current and the voltage across the secondary rectifiers.

After S_1 and S_2 have been conducting S_1 is turned off at instant t_0. After a short dead time t_{safe}, transistor S_3 is turned on, thus enabling a freewheeling route for the reflected load current through the S_3 body diode and S_2. The leakage inductance resonates with the output capacitances of S_2 and S_4 charging the S_2 capacitor and discharging the S_4 capacitor. Transistor S_4 can be switched under zero voltage if its output capacitor has completely discharged and the body

diode is conducting before t_1. The critical current for the ZVS condition for S_2 and S_4 can be calculated from (Sabate et al., 1990; Mweene et al., 1991)

$$I_{\text{crit}} = \sqrt{\frac{2}{L_{\text{lk}}}\left(\frac{4}{3}C_{\text{ds}}{V_{\text{DC}}}^2 + \frac{1}{2}C_{\text{TR}}{V_{\text{DC}}}^2\right)}, \tag{2.2}$$

where C_{ds} is the drain-source capacitance of a primary transistor, C_{TR} is the transformer winding capacitance, L_{lk} is the leakage inductance as referred to the primary circuit and V_{DC} is the converter input voltage. The minimum load current corresponding to this critical primary current is (Sabate et al., 1990)

$$I_{\text{load}} > \frac{N_{\text{pri}}}{N_{\text{sec}}}I_{\text{crit}} - \frac{\Delta I_{\text{L}_{\text{out}}}}{2} + \frac{V_{\text{out}}}{L_{\text{out}}}(1-D)\frac{T}{2}, \tag{2.3}$$

where D is duty cycle in the primary, N_{pri} and N_{sec} are the number of primary and secondary transformer turns, respectively, ΔI_{Lout} is the output inductor current ripple and T is the period length. For transistors S_1 and S_3 the ZVS is provided by the energy in the output inductor, which typically is high enough to provide ZVS over the whole load range.

2.2.1 Zero voltage switching and turn-on losses

The importance of zero voltage switching is emphasized at higher input voltages and switching frequencies. In low voltage and high current applications the difference in switching losses may not be significant. There are always some losses related to ZVS, as the switch freewheeling diode is conducting the circulating current and there is a forward voltage drop across the diode. The reverse recovery loss in the MOSFET intrinsic diode is negligible despite the large forward current during conduction, as the voltage across the switch remains near zero during the recovery. Figures 2.7 and 2.8 demonstrate the differences between hard switching and zero voltage switching in the topology of Figure 2.1.

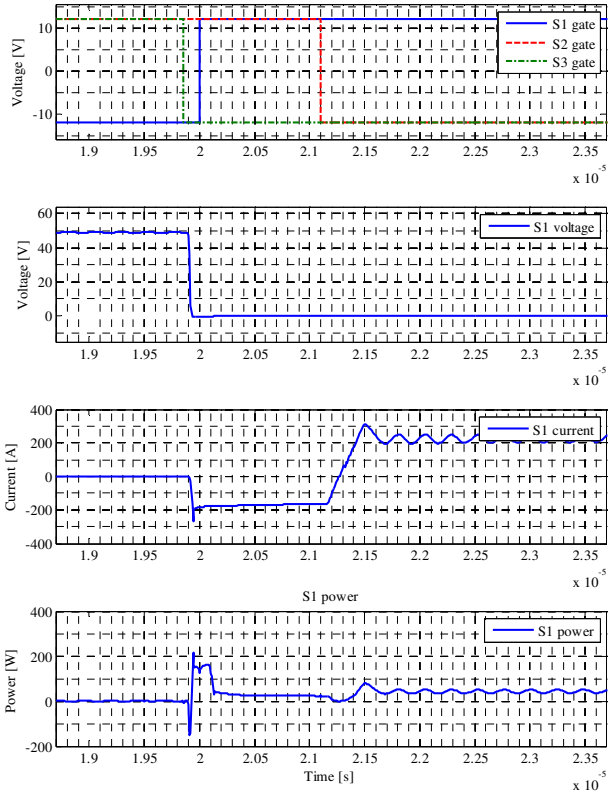


Figure 2.7: Zero voltage switching in the phase-shift PWM converter for transistor S_1, in which the ZVS is provided by the energy in the output inductor. The S_1 body diode begins to freewheel the reflected load current after transistor S_3 is turned off and the voltage across S_1 drops at the forward voltage of the freewheeling diode.

The simulated turn-on loss in Figure 2.7 is 3 W per transistor. The majority of the losses are conduction losses from the transistor channel since the current commutates from the body diode to the transistor channel after the gate voltage has been applied. Therefore, the turn-on losses are strongly dependent on the freewheeling current amplitude, which is the reflected secondary current times the turns ratio, and the dead time and freewheeling period lengths. If the current commutation from the body diode to the transistor channel takes time or if the dead time is long, the diode conduction losses can be high due to a large average and RMS current. This is demonstrated in chapter 4.

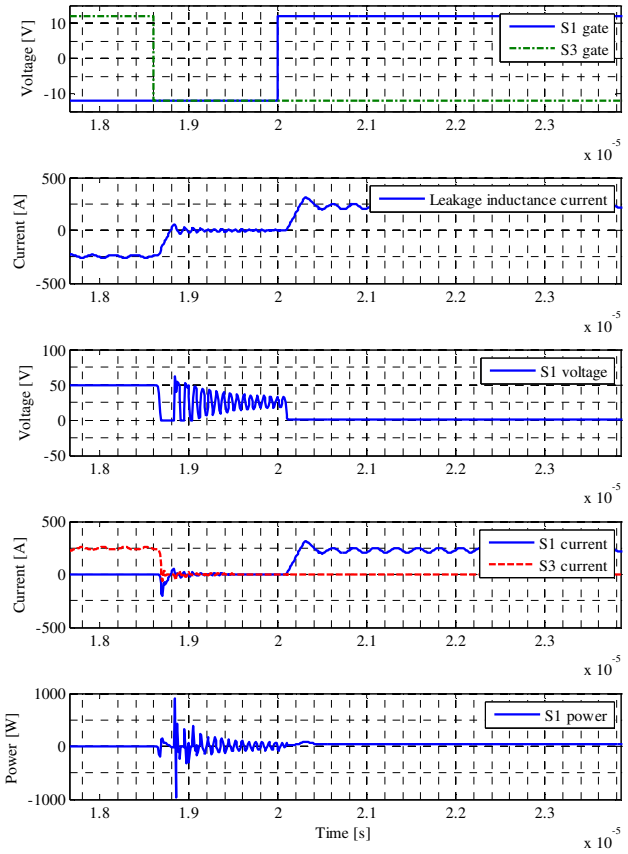


Figure 2.8: Turn-on behavior of S_1 in the hard switched voltage-fed converter at D = 0.43. After transistors S_3 and S_4 are turned off, the output current freewheels through the secondary rectifier diodes. This causes small resonance currents at the primary circuit, which are seen as fluctuating voltage across transistor S_1. The voltage is pulled down to zero before S_1 conducts the whole current, as the leakage inductance presents a high impedance for the current at turn-on.

The simulated turn-on loss in Figure 2.8 is 6 W per switch, which is more than in the zero voltage switched phase-shift PWM converter. The reason for the higher losses is that the losses occur in the transistor body diode, as no gate voltage is applied to S_1 while the transistor current and voltage are resonating. After transistor S_3 is turned off, the voltage of transistor S_1 is pulled down to the forward voltage of the intrinsic diode since the diode is conducting the difference current between transistor S_3 and the leakage inductance. If the leakage inductance is large enough to keep the current circulating until S_1 is turned on, transistor S_1 is turned on with zero voltage.

In the case of hard switching and MOSFETs, the increase in primary voltage requires more power handling capacity from the gate drive circuit to overcome the Miller effect in order to keep the switching transitions and thus the gate voltage plateaus, during which the transistor is in the linear region dissipating a great deal of power, short in duration. With zero voltage switching, the Miller effect is eliminated at turn-on, while still present at turn-off.

2.2.2 Turn-off losses

As demonstrated in the previous section and by Nymand (2010), the energy in the circuit inductances is usually great enough to discharge the output capacitances of the switches before the switches conduct the whole load current. In addition, the inductances also delay the current rise before the voltage across the switch is pulled down. This results in very small turn-on losses in low voltage applications. In the case of ZVS, the turn-on Miller effect is negligible, and consequently, the switching transitions through the linear region can be very fast, thus reducing losses.

Figure 2.9 shows the turn-off process when there is 60 nH inductance in series with the input capacitor. In practice this can result from the capacitor itself and the external connections. The rapidly changing capacitor current generates an opposing voltage in the parasitic inductance and there is a voltage overshoot and oscillation between the inductance and circuit capacitances. The transformer leakage inductance aims to maintain the flowing current at turn-off and extends the overlap between the increasing transistor voltage and decreasing current. In the Figure 2.9, there is a 15 kW peak loss power with a current fall-time of 350 ns, which would result in a loss energy of 2.6 mJ and a total turn-off loss of 130 W at 50 kHz. This illustrates the insignificance of turn-on losses (3 W in Figure 2.7) compared to the turn-off losses. The same phenomenon is demonstrated with calculations in chapter 4.

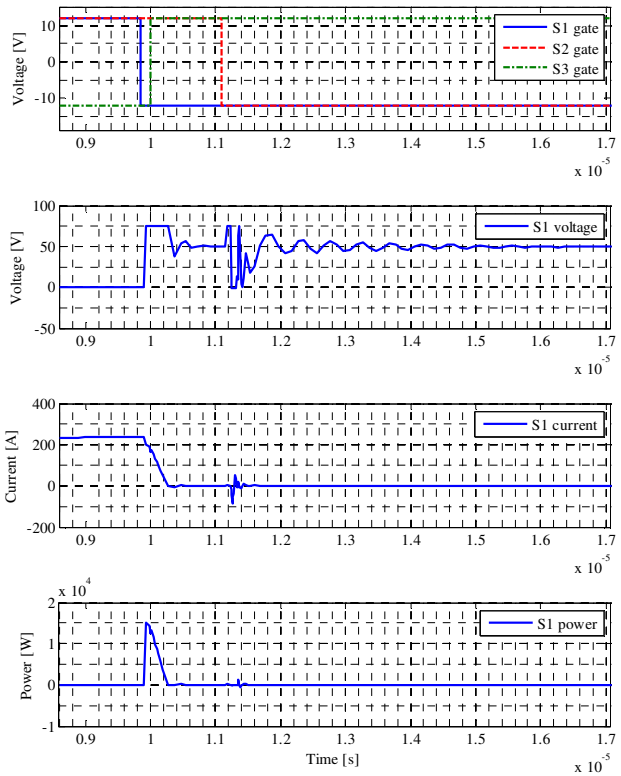


Figure 2.9: Simulated turn-off behavior of S_1 in the phase-shift PWM converter. There is a voltage overshoot and oscillation caused by the input capacitor ESL.

The turn-off losses of the phase-shift converter as well as the hard switched counterpart can be reduced by selecting an input capacitor with low ESL, minimizing the parasitic inductances in the circuit layout and using as fast a transistor gate turn-off as possible. The turn-on and turn-off behavior described previously can also be seen in the waveforms measured from a 150 W converter (Figure 2.10).

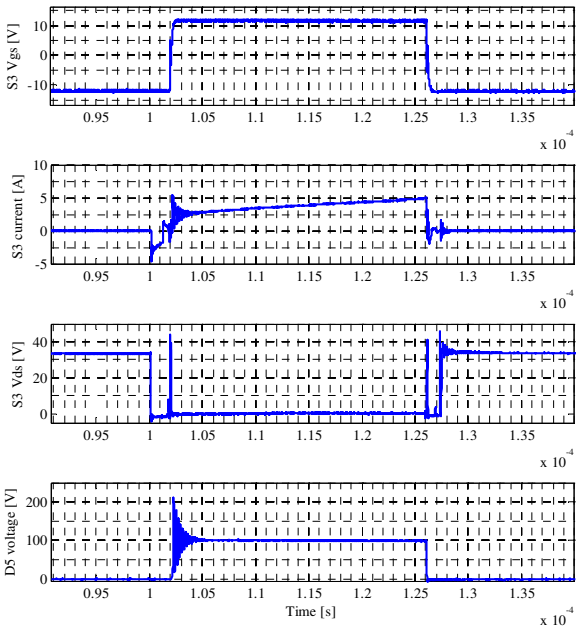


Figure 2.10: Measured waveforms from a 150 W phase-shift FB converter.

The nominal primary voltage in the measurement was 35 V and nominal output voltage was 100 V. The transistor drain-source voltage spikes exceeding the primary voltage are caused by the parasitic inductances including the input capacitor ESL. The secondary rectifier ringing is clearly visible and the maximum voltage peak is more than two times the nominal output voltage. In this case, 400 V rectifiers were used.

2.2.3 Output inductor current ripple

During the time period t_0-t_1 in Figure 2.6 the leakage inductance current flows on the primary side and the current generates a voltage drop across the primary winding resistance, the transistor S_2 drain-source resistance and the body diode of the transistor S_3 (Figure 2.11). On the secondary side, the current has been flowing through D_5 and D_8 before t_0, but after t_0, part of the current starts to freewheel also through D_6 and D_7.

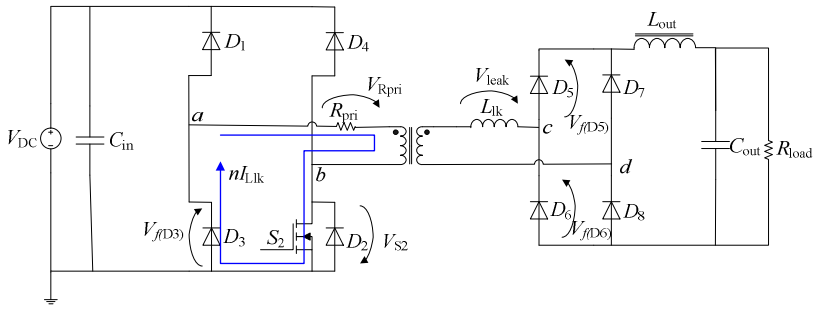


Figure 2.11: Reflected leakage inductance current in the primary circuit (leakage inductance referred to the secondary side) and the voltage drops generated by the freewheeling current.

The voltage drop generated by the freewheeling leakage inductance current is seen in the transformer primary and reflected on the secondary through the transformer turns ratio. The voltage across the leakage inductance during t_0-t_1 can be expressed as

$$V_{\text{leak}} = n\left(\left|V_{\text{S2}}\right| + \left|V_{\text{Rpri}}\right| + \left|V_{\text{f(D}_3\text{)}}\right|\right) + \left|V_{\text{f(D}_5\text{)}} - V_{\text{f(D}_6\text{)}}\right| \tag{2.4}$$

where the turns ratio n is defined as $N_{\text{sec}}/N_{\text{pri}}$. The rate of change in the leakage inductance current during t_0-t_1 can be calculated from

$$\frac{dI_{\text{L}_{\text{lk}}}}{dt} = \frac{V_{\text{leak}}}{L_{\text{lk}}} \tag{2.5}$$

and the length of time interval t_0-t_1 is

$$t_1 - t_0 = \left[(0.5 - D)T\right] - t_{\text{safe}}, \tag{2.6}$$

where D is the primary duty cycle and t_{safe} is the safe time between the transistors in the same switching leg. Approximating the peak leakage inductance current at instant t_0 to be equal to the load current, the leakage inductance current at instant t_1 is

$$I_{\text{L}_{\text{lk}}}(t_1) = I_{\text{load}} - \frac{V_{\text{leak}}}{L_{\text{lk}}}(t_1 - t_0). \tag{2.7}$$

The length of time interval t_1-t_2 can now be calculated from

$$t_2 - t_1 = \frac{\left(I_{\text{L}_{\text{lk}}}(t_1) + I_{\text{load}}\right)L_{\text{lk}}}{n \cdot V_{\text{DC}}} \tag{2.8}$$

and the output inductor discharge time interval t_2-t_0 from

$$t_2 - t_0 = \frac{L_{\text{leak}}\left(2I_{\text{load}} + \dfrac{V_{\text{leak}}\left(t_{\text{safe}} + (D - 0.5)T\right)}{L_{\text{lk}}}\right)}{n \cdot V_{\text{DC}}} - (D - 0.5)T - t_{\text{safe}}. \tag{2.9}$$

If the leakage inductance is so small that the leakage inductance current goes to zero before instant t_1, Equation (2.9) is no longer valid. The output inductor discharge time in this case is

$$t_2 - t_0 = (0.5 - D)T + \left(\frac{I_{\text{load}} L_{\text{lk}}}{n \cdot V_{\text{DC}}} \right). \tag{2.10}$$

The output inductor current ripple percentage (peak-to-peak) can now be calculated from

$$r = \frac{V_{\text{out}}}{L_{\text{out}}} (t_2 - t_0) \,. \tag{2.11}$$

The output inductor current ripple is dependent on the output inductance and output voltage but also on the duty cycle, freewheeling current amplitude and corresponding primary voltage drops and the leakage inductance. The output inductor discharge time increases if the leakage inductance is increased. Therefore, in order to maintain the same output current ripple with a larger leakage inductance and thus a wider zero voltage switching range, the output inductor must have a higher inductance. This can result in higher output inductance winding losses.

2.2.4 Duty cycle loss

The primary voltage applied to the transformer primary is not completely applied to the load, as the secondary rectifiers are effectively short circuited when the primary current is changing its direction. The transformer secondary voltage is not seen across the secondary rectifiers until the freewheeling rectifier pair stops conducting and completes the reverse recovery process. The duty cycle loss can be seen in Figure 2.6 as a grey shaded area in V_{cd} and the effective duty cycle can be calculated from

$$D_{\text{eff}} = \frac{DT - (t_2 - t_1)}{T} \,. \tag{2.12}$$

If the leakage inductance current goes to zero before instant t_1, the effective duty cycle is

$$D_{\text{eff}} = \frac{DT - \left(\frac{I_{\text{load}} L_{\text{lk}}}{n \cdot V_{\text{DC}}} \right)}{T} \tag{2.13}$$

The duty cycle loss is made worse by increasing the leakage inductance since the leakage inductance current commutation interval t_1-t_2 is increased.

2.2.5 Transformer secondary voltage and output regulation

During the time interval t_2-t_3 when the output inductor is charging, there is a voltage across the output inductor according to

$$V_{\text{L}_{\text{out}}} = V_{cd} - V_{out} \quad . \tag{2.14}$$

During the time interval t_0-t_2 the voltage across the output inductor is $-V_{out}$. To obtain a certain output voltage, the transformer secondary voltage during $D_{eff}T$ must be

$$V_{cd} = \frac{V_{out}}{2D_{eff}}. \tag{2.15}$$

This secondary voltage requirement is directly related to the output voltage regulation, as in the basic buck converter, in which the output voltage $V_{out} = DV_{in}$, where the duty cycle range is $0 < D < 1$.

2.2.6 Advantages and disadvantages of the phase-shift PWM full-bridge converter

+ Low component count if snubbers are not needed in the secondary.
+ Low voltage stress on primary switches.
+ ZVS turn-on possibility for the primary switches.
− Large circulating currents at the primary can cause relatively high turn-on losses despite ZVS.
− The input current ripple can be high due to discontinuous operation.
− The effective duty cycle is limited between $0 < D < 0.5$ and in practice the dead time requirement reduces the maximum duty cycle even further.
− Relatively high turn-off and RMS current on primary switches.
− A large turns ratio is needed in boosting applications.
− Large voltage spikes at the secondary rectifier diodes.
− Leakage inductance related duty cycle loss.
− Output inductor related voltage loss from transformer secondary to output.
− Prone to transformer flux walking and saturation.
− There is no input inductor to limit the current *di/dt* in the case of a switching leg short circuit.

2.3 Phase-shifted PWM FB ZVS converter with auxiliary saturable resonant inductor

The duty cycle loss described in section 2.2.3 can be reduced by minimizing the transformer leakage inductance and adding a saturable inductor in series with the transformer primary, as in Figure 2.12 (Hua et al., 1993; Chen et al., 1995).

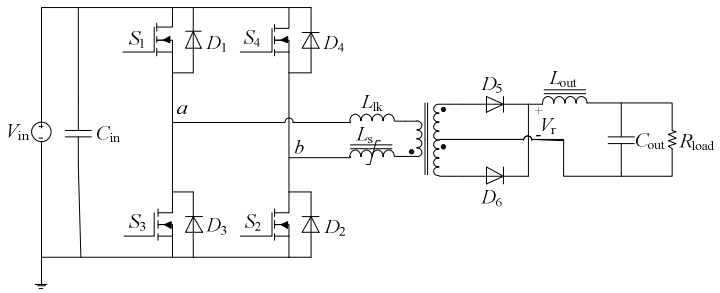


Figure 2.12: Phase-shifted PWM full-bridge converter with an auxiliary saturable resonant inductor to reduce the duty cycle loss.

The saturable inductor is designed so as to include the desired inductance value at the reflected load current values below the critical current I_{crit}. Figure 2.13 shows the theoretical waveforms for the phase-shift converter when utilizing a saturable resonant inductor.

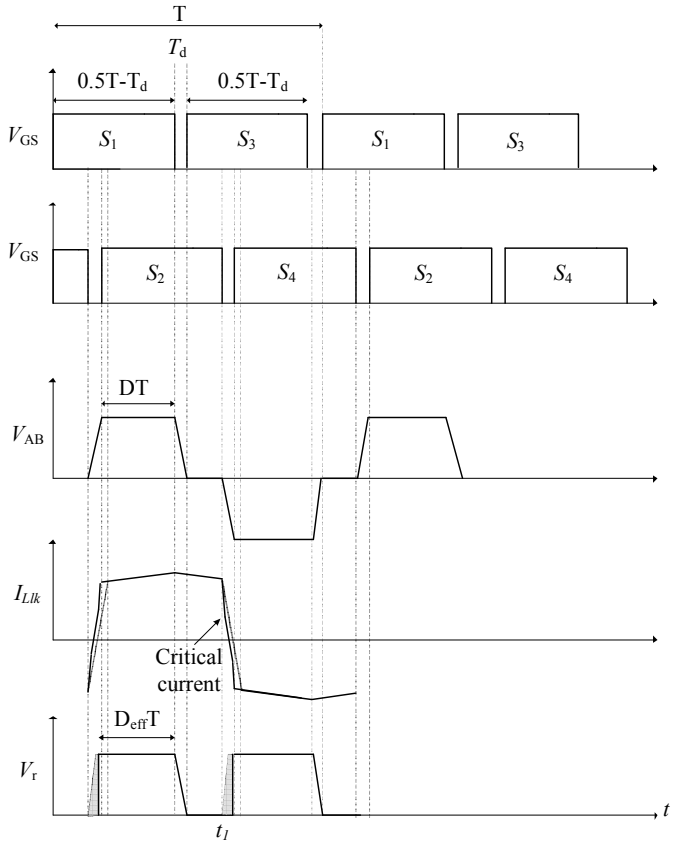


Figure 2.13: Phase-shift PWM converter gate control waveforms, transformer primary voltage, primary current and the voltage across the secondary rectifiers when utilizing a saturable resonant inductor.

When transistor S_2 is turned off at instant t_1, the primary current falls rapidly to the critical current. Below this critical current the inductor is no longer saturated and starts to resonate with output capacitances of S_2 and S_4 in such a manner that the S_2 capacitor is charged and the S_4 capacitor is discharged before the instant when S_4 is turned on. The same applies to the next switching cycle in reverse order. The ZVS for the transistors S_1 and S_3 is obtained through the output inductor energy as described in section 2.2.

The saturable resonant inductor approach can outperform the conventional phase-shift converter in efficiency over the entire load range (Chen et al., 1995), as the duty cycle loss at the secondary is reduced because the current commutation times are shorter and the ZVS range is larger than in the conventional phase-shift converter. The problem with the saturable inductor is large core losses at high switching frequencies, as the flux swings between positive and negative saturation levels. There are also additional skin effect and proximity losses in the saturable inductor windings, as the inductor current is mainly an alternating current. The other advantages and disadvantages of this converter topology are very similar to the ones presented in section 2.2.

2.4 Phase-shifted PWM FB ZVS converter with secondary side control

The previous two approaches to achieve the ZVS condition for the bridge switches are load current dependent. This means that the reflected load current, provided either by the output inductor or the transformer leakage inductance, is large enough to provide oscillation in the primary circuit, which charges and discharges the switch output capacitances. In order to reduce the ZVS load dependence, a phase-shifted full-bridge converter with secondary side control has been proposed by Watson and Lee (1998). The primary circuit is identical to the basic phase-shift full-bridge converter, but there are two additional switches at the secondary side and a freewheeling diode for the output current, as the secondary switches are both off (or in a high impedance state) for a while.

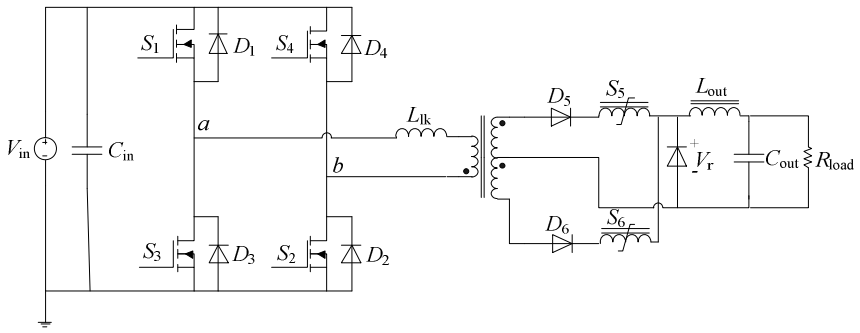


Figure 2.14: Phase-shifted PWM full-bridge ZVS converter with secondary side switches enabling the utilization of magnetizing inductance to achieve zero voltage switching.

Switches S_5 and S_6 can be realized with any controllable switching element, but Watson and Lee (1998) used magnetic amplifiers. A magnetic amplifier consists of a magnetic core with near square hysteresis characteristics, a main winding to carry the load current and a control winding to provide sufficient DC bias to drive the magnetic core to saturated or unsaturated state.

The theoretical switching waveforms for the phase-shifted converter with secondary control are depicted in Figure 2.15.

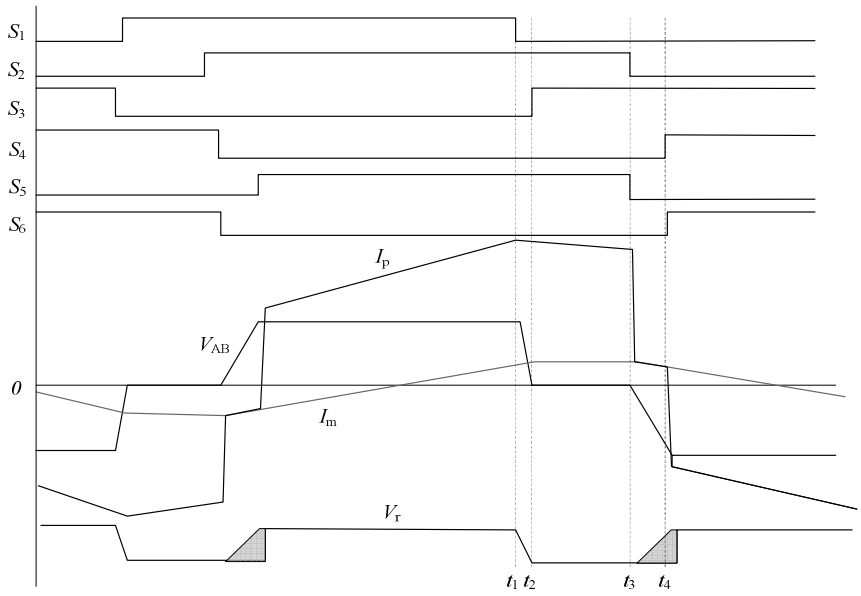


Figure 2.15: Phase-shift PWM converter gate control waveforms when utilizing the transformer magnetizing current for ZVS.

At instant t_1, S_1 is turned off while S_2 is still on and D_5 and S_5 are conducting the load current. Between t_1 and t_3, the reflected output current plus magnetizing current is freewheeling through S_2 and D_3 while the output capacitances of S_1 and S_3 are charged and discharged, respectively, providing zero voltage turn-on for S_3. At t_3, transistor S_2 is turned off and switches S_5 and S_6 are set in a high impedance state leaving the transformer secondary in an effectively open state, which causes the primary current to fall to its magnetizing current value. The primary current has a high *di/dt* during this transition, as the leakage inductance is small. Between t_3 and t_4, the open secondary allows the magnetizing inductance together with the leakage inductance to resonate with the output capacitances of S_2 and S_4, and before t_4, the body diode of S_4 is conducting and thus S_4 can be switched on under zero voltage.

The required magnetic switch core size can be determined by calculating the area product (in cm^4) based on the wire size, the blocking time in volt-seconds and the core parameters as follows (Mammano, 2001):

$$A_p = A_w A_c = \frac{A_{wire} \cdot \Lambda \cdot 10^4}{(B_{sat} - B_{reset}) \cdot K}, \tag{2.16}$$

where A_w is the core window area in cm^2, A_c is the core effective area, A_{wire} is the wire cross-sectional area, Λ is the required blocking time in volt-seconds, B_{sat} is the core saturation flux density in Tesla, B_{reset} is the required resetting flux density for the magnetic amplifier and K is a fill factor typically ranging between $0.1 \leq K \leq 0.3$. The number of turns needed is acquired from

$$N = \frac{\Lambda \cdot 10^4}{(B_{sat} - B_{reset}) \cdot A_c} \tag{2.17}$$

It can be seen from (2.16) that with high output voltages, such as in a DC-DC converter interfacing a three phase inverter DC-link, the required area product for a single magnetic switch is large, as the voltage dependent blocking time is in the numerator. Also the number of turns (2.17) is increased together with the increased volt-second requirement. A possible solution would be to use several switches in series, but this increases both conduction and total core losses. The use of semiconductor switches requires high voltage transistors or IGBTs and there are large switching and conduction losses involved. The achieved efficiency of this converter topology presented by Watson and Lee (1998) was between 85-91% in the power range of 250-1000 W. Chen et al. (1995) reported efficiencies between 90-95% at a load range of 100-1000 W.

The increased magnetizing current causes extra conduction losses in the primary. Therefore, an alternative configuration and control for the secondary switches has been proposed by Hitchcock et al. (1992). In this solution the secondary switches are on the cathode side of the rectifier diodes and the control signals of the switches are overlapping allowing the output inductor freewheeling current to employ ZVS for the primary switches. Also, no separate freewheeling diode is needed for the secondary switches.

The advantages/disadvantages for these approaches compared to the basic phase-shift topology can be summarized as follows:

+ Wide and load independent ZVS range.

+ Very small secondary diode voltage oscillation and thus no need for snubbers.

+ Possibility for secondary side voltage regulation.

- Additional freewheeling diode and snubber required in the non-overlapping approach (Watson and Lee, 1998).

- Increased conduction losses in the non-overlapping approach due to an increased magnetizing current.

- Design issues and losses with secondary switches in high voltage applications whether implemented with magamps or semiconductors.

2.5 Phase-shifted PWM FB converter with ZVS and ZCS using voltage doubler secondary

The phase-shifted PWM converter can be realized with a voltage doubler secondary as in the study by Lee et al. (2008). The large output inductor can be eliminated since the voltage doubler circuit acts as an LC filter in this case. The transistor control for the converter is similar to that of the basic phase-shift converter.

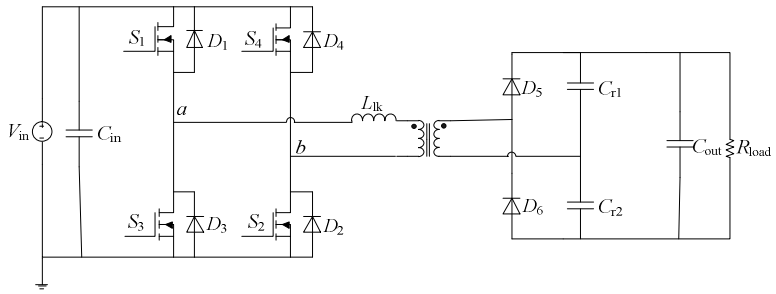


Figure 2.16: Phase-shifted PWM converter with a voltage doubler output. The output inductor can be neglected or included for tuning the resonant frequency.

As seen in Figure 2.16, primary switches can be operated in both ZCS and ZVS and the secondary rectifier diodes in ZCS. There is no diode voltage overshoot, as the voltage is clamped to the maximum secondary voltage value.

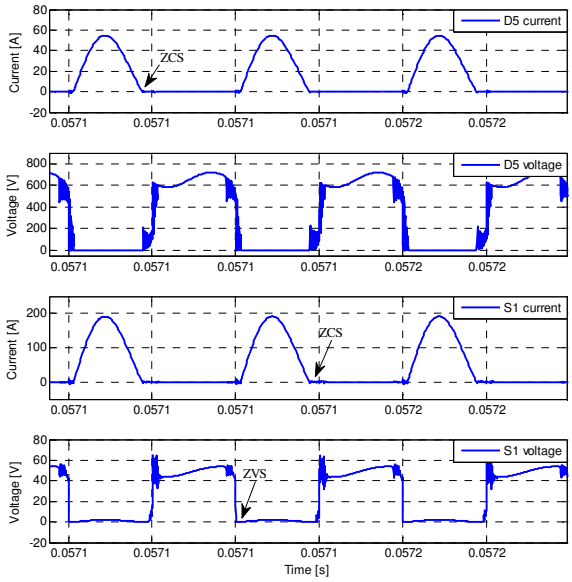


Figure 2.17: Simulated waveforms of a phase-shifted PWM converter with ZCS and ZVS. The switching losses are very small, but the currents of the switches and secondary diodes are comparatively higher, which increases conduction losses.

The problem with the PSFBVD topology is the poor output voltage regulation as a function of the duty cycle. Since there is the voltage doubler configuration and no output inductor to provide the regulation, the average output voltage is dependent on the resonant circuit characteristics and the output RC discharge time constant during a time period of $T/2$-$D_{eff}T$. Figure 2.18 illustrates an example of the V_{out}/V_{in} characteristics in step-down operation when calculated with the circuit parameters and the operating conditions given by Lee et al. (2008).

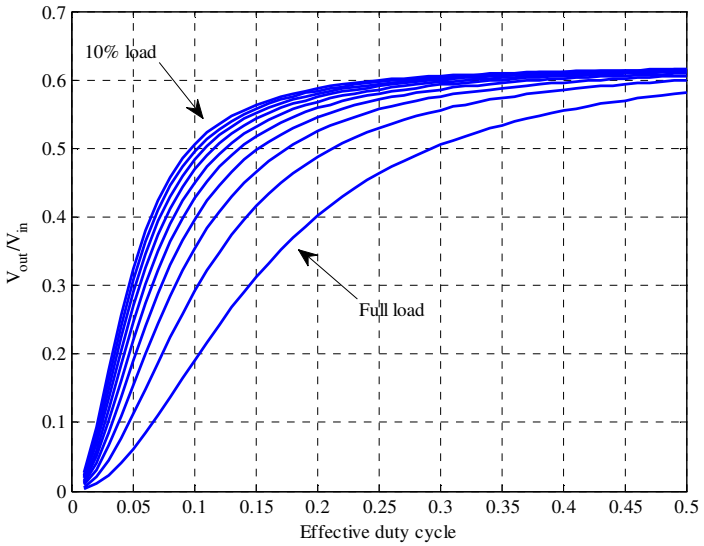


Figure 2.18: PSFBVD output voltage regulation as a function of the effective duty cycle in step-down operation when calculated with the circuit parameters and the operating conditions given by Lee et al. (2008).

The advantages/disadvantages of this approach can be summarized as follows:

+ ZVS and ZCS for the primary switches, particularly effective for reducing switching losses in the case of high voltages and/or currents.

+ ZCS for the secondary rectifier diodes, eliminates the reverse recovery effects.

+ Rectifier diode voltage clamped at output voltage, no need for diode snubbers.

+ Reduced transformer turns ratio.

+ Increased tolerance for flux walking due to inherent balancing by the voltage doubler capacitors.

+ No bulky output inductor.

- Large current stress on primary switches, output rectifier diodes and capacitors.

- Discontinuous input current leading to potentially high current ripple and stress on the input capacitors.

- Poor output voltage regulation as a function of duty cycle, which can result in a narrow input voltage range.

2.6 Current harmonics of the basic voltage-fed topologies

The frequency bandwidth of the electromagnetic emissions of an electrical switching circuit is dependent on the maximum rise/fall times in the circuit. The shorter the transition times, the wider the emission frequency bandwidth. The rise and fall times are dependent on the properties of the switching components and on the operational principle of the converter. For example in a resonance converter the maximum rate of change in current is often limited by the resonance components, not by the switch itself. The maximum amplitude for the fundamental component in the frequency spectrum is determined by the maximum current in the system and the frequency of the fundamental and its harmonic components are determined by the switching frequency.

The other frequency components and their amplitudes in the spectrum are dependent on the switching transitions and the resonances related to them and the shape of the current waveforms. In non-resonance converters with near square current waveforms there are many high frequency components involved and if zero voltage or zero current switching is not utilized, there can be high frequency oscillations in current and voltage at each switching transition. Figure 2.19 shows an example of the current harmonics in three different voltage-fed topologies.

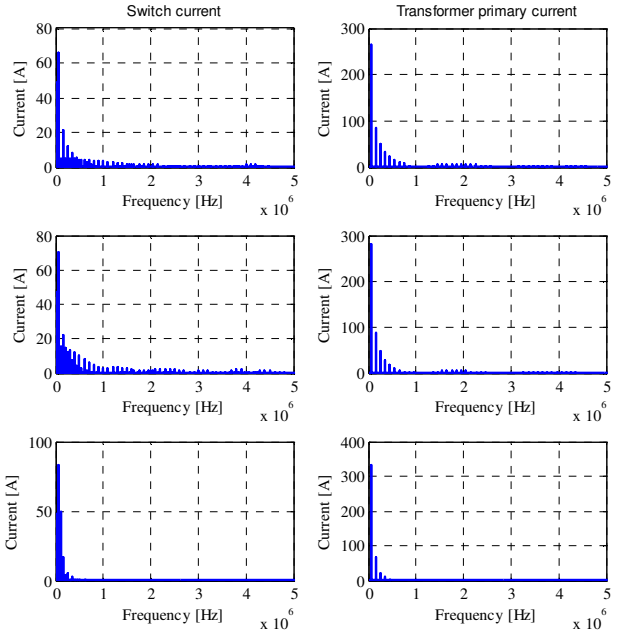


Figure 2.19: Simulated harmonic current spectrum in a hard switched full-bridge (top), a phase-shifted full-bridge (middle) and a phase-shifted full-bridge with a voltage doubler secondary (bottom). The ZVS and ZCS operation together with resonant current waveforms in the voltage doubler configuration results in the lowest harmonic content.

The spectra of the hard switched converter and the basic phase-shifted converter are very similar and no significant advantage in reduced harmonics can be seen in the phase-shifted converter in

spite of the ZVS operation. Both converters operate with near square current waveforms with oscillations at turn-on and turn-off, and there is an additional circulating primary current component in the phase-shift converter. The high frequency components in the transformer primary current will result in increased conduction losses, as the proximity effects increase dramatically in tightly packed and stacked windings, which often is the case in a transformer with a large number of turns.

2.7 Summary

The experimental efficiencies of the presented phase-shift PWM voltage-fed converters are summarized in Table 2.1.

Table 2.1: Summary of experimental efficiencies for phase-shift PWM voltage-fed converters.

Topology	Source	Power range	Efficiency
2.2	Sabate et al. (1990)	180-2000 W	76-94.5%
2.2	Chen et al. (1995)	100-1000 W	80-94.7%
2.3	Hua et al. (1993)	50-200 W	77-88%
2.3	Chen et al. (1995)	100-1000 W	86-95.1%
2.4a	Chen et al. (1995)	100-1000 W	89-94.7%
2.4a	Watson and Lee (1998)	100-1000 W	73-91%
2.4b	Chen et al. (1995)	100-1000 W	88-95.1%
2.5	Lee et al. (2008)	45-450 W	86-96%

The efficiency of the basic phase-shift PWM converter presented by Sabate et al. (1990) was nearly constant after the ZVS condition was achieved at a 650 W load. In a comparative analysis presented in the study by Chen et al. (1995) it was noted that due to the large linear resonant inductor, a lossy secondary rectifier snubber had to be used in order to reduce the voltage ringing, and that the narrow ZVS range degraded the efficiency at light loads.

In the phase-shift converter with a saturable inductor introduced by Chen et al. (1995) the voltage ringing was lower than with the linear resonant inductor and more efficient snubbers with a smaller capacitor and larger resistor could be used. Also the duty cycle loss was smaller and the ZVS range was wider than in the basic phase-shift converter.

Converters with secondary side control were also implemented by Chen et al. (1995). The efficiency of the approach with non-overlapping secondary control (Watson and Lee, 1998) was slightly lower than with the overlapping control (Hitchcock et al., 1992). In the non-overlapping approach, a lossy snubber circuit is needed for the freewheeling diode of the secondary switches, whereas the overlapping approach does not require the extra diode and snubbers. Also the increased magnetizing current in the non-overlapping approach results in increased conduction losses. Both approaches have very low secondary ringing if using saturable reactors.

The reported efficiency for a converter using the voltage doubler secondary (Lee et al., 2008) was slightly over 96% with a 450 W output power. The efficiency was measured in a case of quasi-sinusoidal current waveforms in order to reduce the maximum current stresses and conduction losses, and thus the primary switches and secondary diodes were not switched under zero current. In high primary current and high secondary voltage applications the utilization of ZCS can overcome the increased conduction losses in terms of reduced switching losses.

In measurements conducted by the author (see Appendix B for equipment), the basic phase-shift converter efficiencies ranged from 87% to 94% at the power range of 50-150 W. The secondary rectifier voltage ringing had the largest negative impact on the efficiency.

3 Isolated current-fed topologies for medium to high power applications

The current-fed converters can operate both below and above a duty cycle of 50%. Duty cycles below 50% require an additional freewheeling circuit for the input inductor current and a primary snubber circuit can serve this purpose. The primary input energy storage component is an inductor and the maximum voltage achievable at transformer primary depends on the volt-seconds applied to the input inductor.

3.1 Full-bridge boost

The common variants of a full-bridge-based current-fed DC-DC converter topology can be divided into active clamped and passive clamped converters or a combination of passive and active clamping as in the work of Zhu (2006). The full-bridge boost topology does not necessarily need any clamping circuits if the transformer is optimized for a small leakage inductance (Nymand and Andersen, 2008). The basic current-fed full-bridge topology without clamping circuits is presented in Figure 3.1.

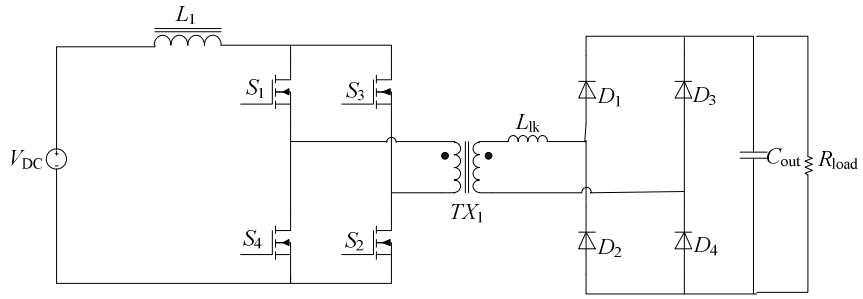


Figure 3.1: The basic current-fed full-bridge topology without clamping circuits.

The unclamped topology can be implemented with three different secondary configurations: a diode bridge, a center-tapped transformer and two diodes, or with a voltage doubler. Each of the output configurations has its own advantages and disadvantages. The diode bridge and the center-tapped configuration provide a smaller current stress on the diodes, but they cannot oppose transformer flux walking in the case of primary switching asymmetries. The use of a center-tapped transformer allows a reduction in the number of diodes, but it complicates the transformer structure and winding layout optimization. The voltage doubler brings out the following design points:

- A VD needs only half of the turns in the secondary winding compared with a diode bridge, but it needs larger copper area to handle the increased current.
- No transformer center tapping is needed, which simplifies the transformer structure.
- Only two diodes are needed in the secondary, but the diodes must be able to handle twice the average current.
- The VD capacitors must be able to withstand large pulse and RMS currents.

- The voltage doubler configuration is more tolerant of switching asymmetries, and it inherently opposes transformer flux walking (Väisänen et al., 2010).

3.1.1 Operating principle of the full-bridge boost converter

Figure 3.2 presents the basic operating waveforms of a full-bridge boost converter.

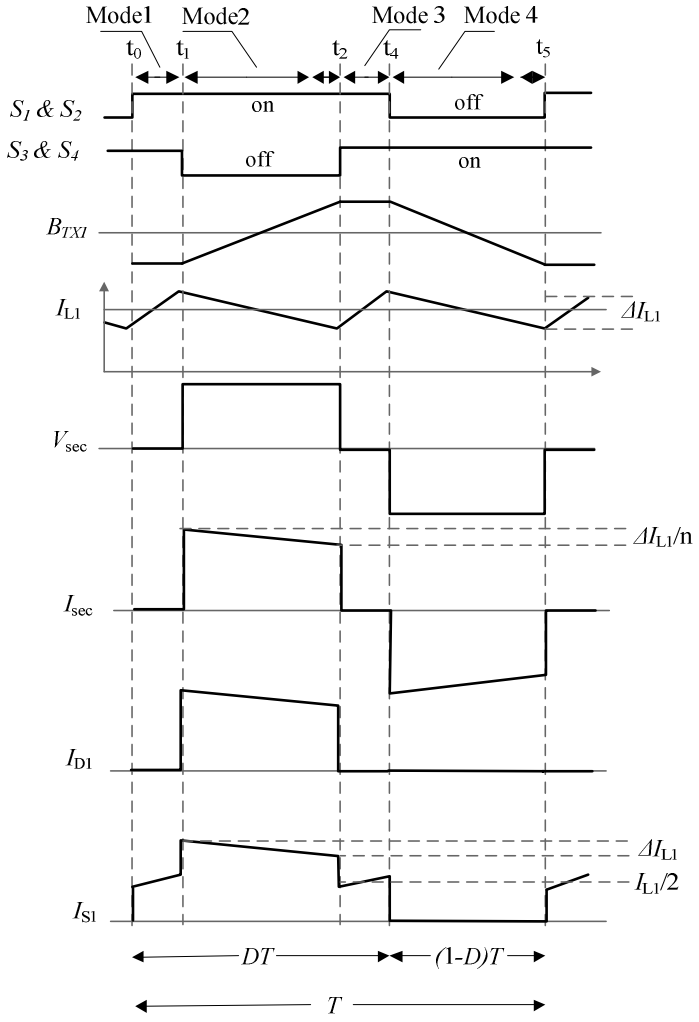


Figure 3.2: Basic operating waveforms for a full-bridge boost converter.

Mode 1

At instant t_0, all transistors are conducting, the input current is divided between both switching legs and a small magnetizing current is flowing through the transformer primary winding. The load current is supplied by the output capacitor.

Mode 2

At instant t_1, transistors S_3 and S_4 are turned off and the current through S_1 and S_2 increases to the peak inductor current after which it decreases at a rate determined by the input inductor. The peak-to-peak inductor current ripple can be determined from

$$\Delta I_{\mathrm{L1}} = \frac{|D-0.5|\cdot V_{\mathrm{DC}}}{L_1 f}, \tag{3.1}$$

where f is the converter switching frequency. Diodes D_1 and D_4 are conducting and the diode peak current is the peak inductor current divided by the transformer turns ratio. The transformer secondary voltage during this mode is

$$\frac{nV_{\mathrm{DC}}}{2(1-D)}, \tag{3.2}$$

where the turns ratio n is defined as $N_{\mathrm{sec}}/N_{\mathrm{pri}}$.

Mode 3

Transistors S_3 and S_4 are turned on while S_1 and S_2 are still conducting. Operation is otherwise analogous to mode 1. Mode 4 is identical to mode 2, but with the opposite switching elements.

3.1.2 Secondary rectifier voltage ringing

The voltage ringing across the transformer leakage inductance is present also in the current-fed topologies and the leakage inductance voltage is a function of the leakage inductance and the current *di*/*dt*. Resonant topologies such as ZVS boost and resonant push-pull have inherently lower voltage overshoots due to a reduced *di*/*dt*, while the hard switched topologies experience large transient voltage spikes during the transformer current transitions. Figure 3.3 presents the full-bridge boost output rectifier diode voltage stresses during the switching states.

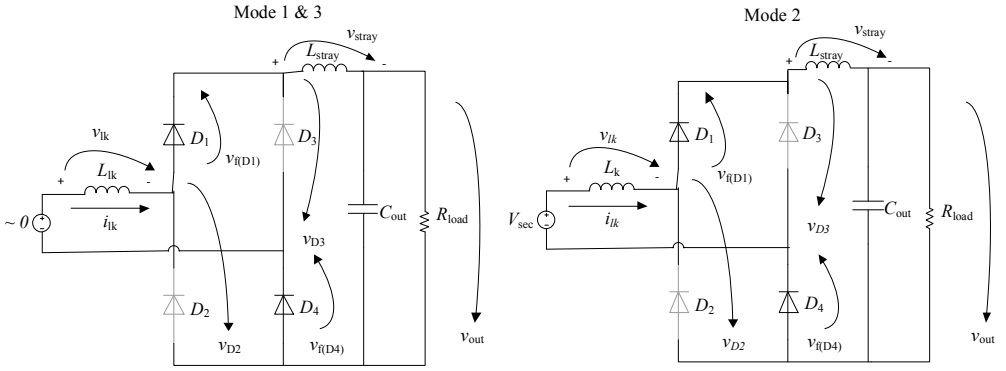


Figure 3.3: Output rectifier diode conduction states and the corresponding voltages for the diodes when using a diode bridge.

During modes 1 and 3 the leakage inductance current is ringing and the leakage inductance voltage is clamped to the output capacitor voltage alternatively via D_1-D_4 or D_2-D_3. The voltage across the rectifiers is ringing, but is limited in the amplitude and decreasing towards half of the output voltage.

In mode 2, voltage is applied to the transformer secondary, D_1 and D_4 are conducting and a high voltage v_{lk} is generated across the leakage inductance. The sum of transformer secondary voltage and leakage inductance voltage is clamped to the secondary voltage via D_1 and D_4. The clamping current is seen as an overshoot in the diode current. When the leakage inductance current has reached its maximum value, the current begins changing in the negative direction and the sign of i_{lk} and v_{lk} changes. The leakage inductance current resonates in this manner for a while until it reaches its steady state value. The voltages for the non-conducting diodes are

$$\begin{aligned} v_{D2} &= v_{out} + v_{stray} + v_{f(D1)}(t) \\ v_{D3} &= v_{out} + v_{f(D4)}(t) \end{aligned} \tag{3.3}$$

The maximum cathode-anode voltage for a non-conductive rectifier diode depends on the impedance of the loop between the diode cathode and the output capacitor and on the forward voltage, including the forward recovery voltage, of a conducting diode. In the hard switched and phase-shifted full-bridge the output inductor creates high impedance on the clamping loop. Thus, in order to limit the rectifier diode overshoot a separate clamping circuit needs to be implemented before the output inductor.

Figure 3.4 describes the diode voltage stresses when using a voltage doubler secondary.

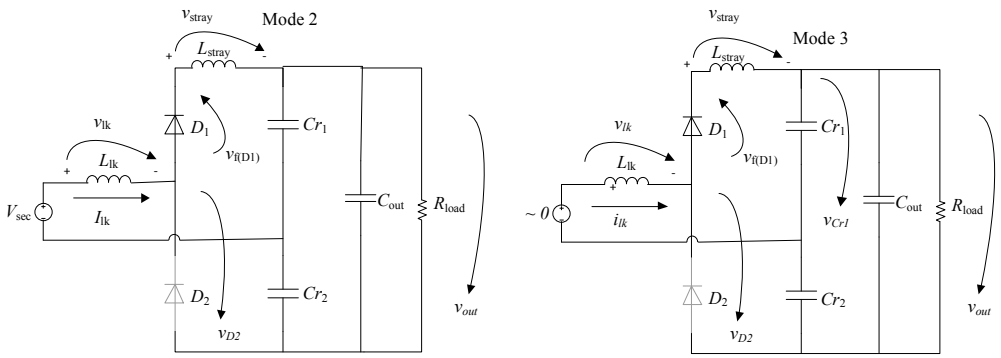


Figure 3.4: Output rectifier diode conduction states and the corresponding voltages for the diodes when using a voltage doubler.

At the beginning of mode 2, voltage is applied to the transformer secondary, the leakage inductance current is changing in the positive direction and a high voltage is generated across the leakage inductance. When the leakage inductance current has reached its maximum value, the current begins changing in the negative direction and the sign of voltage v_{lk} changes. The leakage inductance current and voltage oscillate in this manner until the steady state value is reached. The voltage across diode D_2 during mode 2 is

$$v_{D2}(t) = v_{out} + v_{stray} + v_{f(D1)}(t) \tag{3.4}$$

The maximum voltage across a non-conducting diode is ideally the output voltage plus the voltage drop of a conducting diode, but in practice, there is a small voltage overshoot caused by the stray inductance L_{stray}. During mode 3, the leakage inductance current is resonating and diodes D_1 and D_2 are conducting alternately. The maximum voltage across a non-conduction diode is limited as in the previous mode. The oscillating voltage across D_1 is decreasing towards $v_{Cr1}(t)$ and the voltage across D_2 towards V_{out}-$v_{Cr1}(t)$.

If the output capacitor is large enough to keep the output voltage constant during modes 1 and 3, voltage $v_{Cr1}(t)$ is nearly equal to $V_{Cr1}(t_2)$, which is the voltage in which capacitor C_{r1} is charged during mode 2. In addition, $V_{Cr1}(t_2)$ is also the sum of the transformer secondary voltage and the voltage across the leakage inductance while the secondary current is varying at a certain *di/dt*:

$$V_{Cr1}(t_2) = V_{sec}(t_2) + \left|V_{leak}(t_2)\right| . \tag{3.5}$$

Mode 1 is otherwise similar to mode 3, but with the difference that

$$\begin{aligned} V_{Cr1} &= V_{out} - V_{Cr2} \\ V_{Cr2} &= V_{sec} + \left|V_{leak}\right| \end{aligned} \tag{3.6}$$

3.1.3 Full-bridge boost clamping circuits

The purpose of clamping and assisting commutating circuits in this topology is to circulate and recover the energy stored in the isolating transformer leakage inductance and to limit the inductive voltage transients caused by changes in the current direction. The effect of the leakage inductance can be seen in Figure 3.5. During each boost period, the input current rises with the ramp V_{DC}/L_1 and the transformer current is the magnetizing current through shorted magnetizing inductance and leakage inductance. After the first boost period seen in the figure, transistors S_3 and S_4 are turned on and the transformer primary current is decreasing with the ramp $(V_{DC}$-$V_{sec}/n)/(L_1+L_{lk})$. In this case, as the transistors go into avalanche breakdown due to the large induced voltage across the leakage inductance, the rate of change of the current is determined by the MOSFET breakdown voltage and the circuit inductances.

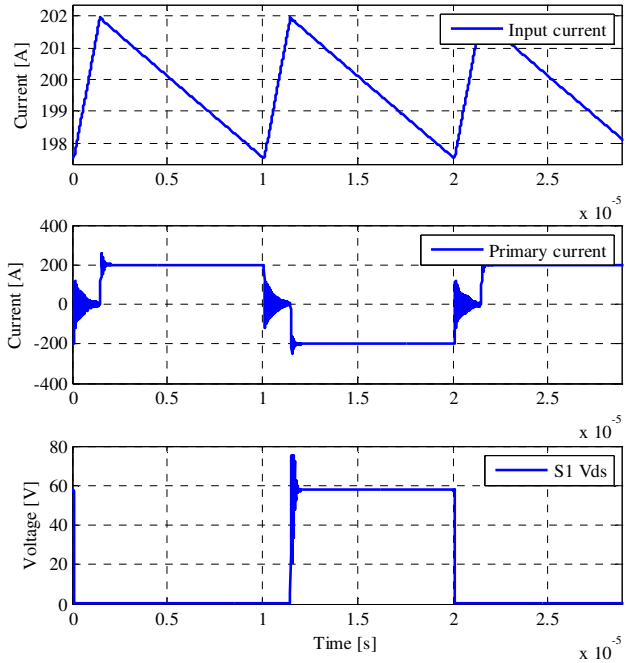


Figure 3.5: Simulation of primary voltage transients induced by the changes in the transformer current direction. There is also a visible overshoot in the primary current, the amplitude of which is dependent on the damping factor of the RLC circuit formed by primary and secondary resistances, inductances and capacitances. The input current is not significantly affected by the primary current overshoot.

The voltage transients during switching cannot be totally avoided as there will always be undesired inductances in the circuit. However, the leakage energy circulation and the voltage transients can be greatly reduced using winding interleaving, which reduces the transformer leakage inductance and thus shortens the current commutation times. If a clamp circuit is omitted, this circulating energy will be dissipated in the MOSFETs, which need to be fully avalanche rated. Avalanche-based voltage clamping can be used as long as the dissipated energy does not exceed the specified maximum avalanche energy in either a single pulse or repetitive pulsing. The MOSFET can fail if the avalanche breakdown raises the junction temperature beyond the maximum junction temperature rating.

As described by Yakushev et al. (1999), the bridge switches can be switched under zero voltage switching provided that the leakage inductance is large enough. When the clamp switch is turned off as the current direction is from drain to source and the clamp capacitor is discharged, the body diodes of the non-conducting bridge switches are forced to conduct and the voltage across these switches drops to zero. As the boost period following the snubber switch turn-off takes place, all the bridge switches are operated under zero voltage.

In the study by Park et al. (2004) the resonance period between the leakage inductance and the clamp capacitance was dimensioned in a way that the clamping transistor was turned off under zero current (Figure 3.6). Zero voltage switching is inherently present in the active clamp, as the clamping transistor body diode is always conducting before the transistor is turned on. If the

clamp branch has low inductance, the transistor drain-source voltage and thus the clamp capacitor voltage are limited to their maximum value, which is a function of leakage and magnetizing inductance and the output power level, as demonstrated by Yakushev et al. (1999).

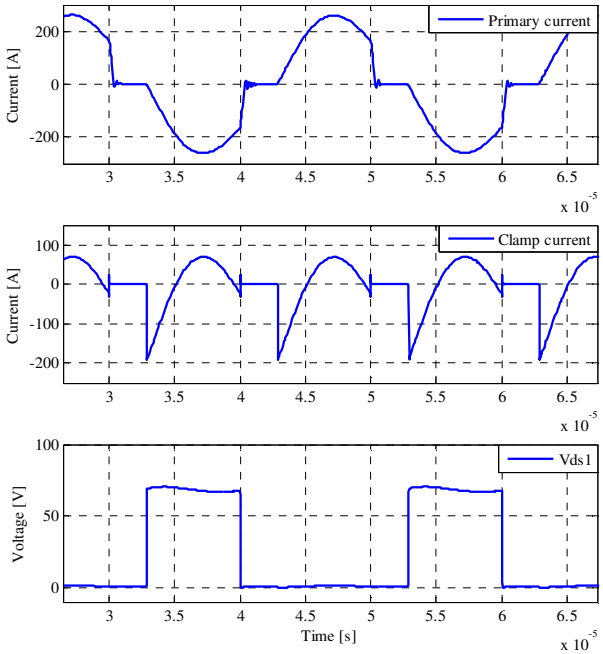


Figure 3.6: Dimensioning of the active snubber to achieve zero voltage and near zero current switching for the clamping transistor (simulated example).

Compared to the conventional scheme presented by Yakushev et al. (1999), the switching losses of the clamping transistor are greatly reduced when tuning the clamp to zero current switching. This overcomes the slightly increased conduction losses caused by larger peak currents. Also the bridge transistors experience smaller turn-off losses due to a reduced drain-source voltage when they are turned off.

In passive clamp solutions such as those described by Mohr and Fuchs (2006), the active clamp transistor is replaced with a diode and the clamp capacitor is discharged through a resistor (Figure 3.7). The drawback of this solution is that besides diode losses and capacitor ESR losses, the energy stored in the clamp capacitor is dissipated in the resistor, which means that a majority of the switching losses are simply transferred from the bridge transistor to the clamping circuit. Active clamping is also mentioned by Mohr and Fuchs (2006), but also the active clamping circuit has its own efficiency, and some energy is lost.

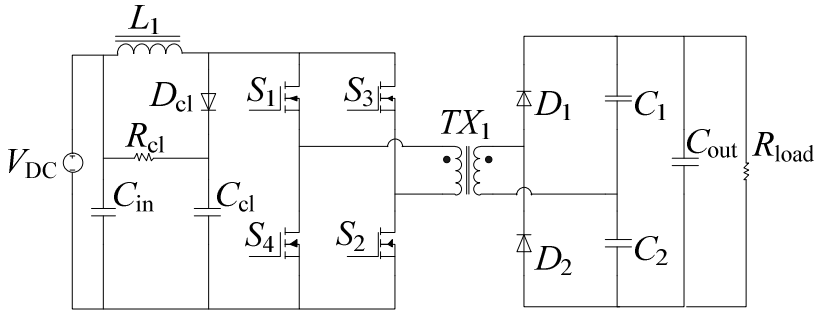


Figure 3.7: Passive clamped current-fed full-bridge topology, where the leakage energy is dissipated in a resistor.

Another form of passive clamping is the utilization of the transformer leakage inductance and parasitic capacitance in order to achieve zero current switching and voltage transient limiting, as seen in Figure 3.8 (Chen et al., 2008).

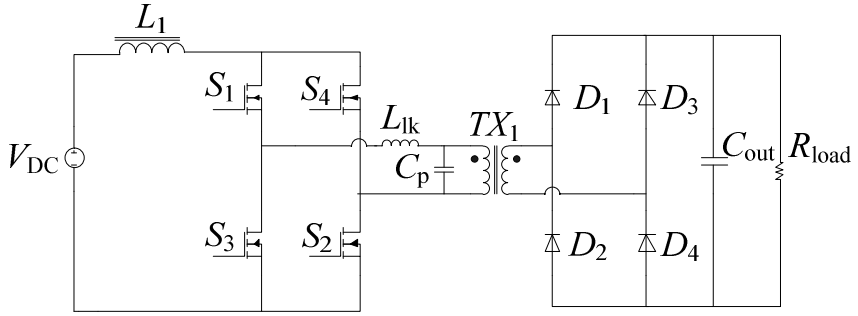


Figure 3.8: Full-bridge boost DC-DC converter with a resonance tank utilizing the transformer leakage inductance and parasitic capacitance.

Using the proposed approach, the zero current switching conditions are quite easily met with low operating power levels and voltages. When considering a SOFC application with the operating conditions mentioned in the introduction, determining the values of leakage inductance and parasitic capacitance required for the ZCS may become cumbersome or impossible. The fine tuning of transformer parasitic components by modifying the transformer structure is not an easy task in practice especially if the required leakage inductance or parasitic capacitance is very large or small. Therefore, external resonance components would be needed. These components will experience high current peaks due to the resonant process, which will result in additional power losses, reliability issues, and costs.

An approach that combines active and passive clamping is presented by Zhu (2006). The proposed converter consists of a passive clamp in the primary circuit and a controlled rectifier bridge in the secondary circuit (Figure 3.9).

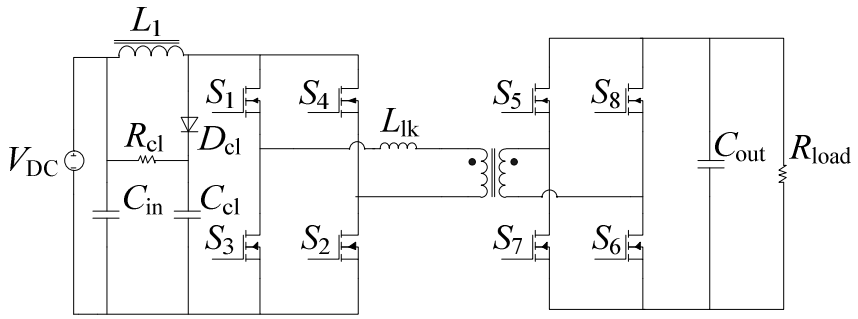


Figure 3.9: Full-bridge boost DC-DC converter employing a passive clamp at the primary circuit and an active rectifier bridge at the secondary.

The advantage of the proposed approach is that the current difference between the boost inductor and the transformer leakage inductance remains much smaller than in the previous snubber solutions. Thus, the energy pushed back into the snubber circuit is smaller, resulting in smaller component stresses. The difference current is minimized by presetting the transformer current through a resonant tank on the secondary side during the boost mode. The secondary transistors are also used to accelerate the current commutation between the boost and energy transfer modes. All of the secondary transistors achieve zero voltage switching. The solution also enables bi-directional operation, which extends the application areas of the converters of this kind. The feasibility of the proposed approach in uni-directional applications, such as in fuel cell and solar power conversion, might be questioned from the viewpoint of economic efficiency. The question is whether the additional circuit complexity and component cost, especially because of the active rectifier bridge at the secondary, pays off in terms of increased efficiency and savings during the power conversion unit life cycle.

3.1.4 Advantages and disadvantages of the full-bridge boost converter

+ Low primary switch voltage rating allowing the usage of low $R_{ds(on)}$ transistors.

+ Low input inductor energy storage requirement, as demonstrated in section 5.2.

+ The secondary rectifier voltage is clamped and there is no need for snubbers.

+ There is a small voltage drop from the transformer secondary to the converter output, and hence the transformer turns ratio does not need to be increased in order to compensate the voltage drop.

+ No external snubber circuits are required if the transformer leakage inductance is small enough.

- Small leakage inductance is required in order to avoid the dissipation of excessive avalanche energy in the primary transistors. Leakage inductance can be reduced by transformer winding interleaving and as an additional advantage the transformer AC resistances are also reduced.

- A relatively high turns ratio is required especially when using a diode bridge output.

3.2 ZVS boost

Figure 3.10 presents the schematics of a ZVS boost converter which was introduced by Hyungoon et al. (2010).

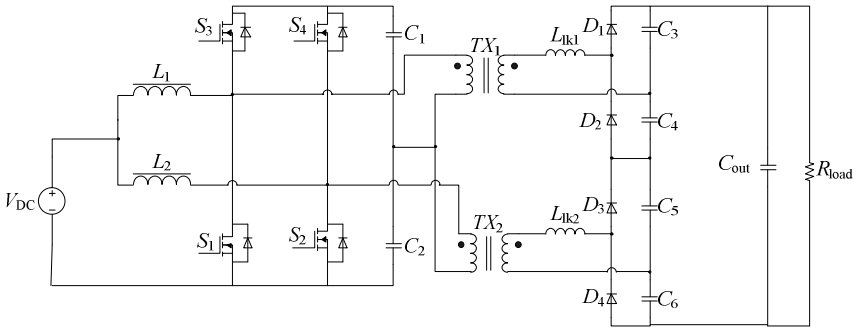


Figure 3.10: Schematics of the ZVS boost converter.

Capacitors C_{c1} and C_{c2} are dimensioned to be large DC capacitors, while C_{r1} and C_{r2} are smaller resonance capacitors and their capacitances depend on the desired resonant frequency.

3.2.1 Operating principle of the ZVS boost converter

Figure 3.11 presents the simplified operating waveforms for the ZVS boost converter. The waveforms are drawn for a case where all of the output rectifier diodes are operating under ZCS and transistors S_1 and S_2 are hard switched, i.e. not operated under ZVS. As demonstrated in section 3.2.2, it may be difficult to achieve ZVS operating conditions for transistors S_1 and S_2. In the study by Hyungoon et al. (2010) the output rectifiers were hard switched and all the primary transistors soft switched.

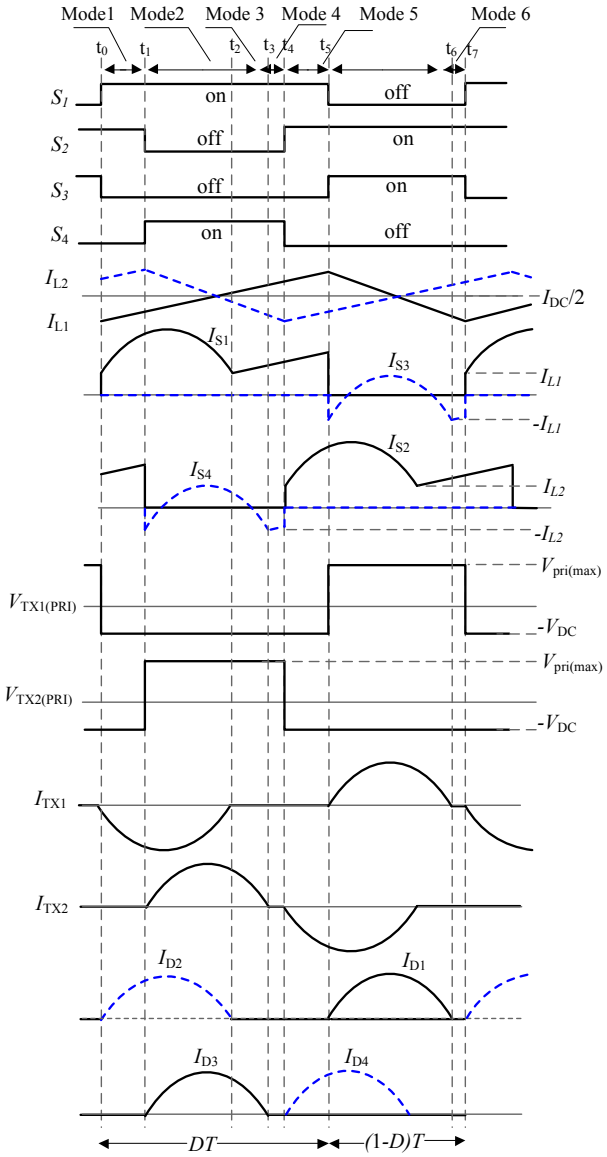


Figure 3.11: Simplified operating waveforms for a ZVS boost converter with $D > 0.50$ while operating the secondary rectifiers under ZCS.

Mode 1

Transistors S_1 and S_2 are both conducting and the voltage at both transformer primaries is negative input voltage. Resonance between leakage inductance L_{lk1} and capacitors C_3+C_4 takes place and the resonance current is flowing through transformer TX_1 and diode D_2. The reflected resonance current is flowing through S_1 with an offset of I_{L1} while S_2 is carrying current I_{L2}.

There is only magnetizing current flowing through the transformer TX_2 primary during mode 1 since diode D_3 is reverse biased until instant t_1.

Mode 2

Transistor S_2 is closed while S_1 is still conducting. The voltage at TX_2 rises to $V_{\text{pri(max)}}$, which is defined as

$$\begin{aligned} V_{\text{pri(max)}} &= L_2 \frac{\Delta I_{\text{L}_2}}{(1-D)T} = \frac{D}{1-D} V_{\text{DC}} \\ V_{\text{S2(max)}} &= \frac{D}{1-D} V_{\text{DC}} + \frac{V_{\text{out}}(1-D)}{2n} \end{aligned} \tag{3.7}$$

where D is the primary duty cycle and n is the turns ratio defined as $N_{\text{sec}}/N_{\text{pri.}}$ A resonant current is flowing through TX_2 and D_3 with a resonance period determined by the voltage difference between TX_2 secondary and resonance capacitors C_5 and C_6. Transistor S_4 is carrying the current of TX_2 with an offset of I_{L2}.

Mode 3

Mode 3 starts as the reflected resonance current through transformer TX_1 decreases to the magnetizing current value and diode D_2 is turned off at zero current. The current through transistor S_1 is the inductor L_1 current rising at the rate V_{DC}/L_1. The peak inductor current ripple between t_0 and t_5 can be calculated from

$$\Delta I_{\text{L}} = \frac{D \cdot V_{\text{DC}}}{L \cdot f}. \tag{3.8}$$

Mode 4

Mode 4 starts as the reflected resonance current through transformer TX_2 decreases to the magnetizing current value and diode D_3 is turned off at zero current. The current through S_4 is limited to current I_{L2}. Mode 4 ends when transistor S_2 is turned on.

Modes 5, 6, 7 and 8 are analogous to the previous modes, but with the opposite set of transistors and diodes.

3.2.2 Determination of the ZVS range

According to Hyungoon et al. (2010), transistors S_3 and S_4 are typically switched on with zero voltage over the entire load range. To ensure ZVS for transistor S_1, the following condition should to be satisfied:

$$\frac{1}{2} L_{\text{lk1}} I_{\text{L}_{\text{lk1}}(\text{max})}{}^2 - \frac{1}{2} L_1 I_{\text{L}_1(\text{min})}{}^2 > C_{\text{oss}} \left(\frac{V_{\text{DC}}}{1-D} \right)^2, \tag{3.9}$$

where

$$I_{\mathrm{L_{lk1}(max)}} = \frac{D\left(2nV_{\mathrm{DC}} - V_{\mathrm{out}} + DV_{\mathrm{out}}\right)}{2nL_{\mathrm{lk1}}f}$$
$$I_{\mathrm{L_1(min)}} = \frac{1}{2}\left(\frac{P_{\mathrm{o}}}{V_{\mathrm{DC}}} - \frac{DV_{\mathrm{DC}}}{L_1 f}\right) \tag{3.10}$$

and C_{oss} is equal to (C_{ds} + C_{gd}). The ZVS criteria for transistor S_2 are determined in the same way with the corresponding leakage inductance L_{lk2} and inductance L_2. Figure 3.12 presents the ZVS range for a range of input inductance and primary leakage inductance values when operating under the given operating conditions.

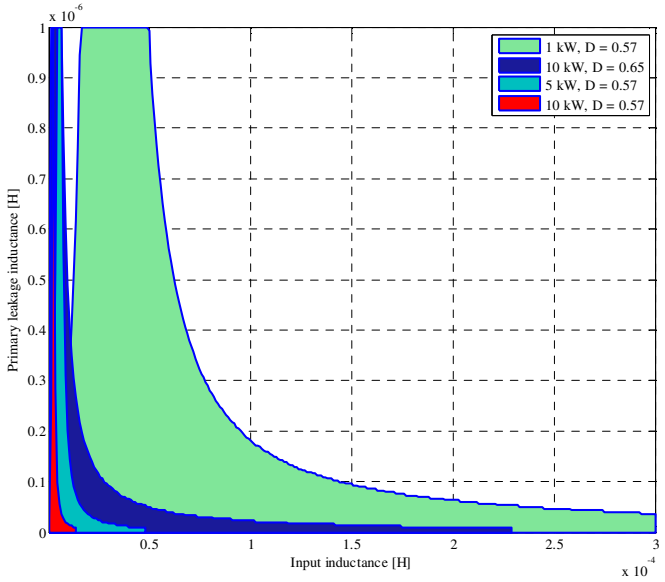


Figure 3.12: ZVS range under the following operating conditions: V_{in} = 50 V, V_{out} = 660 V, n = 3, f = 50 kHz and C_{oss} = 977 pF.

The ZVS range can be widened by increasing the duty cycle and/or reducing the transformer turns ratio. With small duty cycles and high output powers the ZVS range can be very narrow, as seen from Figure 3.12. High power or high voltage MOSFETs typically have a larger C_{oss} than their low voltage or low power counterparts, and consequently, when scaling up in converter size the ZVS area is limited. In order to achieve ZVS in the demonstrated 10 kW case the input inductor should be very small which is not practically feasible since the inductor loss caused by large current ripple is very likely to overshadow the reduction in transistor turn-on losses in low voltage applications. The requirement of a small leakage inductance is not a problem if winding interleaving can be used and by minimizing the leakage inductance with interleaving the proximity losses in the windings are also reduced.

3.2.3 Tolerance of switching asymmetries

Even a small variation in duty cycles can cause a large asymmetry between the inductor currents depending on the resistances on each inductor current loop. If there is a duty cycle difference between S_1 and S_2, there is a difference between the volt-seconds applied to inductors L_1 and L_2. Since the transformers share a common primary and secondary, the transformer RMS voltages and current must be nearly equal despite the switching asymmetry. The difference between the transformer primary currents flows through capacitors C_1 and C_2 increasing their current stress. The switching asymmetry has the greatest effect on the currents of inductors L_1 and L_2 as well as transistors S_1 and S_2. Table 3.1 presents the simulated currents for the primary components with various duty cycle differences where the S_1 duty is 0.57 and the S_2 duty is increased.

Table 3.1: Effects of duty cycle asymmetry on primary currents in the ZVS boost topology.

ΔD	L_1/L_2	S_1/S_2	S_3/S_4	TX_1/TX_2	C_1/C_2
0	100 A/100 A	141 A/141 A	37 A/37 A	107 A/107 A	53 A/63 A
0.001	97 A/103 A	139 A/143 A	37 A/37 A	107 A/107 A	53 A/63 A
0.01	69 A/132 A	115 A/167 A	45 A/40 A	105 A/105 A	60 A/71 A

A solution suggested by Hyungoon et al. (2010) for the practically inevitable volt-second balance problem was a modification to the primary capacitor configuration (Figure 3.13). The common clamp capacitor C_1 has now been split into two separate clamp capacitors, one for each switching leg.

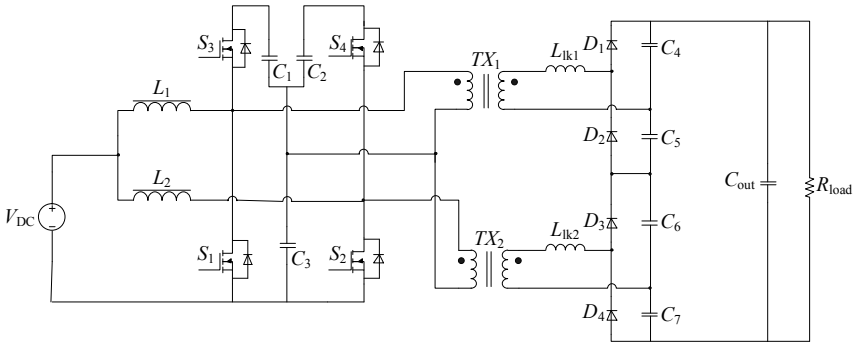


Figure 3.13: Re-arranged primary clamp capacitors to overcome the volt-second balance problem.

Table 3.2 presents the modified circuit primary currents corresponding to the duty cycle variations in Table 3.1. It can be seen that the volt-second imbalance is corrected by the separate clamp capacitors.

Table 3.2: Effects of duty cycle asymmetry on primary currents in the modified ZVS boost topology.

ΔD	L_1/L_2	S_1/S_2	S_3/S_4	TX_1/TX_2	$C_1/C_2/C_3$
0	100 A/100 A	141 A/141 A	37 A/37 A	107 A/107 A	37 A/37 A/63 A
0.001	100 A/100 A	141 A/141 A	37 A/37 A	107 A/107 A	37 A/37 A/63 A
0.01	99 A/101 A	140 A/141 A	36 A/36 A	105 A/105 A	36 A/36 A/64 A

3.2.4 Secondary rectifier voltages

As in other current-fed topologies presented in this thesis, the amplitude of the rectifier voltage is also inherently limited in the ZVS boost converter, and additionally, it is possible to eliminate the rectifier voltage ringing almost completely. If the unmodified converter is operated as in Figure 3.11, the voltages for rectifiers D_1 and D_2 (similar analysis applies also for D_3 and D_4) are as described in Figure 3.14.

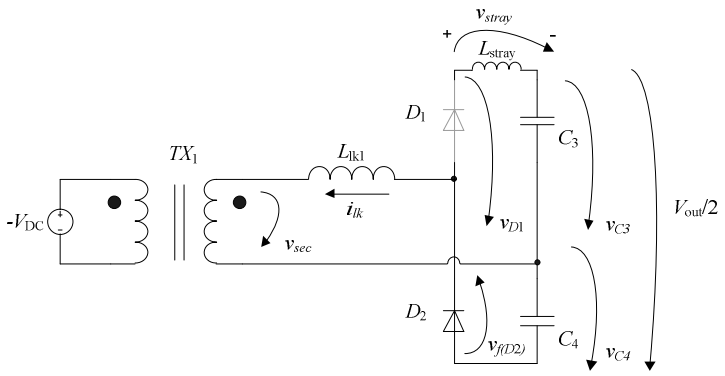


Figure 3.14: Definitions of the circuit voltages during the operating modes.

After instant t_0 (Figure 3.11), diode D_2 starts conducting, the leakage inductance L_{lk1} current is changing in the negative direction, capacitor C_3 is discharging and capacitor C_4 is charging. The voltage across D_1 during modes 1 and 2 is

$$\begin{aligned} v_{D1}(t) &= v_{C3}(t) + v_{C4}(t) + v_{f(D2)}(t) + v_{stray}(t) \\ V_{C3}(t_0) &= \frac{V_{out}}{2} D - \frac{I_{load}}{\frac{2}{T}(C_3 + C_4)} \\ V_{C4}(t_0) &= \frac{V_{out}}{2} - V_{C3}(t_0) \end{aligned} \quad , \tag{3.11}$$

$V_{C3}(t_0)$ and $V_{C4}(t_0)$ are the initial voltages of C_3 and C_4 where they have charged or discharged, respectively, before the beginning of mode 1.

During modes 3-5 (time instants t_2-t_5), only small resonance currents flow through the rectifiers and the diode voltages oscillate while the rectifiers are conducting alternatively. The voltage $v_{sec}(t)$ is negative and the voltage $v_{C3}(t)$ is positive, so the voltages for D_1 and D_2 are now

$$\begin{aligned} v_{D1}(t) &= \left|v_{sec}(t)\right| + v_{C3}(t) + v_{stray}(t) \\ v_{D2}(t) &= \frac{V_{out}}{2} - v_{D1}(t) \end{aligned} \quad . \tag{3.12}$$

V_{C3} is the voltage where C_3 has been discharged during modes 1 and 2. Since the voltage of capacitor C_3 has decreased during modes 1 and 2, the maximum voltage across D_1 is smaller in modes 3 and 4. However, the voltage oscillation across the rectifiers causes additional switching losses. Figure 3.15 presents the simulated rectifier voltages in the cases described above.

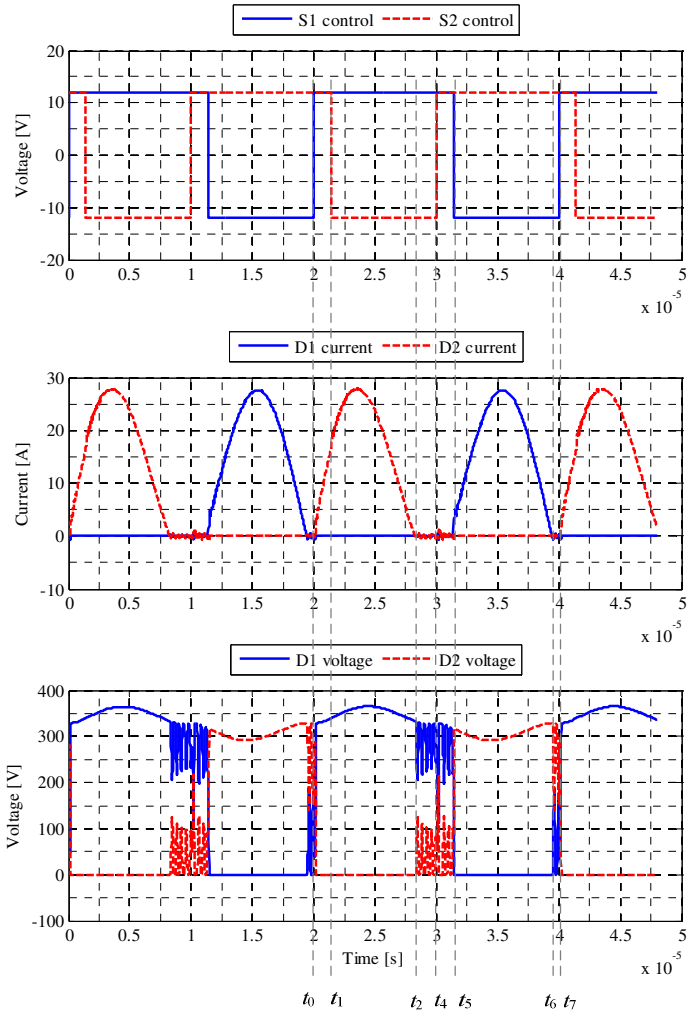


Figure 3.15: Simulated currents and voltages of D_1 and D_2 in a 10 kW ZVS boost converter with V_{out} = 654 V. The time instants and the corresponding operating modes are identical with Figure 3.11.

There are no modes 3 and 4 or voltage oscillation across the secondary rectifiers if the resonance period of the leakage inductance current is long enough for the currents through D_1 and D_2 not to be cut off until instants t_7 and t_4, respectively, and if the leakage inductance is large enough to support the D_2 current until instant t_5. The smaller the leakage inductance is in comparison to the voltage doubler capacitors while keeping the resonant period length constant, the smaller the rectifier voltage oscillations are during modes 3 and 4. The measured voltage waveform across one diode in this case can be seen in Figure 3.24.

3.2.5 Advantages and disadvantages of the ZVS boost converter

+ A very small turns ratio and half the total volt-ampere rating for a single transformer.

+ Possibility to operate all primary transistors under ZVS, although the ZVS range for transistors S_1 and S_2 can be very narrow.

+ Possibility to operate all secondary rectifiers under ZCS.

+ Very clean secondary rectifier voltage waveforms and small voltage stresses for a single rectifier (Figure 3.24).

+ Wide duty cycle range $0 < D < 1$.

+ Very tolerant for switching asymmetry induced flux imbalances due to the clamp capacitors and the voltage doubler secondary.

- High voltage rating for the primary transistors, which limits the selection of low $R_{ds(on)}$ devices (3.7).

- Large current ripple for a single input inductor (3.8).

- High current stresses in the primary capacitors.

- High diode conduction losses and total costs due to large number of rectifiers.

- The unmodified topology has very small tolerance for switching asymmetries.

3.3 Resonant push-pull boost

The resonant push-pull boost topology was originally presented by Kwon et al. (2009) with a 1.5 kW prototype. The scalability of this converter topology was investigated by the author of this thesis and a 10 kW prototype was built and successfully integrated into a SOFC demonstration unit designed and operated by the VTT Technical Research Centre of Finland (Halinen et al., 2011). The schematic of the resonant push-pull converter can be seen in Figure 3.16.

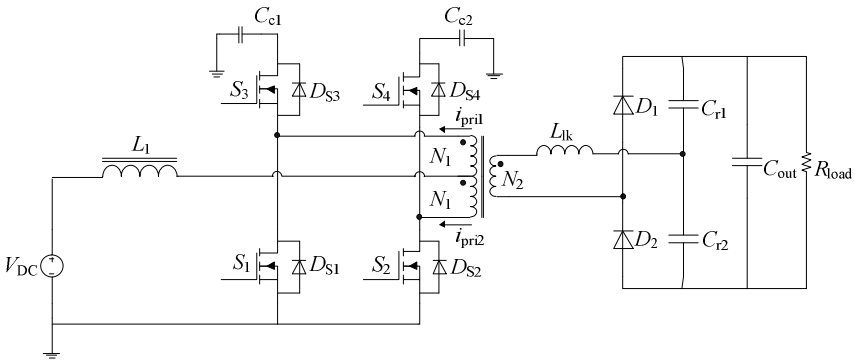


Figure 3.16: Schematic of the resonant push-pull converter. The positive directions for the primary currents i_{pri} and i_{pri2} are marked with arrows.

Capacitors C_{c1} and C_{c2} are dimensioned to be large DC capacitors, while C_{r1} and C_{r2} are smaller resonance capacitors and their capacitances depend on the desired resonant frequency (3.16).

3.3.1 Operating principle of the resonant push-pull boost

The theoretical converter waveforms and operating modes for $D > 0.5$ can be seen in Figure 3.17.

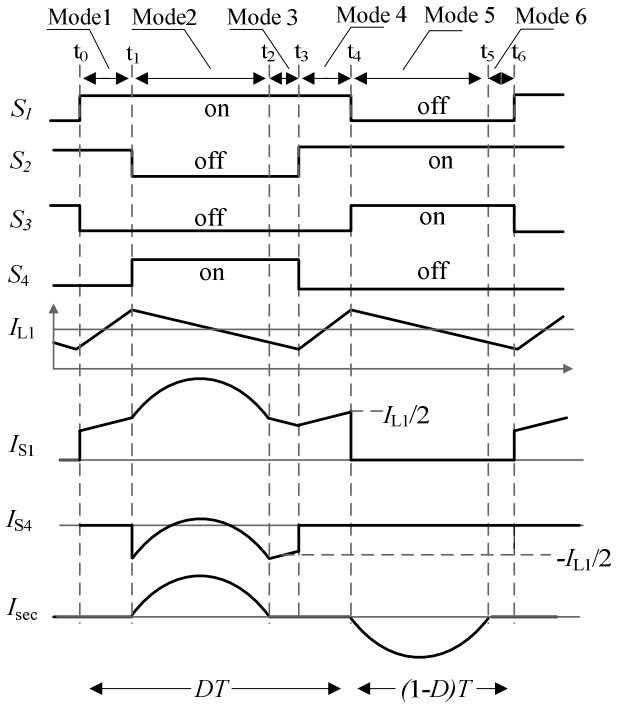


Figure 3.17: Theoretical operation modes for resonant push-pull converter with $D > 0.5$.

Mode 1

At t_0, transistor S_1 is turned on while S_2 is still conducting. The input inductor current begins to rise with a rate determined by V_{DC}/L_1, and the current is divided equally between S_1 and S_2. The voltage across all the windings is zero, the rectifier diodes are reverse biased, and no current is transferred into the secondary.

Mode 2

At t_1, transistor S_2 is turned off while S_1 is still conducting. The input inductor current begins to decrease with rate determined by

$$\frac{0.5V_{\text{pri(max)}} - V_{\text{DC}}}{L_1}, \tag{3.13}$$

where $V_{\text{pri(max)}}$ is the maximum voltage seen by all the primary components and it can be calculated from

$$V_{\text{pri(max)}} = \frac{V_{\text{DC}}}{1-D}. \tag{3.14}$$

The current starts to flow in the transformer secondary as diode D_1 forward biases. The transformer secondary current can then be expressed as

$$i_{\text{sec}}(t) = \frac{nV_{\text{pri(max)}} - V_{\text{Cr}}}{Z_{\text{r}}} \sin \omega_{\text{r}}(t - t_1), \tag{3.15}$$

where V_{Cr1} is the initial resonant capacitor voltage, Z_r is the characteristic resonant impedance and ω_r is the resonant frequency. The damping caused by the circuit resistances which reduces the resonance amplitude is not accounted for in (3.15). The transformer turns ratio n is $(N_2)/(2N_1)$. The characteristic resonant impedance and frequency is obtained from

$$\omega_{\text{r}} = \frac{1}{\sqrt{L_{\text{lk}} C_{\text{r}}}} \quad Z_{\text{r}} = \sqrt{\frac{L_{\text{lk}}}{C_{\text{r}}}} \quad C_{\text{r}} = C_{\text{r1}} + C_{\text{r2}} \tag{3.16}$$

The initial resonant capacitor voltage $V_{C\ \text{r1}}$ can be derived using the maximum resonant capacitor voltage ripple assuming that the converter is symmetrically operated and the output voltage is equally divided between the resonant capacitors.

$$V_{\text{Cr}} = \frac{V_{\text{out}}}{2} - \Delta V_{\text{Cr}}, \tag{3.17}$$

where ΔV_{Cr} is the maximum capacitor voltage deviation from the average voltage defined as

$$\Delta V_{\mathrm{Cr}} = \frac{I_{\mathrm{load}}}{\frac{2}{T_{\mathrm{s}}}\left(C_{\mathrm{r1}} + C_{\mathrm{r2}}\right)}. \tag{3.18}$$

Transistor S_4 is turned on shortly after instant t_1 with zero voltage switching, as the transistor body diode is conducting. The sum of magnetomotive forces in the transformer is zero

$$N_1 i_{\mathrm{pri1}}(t) - N_1 i_{\mathrm{pri2}}(t) - N_2 i_{\mathrm{sec}}(t) = 0 \tag{3.19}$$

and the input current is the sum of the primary currents. Therefore, the transistor currents in mode 2 are

$$\begin{aligned} i_{\mathrm{S1}}(t) &= \frac{i_{\mathrm{L1}}(t)}{2} + n i_{\mathrm{sec}}(t) \\ i_{S4}(t) &= -\frac{i_{\mathrm{L1}}(t)}{2} + n i_{\mathrm{sec}}(t) \end{aligned}. \tag{3.20}$$

Mode 3

In this mode the secondary diodes are switched off with zero current, which practically eliminates the reverse recovery effects. The input inductor current is divided equally between transistors S_1 and S_4 so that

$$i_{\mathrm{S1}}(t) = \frac{i_{\mathrm{L1}}}{2} \quad i_{\mathrm{S4}}(t) = -\frac{i_{\mathrm{L1}}}{2} \tag{3.21}$$

Mode 3 does not occur if the secondary current does not become zero before t_3. In that case, the secondary current is cut off in mode 2 at t_3 and the current decreases at the rate (A/µs)

$$\frac{di_{\mathrm{sec}}(t)}{dt} = \frac{0.5V_{\mathrm{out}} + \Delta V_{\mathrm{Cr}}}{L_{\mathrm{lk}}} \cdot 10^{-6}. \tag{3.22}$$

This rate of change in current determines the maximum diode reverse recovery current and recovery time if operating the converter without mode 3. Operation in modes 4-6 is similar as in modes 1-3.

3.3.2 Scalability issues in the resonant push-pull converter

The scalability issues of the resonant push-pull converter have been discussed by Väisänen et al. (2011). The center-tapped transformer results inevitably in higher winding losses if the number of primary-secondary intersections is kept the same as in a two winding transformer (Figure 3.18). The AC to DC resistance ratios are calculated based on the principles introduced in the study by Vandelac and Ziogas (1988).

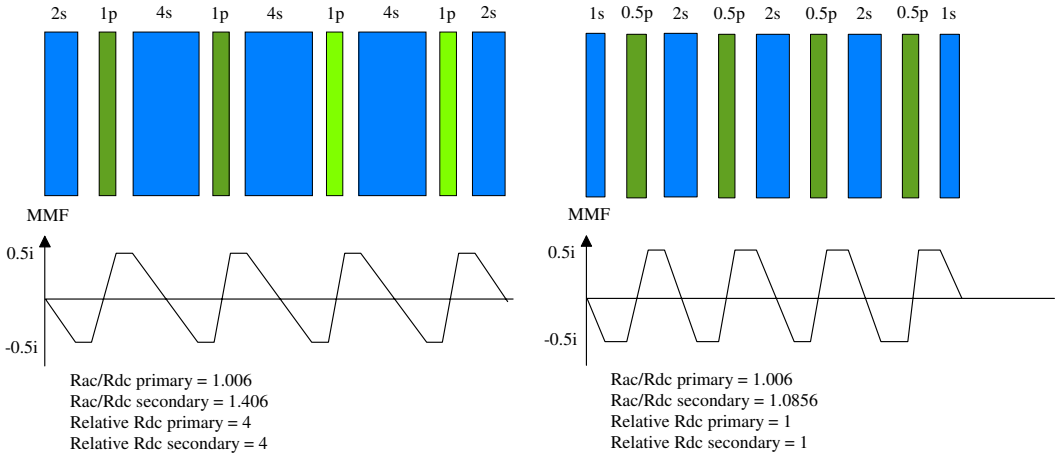


Figure 3.18: Calculated resistance ratios in transformers for resonant push-pull (a) and full-bridge boost with a voltage doubler (b) interleaved with eight intersections. Both transformers operate with a winding thickness of one skin depth at 50 kHz and a turns ratio of 1:3.

For the same number of primary-secondary intersections the primary winding in the two winding transformer can be split into parallel turns while maintaining a smaller number of secondary turns. This results in lower DC resistances and AC to DC resistance ratios than in the resonant push-pull transformer and this allows more power to be transferred through a single core in the two winding transformer (Väisänen et al., 2011).

It is more preferable to operate the resonant push-pull converter with a long resonance period (with secondary rectifiers hard switched) if using fast or ultrafast secondary rectifiers and if the leakage inductance to limit diode *di/dt* is large. The decrease in diode switching losses while operating the rectifiers with zero current switching can easily be overshadowed by the increase in primary conduction and switching losses. Figure 3.19 illustrates the effect of the resonance half period length in primary clamp currents.

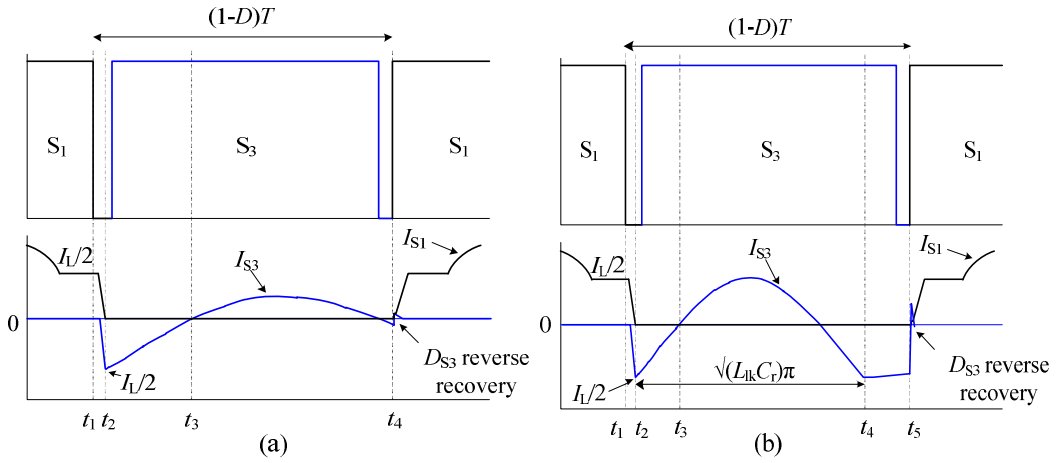


Figure 3.19: Clamp transistor currents while operating the converter with hard switched secondary rectifiers (a) and zero current switched rectifiers (b).

When operating the converter with a short resonance period the clamp RMS current is significantly increased (as can be calculated from the clamp transistor current equation given in Table 2 of Appendix A). Moreover, the high intrinsic diode forward current combined to a large *di/dt* during diode switch off at instant t_5 lead to an increased recovery current peak and switching losses, as seen from the diode section later on. Large *dv/dt* rates at diode recovery combined with a high junction temperature can subject the transistor to latchup and/or thermal failure. The current stress and losses on the snubber capacitors are also increased.

The peak reverse recovery current of the clamp transistor is seen by the lower transistor at turn-on. If operating the converter as in Figure 3.19 (b), the reverse recovery peak can be high increasing the turn-on losses in the lower transistor. This situation is illustrated in Figure 3.20, taken from a measurement with a 150 W converter.

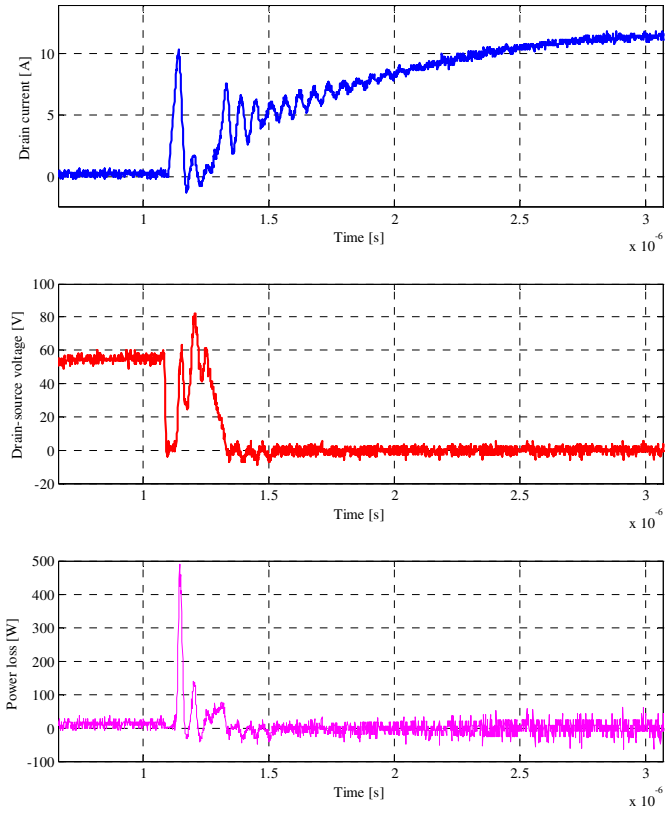


Figure 3.20: Measured turn-on waveforms for transistor S_1 in a 150 W resonant push-pull converter. The secondary rectifiers are operated under zero current switching.

As seen from Figure 3.20, most of the turn-on losses are related to the current spike caused by reverse recovery of the transistor S_3 body diode. The reverse recovery spike is seen also in Figure 3.19 (a) and Figure 4.4, but since the S_3 diode current is cut off near zero, the reverse recovery current peak is much smaller.

There is a possibility to turn on transistors S_1 and S_2 under zero voltage with $D > 0.50$ if the leakage inductance is large enough and if the current of transistors S_3 and S_4 is cut off while the body diode is not conducting. Figure 3.21 illustrates the zero-voltage switching conditions in the resonant push-pull converter.

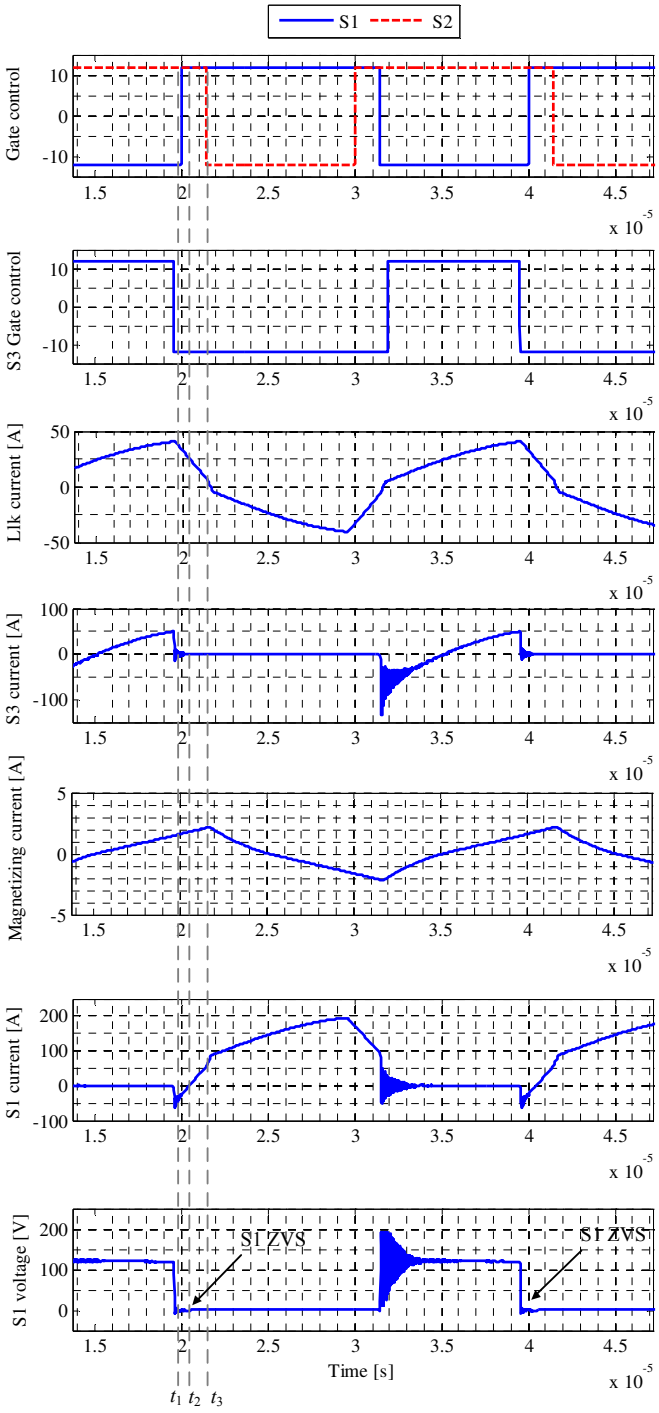


Figure 3.21: Simulated zero voltage switching waveforms for S_1 and S_2 in the resonant push-pull converter. The voltage transients at S_1 turn-off are related to parasitic inductances in the clamping circuit.

At instant t_1, clamp transistor S_3 is turned off. The body diode of S_1 starts conducting and carries the current

$$i_{D_{S1}} = ni_{L_{lk}} + i_m - i_{S3} - \frac{i_{L1}}{2}, \tag{3.23}$$

where i_{Llk} is the leakage inductance current, i_m is the transformer magnetizing current and i_{L1} is the input inductor current. The current i_{S3} is the transistor S_3 current which decreases after transistor S_3 turn-off. In low voltage and high current applications, the magnetizing current is typically small compared to the other currents. Therefore, the magnetizing current has no significant effect on the ZVS process.

Since the voltage across transistor S_1 decreases to the body diode forward voltage soon after instant t_1, transistor S_1 can be turned on with zero voltage at instant t_2. At instant t_3, transistor S_2 is turned off. After the increase, the transistor S_1 current equals $i_{L1}/2$, the transformer magnetizing current changes direction and the current through S_1 can be expressed as

$$i_{S1} = ni_{L_{lk}} - i_m + \frac{i_{L1}}{2}. \tag{3.24}$$

To achieve zero voltage switching for transistor S_1, the following conditions must be satisfied:

$$\begin{cases} i_{S3(drain)}(t_1) > 0 \\ i_{D_{S1}}(t_2) = ni_{L_{lk}} + i_m - \dfrac{i_{L1}}{2} > 0 \end{cases}. \tag{3.25}$$

A similar analysis applies for transistor S_2. The required leakage inductance can be calculated from

$$L_{lk} = V_{lk} \cdot \frac{dt}{di} = (V_{out} - V_{Cr}) \cdot \frac{t_2 - t_1}{I_{Lk} - \dfrac{I_{L1}}{2n}}, \tag{3.26}$$

where I_{Lk} is the leakage inductance current at time instant t_1 and the time interval t_2-t_1 is equal to the safe time between transistors S_1 and S_3 (or S_2 and S_4). If the resonance capacitors are made larger in size to increase V_{Cr}, the required leakage inductance to achieve ZVS is reduced. However, there is a lower limit for the leakage inductance since the voltage driving the leakage inductance current change is at least half the output voltage, even if the resonant capacitor voltage ripple (3.18) is zero.

3.3.3 Advantages and disadvantages of the resonant push-pull converter

+ A low inductor energy requirement for a certain current ripple, which makes the input inductor easily scalable. This is demonstrated in section 5.2. In theory, the converter can be operated with zero current ripple at $D = 0.50$.

+ Wide duty cycle range $0 < D < 1$.

+ The primary voltage twice as high as in the full-bridge boost for the same duty cycle, leading to a high voltage conversion ratio (3.14).

+ Possibility to operate all primary transistors under ZVS, although the ZVS of S_1 and S_2 may require a large characteristic impedance of the resonant circuit.

+ Possibility to operate all secondary rectifiers under ZCS, but not if S_1 and S_2 are zero voltage switched.

+ Very tolerant for switching asymmetry induced flux imbalances due to the clamp capacitors and voltage doubler secondary.

+ Relatively low component count.

- The center-tapped transformer increases transformer losses, unless the transformer structure is properly optimized.

- High voltage rating for the primary transistors, which limits the selection of low $R_{ds(on)}$ devices (3.14).

- High current stresses for the primary clamp capacitors.

3.4 Summary

The current-fed converters provide many advantages in low voltage, high current applications. The most important advantages are the high voltage conversion ratio, low secondary rectifier losses and tolerance for switching asymmetries. The experimental step-up current-fed converter efficiencies obtained either from publications or measurements conducted by the author are summarized in Table 3.3.

Table 3.3: Summary of experimental efficiencies for current-fed converters.

Topology	Source	Power range	Efficiency
FB boost	Park et al. (2004)	1000-5000 W	86-88.5%
	Zhu (2006)	500-3000 W	89-86%
	Nymand and Andersen (2008)	100-1500 W	92-97.9%
	Nymand et al. (2009)	100-1500 W	92-97.9%
	Nymand and Andersen (2009)	1000-10000 W	92.5-98.2%
	Author	50-150 W	95-91%
	Author	500-2000 W	90.6-92.2%
ZVS boost	Hyungoon et al. (2010)	100-1000 W	84-94.5%
	Author	50-150 W	87.5-86.5%
RPP	Kwon et al. (2009)	100-1500W	92.5-92.75%
	Author	50-150 W	92.5-92%
	Author	100-10000 W	92.5-93.6%

In the FB boost topology the efficiencies reported in the studies of Park et al. (2004) and Zhu (2006) were measured with a clamped topology, while the measurements conducted by Nymand et al. and the author of this thesis were carried out with an unclamped topology. Figure 3.22 presents the measured efficiencies for the 150 W current-fed prototypes.

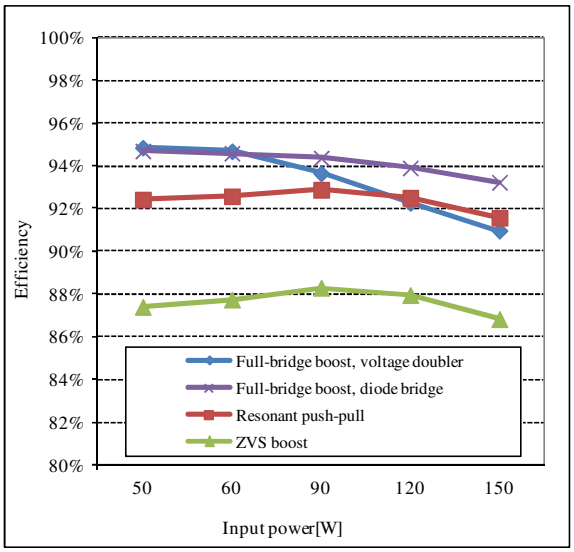


Figure 3.22: Experimental efficiencies for the 150 W current-fed prototypes.

Figure 3.22 displays the efficiency differences between the voltage doubler and diode bridge full-bridge boost converters. Since SiC diodes with a relatively large forward voltage drop were used, the voltage doubler configuration was notably less efficient, as demonstrated in section 4.4.

In the full-bridge boost measurements by the author of this thesis the transformer leakage inductance was not as small as it could have been (interleaving was performed with only two primary-secondary intersections) and the transistors did not have the lowest $R_{ds(on)}$ available for the voltage range. In general, the topology was robust in operation and there is potential for very high efficiencies, as demonstrated by Nymand et al. if the transformer leakage inductance is reduced to a minimum and the primary clamp circuit is omitted.

The reason for the lower measured efficiency in the 150 W ZVS boost prototype was that it used exactly the same components as the full-bridge boost and resonant push-pull topologies. While the transistor requirements are basically the same as in the RPP topology, the input inductor needs to be much larger whereas the secondary diodes can have a lower breakdown voltage rating, which typically increases the diode switching speed and improves the forward characteristics when maintaining the same current rating.

Figure 3.23 presents the measured efficiencies for the medium- and high-power prototypes. The RPP efficiency behavior with a variable duty cycle was calculated using the principles described in this thesis and in Väisänen et al. (2011).

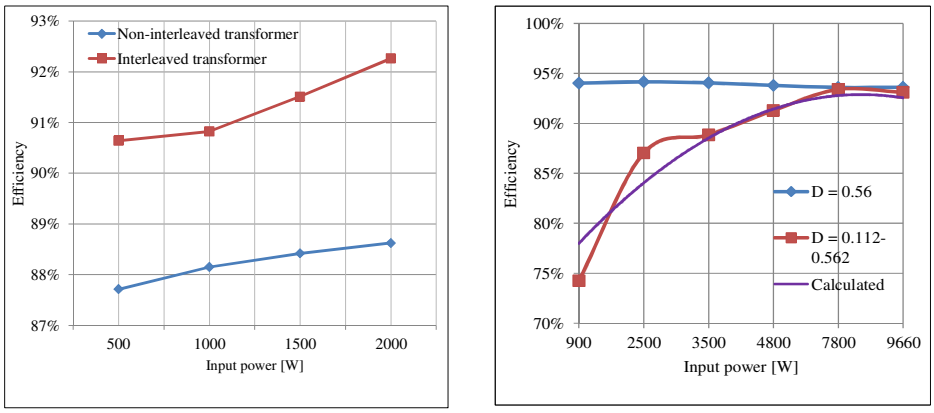


Figure 3.23: Experimental efficiencies for the full-bridge boost converter (a) and for the resonant push-pull (b).

In Figure 3.23, the full-bridge boost converter was operated with a constant duty cycle of 0.65 and the resonant push-pull with both fixed and variable duty cycles. The resonant push-pull measurement demonstrates the effect of the duty cycle in the converter efficiency. When a certain power is transferred with a small duty cycle, the losses can be much higher compared to a situation where the same power is transferred with a higher duty cycle. The duty cycle effects are discussed in the following chapters.

The resonant push-pull has higher transformer losses than the other current-fed topologies if the number of primary-secondary intersections is identical. This degraded the efficiency in the 10 kW prototype measurements since only a non-interleaved litz wire transformer, the specifications of which are given in section 5.3.3, was available at the time of measurement. Also the transistors had a higher $R_{ds(on)}$ than would have been available for the voltage range. If these loss mechanisms are properly addressed, efficiencies in excess of 95% can easily be achieved with the resonant push-pull topology.

Figure 3.24 presents the measured diode current and voltage waveforms of 150 W current-fed converter prototypes. It can be seen that the secondary rectifier voltage oscillation amplitude during the switching instants is limited in all topologies. The nominal output voltage in each topology was 150 V.

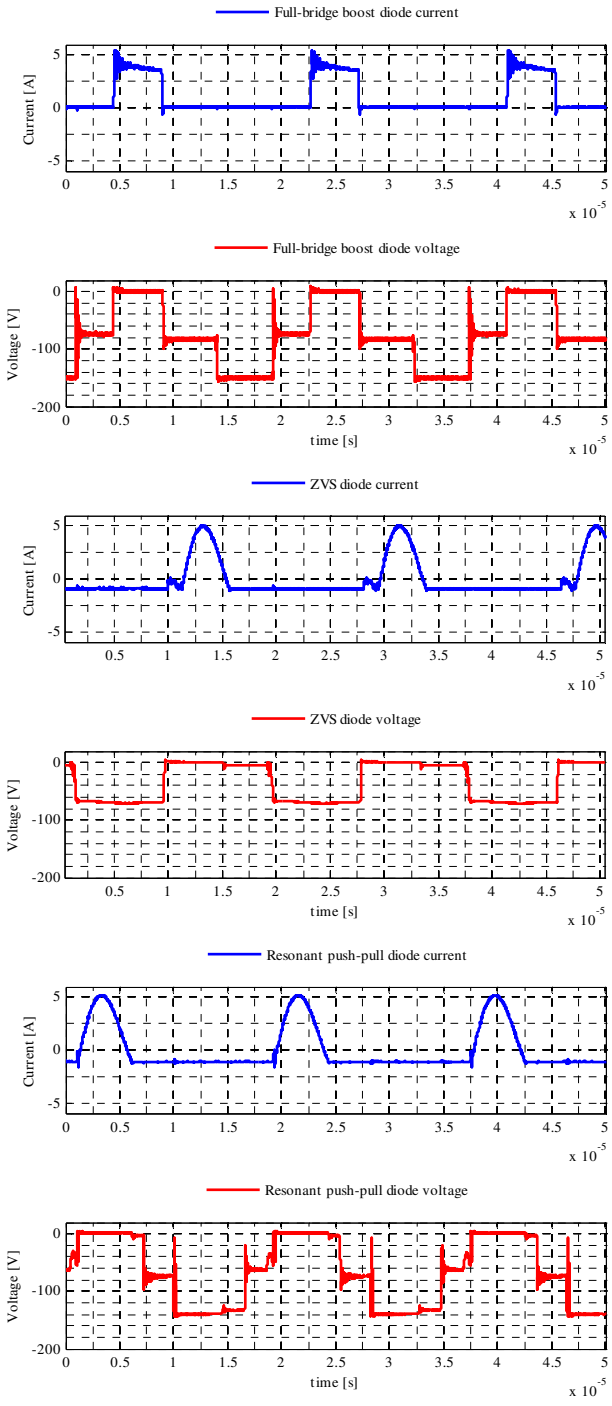


Figure 3.24: Measured secondary rectifier current and voltage waveforms of 150 W current-fed converters.

4 Semiconductor scaling issues

This chapter presents the calculation of conduction and switching losses for MOSFET transistors and rectifier diodes based on the characteristics of the compared converter topologies. The diode conduction losses of the diode bridge and voltage doubler configurations are compared with each other and the advantages of diode paralleling in both configurations are discussed.

4.1 Transistor conduction losses

The transistor conduction losses are compared by presenting the transistor RMS current equations for the topologies (see Appendix A) and by calculating a loss example in a 10 kW (50 V, 200 A) converter application. The first of the two RMS equations in the ZVS boost and RPP indicate the situation where the resonance half period $\sqrt{(L_{lk}C_r)}\pi$ is smaller than $(1\text{-}D)T$.

The conduction losses are now calculated with parameters D = 0.57 (current-fed), D_{eff} = 0.43 (voltage-fed), V_{DC} = 50 V, I_{DC} = 200 A and V_{out} = 660 V. The inductors in the PSFB and FB boost topologies are dimensioned to provide the same 5% peak-to-peak current ripple when referring to the primary circuit. The transformer turn ratios are calculated as in Appendix A.

The peak and RMS currents for the resonant topologies are calculated so that the resonant half period length $\sqrt{(L_{lk}C_r)}\pi$ is equal to $(1\text{-}D)T$ or $D_{eff}T$, and consequently all the secondary rectifiers are zero current switched. This is achieved with identical leakage inductance and voltage doubler capacitor values. The partially zero voltage switched PSFB has a primary leakage of 11 nH, and consequently, transistors S_2 and S_4 are hard switched. When all PSFB transistors are zero voltage switched with a ZVS range from 80% to full load, the primary leakage inductance is 50 nH.

Table 4.1: Transistor peak and RMS currents in the compared topologies for non-clamp transistors.

Topology	Transistor	Transistor I_{peak}	Transistor I_{rms}	Total conduction losses
PSFB, partial ZVS	IRFP4368PBF	235 A	151 A	134 W
PSFB, full ZVS	IRFP4368PBF	247 A	159 A	148 W
PSFBVD	IRFP4368PBF	366 A	170 A	168 W
FB boost	IRFP4368PBF	205 A	137 A	110 W
ZVS boost	IRFP4568PBF	257 A	140 A	198 W
RPP	IRFP4568PBF	257 A	140 A	198 W

The turns ratio in the PSFB topology needs to be much higher than the ideal value due to the duty cycle loss as well as the output inductor voltage loss. The increase in the turns ratio

increases also the PSFB conduction losses, resulting in the full-bridge boost having ultimately the lowest conduction losses among the compared topologies.

The PSFBVD topology has conduction losses similar to the ZVS boost and the RPP despite the possibility to use low $R_{DS(on)}$ transistors. The low primary voltage combined to the resonance operation results in a high peak and RMS current especially if the secondary diodes are zero current switched. The RPP can have lower conduction losses than the ZVS boost when operating under the condition $\sqrt{(L_{lk}C_r)}\pi > (1\text{-}D)T$. In this case, when transistors S_1 and S_2 are both on in the RPP, the current through the transistors equals half the input current, whereas in the ZVS boost the transistors can carry half the input current plus the resonance current.

While the transistor RMS currents in the ZVS boost and RPP topologies are in the same range with the PSFB and the FB boost, the MOSFETs with a higher voltage rating and an inevitably larger $R_{DS(on)}$ result in higher conduction losses, although there are only two transistors conducting the current instead of four.

The clamp transistor conduction losses in the ZVS boost and RPP topologies can be calculated with the equations in Appendix A. The distribution of the clamp transistor current between the body diode and the transistor channel depends on the dead times and on the MOSFET characteristics. A simplified example of the clamp transistor losses in the case that all current would flow in the transistor channel is presented in Table 4.2. The resonance parameters are the same as in Table 4.1.

Table 4.2 : Transistor peak and RMS currents in the compared topologies for clamp transistors.

Topology	Transistor	Transistor I_{peak}	Transistor I_{rms}	Total conduction losses
ZVS boost	IRFP4568PBF	100 A	32 A	5 W
RPP	IRFP4568PBF	100 A	32 A	5 W

The clamp transistor losses can be minimized if the clamp transistors are operated as in Figure 3.19 (a), where the clamp current is cut off near zero.

4.1.1 Duty cycle and transistor conduction losses

Figure 4.1 presents the conduction losses in the topologies compared as a function of the duty cycle when operating under the conditions of Table 1.1.

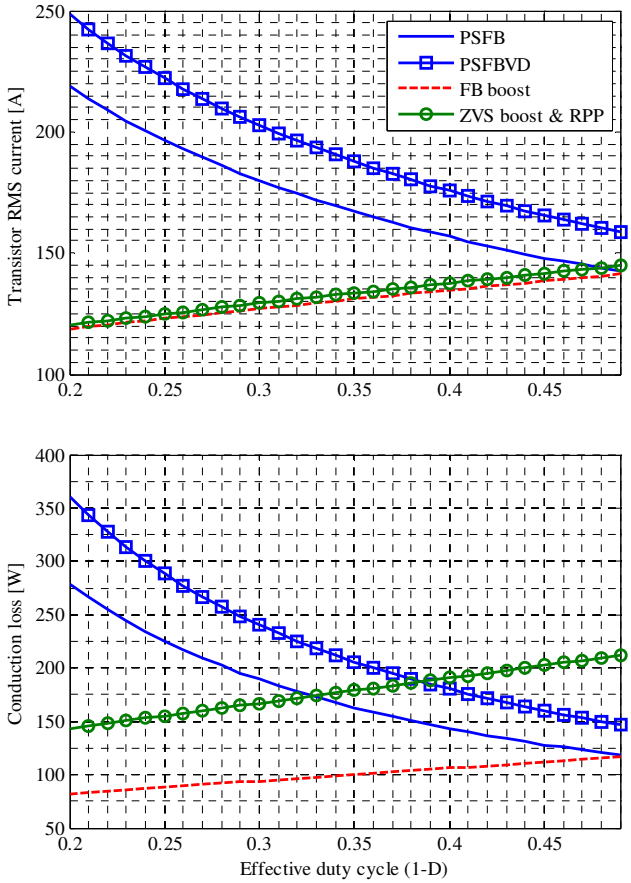


Figure 4.1: Transistor RMS currents and conduction losses as a function of the duty cycle in the case of one transistor.

The current-fed topologies have the weakest dependence between the transistor conduction losses and the duty cycle, indicating that in terms of the transistor losses the topologies are the most flexible for selecting the operating point. Although the RMS currents are nearly equal in all of the current-fed topologies, the FB boost has the lowest conduction losses because the transistors have a low $R_{DS(on)}$.

The conduction losses in the PSFB topology are increased because of the low primary voltage and the need for greater transformer regulation compared to the other topologies. The conduction losses in the PSFBVD topology are increased by the low primary voltage and the resonance operation. The turns ratio is higher than in the current-fed resonant topologies, and consequently, the peak and RMS currents reflected on the primary circuit are also higher.

4.2 Switching losses

In this section the switching losses for the compared topologies are analyzed. The switching losses are divided into turn-on losses (including the losses for zero voltage switched transistors) and turn-off losses.

4.2.1 Turn-on losses in hard switched transistors

The turn-on switching characteristics in all of the topologies compared are a mix of inductive and resistive switching. The resistance in the switching loop results from the transistor resistance, connection resistances and the transformer resistances, while the inductances include parasitic inductances in the transistors, self and mutual inductances in the conductors as well as the leakage inductance of the transformer. To illustrate the effect of drain inductance on turn-on characteristics, a PSpice simulation model according to Figure 4.2 is designed.

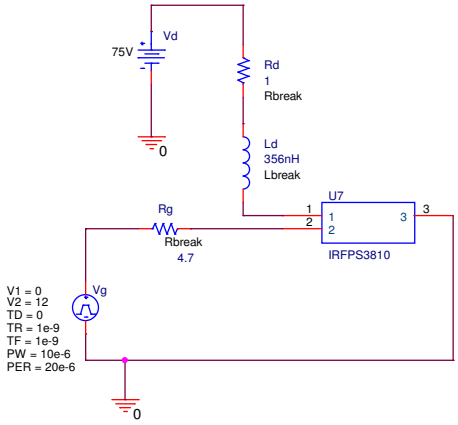


Figure 4.2: Simulation model to test the MOSFET turn-on characteristics in the case of pure resistive as well as combined resistive and inductive switching. The switching frequency is 50 kHz.

The MOSFET IRFPS3810 is a 100 V, 170 A device and its PSpice subcircuit is provided by International Rectifier. The simulation was conducted with and without the inductor while keeping the resistor unchanged. The results from the simulation can be seen in Figure 4.3.

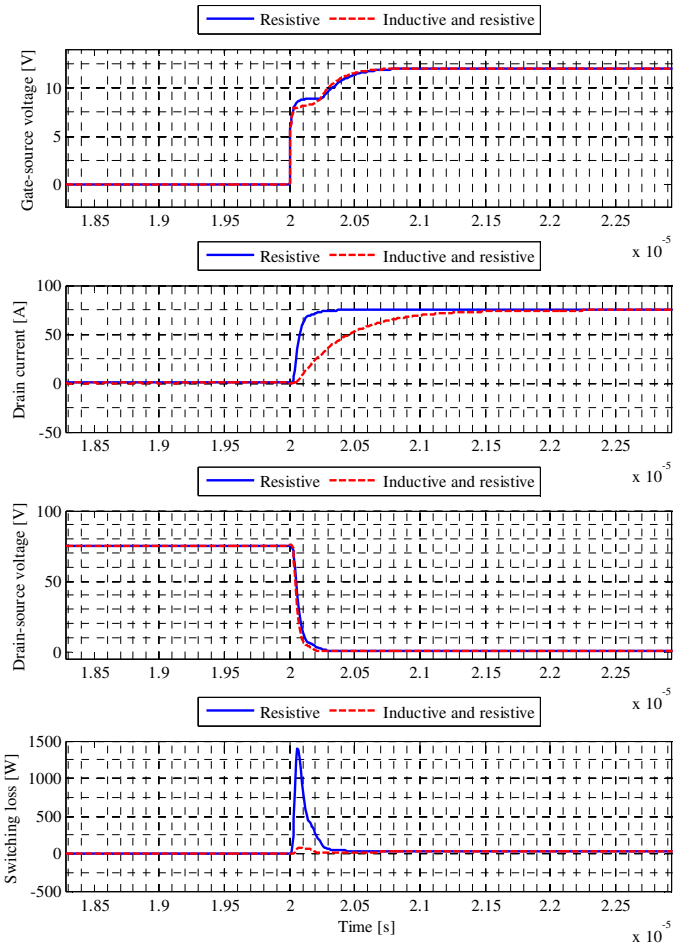


Figure 4.3: Simulated turn-on losses in a purely resistive and in a both resistive and inductive case.

The inductance delays the current rate-of-rise at turn-on, whereas the drain-source voltage drops slightly faster than in the purely resistive case. The result is that the drain-source voltage has dropped to its on-state voltage before the current has risen near its final value. Since there is no significant overlap between voltage and current, the turn-on losses are greatly decreased. In the example in Figure 4.3 the purely resistive switching results in a switching loss of 7 W when the switching frequency is 50 kHz, while the turn-on loss with inductance is only 0.54 W.

The drain-source voltage fall time can be divided into two parts. Firstly, after the gate-source voltage has reached the threshold voltage, the drain current begins to increase. At this point, the capacitor C_{rss} (C_{gd}) is discharged by the gate current, which causes the drain-source voltage to start decreasing at a rate of (Mohan et al., 2003)

$$\frac{dv_{\mathrm{ds}}}{dt} = \frac{V_{\mathrm{G}} - V_{\mathrm{Miller}}}{\left(R_{\mathrm{G(ext)}} + R_{\mathrm{G(int)}}\right)C_{\mathrm{rss}}} \tag{4.1}$$

where the estimate of the Miller plateau voltage V_{Miller} (the near constant gate-source voltage during the decrease in drain-source voltage) is

$$V_{\text{Miller}} = V_{\text{GS(th)}} + \frac{I_{\text{D}}}{g_{\text{m}}}. \tag{4.2}$$

In Equation (4.2), g_{m} is the transconductance, I_{D} is the drain current at which the transconductance is determined and $V_{\text{gs(th)}}$ is the MOSFET threshold voltage. Resistors $R_{\text{G(ext)}}$ and $R_{\text{G(int)}}$ in (4.1) represent an external gate resistor and a gate driver internal pull-up or pull-down impedance, respectively. The Miller voltage is not completely constant, but changes according to the change in drain current. The decrease in drain-source voltage at a rate determined by (4.1) continues until the MOSFET leaves the active region and enters the ohmic region, where $v_{\text{GS}} > v_{\text{DS}}$. While the transistor is in the active region, capacitor C_{rss} can be approximated as a discrete capacitor having the capacitance value C_{rss} @ $V_{\text{DS(off)}}$. Furthermore, while the transistor is in the ohmic region, the capacitor value can be approximated as C_{rss} @ $V_{\text{DS(on)}}$ (Mohan et al., 2003). In the ohmic region, the drain-source voltage waveform decays from voltage v_{GS} to the transistor on-state voltage during the discharge of C_{rss} @ $V_{\text{DS(on)}}$.

The discharge of C_{rss} can also be modeled with the capacitive discharge equation

$$\begin{aligned} v_{C_{\text{rss}}} &= V_{\text{DS(off)}} e^{\frac{-t}{RC_{\text{rss(avg)}}}} \\ R &= \frac{V_{\text{DS(off)}}}{(V_{\text{G}} - V_{\text{Miller}}) \,/\!/\, (R_{\text{G(ext)}} + R_{\text{G(int)}})} \end{aligned}, \tag{4.3}$$

where $V_{\text{DS(off)}}$ is the off-state drain-source voltage, V_{G} is the applied gate voltage and the capacitor $C_{\text{rss(avg)}}$ is an average value for the drain-gate capacitor during the change in drain-source voltage. A datasheet value based approximation for the $C_{\text{rss(avg)}}$ in power MOSFETs was given by Balogh (2007) as

$$C_{\text{rss(avg)}} = 2 \cdot C_{\text{rss(spec)}} \cdot \sqrt{\frac{V_{\text{DS(spec)}}}{V_{\text{DS(off)}}}}, \tag{4.4}$$

where $C_{\text{rss(spec)}}$ is a nominal datasheet value for the capacitor C_{rss} and $V_{\text{DS(spec)}}$ is the drain-source voltage at which the capacitance is measured. The drain current rate-of-rise during the drain-source voltage transition depends on the converter topology. The common-source inductance L_{cs}, which is the stray inductance of the loop between the MOSFET source and the gate driver, sets the maximum limits for the current *di/dt* at turn-on and turn-off. At turn-on, the common-source inductance induces a positive voltage at the source terminal depending on the current *di/dt*. The total gate current available for turn-on is now $(V_{\text{G}}\text{-}V_{\text{Miller}}\text{-}V_{\text{Lcs}})/R_{\text{G(total)}}$, indicating that the gate current and thus the drain-source voltage *dv/dt* are reduced. The maximum *di/dt* at which the drain current can change is $V_{\text{Lcs}}/L_{\text{cs}}$. The maximum limit for the voltage that can be induced across the common-source inductance is $V_{\text{G}}\text{-}V_{\text{Miller}}$. Since the exact treatment of the common-source inductance effects is rather complex to implement (Xiao et al., 2004; Yang and Zhang, 2005; Zhang et al., 2008), the maximum *di/dt* limitations are approximated by (4.5) so that V_{G} is 12 V at turn-on and -12 V at turn-off.

Figure 4.4 illustrates the turn-on behavior of the topologies compared. The waveforms are for a single transistor in a 10 kW application, although the practical application would require parallel transistors due to a high current.

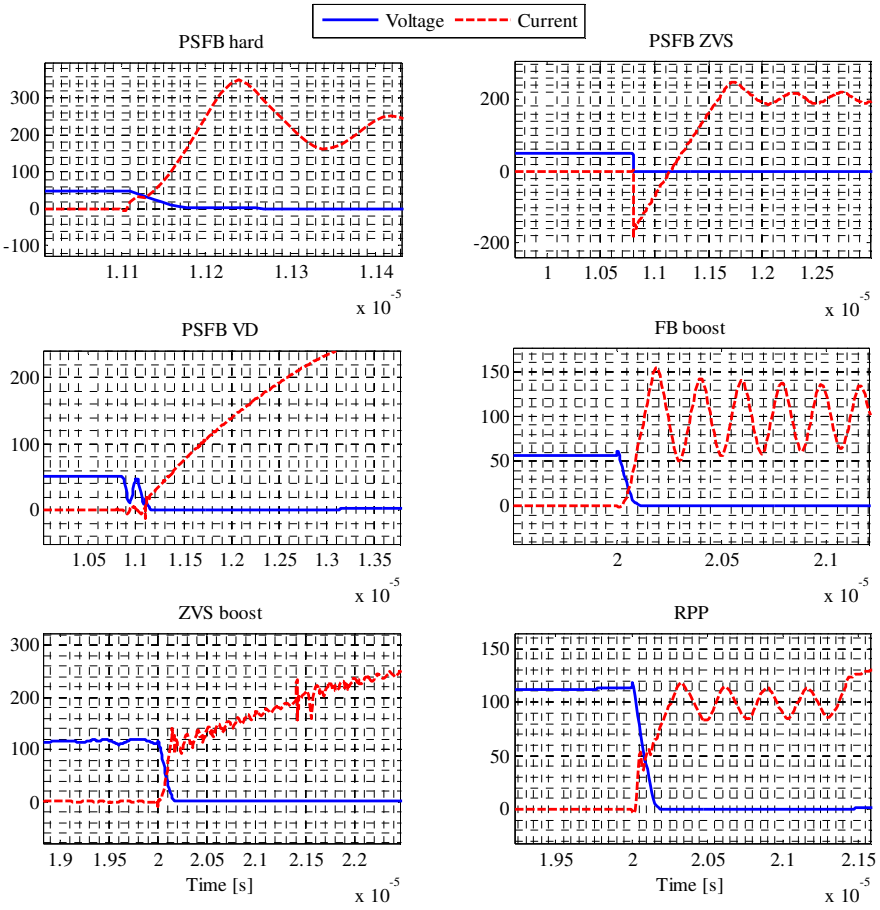


Figure 4.4: Simulated switching waveforms in the compared topologies with D = 0.43 in voltage-fed topologies and D = 0.57 in current-fed topologies. The input voltage is 50 V.

In PSFB, PSFBVD, ZVS boost and RPP topologies the current rises initially to the value of the leakage inductance current after the gate-source voltage threshold is exceeded. The drain current changes at a rate determined by both the clamp circuit inductance (RPP and ZVS boost) and the MOSFET parasitic inductances and transfer characteristics, i.e. the rate at which the drain current changes in relation to the change in gate-source voltage. After the leakage inductance current is achieved, the current rate-of-rise is limited by the *di/dt* determined by the transformer leakage inductance and other inductances in the switch current loop. In FB boost the transistor current rises to the value of half the input inductor current at a rate limited by the transformer leakage inductance *di/dt* and circuit stray inductances. The resonant topologies benefit from small *di/dt*. In addition, the current-fed converters gain advantage from the fact that when operating with $D > 0.5$ the current rises to half the input current during the input inductor charging period, whereas the voltage-fed topologies always switch to a full input current.

Table 4.3 presents the calculated switching losses for each topology when the general converter specifications are as in Table 1.1. To illustrate the effect of leakage inductance on turn-on losses, the leakage inductances are calculated for transformers having two intersections and a PM114/93 core. The general design constraints are listed in Table 5.17. The transformer in the fully zero voltage switched PSFB topology must be calculated with only one intersection in order to achieve large enough leakage inductance and ZVS for transistors S_2 and S_4. The only stray inductance delaying the current rate-of-rise at turn-on is the leakage inductance (conductor inductances are neglected) or the common-source inductance, whichever results in a smaller *di/dt*.

In the PSFB topology, transistors S_1 and S_3 are easily operated with ZVS, and therefore, the turn-on losses are calculated for S_2 and S_4. The turn-on losses in ZVS boost and RPP are calculated for transistors S_1 and S_2 since the clamp transistors are inherently zero voltage switched. The switching time is calculated to the point where the drain-source voltage has fallen to its on-state value. Current transition during the switching time is assumed to be linear, while the voltage changes according to (4.3).

Table 4.3: Calculated turn-on losses per transistor (not clamp transistors or ZVS transistors) in the compared topologies with a 4.7 Ω gate resistor.

Topology	**Transistor**	**Switching time**	**ΔI_d**	**Switching loss**	**Capacitive loss**	**Total**
PSFB, partial ZVS	IRFP4368PBF	232 ns	200 A	5.4 W	0.06 W	11 W
PSFBVD	IRFP4368PBF	232 ns	200 A	5.4 W	0.06 W	11 W
FB boost	IRFP4368PBF	299 ns	100 A	6.9 W	0.07 W	28 W
ZVS boost	IRFP4568PBF	121 ns	109 A	2.7 W	0.25 W	6 W
RPP	IRFP4568PBF	121 ns	109 A	2.7 W	0.25 W	6 W

The differences in current rise times derive from the different transformer turn ratios and thus the different leakage inductance values referred to the primary because the number of primary-secondary intersections was equal. The inductance values and voltages determining the current *di/dt* in Table 4.3 are listed in Table 4.4. In ZVS boost and RPP topologies, transistors S_1 and S_2 will experience a reverse recovery current peak (Figure 3.20) unless the clamp transistors are zero current switched or the clamp transistor body diodes are bypassed with SiC diodes. The reverse recovery peak current (nominal datasheet value) has been included in the calculations of Table 4.3.

Table 4.4: Parameters affecting the current *di/dt* during turn-on. It is assumed that $D = 0.43$ with voltage-fed converters, $D = 0.57$ with current-fed converters, $V_{DC} = 50$ V and $V_{Cr} = 285$ V. It is also assumed that the leakage inductance current is not flowing before primary transistor turn-on in the RPP and ZVS boost topologies, which is the case when operating the secondary rectifiers with ZCS. The inductance limiting the current *di/dt* is expressed without parentheses.

Topology	**Turns ratio**	**Primary leakage**	**Common-source inductance**	**Maximum driving voltage**	$V_{DS(off)}$
PSFB, partial ZVS	2:32	(11 nH)	7 nH	V_{DC}	V_{DC}
PSFBVD	2:14	(7.5 nH)	7 nH	$V_{DC} - \frac{V_{C_r}}{n}$	V_{DC}
FB boost	2:24	(9.4 nH)	7 nH	$\frac{V_{DC}}{2(1-D)}$	$\frac{V_{DC}}{2(1-D)}$
ZVS boost	3:10	(16 nH)	7 nH	$\frac{2D}{1-D}V_{DC}$	$\frac{V_{DC}}{1-D}$
RPP	(2+2):12	(13 nH)	7 nH	$\frac{V_{DC}}{2(1-D)}$	$\frac{V_{DC}}{1-D}$

In these examples, the current *di/dt* at turn-on was limited by small inductances, and therefore, the current rose to its nominal value before the turn-on process was fully completed and the drain-source voltage had decayed to the on-state value. As seen from Figure 3.20 and Figure 4.5, a larger inductance (including all of the stray inductances) can decrease the current *di/dt* so that the voltage across the device can drop before there is any significant change in current. As a result, the only significant turn-on losses are capacitive losses (Nymand, 2010).

The results given in Table 4.3 suggest that the PSFB and the PSFBVD have equal turn-on losses for the hard switched transistors S_2 and S_4 if the turn-on speed is limited by the common-source inductance. If the leakage inductance and the switching loop inductances are large enough to limit the turn-on speed, the PSFBVD has the lowest turn-on losses due to a low voltage and small *di/dt*. Turn-on losses for S_1 and S_3 are negligible since the drain voltage is pulled down before actual turn-on due to a small leakage inductance or magnetizing current through the body diodes. The full-bridge boost benefits from a lower transistor voltage compared to other current-fed topologies, but the large current *di/dt* combined to a longer V_{ds} fall time results in increased turn-on losses. The low $R_{ds(on)}$ transistors have a larger die area, and consequently, the input capacitances are also higher thus explaining the higher V_{ds} fall times in the low voltage topologies. The turn-on loss for the zero voltage switched PSFB topology does not include the body diode conduction losses, which will be discussed later.

The resonant push-pull and ZVS boost can have lower turn-on losses than the FB boost despite the higher voltage especially if the leakage inductance current is cut off at a value larger than zero (no ZCS in the secondary). The leakage inductance current fall rate is determined by the leakage inductance and reflected output voltage. As the transistor current cannot reach the level of half the input current until the leakage inductance current has stopped flowing, the transistor current rate-of-rise in this case is much smaller than in the case where the leakage inductance

current was already near zero. If the leakage inductance current is zero at the transistor turn-on (ZCS in the secondary), the current commutates from transistor S_3 to S_1 (S_4 to S_2) with a *di/dt* limited only by the common-source inductances and the stray inductances in the clamp branch. Also, there are only two hard switched transistors instead of four, which reduces the total losses. The ZVS boost has a much higher drive voltage for the same input voltage and duty cycle, as seen from (3.7), and this results in a higher turn-on *di/dt* when the turn-on speed is limited by the leakage inductance and the switching loop inductance.

The error in the turn-on loss calculation is large if using linear transitions in both the voltage and current. In Figure 4.5 the simulation waveforms of Figure 4.3 are compared to calculated voltage and current waveforms.

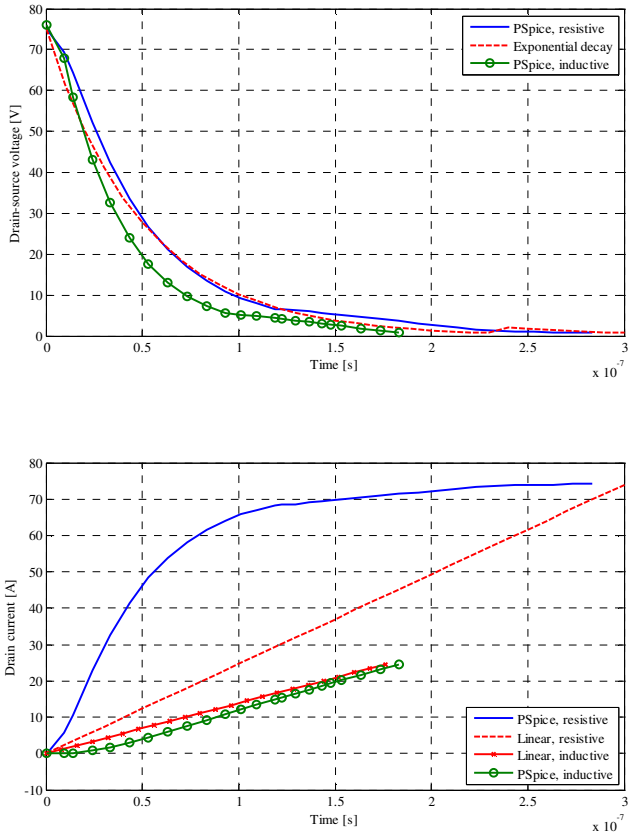


Figure 4.5: Simulated turn-on waveforms versus calculated waveforms. The end point of the curves is the point where the drain-source voltage has decayed to 1% of the initial value.

The drain-source voltage waveform calculated with (4.3) corresponds well to the simulated drain-source voltage waveforms in the resistive case. If the change in voltage was assumed linear, the resulting turn-on losses would be much higher than the actual turn-on losses even if assuming linear transition in current, which results in a smaller current integral than with the actual transistor current. In the inductive case the current *di/dt* is not limited by the transistor itself, but by the inductance. The linear drain current assumption is now more valid, as long as

the final current at a certain drain-source voltage is known. The comparison between the simulated and calculated turn-on losses gives the following results:

- Simulated: 7 W (resistive), 0.7 W (inductive)
- Calculated, voltage and current linear: 14.4 W (resistive), 3.6 W (inductive)
- Calculated, current linear: 4 W (resistive), 0.73 W (inductive)

Calculating with a non-linear voltage and a linear current can give reasonable accuracy in turn-on loss calculations especially when there is inductance in the circuit. Calculations with a non-linear current require knowledge of the relationship between the gate-source voltage and the drain current and the drain current can then be calculated according to the calculated behavior of the gate-source voltage.

4.2.2 Turn-on losses in zero voltage switched transistors

In RPP, the clamp transistor voltage decreases exponentially (discharge of capacitor C_{ds}) after the lower transistor of the switching leg is turned off, allowing the body diode to be forward biased. The diode current increases to half the input inductor current. The diode current increase rate is limited by the turn-off rate of the complementary transistor in the same switching leg. The current *di/dt* during turn-off is limited either by the leakage inductance or the MOSFET common-source inductances, which sets the maximum turn-off speed. If the leakage inductance is the limiting factor, the voltage driving the leakage inductance current change is the difference between the maximum clamp voltage (set either by the snubber circuit or the primary transistor avalanche voltage rating) and the reflected output voltage. If the MOSFET common-source inductance is limiting the drain current *di*/*dt*, the maximum MOSFET turn-off speed can be calculated from (Nymand, 2010)

$$\frac{di_D}{dt} = \frac{v_G - V_{GS}(i_D)}{L_{CS}}, \tag{4.5}$$

where v_g is the gate voltage applied at turn-off (either zero or a negative voltage), $V_{GS}(i_D)$ is the gate-source voltage on a certain drain current (datasheet) and L_{CS} is the common-source inductance including the internal MOSFET inductances and external inductances between the source terminal and the gate driver source connection.

In the ZVS boost topology, the clamp transistor diode current increases to the value of the input inductor current, and as in the RPP, the transistor output capacitor is discharged prior to body diode turn-on. In the PSFB topology a body diode of a zero voltage switched transistor is switched to the freewheeling leakage inductance current at a speed determined by the turn-off of the complementary transistor in the same switching leg, which is limited by the common-source inductances. In all topologies there is an additional forward recovery voltage transient associated with the turn-on of the MOSFET body diode and this forward voltage transient slightly increases the turn-on losses. However, with modern fast switching MOSFET body diodes, the forward voltage loss can be neglected. Figure 4.6 presents the measured zero voltage turn-on waveforms for the PSFB and RPP topologies. The same phenomena can also be seen in the zero voltage switched transistors in the PSFBVD and ZVS boost topologies.

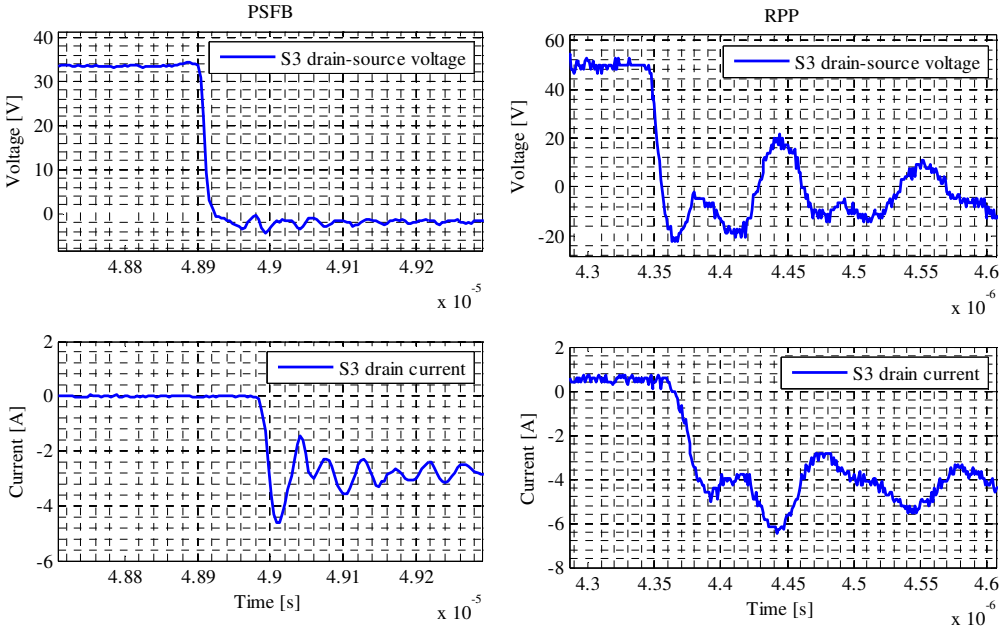


Figure 4.6: Measured zero voltage switching waveforms for the PSFB and RPP topologies. The MOSFET output capacitor is discharged prior to body diode turn-on, and therefore, the turn-on losses are negligible.

The overlap period between the voltage and current is not the only loss mechanism contributing to the total turn-on losses in the PSFB topology. At first, the ZVS mechanism for transistors S_2 and S_4 is explained. The leakage inductance current starts freewheeling through the transistor S_4 body diode at time instant t_2 in Figure 2.6 and this freewheeling current flows through the diode until transistor S_4 is turned on and the current starts commutating to the transistor channel. The leakage current *di/dt* during t_2-t_1 is

$$\frac{di_{L_{lk}}}{dt} = \frac{nV_{DC}}{L_{lk}}. \tag{4.6}$$

The peak leakage inductance current at time instant t_1 referred to the primary and the transistor S_4 body diode can be calculated based on equations (2.4)-(2.8), that is

$$I_{D_4}(t_1) = nI_{L_{lk}}(t_1), \tag{4.7}$$

and the body diode current at instant t_2, when the transistor is turned on, can be calculated from

$$I_{D_4}(t_2) = I_{D_4}(t_1) - \frac{V_{DC}}{L_{lk}/n^2} \cdot t_{safe}. \tag{4.8}$$

Figure 4.7 illustrates the diode current waveform during turn-on.

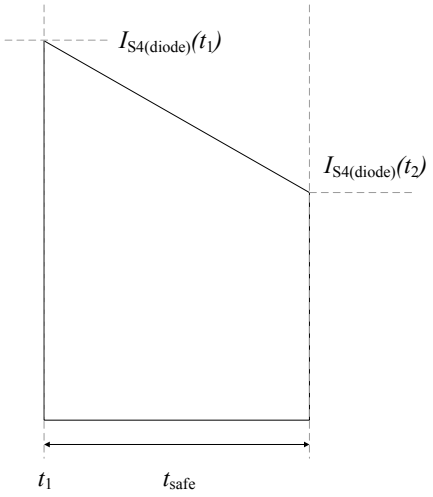


Figure 4.7: Transistor S_2 or S_4 body diode current waveform in the PSFB topology, when operating under ZVS.

The diode RMS current can be calculated based on the safe time and trapezoidal segment RMS equation

$$I_{D_4,rms} = \sqrt{\frac{t_{safe}}{T} \cdot \frac{1}{3}\left(I_{D_4}(t_1)^2 + I_{D_4}(t_1) \cdot I_{D_4}(t_2) + I_{D_4}(t_2)^2\right)} \tag{4.9}$$

and for calculating the diode losses the average current equation needs to be derived as

$$\begin{aligned} I_{D_4,avg} &= \frac{1}{T}\int_0^{t_{safe}} \left(\frac{I_{D_4}(t_1) - I_{D_4}(t_2)}{t_{safe}} \cdot t + I_{D_4}(t_2) \right) dt \\ I_{S4(diode,avg)} &= \frac{t_{safe}\left(I_{D_4}(t_1) + I_{D_4}(t_2)\right)}{2T} \end{aligned} . \tag{4.10}$$

The diode conduction losses can be modeled by a fixed voltage drop in series with a resistive element as

$$P_{cond} = V_D I_{D(avg)} + R_D I_{D(rms)}^{\ 2} . \tag{4.11}$$

The voltage V_D and the series resistance R_D are often not directly given in transistor datasheets, but they can be extracted from the datasheet graphs.

The zero voltage switching for transistors S_1 and S_3 is achieved more easily since the leakage inductance current change during t_1-t_0 or t_3-t_4 is driven by a low voltage. The zero voltage

switching conditions apply as long as the output inductor operates under continuous conduction mode.

In Figure 2.6, transistor S_3 is turned off at instant t_3. The leakage inductance current begins to decrease at the rate described in Equations (2.4) and (2.5), and the leakage inductance current value at instant t_3 can be approximated to be equal to the converter load current. The duration of the current freewheeling through the body diodes of transistors S_1 and S_3 can be calculated from (2.6), while the current *di/dt* can be derived from (2.5). As the initial and final leakage inductance currents are referred to the primary, the body diode losses during the freewheeling period t_4-t_3 can be calculated similarly as with transistors S_2 and S_4.

In order to achieve zero voltage switching for all transistors over a reasonable load range, a large leakage inductance is needed. This can lead to high diode conduction losses in transistors S_2 and S_4, as the diode current slope during t_4-t_3 is very gentle. Table 4.5 presents the calculated diode conduction losses for two cases. In the first case all transistors are zero voltage switched from 80% load to full load. This is achieved with a 50 nH leakage inductance, which is 12 µH as referred to the secondary. In the second case the leakage inductance is reduced to 11 nH so that S_2 and S_4 are hard switched, while S_1 and S_3 are still zero voltage switched. The safe time t_{safe} between the transistors in the same leg is 150 ns and the switching frequency is 50 kHz.

Table 4.5: Comparison of body diode conduction losses in the PSFB topology with hard and soft switching.

Switching scheme	**S1 & S3 diode I_{avg}/I_{rms}**	**S1 & S3 diode conduction losses**	**S2 & S4 diode I_{avg}/I_{rms}**	**S2 & S4 diode conduction losses**
Zero voltage switching	14 A/55 A	14 W	1 A/0.78 A	1 W
Hard switching	11 A/45 A	10 W	0.43 A/0.5 A	0.43 W

The clamp transistor body diode conduction losses related to the turn-on in the ZVS boost and RPP topologies can be evaluated by calculating the average and RMS diode currents according to Appendix A. When conducting the calculations in the same operating conditions as in the PSFB topology, the average diode current with a 150 ns dead time would be 0.8 A and the RMS current 9 A. If these values are used together with the IRFP4568PBF diode parameters (Appendix A), the conduction loss will be 0.6 W per clamp transistor.

The total turn-on losses for the topologies from Tables 4.3 and 4.5 are now:

- PSFB, hard switched S_2 & S_4 = 21 W
- PSFB, soft switched S_2 & S_4 = 15 W
- PSFBVD = 11 W
- FB boost = 28 W
- ZVS boost = 7 W
- RPP = 7 W

The zero-voltage switching in the PSFB topology is beneficial also in low voltage applications if considering strictly the turn-on losses caused by voltage and current overlap. However, since transistors S_1 and S_3 are zero-voltage switched as long as the output inductor operates under continuous conduction mode, there will be high circulating currents through the transistor body diodes whether or not transistors S_2 and S_4 are zero voltage switched.

4.2.3 Turn-off losses in transistors

The voltage rise time across a transistor during turn-off depends on the charging time of the input capacitor via the gate resistor. At first, when gate voltage is pulled down, the gate-source voltage decreases to the Miller voltage and the drain-source voltage starts increasing. The gate current charging the C_{rss} capacitance during this time can be estimated from

$$I_G = \frac{V_{\mathrm{G(off)}} - V_{\mathrm{Miller}}}{R_{\mathrm{off(int)}} + R_{\mathrm{off(ext)}}}. \tag{4.12}$$

It can be seen that if a negative gate voltage is used, there is more gate current available and the turn-off will be faster. The time required to charge the C_{rss} capacitor can be calculated similarly as during turn-on, but in reverse order. Figure 4.8 illustrates the transistor turn-off in the configuration of Figure 4.2.

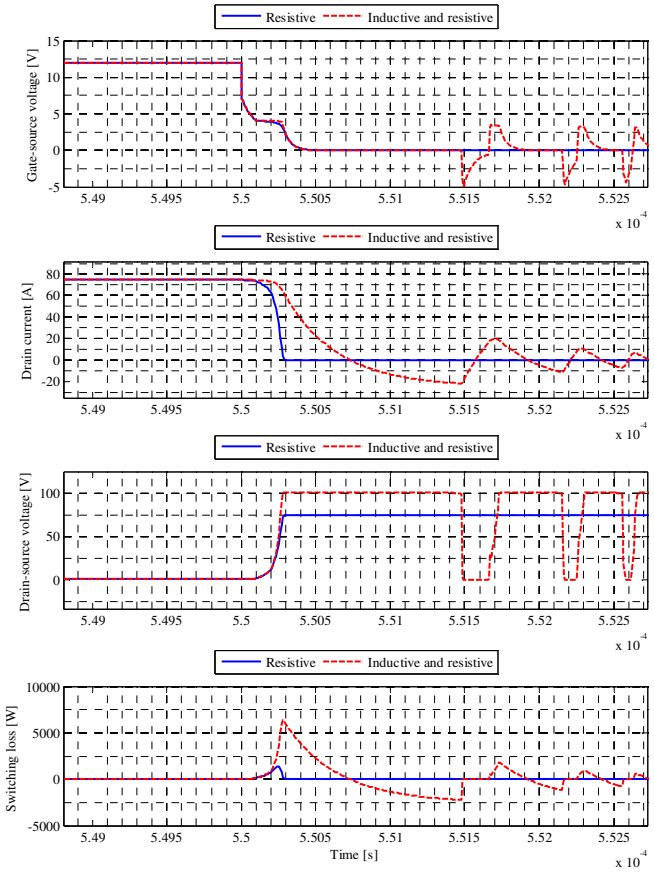


Figure 4.8: Simulated turn-off losses in a purely resistive and in a both resistive and inductive case.

In the inductive switching, the drain-source voltage rises to its clamp value before there is any significant change in current, resulting in a significant overlap between voltage and current. The total turn-off loss including all of the transients is now 22 W in the inductive case, whereas the turn-off loss with only resistance in the circuit is 6 W. The resistive turn-on and turn-off losses are practically equal, but the inductive turn-off losses are much larger than the turn-on losses. Due to the turn-off loss mechanism it is preferable to use turn-off switching that is as fast as possible. This requires a small pull-down resistance from the gate driver and either a very small leakage inductance or common source inductance, whichever is limiting the maximum turn-off speed.

The turn-off conditions for the compared topologies are listed in Table 4.6. Voltage $V_{\mathrm{DS(off)}}$ is the maximum voltage which is seen across the transistor while the transistor current is decreasing.

Table 4.6: Turn-off currents and voltages for the compared topologies. Time instants t_0 and t_1 refer to Figure 4.9.

Topology	Primary leakage	Common-source inductance	$I_{D(off)}$	$V_{DS(off)}$	L_{leak} voltage
PSFB, no ZVS	(11 nH)	7 nH	S_1 & S_3: I_D @ t_3 S_2 & S_4: I_D @ t_1	0-V_{DC}	V_{DC}
PSFB, ZVS	50 nH	(7 nH)	S_1 & S_3: I_D @ t_2 S_2 & S_4: I_D @ t_1	0-V_{DC}	V_{DC}
PSFBVD	7.5 nH	7 nH	0-$I_{D(peak)}$	0-V_{DC}	V_{DC}
FB boost	9.4 nH	7 nH	$I_{DC}/2$	$\frac{V_{DC}}{2(1-D)} < V_{DS(off)} \le V_{BR(DSS)}$	$V_{C(FB\ boost)}$
ZVS boost	(16 nH)	7 nH	$I_{DC}/2$	$\frac{V_{DC}}{1-D}$	$V_{C(ZVS\ boost)}$
RPP	13 nH	7 nH	$I_{DC}/2$	$\frac{V_{DC}}{1-D}$	$V_{C(RPP)}$

The voltages driving the leakage inductance current change in the current-fed topologies can be calculated from

$$\begin{aligned} V_{C(FB\ boost)} &= V_{DS(max)} - \frac{V_{out}}{n} \\ V_{C(ZVS\ boost)} &= V_{DS(max)} - \left(\frac{D}{1-D} V_{DC} - V_{DC} \right). \\ V_{C(RPP)} &= \frac{V_{DS(max)}}{2} \end{aligned} \tag{4.13}$$

Voltage $V_{DS(max)}$ is either a voltage set by the clamp circuit (inherent in the PSFB, PSFBVD, ZVS boost and RPP topologies) or the maximum transistor avalanche breakdown voltage if there is no clamp circuit (or if the clamp circuit series inductance is high) and the current turn-off time is long enough to allow the voltage to rise to the avalanche breakdown level.

The primary transistors in the PSFBVD topology can be tuned for both zero current and zero voltage switching, and thus the turn-off losses are practically negligible. The turn-off losses in the PSFB topology depend on whether the transistors are turned on with zero voltage or not. Figure 4.9 illustrates the different turn-off cases.

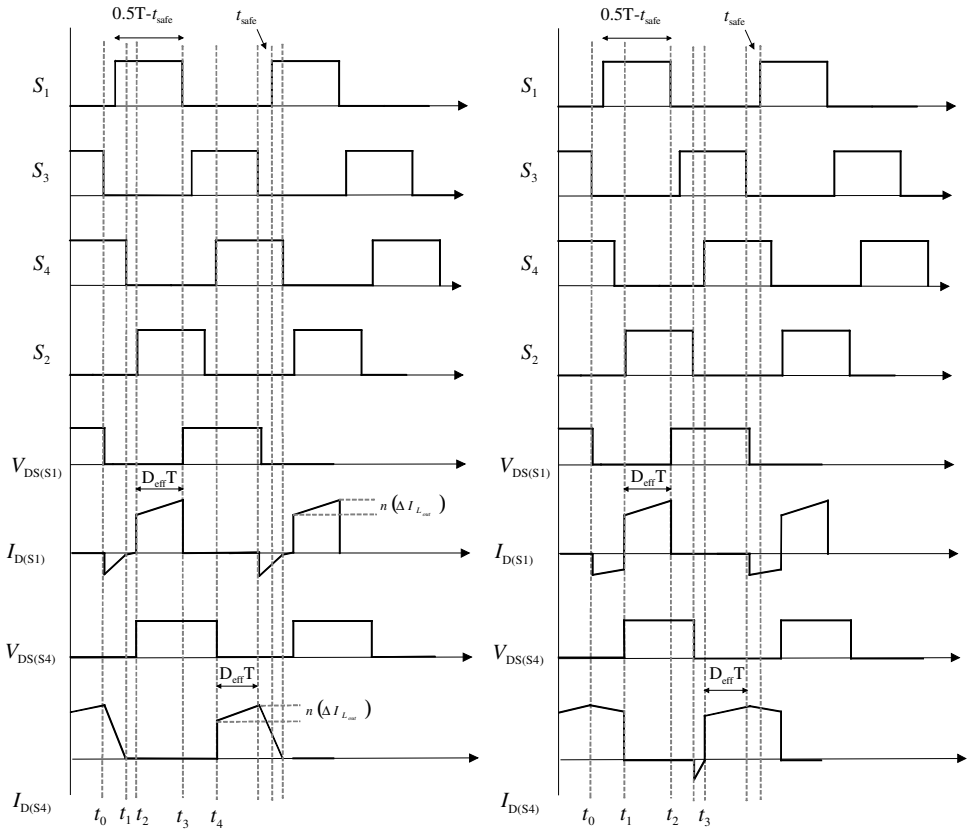


Figure 4.9: Idealized drain current and voltage waveforms for transistors S_1 and S_4 in the PSFB topology in a partially zero voltage switched (a) and fully zero voltage switched (b) case. The similar principles apply also for transistors S_2 and S_3. The current *di/dt* after t_2 (a) and t_3 (b) has been exaggerated for clarity.

At instant t_0 in Figure 4.9 (a), transistor S_3 is turned off. The leakage inductance current is freewheeling through the body diode of S_1 while decreasing rapidly, and the current through transistor S_4 is decreasing at the same rate. At instant t_1, the leakage inductance current has decreased to the magnetizing current value, and this current freewheels through the transistor S_4, keeping the drain-source voltage low until instant t_2, when a current route is opened through transistors S_1 and S_2. At instant t_3, transistor S_1 is turned off and its output capacitor is charged by the transformer current at the same time as the output capacitor of S_3 is discharged. As the freewheeling current amplitude is large, the charging/discharging process of the output capacitors is fast, allowing the drain-source voltage to change rapidly while the drain current is changing. In the partially zero voltage switched case, transistors S_2 and S_4 can be turned off with negligible losses.

In the fully zero voltage switched case in Figure 4.9 (b), the leakage inductance current *di/dt* during t_1-t_0 and the freewheeling current through the body diode of transistor S_1 do not fall to the magnetizing current value before instant t_1. At this instant, the transistor S_4 output capacitor is charged and the output capacitor of S_2 is discharged with a high current, resulting in fast voltage

transitions. While all transistors are turned on with zero voltage, they are turned off with overlapping current and voltage, which results in increased overall switching losses in low voltage, high current applications.

The turn-off losses, if calculated with parameters V_{DC} = 50 V, I_{DC} = 200 A and D = 0.57 (D = 0.43 for the voltage-fed topologies), are listed in Table 4.7. It is assumed that due to inductive turn-off the drain-source voltage is pulled to its $V_{DS(off)}$ value before the drain current starts to decrease. With ideal clamp circuits, the voltage $V_{DS(off)}$ for each topology is the minimum value listed in Table 4.6.

Table 4.7: Calculated turn-off losses for the compared topologies.

Topology	Current fall-time to zero	ΔI_d S1/S2	Losses S_1/S_2	Clamp losses	Total
PSFB, partial ZVS	100 ns/~ 0 ns	235 A/1 A	29 W/~0 W	-	59 W
PSFB, full ZVS	235 ns/115 ns	235 A/115 A	69 W/17 W	-	172 W
PSFBVD	-	0 A	-	-	-
FB boost	43 ns	100 A	6 W	-	24 W
ZVS boost	40 ns	100 A	12 W	6 W	30 W
RPP	40 ns	100 A	12 W	6 W	30 W

As demonstrated in Figure 3.19, the turn-on of transistors S_1 and S_2 in ZVS boost and RPP topologies will force the clamp transistor body diodes into reverse recovery. The larger the forward current at diode turn-off, the larger the stored charge and thus the reverse recovery loss (4.14). As an example, the recovery losses are calculated with the following parameters: f = 50 kHz, Q_{rr} = 515 nC (nominal datasheet value) and V_r = 116 V. In this case, the resulting reverse recovery loss per clamp transistor would be 3 W. Since the reverse recovery charge increases together with temperature and the turn-off di/dt, the given calculation example would be a best case approximation under the given operating conditions.

The main conclusions of the turn-off analysis are that turn-off losses will always dominate over turn-on losses in low voltage, high current applications and that it is easier to achieve lower turn-off losses in current-fed topologies than in the basic phase-shift full-bridge topology.

The phase-shifted full-bridge topology suffers from large turn-off losses in spite of the lowest drain-source voltage at turn-off since the turn-off current is high especially in transistors S_1 and S_3. The turn-off current of S_2 and S_4 depends on the zero-voltage switching conditions and as is demonstrated here, the zero-voltage switching in these transistors comes with a cost of highly increased turn-off losses. In terms of overall switching losses, it may be preferable to keep S_2 and S_4 hard switched.

If the current switching speed is identical, the full-bridge boost topology may have lower turn-off losses compared to the other current-fed topologies since the drain-source voltage is inherently lower than in the ZVS boost and RPP. If the clamp circuits in the topologies are inductive and not able to limit the drain-source voltage to the nominal $V_{DS(off)}$ (as is the case in practice), the turn-off losses will be even higher.

4.2.4 Duty cycle and transistor switching losses

In the current-fed converters, the transistors are always switched on and turned off from a current that is half the input inductor current when operating with $D > 0.50$. Therefore, the switching losses are not dependent on the duty cycle if the input inductor current ripple is constant.

In the PSFB topology, the transistors are switched on and turned off from a current that equals the reflected output current and the output inductor current ripple. If the current ripple and the output current are constant, the peak transistor current is dependent on the transformer turns ratio. Since the required transformer turns ratio increases as a function of the duty cycle, the transistor peak current also increases. The increased turn-off current results in larger turn-off losses. The turn-on losses increase in terms of higher body diode losses since the freewheeling current amplitude increases together with the transformer turns ratio.

In the PSFBVD topology, the turn-off losses as a function of the duty cycle depend on the resonant half-period length. If the transistors can operate under ZCS over the entire duty cycle range, the turn-off losses are unaffected.

4.3 Diode conduction and switching losses

The equations used to calculate average and RMS currents for the output rectifier diodes in the compared topologies are presented in Appendix A. The diodes are selected based on the maximum rectifier voltage if the output voltage is 660 V.

The conduction losses for a diode can be approximated by using (4.11). The diode switching losses can be estimated based on the reverse recovery charge and the capacitive charge as (Mohan et al., 2003; Nymand, 2010; Walters, n.d.)

$$P_{\mathrm{sw}} = Q_{\mathrm{rr}} V_{\mathrm{r}} f + E_{\mathrm{C}} f = \frac{I_{\mathrm{rm(rec)}} t_{\mathrm{rr}}}{2} V_{\mathrm{r}} f + \frac{1}{2} C_{\mathrm{j}} V_{\mathrm{r}}^{\,2} f \,, \tag{4.14}$$

where $I_{\mathrm{rm(rec)}}$ is the peak reverse recovery current dependent on the di/dt value at diode turn-off, t_{rr} is the reverse recovery time, f is the switching frequency, C_{j} is the reverse voltage dependent junction capacitance and V_{r} is the reverse voltage which the diode needs to support.

In PSFB and FB boost topologies, the maximum diode current di/dt can be calculated from Table 4.4 since the diode current changes at the same rate as the leakage inductance current at transistor turn-on. In the resonant topologies, the maximum diode current di/dt can, if the diodes are not zero current switched, be estimated from (3.22).

The ZVS boost topology may have different RMS currents, and thus, different conduction losses in diodes D_1 and D_2 (or D_3 and D_4). It is seen from Figure 3.11 that the resonance current is driven by two different primary voltages. The primary voltage during diode D_1 conduction is $V_{\mathrm{pri(max)}}$, while it is $-V_{\mathrm{DC}}$ during the conduction of diode D_2. The initial resonant capacitor voltages V_{C3} and V_{C4} prior to D_1 or D_2 conduction are

$$V_{C3}(t_5) = \frac{V_{\text{out}}}{2} D - \frac{I_{\text{load}}}{\frac{2}{T}(C_3 + C_4)}$$
$$V_{C4}(t_0) = \frac{V_{\text{out}}}{2}(1-D) - \frac{I_{\text{load}}}{\frac{2}{T}(C_3 + C_4)} \quad (4.15)$$

and these voltages together with the transformer secondary voltage determine the maximum diode peak current. When $\sqrt{(L_{\text{lk}}C_{\text{r}})}\pi$ is smaller than $(1\text{-}D)T$, the peak diode currents and RMS current are ideally equal.

Since the average diode currents are always equal to the load current, the shorter conduction period of diode D_1 when $\sqrt{(L_{\text{lk}}C_{\text{r}})}\pi$ is larger than $(1\text{-}D)T$ results in a higher peak current in this diode. The peak currents for the diodes in this case are

$$I_{\text{peak(D1\&D3)}} = -\frac{I_{\text{avg}} \cdot T \cdot \omega_{\text{r}}}{\cos[T \cdot \omega_r (D-1)] - 1}$$
$$I_{\text{peak(D2\&D4)}} = -\frac{I_{\text{avg}} \cdot T \cdot \omega_{\text{r}}}{\cos(DT \cdot \omega_{\text{r}}) - 1} \quad (4.16)$$

The increased peak current of D_1 and D_3 results in a slightly higher RMS current for these diodes.

Table 4.8 presents the calculated Si diode losses in a 10 kW converter, where the leakage inductances and other parameters are similar to the transistor switching loss calculations. The junction capacitance for the Si-diodes was not given in the datasheets, and consequently, it is neglected. The *di/dt* value in the resonance topologies refers to the *di/dt* which occurs if the leakage inductance current is cut off before it has resonated to zero.

Table 4.8: Calculated diode losses when using Si diodes. Diodes in the resonant topologies are zero current switched and the switching losses are neglected.

Topology	I_{avg}	I_{rms}	***Max di/dt***	P_{cond}	P_{sw}	P_{total}
PSFB, partial ZVS	7.6 A	10.6 A	319 A/µs	13 W	20 W	261 W
PSFB, full ZVS	7.6 A	11.3 A	85 A/µs	13 W	13 W	209 W
PSFBVD	15.2 A	25.7 A	253 A/µs	31 W	-	62 W
FB boost	7.6 A	12 A	86 A/µs	13 W	13 W	105 W
ZVS boost	15.2 A	25.7 A	2300 A/µs	20 W	-	80 W
RPP	15.2 A	25.7 A	985 A/µs	31 W	-	62 W

The high *di/dt* values resulting from small leakage inductances and the high output voltage can result in large diode switching losses even if using fast Si diodes. The resonance topologies can be operated with zero current switched rectifier diodes and the reduction in switching losses can

thus be significant. The resonant topologies will have lower switching losses than the hard switched topologies even if the rectifiers are hard switched, provided that the leakage inductance is increased in order to reduce the *di*/*dt* and the current waveforms are quasisinusoidal, preventing the current from being cut off at its peak value.

The diodes in the partially zero voltage switched PSFB topology suffer from a large *di*/*dt* at turn-off, increasing the switching losses. The conduction losses are only slightly lower than in the fully zero voltage switched case. Due to a high rectifier voltage, there has to be one high voltage rectifier, two lower voltage rectifiers in series or two diode bridges connected in separate transformer secondary windings. In these loss examples, two rectifiers were used in series, and this increases the minimum number of rectifiers to eight, whereas the FB boost topology can operate with four diodes. The PSFBVD and RPP topologies need only two diodes, whereas the ZVS boost requires four diodes, which is seen as increased conduction losses.

Table 4.9: Calculated diode losses when using SiC diodes. The reverse recovery switching losses are neglected in all topologies and the only switching loss is the capacitive loss.

Topology	I_{avg}	I_{rms}	***Max di/dt***	P_{cond}	P_{sw}	P_{total}
PSFB, partial ZVS	7.6 A	10.6 A	319 A/µs	17 W	0.5 W	140 W
PSFB, full ZVS	7.6 A	11.3 A	85 A/µs	18 W	0.5 W	146 W
PSFBVD	15.2 A	25.7 A	253 A/µs	73 W	0.5 W	147 W
FB boost	7.6 A	12 A	86 A/µs	24 W	0.5 W	98 W
ZVS boost	15.2 A	25.7 A	2300 A/µs	47 W	0.3 W	189 W
RPP	15.2 A	25.7 A	985 A/µs	73 W	0.5 W	147 W

When using SiC diodes, the hard switched topologies outperform the resonant topologies in terms of overall diode losses. The increased average and RMS current in the resonant topologies combined with a higher forward voltage drop in the SiC diodes result in high conduction losses, although fewer diodes are needed in total. The ZVS boost topology with the high diode count has the largest rectifier losses, although the 600 V voltage SiC diode used in the comparison had a lower forward voltage drop per diode.

The benefits of SiC diodes in the resonant topologies are questionable if the SiC diode forward characteristics are weaker than with a comparable Si diode and if the diodes are operated in order to minimize the switching losses. However, since the Si diodes have a negative temperature coefficient, the current sharing in the case of diode paralleling cannot be guaranteed, and the losses per diode can be higher than anticipated. When using SiC diodes, the conduction losses can be significantly reduced by paralleling and the positive temperature coefficient helps to ensure current sharing between the diodes.

4.3.1 Duty cycle and diode conduction losses

Figure 4.10 describes the PSFB topology rectifier diode current waveforms in the case that the leakage inductance current falls to zero before transistors S_1 or S_3 are turned on (Figure 2.6).

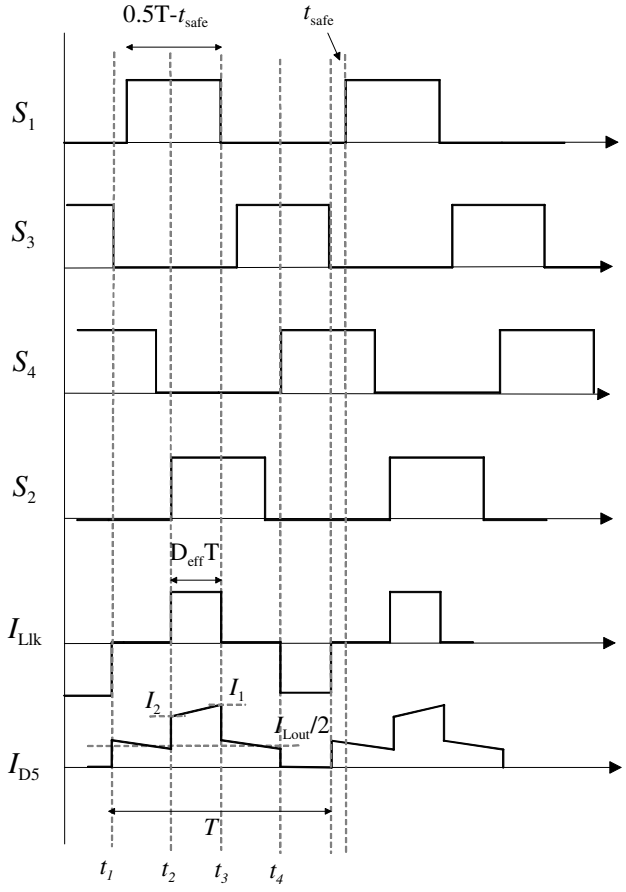


Figure 4.10: Leakage inductance current and diode current in the case of a small leakage inductance and a small effective duty cycle.

Between instant t_2-t_1 and t_4-t_3, the diode conducts half the output inductor current since the current freewheels through all of the rectifier diodes. The total average diode current is half the output inductor average current. The contribution of the time periods t_2-t_1 and t_4-t_3 to the total average diode current is

$$I_{\text{avg(1)}} = \frac{I_{\text{L}_{\text{out}}}}{2} - D_{\text{eff}} I_{\text{L}_{\text{out}}} . \tag{4.17}$$

The rest of the diode average current results from the period t_3-t_2, and it is the difference between the half average inductor current and the current $I_{\text{avg(1)}}$. Considering the average of a trapezoidal segment (4.10), the sum I_1+I_2 can be solved as

$$\left(I_1 + I_2\right) = \frac{I_{\text{L}_{\text{out}}(\text{avg})} - I_{\text{avg(1)}}}{D_{\text{eff}}} . \tag{4.18}$$

The diode RMS current can then be calculated from a piecewise approximation of

$$I_{rms} = \sqrt{(I_1 + I_2)^2 \cdot D_{\text{eff}} - 2D_{\text{eff}} {I_{\text{L}_{\text{out}}}}^2 + {I_{\text{L}_{\text{out}}}}^2} \,. \tag{4.19}$$

If the leakage inductance current does not fall to zero before S_1 or S_3 is turned on, the diode RMS current can be estimated from

$$I_{rms} = I_{out} \sqrt{\frac{t_3 - t_1}{T}} \sqrt{1 + \frac{1}{3}\left(\frac{\Delta I_{\text{L}_{\text{out}}}}{2I_{\text{out}}}\right)^2} \,, \tag{4.20}$$

where t_3 and t_1 refer to Figure 2.6.

Figure 4.11 presents the conduction losses in the topologies compared as a function of the duty cycle when operating under the conditions of Table 1.1 and when using SiC diodes.

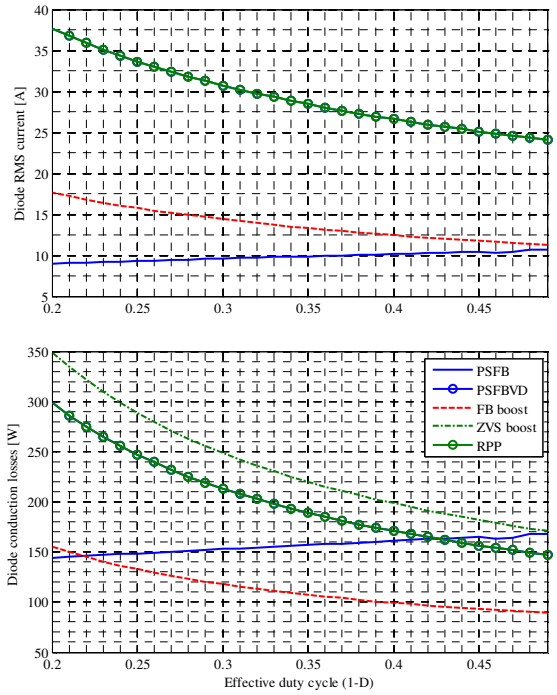


Figure 4.11: Secondary rectifier RMS currents and conduction losses as a function of the duty cycle in the case of one diode.

All of the resonant topologies have the same RMS diode current if the input and output parameters as well as the resonant components are identical. The PSFB diode RMS current increases together with the effective duty cycle, whereas in other topologies it decreases. The ZVS boost has lower conduction losses per single diode than the PSFBVD and RPP topologies,

but since the ZVS boost has a minimum of four diodes, the overall losses are higher than in the topologies with only two diodes.

The FB boost topology has the lowest diode conduction losses among the topologies compared since the average and RMS currents are relatively low and the required number of rectifiers is lower than in the PSFB topology (assuming that a diode snubber is not used).

4.4 Semiconductor losses versus costs

In this section, the initial costs and operating costs of the semiconductor devices are compared. Absolute device costs are used in the calculation and the publicly available costs for the semiconductor devices are listed in Appendix A. The cost of power losses is based on a feeding tariff of € 83.5/MWh.

Table 4.10: Example of the effect of MOSFET paralleling on losses and costs.

Topology	Transistors	Losses [W]	Initial cost [€]	Cost/5 a [€]	Cost/10 a [€]
PSFB, partial ZVS	4/8/12	214/147/125	50/101/151	833/638/607	1616/1176/1063
PSFB, full ZVS	4/8/12	335/261/236	50/101/151	1276/1055/1016	2501/2010/1880
PSFBVD	4/8/12	180/96/67	50/101/151	709/450/397	1367/799/644
FB boost	4/8/12	162/107/89	50/101/151	643/492/475	1235/883/800
ZVS boost	4/6/8	235/142/104	34/51/68	894/571/471	1753/1090/873
RPP	4/6/8	235/142/104	34/51/68	894/571/471	1753/1090/873

The reduction in conduction losses while paralleling transistors is

$$\frac{P_{\text{cond(parallel)}}}{P_{\text{cond(single)}}} = \frac{n\left(\frac{I}{n}\right)^2}{I^2} = \frac{1}{n}, \tag{4.21}$$

where I is the current and n is the number of parallel transistors. The reduction in PSFB transistor body diode conduction losses is

$$\begin{aligned} \frac{P_{\text{S4(parallel)}}}{P_{\text{S4(single)}}} &= \frac{1}{n} - \frac{I_2\left(3V_{\text{D}} - 3V_{\text{D}}n\right) + 3I_1V_{\text{D}} - 3I_1V_{\text{D}}n}{n\left(2R_{\text{D}}{I_1}^2 + 2R_{\text{D}}I_1I_2 + 3V_{\text{D}}I_1 + 2R_{\text{D}}{I_2}^2 + 3V_{\text{D}}I_2\right)} \\ \frac{P_{\text{S1(parallel)}}}{P_{\text{S1(single)}}} &= \frac{1}{n} - \frac{I_4\left(3V_{D} - 3V_{D}n\right) + 3I_3V_{D} - 3I_3V_{D}n}{n\left(2R_{\text{D}}{I_3}^2 + 2R_{\text{D}}I_3I_4 + 3V_{\text{D}}I_3 + 2R_{\text{D}}{I_4}^2 + 3V_{\text{D}}I_3\right)} \end{aligned}, \tag{4.22}$$

where $I_{1\text{-}4}$ are the body diode currents at the corresponding time instants in Figure 2.6.

While the conduction losses are reduced, the switching losses are increased by the capacitive loss multiplied by the number of parallel transistors. The other switching losses are unchanged since

$$\frac{P_{\text{sw(parallel)}}}{P_{\text{sw(single)}}} = n\frac{\int_0^{DT}\left(v_{\text{D}}\cdot\frac{i_{\text{D}}}{n}\right)dt}{\int_0^{DT}(v_{\text{D}}\cdot i_{\text{D}})dt} = 1. \tag{4.23}$$

The PSFBVD topology with the lowest switching losses gains the most advantage from transistor paralleling since the conduction losses, which can be effectively reduced, are the only dominating source of losses. The full-bridge boost topology having the lowest conduction losses and moderate switching losses (mostly turn-off losses) can have the most cost effective transistor setup when using single transistors or moderate paralleling.

The advantages of transistor paralleling in the PSFB topology are diminished by the large switching losses especially in transistors S_1 and S_3 due to the circulating leakage inductance current and the large turn-off current. The advantages of full zero voltage switching is questionable, as the increase in the leakage inductance results in increased overall losses.

The transistors conducting most of the current in the ZVS boost and RPP topologies are S_1 and S_2, and it is beneficial to parallel only these transistors, provided that the clamp transistor current remains reasonable. The result of this is that the ZVS boost and RPP topologies have a smaller number of transistors for the same level of paralleling than the bridge topologies. This is seen as lower initial costs. However, since the transistor currents are slightly higher and since higher $R_{\text{DS(on)}}$ devices must be used, the lower initial costs are overshadowed by higher operating costs in the long run.

Table 4.11: Example of the effect of Si diode paralleling on losses and costs.

Topology	**Diodes**	**Losses [W]**	**Initial cost [€]**	**Cost/5 a [€]**	**Cost/10 a [€]**
PSFB, partial ZVS	8/16/32	261/255/213	66/132/264	1021/1065/1043	1975/1997/1822
PSFB, full ZVS	8/16/32	209/203/174	66/132/264	830/875/901	1595/1617/1537
PSFBVD	2/4/6	62/54/51	17/33/50	243/231/236	470/428/423
FB boost	4/8/12	105/102/87	33/66/99	417/439/417	801/812/735
ZVS boost	4/8/12	80/71/67	26/53/79	319/312/324	611/572/569
RPP	2/4/6	62/54/51	17/33/50	243/231/236	470/428/423

The large number of required diodes in the PSFB topology results in high initial costs and losses. The large *di*/*dt* when using partial zero voltage switching increases the switching losses, leading to total losses and costs higher than in full zero voltage switching. The hard switched full-bridge boost topology suffers from reverse recovery effects and thus the switching losses overshadow the low conduction losses.

The PSFBVD and RPP topologies utilizing zero current diode switching have very low losses and costs since the only dominating losses are conduction losses and the Si diodes are relatively low-cost. The ZVS boost, although having double the amount of diodes, can use less expensive low voltage diodes, which typically have better forward characteristics than their high voltage counterparts having the same current rating. This decreases the cost difference compared to other voltage doubler topologies.

Table 4.12: Example of the effect of SiC diode paralleling on losses and costs.

Topology	Diodes	Losses [W]	Initial cost [€]	Cost/5 a [€]	Cost/10 a [€]
PSFB, partial ZVS	8/16/32	169/130/117	393/785/1570	1011/1261/1998	1629/1736/2426
PSFB, full ZVS	8/16/32	179/135/121	393/785/1570	1047/1279/2013	1702/1773/2455
PSFBVD	2/4/6	163/104/85	98/196/294	694/577/605	1290/957/916
FB boost	4/8/12	98/74/67	196/393/589	555/663/834	913/934/1079
ZVS boost	4/8/12	189/119/97	83/167/250	775/602/605	1466/1037/959
RPP	2/4/6	163/104/85	98/196/294	694/577/605	1290/957/916

The advantages of paralleling with SiC diodes in terms of overall losses are more obvious than with Si diodes. However, since the SiC devices are much more expensive than their Si counterparts, the improved efficiency in the hard switched topologies cannot compensate the increase in the initial costs even in a ten year time span. The difference between the diode bridge losses and the voltage doubler diode losses is reduced as the number of parallel diodes is increased. The reasons for this are analyzed next.

The ratio of conduction losses between a single diode and parallel diodes can be derived as follows:

$$\frac{P_{\text{cond(parallel)}}}{P_{\text{cond(single)}}} = \frac{n\left(V_{\text{D}}\frac{I_{\text{D(avg)}}}{n} + R_{\text{D}}\left(\frac{I_{\text{D(rms)}}}{n}\right)^2\right)}{V_{\text{D}}I_{\text{D(avg)}} + R_{\text{D}}I_{\text{D(rms)}}^{\ 2}} = \frac{nV_{\text{D}}I_{\text{D(avg)}} + R_{\text{D}}I_{\text{D(rms)}}^{\ 2}}{n\left(V_{\text{D}}I_{\text{D(avg)}} + R_{\text{D}}I_{\text{D(rms)}}^{\ 2}\right)}. \tag{4.24}$$

The reduction in diode conduction losses for a certain level of paralleling is smaller with diodes than with MOSFETs. The capacitive switching losses for a single diode are multiplied with the number of parallel diodes to obtain the total capacitive losses. The reverse recovery *di*/*dt* is divided by the number of parallel diodes as well as the forward current at turn-off. This leads to a reduced reverse recovery charge depending on the diode characteristics. In the calculation examples, it is assumed that the reverse recovery charge is halved each time an extra diode is added. This leads to identical reverse recovery losses with single and multiple diodes.

The ratio of the conduction losses between the diode bridge and voltage doubler topologies, if considering an ideal case in the full-bridge boost topology, is

$$\frac{P_{\text{cond(DB)}}}{P_{\text{cond(VD)}}} = \frac{4n\left(V_{\text{D}}\frac{I_{\text{D(avg)}}}{n} + R_{\text{D}}\left(\frac{I_{\text{D(rms)}}}{n}\right)^2\right)}{2n\left(V_{\text{D}}\cdot\frac{2I_{\text{D(avg)}}}{n} + R_{\text{D}}\left(\frac{2I_{\text{D(rms)}}}{n}\right)^2\right)} = 1 - \frac{R_{\text{D}}{I_{\text{D(rms)}}}^2}{nV_{\text{D}}I_{\text{D(avg)}} + 2R_{\text{D}}{I_{\text{D(rms)}}}^2}. \quad (4.25)$$

If the average and RMS currents from Table 4.8 are inserted into (4.25) and if there are no parallel diodes, the calculated conduction loss ratio is 0.88. If there are two diodes in parallel, the ratio is increased to 0.93, indicating that the diode bridge conduction losses approach the conduction losses of the voltage doubler when the number of parallel diodes is increased. The diode forward characteristics have a strong impact on the loss ratio, and therefore, diodes having a large V_{D} and R_{D} benefit more from paralleling than diodes with a low voltage drop. The ratio with a single IDH15S120 SiC diode is 0.647, and with two parallel diodes, the ratio is 0.73.

The peak of a sinusoidal current segment compared to the peak of a square segment, if both have the same length of (1-*D*)**T* and the same average, is

$$\frac{I_{\text{peak(sinusoidal)}}}{I_{\text{peak(square)}}} = -\frac{\omega_r T(D-1)}{2\sin\left[\frac{\omega_r T(D-1)}{2}\right]^2}. \quad (4.26)$$

Now, if ω_{r} is $\pi/((1\text{-}D)^*T)$, in which case the pulses have the same length, the ratio becomes 1.5708. If the ratio of the RMS currents is calculated with this peak current ratio, the ratio becomes

$$\frac{I_{\text{rms(sinusoidal)}}}{I_{\text{rms(square)}}} = \frac{\sqrt{\frac{1}{T}\int_0^{(1-D)T}\left[\frac{I_{\text{peak(sinusoidal)}}}{I_{\text{peak(square)}}}I_{\text{peak(square)}}\sin\left(\frac{\pi}{(1-D)T}t\right)\right]^2 dt}}{\sqrt{\frac{1}{T}\int_0^{(1-D)T}{I_{\text{peak(square)}}}^2}} = \frac{\sqrt{-{I_{\text{peak(square)}}}^2\cdot\left(\frac{I_{\text{peak(sinusoidal)}}}{I_{\text{peak(square)}}}\right)^2(2D-2)}}{2\sqrt{-{I_{\text{peak(square)}}}^2(D-1)}}. \quad (4.27)$$

The RMS of a sinusoidal current segment is thus 1.11 times larger than that of a square segment having the same average. The ratio between the RMS currents of a sinusoidal segment and a square segment including a linear ripple component is

$$\frac{I_{\text{rms(sinusoidal)}}}{I_{\text{rms(square with ripple)}}} = \frac{\sqrt{\frac{1}{T}\int_0^{(1-D)T}\left[\frac{I_{\text{peak(sinusoidal)}}}{I_{\text{peak(square)}}} I \sin\left(\frac{\pi}{(1-D)T} t\right)\right]^2 dt}}{\sqrt{\frac{(1-D)T}{T}\cdot\frac{1}{3}\left((I-\Delta I)^2+(I-\Delta I)\cdot(I+\Delta I)+(I+\Delta I)^2\right)}} = \frac{\sqrt{-I^2\cdot\left(\frac{I_{\text{peak(sinusoidal)}}}{I_{\text{peak(square)}}}\right)^2(6D-6)}}{\sqrt{2\left[-(3I^2+\Delta I^2)(D-1)\right]}} \quad (4.28)$$

Current I in (4.28) is the peak current of a square pulse having the same average as the pulse with the ripple component, and ΔI is half of the peak-to-peak current ripple. The larger the ripple, the smaller the RMS current difference between the sinusoidal segment and the square segment with a ripple component.

The conclusion of the RMS current and conduction loss analysis is that rectifier diodes in the topologies utilizing sinusoidal resonance are always less effective than in the topologies having square wave current waveforms with a ripple, unless the ripple component is very large. As the doubled average current and the increased RMS current in the voltage doubler topologies utilizing sinusoidal resonance are taken into account, the conduction losses compared to the FB boost topology using a diode bridge are

$$\frac{P_{\text{cond(DB)}}}{P_{\text{cond(VD)}}} = \frac{4n\left(V_{\text{D}}\frac{I_{\text{D(avg)}}}{n}+R_{\text{D}}\left(\frac{I_{\text{D(rms)}}}{n}\right)^2\right)}{2n\left(V_{\text{D}}\cdot\frac{2I_{\text{D(avg)}}}{n}+R_{\text{D}}\left(\frac{2I_{\text{D(rms)}}\cdot\frac{I_{\text{rms(sinusoidal)}}}{I_{\text{rms(square with ripple)}}}}{n}\right)^2\right)} = \frac{nV_{\text{D}}I_{\text{D(avg)}}+R_{\text{D}}{I_{\text{D(rms)}}}^2}{nV_{\text{D}}I_{\text{D(avg)}}+2R_{\text{D}}{I_{\text{D(rms)}}}^2\left(\frac{I_{\text{rms(sinusoidal)}}}{I_{\text{rms(square with ripple)}}}\right)^2} \quad (4.29)$$

The final form of (4.29) assumes that diodes with the same parameters are used. When using the average and RMS current from Table 4.8, the conduction loss ratio with one DSEI30-10A Si diode is 0.63 and with two diodes 0.73. The corresponding ratios with the IDH15S120 SiC diode are 0.556 and 0.645, respectively. It is thus concluded that the diode bridge can be made more efficient than a voltage doubler by using similar diodes. In the voltage doubler configuration, the capacitor losses must be added to the loss budget, which increases the difference even further.

The minimum losses and minimum cost configurations from the preceding examples are summarized in Table 4.13.

Table 4.13: Minimum loss and minimum cost configuration for the compared topologies.

Topology	Parallel transistors, min loss	Parallel diodes, min loss	Losses [W]	Parallel transistors, min cost	Parallel diodes, min cost	Cost/10 a [€]
PSFB, partial ZVS	3	3 (SiC)	331	3	1 (SiC)	2692
PSFB, full ZVS	3	3 (SiC)	357	3	3 (Si)	3417
PSFBVD	3	3 (Si)	107	3	3 (Si)	1067
FB boost	3	3 (SiC)	156	3	3 (Si)	1535
ZVS boost	3	3 (Si)	177	3	3 (Si)	1442
RPP	3	3 (Si)	161	3	3 (Si)	1296

The functionality of Si diodes when connecting them in parallel requires that the forward characteristics are very similar and that the thermal connection between the diodes is good. If SiC diodes are used to ensure current sharing, the diode bridge topologies may become more expensive over time when adding diodes in parallel. The voltage doubler topologies can have fewer costs over a ten year period when the number of parallel diodes is increased.

4.5 Summary

It has been demonstrated that the turn-on losses, if considering only the transitions between voltage and current, are relatively small in the galvanically isolated, high current DC-DC converters. It was demonstrated that even a small common-source inductance will slow down the switching process to a larger extent than the stray inductances on the drain if the inductance values are in the same range. This was shown also in the study by Xiao et al. (2004). If the transistor body diodes are involved in the turn-on process, the losses for these diodes need to be considered in the overall turn-on losses. In the basic phase-shifted full-bridge converter, the circulating leakage inductance current used to generate zero voltage turn-on for the primary transistors generates additional conduction losses in the primary freewheeling diodes. These losses can decrease the overall efficiency. The output rectifier diode conduction losses are also increased if the leakage inductance is increased in order to widen the zero voltage switching range. Obtaining a sufficiently large leakage inductance for the ZVS in high current transformers may be cumbersome since the number of primary turns has to be low and the winding width has to be large in order to avoid excessive winding losses. The number of primary-secondary intersections may also have to be increased in order to reduce the AC resistances in the windings. All of these constraints tend to reduce the leakage inductance, as seen from (5.44).

The conduction losses in the resonant topologies are inherently higher than in the hard switched topologies due to an increased RMS current, while having the same average current. The ZVS boost and resonant push-pull topology require transistors with a higher voltage rating than the other compared topologies and this narrows the range of available devices with low $R_{DS(on)}$. The

advantage in the ZVS boost and RPP topologies is that the largest part of conduction losses are caused by a minimum of two transistors, whereas the conduction losses in the bridge topologies are generated by at least four transistors.

The turn-off losses can be minimized with high current switching speed, which can be achieved by small transformer leakage inductance, small stray inductances in the circuit layout and by transistors having a small common-source inductance. The current-fed topologies gain significant advantage over the voltage-fed topologies in turn-off since the current-fed topologies are turned off with half the current, when operating with $D > 0.50$. The leakage inductance of the phase-shifted full-bridge determines the current at which transistors S_2 and S_4 (lagging leg) are turned off. With a small leakage inductance these transistors can be zero current switched and the turn-off losses can thus be neglected. In low current applications the rate at which the transistor output capacitors are charged to the off-state voltage can be slow compared to the transistor turn-off speed (current fall rate), but in high current applications the drain-source voltage rises rapidly, thus resulting in large turn-off losses.

It has been shown that a diode bridge rectifier is more efficient than a voltage doubler rectifier, although the difference is reduced as diodes are paralleled. It has also been shown that topologies carrying sinusoidal currents have inherently larger diode conduction losses than the topologies having trapezoidal current waveforms if the average currents are identical.

Silicon carbide diodes have superior switching characteristics compared to Si diodes and the hard switched topologies gain a large benefit in terms of reduced switching losses. The resonant topologies capable of zero current switching do not benefit from SiC diodes, unless the forward voltage drop is lower or equal than the voltage drop of a comparable Si diode. The SiC diodes gain an advantage when paralleling, as the positive temperature coefficient helps to ensure that the current is distributed equally between the parallel diodes. The current high cost of the SiC diodes need to be taken into account when evaluating the most cost efficient rectifier solution for each topology.

5 Magnetic component scaling issues

This chapter presents the magnetic component design and scaling considerations in the isolated DC-DC converters presented in this thesis.

5.1 Calculation of inductor parameters and losses

This section presents the methods used in this thesis to calculate inductor losses. The core materials selected for the study are the amorphous iron-based magnetic alloy 2605SA1 from Metglas and the KoolMu powder cores from Magnetics. Both core materials have low core losses at high frequencies and a high saturation density, which is favorable for a high current DC choke.

5.1.1 Gapped inductors using amorphous cores

The inductance-current product of an inductor can be expressed in terms of inductor turns and the peak flux as

$$L\hat{I} = N\hat{\phi}, \tag{5.1}$$

where the flux is a product of the core area A_c and maximum flux density B_{max} as $\hat{\phi} = A_c B_{max}$. The peak current is used instead of RMS current to ensure that the inductor can conduct the current ripple without saturating. The number of turns required for a desired inductance can now be expressed as

$$N = \frac{L\hat{I}}{A_c B_{max}}. \tag{5.2}$$

An air gap is needed to control the inductor DC flux under bias. The larger the air gap the smaller the DC flux if the inductor current remains unchanged. The required air gap length in centimeters can be determined from (Metglas, n.d.)

$$l_g = \frac{0.4\pi N\hat{I}\left(10^{-4}\right)}{B_{max}} - \frac{l_m}{\mu\Delta}, \tag{5.3}$$

where l_m is the core magnetic path length in cm and $\mu\Delta$ is an incremental permeability factor which is equal to ΔB (Gauss)/ΔH (Oersted) in the operating area. The presence of the air gap results in some of the flux inducing outside of the gap and this fringing flux decreases the effective air gap length. To compensate the effect of the fringing flux a correction factor can be defined as (McLyman, 2004)

$$F = 1 + \frac{l_g}{\sqrt{A_c}} \ln\frac{2G}{l_g} \tag{5.4}$$

The fringing flux factor indicates how much the inductance value is increased due to a decrease in the air gap length. The winding width G is dependent on the core geometry, as can be seen in Figure 5.1.

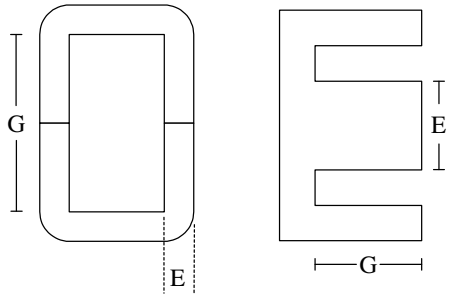


Figure 5.1: Definition of winding width G and tongue width E for C and E cores.

The fringing flux corrected number of turns can now be calculated as (Metglas, n.d.)

$$N = \sqrt{\frac{L \cdot \left(l_{\mathrm{g}} + \frac{l_{\mathrm{m}}}{\mu\Delta} \right) \cdot 10^{8}}{0.4\pi A_{\mathrm{c}} F}}, \tag{5.5}$$

According to McLyman (2004) the losses due the air gap can be approximated as

$$P_{\mathrm{g}} = K_{\mathrm{i}} E l_{\mathrm{g}} f B_{\mathrm{ac}}{}^{2}, \tag{5.6}$$

where E is the tongue width as defined in Figure 5.1 (in cm) and K_{i} is a constant which depends on the winding and core configuration according to Table 5.1. It was stated by Rylko et al. (2011) that (5.6) will result in overestimated gap losses when the gap length is increased in cores with very thin laminations and high resistivity. However, no actual modifications were proposed to (5.6). The cores requiring a large air gap for a certain DC flux are relatively small in area, and therefore, the cores are likely to be winding and core loss limited before they are gap loss limited. When the inductor core is selected with an adequate area product considering the operating conditions, the gap losses will be small in proportion even if there is some overestimation.

Table 5.1: Gap loss coefficient with various winding and core configurations (McLyman, 2004).

Configuration	K_{i}
Coil in both tongues of a C core	0.0388
Coil in one tongue of a C core	0.0775
Laminated core	0.1550

The AC flux density is calculated based on the resulting inductor current ripple $r \in [0,1]$ as

$$B_{\mathrm{ac}} = \frac{0.4\pi N \frac{rI_{\mathrm{dc}}}{2} \cdot 10^{-4}}{l_{\mathrm{g}}} \tag{5.7}$$

The inductor core losses are calculated by using a curve fit equation provided for the 2605SA1 material (Metglas, n.d.)

$$P_{\mathrm{c}} = \left(6.5 f^{1.51} B_{\mathrm{ac}}{}^{1.74}\right) m_{\mathrm{c}}, \tag{5.8}$$

where f is the ripple frequency in kHz seen by the inductor and m_{c} is the core mass in kg.

The AC winding losses are divided into skin effect and proximity losses and calculated using the same methods as the transformer losses. The inductor RMS current is calculated using the RMS equation for DC current with a linear ripple component

$$I_{\mathrm{rms}} = I_{\mathrm{dc}} \sqrt{1 + \frac{1}{3}\left(\frac{0.5\left(I_{\mathrm{dc(max)}} - I_{\mathrm{dc(min)}}\right)}{I_{\mathrm{dc}}}\right)^2} \tag{5.9}$$

The DC losses are obtained by calculating the resistance per unit length and calculating the winding length by calculating the mean turn length, which is the length of a turn at the center of the winding window. The length of the turns on the top of the winding is then slightly overestimated and the length of the turns at bottom slightly underestimated. It is assumed that the specified winding width for each core has been fully utilized, whereas the utilization of the window height is limited by the maximum fill factor.

5.1.2 Non-gapped inductors using powder cores

The required number of turns for the desired inductance can be calculated using the inductance factor A_{L} (nH/1000 turns or nH/T^2), if provided by the manufacturer. The number of turns can be calculated from (Magnetics, 2011)

$$N = \sqrt{\frac{10^9 L}{(100\% - \Delta A_{\mathrm{L}}) A_{\mathrm{L}}}}, \tag{5.10}$$

where ΔA_{L} is the worst case negative tolerance for the inductance factor A_{L}.

In order to find out the remaining core permeability at the operating point, the DC bias H needs to be calculated

$$H\left[\frac{A \cdot T}{cm}\right] = \frac{NI_{\mathrm{DC}}}{l_{\mathrm{m}}}, \tag{5.11}$$

where l_{m} is the core magnetic path length in cm. The initial permeability μ_{i} often given in the material datasheets refers to the relative permeability μ_{r} at low values of B (below 0.1 T). As the electric field H is increased, the relative permeability of the material decreases. The degree of

the change in relative permeability as a function of the applied field is specific to the core material and its initial permeability. Figure 5.2 shows an example of the permeability behavior of the KoolMμ material.

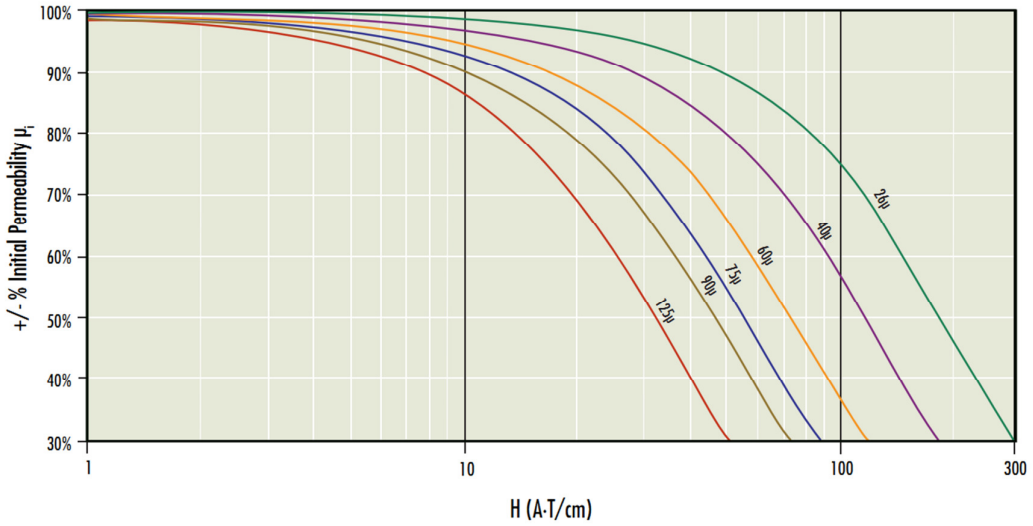


Figure 5.2: Change in the initial permeability in the KoolMμ material as a function of the applied electric field (Magnetics, 2011).

After the DC bias is calculated, the corresponding relative permeability can be calculated with a curve fit formula, which in the case of Magnetics cores is (Magnetics, 2011)

$$\mu\left[per\,unit\right] = a + bH + cH^2 + dH^3 + eH^4 \tag{5.12}$$

The coefficients used for the KoolMu material are listed in Table 5.2.

Table 5.2: Coefficients for the permeability curve fit formula for the KoolMu material (Magnetics, 2011).

μ_i	*a*	*b*	*c*	*d*	*e*
26 μ	1	-1.248E-3	-2.020E-5	8.354E-8	-9.503E-11
40 μ	1	-2.799E-3	-3.312E-5	2.126E-7	3.466E-10
60 μ	1	-4.445E-5	-8.763E-5	9.446E-7	-2.616E-9
75 μ	1	-6.120E-3	-1.380E-4	1.943E-6	-6.956E-9
90 μ	1	-9.031E-3	-1.218E-4	2.254E-6	-9.287E-9
125 μ	1	-9.918E-3	-5.044E-4	1.267E-5	-8.284E-8

Due to decrease in permeability the initially calculated number of turns needs to be increased in order to obtain the desired inductance:

$$N_{corr} = \frac{N}{\mu\,[per\ unit]}. \tag{5.13}$$

In order to determine the final inductance the resulting DC bias is calculated using the corrected number of turns

$$H\left[\frac{A \cdot T}{cm}\right] = \frac{N_{\mathrm{corr}} I_{\mathrm{DC}}}{l_{\mathrm{m}}}. \tag{5.14}$$

The resulting inductance is then

$$L\,[\mu H] = \frac{\mu\,[per\ unit]\left[(100\,\% - \Delta A_{\mathrm{L}})A_{\mathrm{L}} N_{\mathrm{corr}}{}^{2}\right]}{10^{9}}. \tag{5.15}$$

The maximum and minimum electric field seen by the inductor is

$$\begin{aligned} H_{\min}\left[\frac{A \cdot T}{cm}\right] &= \frac{N_{\mathrm{corr}}}{l_{\mathrm{m}}}\left(I_{\mathrm{dc}} + \frac{rI_{\mathrm{dc}}}{2}\right) \\ H_{\max}\left[\frac{A \cdot T}{cm}\right] &= \frac{N_{\mathrm{corr}}}{l_{\mathrm{m}}}\left(I_{\mathrm{dc}} - \frac{rI_{\mathrm{dc}}}{2}\right) \end{aligned}. \tag{5.16}$$

The flux in the inductor core is related to the relative permeability μ_{r}, vacuum permeability μ_0 and applied field H as follows:

$$B = \mu_r \mu_0 H. \tag{5.17}$$

The resulting flux swing can also be calculated using the magnetization curves and curve fit equations provided by Magnetics so that

$$\begin{aligned} B_{\min} &= \left(\frac{a + bH_{\min} + cH_{\min}{}^{2}}{1 + dH_{\min} + eH_{\min}{}^{2}}\right)^{x} \\ B_{\max} &= \left(\frac{a + bH_{\max} + cH_{\max}{}^{2}}{1 + dH_{\max} + eH_{\max}{}^{2}}\right)^{x} \end{aligned}. \tag{5.18}$$

The coefficients for the magnetization curves with KoolMμ cores are presented in Table 5.3.

Table 5.3: Coefficients for the magnetization curve fit formula for the KoolMμ material (Magnetics, 2011).

μ_i	*a*	*b*	*c*	*d*	*e*	*x*
26 μ	5.868E-05	9.362E-05	9.011E-06	-3.682E-04	8.747E-06	0.5
40 μ	8.870E-05	5.592E-05	2.700E-05	2.928E-04	2.574E-05	0.5
60 μ	1.658E-04	2.301E-05	7.297E-05	5.906E-03	6.053E-05	0.5
75 μ	1.433E-05	9.724E-05	1.323E-04	7.255E-03	1.131E-04	0.5
90 μ	5.660E-04	-1.216E-04	1.974E-04	7.278E-03	1.698E-04	0.5
125 μ	7.808E-05	5.088E-04	2.595E-04	3.922E-03	2.285E-04	0.5

The resulting AC flux density in the inductor core is

$$B_{\mathrm{ac}} = \frac{B_{\max} - B_{\min}}{2}. \tag{5.19}$$

Knowing the AC flux density, the inductor core loss density can be calculated using the curve fit equation

$$P_{\mathrm{cld}}\left[\frac{mW}{cm}\right] = aB_{\mathrm{ac}}{}^{b} f^{c}, \tag{5.20}$$

where the ripple frequency f is in kHz and the coefficients for KoolMμ material are as expressed Table 5.4.

Table 5.4: Coefficients for the core loss density curve fit formula for the KoolMμ material (Magnetics, 2011).

μ_i	*a*	*b*	*c*
26 μ	120	2.09	1.46
40 μ	120	2.09	1.46
60 μ	193	2.01	1.29
75 μ	193	2.01	1.29
90 μ	193	2.01	1.29
125 μ	91.58	2.2	1.63

As the core loss density is known, the actual core loss can be calculated from

$$P_{\mathrm{c}}\,[W] = \frac{P_{\mathrm{cld}} l_{\mathrm{m}} A_{\mathrm{c}}}{1000}. \tag{5.21}$$

The AC and DC winding losses are calculated in the same manner as with the gapped cores.

5.2 Inductor design approaches

Four different inductor design approaches are studied in a 10 kW system with a nominal input voltage of 50 V, a switching frequency of 50 kHz and a duty cycle of 57%. The inductor design approaches are applied in five different topologies, which are phase-shifted full-bridge (PSFB), phase-shifted full-bridge with a voltage doubler (PSFBVD), full-bridge boost, ZVS boost and resonant push-pull (RPP). In the voltage-fed PSFB and PSFBVD topologies the inductor is on the secondary side and in the PSFBVD topology the output inductor can be neglected, as the voltage doubler capacitors form an LC-filter together with the leakage inductance.

The minimum inductor loss for each topology is found by sweeping through all of the available cores and selecting the minimum loss from among the configurations in which the inductance is near the desired value. The current density is at the design point which results in minimum overall losses. The following assumptions are made in the inductor design:

- Copper foil or stranded conductor winding is used;
- The foil width equals to either bobbin width or core winding window width;
- The maximum number of parallel solid conductors is three and the conductors are twisted together for uniform current distribution;
- The stranded conductor is Radox GKW with the cable dimensions specified in the manufacturer datasheets;
- The maximum fill factor including the insulations is 90%;
- The maximum DC flux density is 1 T.
- The maximum core temperature does not exceed 100°C , thus allowing the neglect of the temperature effects;
- The initial temperature is 25°C.

The main limitations to the applicability of various cores in each case are:

- The smallest cores may not be able to fit enough turns at low current densities to obtain the desired inductance, which leads to high DC winding losses.
- The cores may not be able to maintain permeability and thus the required inductance in case there is a large number of turns and a high current (high DC bias).
- The losses increase the core temperature excessively.

The core numbering and corresponding core types used in the analysis are listed in Table 5.5. The masses for the E cores are given only for a permeability of 26μ because the masses are given for comparison only and the mass variation between different permeabilities is small.

Table 5.5: Core numbering and the corresponding core types.

Core number	Metglas C core type	Area [cm^2]	Mass [g]	Magnetics E core type	Area [cm^2]	Mass [g]
1	AMCC 4	1.11	99	00K1808E	0.228	2.61
2	AMCC 6.3	1.6	154	00K2510E	0.385	6.75
3	AMCC 8	1.8	172	00K3007E	0.601	11.3
4	AMCC 10	1.8	198	00K3515E	0.84	15.6
5	AMCC 16A	2.3	248	00K4017E	1.28	31.1
6	AMCC 16B	2.3	281	00K4020E	1.83	48.0
7	AMCC 20	2.7	337	00K4022E	2.37	63.3
8	AMCC 25	2.7	379	00K4317E	1.52	33.1
9	AMCC 32	3.2	454	00K5528E	3.5	115.9
10	AMCC 40	3.7	530	00K5530E	4.17	139.7
11	AMCC 50	3.3	586	00K6527E	5.4	213.3
12	AMCC 63	3.9	703	00K7228E	3.68	143.0
13	AMCC 80	5.2	938	00K8020E	3.89	197.0
14	AMCC 100	5.9	1055	00K8044E	3.89	222
15	AMCC 168S	3.35	1101	00K130LE	10.8	618.0
16	AMCC 125	5.5	1166	00K160LE	7.78	516
17	AMCC 160	6.2	1333	-		
18	AMCC 200	7.8	1666	-		
19	AMCC 367S	5.29	1668	-		
20	AMCC 250	9.3	2095	-		
21	AMCC 320	9	2167	-		
22	AMCC 400	11.7	2817	-		
23	AMCC 500	11.3	2890	-		
24	AMCC 630	14.3	3678	-		
25	AMCC 800A	17.4	4466	-		
26	AMCC 800 B	21.0	5972	-		
27	AMCC 1000	23.0	7109	-		

The maximum losses for a given temperature rise for each core are calculated according to the dimensions shown in Figure 5.3.

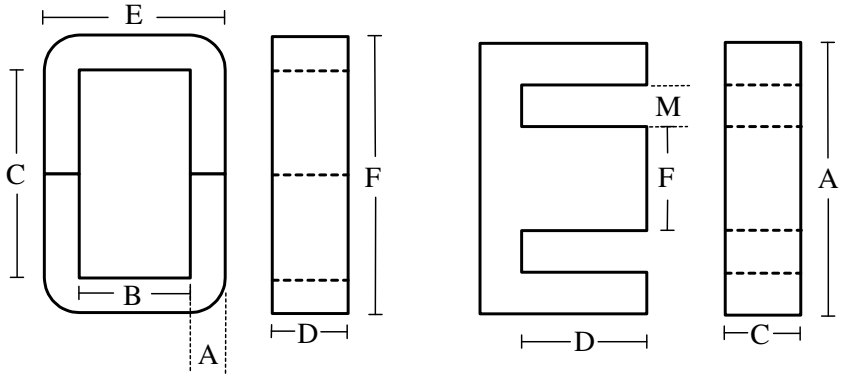


Figure 5.3: Core dimensions for the C and E cores as given in the manufacturer datasheets.

The temperature rise for a core under natural convection can be estimated from the total power losses P_{tot} and the core surface area SA as (Magnetics, 2011; Metglas)

$$\Delta T\left[^{\circ}C\right]=\left(\frac{P_{tot}\left[mW\right]}{SA\left[cm^2\right]}\right)^{0.833} \tag{5.22}$$

For C cores the surface area can be calculated from (Metglas)

$$SA = 2F(B+D)+2(B+D)(B+E)+2F(B+E) \tag{5.23}$$

and when using E cores from Magnetics the surface area can be calculated from

$$SA = 4(AB + AC + BC + 2CD + DF - 2DM). \tag{5.24}$$

The given temperature rise estimation does not take the winding into account, and therefore, the resulting surface area is slightly smaller than in the actual wound component. However, taking only the core surface area into account, a worst case scenario for the temperature rise is obtained. Table 5.6 presents the calculated surface areas for the studied cores and the allowable power losses P_{tot} for a temperature rise of 75 °C.

Table 5.6: Calculated surface areas for the studied cores and allowable power losses for a temperature rise of 75 °C.

Core number	Metglas C core	Surface area [cm^2]	P_{tot} [W]	Magnetics E core	Surface area [cm^2]	P_{tot} [W]
1	AMCC 4	83.0	6.2	00K1808E	12.6	0.9
2	AMCC 6.3	103.4	7.8	00K2510E	20.2	1.5
3	AMCC 8	115.9	8.7	00K3007E	34.0	2.6
4	AMCC 10	132.1	9.9	00K3515E	42.6	3.2
5	AMCC 16A	143.1	10.7	00K4017E	72.7	5.5
6	AMCC 16B	160.3	12.0	00K4020E	90.0	6.7
7	AMCC 20	172.3	12.9	00K4022E	107.2	8.0
8	AMCC 25	202.2	15.2	00K4317E	64.6	4.8
9	AMCC 32	216	16.2	00K5528E	156.2	11.7
10	AMCC 40	230	17.3	00K5530E	175.3	13.1
11	AMCC 50	303.5	22.8	00K6527E	234.1	17.6
12	AMCC 63	321	24.1	00K7228E	174.3	13.1
13	AMCC 80	356	26.7	00K8020E	237.7	17.8
14	AMCC 100	373	28.0	00K8044E	268.6	20.1
15	AMCC 168S	687.5	51.6	00K130LE	554.8	41.6
16	AMCC 125	464	34.8	00K160LE	535.8	40.2
17	AMCC 160	485	36.4	-		
18	AMCC 200	526	39.5	-		
19	AMCC 367S	1161.1	87.1	-		
20	AMCC 250	592	44.4	-		
21	AMCC 320	707	53.0	-		
22	AMCC 400	780	58.5	-		
23	AMCC 500	854.5	64.1	-		
24	AMCC 630	934	70.1	-		
25	AMCC 800A	1013	76.0	-		
26	AMCC 800 B	1171	87.8	-		
27	AMCC 1000	1292	96.9	-		

5.2.1 Minimum inductance over defined load range

The definition for an acceptable level of high frequency current ripple is not very clear. Low frequency ripple is generally considered harmful, as it can cause overloading peaks where the reactants run out from the cells and it can also force the fuel cell stack out of the normal, ohmic operating area. It was also reported by Pradhan et al. (2007) that a low frequency ripple current increased the area specific resistance in the fuel cell stack, which decreased the power output and efficiency. The following specifications have been given for ripple in a typical fuel cell (not necessarily SOFC) power conditioning system for standalone U.S. loads (Handbook, 2004):

- 60 Hz ripple: < 10% of a 10% to 100% load range;
- 120 Hz ripple: < 15% of a 10% to 100% load range;
- > 10 kHz ripple: < 60% of a 10% to 60% load range.

Moon et al. (2006) specified the maximum low frequency current ripple to be under 5.6% peak-to-peak in order to avoid the SOFC balance of plant controller instability. The effects of a high frequency current were not covered.

Studies conducted by Acharya et al. (2003) and Mazumder et al. (2004) suggest that the high frequency ripple has a negligible effect on the SOFC in a short time frame. Pradhan et al. (2007) have stated that high frequency ripple had an effect on the electrochemical impedance of the investigated planar SOFC, but the impact on performance was negligible since the ripple time constants were much smaller than the electrochemical time constants of the SOFC.

The high frequency current ripple limit is specified to be < 15% over a load range of 20%-100%. The inductors are realized with Magnetics E cores by starting with the required inductance at a 20% load and allowing a reduction in the initial permeability at the maximum current so that the minimum inductance is still met. The resulting input current ripple depends on the resonant frequency of the LCL filter formed at the converter input by the source impedance (including both internal and external cabling), the input capacitors and the boost inductor. If the source impedance is small, large capacitors are needed in order to damp the high frequency current ripple to an acceptable level. The current stress on the input capacitors can be quite high and the requirement for low ESR is obvious in order to minimize additional losses and reliability problems.

Table 5.7: Minimum inductor sizes and peak-to-peak current ripples for various topologies in a 10 kW system. The design approach is to limit the HF current ripple to ≤ 15% at a load range of 20-100%.

Topology	**Inductance (20%/100%)**	**Ripple frequency**	**Inductor current ripple pk-pk (20%/100%)**	**Inductor DC current (20%/100%)**
PSFB	1720 µH /515 µH	100 kHz	15%/15%	3 A/15 A
FB Boost	11.9 µH/2.38 µH	100 kHz	15%/15%	40 A/200 A
ZVS Boost	190 µH/38 µH	50 kHz	15%/15%	20 A/100 A
RPP	11.9 µH/2.38 µH	100 kHz	15%/15%	40 A/200 A

The nominal ripple of the ZVS boost refers to the ripple of an individual inductor. In the ZVS boost topology the ripple for an individual inductor is higher than the input current ripple, as the input current ripple is reduced by interleaved operation. The inductor current in the ZVS boost topology is half the total input current.

An example of the inductor losses with various powder cores in a 10 kW resonant push-pull converter are presented in Figure 5.4. The specifications for part load and full load inductances are described in Table 5.7.

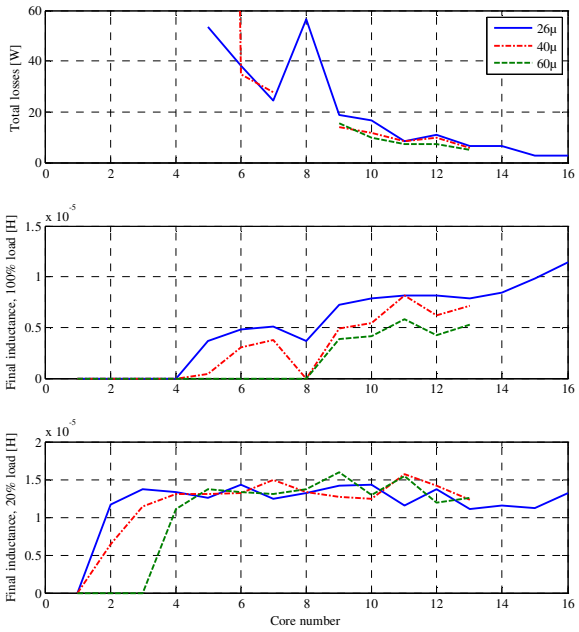


Figure 5.4: Losses for powder E core inductors satisfying both 20% load and 100% load inductance requirements.

The lowest losses of are obtained with core number 16 having a permeability of 26µ. The final inductance 11.4 µH is quite large and results in full load current ripple of 3.1%, which is much smaller than the allowed 15%. This is seen as smaller AC winding losses and core losses than would result from the minimum inductance. The smallest usable core having the lowest losses is core number 10 with a permeability of 60µ. The loss breakdown of these two inductors is presented in Table 5.8. The upper loss values on a row are for foil winding and the lower loss values are for solid conductor winding.

Table 5.8: Loss breakdown for Magnetics E cores satisfying the inductance criteria for both 20% and 100% loads. The single inductor losses in the ZVS boost topology are doubled in order to obtain the total losses.

Topology	Core	Turns	DC loss	AC loss	Core loss	Total
PSFB (1)	- 16 (26µ)	- 104 (2 x 2.5 mm^2)	- 19 W	- 0.004 W	- 0.16 W	- 20 W
PSFB (2)	- 16 (26µ)	- 104 (2 x 2.5 mm^2)	- 19 W	- 0.004 W	- 0.16 W	- 20 W
ZVS Boost (1)	16 (26µ) -	36 -	15.7 W -	10.7 W -	0.18 W -	53.2 W -
ZVS Boost (2)	16 (26µ) -	36 -	15.7 W -	10.7 W -	0.18 W -	53.2 W -
FB Boost & RPP (1)	16 (26µ) 16 (26µ)	8 8 (3 x 35 mm^2)	1.8 W 12 W	0.57 W 0.1 W	0.13 W 0.1 W	2.5 W 12.7 W
FB Boost & RPP (2)	10 (60µ) 16 (26µ)	9 8 (3 x 35 mm^2)	9.7 W 12 W	1.57 W 0.1 W	0.29 W 0.1 W	11.6 W 12.7 W

A large number of turns is needed to obtain high inductance values with cores having small cross section areas. If the copper cross section area is adjusted according to the number of required turns and the available window area, small cores suffer from high current densities and thus, from large DC losses at high currents. Since there are many stacked turns especially in a foil winding, the AC resistance is very high compared to the DC resistance. This can be seen as high AC losses. The smaller cores suffer also from higher core losses since the variation in the applied electrical field (5.14) is increased due to a large number of turns and a short magnetic path, while the peak-to-peak current ripple remains in the same range.

The main limiting factor is the required copper area together with the number of required turns. The most cost efficient design criteria may not be the minimum loss criteria if the costs of the inductor core and the winding materials overshadow the savings from lower losses. A smaller core with slightly higher losses may result in lower overall costs during the operating period. This is demonstrated later in connection with the non-ripple limited inductor design.

The feasibility of foil windings in the phase-shifted full-bridge output inductor is questionable. The turns count is high and in order to avoid an excessive increase in winding capacitance, the insulator between the turns must be quite thick. An increase in insulator thickness reduces the available window area which can be used for copper, and this can result in high winding losses. The higher voltage at the secondary side increases the inductor insulation requirements, which results in thicker wire or foil insulators. Consequently, fewer turns can be fitted in the winding

window if the same copper cross section area is used as in the current-fed topologies, where the inductor is at the low voltage side.

Although the input current ripple is in the same range in all current-fed topologies, the ZVS boost suffers from a large inductor current ripple due to a large number of stacked turns, which increases the AC resistance dramatically. The dominant losses in the ZVS boost inductor in this case are AC winding losses. The approach presented by Nymand et al. (2009) having separate DC and AC foil windings on the same core could be used to reduce the high frequency losses. Also using a core where the winding could be split into several sections would reduce the increase in AC resistance. Since there are two inductors in the ZVS boost topology, the total inductor losses are doubled.

5.2.2 Minimum inductance at full load

An approach is investigated where the inductor is designed to provide the 15% maximum current ripple only at full load. The full load inductance requirement is the same as in Table 5.7 and the low load inductances are somewhat higher than the full load inductances depending on the inductor core bias versus permeability characteristics. The resulting current ripple at low loads can be higher than 15%. The conductor cross section areas in each core are made equal by adjusting the conductor diameter according to the required current density and the available winding width. The loss breakdown for inductors having the minimum inductance at full load are presented in Table 5.9.

Table 5.9: Loss breakdown for Magnetics E cores satisfying the full load minimum inductance criteria in a 10 kW converter.

Topology	Core	Turns	DC loss	AC loss	Core loss	Total loss
PSFB (1)	11 (40µ) 16 (26µ)	61 59 (2 x 4 mm^2)	3.2 W 6.9 W	1.2 W 0.021 W	1.2 W 0.51 W	5.6 W 7.4 W
PSFB (2)	9 (26µ) 16 (26 µ)	87 59 (2 x 4 mm^2)	5.4 W 6.9 W	1.9 W 0.021 W	0.7 W 0.51 W	8 W 7.4 W
ZVS Boost (1)	15 (26µ) 16 (26µ)	15 17 (2 x 25 mm^2)	2.73 W 13.9 W	9.6 W 0.3 W	0.88 W 0.78 W	26.5 W 30 W
ZVS Boost (2)	16 (26µ) 16 (26µ)	14 17 (2 x 25 mm^2)	2.05 W 13.9 W	12.8 W 0.3 W	0.78 W 0.78 W	31.2 W 30 W
FB Boost & RPP (1)	16 (26µ) 16 (26µ)	4 4 (2 x 95 mm^2)	0.44 W 3.4 W	0.99 W 0.8 W	0.51 W 0.51 W	1.94 W 4.7 W
FB Boost & RPP (2)	9 (60µ) 13 (40µ)	4 5 (2 x 25 mm^2)	1.64 W 8.2 W	1.2 W 0.7 W	2.06 W 1.2 W	4.9 W 10.1 W

Allowing a higher ripple percentage at light loads results in inductors having lower losses at full load, because the required turns count is smaller. The current ripple amplitude is the same at full load and low load. Hence, when dimensioning the input capacitors to filter the maximum ripple amplitude at full load, they will handle the same ripple also at low load. The ZVS boost topology suffers from a large turns count in relation to the current and the foil designs suffer from large AC winding losses. The winding losses can be shifted from AC losses towards DC losses by using wire.

In the case of gapped amorphous C cores with high permeability the number of turns required for small inductances is very low and thus the winding losses are very small. However, in high current ripple conditions the core losses in the 2605SA1 alloy cores are much higher than in the KoolMu powder cores. Figure 5.5 presents the proportion of the core losses to the total losses in the case of the amorphous C cores. The core losses are proportional to the core loss density and core mass, and since the core loss density is in the same range with every core, the large and heavy cores experience higher core losses.

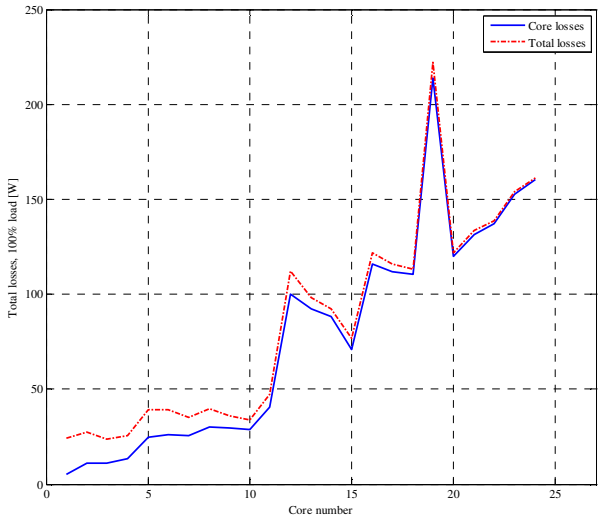


Figure 5.5: Proportion of core losses to total losses when using amorphous C cores when applying the minimum inductance at full load approach. The core losses are calculated with (5.8).

5.2.3 Minimum input current ripple at full load

If the high frequency current ripple is limited by the input inductor, no input capacitors are needed and the maximum current ripple is known regardless of the source impedance.

To investigate the inductor design with the minimum current ripple approach, the peak-to-peak input current ripple limit is set to 2% at full load. The resulting inductance requirements are listed in Table 5.10. The operating conditions are similar to Table 1.1.

Table 5.10: Required inductor sizes and peak-to-peak inductor current ripples for various topologies in a 10 kW system when applying the full load minimum current ripple approach.

Topology	Inductance (20%/100%)	Ripple frequency	Inductor current ripple pk-pk (20%/100%)	Inductor DC current (20%/100%)
PSFB	3850 µH/3850 µH	100 kHz	6.7%/2%	3 A/15 A
FB Boost	18 µH/18 µH	100 kHz	9.9%/2%	40 A/200 A
ZVS Boost	280 µH/280 µH	50 kHz	10.2%/2%	20 A/100 A
RPP	18 µH/18 µH	100 kHz	9.9%/2%	40 A/200 A

The only Magnetics powder core permeability by which the 18 µH or larger inductance can be realized is 26µ. With permeabilities of 40µ and 60µ the three largest cores are unavailable, limiting the winding space so that high current densities are required in order to fit the turns needed for the desired inductance. This increases the winding losses beyond the maximum limits. Table 5.11 presents the loss breakdown of the inductors designed for the compared topologies with the criteria presented in Table 5.10.

Table 5.11: Loss breakdown for Magnetics E cores providing the minimum loss (1) and cores of the minimum size (2) satisfying the full load minimum current ripple criteria in the compared topologies.

Topology	Core	Turns	DC loss	AC loss	Core loss	Total loss
FB Boost & RPP (1)	16 (26µ)	12 12 (3 x 25 mm^2)	4.03 W 26 W	0.47 W 0.05 W	0.06 W 0.06 W	4.56 W 26.1 W
FB Boost & RPP (2)	16 (26µ)	12 12 (3 x 25 mm^2)	4.03 W 26 W	0.47 W 0.05 W	0.06 W 0.06 W	4.56 W 26.1 W

The losses in phase-shifted full-bridge and ZVS boost inductors were too high in all designs, and consequently, the results for these topologies are omitted from Table 5.11. The limitations can be linked to the required inductor energy storage capability and area product. The inductor energy is

$$E_{\mathrm{L}} = \frac{LI^2}{2} \tag{5.25}$$

and in Magnetics catalogues (Magnetics, 2011) it is used as a dimensioning guideline without the divider and such that the inductance is in mH. If considering the requirements for the ZVS boost inductor (280 µH, 100 A), the LI^2 product is 2800, which is off the charts for the Magnetics E cores. The energy handling capability is related to the area product resulting from (McLyman, 2004)

$$A_p\left[cm^4\right]=\frac{2E_L\cdot 10^4}{B\cdot J\cdot K_{cu}}, \tag{5.26}$$

where B is the flux density in Tesla, J is the current density in A/cm^2 and K_{cu} is the window utilization factor in terms of copper. The area product for a certain core can be calculated from

$$A_p\left[cm^4\right]=W_a A_c, \tag{5.27}$$

where W_a is the core window area and A_c the core cross section area. Considering the ZVS boost inductor with parameters L = 280 µH, I = 100 A, B = 0.6 T, J = 138 A/cm^2 and K_{cu} = 0.85 as was the case in the calculation of Table 5.11, the required area product would be 398 cm^4. This cannot be satisfied with a single Magnetics E core, where the maximum area product for core number 16 is 239 cm^4.

Table 5.12 presents the loss breakdown of the amorphous C cores in the compared topologies.

Table 5.12: Loss breakdown for Metglas C cores providing the minimum loss (1) and cores of the minimum size (2) satisfying the full load minimum current ripple criteria in the compared topologies.

Topology	**Core**	**Turns**	**DC loss**	**AC loss**	**Core loss**	**Gap loss**	**Total loss**
PSFB (1)	- 23	- 56 (2 x 6 mm^2)	- 4.4 W	- 0.14 mW	- 4.9 W	- 0.29 W	- 9.6 W
PSFB (2)	- 15	- 176 (1 x 2.5 mm^2)	- 24 W	- 0.11 mW	- 1.6 W	- 0.64 W	- 27 W
ZVS Boost (1)	27 27	13 13 (2 x 50 mm^2)	4.2 W 7.1 W	0.1 W 0.002 W	7.4 W 7.4 W	0.54 W 0.54 W	24 W 30 W
ZVS Boost (2)	24 19	22 50 (1 x 35 mm^2)	26 W 58 W	0.23 W 0.005 W	3.6 W 1.3 W	0.61 W 1.2 W	60 W 120 W
FB Boost & RPP (1)	15 23	10 4 (3 x 95 mm^2)	2.44 W 2.3 W	0.076 W 0.006 W	2.42 W 6.2 W	0.83 W 0.29 W	5.8 W 8.8 W
FB Boost & RPP (2)	10 13	10 8 (1 x 50 mm^2)	14 W 17 W	0.16 W 0.009 W	1.1 W 2.2 W	0.46 W 0.44 W	15 W 19 W

In this case the losses in the amorphous C cores are generally higher than in the powder cores, which results from the increased core losses and additional gap losses. Both AC and DC winding losses can be pushed lower since the winding windows are relatively large and fewer

turns are needed in order to achieve the desired inductances. The advantages of foil windings can be seen in full-bridge boost and resonant push-pull inductors, which have a low turns count and high current. The obtainable copper fill factor and cross section area is large with foil windings and the total winding losses are lower than with wire windings as long as the AC resistances remain low enough. When using wire windings in high current inductors, multiple smaller gauge wires need to be paralleled in order to achieve adequately low DC resistances and to avoid excessive skin effects in single large diameter wires.

5.2.4 Minimum input current ripple over defined load range

The inductor is designed with the criterion that the input current ripple is < 2% over a load range of 20% - 100%. The resulting inductance requirements are listed in Table 5.13.

Table 5.13: Minimum inductor sizes and peak-to-peak current ripples for various topologies in a 10 kW system. The design approach is to limit HF input current ripple to < 2% at load range of 20-100%.

Topology	Inductance (20%/100%)	Ripple frequency	Inductor current ripple pk-pk (20%/100%)	Inductor DC current (20%/100%)
PSFB	12.9 mH/3850 µH	100 kHz		3 A/15 A
FB Boost	90 µH/18 µH	100 kHz	2%/2%	40 A/200 A
ZVS Boost	1450 µH/280 µH	50 kHz	2%/2%	20 A/100 A
RPP	90 µH/18 µH	100 kHz	2%/2%	40 A/200 A

Using a large inductor to limit the input current ripple over a wide load range is not a good solution in terms of losses and cost. The winding capacitance increases together with a large copper area and a large number of stacked turns, which can reduce the inductor resonance frequency near or below the fundamental ripple frequency. The resonance frequency can be increased by using thicker insulators, but this reduces the winding space and thus the current density has to be higher.

5.2.5 Inductor losses in a non ripple-constrained design

In the previous sections the inductance has been constrained to a certain value to allow a certain current ripple, while the current density has been selected from an allowable range to produce the minimum total losses. In this section the minimum loss or minimum cost inductors are found with brute force optimization using the following constraints:

- The minimum inductance is 0.1 µH.
- The minimum current density is 10 A/cm^2 (or the minimum current density defined by the core, insulator thickness and maximum fill factor).
- The minimum insulator is a 0.13 mm Nomex 410, and if the resonance frequency is too low, the insulator thickness is increased until the criterion is met.
- The gap losses are calculated with $K_i = 0.1550$.

- The cost of power losses are € 0.0000835/Wh and the operating time range is 10 years.
- The cost of copper is € 6.446/kg.
- The cost of insulators is not included.

Tables 5.14 and 5.15 present the inductor losses in the compared topologies when the only constraints are the minimum inductance, minimum current density and insulator thickness.

Table 5.14: Loss breakdown for Magnetics E cores providing the minimum loss (1) and cores of the minimum size (2) in the compared topologies.

Topology	Core	Turns	DC loss	AC loss	Core loss	Total loss
PSFB (1)	13 (26µ) 16 (26µ)	33 37 (2 x 10 mm^2)	2.57 W 1.7 W	0.9 W 0.13 W	2.9 W 1.3 W	6.4 W 3.2 W
PSFB (2)	10 (26µ) 11 (26µ)	30 23 (2 x 1.5 mm^2)	3.3 W 3.6 W	0.75 W 1.1 W	5.6 W 6.1 W	9.7 W 11 W
ZVS Boost (1)	15 (26µ) 16 (26µ)	16 10 (2 x 50 mm^2)	3.1 W 4.1 W	9.3 W 3 W	0.78 W 2.2 W	26.4 W 18.6 W
ZVS Boost (2)	15 (26µ) 14 (26µ)	16 11 (2 x 16 mm^2)	3.1 W 7 W	9.3 W 4.9 W	0.78 W 5.3 W	26.4 W 34.4 W
FB Boost & RPP (1)	16 (26µ)	5 4 (2 x 95 mm^2)	0.75 W 3.4 W	0.81 W 0.77 W	0.33 W 0.51 W	1.9 W 4.7 W
FB Boost & RPP (2)	7 (60µ) 13 (60µ)	3 4 (2 x 35 mm^2)	1.64 W 4.67 W	2.03 W 1.34 W	4.02 W 2.13 W	7.9 W 8.1 W

The full load peak-to-peak ripple percentages and corresponding inductances were as follows:

- PSFB (1), foil: 44%, 152 µH
- PSFB (1), wire: 31%, 220 µH
- PSFB (2), foil: 74.6%, 89.4 µH
- PSFB (2), wire: 89%, 76 µH
- ZVS Boost (1), foil: 11.5%, 49.7 µH (corresponding input current ripple 1.4%)
- ZVS Boost (1), wire: 38%, 15 µH (corresponding input current ripple 4.8%)
- ZVS Boost (2), foil: 11.5%, 49.7 µH (corresponding input current ripple 1.4%)
- ZVS Boost (2), wire: 63.5%, 9 µH (corresponding input current ripple 7.9%)
- FB Boost & RPP (1), foil: 9%, 3.85 µH

- FB Boost & RPP (1), wire: 14.3%, 2.5 µH
- FB Boost & RPP (2), foil: 37%, 0.934 µH
- FB Boost & RPP (2), wire: 17.9%, 1.99 µH

The very low core losses of the KoolMµ material allows high ripple percentages such as 37% in the high current topologies. Ripples of this magnitude can be expensive and difficult to filter out. Therefore, the maximum ripple magnitude is more likely to be limited by the external components, not the inductor itself. Topologies with the inductor having a large turns count and relatively low current benefit from wire winding since the reduction in AC losses compensate the increased DC losses caused by the lower fill factor. If there is no wire paralleling, the minimum inductor losses in Table 5.14 are:

- PSFB: 3.6 W (21 turns of 1 x 16 mm^2)
- ZVS boost: 2 x 11.4 W (10 turns of 1 x 50 mm^2)
- FB boost & RPP: 7 W (4 turns of 1 x 95 mm^2)

The non-paralleled wire winding is still advantageous in the phase-shift full-bridge and the ZVS boost, but in the high inductor current topologies, there is an obvious increase in losses when using a single wire.

Table 5.15: Loss breakdown for Metglas C cores providing the minimum loss (1) and cores of the minimum size (2) in the compared topologies.

Topology	**Core**	**Turns**	**DC loss [W]**	**AC loss [W]**	**Core loss [W]**	**Gap loss [W]**	**Total loss [W]**
PSFB (1)	- 27	- 54 (1 x 16 mm^2)	- 4.2 W	- ~ 0 W	- 4.2 W	- 0.1 W	- 8.5 W
PSFB (2)	- 11	- 59 (1 x 4 mm^2)	- 7.1 W	- 0.003 W	- 6.8 W	- 1.7 W	- 16 W
ZVS Boost (1)	27 27	14 14 (1 x 95 mm^2)	5.2 W 8 W	0.11 W 0.001 W	6.3 W 6.3 W	0.5 W 0.48 W	24.2 W 30 W
ZVS Boost (2)	12 14	21 11 (1 x 35 mm^2)	10 W 8.8 W	0.88 W 0.037 W	5.9 W 13 W	4.5 W 4 W	44.8 W 51 W
FB Boost & RPP (1)	27 25	5 4 (3 x 95 mm^2)	1.5 W 2.9 W	0.004 W 0.003 W	2.8 W 4.2 W	0.09 W 0.14 W	4.3 W 7.2 W
FB Boost & RPP (2)	6 9	6 4 (2 x 25 mm^2)	4.6 W 6.4 W	0.25 W 0.17 W	3.5 W 6.9 W	1.9 W 1.7 W	10 W 15 W

The full load peak-to-peak ripple percentages and corresponding inductances were as follows:

- PSFB (1), wire: 0.83%, 7.2 mH
- PSFB (2), wire: 4.9%, 1.2 mH
- ZVS Boost (1), foil: 2%, 283 µH (corresponding input current ripple 0.3%)
- ZVS Boost (1), wire: 2%, 283 µH (corresponding input current ripple 0.3%)
- ZVS Boost (2), foil: 7.5%, 76.6 µH (corresponding input current ripple 0.9%)
- ZVS Boost (2), wire: 9.6%, 59 µH (corresponding input current ripple 1.2%)
- FB Boost & RPP (1), foil: 0.7%, 48 µH
- FB Boost & RPP (1), wire: 1.2%, 29 µH
- FB Boost & RPP (2), foil: 4.4 %, 7.9 µH
- FB Boost & RPP (2), wire: 5.7 %, 6.1 µH

If considering a single wire winding, the minimum inductor losses are:

- PSFB: 8.5 W (54 turns of 1 x 16 mm^2)
- ZVS boost: 2 x 15 W (14 turns of 1 x 95 mm^2)
- FB boost & RPP: 11 W (6 turns of 1 x 95 mm^2)

Selecting the core providing the lowest losses is the best solution in terms of operating costs, but the overall initial costs including the core price and the cost of winding materials can easily be higher than the operating costs. This biases the core selection towards smaller cores and slightly higher losses. Figure 5.6 presents the losses versus cost comparison in the case of inductors from Table 5.15. The lowest losses are obtained with the largest core in all topologies, but the lowest overall costs over 10 years of operating time are obtained with the following cores:

- PSFB: core 16 (wire)
- ZVS boost: core 16 (foil), core 18 (wire)
- FB boost & RPP: core 11 (foil), core 11 (wire)

It is noteworthy that in this case these minimum cost cores are not the minimum usable cores defined by the maximum allowable losses.

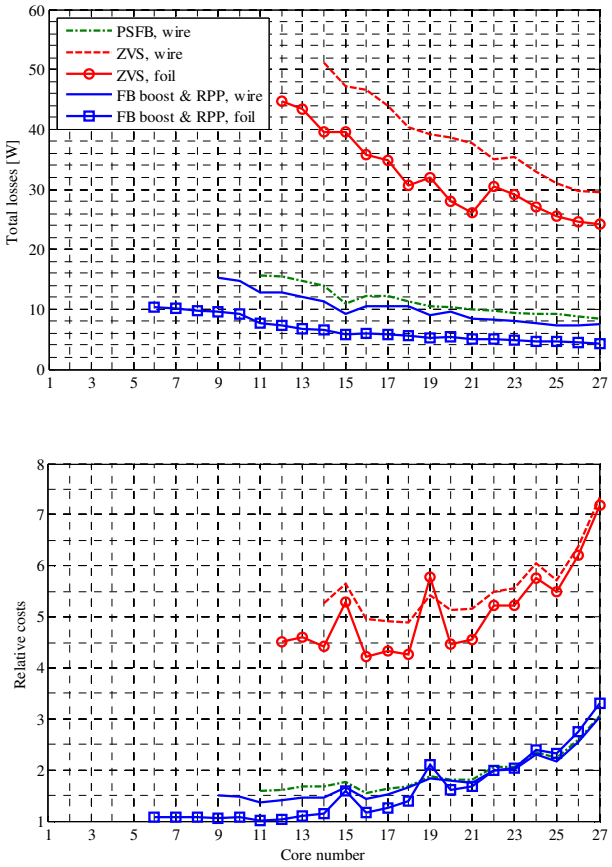


Figure 5.6: Total losses and relative total costs of the studied inductors in the case of amorphous C cores in a non ripple-constrained 10 kW design. The operating time is 10 years. The costs include core price, copper price and the cost of power losses.

If the core and gap losses are added together, it is seen that in the minimum loss designs the combined core and gap losses tend to approach each other when using amorphous C cores (Figure 5.7). The sudden increase in core and gap losses in the ZVS boost after core 12 when using foil is due to an increase in the required winding insulator thickness, which reduces the copper fill factor available. Thus, a smaller number of turns are selected in the minimum loss design.

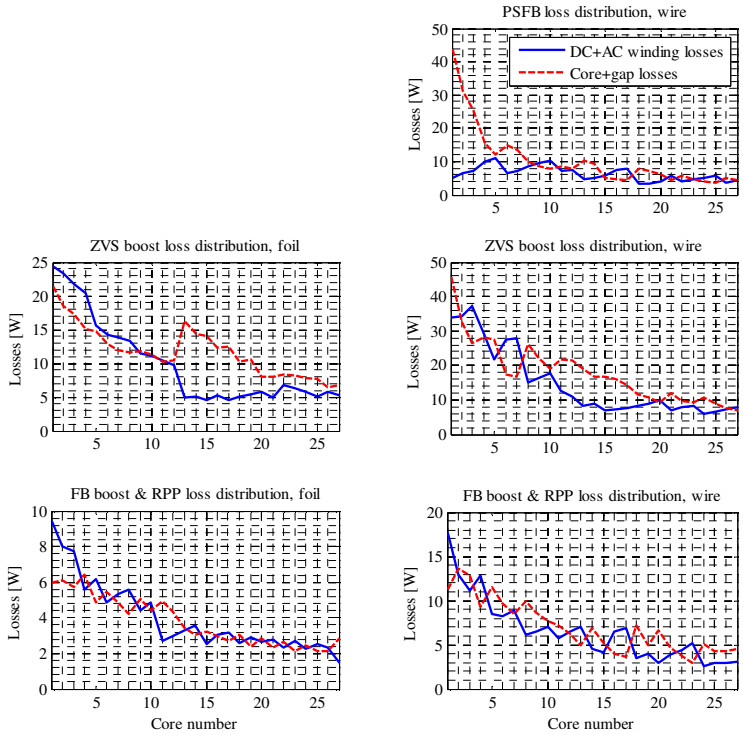


Figure 5.7: Winding losses, core losses and gap losses in Metglas C core inductors in the case of a non ripple-constrained 10 kW design.

Figure 5.8 illustrates the situation where the core and gap losses are separated. It is seen that cores where the gap losses are larger than the core losses and where the difference between the core and winding losses is large do not satisfy the minimum usable core criteria in Table 5.15. The minimum costs are obtained with the first core satisfying the minimum loss criteria and having the core and winding losses close to each other.

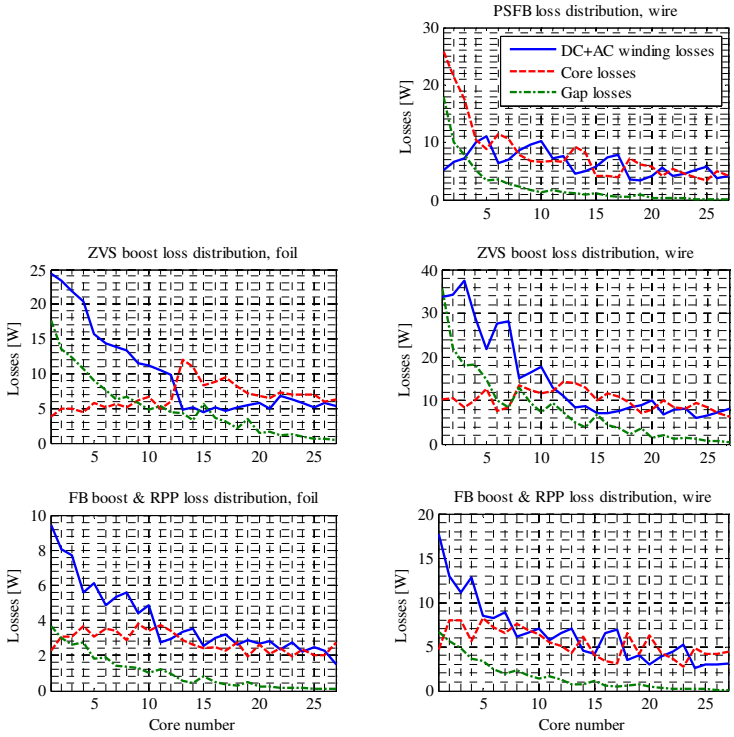


Figure 5.8: Winding losses, core losses and gap losses in C core inductors in the case of a non ripple-constrained 10 kW design.

Figure 5.9 presents the total losses and relative costs in the compared topologies when using Magnetics E cores. The curves are for KoolMμ with an initial permeability of 26μ. The cores providing the lowest costs during the 10 year operating time are:

- PSFB: core 11 (foil), core 16 (wire)
- ZVS boost: core 15 (foil), core 16 (wire)
- FB boost & RPP: core 11 (foil), core 15 (wire)

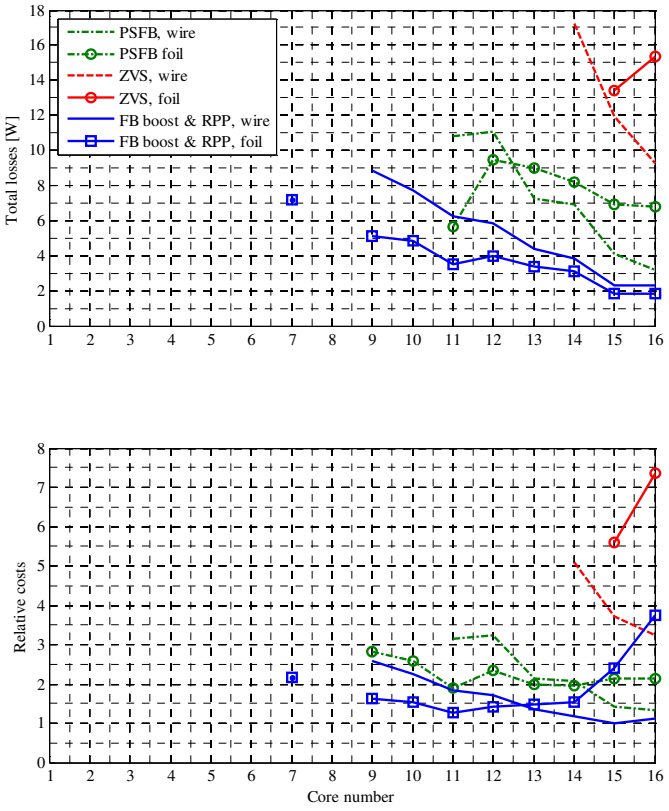


Figure 5.9: Total losses and relative costs of the studied inductors in case of Magnetics E cores in a non ripple-constrained 10 kW design. The operating time is 10 years. Core prices are not included in the calculation.

The lack of core price data pushes the minimum price point towards very low losses, which are achieved with large cores having large copper cross sections. With foil windings there is a price increase in the largest cores since the amount of copper is large and the loss increase in the smaller cores is not as steep as with wire windings.

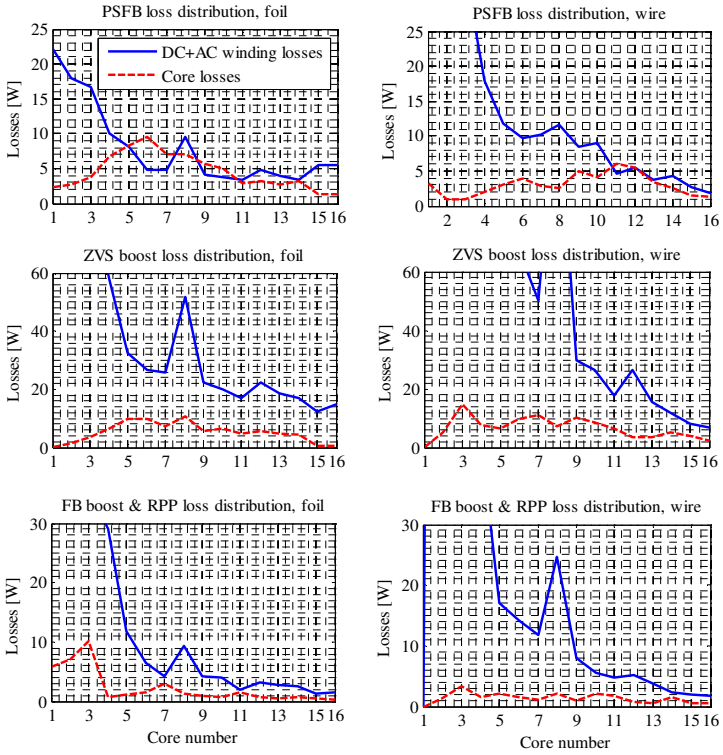


Figure 5.10: Winding losses and core losses in Magnetics E core inductors in the case of a non ripple-constrained 10 kW design.

The loss distributions indicate which winding type, foil or wire, is more appropriate for each topology in the given operating conditions. In all topologies the gap between winding and core losses is smaller in the foil designs and the total losses are also lower. The foil winding also enables a wider range of cores that can be used, although the differences in losses between the foil and wire windings are rather small, provided that parallel wires can be used.

5.2.6 Duty cycle and inductor losses

Figure 5.11 presents the achievable minimum loss for one C core as a function of the duty cycle in the compared topologies. The winding in every case is a single wire winding.

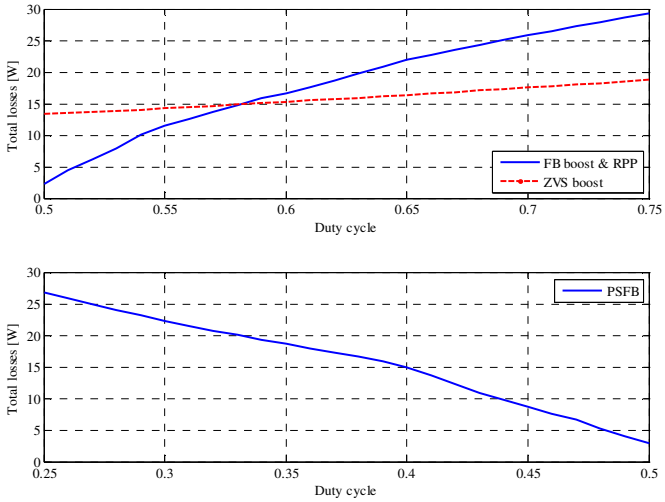


Figure 5.11: Behavior of C core losses as a function of duty cycle.

It can be seen that the ideal duty cycle in terms of inductor design would be 0.50, as the ripple component is at minimum and the losses are mostly DC losses. The only topologies which can be operated at a duty cycle of 0.50 are ZVS boost and RPP with a duty cycle range of $0 < D < 1$. However, if the inductor is designed strictly for this duty cycle, the inductance is small and there is very little tolerance for increased current ripple as the duty cycle deviates from 0.50 depending on the operating conditions. The ZVS boost is most insensitive to duty cycle variations in terms of inductor losses whereas the FB boost, RPP and PSFB exhibit very similar sensitivities. There are no fundamental differences in the loss behavior and between the topologies when using Magnetics E cores.

5.2.7 Frequency and inductor losses

Figure 5.12 describes the behavior of inductor losses as a function of switching frequency.

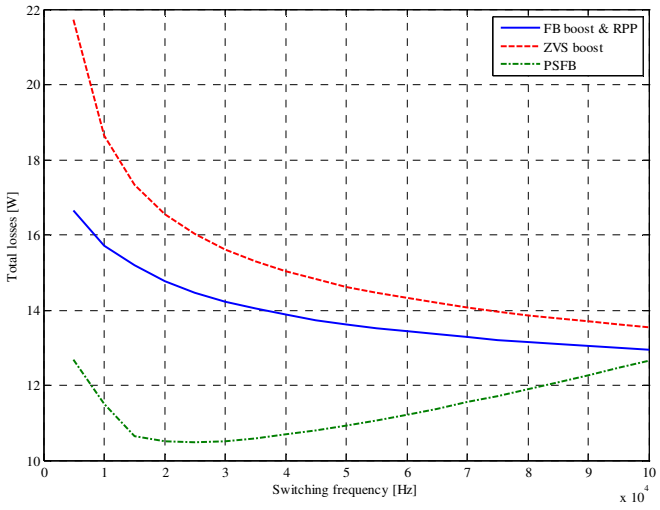


Figure 5.12: Behavior of C core losses as a function of switching frequency with duty cycle of 0.57.

The general trend is that higher frequencies allow smaller inductors to achieve a certain current ripple and the reduction in winding losses is larger than the increase in core losses, especially with high currents. In PSFB the output inductor losses tend to have a certain minimum at a frequency between the minimum and maximum frequency limits, and this optimum frequency depends on the operating parameters described in section 2.2.3. The switching frequency has the largest impact on the inductor losses in the ZVS boost topology. The inductor loss behavior as a function of frequency is more similar to the Magnetics E cores than to the Metglas C cores.

5.2.8 Summary

The main limiting factor for inductor scaling is the required inductor energy product, which is linked to the inductor area product via the maximum flux density, current density and copper fill factor. The required energy product to achieve a certain inductor current ripple is a topology dependent parameter and of the compared topologies the ZVS boost has the largest inductor energy products.

The maximum allowable inductor current ripple depends on the requirements set by the external components and on the inductor core material and allowable inductor losses. Very low core loss materials, such as the KoolMμ, may allow current ripples which are practically too high to be filtered out. In minimum loss inductors the winding and core losses tend to approach each other as can be seen from Figures 5.8 and 5.10. When using gapped C cores the situation where gap losses exceed core losses and there is a large gap between core losses and winding losses indicate that the core in question is too small for the given operating conditions. In all of the compared topologies the inductor losses decrease as the duty cycle approaches 50%. FB boost and RPP inductor losses decrease as a function of frequency whereas the minimum loss frequency point of a PSFB output inductor varies according to the operating conditions.

When the inductor has a large turns count and relatively low current, such as in PSFB and ZVS boost, a wire winding can be more efficient than a foil winding even if parallel wires are not used. With wire winding there are fewer stacked winding layers which reduces the proximity losses. Also the winding capacitances are smaller than with a foil winding with thin turn-to-turn insulators. If the insulator thickness is increased in a foil winding the available window area for copper may decrease to a point where the winding losses become unacceptably high.

5.3 Transformer scaling limitations

In this section, the various calculation methods for estimating the transformer AC resistance and the leakage inductance are demonstrated and compared to measurements as well as FEM simulations. The dependencies between the core and winding losses are introduced as a function of duty cycle and frequency. The feasibility of the litz wire is evaluated against a copper foil winding.

5.3.1 Methods for calculating transformer winding losses

The two most common materials for high frequency power transformer windings are copper foil and litz wire. The methods for deriving the AC-resistance factor for foil windings have been proposed in various forms for example by Dowell (1966), Vandelac and Ziogas (1988) and Hurley et al. (2000).

Assuming that the magnetic field lines are nearly parallel to the winding layers and that the primary and secondary currents are in phase, the ratio R_{ac}/R_{dc} for a multilayer winding can be calculated from (Erickson and Maksimovic, 2001; Vandelac and Ziogas, 1988)

$$F_r = \frac{R_{ac}}{R_{dc}} = \varphi\left[G_1(\varphi) + \frac{2}{3}\left(M^2 - 1\right)\cdot\left(G_1(\varphi) - 2G_2(\varphi)\right)\right], \tag{5.28}$$

where φ is the relation factor between the conductor height and skin depth and is defined for a foil conductor as

$$\varphi = \frac{h}{\delta} = \frac{h}{\sqrt{\frac{\rho}{\pi\mu_r\mu_0 f}}}\cdot \tag{5.29}$$

A layer of round conductor winding can be approximated as a layer of foil winding as demonstrated in Figure 5.13 (Erickson and Maksimovic, 2001; Vandelac and Ziogas, 1988).

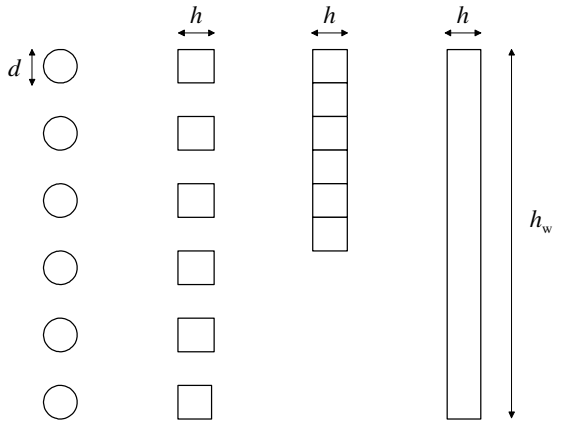


Figure 5.13: Approximation of a layer of round conductors as an effective foil conductor.

The equal foil thickness h is obtained from the wire diameter d by setting the square conductor cross section area equal to the circular conductor area

$$h = \sqrt{\frac{\pi}{4}} \cdot d \tag{5.30}$$

When the square conductors are approximated as a single foil conductor stretched along the winding window, the actual copper area is smaller than the area of the approximated foil conductor. The ratio of the actual copper area to the approximated copper area is called the porosity factor and it is defined as

$$\eta = \sqrt{\frac{\pi}{4}} \cdot d \cdot \frac{n}{h_w}, \tag{5.31}$$

where n is the number of round wires on a winding layer. The factor φ for a round conductor can now be calculated from

$$\varphi = \sqrt{\eta}\sqrt{\frac{\pi}{4}} \cdot \frac{d}{\delta}. \tag{5.32}$$

The functions $G_1(\varphi)$ and $G_2(\varphi)$ in (5.28) are

$$\begin{aligned} G_1(\varphi) &= \frac{\sinh(2\varphi)+\sin(2\varphi)}{\cosh(2\varphi)-\cos(2\varphi)} \\ G_2(\varphi) &= \frac{\sinh(\varphi)\cos(\varphi)+\cosh(\varphi)\sin(\varphi)}{\cosh(2\varphi)-\cos(2\varphi)} \end{aligned}. \tag{5.33}$$

The term M in (5.28) refers to the number of stacked winding layers in a portion, while a portion is defined as a group of winding layers between peak and zero MMF. Figure 5.14 describes a situation with a 2:8 transformer interleaved with two intersections.

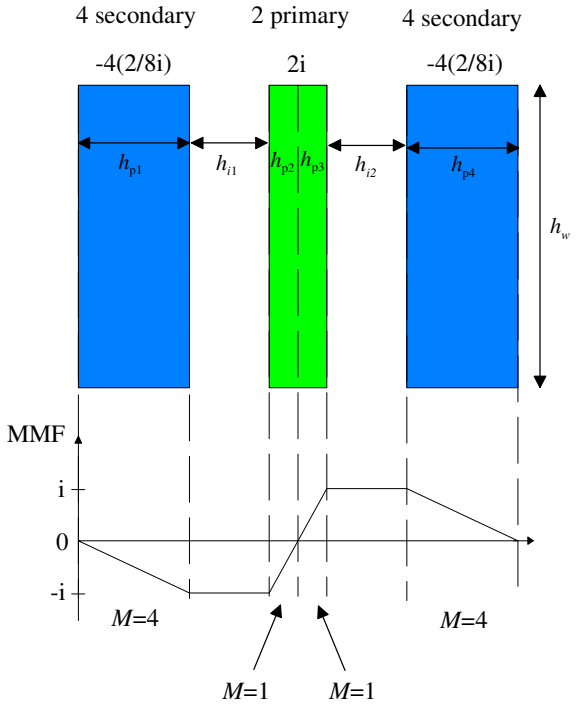


Figure 5.14: Definition of a winding portion and the parameter M in a two winding transformer with two primary-secondary intersections.

In Figure 5.14 there are four secondary layers in a winding portion, and therefore, the parameter M in (5.28) would be 4 when calculating the secondary winding resistance ratio. The primary winding is divided into two portions with one winding layer in a portion, and thus for the primary winding $M = 1$. The total AC resistance for each winding can be calculated based on the copper resistivity ρ, wire area A_w and winding length l_w as

$$R_{ac} = F_r R_{dc} = F_r \cdot \frac{\rho \cdot l_w}{A_w}. \tag{5.34}$$

In case the transformer is unidirectionally excited, there is a DC or average component in the winding current. This DC current component does not produce any proximity losses and the only losses are caused by the winding DC resistance. The AC loss components can be calculated via harmonic analysis and the resulting total copper losses in the winding are (Erickson and Maksimovic, 2001)

$$\frac{P_{ac}}{P_{dc}} = I_{dc}{}^2 R_{dc} \frac{\sum_{j=1}^{\infty} I_j{}^2 R_{dc} \sqrt{j\varphi_1} \left[G_1\left(\sqrt{j\varphi_1}\right) + \frac{2}{3}\left(M^2 - 1\right)\left(G_1\left(\sqrt{j\varphi_1}\right) - 2G_2\left(\sqrt{j\varphi_1}\right)\right)\right]}{I_1{}^2 R_{dc} F_r} F_r I_1{}^2 R_{dc} \qquad (5.35)$$

where j is the harmonic number and φ_1 is the relation factor between the conductor height and skin depth at the fundamental frequency.

The method used in this work to calculate litz wire losses is based on the principles introduced in the works of Bartoli et al. (1996). Equations (5.36) and (5.43) presented by Bartoli et al. (1996) give negative or Not a Number values if implemented as such in mathematical software such as MATLAB. Therefore, (5.36) and (5.43) are rearranged to provide an accurate prediction of R_{ac}/R_{dc} when using the MATLAB scripts given in Appendix D. A simple litz wire winding configuration is presented in Figure 5.15 to define the parameters needed for the calculations.

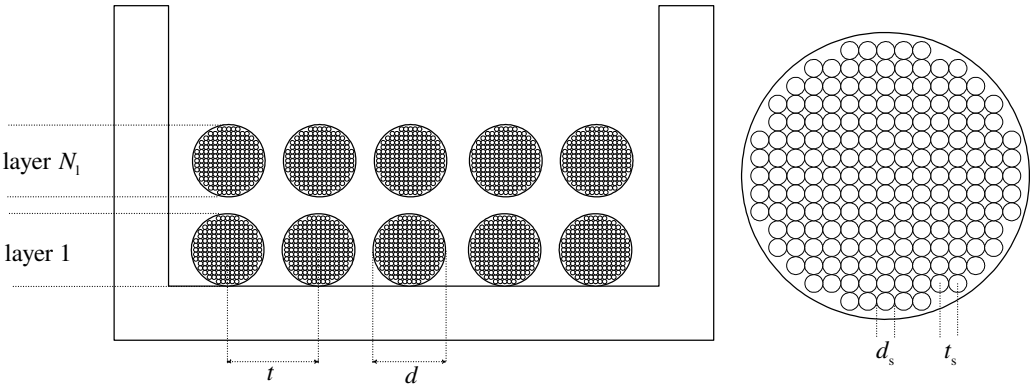


Figure 5.15: A simple litz wire configuration with various calculation parameters. The wire insulators keeping the conductors apart are not shown.

In Figure 5.15 d displays the litz wire diameter excluding the insulation layer, t is the distance between two adjacent litz conductors, d_s is the diameter of a single strand excluding the strand insulation layer, t_s is the distance between two adjacent strands in the same bundle and N_l is the total number of winding layers.

The total AC resistance of a litz winding can be calculated from

$$
\begin{aligned}
R_{ac} &= R_{dc} \cdot \frac{\gamma}{2} \cdot (A - B \cdot C) \\
A &= \frac{ber(\gamma)bei'(\gamma) - bei(\gamma)ber'(\gamma)}{[ber'(\gamma)]^2 + [bei'(\gamma)]^2} \\
B &= 2\pi \left[\left(\frac{4(N_1^{\,2} - 1)}{3} + 1 \right) \cdot n_s^{\,2} \cdot \left(\eta_{ext}^{\,2} + \eta_{int}^{\,2} \cdot \frac{p}{2\pi \cdot n_s} \right) \right] \\
C &= \frac{ber_2(\gamma)ber'(\gamma) + bei_2(\gamma)bei'(\gamma)}{ber(\gamma)^2 + bei(\gamma)^2}.
\end{aligned}
\tag{5.36}
$$

The DC resistance for a litz wire conductor can be calculated as

$$
R_{dc} = \frac{4\rho}{n_s \cdot \pi \cdot d_s^{\,2}} \cdot N \cdot MLT \ , \tag{5.37}
$$

where N is the number of turns and MLT is the mean length per turn. The term γ is the ratio of the single strand diameter to the diagonal of a square, which has a side length of one skin depth. This ratio derives from the transformation of the round conductors to an equivalent square conductor.

$$
\gamma = \frac{d_s}{\delta\sqrt{2}} \tag{5.38}
$$

The external and internal porosity factors η_{ext} and η_{int} have an impact on external and internal proximity effects, respectively, and they can be calculated from

$$
\begin{aligned}
\eta_{ext} &= d_s \frac{\sqrt{\pi}}{2t} \\
\eta_{int} &= d_s \frac{\sqrt{\pi}}{2t_s}
\end{aligned}
\ . \tag{5.39}
$$

The Kelvin functions $ber_v(x)$ and $bei_v(x)$ are real and imaginary parts, respectively, of (Råde and Westergren, 2001)

$$
J_v\left(xe^{\frac{3\pi j}{4}} \right), \tag{5.40}
$$

where x is real and $J_v(z)$ is the v^{th} order Bessel function of the first kind. The special cases of $ber_0(x)$ and $bei_0(x)$ are commonly denoted as $ber(x)$ and $bei(x)$ and they have series expansions of

$$ber(x) = 1 + \sum_{k\geq 1}\left(\frac{(-1)^k\left(\frac{x}{2}\right)^{4k}}{[(2k)!]^2}\right)$$
$$bei(x) = \sum_{k\geq 0}\left(\frac{(-1)^k\left(\frac{x}{2}\right)^{4k+2}}{[(2k+1)!]^2}\right). \tag{5.41}$$

The ber'(x) and bei'(x) are real and imaginary parts of derivative of (5.40) with respect to x.

The litz packing factor p ranges from $0 < p < N$ and is defined as

$$p = \frac{N\pi {d_s}^2}{\pi {d}^2}. \tag{5.42}$$

The method can be applied also to solid round conductors. In this case the expression for the AC resistance is otherwise identical to the litz wire, but the internal porosity factor is neglected.

$$\begin{aligned} R_{ac} &= R_{dc}\cdot\frac{\gamma}{2}\cdot(A - B\cdot C)\\ A &= \frac{ber(\gamma)bei'(\gamma) - bei(\gamma)ber'(\gamma)}{[ber'(\gamma)]^2 + [bei'(\gamma)]^2}\\ B &= 2\pi\left[\left(\frac{4({N_1}^2-1)}{3}+1\right)\cdot{\eta_{ext}}^2\right]\\ C &= \frac{ber_2(\gamma)ber'(\gamma) + bei_2(\gamma)bei'(\gamma)}{ber(\gamma)^2 + bei(\gamma)^2} \end{aligned} \tag{5.43}$$

The solid wire DC resistance is obtained from (5.37) by setting $n_s = 1$, as there is only one single conductor carrying the current.

5.3.2 Calculation of transformer leakage inductance

The transformer leakage inductance for a winding can be estimated from (Dowell, 1966; Mohan et al., 2003; Nymand, 2010)

$$L_{leak} = \frac{\mu_0 N^2 l_w}{P^2 h_w}\left(\frac{1}{3}\sum_{p=1}^{2P} h_p + \sum_{i=1}^{P} h_i\right), \tag{5.44}$$

where N is the number of turns of the winding in question, l_w is the total winding length, P is the total number of primary-secondary intersections, h_w is the winding width, h_p is the height of

the p^{th} winding portion and h_i is the height of i^{th} primary-secondary insulation layer, as indicated in Figure 5.14.

The leakage inductance given by this method is not frequency dependent, but gives a fixed leakage inductance value depending on the winding parameters in (5.44). In reality, the leakage inductance decreases with frequency since the current moves closer to the surface of the conductor at the isolation boundary between the winding layers. This reduces the effective portion height and thus the leakage inductance.

It is noteworthy that the leakage inductance is dependent on the number of turns squared, and hence, the larger the required number of turns in a transformer, the higher the leakage inductance, unless the leakage inductance is reduced by increasing the number of primary-secondary intersections with winding interleaving. The total winding length is also increased together with increased turns count, which increases the leakage inductance further. Thick windings and winding insulators also result in an increased leakage inductance.

5.3.3 Comparison of calculated and measured transformer parameters

The methods described above are compared against measurements as well as 1D and 2D FEM simulations in the case of copper foil winding, solid round copper winding and litz wire. The measurements were conducted with an HP 4284A LCR meter and the FEM simulator was ANSYS Maxwell 14.0. The estimated LCR measurement error is ±0.45% with f ≤ 100 kHz and ±1.13% with f > 100 kHz. The maximum allowable FEM error tolerance was set to ±1.5%.

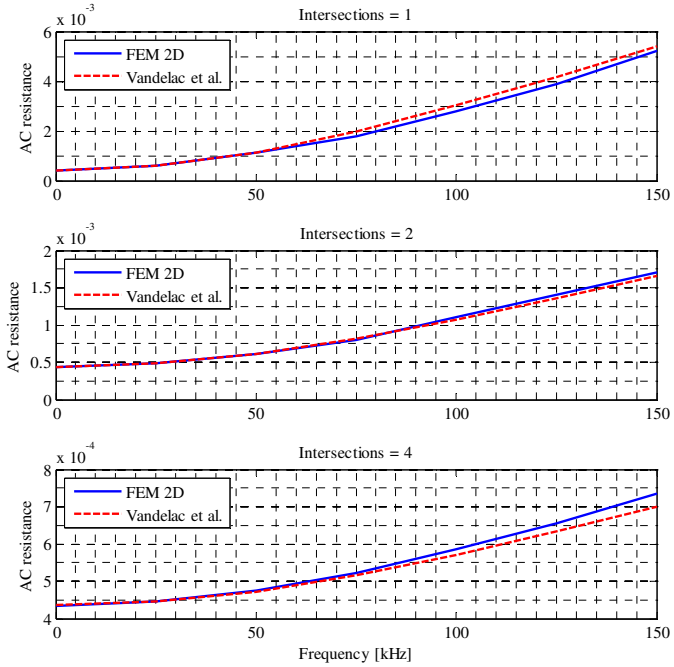


Figure 5.16: Simulated and calculated foil winding transformer AC resistances referred to primary in a 2:8 transformer. The foil dimensions are 56 mm x 0.29519 mm and the windings are wound on a PM114/93 core. FEM simulations are conducted with an air core to eliminate the core resistance.

Figure 5.16 demonstrates that the method presented by Vandelac et al. gives results very similar to the 2D FEM simulation. The winding resistances were calculated separately for primary and secondary windings and then the secondary resistance was added to the primary resistance through the transformer turns ratio. The total primary resistance given by the FEM simulation was obtained through a small signal test, which takes the overall magnetic component behavior into account.

The calculated and simulated leakage inductances for the transformers in Figure 5.16 are listed in Table 5.16. The leakage inductance is calculated and simulated at 50 kHz, as the winding thickness was equal to one skin depth at this frequency.

Table 5.16: Leakage inductances simulated with a 2D FEM simulator compared to leakage inductances calculated with (5.44).

Primary-secondary intersections	**1**	**2**	**4**
Simulated primary leakage	18 nH	5.6 nH	1.8 nH
Calculated primary leakage	19.6 nH	5.7 nH	1.8 nH

The calculated leakage inductances correspond very well with the simulated leakage inductances. It is seen that even the simple interleaving with two intersections reduces the leakage inductance by 69% compared to the non-interleaved winding. Using a total of four intersections reduces the leakage inductance further by 68%, leading to a reduction of 90% compared to the non-interleaved case. This illustrates the importance of winding interleaving in obtaining small leakage inductances and fast current commutation times.

Figure 5.17 presents the calculated, simulated and measured resistances for a single winding wound on an ETD39 bobbin. The winding is measured with both one layer and two layers and the resulting winding porosity is taken into account in calculations and simulations.

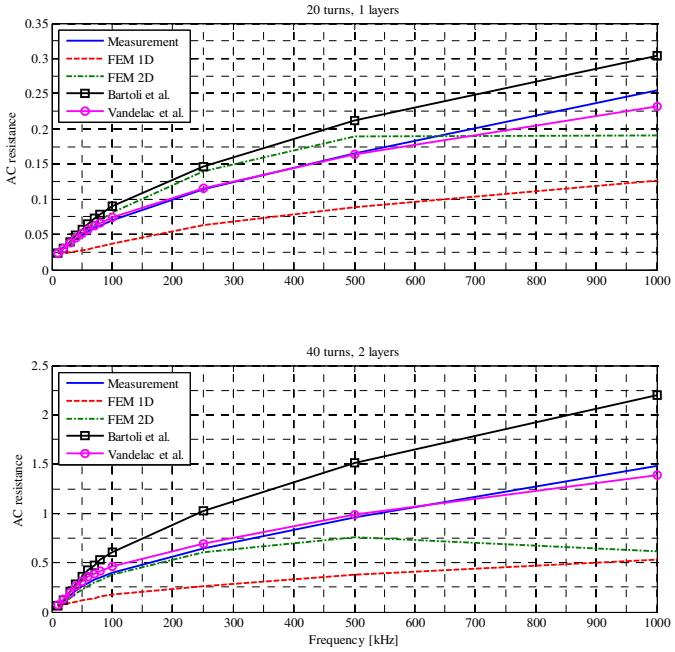


Figure 5.17: Measured, calculated and simulated AC resistances for a solid 0.78 mm^2 wire wound on an ETD39 core.

With a one layer winding, the best correlation with the measurements is achieved with the method of Vandelac et al. over the entire frequency range. The method introduced by Bartoli et al. gives results very similar to the 2D FEM simulation up to 250 kHz, while the resistance values are slightly higher than the measured resistances. The poorest correlation is achieved with 1D FEM simulations. With two winding layers the resistances obtained with the method of Vandelac et al. and the 2D FEM simulation are very close to the measured resistances, but after 250 kHz the FEM resistances begin to decrease significantly compared to the measured values. The method of Bartoli et al. is sensitive to the number of layers whereas that of Vandelac et al. is sensitive to the porosity factor, i.e. the ratio of the total winding width to the winding window width.

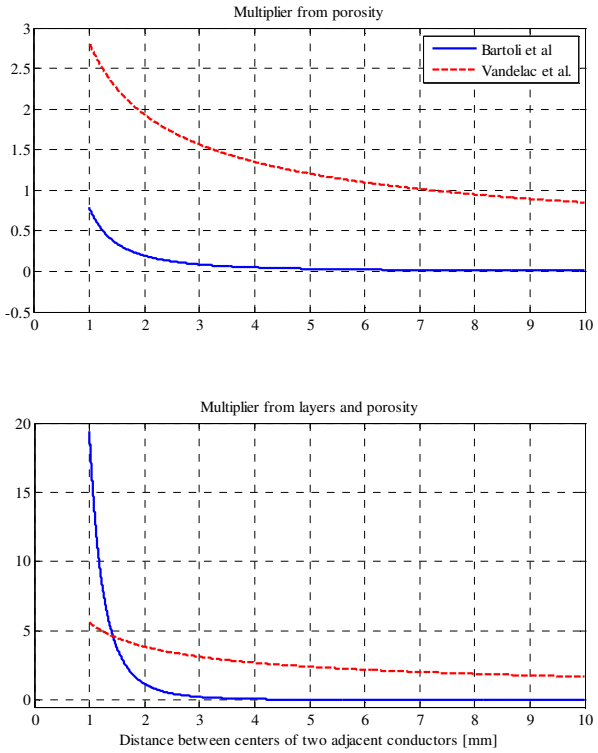


Figure 5.18: Multipliers from the winding porosity and the total number of layers in the calculation methods of Bartoli et al. and Vandelac et al., when using the double layer winding of Figure 5.17.

It can be seen from Figure 5.18 that the combined multiplier of winding layers and the porosity factor remains larger in the Vandelac et al. method when the distance between the centers of adjacent conductors is increased. In this case, when the distance is increased beyond 2 mm, which is roughly twice the conductor diameter, the multiplier B in (5.43) is smaller than 1 and the AC resistance given by the Bartoli et al. method is nearly equal to a single layer winding resistance despite of increase in winding layers. The porosity correction of the method introduced by Vandelac et al. results in a smaller resistance error with large porosity factors and multiple winding layers. This is demonstrated in Figure 5.19, where the method of Bartoli et al. gives nearly the same resistance values for both a single and a double layer winding. On the other hand, the higher resistance of the double layer winding is seen in the Vandelac et al. method, although the resistance values are smaller than those given by the 2D FEM simulation.

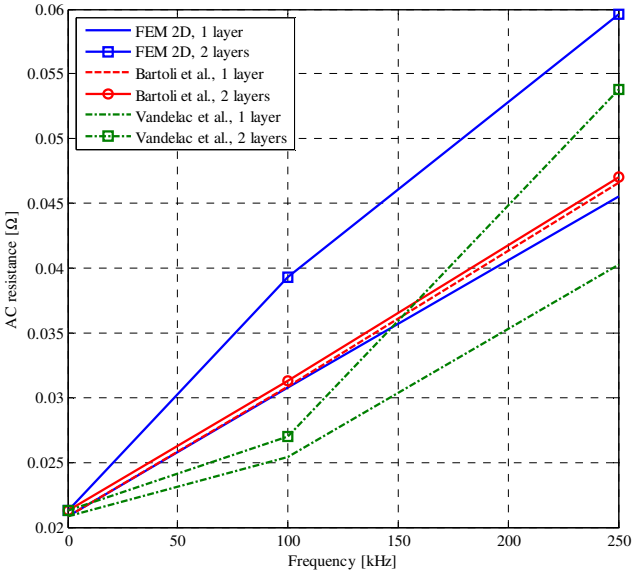


Figure 5.19: Effect of the large porosity factor on the calculation accuracy in the compared methods. The six turn winding is wound on a winding window with a width of 57.3 mm and the distance between 0.78 mm^2 wires is 10 mm in the single layer case and 26 mm in the double layer case.

To test the litz wire calculation with the method by Bartoli et al., a transformer for the resonant push-pull topology has been measured, calculated and simulated. The transformer had the following specifications:

- PM114/93 core and bobbin
- Primary winding: 2+2 turns, 48 mm^2 litz wire, 96 x 0.8 mm
- Secondary winding: 12 turns, 6.8 mm^2 litz wire, 200 x 0.2 mm

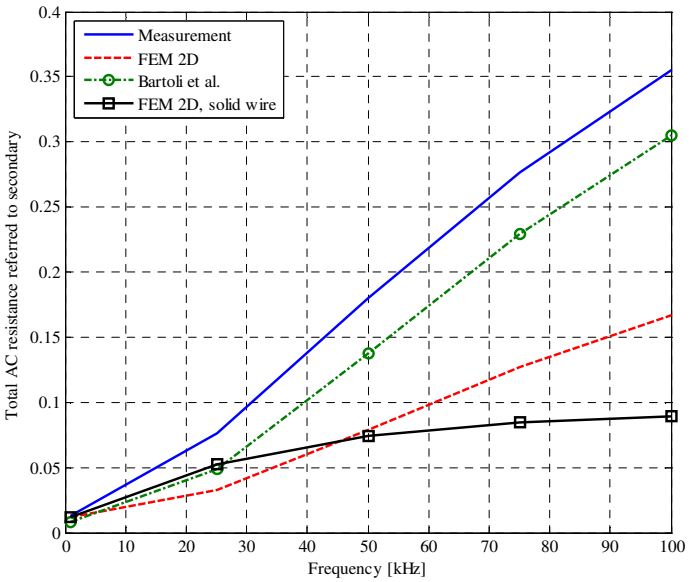


Figure 5.20: Measured, calculated and simulated AC resistance for a 4:12 litz transformer.

The calculated and simulated AC resistances do not include primary and secondary connection cables, which were included in the measurement. Considering an estimated ±3% measurement error from an imperfect short circuit and taking into account the variations in the transformer winding structure (the winding distances are not equal and the windings are not perfectly aligned) and the presence of the transformer core, the resistance estimate given by the Bartoli et al. method corresponds quite well to the measurement. The resistances given by the FEM simulator are much smaller than the measured and calculated values, but the comparison against an equivalent solid wire gives similar results in terms of the litz wire having a larger AC resistance at higher frequencies.

According to the ANSOFT PExprt modeller manual, the 2D FEM simulator does not directly model the litz wire as insulated twisted strands, but it converts the litz wire to an equivalent solid conductor with a diameter of

$$D = d_s \sqrt{n_s} \,, \tag{5.45}$$

where D is the round conductor diameter in Maxwell 2D, d_s is the individual strand diameter and n_s is the number of strands. The strands are taken into account by neglecting the eddy current effects in the 2D simulation and calculating the strand AC resistances by using an analytical method introduced by Lofti and Lee (1993).

To demonstrate the effect of wire separation on the calculated AC resistances, a transformer having the following specifications was measured:

- PM54/28/19 core and bobbin
- Primary winding: 7 turns, 6.2 mm^2 litz wire, 7 x 9 x 0.355 mm. One layer.

- Secondary winding: 50 turns, 0.75 mm^2 litz wire, 19 x 0.224 mm. Two layers.

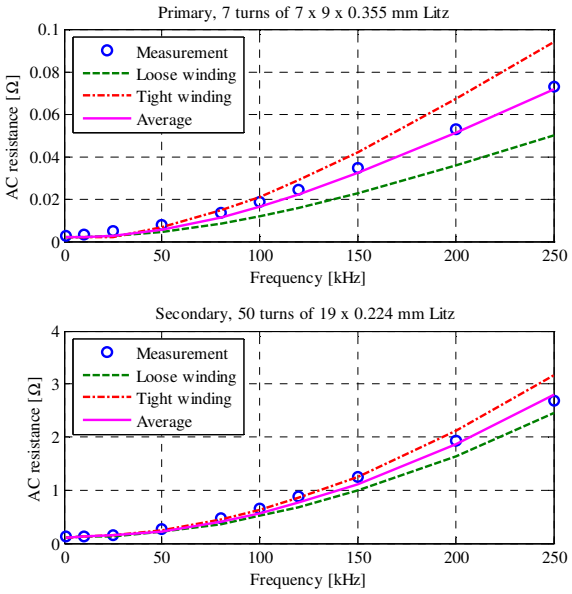


Figure 5.21: Measured and calculated winding resistances in a 7:50 litz transformer.

The effect of wire separation can be seen in the calculated results. The definition of a loose winding is that the wires are separated by a gap which is dictated by the winding window width, the number of turns and the nominal wire diameter. The tight winding is calculated so that the distance between the centers of the conductors is exactly the nominal wire diameter. In the practical winding, the distance between the conductors varies from turn to turn, and therefore, the resistances are calculated also with an average separation. The calculations with the average separation are in good correlation with the measured resistances.

5.3.4 Maximum power losses for a certain core

The evaluation of suitable core size for a certain power loss is based on the maximum allowable core temperature, which in this analysis is 100°C. The heat is transferred through radiation and convection based on the dimensions of the core and the winding. The area exposed to radiative heat transfer is the total vertical surface area and the area exposed to convective heat transfer is the total horizontal surface area. The radiative thermal resistance is calculated from (Mohan et al., 2003)

$$R_{\theta,\mathrm{rad}} = \frac{T_{\max} - T_{\mathrm{amb}}}{5.7 \cdot 10^{-8} EA_{\mathrm{c}} \left({T_{\max}}^4 - {T_{\mathrm{amb}}}^4 \right)}, \tag{5.46}$$

where E is the emissivity of the surface, A_c is the core area, T_{max} is the maximum core temperature and T_{amb} is the ambient temperature. The temperature unit is Kelvin. The convective thermal resistance is calculated from

$$R_{\theta,conv} = \frac{1}{1.34\,A_{vert}}\left(\frac{d_{vert}}{T_{max} - T_{amb}}\right)^{\frac{1}{4}}, \tag{5.47}$$

where A_{vert} is the total vertical surface area and d_{vert} is the maximum vertical height of the object. The temperature unit is Kelvin. The equation is valid for objects having a vertical height less than approximately 1 m (Snelling, 1988; Mohan et al., 2003) .

When the thermal resistances are known, the maximum allowable power losses for a certain temperature rise can be calculated from

$$P_{max} = \frac{T_{max}\left(R_{\theta,rad} + R_{\theta,conv}\right)}{R_{\theta,rad}\,R_{\theta,conv}} \tag{5.48}$$

The maximum allowable power losses for various ferrite cores and the parameters used in the calculation are given in Appendix A.

5.3.5 Optimal ratio between core losses and winding losses

The minimum losses in a transformer occur when the core losses and winding losses are equal or close to each other. The exact relation between the losses depends on the ratio by which the core losses decrease as a function of primary turns and how the winding losses are increased as the number of turns in increased. If we look at the core loss density versus the AC flux density graph from the N87 ferrite datasheet, it can be seen that the core loss density (and thus the core loss, as the core volume is constant) drops approximately 80% each time the AC flux density is halved. For the analysis the reduction coefficient is marked as $R = 0.20$.

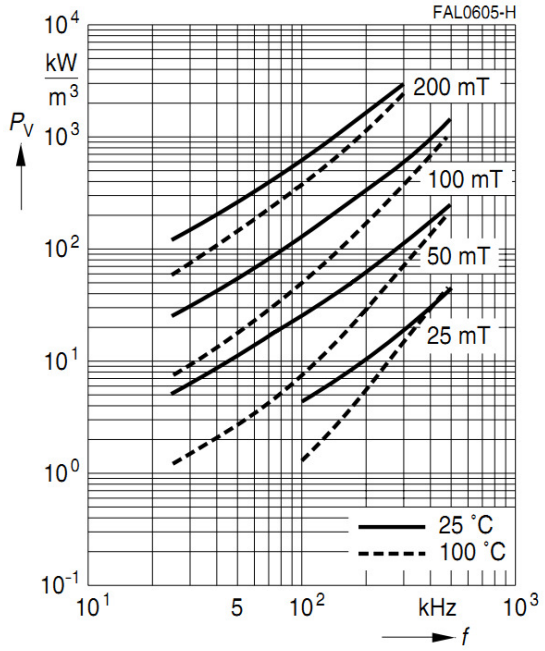


Figure 5.22: Behavior of the core loss density as a function of frequency and AC flux density in the N87 ferrite (Epcos, 2006).

The AC flux density is calculated from (McLyman, 2004)

$$B_{ac} = \frac{V_{pri} \cdot 10^4}{kN_{pri} A_c f}, \tag{5.49}$$

where V_{pri} is the maximum primary voltage, k is a waveform coefficient (4 for the square wave, 4.44 for the sine wave) and N_{pri} is the number of primary turns. If the other parameters remain constant but the number of primary turns in changed, the AC flux density is reduced by a factor of $1/N_{pri}$. If the core loss with one turn, indicated as $P_{core,init}$, is known, the core loss with N_{pri} primary turns can be approximated to be

$$P_{core,N} = P_{core,init} \cdot R^{\frac{N_{pri}}{2}} \quad , N_{pri} \geq 2 \ . \tag{5.50}$$

The core loss thus decreases exponentially with a rate determined by the material characteristics.

The winding losses, if considering only DC losses, are increased linearly by

$$P_{\text{winding, pri}} = N_{\text{pri}} R_{\text{dc,pri}} I_{\text{pri}}{}^2$$
$$P_{\text{winding, sec}} = nN_{\text{pri}} R_{\text{dc,sec}} \left(\frac{I_{\text{pri}}}{n} \right)^2, \tag{5.51}$$

where n is the transformer turns ratio. The AC winding losses are not increased linearly, but the ratio between AC and DC losses depends on the stacked winding layers and on the winding thickness in relation to the skin depth. Figure 5.23 presents the plot of (5.34) as a function of various conductor thicknesses and stacked winding layers.

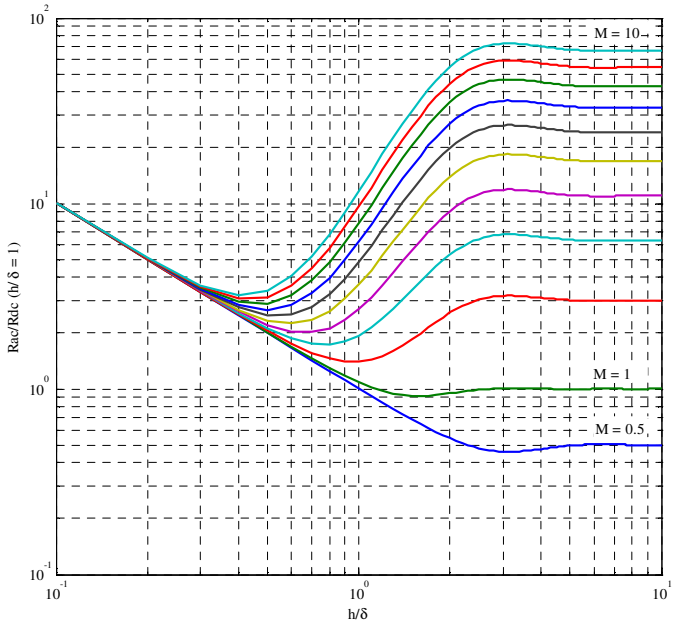


Figure 5.23: Ratio of AC winding losses to the DC losses of a conductor having a thickness of one skin depth.

It can be seen from Figure 5.23 that the lowest AC losses are obtained with a winding having a winding thickness of approximately 3δ, while the number of effective layers is 0.5. It can also be seen that increasing the conductor thickness beyond 6δ does not result in any significant change in winding losses.

The AC winding losses are now increasing according to

$$P_{\text{winding,pri}} = \varphi_{\text{pri}} \left[G_1(\varphi_{\text{pri}}) + \frac{2}{3} \left(\left(\frac{N_{\text{pri}}}{p} \right)^2 - 1 \right) \cdot \left(G_1(\varphi_{\text{pri}}) - 2G_2(\varphi_{\text{pri}}) \right) \right] \left(N_{\text{pri}} R_{\text{dc,pri}} \right) I_{\text{pri}}{}^2$$
$$P_{\text{winding,sec}} = \varphi_{\text{sec}} \left[G_1(\varphi_{\text{sec}}) + \frac{2}{3} \left(\left(\frac{nN_{\text{pri}}}{p} \right)^2 - 1 \right) \cdot \left(G_1(\varphi_{\text{sec}}) - 2G_2(\varphi_{\text{sec}}) \right) \right] \left(nN_{\text{pri}} R_{\text{dc,sec}} \right) \left(\frac{I_{\text{pri}}}{n} \right)^2 \tag{5.52}$$

where p is the number of primary-secondary intersections. The minimum number of effective layers (N_{pri}/p) in (5.52) can be 0.5. To find the equation for the optimal number of primary turns, the loss equations (5.50) and (5.52) can be combined, differentiated and solved with respect to N_{pri}. Figure 5.24 presents a comparison between the core and winding losses in a case where only DC winding losses are considered and in another where the AC winding losses are included.

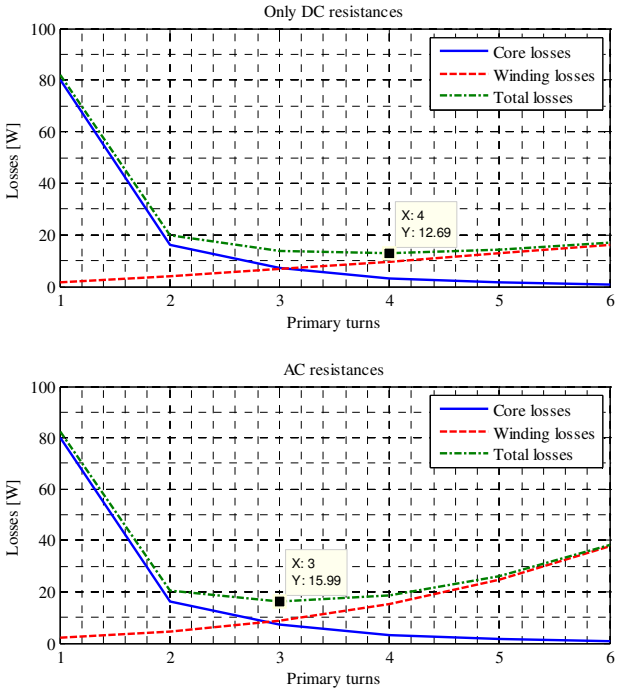


Figure 5.24: Core losses and winding losses as a function of primary turns when considering only DC winding losses (upper figure) and including AC winding losses (lower figure). All operational parameters are equal and the maximum $p = 4$.

In the previous example, the inclusion of the AC resistances decreases the optimal primary turn count by one turn compared to the case where only DC resistances are included. At low currents, the optimal turns count is higher since the core losses are dominating. As the current is increased, the optimal turns count decreases since the winding losses begin to dominate. Generally speaking, the optimal number of primary turns in the cases where also AC winding losses are included is the nearest integer to the core loss and winding loss intersection point.

5.3.6 Switching frequency and losses

A decrease in the switching frequency increases the skin depth and thus the maximum effective conductor thickness. On the other hand, the number of primary turns and thus total transformer turns must be increased to compensate the increased AC flux density.

As the switching frequency changes, the conductor skin depth changes by $\sqrt{(1/f)}$. The AC flux density changes by $1/(N_{pri}f)$. To maintain the same AC flux density with a lower frequency f_{low}, the number of primary turns must be increased by a ratio of f_{init}/f_{low}. From Figure 5.22, it can be approximated that the core loss density and thus the core loss drops 54% each time the frequency is halved. The change in total losses as the frequency and the turns ratio are changed can be written as

$$P_{total}(f) = P_{core,\,init}\, R^{0.5\left(\frac{f_{init}\,X}{f_{init}}\right)} + \frac{f_{init}\,X}{f_{init}}\sqrt{\frac{f_{init}}{f_{init}\,X}}\,I_{pri}^{\,2} + n\frac{f_{init}}{f_{low}}\sqrt{\frac{f_{init}}{f_{init}\,X}}\left(\frac{I_{pri}}{n}\right)^2 \qquad (5.53)$$

where X is the divider for the frequency. Figure 5.25 presents the normalized core and DC winding losses with three different frequencies and various transformer turn ratios.

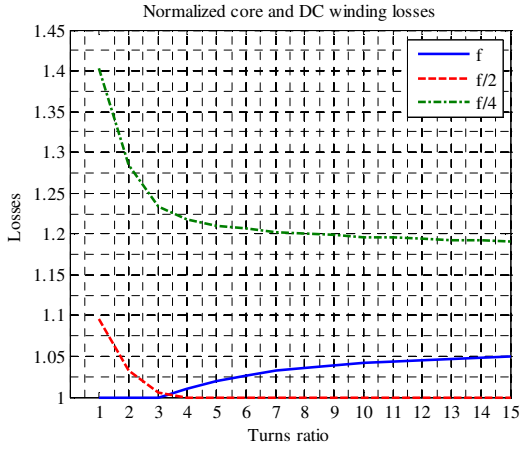


Figure 5.25: Idealized behaviour of core and DC winding losses, as the frequency is changed under the condition that the AC flux density is unchanged.

As the frequency is halved, the total DC winding losses are increased with a ratio of $2*\sqrt{2}$. When the frequency is reduced to one fourth of the initial frequency, the winding losses are increased with a ratio of 4. The corresponding reductions in the core losses with the core material in question are 0.46 and 0.21, respectively. The increase in the winding losses is likely to exceed the decrease in the core losses at some lower frequency, as can be seen in Figure 5.25. Also, if considering the AC winding losses, the increase in the turns count requires more extensive interleaving in order to maintain the same R_{ac}/R_{dc} ratio. If the number of primary-secondary intersections cannot be increased, the ratio in which the winding losses are increased is further multiplied with the R_{ac}/R_{dc} ratio. The resistance reduction at low frequencies results only from the increase in the skin depth. Consequently, if the core window space constraints do not allow the increase in conductor thickness, the losses will inevitably increase as the frequency is decreased.

Let us consider another case where the core loss density is kept unchanged as the frequency changes. This allows the AC flux density to be higher and the primary turn count smaller. When approximating from Figure 5.22 that the AC flux density can be 50% higher as the frequency is

halved, the primary turns count needs to be increased only by 4/3 instead of 2. Since the core losses are now unchanged, the total losses can now be written as

$$\begin{cases} P_{\text{total}}(f) = P_{\text{core}} + {I_{\text{pri}}}^2 + n\left(\frac{I_{\text{pri}}}{n}\right)^2, & f_{\text{low}} = f_{\text{init}} \\ P_{\text{total}}(f) = P_{\text{core}} + \frac{2X}{3}\sqrt{\frac{f_{\text{init}}}{f_{\text{init}}\,X}}{I_{\text{pri}}}^2 + n\frac{2X}{3}\sqrt{\frac{f_{\text{init}}}{f_{\text{init}}\,X}}\left(\frac{I_{\text{pri}}}{n}\right)^2, & else \end{cases} \tag{5.54}$$

Figure 5.26 presents (5.54) as plotted with various transformer turns ratios.

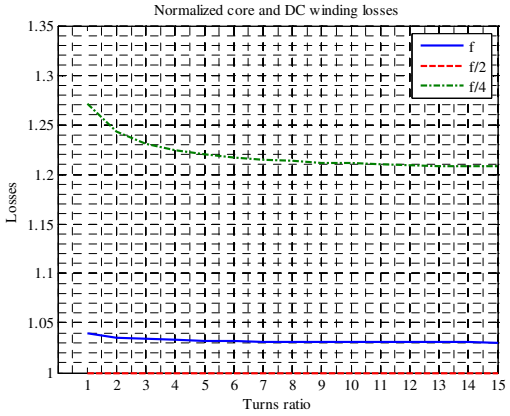


Figure 5.26: Idealized behavior of core and DC winding losses, as the frequency is changed under the condition that the core loss density is unchanged.

The frequency after which the resistance multiplier becomes greater than unity is $0.44f_{\text{init}}$. However, since the winding window dimensions may limit the maximum conductor thickness, the advantages gained from the increased skin depth and utilizable conductor thickness may be lost.

5.3.7 Duty cycle and losses

The transformer can be designed with a smaller turns ratio if the converter is operated with a higher duty cycle. However, the larger primary voltage requires more primary turns in order to limit the AC flux density and core losses. The transformer RMS current also changes as a function of the duty cycle, as seen from the equations in Appendix A. Figure 5.27 presents the relative differences in transformer primary currents as a function of the effective duty cycle.

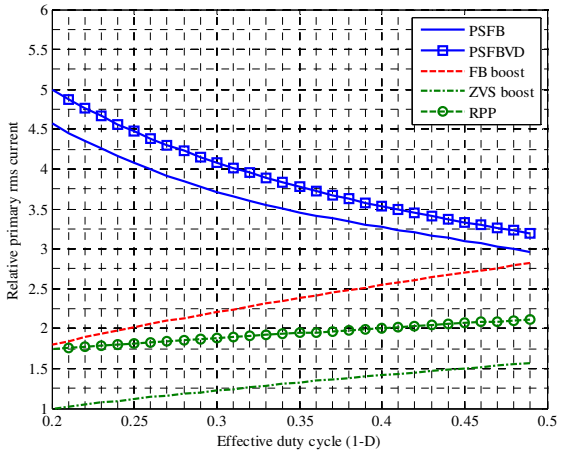


Figure 5.27: Relative differences in transformer primary currents as a function of the effective duty cycle (1-*D*).

The primary current in the voltage-fed topologies is decreased as the effective duty cycle is increased because the primary voltage is constant and in order to transfer the same power during a longer period of time the current can be lower. In the current-fed topologies, the primary current is increased as the effective duty cycle is increased since the primary voltage is decreased and more current is needed to transfer a certain power.

In the voltage-fed converters having a maximum primary voltage equal to the input voltage, the AC flux density does not change with the duty cycle, and thus the number of primary turns does not need to be increased in order to reduce core losses. In the current-fed converters, the primary voltage is increased along with the required number of primary turns, but the required turns ratio is decreased at the same time. To evaluate the combined effect of all of the changing parameters, a MATLAB script is written, finding the minimum loss combinations under the constraints given in Table 5.17

Table 5.17: Transformer design constraints used in the transformer loss comparisons.

Design parameter	Value
Nominal input voltage	50 V
Nominal output voltage	660 V
Nominal input power	10 kW
Magnetic core	PM114/93, N87
Maximum number of primary-secondary intersections	16
Minimum number of layers M	0.5
Number of primary turns	1-10
Layer insulator thickness	0.05 mm
Primary-secondary insulator thickness	0.13 mm
Foil current density	10-1000 A/cm^2
Maximum fill factor including insulators	90%
Copper foil width	90% of the window width
Input/output inductor ripple	5% of nominal current
Voltage-fed converter output inductor	1 mH
Resonant half period length	(1-D)

The transformer losses at various duty cycles are scaled so that the minimum loss is 1. Figure 5.28 presents the minimum transformer losses obtained with the constraints of Table 5.17.

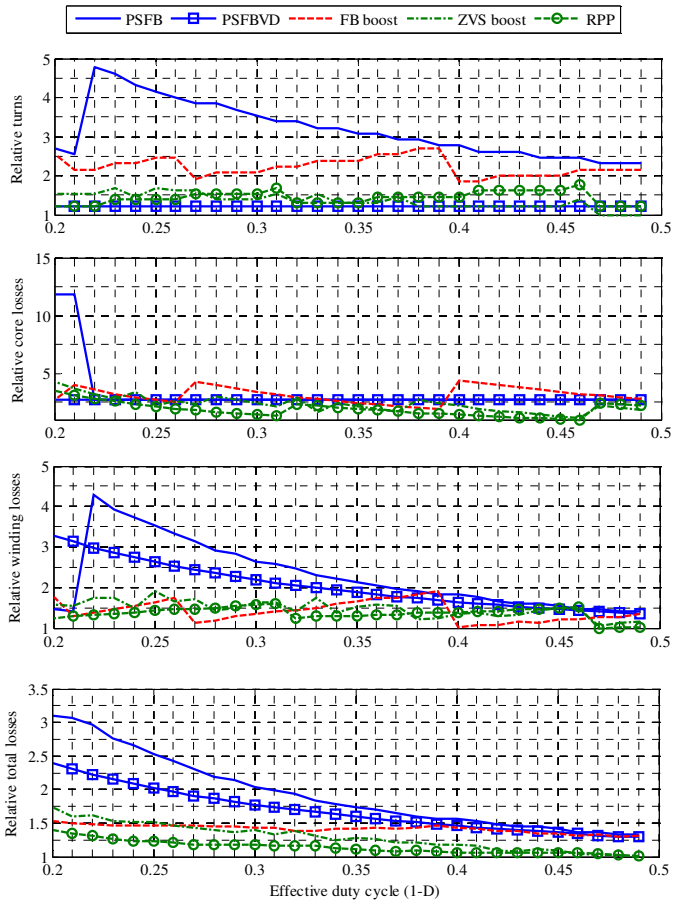


Figure 5.28: Behavior of losses as a function of the effective duty cycle.

The PSFB and PSFBVD transformers are more sensitive to duty cycle variations than the current-fed topologies. The reason for this is that in the voltage-fed topologies the transformer RMS currents are changing more steeply as a function of the duty cycle than in the current-fed topologies. The PSFB topology also requires more turns ratio regulation due to the output inductor voltage loss. The conclusion is that in terms of transformer losses, the best operating area is close to the maximum effective duty cycle. The same conclusion was reached also with the inductors.

5.3.8 Litz wire design considerations

The use of the litz wire allows more winding turns to be fitted into one layer, which reduces the proximity effects caused by stacked winding layers. However, the winding window fill factor is not as high as with rectangular conductors, as there will be empty space between the round conductors. As there is less utilizable winding window space to be used for copper, the round wire DC resistance will be higher for the same window utilization ratio.

Figure 5.29 presents the plot of (5.36) as a function of various strand diameters and numbers of strands. The AC resistances are scaled in relation to the DC resistance of one strand having a diameter of one skin depth.

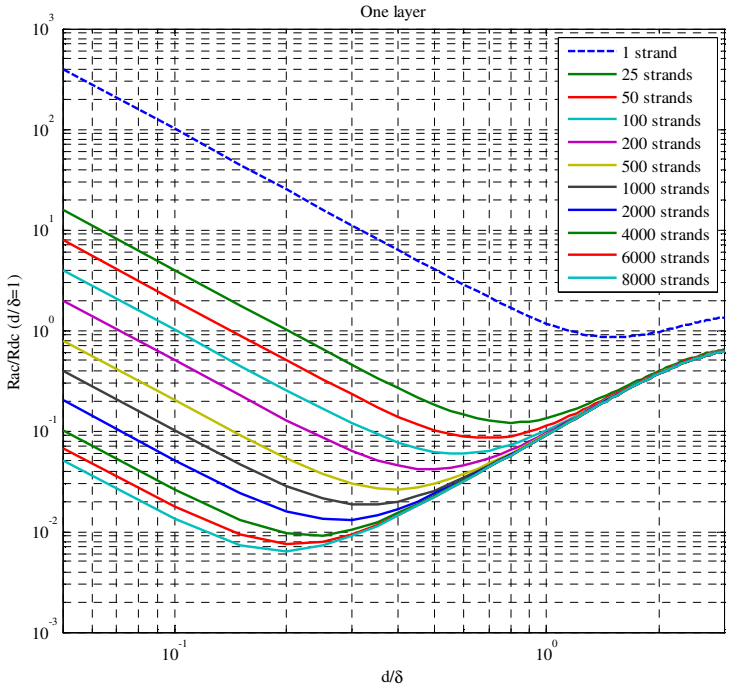


Figure 5.29: Ratio of AC winding losses to the DC losses of a strand having a thickness of one skin depth. The winding is in one layer.

It is seen from Figure 5.29 that when the number of strands is increased, the lowest AC losses are not obtained with the thinnest strands although they provide the smallest AC resistance ratio. The reason for this is the increased DC resistance. The thinnest strands have the thinnest insulators, but the insulator thickness is not in direct proportion to the wire diameter. In small-diameter conductors, the proportion of the insulator in the total cross-section area is greater than in large-diameter conductors.

The strand insulator thickness in mm for wire sizes between 14 and 30 AWG can be estimated from (Sullivan, 1999)

$$d_{\text{insulator}} = 0.0254\, e^{X - \frac{5\,AWG}{224}}, \tag{5.55}$$

where X is 0.518 for a single build insulation and 0.818 for a heavy build one (double insulation). The equations are based on curve fits of manufacturer wire data. A better correlation of the insulator thickness for wires in the range of 30 and 60 AWG is obtained from (Sullivan, 1999)

$$d_{\text{insulator}} = \frac{\left(d_{\text{ref}} \alpha \frac{d_{\text{s}}}{d_{\text{ref}}} \right)^{\beta} - d_{s}}{2}, \tag{5.56}$$

where d_s is the strand diameter excluding the insulation layer, $\alpha = 1.12$ and $\beta = 0.97$ for a single build insulation and $\alpha = 1.24$ and $\beta = 0.94$ for a double build insulation with a reference diameter of d_{ref}, chosen to be the diameter of a 40 AWG wire (0.079 mm).

The optimal strand diameter for a litz wire having several thousand strands and one winding layer per portion is approximately 0.2δ and the optimal strand diameter shifts towards the skin depth as the number of strands is decreased. It is noteworthy that as the strand diameter approaches the skin depth, the increase in the number of strands does not change the overall AC resistance. If the litz wire cross-section area needs to be increased in order to achieve a lower resistance, the strand diameter must be decreased accordingly. Figure 5.30 presents the relative AC winding losses for a case of two winding layers. The behavior is otherwise similar than with one winding layer, but the optimal strand diameter is reduced and the resistances are increased.

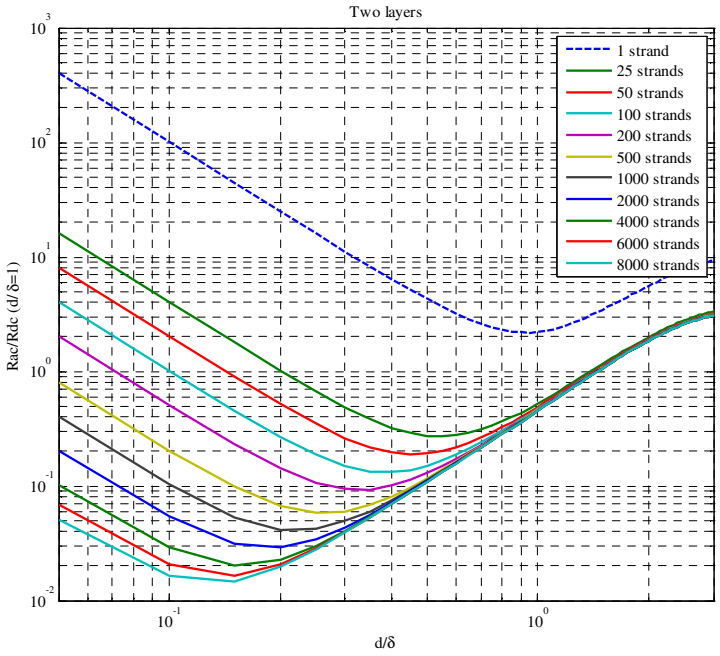


Figure 5.30: Ratio of AC winding losses to the DC losses of a strand having a thickness of one skin depth. The winding is in two layers.

To increase the litz wire current capacity, it is more preferable to split the large wire into multiple parallel wires instead of increasing the wire diameter. If the turns are paralleled, they must be kept in the same winding layer for equal current distribution. For example in Figure 5.29, the AC resistance increase when moving from a 4000 strand wire to a 2000 strand wire is

66%, but the when considering the halved current, the total AC losses of the 2000 strand wire would be 41.5% lower.

To compare the AC resistances between a litz winding and a foil winding, equations (5.34) and (5.36) are plotted in the same figure so that all resistances are scaled to the DC resistance of a foil having a thickness of one skin depth. The foil diameter is the same as the litz wire strand diameter, and to obtain equal cross-section areas and thus DC resistances, the foil width is increased accordingly. Figure 5.31 presents the comparison with two different strand counts.

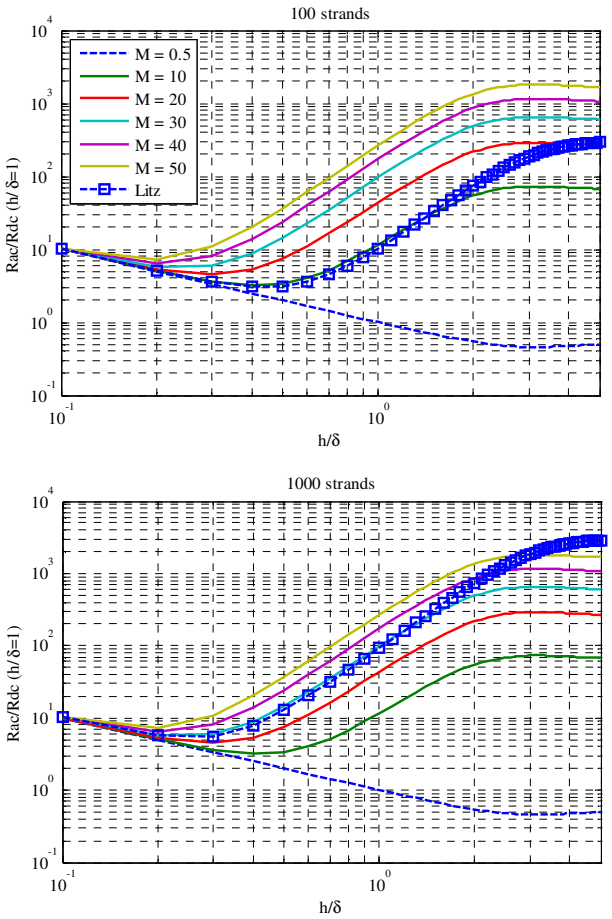


Figure 5.31: Litz wire AC resistances as a function of the strand diameter compared to foil winding AC resistances when the DC resistances are equal. The calculation is performed with one litz winding layer per portion.

With a strand count of 100, the litz wire can outperform the foil winding if the foil winding has more than 10 stacked winding layers. When the strand count is increased to 1000, the litz wire AC resistance ratio increases steeply after the optimal strand diameter is exceeded and thus the foil winding has a smaller AC resistance until the number of stacked winding layers exceeds 30. Figure 5.32 illustrates the AC winding losses in a case where the litz winding is split in two

parallel wires wound in the same winding layer. The reduction in AC losses is obvious compared to the single wire case.

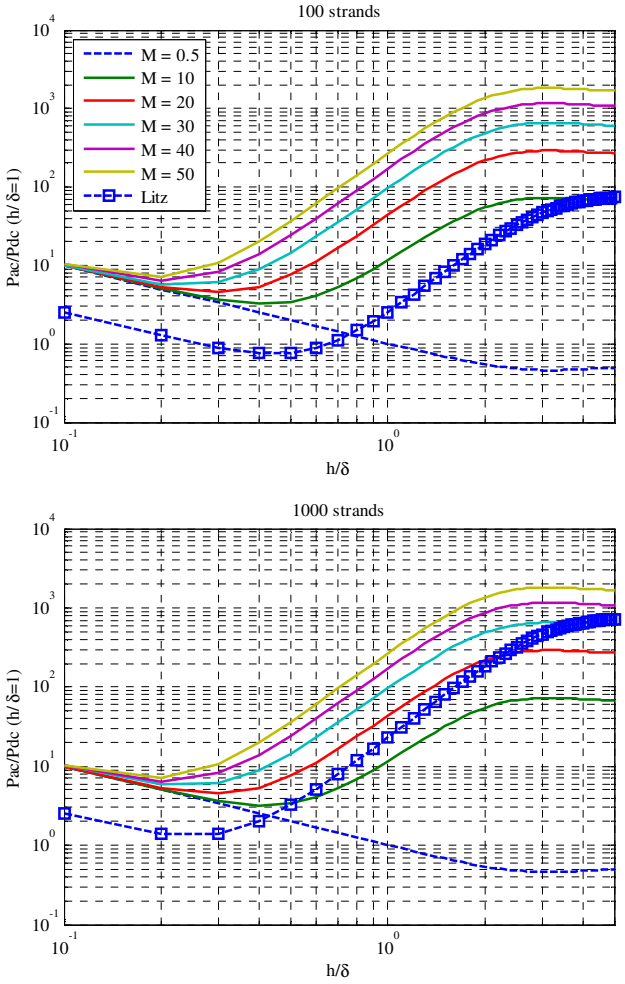


Figure 5.32: Litz wire AC losses as a function of the strand diameter compared to foil winding AC losses when the DC losses are equal. The calculation is performed with one litz winding layer per portion and two litz wires in parallel.

Based on the analysis above, it can be concluded that the litz wire is advantageous when the number of turns in a winding is large and when the current is relatively small, enabling a small strand count with an optimal (smaller than skin depth) strand diameter. It is also preferable to use only one litz winding layer per portion to maintain the lowest possible AC resistance ratio. In primary windings having a small turns count and high current, the optimal litz wire has a large number of strands, a very small strand diameter and a large overall diameter, which results in a poor fill factor compared with a foil winding.

In these comparisons, the fill factor limitations were neglected. In practice, the litz wire has a lower fill factor, and consequently, a litz winding having an equal DC resistance with a foil winding would require a larger winding window, which in turn would allow a foil winding with even lower DC resistance, and so forth. However, in applications where there is a relatively large number of turns and not much winding interleaving (if there are many stacked foil windings), the litz wire can have a lower AC resistance despite the higher DC resistance.

Figure 5.33 illustrates the winding resistances in a case where 50 secondary turns are fitted in an ETD54 bobbin. It is assumed that 50% of the available winding window height is allocated for the secondary winding and that a 0.05 mm thick insulator is used between the foil winding layers. The winding window width is assumed to be fully utilized and the litz wires are tightly packed. The litz wire strand counts are selected based on the lowest achievable AC resistance when considering commercially available wires with a maximum diameter of 1.47 mm (HM Wire International Inc., 2009). The operating frequency in the example is 50 kHz corresponding to a skin depth of 0.29519 mm.

It is seen in Figure 5.33 that with one litz winding layer (corresponding to two primary-secondary intersections and 25 stacked foil winding layers), the maximum usable strand diameter when neglecting external wire insulators would be 0.72δ (0.21 mm) and this strand diameter would also result in the lowest litz winding AC resistance. The nearest commercially available litz wire satisfying the maximum outer diameter requirement from HM Wire catalogs has a strand diameter of 0.54δ. With this strand diameter, the litz winding AC resistance would be approximately equal to a foil winding having 30 stacked layers and a copper foil diameter of 0.48δ (0.14 mm). However, since the foil diameter could be reduced to 0.43δ (0.127 mm), the foil winding having 25 stacked layers would have a lower AC resistance than the litz winding.

If there are two stacked litz winding layers (corresponding to one primary-secondary intersection and 50 stacked foil winding layers), the commercial litz wire with a suitable outer diameter and the lowest AC resistance will have a strand diameter of 0.27δ (0.08 mm). With this wire, the litz winding will have a lower AC resistance than a foil winding with 50 stacked layers and a copper foil having a diameter of 0.43δ (0.127 mm).

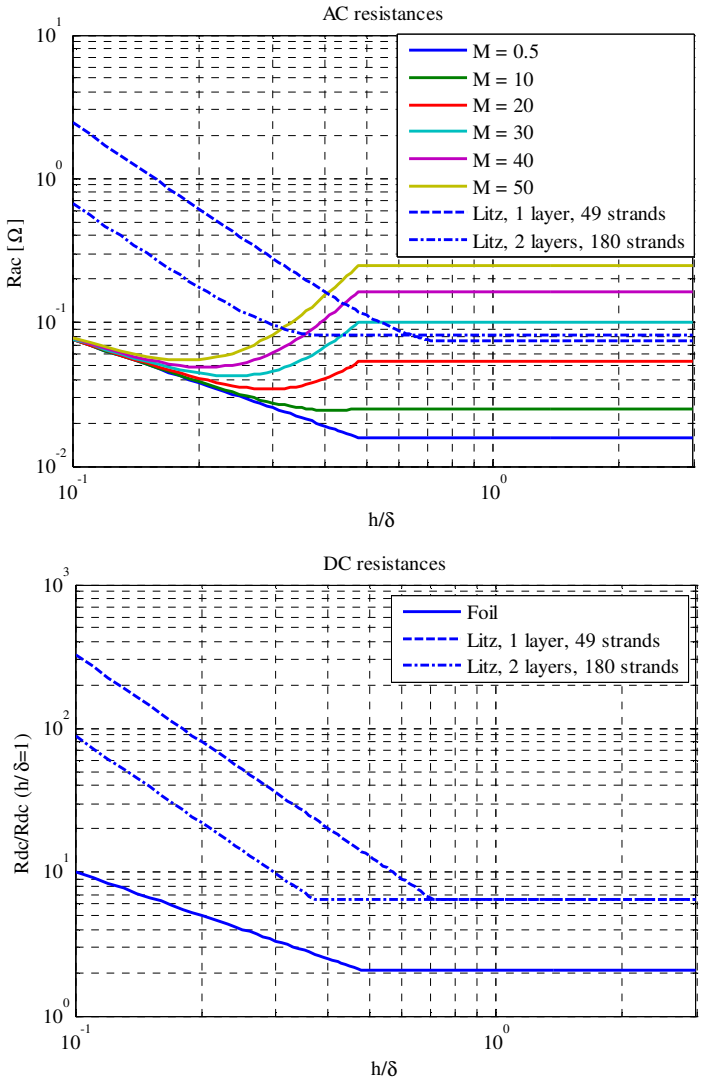


Figure 5.33: Foil and litz winding AC resistances and normalized DC resistances. The DC resistances are normalized with the DC resistance of a foil having a thickness of one skin depth. The flat portions in the curves indicate that the maximum strand (or foil) diameter is reached.

The litz winding will benefit from an increased operating frequency since the strand count and strand diameter can be adjusted quite flexibly, whereas the foil winding has practical limitations concerning the minimum manageable foil thickness.

5.3.9 Differences in transformer structure and losses between topologies

The required transformer turn ratios for a given input-to-output voltage conversion ratio are given in Appendix A. It is assumed that the output capacitor is large enough to hold the output

voltage nearly constant during the period when voltage is not applied to the transformer secondary. The output capacitor is charged to the secondary peak voltage minus the voltage drops. The general design constraints are listed in Table 5.17 and the maximum effective duty cycle is 0.43.

Table 5.18: Transformer configurations providing the minimum losses under given design constraints.

Topology	N_{pri}/h_{pri} **[mm]**	N_{sec}/h_{sec} **[mm]**	p	P_{core}	P_{pri}	P_{sec}	P_{total}	D_{opt}
PSFB	3/0.9	46/0.14	6	4.5	14.8	5.8	25.1 W	0.43
PSFBVD	2/0.9	14/0.2	4	11.6	12.5	6.8	30.8 W	0.43
FB boost	3/0.9	36/0.16	6	6.5	11.2	5.1	22.8 W	0.43
ZVS boost	4/0.9	12/0.33	8	3.4	4.6	3.8	2 x 12 W	0.43
RPP	3+3/0.9	18/0.34	12	5.3	13.3	3.1	21.7 W	0.44

The differences in transformer losses between the topologies will be rather small if the transformer structure is optimized. The primary conductor diameter was approximately 3δ in all topologies, which is understandable if looking at Figure 5.23 with $M = 0.5$. The secondary conductor thicknesses are also close to the optimal values, when observing the number of stacked winding layers and Figure 5.23.

The ZVS boost topology has the lowest losses per transformer due to a low turns ratio and RMS current, but since there are two transformers, the total losses are very close to the RPP transformer losses. The losses in the RPP transformer are strongly dependent on the maximum number of primary-secondary intersections. Since there are two primary windings instead of one, there have to be twice as many primary-secondary intersections in order to maintain the same number of effective layers as in the single primary winding transformers.

The use of the ZVS boost topology could be justified by the possibility to use smaller transformer cores efficiently, and since the smaller cores are typically less costly, savings can be achieved in the initial costs. How great is this difference? Figure 5.34 presents the transformer losses and costs for the compared topologies when operating under the constraints of Table 5.17. The cores used in the comparison are listed in Appendix A and the prices for the cores and bobbins are obtained from the websites of Elfa Distrelec and Farnell.

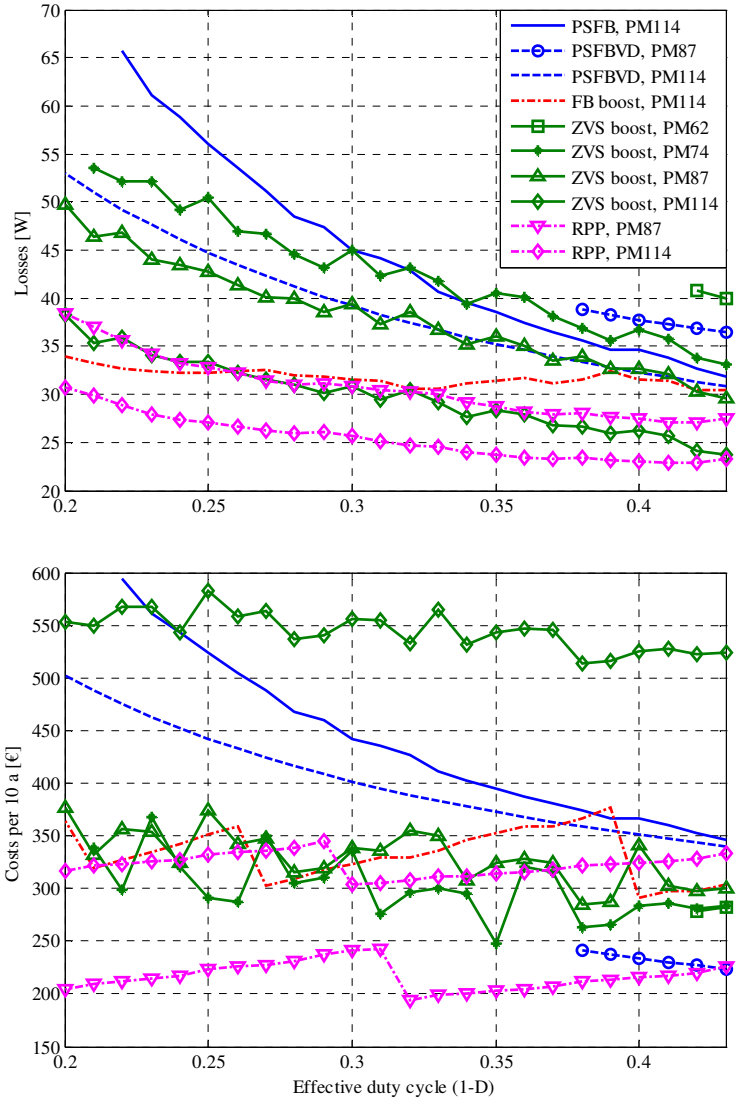


Figure 5.34: Transformer losses and costs in a ten-year operating period. The short graph lines of the smaller cores indicate that the losses for these particular cores become too high after a certain effective duty cycle.

The selection of available cores is largest when using the ZVS boost topology. By using a smaller core, the small initial costs can overcome the increased operating costs (increased losses) over the operating period. The lowest costs were obtained with the RPP topology due to the smallest losses and the moderate initial cost of the PM87 core assembly and its windings. At low power levels, the costs are mainly dictated by the core assembly costs since the losses are very low. Therefore, the PSFBVD, ZVS boost and RPP topologies allowing the largest selection of cores will have the lowest costs.

5.4 Summary

With appropriate component optimization, the resonant push-pull topology can have the lowest inductor and transformer losses and costs. The resonant push-pull transformer design is more complicated than in the other topologies because there are two primary windings. Thus, the required number of primary-secondary intersections is doubled in order to achieve similar AC resistance ratios as in the transformer having only one primary winding. In general, the current-fed converters are more flexible in terms of magnetic component design than the voltage-fed ones. Current-fed converters may have the following advantages:

- The required inductance for a certain current ripple is smaller, thus enabling smaller and more efficient inductors.
- The transformer turns ratios are smaller, thus simplifying the optimization of the winding layout.
- The changes in losses as a function of the duty cycle and frequency are not as steep as in the voltage-fed converters.

The inductor and transformer losses tend to increase as the duty cycle is increased in the current-fed converters or decreased in the voltage-fed ones. The losses are also increased as the switching frequency is decreased.

The optimal inductor and transformer designs are found near the point where the core losses and the winding losses intersect. In gapped inductor cores, the situation where the gap losses exceed the core losses indicates that the core in question has an excessively small area product for the given operating parameters. In order to maintain a large flux in a small core, a large air gap is needed. The increased air gap results in increased gap losses and a large fringing flux factor. As the fringing flux factor increases, more winding turns are required in order to achieve the desired inductance. The increased number of turns may also require thinner conductors, which increases the winding losses.

The litz wire can be a worthy alternative to copper foil in transformer windings if the following considerations are taken into account:

- The litz wire strand diameter is chosen to be a certain fraction of the skin depth according to the number of strands (Figures 5.29 and 5.30).
- A litz wire with a small number of strands performs better than a wire with a large number of strands compared to a foil winding having an equal DC resistance.
- After a certain number of stacked foil winding layers, a litz wire with an equal DC resistance has a lower AC resistance (Figure 5.31). In step-up transformers, this situation is more likely to occur on the secondary side having a large turns count.
- When the fill factor limitations are taken into account, the foil winding is advantageous over the litz winding even with a rather large number of stacked foil layers (Figure 5.33). The litz winding is beneficial at higher frequencies, where the minimum manageable foil thickness becomes a limiting factor.
- The litz wire AC resistance can be effectively reduced if the large wires can be divided into smaller wires and wound parallel in one layer (Figure 5.32). This, however,

requires that the wire diameter is not reduced by a factor larger than $\sqrt{N}$, where N is the number of parallel wires.

- At the optimum strand diameter, the litz wire AC to DC resistance ratio $F_r = 2$. This is demonstrated in Figure 5.35. A similar result was obtained also in the study of Wojda and Kazimierczuk (2012) using modified Dowell's equations.

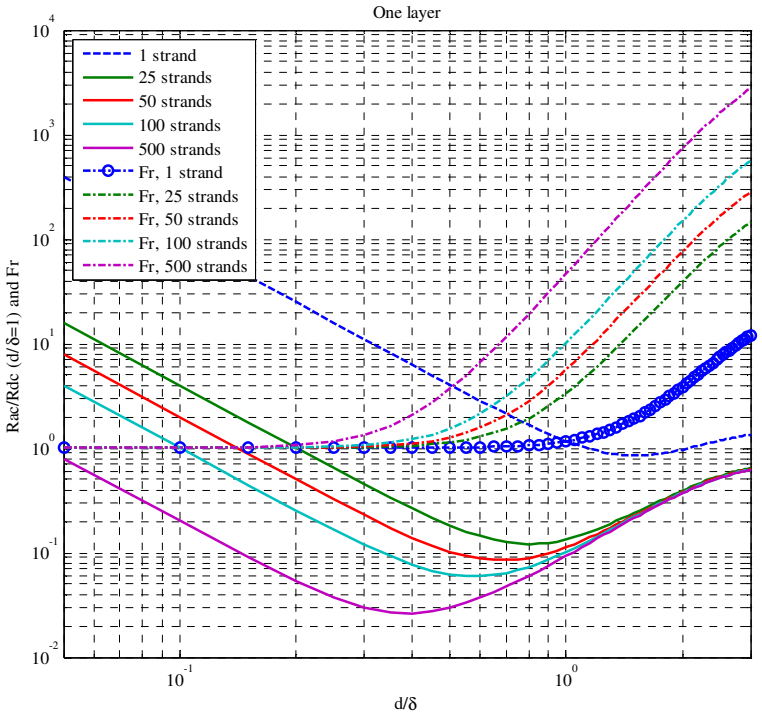


Figure 5.35: Ratio of AC winding losses to the DC losses of a strand having a thickness of one skin depth and the corresponding AC to DC resistance ratios. The winding is in one layer.

6 Summary and future work

To illustrate the differences in the loss distributions between the compared topologies, the calculated losses from the previous chapters have been summarized in Table 6.1. The transistor losses are for three parallel transistors and the diode losses are for three parallel SiC diodes (to assume equal current distribution).

Table 6.1: Summary of the calculated losses in the compared topologies. The components used in the calculations are given in Appendix A and in the chapters 4 and 5.

Topology	MOSFET cond.	MOSFET sw.	Diode cond.	Diode sw.	Inductor	Transformer	Eff.
PSFB	45 (16%)	80 (29%)	117 (43%)	0,5 (0%)	6,4 (2%)	25,1 (9%)	97,3%
PSFBVD	56 (31%)	11 (6%)	85 (46%)	0,5 (0%)	0 (0%)	30,8 (17%)	98,2%
FB boost	37 (20%)	52 (29%)	67 (37%)	0,5 (0%)	1,9 (1%)	22,8 (13%)	98,2%
ZVS boost	72 (29%)	37 (15%)	97 (39%)	0,3 (0%)	18,6 (7%)	24 (10%)	97,5%
RPP	72 (33%)	37 (17%)	85 (39%)	0,5 (0%)	1,9 (1%)	21,7 (10%)	97,8%

Based on the analysis, it can be stated that in the given operating conditions, the FB boost and PSFBVD topologies have the ability to provide the lowest losses when operating under the conditions of Table 1.1. However, the PSFBVD efficiency advantages are shadowed by the narrow input voltage range, which results from the fact that the peak primary voltage cannot be controlled and the regulation provided by the output resonant circuit is quite limited at light loads (Figure 2.18). The PSFB topology, on the other hand, has the highest losses and costs under the given design constraints.

The efficiency differences between the topologies are quite small (within a few percentage points) if every topology is optimized to the maximum. However, if the level of optimization is reduced for reasons such as manufacturing complexity or cost, the efficiency differences between the topologies are likely to increase. For example, in case of transformers the level of winding interleaving has a great impact on transformer losses (see, for example, Figures 3.18 and 3.23 (a)) and also on semiconductor switching losses, as described in chapter 4.

Even though the converter efficiencies can be quite close to each other, there are some distinctive differences in the required component costs in order to achieve these efficiencies. In the given operating conditions, the RPP and PSFBVD topologies can provide the lowest costs due to low transistor and diode count as well as relatively inexpensive magnetic components. On the other hand, the RPP as well as the ZVS boost require clamp capacitors in the primary and since these capacitors must be dimensioned as high current DC capacitors, the total capacitor costs can be quite high.

In general, the current-fed converters have many favorable characteristics in low voltage, high current applications, such as a high voltage conversion ratio, low secondary rectifier losses and tolerance for switching asymmetries. The current-fed converters also provide a wide input voltage range and the changes in overall losses as a function of the duty cycle and frequency are not as steep as in the voltage-fed converters.

The factors with the greatest impact on the efficiency and cost in the topologies compared are discussed next.

PSFB

The large circulating currents cause high conduction losses in the intrinsic diodes of transistors S_1 and S_3. The turn-off losses of these transistors are also inevitably high due to a large current at turn-off. Transistors S_2 and S_4 can be turned off while only the magnetizing current is flowing through the transistors if the leakage inductance is small enough to enable hard switching. The transistor conduction losses increase rapidly as the duty cycle is decreased since the transistor RMS current changes steeply as a function of the duty cycle. The same observation can be made about the transformer winding losses. The costs are highly increased by the large number of SiC diodes. A passive or active snubber would eliminate the need for additional diodes, but of course, not even the snubber circuit comes without losses and costs. The transformer losses for a fully zero voltage switched PSFB were calculated using a copper foil transformer. In order to achieve adequate leakage inductances, the number of intersections had to be reduced to one and the insulator thicknesses needed to be increased, leaving less space for copper. This resulted in higher winding losses compared to the partially zero voltage switched case. A more suitable solution in the fully zero voltage switched case would be a wire winding or a combination of copper foil and wire winding.

PSFBVD

Since the primary circuit can be operated with both zero current and zero voltage switching and the secondary circuit with zero current switching, the switching losses are very small. It is easier to reduce the transformer losses than in the PSFB topology due to a lower number of turns, although the transformer RMS currents are higher due to the resonant operation. The possibility to operate the topology without a separate filter inductor makes a great difference in both losses and costs.

FB boost

The FB boost topology has the lowest transistor conduction losses among the topologies compared. The transistor turn-off losses tend to be high since the transistor voltage is pulled to the off-state voltage before the drain current starts to decrease. The turn-off losses can be reduced by using a fast gate drive and by minimizing the stray inductances.

The FB boost also has the lowest current average and RMS current stress in the secondary rectifier diodes. As it is advantageous to minimize the transformer leakage inductance in this topology, the rectifier diode *di/dt* can be high. The hard switching operation combined to the fast current transitions requires the usage of SiC diodes, which have negligible switching losses. Since the SiC diodes had weaker forward characteristics compared to the Si diodes, the diode conduction losses in the FB boost topology were higher than in the zero current switched

topologies using Si diodes. The overall costs were also greatly increased by the high cost of the SiC diodes.

ZVS boost

The ZVS boost topology has the lowest losses and costs per single transformer and single rectifier diode. However, the total transformer and rectifier losses are not very low since there are two transformers and double the amount of rectifier diodes compared to other topologies having a voltage doubler secondary. The required input inductor inductance to achieve a certain current ripple is $2D/(D\text{-}0.5)$ times higher than in the other current-fed topologies. The applied volt-seconds per period is DT, while in the other current-fed topologies it is $(D\text{-}0.5)T$. The current in one ZVS boost inductor is half of the total input current.

RPP

The resonant push-pull topology enables rectifier diode losses as low as the PSFBVD topology, but lower transformer and transistor conduction losses at lower effective duty cycles. The resonant push-pull transformer can be made efficient because the transformer RMS currents are relatively low and the total number of turns is low. However, since there are two primary windings, the required optimization effort is greater than in transformers with only one primary winding. As in the ZVS boost, the overall efficiency is degraded by the requirement of high voltage transistors having an increased on-state resistance.

General remarks

When using diodes with similar forward characteristics, the topologies utilizing hard switching and a diode bridge secondary can achieve lower diode conduction losses than the topologies utilizing sinusoidal resonance and a voltage doubler. This was demonstrated in chapter 4. The paralleling of diodes is less effective than the paralleling of MOSFETs due to a smaller decrease in the conduction losses. As shown in Table 6.1, the diode conduction losses were a largest source of losses in all topologies.

As demonstrated in chapter 5, the inductor scaling limitations are related to the required area product. The only topology struggling with inductor scaling at 10 kW was the ZVS boost in spite of the lower current compared to the other current-fed topologies. On the other hand, the ZVS boost topology has the lowest transformer area product requirement compared to the other topologies. As can be seen from Figure 5.34, the selection of suitable transformer cores becomes narrow at the 10 kW power level. If scaling upwards in power, the only viable core is PM114 or an equivalent with a large effective area.

A solid wire or a litz winding can be beneficial in topologies having a large turns count in the inductor or the transformer. The winding selection criteria were discussed in chapter 5. Although the AC resistances could be decreased more with a wire than with a copper foil, the leakage inductances tend to be higher when using a wire winding. With the same number of primary-secondary intersections and copper areas, the winding portion height is greater with a wire than with a foil. In resonant or zero voltage switched topologies the leakage inductance can be effectively utilized, but especially in the full-bridge boost topology the larger leakage inductance is a hindrance.

6.1 Suggestions for future work

In this thesis, the optimization efforts have concentrated on individual components, and the dependencies between the components have been limited mainly to the effects of the leakage inductance on the various losses. In order to evaluate the best component configuration in the different topologies, an overall loss function with all of the relevant operating parameters and constraints has to be formulated and optimized.

The basic phase-shift full-bridge topology is clearly not the best alternative to low voltage, high current applications because of the high circulating current. The circulating current problem has been addressed in various publications, such as the ones demonstrated in sections 2.3 and 2.4. However, the feasibility of the methods used to reduce the circulating energy should be evaluated under similar operating conditions, as done in this thesis.

Since many of the topologies compared are capable of zero voltage switching, the input voltage and power limits for efficient ZVS utilization should be derived. Operating with a higher primary voltage changes the loss distributions, possibly leading to results quite different from the results obtained with a low voltage.

The transformer optimization requires extensive winding interleaving, which increases the capacitance between the primary and secondary windings. The increased capacitance may become a problem when using the DC-DC converter together with a grid-tie inverter since the amount of injected common-mode current increases. The effects of the transformer interwinding capacitance should be evaluated under conditions with large common-mode voltages present. The increased winding capacitance also increases the required primary current for ZVS (2.2) in the phase-shift topologies, and therefore, the winding interleaving may narrow the ZVS range and degrade efficiency at light loads especially when the input voltage is higher.

The operating conditions where the copper foil winding outperforms the litz wire winding (or a solid conductor winding) should be formulated more exactly as a function of relevant design parameters and constraints.

References

Acharya, K., et al. (2003). System-interaction analyses of solid-oxide fuel cell (SOFC) power-conditioning system. In: *Industry Applications Conference, 2003, 38th IAS Annual Meeting*, 3, pp. 2026-2032.

Balogh, L. (2007). Design and application guide for high speed MOSFET gate drive circuits. Texas Instruments. [Retrieved Dec. 16, 2011], url: http://www.ti.com/lit/ml/slup169/slup169.pdf.

Bartoli, M., Noferi, N., Reatti, A., and Kazimierczuk, M.K. (1996). Modeling Litz-wire winding losses in high-frequency power inductors. In: *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, pp. 1690-1696.

Brown, J.T. (1998). Solid oxide fuel cell technology. *IEEE Transactions on Energy Conversion*, 3.

Chen, J.-F., Chen, R.-Y., and Liang, T.-J. (2008). Study and implementation of a single-stage current-fed boost PFC converter with ZCS for high voltage applications. *IEEE Transactions on Power Electronics*, 23, pp. 379-386.

Chen, W., Lee, C.F., M., J.M., and Sabate, A.J. (1995). A comparative study of a class of full bridge zero-voltage-switched PWM converters. *Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual*, 2, pp. 893-899.

Demin, A. and Panagiotis, T. (2001). Thermodynamic analysis of a hydrogen fed solid oxide fuel cell based on a proton conductor. *International Journal of Hydrogen Energy*, 26, pp. 1103-1108.

Dowell, P.L. (1966). Effects of eddy currents in transformer windings. *Electrical Engineers, Proceedings of the Institution of*, 113, pp. 1387-1394.

Epcos (2006). Ferrites and accessories, SIFERRIT material N87. [Retrieved Feb. 6, 2012], url: http://www.epcos.com/web/generator/Web/Sections/ProductCatalog/Ferrites/Materials/PDF/PDF__N87,property=Data__en.pdf;/PDF_N87.pdf.

Erickson, R.W. and Maksimovic, D. (2001). *Fundamentals of Power Electronics*, 2nd edn. ISBN 978-81-8128-363-4.

Farnell (2012). *Farnell product search*. [Retrieved Jan. 2012, 25], url: http://fi.farnell.com.

Fontell, E., Kivisaari, T., Christiansen, N., and Hansen, J.-B. (2004). Conceptual study of a 250kW planar SOFC system for CHP application. *Journal of Power Sources*, 131, p. 49–56.

Halinen, M., Rautanen, M., Saarinen, J., Pennanen, J., Pohjoranta, A., Kiviaho, J., Pastula, M., Nuttall, B., Rankin, C., and Borglum, B. (2011). Performance of a 10 kW SOFC Demonstration Unit. *ECS Transactions*, 35, pp. 113-120.

Handbook, F.C. (2004). *Fuel Cell Handbook*, 7th edn. U.S. Department of Energy.

Hitchcock, J.L., Walters, M.M., and Wunderlich, A.R. (1992). *Resonant-transition DC-to-DC converter*. Pat. 5132889.

HM Wire International Inc. (2009). *Product catalogs*. [Retrieved Sep. 5, 2012], url: http://www.hmwire.com/products.html.

Hua, G., Lee, F.C., and Jovanovic, M.M. (1993). An improved full-bridge zero-voltage-switched PWM converter using a saturable inductor. *IEEE Transactions on Power Electronics*, 8, pp. 530-534.

Huayang, Z. and Kee, J.R. (2006). Thermodynamics of SOFC efficiency and fuel utilization as functions of fuel mixtures and operating conditions. *Journal of Power Sources*, 161, p. 957–964.

Hyungoon, K., Changwoo, Y., and Sewan, C. (2010). An improved current-fed ZVS isolated boost converter for fuel cell applications. *IEEE Transactions on Power Electronics*, 25(9), pp. 2357-2364.

Kwon, J.-M., Kim, H.-E., Kwon, H.-B., and Nam, H.-K. (2009). High-efficiency fuel cell power conditioning system with input current ripple reduction. *IEEE Transactions on Industrial Electronics*, 56, pp. 826-834.

Lee, W.-J., Kim, C.-E., Moon, G.-W., and Han, S.-K. (2008). A new phase-shifted full-bridge converter with voltage-doubler-type rectifier for high-efficiency PDP sustaining power module. *IEEE Transactions on Industrial Electronics*, 55, pp. 2450-2458.

Lofti, A.W. and Lee, F.C. (1993). A high-frequency model for Litz-wire for switch-mode magnetics. In: *Industry Applications Society Annual Meeting*, 2, pp. 1169-1175.

Magnetics (2011). Magnetics Powder Core Catalog. [Retrieved Aug. 3, 2011], url: http://www.mag-inc.com/File%20Library/Product%20Literature/Powder%20Core%20Literature/MagneticsPowderCoreCatalog2011.pdf.

Mammano, B. (2001). Magnetic amplifier control for simple, low-cost, secondary regulation. Texas Instruments. [Retrieved May 11, 2011], url: http://focus.ti.com/lit/ml/slup129/slup129.pdf.

Mazumder, S.K., et al. (2004). Solid-oxide-fuel-cell performance and durability: resolution of the effects of power-conditioning systems and application loads. *IEEE Transactions on Power Electronics*, 19, pp. 1263-1278.

McLyman, W.T. (2004). *Transformer and inductor design handbook*, 3rd edn.

Metglas (n.d.). Power factor correction inductor design for switched mode power supplies using Metglas Powerlite C-cores. [Retrieved Aug. 25, 2011], url: http://www.metglas.com/downloads/apps/pfc.pdf.

Mohan, N., Robbins, W.P., and Undeland, T.M. (2003). *Power Electronics: Converters, Applications and Design, Media Enhanced Third Edition*, 3rd edn. John Wiley & Sons.

Mohr, M., Franke, W.T., Wittig, B., and Fuchs, F.W. (2010). Converter systems for fuel cells in the medium power range a comparative study. *IEEE Transactions on Industrial Electronics*, 57, pp. 2024-2032.

Mohr, M. and Fuchs, W.-F. (2006). Voltage fed and current fed full bridge converter for the use in three phase grid connected fuel cell systems. In: *Power Electronics and Motion Control Conference, 2006*, 1, pp. 1-7.

Moon, S.-R., Lai, J.-S., Park, S.-Y., and Liu, C. (2006). Impact of SOFC fuel cell source impedance on low frequency AC ripple.

Mweene, L.H., Wright, C.A., and Schlecht, M.F. (1991). A 1 kW 500 kHz front-end converter for a distributed power supply system. *IEEE Transactions on Power Electronics*, 6, pp. 398-407.

Nymand, M. (2010). *High efficiency power converter for low voltage high power applications*. Technical University of Denmark.

Nymand, M. and Andersen, M.A.E. (2008). A new approach to high efficiency in isolated boost converters for high-power low voltage fuel cell applications. *EPE-PEMC*.

Nymand, M. and Andersen, M.A.E. (2009). A new very-high-efficiency R4 converter for high-power fuel cell applications. In: *International Conference on Power Electronics and Drive Systems*, pp. 997-1001. ISBN 978-1-4244-4166-2.

Nymand, M., et al. (2009). Reducing ac-winding losses in high-current high-power inductors. In: *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, pp. 777-781.

Nymand, M., et al. (2009). What is the best converter for low voltage fuel cell applications- a Buck or Boost? In: *IECON '09. 35th Annual Conference of IEEE*, pp. 962-970.

Oates, M.D.C., Crookes, W.R., Pyke, H.S., and Leah, T.R. (2002). Power conditioning for solid oxide fuel cells. *Power Electronics, Machines and Drives*.

Ono, T., Miyachi, I., Suzuki, M., and Higaki, K. (2011). Development of Residential SOFC Cogeneration System. *IOP Conference Series: Materials Science and Engineering*, 18, p. 132007.

Park, E.-S., Choi, S.J., Lee, J.M., and Cho, B.H. (2004). A soft-switching active-clamp scheme for isolated full-bridge boost converter. In: *Applied Power Electronics Conference and Exposition, 2004*, 2, pp. 1067 - 1070 vol.2.

Pradhan, S.K., Mazumder, S.K., Hartvigsen, J., and Hollist, M. (2007). Effects of electrical feedbacks on planar solid oxide fuel cell. *Journal of Fuel Cell Science and Technology*, 4, pp. 154-166.

Pressman, A.I. (1998). *Switching Power Supply Design*, 2nd edn. McGraw-Hill Professional.

Prieto, R., Cobos, A.J., Garcia, O., and Uceda, J. (1997). Interleaving techniques in magnetic components. In: *Applied Power Electronics Conference and Exposition, 1997*, 2, pp. 931-936.

Reatti, A. and Kazimierczuk, M.K. (2002). Comparison of various methods for calculating the ac resistance of inductors. *IEEE Transactions on Magnetics*, 38(3), pp. 1512-1518.

Riipinen, T., et al. (2008). Requirements for power electronics in solid oxide fuel cell system. *EPE 2008, 13th International Conference on Power Electronics and Motion Control*, pp. 1233-1238.

Rylko, M.S., Hayes, J.G., Lyons, B.J., and Egan, M.G. (2011). Revised magnetics performance factors and experimental comparison of high-flux materials for high-current DC–DC inductors. *IEEE Transactions on Power Electronics*, 26(8), pp. 2112-2126.

Råde, L. and Westergren, B. (2001). *Mathematics Handbook for Science and Engineering*, 4th edn. Studentlitteratur, Lund. ISBN 91-44-00839-2.

Sabate, J.A., et al. (1990). Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter. In: *Applied Power Electronics Conference and Exposition, 1990*, pp. 275-284.

Sarén, H. (2005). *Analysis of the voltage source inverter with small dc-link capacitor*. Lappeenranta University of Technology.

Sidwell, R.W. (2005). Large limits of electrical efficiency in hydrocarbon fueled SOFCs. *Journal of Power Sources*, 143, pp. 166-172.

Snelling, E.C. (1988). *Soft ferrites: properties and applications*. Butterworths.

Sullivan, C.R. (1999). Optimal choice for number of strands in a Litz-wire transformer winding. *IEEE Transactions on Power Electronics*, 14(2), pp. 283-291. ISSN 0885-8993.

Walters, K. (n.d.). *Rectifier reverse switching performance*. MicroNote Series 302, Tech. Rep. Microsemi.

Vandelac, J.-P. and Ziogas, P.D. (1988). A novel approach for minimizing high-frequency transformer copper losses. *IEEE Transactions on Power Electronics*, 3, pp. 266-277.

Watson, R. and Lee, F.C. (1998). Analysis, design, and experimental results of a 1-kW ZVS-FB-PWM converter employing magamp secondary-side control. *IEEE Transactions on Industrial Electronics*, 45, pp. 806-814.

Wojda, R.P. and Kazimierczuk, M.K. (2012). Winding resistance of litz wire and multi-strand inductors. *Power Electronics, IET*, 5(2), pp. 257-268.

Väisänen, V., Riipinen, T., Hiltunen, J., and Silventoinen, P. (2011). Design of 10 kW resonant push-pull DC-DC converter for solid oxide fuel cell applications. In: *Proceedings of the 14th European Conference on Power Electronics and Applications (EPE 2011)*.

Väisänen, V., Riipinen, T., and Silventoinen, P. (2010). Effects of switching asymmetry on an isolated full bridge boost converter. *IEEE Transactions on Power Electronics*, 25(8), pp. 2033-2044.

Xiao, Y., Shah, H., Chow, T.P., and Gutmann, R.J. (2004). Analytical modeling and experimental evaluation of interconnect parasitic inductance on MOSFET switching characteristics. In: *Applied Power Electronics Conference and Exposition (APEC)*, 1, pp. 516-521. ISBN 0-7803-8269-2.

Yakushev, V., Meleshin, V., and Fraidlin, S. (1999). Full-bridge isolated current fed converter with active clamp. In: *Applied Power Electronics Conference and Exposition, 1999*, 1, pp. 560-566.

Yang, B. and Zhang, J. (2005). Effect and utilization of common-source inductance in synchronous rectification. In: *Applied Power Electronics Conference and Exposition (APEC)*, 3, pp. 1407-1411. ISBN 0-7803-8975-1.

Zhang, Z., et al. (2008). Optimal design of resonant gate driver for buck converter based on a new analytical loss model. *IEEE Transactions on Power Electronics*, 23(2), pp. 653-666. ISSN 0885-8993.

Zhu, L. (2006). A Novel Soft-Commutating Isolated Boost Full-Bridge ZVS-PWM DC-DC Converter for Bidirectional High Power Applications. *IEEE Transactions on Power Electronics*, 21, pp. 422-429.

Appendix A: Additional tables

Table 1: Transistor peak and RMS currents in the compared topologies for non-clamp transistors. The first of the two RMS equations in the ZVS boost and RPP indicate the situation where the resonance half period $\sqrt{(L_{lk}C_r)}\pi$ is smaller than $(1\text{-}D)T$.

Topology	**Transistor I_{peak}**	**Transistor I_{rms}**
PSFB (Nymand et al., 2009)	$n\left(I_{L_{out}(max)}\right)$	$I_{out} n \sqrt{D_{eff}} \sqrt{1+\frac{1}{3}\left(\frac{n\Delta I_{L_{out}}}{2nI_{out}}\right)^2}$
PSFBVD	$n\frac{\omega_r I_{out} T}{2}$	$\sqrt{\frac{1}{T}\int_0^{\sqrt{L_{lk}C_r}\pi}\left(n\frac{\omega_r I_{out} T}{2}\sin\omega_r t\right)^2 dt}$
FB boost (Nymand et al., 2009)	$I_{L(max)}$	$I_L \frac{\sqrt{3-2D}}{2}\sqrt{1+\frac{1}{3}\left(\frac{\Delta I_L}{2I_L}\right)^2}$
ZVS boost	$n\frac{\omega_r I_{out} T}{2}+I_L$	$\sqrt{\frac{1}{T}\int_0^{\sqrt{L_{lk}C_r}\pi}\left(n\frac{\omega_r I_{out} T}{2}\sin\omega_r t+I_L\right)^2 dt+\frac{1}{T}\int_0^{DT-\sqrt{L_{lk}C_r}\pi}(I_L)^2 dt}$ $\sqrt{\frac{1}{T}\int_0^{DT}\left(n\cdot\frac{\omega_r I_{out} T}{2}\sin\omega_r t+I_L\right)^2 dt}$
RPP	$n\frac{\omega_r I_{out} T}{2}+\frac{I_L}{2}$	$\sqrt{\frac{1}{T}\int_0^{\sqrt{L_{lk}C_r}\pi}\left(n\frac{\omega_r I_{out} T}{2}\sin\omega_r t+\frac{I_L}{2}\right)^2 dt+\frac{1}{T}\int_0^{DT-\sqrt{L_{lk}C_r}\pi}\left(\frac{I_L}{2}\right)^2 dt}$ $\sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(n\cdot\frac{\omega_r I_{out} T}{2}\sin\omega_r t+\frac{I_L}{2}\right)^2 dt+\frac{1}{T}\int_0^{(D-0.5)T}\left(\frac{I_L}{2}\right)^2 dt}$

Table 2: Transistor peak and RMS currents in the compared topologies for clamp transistors. The first of the two RMS equations in the ZVS boost and RPP indicate the situation where the resonance half period $\sqrt{(L_{lk}C_r)}\pi$ is smaller than $(1\text{-}D)T$.

Topology	**Transistor I_{peak}**	**Transistor I_{rms}**
ZVS boost	I_L	$\sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t - I_L\right)^2 dt + \frac{1}{T}\int_0^{(1-D)T-\sqrt{L_{lk}C_r}\pi}(I_L)^2 dt}$ $\sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t - I_L\right)^2 dt}$
RPP	$\frac{I_L}{2}$	$\sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t - \frac{I_L}{2}\right)^2 dt + \frac{1}{T}\int_0^{(1-D)T-\sqrt{L_{lk}C_r}\pi}\left(\frac{I_L}{2}\right)^2 dt}$ $\sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t - \frac{I_L}{2}\right)^2 dt}$

Table 3: Transistor datasheet parameters used in this thesis.

Transistor	**$V_{BR(DSS)}$ [V]**	**$R_{DS(on)}$ [mΩ]**	**$C_{rss,\,avg}$ [pF]**	**C_{oss} [pF]**	**V_D [V]**	**R_D [mΩ]**
IRFP4368PBF	75	1.46	1442	1700	0.5	2.25
IRFP4568PBF	150	4.8	267	900	0.52	2.15

Table 4: Diode average and RMS currents in the compared topologies. Time instants t_1 and t_4 refer to Figure 2.6. The first of the two RMS equations in the ZVS boost and RPP indicate the situation where the resonance half period $\sqrt{(L_{lk}C_r)}\pi$ is smaller than $(1\text{-}D)T$.

Topology	Diode I_{avg}	Diode I_{rms}
PSFB, partial ZVS	$\frac{I_{out}}{2}$	See section 4.3
PSFB, full ZVS		$I_{out}\sqrt{\frac{t_4-t_1}{T}}\sqrt{1+\frac{1}{3}\left(\frac{\Delta I_{L_{out}}}{2I_{out}}\right)^2}$
PSFBVD	I_{out}	$\sqrt{\frac{1}{T}\int_0^{\sqrt{L_{lk}C_r}\pi}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t\right)^2 dt}$ $\sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t\right)^2 dt}$
FB boost (Nymand et al., 2009)	$\frac{I_{out}}{2}$	$\frac{I_L}{n}\sqrt{1-D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta I_L}{2I_L}\right)^2}$
ZVS boost, D_1 & D_3	I_{out}	$\sqrt{\frac{1}{T}\int_0^{\sqrt{L_{lk}C_r}\pi}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t\right)^2 dt}$ $\sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t\right)^2 dt}$
ZVS boost, D_2 & D_4		$\sqrt{\frac{1}{T}\int_0^{\sqrt{L_{lk}C_r}\pi}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t\right)^2 dt}$ $\sqrt{\frac{1}{T}\int_0^{DT}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t\right)^2 dt}$
RPP	I_{out}	$\sqrt{\frac{1}{T}\int_0^{\sqrt{L_{lk}C_r}\pi}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t\right)^2 dt}$ $\sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t\right)^2 dt}$

Table 5: Si-diode datasheet parameters used in this thesis. It is assumed that the diode voltage overshoot in the PSFB topology is limited to twice the output voltage without a snubber circuit. The maximum diode voltage in the other topologies is assumed to be clamped to the output voltage.

Topology	**Max diode voltage**	**Si diode**	V_D	R_D	I_{rm}	t_{rr}
PSFB, partial ZVS	1320 V	2 x DSEI30-10A	1.5V	12.5 mΩ	32 A	35 ns
PSFB, full ZVS	1320 V	2 x DSEI30-10A	1.5 V	12.5 mΩ	32 A	35 ns
PSFBVD	660 V	DSEI30-10A	1.5 V	12.5 mΩ	32 A	35 ns
FB boost	660 V	DSEI30-10A	1.5 V	12.5 mΩ	32 A	35 ns
ZVS boost	330 V	DSEI30-06A	1.01 V	7.1 mΩ	19 A	35 ns
RPP	660 V	DSEI30-10A	1.43 V	12.5 mΩ	32 A	35 ns

Table 6: SiC-diode datasheet parameters used in this thesis. It is assumed that the diode voltage overshoot in the PSFB topology is limited to twice the output voltage without a snubber circuit. The maximum diode voltage in the other topologies is assumed to be clamped to the output voltage.

Topology	Max. diode voltage	SiC diode	V_D	R_D	C_j @ Max V
PSFB, partial ZVS	1320 V	2 x IDH15S120	0.9 V	90 mΩ	50 pF
PSFB, full ZVS	1320 V	2 x IDH15S120	0.9 V	90 mΩ	50 pF
PSFBVD	660 V	IDH15S120	1.43 V	90 mΩ	50 pF
FB boost	660 V	IDH15S120	1.43 V	90 mΩ	50 pF
ZVS boost	330 V	IDH16S60C	0.8 V	53 mΩ	100 pF
RPP	660 V	IDH15S120	1.43 V	90 mΩ	50 pF

Table 7: Costs per single MOSFET (Farnell, 2012).

Device	Cost per single device	Cost per 250+ devices
IRFP4368PBF	€ 12.60	€ 4.50
IRFP4568PBF	€ 8.55	€ 4.75

Table 8: Costs per single diode (Farnell, 2012).

Device	Cost per device	Cost per 250+ devices
DSEI30-06A	€ 6.58	€ 1.77
DSEI30-10A	€ 8.26	€ 2.23
IDH16S60C	€ 20.83	€ 13.27
IDH15S120	€ 49.07	€ 31.26

Table 9: Required transformer turn ratios for a given V_{out}/V_{in}.

Topology	**Turns ratio N_{sec}/N_{pri}**
PSFB	$\frac{V_{out} + \frac{2V_{out}(t_2 - t_0)}{T - 2(t_2 - t_0)}}{V_{DC}}$
PSFBVD	$\frac{0.5V_{out}}{V_{DC}}$
FB boost	$\frac{2(1-D)V_{out}}{V_{DC}}$
ZVS boost	$\frac{V_{out} - DV_{out}}{2V_{DC}}$
RPP	$\frac{V_{out} - DV_{out}}{2V_{DC}}$

Table 10: Transformer RMS currents in the compared topologies. The first of the two RMS equations in the ZVS boost and RPP indicate the situation where the resonance half period $\sqrt{(L_{lk}C_r)}\pi$ is smaller than $(1-D)T$.

Topology	Transformer I_{rms}
PSFB	$\sqrt{2D_{eff}RMS(1)+2(t_1-t_0)RMS(2)+2(t_2-t_1)RMS(3)}$ $RMS(1)=\frac{1}{3}\sqrt{(nI_{L_{out}(max)})^2+nI_{L_{out}(max)}nI_{L_{out}(min)}+(nI_{L_{out}(min)})^2}$ $RMS(2)=\frac{1}{3}\sqrt{(nI_{L_{out}(max)})^2+nI_{L_{out}(max)}nI_{t1}+(nI_{t1})^2}$ $RMS(3)=\frac{1}{3}(nI_{t1})^2$
PSFBVD	$\sqrt{\frac{2}{T}\int_0^{\sqrt{L_{lk}C_r}\pi}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t\right)^2 dt}$
FB boost	$I_L\sqrt{\frac{(1-D)T}{0.5T}}\sqrt{1+\frac{1}{3}\left(\frac{\Delta I_L}{I_L}\right)^2}$
ZVS boost	$\sqrt{\frac{2}{T}\int_0^{\sqrt{L_{lk}C_r}\pi}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t\right)^2 dt}$ $\sqrt{\frac{1}{T}\int_0^{DT}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t\right)^2 dt+\frac{1}{T}\int_0^{(1-D)T}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t\right)^2 dt}$
RPP	$\sqrt{\frac{1}{T}\int_0^{\sqrt{L_{lk}C_r}\pi}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t+\frac{I_L}{2}\right)^2 dt+\frac{1}{T}\int_0^{\sqrt{L_{lk}C_r}\pi}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t-\frac{I_L}{2}\right)^2 dt+\frac{1}{T}\int_0^{DT-\sqrt{L_{lk}C_r}\pi}\left(\frac{I_L}{2}\right)^2 dt}$ $\sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t+\frac{I_L}{2}\right)^2 dt+\frac{1}{T}\int_0^{(1-D)T}\left(n\frac{\omega_r I_{out}T}{2}\sin\omega_r t-\frac{I_L}{2}\right)^2 dt+\frac{1}{T}\int_0^{(D-0.5)T}\left(\frac{I_L}{2}\right)^2 dt}$

Table 11: Maximum allowable power losses for various cores with parameters $E = 0.9$, $T_{max} = 100°C$, $T_{amb} = 30°C$. The winding window is assumed 90% full including insulators.

Core	Maximum allowable power loss [W]
ETD29	5
ETD34	6
ETD39	8
ETD44	10
ETD49	12
ETD54	15
ETD59	18
PM50	13
PM62	20
PM74	29
PM87	39
PM114	66

Appendix B: Measurement equipment

The following measurement devices were used in the measurements of this thesis:

- Oscilloscopes: LeCroy LC574A, Tektronix TDS3052.
- Current probes: Fluke 80i-110s, LeCroy AP015
- Multimeters: Fluke True RMS 187, Fluke 8840A
- LCR meter: HP 4284A

Figure 1 presents the low power prototypes used for the topology evaluation.

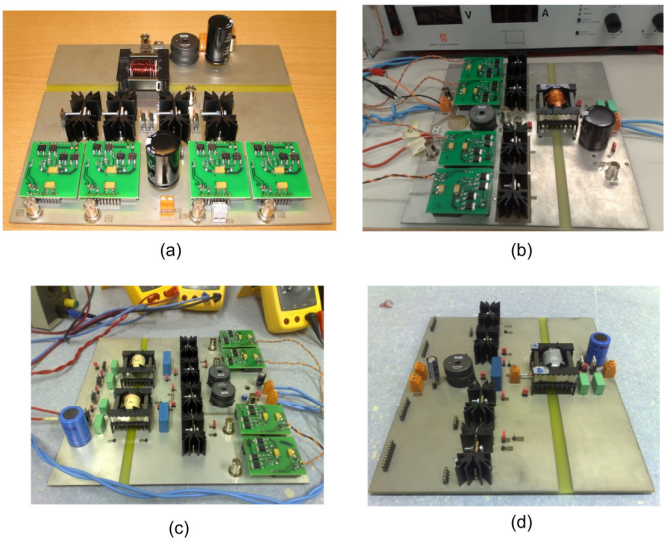


Figure 1: Pictures of the low power prototypes used in the evaluations. The topologies are phase-shifted full-bridge (a), full-bridge boost (b), ZVS boost (c) and resonant push-pull (d).

Table 1. General specifications for the low power prototypes.

Nominal input voltage	35 V
Nominal input current	4.3 A
Nominal output voltage	150 V (100 V for the PSFB)
Switching frequency	50 kHz (20 kHz for the PSFB)

The components used in the low power prototypes were the following:

Inductor: Murata 1447440C, 470 µH (all topologies)

Transistor: IRFB4310Z (all topologies)

Transformer:

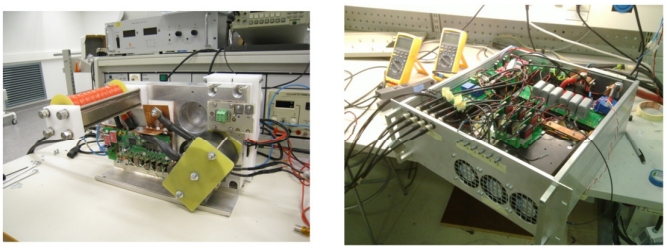
- **PSFB**: ETD39, 3C90. Primary 13 turns of 0.94 mm^2 litz, secondary 38 turns of 0.74 mm^2 litz.
- **FB boost with diode bridge**: ETD39, 3C90. Primary 15 turns of 0.94 mm^2 litz, secondary 35 turns of 0.74 mm^2 litz.
- **FB boost with voltage doubler**: ETD39, 3C90. Primary 15 turns of 0.94 mm^2 litz, secondary 18 turns of 0.94 mm^2 litz.
- **ZVS boost**: ETD39, 3C90. Primary 14 turns of 0.94 mm^2 litz, secondary 19 turns of 0.94 mm^2 litz.
- **RPP**: ETD39, 3C90. Primary (7+7) turns of 0.94 mm^2 litz, secondary 19 turns of 0.94 mm^2 litz.

Rectifier: Cree C2D02060, 600 V (all topologies)

Input/output capacitor: Panasonic 1000 µF, 250 V (all topologies)

Voltage doubler capacitor: Vishay MKT, 1 µF

Figure 2 illustrates the medium and high power prototypes.



(a) (b)

Figure 2: Pictures of the medium- and high-power prototypes used in the evaluations. The topologies are full-bridge boost (a) and resonant push-pull (b).

Table 2. General specifications for the medium- and high power prototypes.

Nominal input voltage	50 V
Nominal input current	200 A
Nominal output voltage	700 V (grid tie inverter DC link voltage set at 660 V)
Switching frequency	50 kHz

The components used in the medium- and high power prototypes were the following:

Inductor: AMCC168s, 11 turns of 35 mm2 stranded wire in one layer, air gap 2.8 mm, nominal inductance 25 µH. (all topologies)

Transistor:

- **FB boost**: 8 x IRFP4568PBF
- **RPP**: 6 x IXFN180N20

Transformer:

- **FB boost with diode bridge**: PM114/93, N87. Primary 3 turns of 12 x 0.1 x 50 mm copper foil with 0.05 mm Nomex 410 insulators, secondary 30 turns of 0.1 x 50 mm copper foil with 0.05 mm Nomex 410. Two primary-secondary intersections with 5 x 0.05 mm Nomex 410.
- **RPP**: 2 parallel PM114/93, N87 cores. Primary 2 + 2 turns of 48 mm^2 litz, secondary 12 turns of 6.3 mm^2 litz. One primary-secondary intersection.

Rectifier:

- **FB boost**: DSI45-12A, 1200 V
- **RPP**: DSEI2x101-12A, 1200 V

Output capacitor:

- **FB boost**: 2 x Evox Rifa 4700 µF, 450 V in series
- **RPP**: Cornell Dubilier, 230 µF

Voltage doubler capacitors: 2 x 2 x 680 nF polypropylene, 27.5 mm (RPP)

Clamp capacitors: 2 x 3 x 20 uF polypropylene, 37.5 mm (RPP)

Appendix C: PSpice simulation modelling

Figure 1 illustrates the PSpice simulation model used to simulate the waveforms in Figure 2.4.

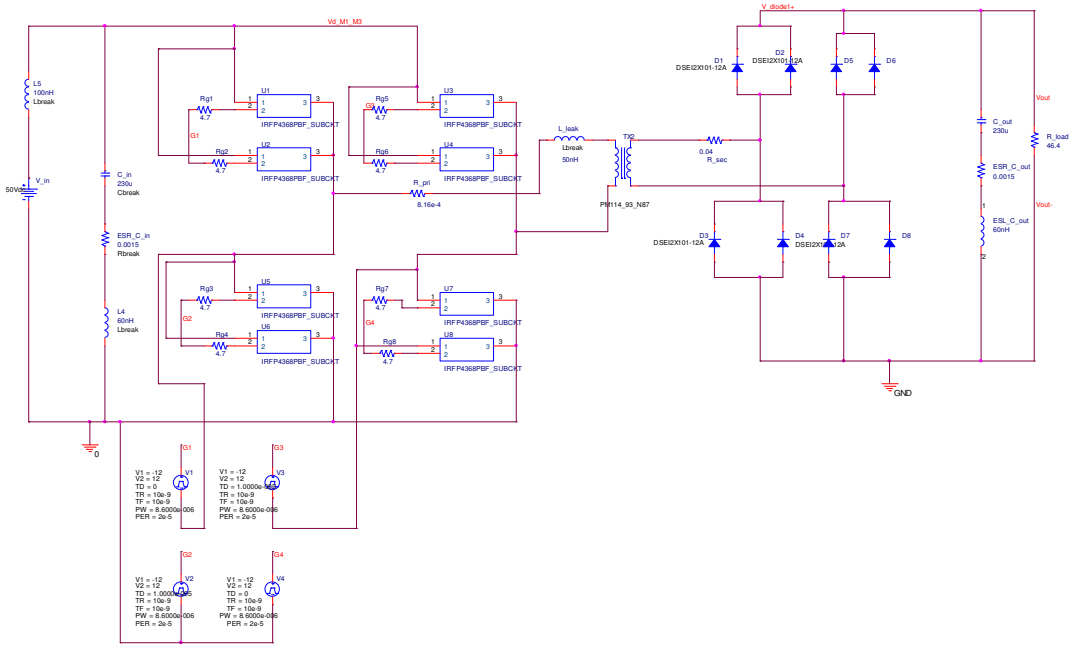


Figure 1: PSpice simulation model for the basic voltage-fed converter (Figure 2.1).

All simulation models in this thesis and in Väisänen et al. (2010) are designed using the following principles:

- Capacitors are modeled to include series resistors and series inductors.
- MOSFETs are modeled using manufacturer subcircuits (if available) or by using a custom subcircuit including the parasitic components illustrated in Figure 2.

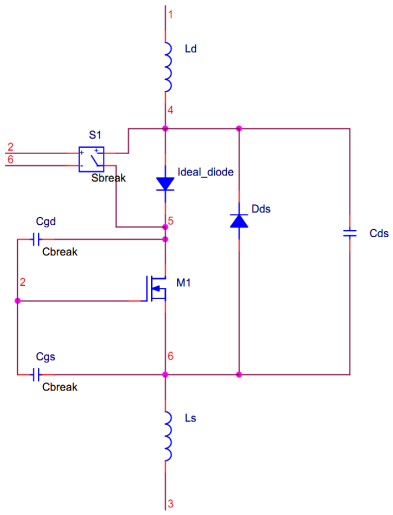


Figure 2: MOSFET subcircuit model used when manufacturer subcircuits did not exist. The MOSFET model includes voltage-current characteristics and the channel resistance. The body diode is modeled separately according to the nominal datasheet values. The ideal switch on the drain allows bidirectional power flow through the transistor channel if a large enough positive gate voltage is applied.

- Diodes are manufacturer models (if available) or custom models modeled with the PSpice model editor. The models include voltage-current characteristics, simplified reverse recovery characteristics (no soft recovery) and the junction capacitance characteristics.
- The transformers are modeled to include the leakage inductance, winding resistances and a non-linear core model based on the material B-H curves and the actual core dimensions.

Figure 3 illustrates the effect of diode reverse recovery during time instants t_1-t_2 in Figure 2.4

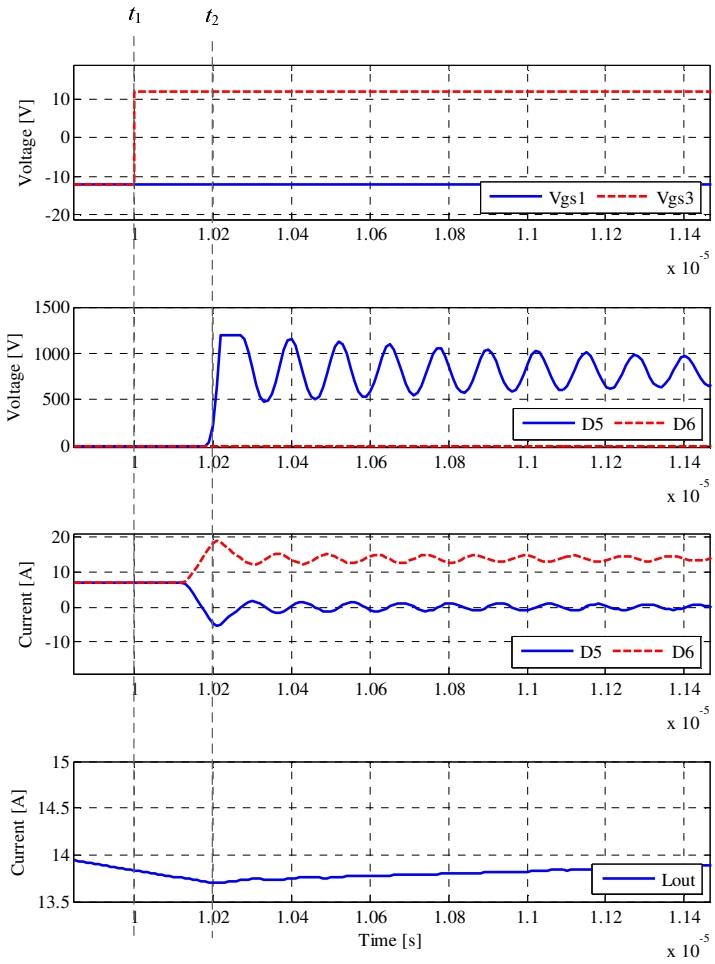


Figure 3: The diode reverse recovery phenomena and the diode voltage oscillation in the hard switched voltage-fed full-bridge converter. The inherent PSpice diode model supports only abrupt recovery, which is seen as prolonged oscillation in the diode voltage and current.

Appendix D: MATLAB functions for calculating the litz resistances

```
  function value = ber(n,x)
value=real(besselj(n,x*exp((3*1i*pi/4))));


  function value = bei(n,x)
value=imag(besselj(n,x*exp((3*1i*pi/4))));


  function value = Dber(n,x) % Calculate ber'(γ) with order of n
syms z;
syms nu;
eq=diff(besselj(nu,z*exp(3*1i*pi/4)),z);
value=real(subs(eq,{nu,z},{n,x}));


  function value = Dbei(n,x) % Calculate bei'(γ) with order of n
syms z;
syms nu;
eq=diff(besselj(nu,z*exp(3*1i*pi/4)),z);
value=imag(subs(eq,{nu,z},{n,x}));


  gamma=d/(skin_depth*sqrt(2));
  A=(ber(0,gamma)*Dbei(0,gamma)-
bei(0,gamma)*Dber(0,gamma))/(Dber(0,gamma)^2+Dbei(0,gamma)^2);


  C=(ber(2,gamma)*Dber(0,gamma)+bei(2,gamma)*Dbei(0,gamma))/(ber(0,gamm
a)^2+bei(0,gamma)^2);
```

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