Lappeenranta
University of Technology

Juho Tyster

POWER SEMICONDUCTOR NONLINEARITIES IN ACTIVE DU/DT OUTPUT FILTERING

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Abstract

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This doctoral thesis introduces an improved control principle for active du/dt output filtering in variable-speed AC drives, together with performance comparisons with previous filtering methods. The effects of power semiconductor nonlinearities on the output filtering performance are investigated. The nonlinearities include the timing deviation and the voltage pulse waveform distortion in the variable-speed AC drive output bridge. Active du/dt output filtering (ADUDT) is a method to mitigate motor overvoltages in variable-speed AC drives with long motor cables. It is a quite recent addition to the du/dt reduction methods available. This thesis improves on the existing control method for the filter, and concentrates on the low-voltage (below 1 kV AC) two-level voltage-source inverter implementation of the method. The ADUDT uses narrow voltage pulses having a duration in the order of a microsecond from an IGBT (insulated gate bipolar transistor) inverter to control the output voltage of a tuned LC filter circuit. The filter output voltage has thus increased slope transition times at the rising and falling edges, with an opportunity of no overshoot. The effect of the longer slope transition times is a reduction in the du/dt of the voltage fed to the motor cable. Lower du/dt values result in a reduction in the overvoltage effects on the motor terminals. Compared with traditional output filtering methods to accomplish this task, the active du/dt filtering provides lower inductance values and a smaller physical size of the filter itself. The filter circuit weight can also be reduced. However, the power semiconductor nonlinearities skew the filter

control pulse pattern, resulting in control deviation. This deviation introduces unwanted overshoot and resonance in the filter. The control method proposed in this thesis is able to directly compensate for the dead time-induced zero-current clamping (ZCC) effect in the pulse pattern. It gives more flexibility to the pattern structure, which could help in the timing deviation compensation design.

Previous studies have shown that when a motor load current flows in the filter circuit and the inverter, the phase leg blanking times distort the voltage pulse sequence fed to the filter input. These blanking times are caused by excessively large dead time values between the IGBT control pulses. Moreover, the various switching timing distortions, present in real-world electronics when operating with a microsecond timescale, bring additional skew to the control. Left uncompensated, this results in distortion of the filter input voltage and a filter self-induced overvoltage in the form of an overshoot. This overshoot adds to the voltage appearing at the motor terminals, thus increasing the transient voltage amplitude at the motor. This doctoral thesis investigates the magnitude of such timing deviation effects. If the motor load current is left uncompensated in the control, the filter output voltage can overshoot up to double the input voltage amplitude. IGBT nonlinearities were observed to cause a smaller overshoot, in the order of 30%. This thesis introduces an improved ADUDT control method that is able to compensate for phase leg blanking times, giving flexibility to the pulse pattern structure and dead times. The control method is still sensitive to timing deviations, and their effect is investigated. A simple approach of using a fixed delay compensation value was tried in the test setup measurements. The ADUDT method with the new control algorithm was found to work in an actual motor drive application. Judging by the simulation results, with the delay compensation, the method should ultimately enable an output voltage performance and a du/dt reduction that are free from residual overshoot effects.

The proposed control algorithm is not strictly required for successful ADUDT operation: It is possible to precalculate the pulse patterns by iteration and then for instance store them into a look-up table inside the control electronics. Rather, the newly developed control method is a mathematical tool for solving the ADUDT control pulses. It does not contain the timing deviation compensation (from the logic-level command to the phase leg output voltage), and as such is not able to remove the timing deviation effects that cause error and overshoot in the filter. When the timing deviation compensation has to be tuned-in in the control pattern, the precalculated iteration method could prove simpler and equally good (or even better) compared with the mathematical solution with a separate timing compensation module. One of the key findings in this thesis is the conclusion that the correctness of the pulse pattern structure, in the sense of ZCC and predicted pulse timings, cannot be separated from the timing deviations. The usefulness of the correctly calculated pattern is reduced by the voltage edge timing errors.

The doctoral thesis provides an introductory background chapter on variable-speed AC drives and the problem of motor overvoltages and takes a look at traditional solutions for overvoltage mitigation. Previous results related to the active du/dt filtering are discussed. The basic operation principle and design of the filter have been studied previously. The effect of load current in the filter and the basic idea of compensation have been presented in the past. However, there was no direct way of including the dead time in the control (except for solving

the pulse pattern manually by iteration), and the magnitude of nonlinearity effects had not been investigated. The enhanced control principle with the dead time handling capability and a case study of the test setup timing deviations are the main contributions of this doctoral thesis. The simulation and experimental setup results show that the proposed control method can be used in an actual drive. Loss measurements and a comparison of active d*u*/d*t* output filtering with traditional output filtering methods are also presented in the work. Two different ADUDT filter designs are included, with ferrite core and air core inductors. Other filters included in the tests were a passive d*u*/d*t*filter and a passive sine filter. The loss measurements incorporated a silicon carbide diode-equipped IGBT module, and the results show lower losses with these new device technologies.

The new control principle was measured in a 43 A load current motor drive system and was able to bring the filter output peak voltage from 980 V (the previous control principle) down to 680 V in a 540 V average DC link voltage variable-speed drive. A 200 m motor cable was used, and the filter losses for the active d*u*/d*t* methods were 111 W–126 W versus 184 W for the passive d*u*/d*t*. In terms of inverter and filter losses, the active d*u*/d*t* filtering method had a 1.82-fold increase in losses compared with an all-passive traditional d*u*/d*t* output filter. The filter mass with the active d*u*/d*t* method was 17% (2.4 kg, air-core inductors) compared with 14 kg of the passive d*u*/d*t* method filter. Silicon carbide freewheeling diodes were found to reduce the inverter losses in the active d*u*/d*t* filtering by 18% compared with the same IGBT module with silicon diodes. For a 200 m cable length, the average peak voltage at the motor terminals was 1050 V with no filter, 960 V for the all-passive d*u*/d*t* filter, and 700 V for the active d*u*/d*t* filtering applying the new control principle.

Keywords: Variable-speed AC drives, output filtering, dead time compensation, IGBT loss measurements
UDC 621.314.5:681.527.7:681.532.5:621.382.33

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Lappeenranta, May 18th, 2014

Juho Tyster

Contents

List of Symbols and Abbreviations

Roman letters

C	Capacitance
C_{f}	Filter capacitance
f_{sw}	PWM switching frequency
g_{fs}	Transistor forward transconductance
I	Steady-state current
i	Transient current
i_{C}	Collector current
i_{c}	Collector current at switching transient
$i_{\mathrm{c(off)}}$	Collector current at turn-off
$i_{\mathrm{c(on)}}$	Collector current at turn-on
I_{f}	Filter resonant current
I_{f3}	Filter characteristic peak current
$\hat{I}_{\mathrm{f}}$	Filter peak current
i_{L}	Filter inductor current
i_{L0}	Initial inductor current
I_{out}	Load circuit current
I_{RR}	Diode reverse-recovery peak current
I_{SR}	Phase leg shoot-through current
K	Empirical du/dt coefficient for ADUDT
ℓ_{max}	Maximum cable length

L	Inductance
L_{f}	Filter inductance
L_{s}	Parasitic inductance
Q_{H}	High-side logic-level gate command before gate driver
Q_{h}	High-side logic-level gate command from PWM controller
Q_{L}	Low-side logic-level gate command before gate driver
Q_{l}	Low-side logic-level gate command from PWM controller
R	Electric resistance
R_{th}	Thermal resistance
S_{OE}	Overshoot envelope area
t_{a}	A-pulse duration
$t_{\mathrm{a,min}}$	Minimum A-pulse width
t_{b}	B-pulse duration
t_{blank}	Blanking time appearing in phase leg
$t_{\mathrm{b,min}}$	Minimum B-pulse width
t_{ch}	Gate charge time
$t_{\mathrm{d,off}}$	Turn-off delay
$t_{\mathrm{d,on}}$	Turn-on delay
t_{d1}	First dead time
$t_{\mathrm{driver(off)}}$	Gate driver delay at turn-off
$t_{\mathrm{driver(on)}}$	Gate driver delay at turn-on
t_{d3}	Third dead time
t_{d2}	Second dead time
t_{f}	Current fall time
t_{fw}	Free-wheeling period duration
t_{M}	Miller plateau time
$t_{\mathrm{M(off)}}$	Turn-off Miller plateau duration
$t_{\mathrm{M(on)}}$	Turn-on Miller plateau duration
t_{r}	Current rise time

t_{res}	Inductor current reset-to-zero time
t_{rr}	Diode reverse-recovery time
t_{s}	Gate storage time
t_{V}	Virtual edge delay
$t_{\mathrm{V(off)}}$	Virtual edge delay at turn-off
$t_{\mathrm{V(on)}}$	Virtual edge delay at turn-on
t_{ZCC}	Zero-current clamping (ZCC) period
t_{ZCC1}	First ZCC period
t_{ZCC2}	Second ZCC period
U	Steady-state voltage
u	Transient voltage
u_{U}	Inverter output phase U voltage
u_{V}	Inverter output phase V voltage
u_{W}	Inverter output phase W voltage
u_{C}	Filter capacitor voltage
$U_{\mathrm{CE(on)}}$	Collector-emitter saturation voltage
u_{CE}	Collector-emitter voltage
U_{DC}	DC link average voltage
U_{dc}	DC link transient voltage
u_{dc}	DC link transient voltage
U_{FR}	IGBT forward-recovery voltage
u_{G}	Gate-emitter voltage
$U_{\mathrm{G-}}$	Negative (turn-off) gate driver voltage
$U_{\mathrm{G+}}$	Positive (turn-on) gate driver voltage
U_{M}	Miller plateau voltage
U_{M1}	Turn-on Miller plateau voltage
U_{M2}	Turn-off Miller plateau voltage
u_{out}	Phase leg output voltage
$\hat{u}_{\mathrm{F}}$	Peak negative value of overshoot envelope

$\hat{u}_\mathrm{R}$	Peak positive value of overshoot envelope
U_T	Gate threshold voltage
v_p	Propagation velocity
Y	Admittance
Y_f	Filter admittance
Z	Impedance
Z_0	Transmission line characteristic impedance
Z_f	Filter impedance
Z_L	Load impedance
Z_S	Source impedance
Z_σ	Parasitic impedance component

Greek letters

α	Attenuation factor
β	Wave number
Δ	Change, differential
Δz	Length, differential
ε	Dielectric coefficient
η	Efficiency
ϕ	Phase shift angle
Γ	Reflection coefficient
γ	Propagation factor
Γ_L	Load reflection coefficient
Γ_S	Source reflection coefficient
λ	Wave length
ω	Angular frequency
τ	Angular period
τ_f	Filter period, filter time constant
τ_gate	Gate time constant
ω_f	Filter angular frequency

Acronyms

AC	Alternating current
ADUDT	Active du/d$t$output filtering
PDUDT	Passive du/d$t$output filtering
BJT	Bipolar junction transistor
D_1	High-side ideal diode
D_2	Low-side ideal diode
du/dt	Voltage rate of change i.e. time derivative
DC	Direct current
EMI	Electromagnetic interference
FPGA	Field-programmable gate array
GTO	Gate turn-off thyristor
di/dt	Current rate of change i.e. time derivative
$IGBT_H$	High-side IGBT
$IGBT_L$	Low-side IGBT
IGBT	Insulated gate bipolar transistor
MCU	Microcontroller
MOSFET	Metal-oxide-semiconductor field-effect transistor
PWM	Pulse width modulation
RR	Reverse-recovery
RTD	Resistance temperature detector
S_1	High-side ideal switch
S_2	Low-side ideal switch
SiC	Silicon carbide
SOA	Safe operating area
VFD	Variable-frequency drive
VSI	Voltage source inverter
ZCC	Zero-current clamping

Chapter 1

Introduction

Electric motors drive the industry. Pulp and paper mills, steel mills, oil refineries, and chemical plants are but a few examples of targets where electric motors are used in various duties. Individual motor power can be expected to span from hundreds of watts to a megawatt range. At the same time, the industry consumes the majority of all the electric energy produced in the world. The economic and industrial strength in countries such as China and India is growing. It is reasonable to expect that the number of installed electric motors will be high and increase further in the future.

Energy efficiency is a central topic in discussions on more environment-friendly ways of energy production and consumption (Bertoldi and Atanasiu, 2007). By energy efficiency we mean the use of electric energy to do work wasting as little energy as possible. The extra waste of energy in an industrial setting, in a process where electric motors are used, is typically in the form of waste heat, noise, and other forms of emissions. These do not contribute to the actual useful work. A typical example is a pump or a fan that is running at full speed according to the nominal value of the motor, with the fluid flow then controlled and limited by a valve. The useful work here is the fluid flowing through the valve into the process. If the speed of the pump is constant, all the extra effort is wasted in the pump as heat. As the full speed in the pump is not needed by the process, the energy could be saved by controlling the speed of the pump instead of throttling the flow with a valve. Similar examples can also be found in other electric motor applications. A very large proportion of the electric energy used in motors is consumed by pump, fan, or compressor drives (Popovic-Gerber et al., 2012). Thus, it is logical to assume that industry is using speed-controlled motor drives, and will implement them in ever-increasing numbers in the near future. The ability to control the speed and torque of a motor drive is a key solution towards more energy-efficient applications.

A three-phase asynchronous low-voltage motor with a squirrel-cage rotor winding is a widely used motor type in the industry (Krause et al., 2002). This is also called a squirrel-cage induction motor. ‘Low voltage’ means that the rated voltage of the motor is under 1 kV AC. It

is due to the mechanically rugged construction and a relatively low unit cost that this motor type is so widely used. Compared with direct current motors and other motor types with rotating electric contacts (slip rings and commutators), the induction motor has no maintenance-requiring parts apart from bearings. However, the speed and torque control of this induction motor requires alterations to the input voltage and frequency. With the advent of power electronic converters suitable for the three-phase AC motor use, implementing a variable-speed AC drive with an induction motor is reasonably economical and straightforward. The speed and torque control of this motor type using an electronic converter dates back to the 1970s (Rodriguez et al., 2012). With converters available from many vendors in all required power ratings, these variable-speed drives are not necessarily limited to low-voltage induction motors. Higher voltages are commonly used when the drive power extends to the megawatt range. The electric motor can also be of different types. Synchronous motors are also used, with a wound rotor or permanent magnet construction. The electronic converter used in any of these variable-speed motor applications is typically called a frequency converter or a variable frequency drive (VFD).

Frequency converters are used in great numbers where the induction motor speed and torque must be controlled (Rodriguez et al., 2012). This is to achieve energy savings and to increase the process efficiency. However, ever since the use of these converters has been established, a certain adverse effect has been reported and widely studied. It is known as the motor cable reflection, causing transient overvoltages at the motor terminals. This problem is related to the way the converter works and to the electromagnetic wave propagation through a transmission line (Saunders et al., 1996). Specifically, it is because the power electronic converter uses switching devices to shape the voltage and current. In order for the converter to work, it must use electronic switching devices (transistors) to shape the voltage with a variable amplitude and frequency. Most often in an industrial low-voltage frequency converter, these transistors are arranged to a circuit called a three-phase voltage-source inverter (Mohan et al., 2003), (Krause et al., 2002). With the electric energy coming from the grid that feeds the converter, the inverter with transistors produces a series of voltage pulses to its output. The electric motor is connected to the frequency converter output. Varying the width of the pulses with respect to time, a three-phase current that has the required form to produce the correct speed and torque is generated in the motor. This basic operating principle is shown in Figure 1.1.

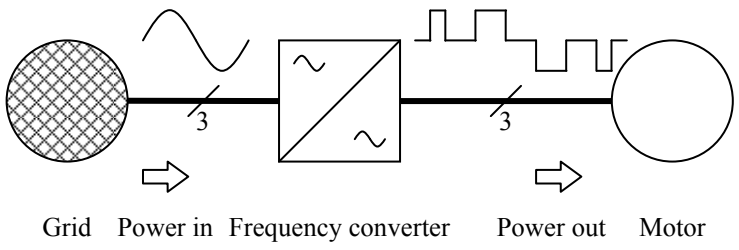


Figure 1.1. Operating principle of a variable-speed AC motor drive.

The problem with the voltage pulses is their rapid voltage rise time. The insulated gate bipolar transistors (IGBT), which are employed in the converters today, produce pulse edge transition times in the order of 100 ns (Finlayson, 1998). Fast action of the transistors is desirable in

terms of losses when the transistors are switched on and off. A simplified principle is that when the transistor spends as little time as possible on the edge of individual pulses (forming a certain slope at the edge), the wasted energy caused by pulse production is minimized (Mohan et al., 2003). This is in agreement with the objective to cut down the energy wasted in the converter itself. Nevertheless, the fast voltage transients present at the inverter output, when combined with a motor cable physically long enough, will result in an overvoltage in the motor. This overvoltage can be detrimental to the motor insulations and cause damage to the motor bearings (Busse et al., 1997a), (Melfi et al., 1998). The overvoltage phenomenon itself is based on the basic transmission line theory and has been widely studied (Persson, 1992). A typical example of voltage reflection causing overvoltage at the motor terminals is shown in Figure 1.2.

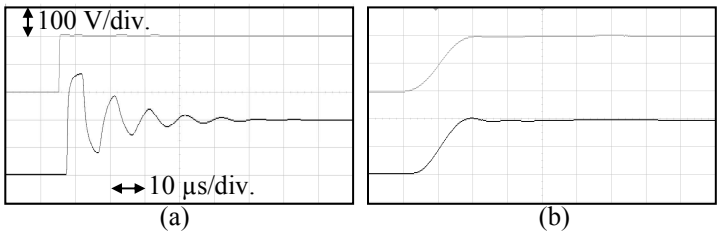


Figure 1.2. In (a), a steep voltage edge (upper waveform) causes overvoltages at the motor terminals (lower waveform). When the voltage rate of change is reduced in (b), the effect of reflection is lowered. Overvoltage can be completely removed, as in this example. The motor cable length here is 300 m. A measured example from the experimental setup of the thesis work, with active du/dt output filtering in (b).

The amplitude and rate of change of the voltage can have a detrimental effect on the lifetime of the motor (Melfi et al., 1998). Thus, there is a need to reduce the reflection-related effects.

Inhibiting the overvoltage effect requires either a shorter motor cable, slower voltage edge transition times in the inverter output, or filtering of the voltage before the motor cable, as reported in (Saunders et al., 1996), (Kerkman et al., 1997), and (Finlayson, 1998). The motor insulations can also be designed to withstand the overvoltage, and moreover, using insulated bearings can extend the motor lifetime under harmful voltage conditions (Melfi et al., 1998). This thesis concentrates on a specific solution that aims to reduce the voltage transition du/dt experienced by the motor cable on the VFD side. It is called the active du/dt output filtering (ADUDT), previously studied for instance in (Ström et al., 2011). The term 'active' refers to using the active control participation of the variable-frequency drive unit (including the power electronic switching devices) in the operation. This method has a potential for making the output filter lighter and smaller in size, simultaneously achieving superior reduction in the voltage edge rise and fall rates when compared with traditional du/dt filtering methods. The concept of active du/dt output filtering is shown in Figure 1.3. The basic operation principle and filter topology has been published in (Ström, 2009). Although this thesis limits the study to three-phase systems, the ADUDT principle itself can work with any number of phases, starting from a half-bridge inverter.

This work describes an improved control method and an analysis of the dead time and non-

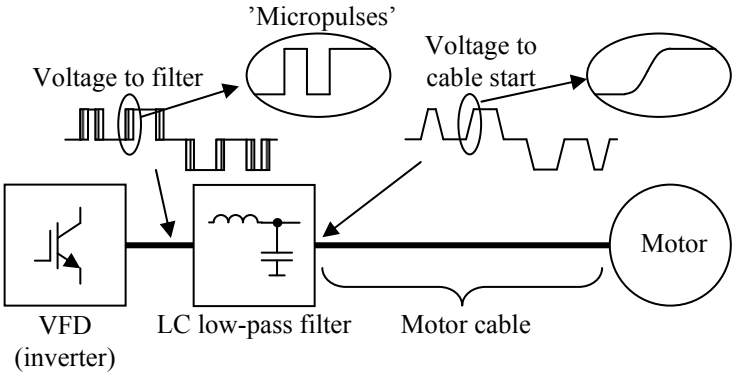


Figure 1.3. In active d*u*/d*t* output filtering, the original motor control voltage pulses, produced in the VFD, are further shaped to have serrated edges. This edge-modulated PWM voltage is then processed in a passive LC filter. The voltage at the motor cable input has a reduced d*u*/d*t*.

linearity problems encountered when applying the active d*u*/d*t* output filtering method to actual IGBT VFDs. It has been previously stated in (Ström, 2009) and (Ström et al., 2011) that switching behavior deviations and performance limitations such as the phase leg shoot-through prevention can make the implementation of the active d*u*/d*t* output filtering challenging with actual devices.

The open issues in the previous studies on the active d*u*/d*t* filtering are related to the non-idealities and limitations on IGBT variable frequency drives when operated with this new filtering scheme. The inclusion of the blanking times and possible minimum pulse width limitations, together with the noninstantaneous voltage transition edges and switching delays from the IGBT half-bridge itself, complicates the operation of the active d*u*/d*t* method when compared with the operation analysis with ideal switching components. The operation of the active d*u*/d*t* filtering requires narrow voltage pulses from the transistors. In the timescale of the active d*u*/d*t* operation for every voltage pulse fed into the motor cable, the transistors show pronounced nonideal behavior. The timing deviations and delays of switching operations in the transistors constitute a significant proportion of the pulse durations used in the active d*u*/d*t* method. Relating these nonidealities to the filtering operation is the very scope of this thesis. A simplified block diagram of the timing distortion affecting the active d*u*/d*t* output filtering method is shown in Figure 1.4.

As the question of drive efficiency and losses is also an integral part of an analysis of variable-speed drives, the loss measurements and the analysis of losses with active d*u*/d*t* filtering are included in the work. By using calorimetric measurement chambers, the effect of active d*u*/d*t* filtering on the losses in the variable-frequency drive unit and the filter circuit has been measured. These results are compared with the ones obtained by traditional passive filtering methods. The overvoltage reduction performance is also addressed. Transistors equipped with silicon carbide (SiC) freewheeling diodes were available for measurements, and the use of SiC diodes is demonstrated.

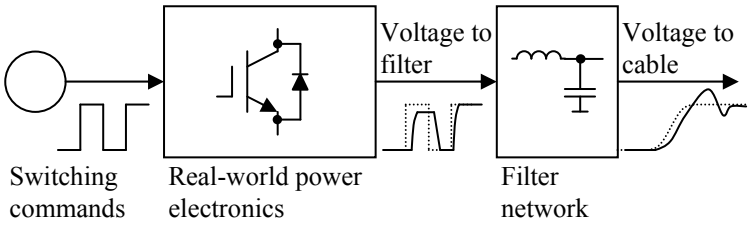


Figure 1.4. Control electronics produces the switching commands for the power electronic switches. The resulting output voltage from the inverter is not quite as expected because of the timing distortion and nonidealities in the actual electronics. As a result, the filtering operation is disturbed and the voltage fed to the cable is not a clean slope as previosly shown, but has artifacts. The more distorted the timing and shape of the filter input voltage pulse waveform are, the more distorted the filter output voltage becomes.

To summarize, the objectives and research questions in this doctoral thesis work are:

- Expanding the previous ADUDT control principle by introducing provisions for phase-leg dead time and IGBT delay compensation. The target is to achieve error-free ADUDT control operation even when nonideal power electronics is used. The control method should be flexible in terms of dead time insertion. This method is a direct improvement to the work presented in (Ström, 2009).
- Comparing the du/dt reduction performance with traditional passive filtering methods, as used in typical industrial applications.
- Comparing the losses associated with these filtering methods. The ADUDT method with two different filter designs is compared with all-passive du/d$t$and sine filters. Future trends in semiconductor device improvement are included by tests with SiC diode-equipped IGBT modules.

1.1 Motivation of the work

The active du/dt output filtering (ADUDT) method as discussed in this thesis has previously been presented for overvoltage limitation in variable-speed AC motor drives in (Ström, 2009). There are other du/d$t$reduction methods that rely on active control, such as the resonant DC link method in (Choi and Sul, 1995b), (Kim and Sul, 1995), and (Kedarisetti and Mutschler, 2011), and the various methods that directly affect the phase leg output du/d$t$such as in (Idir et al., 2006), (Kagerbauer and Jahns, 2007). The acronym ADUDT, however, is exclusively reserved for the kind of active voltage pulse control of an LC circuit as described in this thesis, and as presented in (Ström, 2009). The method uses narrow voltage pulses from a variable-frequency drive in conjunction with a passive filter network to achieve reduced voltage transition rates on the motor cable. With the future improvements in the power semiconductor

switching device technology for the variable-speed drive use, the method can provide a physically smaller and lighter filter network construction compared with the traditional passive du/dt filters, which does not use the active participation of switching devices in the control of the voltage slope shape. Furthermore, the quality of the voltage fed to the motor cable can be made superior compared with the traditional all-passive du/dt filters. In theory, the losses in the filter network itself can be made zero with the active method, since the step response damping is not dependent on the passive damping. This is also a difference compared with traditional du/dt filters, which, to a varying degree, rely on the ohmic losses for correct operation (damping), as published for instance in (von Jouanne and Enjeti, 1997) and (Akagi and Matsumura, 2011). Using active filtering requires no additional power electronic components in the drive system, and it can handle at least the same cable lengths as passive du/dt filters. In addition, the inductance of an ADUDT filter is smaller than that of all-passive methods, thereby causing less voltage loss across the filter, enabling an increased flux, and thus, more motor power (Krause et al., 2002).

The main open issues with using the active du/dt method in actual drive applications concern the nonideal switching characteristics of IGBTs, the proper design of the filter network, and the prediction of losses and component reliability. Previous studies were carried out with a 5.5 kW motor load in (Ström, 2009). The results and analysis suggested a control problem mainly arising from the interaction of the load current and the filter pulse operation. The problem would become more evident if the motor current were to be increased in relation to the filter circuit impedance, leading to an increased overshoot in the filter output voltage and thus, an additional overvoltage at the motor terminals. The analysis and the first solution to the blanking time effect mitigation assumed ideal switches in the inverter (ideal meaning here instantaneous changes in voltage and current commutation), which is not the case in an actual drive. In addition, several publications call for a dead time or a blanking time between two transistors in a phase leg of an inverter, as published in (Holmes and Lipo, 2003), (Leggate and Kerkman, 1997), and (Leonhard et al., 1989). This would leave a time period where the voltage fed to the filter cannot be actively acted on by the transistors. According to the previous knowledge on the active du/dt filter control principle there was no means of compensating for this effect, and therefore, an improved control principle was required.

In reality, the switching timing of an actual IGBT phase leg has timing deviations, and this further complicates the implementation of the ADUDT in a drive system. All in all, it was found that leaving the timing deviation and the dead time problem unsolved would result in an unsatisfactory output voltage performance, leading to a self-induced overshoot in the output voltage. As the problem becomes more pronounced when the load current to filter impedance ratio is increased, the improved control principle had to be designed to enable the ADUDT use with ever-increasing load current ratings. The effects of IGBT timing deviations were investigated in a case study, and a simple fixed compensation value was tried as a method to limit the timing deviation effects. It must be noted that in the control method proposed in this thesis, and in previous ADUDT studies, the filter topology is fixed as an LC low-pass with a capacitor return path to the VFD lower DC bus, as shown in Figures 1.3 and 2.11. It is possible that changing the filter topology also changes the method's sensitivity to the nonlinearity and load effects. Such a study would be in the scope of future studies.

1.2 Objectives and outline of the thesis

Figure 1.5 (appearing later) shows the block diagram timeline and structure of the study as presented in this thesis.

The first objective of the work presented in this thesis is to provide an improved solution for the active d*u*/d*t* filtering control method when the limitations of IGBT switching operation are included in the analysis. The target is to produce a control method that will take the blanking times of the IGBT inverter into account. The objective is to have a control algorithm that solves the timing parameters for the active d*u*/d*t* control sequence, preferably compensates for timing deviations to some extent, and achieves a filter output voltage with a minimum overshoot, regardless of the load current value and parameter variations. This will then enable the application of the ADUDT in a variable-speed drive prototype. The previous setup had a sufficiently low motor current (11.5 A) to show no noticeable effect on the filter operation, as described above. Thus, the requirement for the load current compensation pulse was not yet conceived, and any dead time effects were unknown (see pulse pattern nomenclature in Figure 2.14). A 22 kW motor with 43 A motor current is sufficient to produce a noticeable control error with that same filter. Current compensation pulse was required, but in order to implement that pulse, the dead times within the ADUDT pulse pattern were required, complicating the control principle. With dead times, zero-current clamping periods may appear, during which the control needs further compensation. The control method was reiterated to include this compensation, as presented in this thesis.

Initially, the dead time between the control of the transistors, possibly translating into a short period of time with no option to choose the filter input voltage, was assumed to be the main nonideality in the transistors, and thus, the obvious starting point for developing the enhanced principle. At the same time, it was expected that there would be gate control signal delays affecting the process. These were to be taken into account by compensating the delays and the switching losses. An enhanced control principle was developed, tested in operation, and described in this thesis. However, in the later phase of the study, the timing deviations and the behavior of the blanking time were found to be more deeply involved in the ADUDT operation than previously regarded. The very nature of the enhanced ADUDT control algorithm was reiterated. From that point on, the focus of the study was placed on the nature of phase leg output voltage timing deviations. The study could help in the future development of the active d*u*/d*t* filtering control method. The analysis of the timing distortion, variable blanking times, and phase leg shoot-through is thus the second objective of this thesis. The findings should give a good starting point for future delay compensation study.

The third objective is the overvoltage reduction performance comparison of the ADUDT compared with the traditional all-passive output filtering methods. These tests should be carried out with a loaded motor drive and a significant cable length (200 m used for 43 A tests), including passive filters that are typical for industrial use today.

The fourth objective is to investigate the losses and impact of active d*u*/d*t* filtering on the drive efficiency. This will also cover the comparison with the traditional filtering methods. A comparison with passive d*u*/d*t* filters and passive sinusoidal output filters is provided. A

comparison of different IGBT transistor modules is included, with one module containing silicon carbide freewheeling diodes. This may give an answer to the question of what the most desirable characteristics of the IGBT modules are for the active du/dt filtering use.

Chapter 2 describes variable-speed drives in general. The chapter provides reference literature and background information, and places the work in the context of other research in the field. The operation of a typical variable-speed drive is presented. The transmission line theory is used to explain the nature and source of the motor overvoltage phenomenon. A review of traditional overvoltage mitigation methods is given. The basic operation theory of the active du/dt filtering is presented. The chapter introduces the most significant nonideal switching characteristics of IGBT transistors with freewheeling diodes in bridge configurations, as is the case in an actual drive system. Finally, the insulation properties and bearing deterioration effects in asynchronous induction machines are discussed. This is in strong relation to the very need of overvoltage limitation and output filtering in variable-speed drives.

Chapter 3 includes an analysis of what is currently understood as the main challenge in the application of the active du/dt filtering in motor drives, that is, the dead time and voltage pulse timing deviations. The chapter studies the nonideal characteristics of the IGBT phase leg and their effect on the control principle. A theoretical approach to the IGBT operation is taken as a starting point. Then, the experimental setup and its inverter are used as an example of how the timing deviations are determined, and what are their possible effects in the ADUDT.

Chapter 4 continues by finding an enhanced active du/dt filtering control principle for the ADUDT. Compared with the previous control principle, its main difference is the ability to handle blanking times and pulse width limitations in the control pulse pattern. It shows a step-by-step evolution of the previous control principle to the new one. The control equations produce timing data for switches with no delay, and thereby, there could be a timing compensation module to add corrections to the switch commands. The timing distortions could then be corrected by this compensation module. However, the implementation and development of a full delay compensation module is left for future study, and a simple approach of single fixed compensation values is used in the test setup measurements.

Chapter 5 discusses the implementation of the improved ADUDT control into a drive system, the motor voltage and loss measurement methods, and the results. The control algorithm is programmed in a custom-modified experimental setup. In the next step, the inverter and filter losses are tested in a calorimeter, and the cable reflection performance is measured. Traditional passive output filters with laminated iron cores are available for comparisons. Two different active du/dt output filters, ferrite/Litz wire and air core/ordinary wire, are compared. The results indicate that the new control method works, yields an excellent overvoltage reduction capability, and allows the reduction of filter losses. With the ADUDT, the average peak voltage at the motor terminals is 700 V, compared with 960 V with the traditional all-passive du/dt filtering (1050 V with no filter at all, and a 200 m cable used in all cases). However, the losses in the inverter increase by about 82% because of the active du/dt subpulsing. Silicon carbide freewheeling diodes are compared with silicon diodes in the active du/dt operation, and it is found that the emerging semiconductor technologies can help to improve the loss case for active du/dt filtering (18% decrease in losses, SiC versus Si).

1.3 Scientific contributions

The scientific contributions of this doctoral thesis are:

- Development of an enhanced active du/dt output filtering control method. As a new feature, it can operate with blanking times and pulse width limitations in the IGBT transistor half-bridge. This new method makes it possible to apply active du/dt filtering to motor drives with increasing motor current values, and thereby, drive powers.
- Investigation of IGBT phase leg timing deviation effects on the ADUDT application. The test setup is used as a case study, and synthetic delay values are simulated to study the relation between a timing deviation and the ADUDT filter output voltage quality.
- Investigating the motor overvoltage prevention performance and the design of the ADUDT filter. Comparisons with traditional all-passive filtering methods.
- Loss and motor overvoltage measurements on an active du/dt prototype and a comparison with passive filtering methods. The impact on the total system losses and efficiency in an active du/dt filter-equipped variable-speed drive. The effect of using silicon carbide freewheeling diodes in a variable-speed drive with the active du/dt output filtering is considered.

The new control method is based on the theory of ADUDT filter operation, and applies to any power semiconductor switching devices used in the phase leg. The method used to investigate the nonlinearity effects is applicable to other switching devices than IGBTs. The quantitative results, however, apply to the partical case study only, and the method sensitivity to nonlinearities also depends on the chosen parameters. Thus, the main claim is over the improved method, with nonlinearity effects shown as an example case.

The author has published scientific results and findings as a coauthor in the following publications related to the topic of the doctoral thesis:

P1 J. Tyster, T. Kärkkäinen, J.-P. Ström, J. Korhonen, and P. Silventoinen, IGBT Phase Leg Non-idealities in Active d*u*/d*t* Output Filtering, in *Proc. of the 15th European Conference on Power Electronics and Applications (EPE2013)*, 3–5 Sept. 2013, Lille, France.

P2 J. Tyster, J.-P. Ström, J. Korhonen, and P. Silventoinen, Efficiency Measurements on Active d*u*/d*t* Output Filtering, in *Proc. of the 14th European Conference on Power Electronics and Applications (EPE2011)*, 30 Aug.–1 Sept. 2011, Birmingham, UK.

P3 J.-P. Ström, J. Korhonen, J. Tyster, and P. Silventoinen, Active d*u*/d*t*—New Output Filtering Approach for Inverter-Fed Electric Drives, *IEEE Transactions on Industrial Electronics*, Vol. 58, Iss. 9, pp. 3840–3847.

P4 J. Tyster, M. Iskanius, J.-P. Ström, J. Korhonen, K. Rauma, H. Sarén, and P. Silventoinen, High-speed gate drive scheme for three-phase inverter with twenty nanosecond minimum gate drive pulse, in *Proc. of the 13th European Conference on Power Electronics and Applications (EPE2009)*, 8–10 Sept. 2009, Barcelona, Spain.

P5 J.-P. Ström, J. Tyster, J. Korhonen, K. Rauma, H. Sarén, and P. Silventoinen, Active du/dt filtering for variable-speed AC drives, in *Proc. of the 13th European Conference on Power Electronics and Applications (EPE2009)*, 8–10 Sept. 2009, Barcelona, Spain.

P6 J. Korhonen, T. Itkonen, J.-P. Ström, J. Tyster, and P. Silventoinen, Active motor terminal overvoltage mitigation method for parallel two-level voltage source inverters, in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE 2010)*, 12–16 Sept. 2010, Atlanta, USA, pp. 757–763.

P7 J. Korhonen, J.-P. Ström, J. Tyster, P. Silventoinen, H. Sarén, and K. Rauma, Control of an inverter output active du/dt filtering method, in *Proceedings of the 35th Annual Conference of the IEEE Industrial Electronics Society (IECON2009)*, 3–5 Nov. 2009, Porto, Portugal, pp. 316–321.

J. Tyster has been the primary author in **P1**, **P2**, and **P4**. The operation principle and circuit design in **P4** was performed by M. Iskanius, and the measurements were conducted by J. Tyster. The transmission line transient analysis in **P6** was made by J. Tyster, and the operation principle presented in the publication was provided by J. Korhonen. The preliminary active d*u*/d*t* operation principle analysis in **P3**, **P5**, and **P7** was made by J.-P. Ström, J. Tyster, and J. Korhonen.

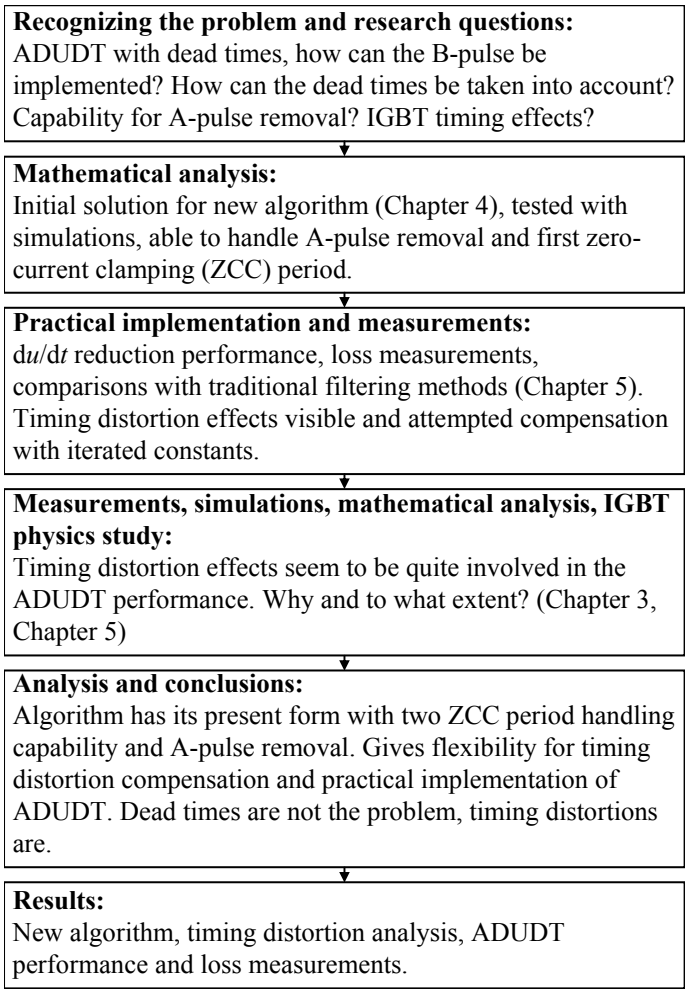


Figure 1.5. Step-by-step phases of the ADUDT study of this thesis. For the nomenclature of A- and B-pulses and ZCC, see Figure 2.15.

Chapter 2

Variable-speed AC drives and active d*u*/d*t* output filtering

Controlling the speed and torque of an AC three-phase motor with a power electronic converter is a well-established technology. From the dawn of controllable power electronic switching devices, through the 1980s when insulated gate bipolar transistors (IGBTs) were introduced, variable-speed AC drives have had a strong foothold in industrial motor drives. We will limit our scope to drives with low-voltage (line-to-line below 1 kV) two-level voltage source inverters. IGBTs are assumed the switching devices in the inverter, as is the case in present-day industrial low-voltage converters. Unless otherwise stated, we assume that the application is a motor drive, where the variable-frequency drive is feeding a motor, producing mechanical work. The motor type considered is a three-phase induction machine with a squirrel cage rotor. Other motor types could be used; for instance, synchronous motors with a field winding or permanent magnets, as the main topic (active d*u*/d*t* filtering) is not integrally dependent on the type of the electric machine. Special applications could also depend on using different switching devices than IGBTs.

The control principles for the motor in such a drive application have been extensively studied. The work in this thesis is based on applications where the three-phase voltages are formed by a method of constant switching frequency pulse width modulation. The rest of the details in the motor control are of less importance when analyzing the operation of active d*u*/d*t* filtering. The example analysis of a motor control application is thus very general, using voltage space vector modulation as a starting point. This chapter discusses the details relevant to the active d*u*/d*t* filtering operation design.

2.1 Operation of a voltage source inverter

The simplified main circuit of a variable-frequency drive with the key components relevant to the drive operation is shown in Figure 2.1. It shows the connection to a three-phase AC grid, providing electric power to the converter. The input filter is of a low-pass type, helping in reducing high grid harmonics otherwise caused by the input bridge rectifier. The rectifier generates a DC voltage on the intermediate circuit capacitor, which acts as a DC voltage source for the three-phase inverter. The three-phase inverter with IGBTs produces a three-phase voltage at the inverter output phases. We assume that the application may require an output filter to make the voltage generated by the inverter more motor-friendly, thereby increasing the quality of the voltage at the motor terminals. The motor is connected via a motor cable, having the phase conductors and usually a protective earth conductor and a shield. The physical length of the cable depends on the installation.

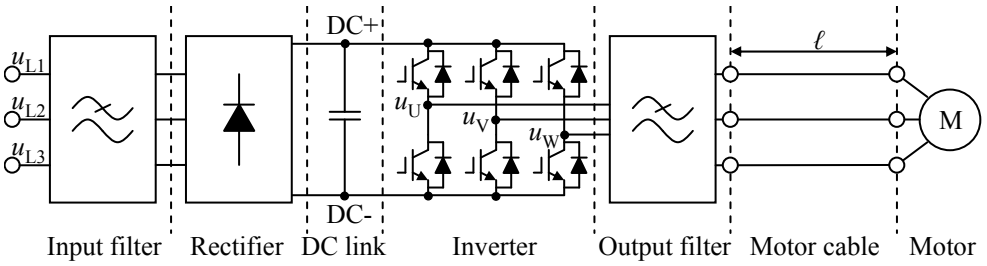


Figure 2.1. Basic configuration of a voltage-source inverter variable-speed drive.

As depicted in Figure 2.1, the inverter consists of three phase legs with two transistors in each leg, the upper and lower transistor. In addition, there are freewheeling diodes connected in parallel with each transistor. A simplified analysis replaces the transistors with ideal switches, with ideal diodes providing a current conduction path for the reverse current flow in the phase leg. We will later refine the analysis of an IGBT phase leg. The transistors are commanded to conduct and form an inverter output voltage that will cause the desired speed and torque in the electric motor. As discussed above, there are numerous control principles for this operation. We will discuss the pulse width modulation method using voltage space vector modulation. What is significant for the active du/dt filtering operation and the motor overvoltage phenomenon is the fact that transistors are used as switches, producing voltage pulses at the inverter output. The above-mentioned concepts will be used in the example analysis, suitable for the scalar U/f control and field-oriented control of an AC induction machine. Other methods are described in the literature (Rodriguez et al., 2012).

Space vector theory is applied to produce the desired output voltage at the inverter (Holmes and Lipo, 2003). Having a constant switching frequency and period and taking an average over that period, the phase leg output voltage can be varied from 0 to U_{DC} by the duty cycle of the two switches. Assuming a complementary operation of these switches with no blanking time between the control signals, the duty cycle of the upper switch is the average voltage of the phase output. The space vector theory further defines the eight possible switch state combinations in the inverter. The remaining combinations result in both the upper and

lower switch conducting in at least one phase leg. This condition would lead to a phase leg shoot-through (also known as a phase leg short circuit, cross conduction), and thus, these combinations are not allowed. A phase leg short circuit leads to a rapid current increase in the switches, which, being physical devices with limits, may be destroyed. When arranged in a proper sequence, the eight permissible combinations result in a three-phase voltage at the inverter output. Since the motor has inductance, the current waveform is not a similar pulse train as the voltage is. Rather, the current takes a form defined by the three-phase quality of the voltage, with some ripple. Often, the motor current is taken as the controlled quantity, with the inverter output voltage seen as an intermediate step in generating that current. The motor control software calculates the desired three-phase current and updates the phase leg duty cycles accordingly, at a sufficiently high repetition rate (common is the same rate as the switching frequency), enabling motor speed and torque control.

A typical inverter output voltage waveform seen between two phase conductors is shown in Figure 2.2. This is a measured case with no motor cable effects. The three-phase voltage will also occur at the motor terminals, causing a motor current to flow. A typical switching frequency for low-voltage drives starts at 1 kHz, with higher switching frequencies used for instance in permanent magnet AC servo motor applications. The choice of the switching frequency depends on many aspects and is not always trivial. Increasing the frequency increases the switching losses in the transistors, but results in a lower current ripple in the motor, thus reducing some of its losses. If sinusoidal output filters are used, a higher switching frequency allows a physically smaller size of the filter. Without a clear boundary, it is typical to use lower switching frequencies in large motor drives and higher frequencies in smaller drives.

A simplified approach is taken here to the motor voltage and current relationship. It suffices for the analysis of ADUDT filter operation under electric machine load. As is the case with sinusoidal motor voltages (e.g. in direct grid connection), the current can have a certain phase shift in relation to the fundamental frequency component of the inverter output voltage. The relation of the three-phase motor voltage to its current depends on the loading of the motor. It is common to use a single-phase equivalent circuit to model the behavior of the voltage and current in the motor. Each motor phase is seen as an equivalent circuit network between the phase terminal and a fictitious neutral point of the winding. This equivalent circuit method is common and suitable for the steady-state analysis of the motor (Krause et al., 2002). Later on, the high-frequency impedance behavior of the motor will be included. In this step, the emphasis is on the fundamental frequency characteristics. This equivalent circuit is shown in Figure 2.3.

The significance of the equivalent circuit is to recognize the inductances in the motor and, in general, that the motor voltage and current waveforms can take a drastically dissimilar shape, as shown above. It also means that the motor load current can be seen as a continuous waveform even though the voltage level constantly changes as a result of the switching operation. This is due to the inductance in the motor. Now, we recall that the voltage pulses generated by the inverter are the means to emulate a sinusoidal three-phase voltage, and to form the current in the motor, there can be four different current commutation/output voltage transition combinations in any given phase leg. Assume that the phase leg switch statuses are about to be changed at some point in time. The current direction can be positive or negative

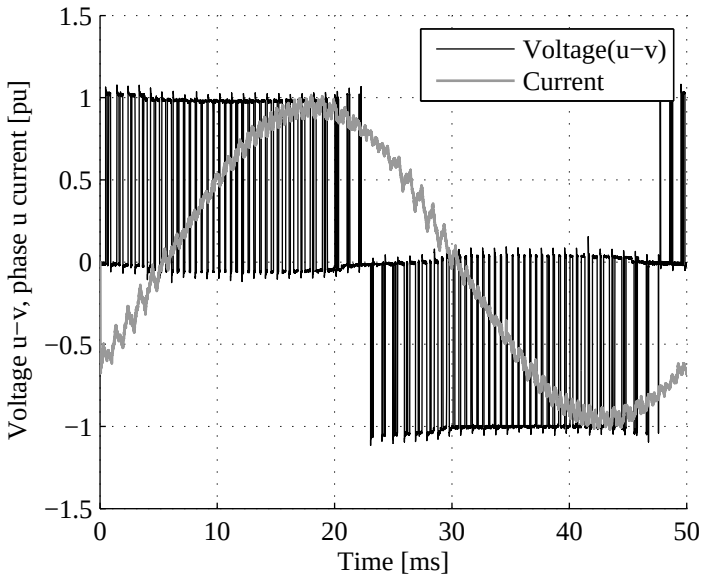


Figure 2.2. Pulse-width-modulated output voltage and motor current at the inverter output. This is a measured case of a loaded 22 kW motor with approx. 25 Hz VFD voltage frequency. 1 pu current has a peak value of 61 A. The voltage pulses have an amplitude of approx. 540 V. See Appendix E for the motor data.

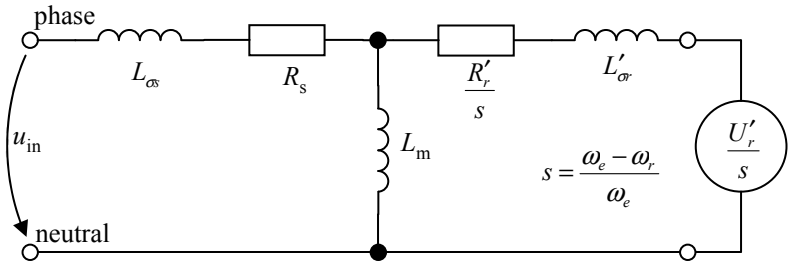


Figure 2.3. Motor equivalent circuit. The motor can be seen to have a certain inductance in series with the part representing mechanical work (Krause et al., 2002).

before this status changes, and the current may change its direction during the switch status change. The switch statuses can be either a command for the upper switch to conduct or the lower switch to conduct, neglecting any possibility of a blanking time at this stage. These status changes correspond to the phase leg instantaneous voltage to be forced to either 0 or U_{DC}, with the reference point being the lower bus bar of the inverter. Thus, the four current commutation/voltage transition combinations are

- Current flowing in the phase leg with the voltage commanded to zero.

- Current flowing in the phase leg with the voltage commanded to U_{DC}.
- Current flowing out of the phase leg with the voltage commanded to zero.
- Current flowing out of the phase leg with the voltage commanded to U_{DC}.

When there is a possible blanking time in the phase half-bridge resulting from dead times, the voltage of the phase output is determined by the current direction only. It is also possible for the leg current to be zero, and if neither of the IGBTs are in conducting state, the leg output is in relatively high-impedance state and floating, in which case the output voltage is determined by the load voltage, within the freewheeling diode clamping limits.

2.2 Power electronic components

Power electronic components refer not only to the transistors and diodes in the drive, but also to the capacitors and inductors in the main circuit. If the components are viewed as ideal, many power electronics design challenges are missed. With the assumption of ideal components, it is possible to design, simulate, and analyze circuits that are not practical in reality, or are impossible to implement in actual hardware. However, at the same time, even new ideas should be given a hardware test, especially if in doubt. For active du/dt filtering operation, with the atypical use of switching commands in contrast to the traditional VSI use, there were doubts if the IGBTs can be used for the purpose at all.

Two immediate targets for the nonideality analysis are the transistors and the diodes in the inverter, with perhaps the intermediate circuit capacitor. The output filter is a circuit consisting primarily of inductors and capacitors, with possible additional active components such as clamping diodes. These components are in the main current path (the motor current), and have to experience the pulsed voltage from the inverter and perform their task in the rated operating conditions. The input rectifier and filter are an integral part of the converter operation, but their nonidealities will not be included in the analysis. This is justified as the active du/dt filtering method mainly affects the inverter components and the intermediate circuit.

2.2.1 IGBTs

The development of the IGBT started in the early 1980s (Baliga, 2008). Before that, bipolar junction transistors (BJT) and metal-oxide semiconductor field effect transistors (MOSFET), in different configurations and combinations, were the only available fully controllable power switching devices suitable for compact low-voltage applications. Gate turn-off thyristors (GTO) were available, but with ratings more suitable for very large medium-voltage multi-level converters. Hence, the BJT and MOSFET devices were the starting point for improvement. Power BJTs suitable for the voltage and current levels of a low-voltage drive have a low current gain, increasing the complexity and cost of the control circuitry. They have

a limited Safe Operating Area (SOA), requiring the use of external protection in switching applications, further making the BJTs unfavorable. BJTs can be designed for reduced losses when conducting current. At the same time, the charge carrier storage time effects limit the switching speed and increase the losses in the transistor when it is being turned on and off. The MOSFET, being a majority-carrier device instead, could be made to switch very fast and have low switching losses. It has an insulated gate structure, requiring minimal control power compared with a BJT. Unfortunately, the original MOSFET has high conduction losses when designed for the voltage levels encountered in a low-voltage drive (600 V, 1200 V, and 1700 V blocking voltages). More recent developments with superjunction MOSFETS have shown reduced on-state losses (Lutz et al., 2011). The IGBT is a component integrating the positive characteristics of both the BJTs and MOSFETs.

The freewheeling diode is normally packaged with the IGBT. The diode is connected in an antiparallel configuration. Its function is to conduct any reverse current flowing through the device in the phase leg. As noted in the motor equivalent circuit analysis, the motor comprises inductive components. This current flowing through the inductive load must always have a path. This is the reason for freewheeling diodes; to provide a path for reactive current. A package containing an IGBT and a diode with electrical connections is called a module. Thus, it is important that the diode with the IGBT and their characteristics are evaluated as a single device.

The primary nonideal characteristics of the IGBT/diode combination with a gate driver, relevant to the ADUDT application, are

- Turn-on and turn-off delays, generally being variable in nature (Figure 2.4(A)),
- Voltage and current rise times and fall times are not zero during switching, and can depend on the current in the phase leg (Figure 2.4(B)),
- When turned off, the IGBT current shows a rather long current tail (Figure 2.4(C)),
- Minimum time between the turn-on and turn-off instances as a result of the diode dynamic characteristics (charge carrier distribution time in soft recovery diodes) (Lutz et al., 2011) (Figure 2.4(D)),
- The diode exhibits reverse recovery when it changes from the conducting state to the blocking state. This introduces a current pulse through the diode caused by the removal of the reverse recovery charge (Figure 2.4(E)).

Furthermore, the variability of these characteristics can challenge the operation. A deviation from ideal operation is simpler to compensate for if it is constant or otherwise known. The deviations related to the timing (delays, rise/fall times) of the current flow and voltage have the highest impact. As the gate driver adds its own delays and pulse distortion, it has been customary to include a dead time between the control signals of the upper and lower transistors in a phase leg. The purpose of this blanking time is to guarantee that no shoot-through occurs in the phase leg. As will be later discussed with the enhanced active d*u*/d*t* control

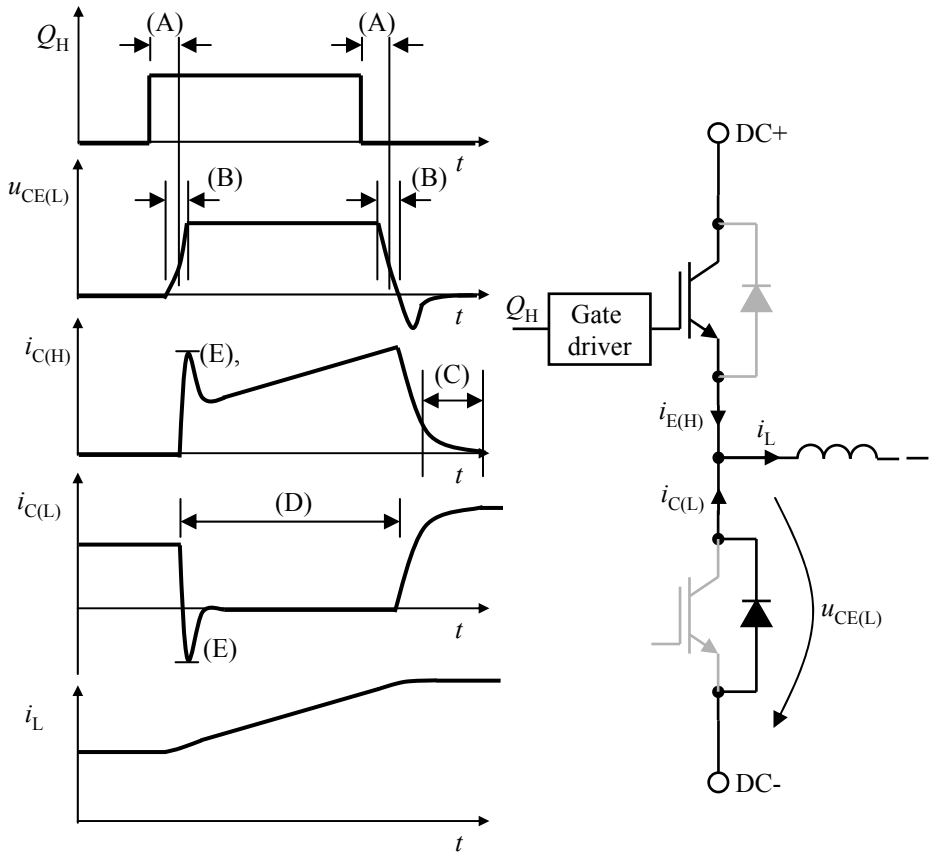


Figure 2.4. The nonideal characteristics of the phase leg that are of main concern in ADUDT nonlinearity effect study. Dead time is not included, as its effect is mainly zero-current clamping (ZCC) in the control pulse pattern, which in principle is not a timing deviation but a completely separate pattern component.

scheme, it is these nonidealities that challenge the implementation of the active d*u*/d*t* filtering in a variable-speed AC drive. Typical turn-on and turn-off delays, voltage and current rise and fall times, and suggested dead times are in the same timescale as the switching sequence of the active d*u*/d*t* filtering.

2.2.2 Inductors and capacitors

There are nonideal characteristics also in the passive components to be taken into account when designing a variable-speed drive (Kerkman et al., 2003). Inductors have resistance because of the limited conductivity of their winding material. The well-known high-frequency phenomena of skin and proximity effects further increase this resistance in the case of high

frequencies in the current flowing through the inductor (Mohan et al., 2003). Losses in the core material can be modeled as a resistance parallel to the inductor. The core design geometry can lead to a stray flux and fringing effect (Mohan et al., 2003), coupling to any nearby conductive material, and thereby losses in external components not necessarily within the inductive component. The problem is more pronounced in cores with large air gaps or inductors without any separate core (air-core inductors). The magnetization strength in the inductor core can be so high that noticeable nonlinear characteristics between the current and the inductance are seen. The inductor starts to saturate, resulting in an inductance being a function of current. If, in this case, the inductor is part of a filter network, the behavior of the filter circuit becomes nonlinear. From all the other nonidealities, this was found to be of the least concern in the filter design. The resistance effects are more profound, as they are linked to the efficiency of the drive. In addition, the winding configuration leads to a parasitic capacitance between the inductor terminals. High-frequency signals can pass through this path, bypassing the inductor. This problem is more pronounced in multilayer windings (Mohan et al., 2003).

The increased bulk weight and size are not generally desirable properties in any converter design. If the targets are a light weight and a small size, an inductor with a laminated steel core is a less attractive option. Having a high inductance in conjunction with a high current rating is a combination leading to a larger size compared with an inductor with less inductance and/or a smaller current rating. This is true with any magnetic component design. Inductance can be traded for saturation current rating and vice versa, if the core dimensions and material properties are kept constant (Mohan et al., 2003).

Capacitors can typically be found in two places in the intermediate circuit-inverter-output filter sections. With a voltage-source inverter, the DC link capacitor provides the bulk DC voltage ripple filtering and acts as a voltage source for the inverter. The bulk capacitance can be provided by aluminum electrolytic or plastic-film-insulated capacitors. The motivation to shift from electrolytic to plastic film capacitors is due to the latter having potentially increased life time and lower losses (Wechsler et al., 2012). Plastic film capacitors often have better high-frequency characteristics, being able to deliver more current at high frequencies with less voltage ripple. Owing to these qualities, they are also used in pulsed-power applications (Rabuffi and Picci, 2002). The second place to find capacitors is the output filter where they are used with inductors to form the desired low-pass function. Plastic film capacitors are invariably used in this application. The capacitor losses and pulse voltage rating limitations are important factors to be considered, and the capacitor loss should be taken into account when designing the ADUDT filter.

2.3 Cable reflections and motor overvoltages

According to the theory of electromagnetic waves in transmission lines, the voltages and the currents in motor cables are the result of such waves traveling along the line. This theory is established in the field, as published in (Heaviside, 1899), and repeated here for introductory purposes. The nomenclature for tansmission line and wave components shown here

follows (Pozar, 2005). At any given time, the voltage measured at any point along the line is the superposition of voltage waves traveling in the line. Simultaneously, current waves are observable in the conductors. What is significant is the way voltage and current should be viewed in this case. The basic circuit theory is not sufficient for wave propagation in the line. A voltage excitation in the form of a pulse or any transient change in relation to time causes a voltage wave to travel along the transmission line formed by the conductors of the motor cable. The voltage wave propagates in the insulation between the conductors. The basic transmission line model to explain the behavior is shown in Figure 2.5.

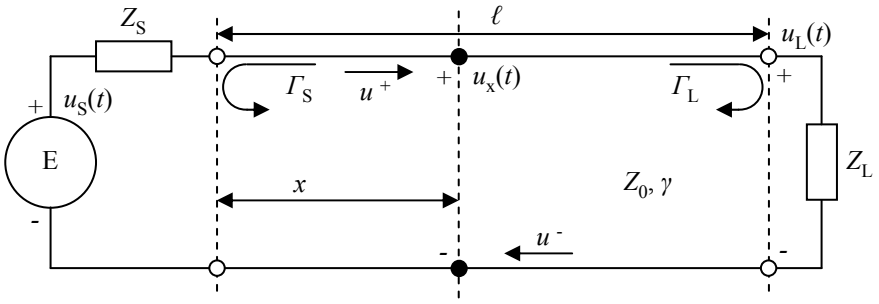


Figure 2.5. Basic transmission line circuit. Voltage waves are generated by a voltage source with some arbitrary impedance Z_S. The line has a characteristic impedance Z_0 and a propagation coefficient γ. The line is terminated with an arbitrary impedance Z_L. The line has a physical length ℓ. Γ_L and Γ_S are the load and source reflection coefficients, respectively.

The transmission line can be seen to form between any of the phase conductors, or between phase conductors and the protective earth conductor and/or the shield. Choosing the right conductor pair for the analysis depends on the voltage of interest. For phenomena related to voltages between the phases, two phase conductors is a natural choice. If the phase to ground voltage is of concern, the protective earth is taken as the second conductor. The actual three-phase motor control model is more complicated, and is discussed for instance in (Akagi and Matsumura, 2011).

The single-phase model can be found in (Moreira et al., 2002) and textbooks (Heaviside, 1899) and (Pozar, 2005). The analysis for the voltage waves are as follows. The line with two conductors is broken down to infinitesimally short sections comprising of the distributed components $R\Delta z$, $L\Delta z$, $G\Delta z$, and $C\Delta z$. These form the model for the transmission line as depicted in Figure 2.6, following the naming convection as shown in (Pozar, 2005).

$R\Delta z$ represents the ohmic losses in the conductors. $L\Delta z$ is the distributed self-inductance of the line, and $C\Delta z$ is the distributed capacitance between the conductors. $G\Delta z$ represents the dielectric losses in the insulation medium. As described by Heaviside's telegrapher's equations e.g. in (Pozar, 2005), as $\Delta z \to 0$, the following differential equations for the current and voltage hold

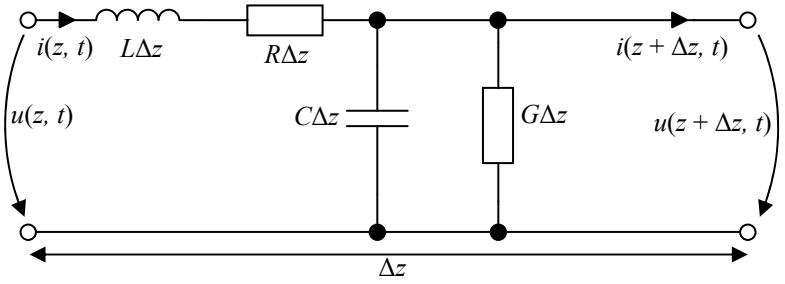


Figure 2.6. Distributed-parameter model for the transmission line, using infinitesimally short line sections (Δz) along the propagation direction (positive direction from left to right).

$$\frac{\partial u(z,t)}{\partial z} = -R'i(z,t) - L'\frac{\partial i(z,t)}{\partial t} \tag{2.1}$$

$$\frac{\partial i(z,t)}{\partial z} = -G'u(z,t) - C'\frac{\partial u(z,t)}{\partial t} \tag{2.2}$$

where the parameters with prime (e.g. L') are short-hand version of the Δz distributed parameters as above.

This partial differential equation pair describes the time-domain behavior of the voltage and current in the line in any given point along its length. The time-domain solution would give the wave solutions for transient voltages and current traveling in the line. Numerical methods can be used for the solution, and some forms of analytical solutions exist. These methods could be used to solve ADUDT voltage edge reflections in transmission lines. Such methods are published for instance in (Djordjevic et al., 1987) and (Marti, 1982).

Finding a solution for voltage and current in the line is simplified for sinusoidal steady-state values. This will not provide a direct answer for transient voltages, but illustrates the concept of cable reflection and the resulting overvoltage for sinusoids. The concept of harmonic analysis states that a periodic trapezoidal signal is composed of a series of harmonic sinusoids, and thus the transmission line and overvoltages can be analyzed in a simplified way, without a time-domain solution of the telegrapher equations.

First, we consider waves having a sinusoidal form and explain the motor overvoltage phenomenon using sinusoidal quantities. The propagation coefficient γ in the transmission line is

$$\gamma = \alpha + j\beta = \sqrt{(R\Delta z + j\omega L\Delta z)(G\Delta z + j\omega C\Delta z)} \tag{2.3}$$

The propagation coefficient γ contains the real part α that corresponds to the wave attenuation

in the line and the wave number β, which is related to the signal wave length in the line by

$$\lambda = \frac{2\pi}{\beta} \tag{2.4}$$

In a general case, the propagation coefficient is a function of signal frequency. For lines with loss components (R and G), the wave number is not linear in relation to the signal angular frequency ω. This is also known as dispersion in the line (Heaviside, 1899), (Pozar, 2005), and results in different harmonic components of a periodic voltage signal to propagate at different velocities. The effect is seen as steep voltage edges fed into a transmission line, which appear slanted at the end of the line.

The phase velocity for a single high-frequency signal propagating in the line is

$$v_p = \frac{\omega}{\beta} = \lambda f. \tag{2.5}$$

For transmission lines with reasonably small losses (low R and low G) compared with other lumped-parameter quantities, the wave propagation equations can be greatly simplified. For a lossless line with α close enough to zero to be omitted in the analysis, the phase velocity can also be expressed as

$$v_p = \frac{1}{\sqrt{L'C'}}, \tag{2.6}$$

where L' and C' again represent the distributed per-length unit parameters of the transmission line. For such a lossless line, the cable characteristic impedance Z_0, the ratio of the voltage wave amplitude to the current wave amplitude in the line, is

$$Z_0 = \sqrt{\frac{L'}{C'}} \tag{2.7}$$

It is in the interface of the load impedance Z_L and the cable characteristic impedance Z_0 where the main cause and motivation for output du/dt filters and the work presented in this thesis are encountered. As the voltage waves propagate in the line and arrive at the transmission line-load interface, the current wave amplitude must hold according to Kirchhoff's law. The current wave value at the load and the transmission line must be equal, but because of different impedances, the voltage must change. The load impedance Z_L may not have a same value as Z_0, and thus, the voltage in the load point is different than that of the incident propagating wave. A reflection occurs in this case, and for the reflected wave we can define a reflection coefficient Γ_L

$$\Gamma_{\mathrm{L}} = \frac{u^-}{u^+} = \frac{Z_{\mathrm{L}} - Z_0}{Z_{\mathrm{L}} + Z_0} \tag{2.8}$$

The voltage amplitude appearing at the load interface is

$$\frac{u_{\mathrm{L}}}{u^+} = 1 + \Gamma_{\mathrm{L}} = \frac{2Z_{\mathrm{L}}}{Z_{\mathrm{L}} + Z_0} \tag{2.9}$$

As the load impedance given by typical motor drive applications has values considerably higher than the transmission line characteristic impedance, the load reflection coefficient approches unity, and the load terminal voltage approaches a value double the incident wave amplitude.

It is true that the previous analysis holds for sinusoidal wave quantities; however, we see that the original telegrapher equations in (2.1) and (2.2) are in the time domain. A direct solution to the time-domain behavior could perhaps be found by solving the partial differential equations and placing the load impedance in the equations. However, it is known from harmonic analysis that increasing the slope rates of a trapezoidal signal also increases its harmonic content. The motor has a relatively high reflection coefficient for the typical switching frequency harmonics (Zhong et al., 1998). As the higher-order harmonics increase, these harmonics reflect at the motor terminals, causing the overvoltage.

The transmission line theory shows that the voltage fed to the motor cable at the inverter must be analyzed as an electromagnetic wave. As the voltage rise rate in the cable starting point (the inverter) is large enough, it will cause the voltage to increase at the motor terminals as a result of the reflection phenomenon. This has been previously studied and reported for instance in (Leggate et al., 1999), (Persson, 1992), (Saunders et al., 1996), and (Skibinski et al., 1998). The key is the voltage change rate versus time with respect to the propagation delay.

With the present-day IGBTs, the voltage rise and fall times experienced at the inverter output (100 ns not uncommon) are sufficient to cause almost doubling of the voltage amplitude at the motor terminals with cable lengths starting from 25 m (von Jouanne et al., 1996a). The motor impedance at high frequencies plays a certain role, but in general, this is a common problem (Persson, 1992). If the cable length is a fixed parameter in the drive design, there are the following solutions available

- Analyze the motor insulation withstand rating. If the overvoltage is not a problem for the insulations, bearings, or any other part of the mechanic system, no further action is needed. New techniques in the motor construction can make the motor less vulnerable to reflection overvoltages (Wheeler, 2005), (von Jouanne et al., 1998).
- Decrease the voltage rise time at the cable start by placing an output filter after the inverter, or otherwise change the operation of the inverter to achieve a lower du/dt

value at the cable input voltage and thus, a lower amount of high-frequency harmonics to reflect at the motor terminals (von Jouanne et al., 1998), (von Jouanne et al., 1996a), (Kagerbauer and Jahns, 2007).

2.4 Motor insulation systems

The motor insulation refers to the lacquer and insulation sheet layers in the windings of the electric machine. Insulation is present between the conductor turns occupying the stator slots in the machine, usually with an additional layer between the wire bundle and the slot walls and edges. During the motor operation, the motor terminal voltages are distributed along the winding turns. At the same time, the motor chassis (stator iron lamination stack and outer structure) is usually connected to the protective earth. Thus, there are potential places where the excess voltage can cause premature deterioration and accelerated aging in the insulations, leading for instance to partial discharge effects, and ultimately, a breakdown as a result of voltage stress. The voltage between the motor terminals is not evenly distributed in transient conditions (Hwang et al., 2005), (Persson, 1992). It has been observed that there may be as much as 85% of voltage drop at the first turn of the motor winding (Persson, 1992). The countermeasure is to increase the insulation of the first turn, and between the turn and the stator stack. The first turn overvoltage effects are of particular importance in random-wound low-voltage motor windings, where the first and last turns in the bundle can be adjacent to each other (Wheeler, 2005). Figure 2.7 shows the structure of a reinforced stator slot insulation system, for use with VFD duty with overvoltages.

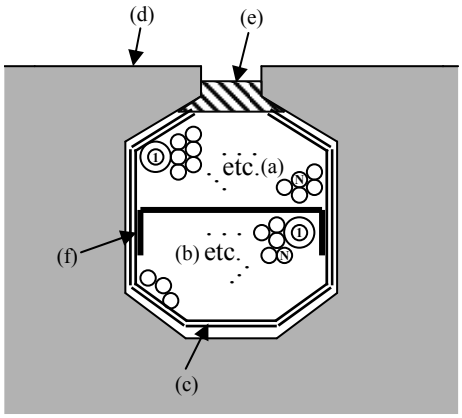


Figure 2.7. Motor winding insulations in the stator slot. The first turn insulation is reinforced against partial discharge (corona) effects. Shown here is a case where two winding bundles (a) and (b) occupy the slot, with insulation (f) in between. (d) is the stator iron, (e) is the insulating slot key, and (c) is the slot wall insulation. With random winding of the bundles, the first and last (N) turns can be located adjacent to each other.

The insulation withstand measurement methods and analysis are discussed in (Cavallini et al., 2010). On the same topic of generator applications, a measurement publication (Gupta et al., 1987) reported the effect of fast transient effects on an electric machine winding system. The conclusion, based on these publications, is that a motor overvoltage has been and still is a problem regardless of the recognition of the problem source. Decreasing the overvoltage will serve to extend the lifetime of the motor. In (Mirafzal et al., 2009), a different overvoltage mechanism is described, which is encountered even in systems with a very short motor cable length. It suggests that even these systems are not immune to a high du/dt.

HF bearing currents are another concern in variable-frequency drive applications. Because of the coupling phenomena in the motor air gap, there may be a small potential difference in the circuit formed by the stator stack, the rotor, and the bearings with rolling elements (Busse et al., 1997a), (Busse et al., 1997b). The increased du/dt in the motor terminals compared with a sine wave duty causes the voltage in the stator-rotor circuit to increase. The thin lubricating oil film on the roller elements breaks down under repetitive voltage pulses, causing erosion of the bearing raceways. Once again, decreasing the du/dt would help in reducing the erosion rate.

2.5 Motor overvoltage mitigation techniques

It is now clear that leaving a variable-speed drive without any consideration of the transient voltages can cause overvoltage problems at the motor. Methods to reduce the du/dt and overvoltage at the motor have been studied together with the development of PWM drive applications, and there are numerous publications on the issue, for instance (Moreira et al., 2005), (Moreira et al., 2002), (von Jouanne et al., 1996b), (Skibinski, 1996), (von Jouanne and Enjeti, 1997), (Finlayson, 1998), and (Akagi and Matsumura, 2011). The usual method is to employ a passive filter in the output of the inverter, before connecting to the cable. This filter network has a step response such that it lowers the du/dt value at the motor cable input. These passive filters, operating on the edges of the voltage pulses coming from the inverter, are known as passive du/dt filters. The basic single-phase equivalent circuit for such a filter is shown in Figure 2.8.

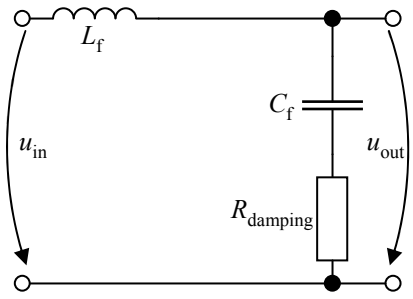


Figure 2.8. Low-pass LC output filter circuit for three-phase applications.

In practice, the filter will have some losses as discussed above. The loss in the filter circuit can occur in the form of copper losses in the windings, hysteresis and eddy current losses in the core material, and possibly when using a discrete resistor in the circuit. Thus, in general, we can view the passive filter as an RCL resonator. In addition to the basic LC circuit shown above, several other circuits have been proposed as a passive output filter solution. Some of these circuits are shown in Figure 2.9. An alternative to connecting a filter network to the output of the inverter is to use a terminating network at the motor terminals. This terminating network aims to form a reflection coefficient closer to zero at the motor terminals to the cable interface, thereby reducing the overvoltage. The circuits shown in Figures 2.9(a)–(c) are passive output filters while (d) is a terminating network.

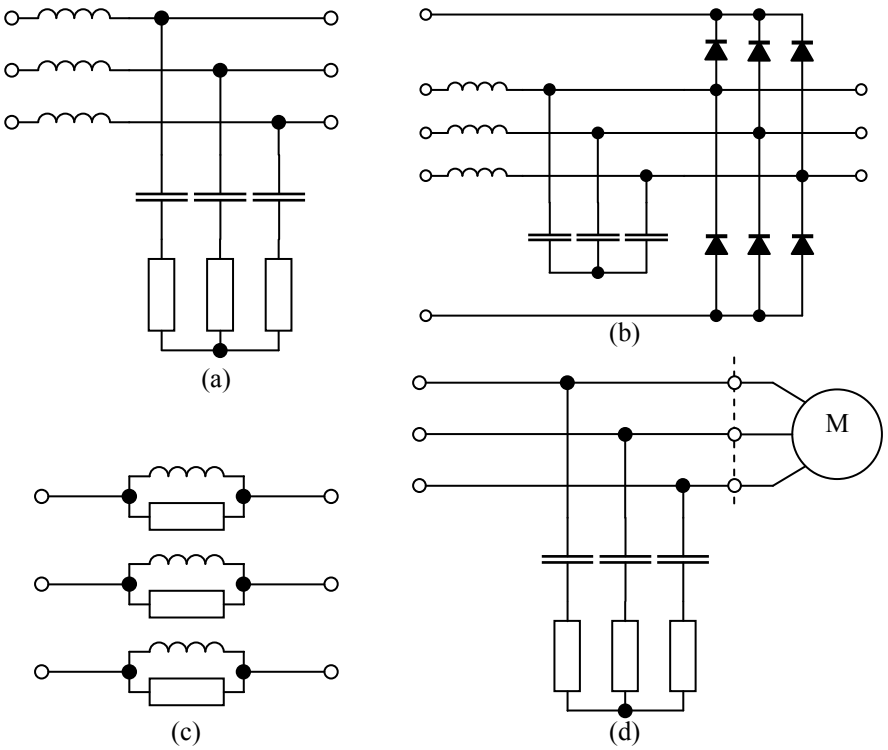


Figure 2.9. Various passive overvoltage mitigation solutions suggested for variable-speed AC drive applications. (a)–(c) are output filters, and (d) and is a terminating network affecting the load reflection coefficient at the motor terminals.

The operation of the terminator network is based on the impedance matching principle. As discussed above, by introducing a load impedance Z_L value closer to the motor cable characteristic impedance Z_0, the overvoltage caused by reflection is reduced. The resistors in the terminating network aim to achieve a load impedance matching the cable characteristic impedance Z_0, while the capacitors decouple the resistances in the steady state (after the edge transient has passed).

The passive output filters shown in Figures 2.9(a)–(b) generate voltage step responses formed by the inductance and the capacitance in the circuit, with the resistance providing the damping for the voltage resonance in (a). In the filter network (b), the voltage resonance is clamped with additional clamp diodes such that the output voltage after the filter will have no overshoot. In (a), the resistance determines the voltage overshoot at the filter output.

The RCL circuit can be modeled as a second-order system with an undamped resonant frequency determined by the inductance and the capacitance, and the damping factor ζ determined by the resistance or loss in the system. For various damping factor values in an exemplary system, the voltage step responses are as shown in Figure 2.10.

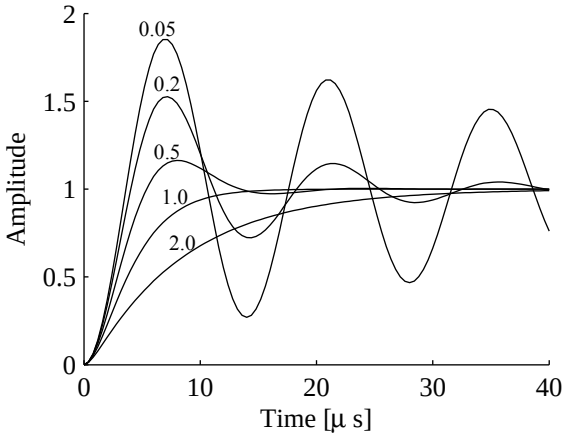


Figure 2.10. As the second-order system (such as an LC output filter) damping factor ζ (values shown) is varied by introducing losses in the circuit, the overshoot and peak rise time characteristics change.

As can be seen in Figure 2.10, a low damping factor will lead to a voltage overshoot. This overshoot is also present at the motor terminals, since it has been already generated by the output filter. On top of the filter-generated overvoltage, the possible cable-reflection-induced overvoltage is added. The diode-clamped output filter does not have this overshoot, since the overshooting voltage part is short-circuited to the DC link.

2.6 Active d*u*/d*t* output filtering method

The operation of the filtering methods described above depend on a suitably constructed filter network, which shapes the voltage pulse edges to reduce the voltage transients experienced by the motor cable. Apart from compensating for the possible voltage loss in the filter, the frequency converter does not play an active role in the transient reduction as such. The filter networks and cable terminating circuits can be seen as plug-in components in the otherwise unchanged drive system, perhaps taking the voltage drop into account in the motor control. However, the power electronics and drive control system could become part of the d*u*/d*t*

reduction operation, possibly working in conjunction with a suitably tuned passive filter or a cable terminator circuit. In this case, the proper overvoltage reduction operation is not completely dependent on the added passive circuitry, but would need some form of an active control of the power electronics system.

2.6.1 Active d*u*/d*t* output filtering (ADUDT), the prior art

The approach discussed throughout this doctoral thesis is the active d*u*/d*t* output filtering (ADUDT). Different types of active output filtering methods for d*u*/d*t* reduction can be divided in categories based on their operating principle. Let us consider the ADUDT, as presented in this thesis and the previous work around it, to form the first category in active d*u*/d*t* filtering methods. The ADUDT defines a solution using a passive output filter network (as in traditional, nonactive methods, but having a relatively high Q) combined with the necessary active control participation of the inverter voltage pulses. It is thus a high-Q resonant, passive output filter coupled with an active control of the inverter switching components in a way that results in a desirable d*u*/d*t* reduction at the motor cable. The use of active control aims to reduce the required physical and electrical size of the filter components (most often, the inductors being the bulkiest ones) while still being competitive or superior to traditional passive output filtering methods regarding the d*u*/d*t* reduction performance and the total drive efficiency. The ADUDT operates on the timescale of the required minimum slope time for zero overvoltage because of the load reflection. Thus, even though a sine filter can be seen as an identical LC network but with different values, and the active damping of the sine filter resonance (Laczynski et al., 2008) as a 'necessary active control participation', it does not meet the definition of ADUDT since the sine filter has a d*u*/d*t* reduction value considerably larger than what would be required for load reflection overvoltage elimination. The key difference is the timescale of the produced voltage edge at the filter output.

In (Deisenroth and Trabert, 1993), a method using a narrow submodulation pulse in the IGBT gate drive control was proposed. The timescale of the control pulses is the same as in the ADUDT. However, their method failed to combine the voltage pulses with a suitable LC filter, instead suggesting the motor cable to be used as one component in the d*u*/d*t* reduction operation. The ADUDT combines the idea of controlling voltage pulses with an LC low-pass filter circuit at the inverter output, tuned to the voltage pulse pattern of the correct structure. A smooth transition in voltage edges could be produced. Here, the active control (the narrow submodulation pulse) effectively cancels the tendency of an LC circuit voltage to overshoot as a result of a low-damped resonance. The ADUDT method has been then studied by (Ström, 2009), (Ström et al., 2011), (Tyster et al., 2011), and (Korhonen et al., 2009). Figure 2.11 illustrates the basic idea behind the method.

Each time the original motor control is to change the voltage at any of the three phase legs, an additional subpulse in the phase leg output voltage is introduced. This subpulse has such a duration that with the corresponding LC output filter, a smooth voltage transition is produced. The LC circuit damping factor can be low, ideally approaching zero, translating into low losses in the filter itself. As the subpulse operation is responsible for canceling the resonant voltage overshoot in the filter, the pulse duration and the filter resonant frequency are coupled

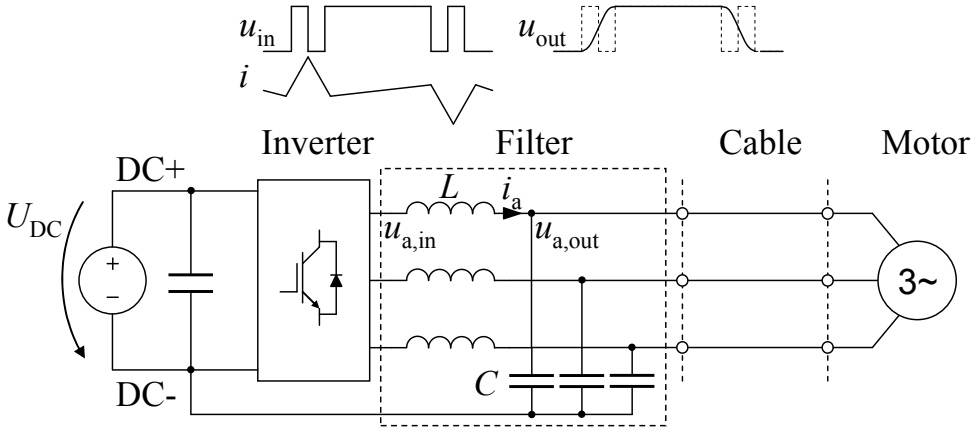


Figure 2.11. Basic arrangement of the ADUDT application. So far this filter topology has been the only one studied in ADUDT. Future studies could investigate the filter with capacitors connected between the phases. (Tyster et al., 2011), ©2011 IEEE.

parameters. This method has been analyzed and the working prototype results are shown in the above-mentioned publications. The work presented in this thesis is related to the previous work by increasing the available drive power from 5.5 kW to 22 kW (running 43 A phase current), while preserving the correct operation of the filtering, and thus, the overvoltage suppression. Previous control methods for the ADUDT did not allow the dead times to be placed flexibly in the pulse pattern. As the dead times can result in zero-current clamping (ZCC) to appear in the phase leg with the ADUDT, the ZCC causes error in the ADUDT control with previous control methods. With the new control method for the ADUDT, the ZCC can be directly compensated, and the placement of dead times does not need to cause any control error. We will now look into the details of prior art in the ADUDT technique, which will lead to the new analysis and an improved ADUDT control principle as given in this thesis.

The fundamental ADUDT working principle assumes a lossless and ideal phase leg/filter equivalent circuit as shown in Figure 2.12. The previous ADUDT control principle as presented in (Ström, 2009) is based on the assumption that no ZCC would appear in the phase leg during an ADUDT sequence. Output voltage delays are also omitted so that with the calculated ideal pulse pattern in Q_H and Q_L, the phase leg output voltage is assumed to be reproduced with no delay or waveform distortion. It must be noted that these assumptions were not made because of the lack of knowledge of what actually happens with real IGBT phase legs, but rather to give some starting point for the method. The new control method proposed in this thesis then adds the ability for ZCC compensation, and gives flexibility to the dead time insertion and pulse width limits. Further, expanding the timing error analysis is among the major contributions of this doctoral thesis.

The control principle of the filtering method can be found for instance in (Ström et al., 2011). It is founded on the basic properties of this LC circuit under pulsed input voltage operation.

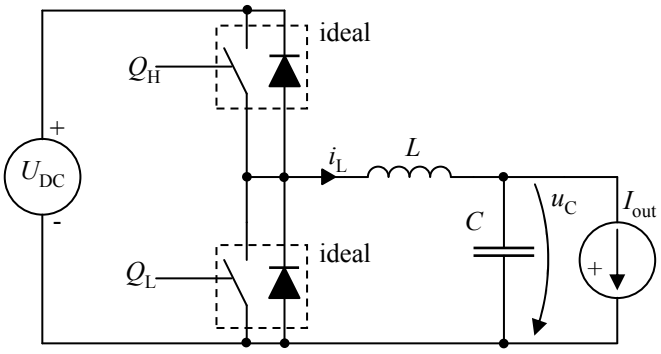


Figure 2.12. Low-pass LC output filter in active d*u*/d*t* operation, per each phase leg. This is the most basic ideal model for developing the ADUDT control principle.

The target of the idealized control is to achieve filter output voltage as shown in Figure 2.13.

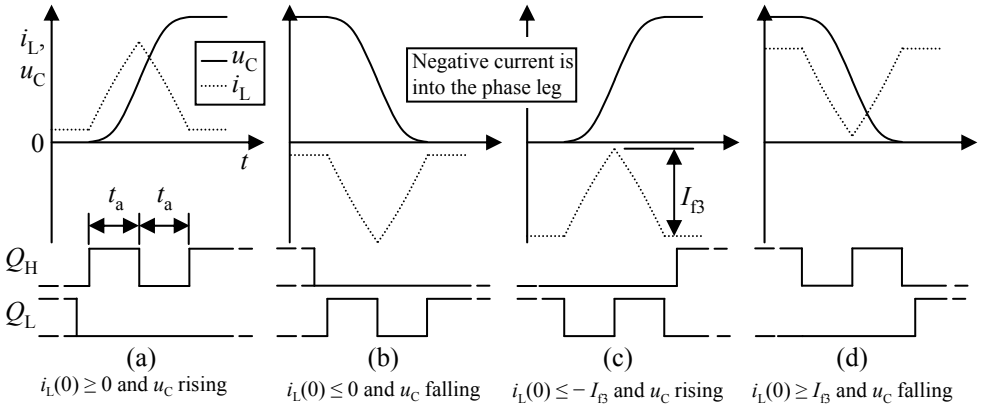


Figure 2.13. These are the four simplest cases of ADUDT control sequences, assuming idealized phase leg and filter circuits. For t_a, see Equation (2.10).

The charge pulse width t_a and the natural peak filter charge current I_{f3} are calculated as

$$t_a = \frac{\pi}{3}\sqrt{LC}, \tag{2.10}$$

$$I_{f3} = \frac{\sqrt{3}U_{DC}}{2\sqrt{\frac{L}{C}}}. \tag{2.11}$$

With this timing rule, the control pulse sequence in Figure 2.13 above is accomplished. The cases (a)–(d) in the figure can be called the ‘easy sequences’ to denote the fact that the filter

inductor current does not change direction. For each (a)–(d), these sequences require only one side IGBT to be used per sequence. In addition, the phase leg diodes participate in the control sequence. Easy sequences are valid when the filter L current i_L meets the condition as indicated. This can be known in advance as the instantaneous load current value I_{out} is known together with I_{f3}. U_{DC} and I_{out} are assumed to be constant during the control sequence. This is done on the basis that they have a considerably lower rate of change than the typical time frame of the ADUDT slope, thus effectively appearing as DC values during the control sequence. It is worth noting that i_L is the sum of the load current I_{out} and the filter charging current in the capacitor. This should be obvious from Figures 2.12 and 2.13.

If the conditions for easy sequences are not met, and thus, the load current/voltage transition direction combination leads to filter current zero-crossing, the control sequence is different. This is shown in Figure 2.14. They are referred to as 'hard' sequences, which only means that they always incorporate a control pulse 'B', used to bring the filter inductor current back to the load current value at the end of the pulse sequence.

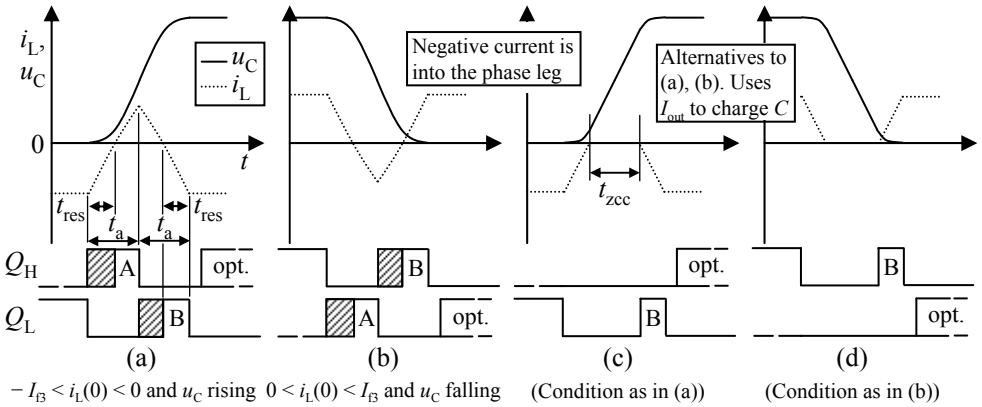


Figure 2.14. 'Hard' sequences involve i_L to cross zero. At the end of these sequences, a current correction pulse 'B' is used to equalize the filter state with load current to avoid resonance. 'A' and 'B' can occupy the shaded areas, respectively. Notice how pulse 'A' can be omitted by using an alternative method of load current to charge/discharge u_C. Equation for t_{res} is described later.

These 'hard' sequences can get more complicated when the excessive dead times cause zero-current clamping to appear. This is especially true for cases (a) and (b), which rely on both high-side and low-side IGBTs in the control, producing 'A' and 'B' pulses. Moreover, the nonideal timing and voltage edge behavior also affect the 'easy' sequences.

Continuing on the hard sequences, the prior art knowledge on the timing parameters was limited to the additional equation for t_{res}, first introduced in (Ström, 2009). It is equal to

$$t_{res} = \sqrt{LC}\arcsin\left(\left|\frac{I_{out}}{I_f}\right|\right)\Bigg|_{I_{out} \le I_{f3}} \tag{2.12}$$

As can be seen above, the actual required pulse width 'A' and 'B' can now be calculated, when t_{res} and t_a are known. There is an option to spread the pulses to the shaded areas in Figure 2.14. In ideal models, without having to worry about device timing deviations, it was convenient to use full-width pulses for 'A' and 'B', both having a duration of t_a.

There was no analytical solution to t_{ZCC}, if 'A' pulse omission was used. Trial-and-error parameter tuning in simulations showed that the method could work. Also in these preliminary studies it was found that a combination method [(a) with (c)] and [(b) with (d)], Figure 2.14, was possible, using 'A' pulse with t_{ZCC}, and of course still requiring 'B' pulse. It was observed that the zero current-clamp time t_{ZCC} could be divided into two parts, resulting in a combined sequence with the charge 'A', the zero-current clamp t_{ZCC}, and the correction 'B'. This combined sequence type is shown in Figure 2.15.

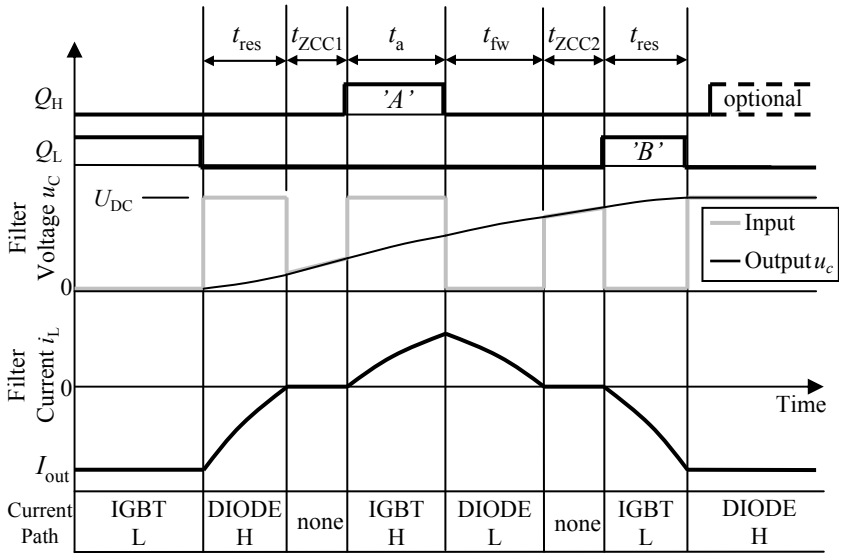


Figure 2.15. Combined ADUDT sequence. It is a general approach to 'hard' sequence, containing 'A' and 'B' pulses together with a floating-leg zero-current clamp (ZCC) part, which can be divided into two parts. The sum of the ZCC parts is t_{ZCC}. Setting t_{ZCC} to zero results in a 'hard' sequence (a), and omitting t_a results in a 'hard' sequence (c).

The value of $t_{ZCC1} + t_{ZCC2} = t_{ZCC}$ was not known in the previous studies. Further, the dependence of t_a and t_{fw} on the ZCC parts, U_{DC}, filter inductance/capacitance, and I_{out} did not have an analytical solution. Through trial-and-error, iteratively solved working examples for ideal power electronics models and a limited set of load current values were presented in (Korhonen, 2012). A summary of the prior art status of ADUDT control principle is:

- Sequence timing components t_a and t_{res} could be solved analytically.
- ADUDT tests with low I_{out} / I_{f3} ratios and no 'B' pulse were possible to show the method to work in principle.

- No opportunity to directly compensate for phase leg output voltage vs. gate drive control timing distortion and pulse width limitations.
- Sequences with a floating phase leg output could not be solved in an analytic form. Numerical solutions through iteration provided some results to show proof-of-concept.
- No analysis on how the (variable) shoot-through prevention deadtime interacts with the sequence, and how it is taken into account in pulse sequence formation.
- For the reasons above, no 'B' pulse was ever tried in the test setup. As the load current value reaches I_{f3}, the filter input voltage becomes 100% erroneous, causing near full doubling of the high-Q filter output voltage. To scale up motor rating, and keeping the filter and VFD current rating within a reasonable value, the ADUDT control had to be improved. Inclusion of the 'B' pulse was found to be necessary.

It is relatively straightforward to show the role of 'B' pulse in the ADUDT control pulse sequence when there are no timing distortions or dead times in the phase leg control. Figure 2.16 shows a simulated case of different load current values versus the characteristic filter peak current I_{f3}.

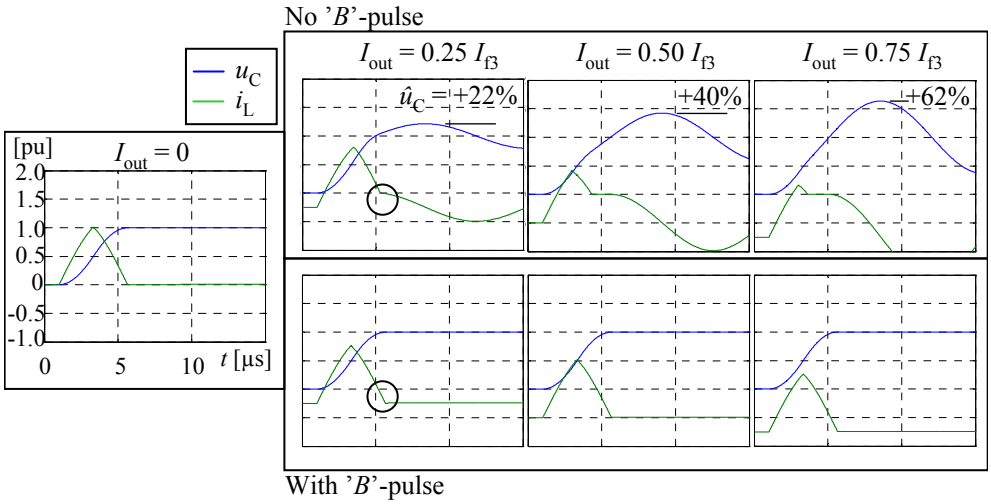


Figure 2.16. Role of 'B' pulse when the load current direction requires the use of a 'hard' sequence. This is an example of what happens if only 'A' pulse is used versus using 'A' + 'B'. The filter output voltage overshoot increases if 'B' is omitted with an increasing load current.

2.6.2 Other methods than ADUDT

The second category of active filtering methods is the reshaping of the IGBT gate drive signals, for instance with injected high-frequency submodulation or multistep voltage transitions. As the IGBTs are to be switched on and off by the control system, an additional circuit

or control block adds a burst of pulses or actively controls the transition of the gate voltage at the original gate drive signal edges. This submodulation of gate drive signal edges aims to shape the gate-emitter voltage of the IGBT resulting in longer turn-on and/or turn-off transients in the IGBT. This effectively emulates a controllable resistance in the gate circuit. Voltage transition rates in the order of 600 V/µs have been demonstrated applying gate voltage shaping techniques (Idir et al., 2006). Another type of direct edge shaping in the IGBT is the d*u*/d*t*/d*i*/d*t* clamp, providing power terminal feedback to gate during the commutation (Kagerbauer and Jahns, 2007). In these publications, the motivation has been the electromagnetic interference (EMI) reduction rather than the motor terminal overvoltage mitigation. Still, these methods can be seen as representing one type of active d*u*/d*t* filtering in a variable-speed AC drive.

A third category includes the resonant topologies built in the DC link. Voltage-source inverters with resonant DC link structures have been studied in (Choi and Sul, 1995b), (Kim and Sul, 1995), and (Kedarisetti and Mutschler, 2011). In order to achieve soft-switching operation to reduce switching losses, the circuit with a proper control principle yields inverter output voltage edges with a reduced d*u*/d*t* compared with basic hard-switching schemes. 600 V/µs d*u*/d*t* ratings have been published, with lower values attainable with component redimensioning and control retuning. This method will require more power electronic switching components in the main current path compared with a traditional hard-switching voltage-source inverter with a capacitor DC link. Furthermore, the active control of the resonant DC link has to be integrated into the original drive control system. The published results with efficiency measurements and d*u*/d*t* reduction are competitive with the performance seen with traditional passive filtering methods. This resonant DC link method could reach similar d*u*/d*t* values as the ADUDT (150 V/µs demonstrated in the ADUDT test setup), and should be included in future studies when comparing the output filtering methods.

Chapter 3

Power electronics nonidealities affecting the output filtering

Power electronics and specifically the IGBT timing nonlinearity effects have been widely studied in the past. Authors of IGBT technology such as (Baliga, 2008) were perfectly aware of the fact that the switching properties would carry inherent timing deviations compared with an 'ideal switch'. The analysis was based on semiconductor physics equations, not considering the phase leg as a whole. Among the earliest studies of timing-related phenomena were the dead time requirements and the motor voltage distortions in variable-speed AC drives. (Murai et al., 1987) discusses the the effect of blanking time between IGBT conduction periods, showing how the dead time is subject to minimization. A similar topic is discussed in (Leonhard et al., 1989) and (Dodson et al., 1990), achieving good results by using motor current feedback and compensation in the controller voltage reference. (Sepe and Lang, 1994) further elaborates the problem of the dead time in the motor drive applications, suggesting it to be minimized, but shows no model or results on how to characterize the output voltage timing. AC motor drive studies continue in (Choi and Sul, 1994), (Choi and Sul, 1995a), (Oh et al., 1995), with (Choi and Sul, 1996) again showing good results in reducing the AC output voltage distortion through current feedback. It is mentioned that very limited studies have been conducted on the actual voltage distortion characteristics of the IGBTs.

(Munoz and Lipo, 1999) demonstrates a compensation method that is based on voltage error measurements by characterizing the actual behavior of the drive output. This is already closer to the approach taken in this thesis. The approach, however, is for average voltage over several pulses, and does not cover the whole range of switches. This works for motor drive voltage compensation, but would require a more detailed model for an open-loop ADUDT application. Then, again, (Kim et al., 2001) refers to how difficult it is to reliably characterize the IGBT output nonlinearity.

However, a new approach is introduced in (Holtz and Quan, 2002), which already involves

phase leg characterization, combined with a switching component behavior model. The application is again for an AC motor drive, in the motor control itself. Still more recent studies for signal injection-based sensorless motor control applications emerged in (Guerrero et al., 2005), (Pellegrino et al., 2010), and (Salt et al., 2011). In this application, the accuracy of the output voltage is important, as it is used to generate an off-band signal for rotor saliency measurements, enabling enhanced performance in low-speed rotor angle estimation. These methods already use phase leg output voltage measurements to construct a compensation model for timing distortions. In this thesis, a similar procedure is conducted to characterize the phase leg and study the timing distortion effect on the ADUDT performance. At the same time, an improved control algorithm suitable for zero-current clamp periods is developed.

The idea of active du/dt output filtering is to provide means to control the VFD voltage rate of change before feeding the PWM voltage to a motor cable. The vast majority of industrial low-voltage three-phase VFDs use IGBTs and silicon diodes to produce the output voltage. Looking at the motor operation and the PWM pulse pattern at the inverter output, these power electronic components seem to do the job as ideal switches. After all, the fast switching edges of the components were the original reason for the need for an output filtering in the first place.

Nevertheless, IGBTs are not ideal switches. The inherent timing inaccuracy becomes more and more evident when zooming into timescale of microseconds and less. Looking at the actual switching between the nonconductive state and the conductive state, the voltage and current of the IGBT/diode component have characteristic deviation from an ideal switch. There is a delay before the component responds to the gate drive signal command changes. For a brief moment, gate capacitance is charged and discharged, making it possible for the IGBT to either conduct or stop conducting the collector current. On the submicrosecond timescale, this takes some time. Then, when the component finally responds to the control change, the change in the current through it and in the voltage across it will be gradual. A typical turn-on current slope time for modern 1200 V-blocking motor drive IGBTs is in the range of a few tens of nanoseconds to a few hundred nanoseconds.

Phase leg inductance plays a role in the current waveform inside the commutation loop. Also, the voltage across IGBTs changes according to the behavior of their internal capacitance (and any external capacitance in parallel). The IGBT also exhibits a rather long decay time of current in the turn-off, called the ‘tail current’. Initially in the turn-off, the current falls fast (with a similar slope time as the turn-on), but later, the current fall slows down. All this happens on a timescale of a microsecond. Furthermore, as the load current uses the freewheeling diodes from time to time as a conduction path, reversing the diode from a forward-biased (conducting) to a reverse-biased (blocking) state causes a momentary backflow to occur in the diode current. This process is the ‘reverse recovery’ of the diode. It manifests itself as a current spike through the phase leg, and its magnitude depends on the initial rate of change in current, the initial phase leg current prior to reverse recovery, and temperature.

From the viewpoint of an inductive load connected to the phase leg output, some details in the current waveform in the phase leg during the IGBT and diode turn-on and turn-off are masked. The load does not ‘see’ the reverse recovery current or the current tail. From the

load viewpoint, the phase leg is a voltage source, with a nonideal pulse waveform shape.

The phase leg is an output voltage 'wish box'. In this analysis, the phase leg comprises not only the IGBTs and freewheeling diodes, but the gate driver circuitry, bus bar inductance, and any deviation from ideal world that could affect the behavior of the output voltage at turn-on or turn-off. Logic-level gate drive signals are fed in for instance from a microcontroller, and eventually, we can observe a change in the phase leg output voltage. This voltage then starts to change the load current. In some cases the load current itself makes the phase leg output voltage to change. For inductive loads, this happens when the load current changes direction, and changes its path from one diode to the opposite. For active du/dt filtering, the phase leg output current can become zero for some time during the pulse pattern, causing a 'floating leg' period, in which case the phase leg output voltage follows the voltage of the filter capacitor. All in all, the 'wish box' is not giving us one-to-one voltage response to the gate drive signals. The nonideality is seen as a voltage edge delay and a noninstantaneous transit of voltage pulse edges. How nonideal it is, how it behaves in regard to the operating parameters such as current, voltage, and temperature, and most importantly, what does is mean when considering the active du/dt filtering control principle?

Some preliminary observations on what happens in the phase leg output on the timescale of typical ADUDT application is shown in Figure 3.1. The plot was captured from the prototype setup used throughout this thesis.

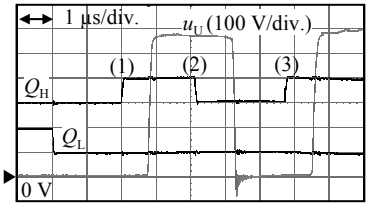


Figure 3.1. High-side and low-side IGBT logic-level gate drive signals (Q_H, Q_L, respectively) control the phase leg output voltage (u_U, relative to the DC bus). The control signal edges (1), (2), and (3), appear delayed in the output voltage, and there is some slope at the voltage edges.

Another example can be seen in Figure 3.2, where a precalculated control pulse pattern was used to control the output voltage of the phase leg, controlling an ADUDT filter output voltage. Everything worked fine in a simulation using ideal switches in place of IGBT/diodes, with no delays or other distortions. In the real setup however, the phase leg output voltage became distorted and apparently caused a noticeable resonant behavior in the filter output voltage, as it could not be controlled in the way it should have been.

Two examples how the combined overshoot error in the filter output voltage looks like in the test setup measurements is shown in Figure 3.3. The ADUDT method was working, but the filter output voltage always showed some amount of residual oscillation that was suspected to be the actual timing distortion and zero-current clamping (ZCC) effects of the phase leg output voltages.

Motivated by the observations of the suspected timing distortion effects, it became desirable

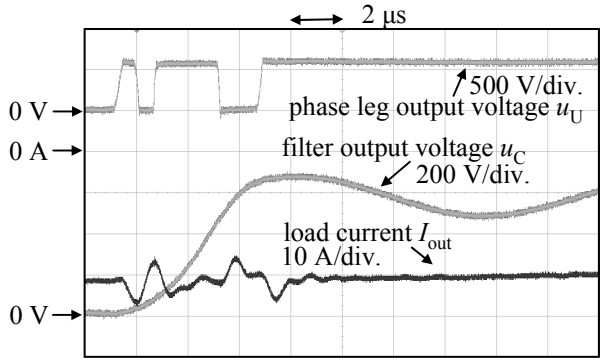


Figure 3.2. Although the gate control signals are not visible here, everything worked fine in the simulations, and the filter output voltage waveform had a smooth transition from zero to 600 V. In this waveform capture, taken from the test setup, something is not right and the filter output voltage has additional oscillation and overshoot. This is because the phase leg output voltage timing gets distorted in relation to the gate driver input signals.

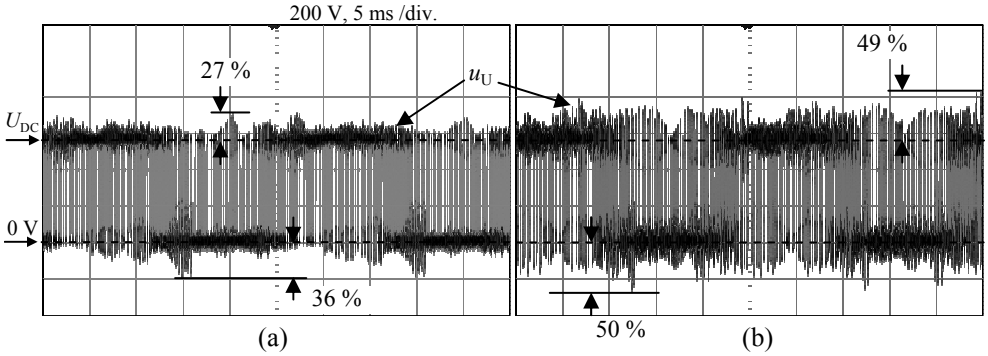


Figure 3.3. Motor test setup using the ADUDT, illustrating the filter output voltages observed during the test. Some amount of delay compensation is in use, removing the average rising and falling edge voltage delays at the phase leg output voltage. These waveforms show the timescale of the motor fundamental frequency. At each PWM pulse edge, the ADUDT is used, but inaccuracies in the control result in the filter output voltage to resonate and overshoot. (a) has a more accurate delay compensation than (b). Both are using the ADUDT algorithm with 1.3 µs minimum B-pulse limitation.

to further investigate the relation of the phase leg output voltage timing distortion effects on the ADUDT method. Closely related to the timing distortions of the IGBTs, the question of phase leg cross-conduction prevention during the pulse pattern also arose early in the test setup implementation. By using dead times in the logic-level gate drive signals, the IGBT cross-conduction shoot-through could be prevented, as is customary in any IGBT bridge application. However, this could lead to a case where the filter inductor goes to zero-current clamping during the ADUDT pulse sequence. During the time when neither the high-side nor the low-side IGBT conducts, the external load current affects the filter current and voltage in such a way that the theoretical solution for the ADUDT pulse pattern becomes more

complicated. The open questions in the ADUDT hardware implementation could thus be summarized as

- VFD output voltage timing distortions affect the performance of the ADUDT method, causing unwanted overshoot at the filter output voltage. Then, there are the ZCC effects that are due to excessive dead time values. How serious could these effects be, and what methods can be used to compensate for the effect? How does it affect the control principle of the filter (what needs to be done for the control pulse pattern)?
- If the pulse pattern cannot be made such that the filter inductor current becomes clamped at zero during the pattern, how has the control algorithm to be altered so that it is more flexible in regard to the pulse pattern structure, possibly helping with the dead time requirements and making it easier to implement the B-pulse required for current compensation in actual ADUDT applications.

The results of the timing distortion study are the timing map method for an IGBT phase leg, and the analysis of the shoot-through prevention in the ADUDT pulse pattern. Later in this thesis, the more advanced control algorithm for the ADUDT is presented, capable of flexible inclusion of variable-length dead times within the pattern. Ultimately, the timing data gathered from the test setup is combined with the new control algorithm in a phase leg simulation model to demonstrate a case study of how the timing distortions affect the ADUDT output voltage. The very same control algorithm is implemented to a test setup, and tests with motor load can be made.

3.1 IGBT phase leg output voltage timing

We start the analysis of phase leg timing distortions by looking into how the phase leg and the VFD is constructed, what kinds of nonideal and parasitic impedances there are in the circuit, and how the ADUDT filter, the motor cable, and the motor load connect and interact in the system. The task of the ADUDT filter is to reduce the motor cable input du/dt with the aid of an actively damped LC low-pass circuit. The simplified approach to the analysis of its operation, as used so far, is that the filter capacitor voltage is controlled per each motor control PWM pulse edge. The aim is to produce a piecewise continuous LC step response, without the natural tendency of the undamped LC circuit to overshoot. This is achieved by using control voltage pulses (micro pulses) from the inverter phase leg, and it is also known that the motor load current can be used to control the filter capacitor voltage in addition to the voltage pulses produced by the phase leg. The phase leg output voltage together with the motor load current control the state of the ADUDT filter. The filter inductor current and the capacitor voltage are the states of the filter. If the motor load current is changing relatively slowly, it can be considered as a constant current source during the ADUDT pulse sequence. This simplifies the operation analysis, as the load current change does not have to be considered during the ADUDT pulse sequence. The duration of an ADUDT pulse pattern,

and thus, the filter output voltage transition time between zero and the DC link voltage, is dimensioned according to the length of the motor cable. This dependency is

$$\ell_{\max} = K v_{\mathrm{p}} \tau_{\mathrm{f}} \tag{3.1}$$

where K is the empirical edge shape factor, arising from the cable reflection overvoltage properties of the active du/dt voltage edge shape, and having a value of $K = 0.32$. v_{p} is the EM wave propagation velocity in the motor cable, and $\tau_{\mathrm{f}} = \sqrt{L_{\mathrm{f}} C_{\mathrm{f}}}$ is the filter time constant. For the motor cable length of 100 m, and assuming a propagation velocity of $v_{\mathrm{p}} = 0.5$c, the desired filter time constant for the minimum reflection overvoltage is 2.08 µs. The shortest possible ADUDT transition time is $2\pi/3\tau_{\mathrm{f}}$, giving approximately 4 µs of time required for the filter output voltage to transit between zero and the DC link voltage. This sequence time will become longer if the IGBT dead times cause zero-current clamp periods to occur, typically adding a few microseconds in the pattern duration. Nevertheless, it can be seen that the duration of the ADUDT pulse sequence in a typical application is in the range of 4 µs to 15 µs for the cable lengths of 100 m to 300 m. If the motor load current does not change considerably during this period, it can be approximated as a constant current source.

We can now see the principle behind the ADUDT output voltage control. On the input side of the filter there is a pulsed voltage source (the phase leg), which can control the filter output voltage, and on the filter output side, the load current can affect the state of the filter. For each PWM pulse edge, the properly timed additional phase leg control pulses can be used to achieve an actively damped filter output voltage edge, such as shown in Figure 3.4.

It will be presented later in this thesis how the timing of the control pulses should be calculated. However, it is important to notice here that the timing and shape of the phase leg output voltage has a direct influence on the filter output voltage behavior. Of course, there are other real-life effects in the phase leg-filter-cable-load combination that make it deviate from the ideal model, and can result in an overshoot in the filter output voltage. In Figure 3.5 some of these nonideal characters are shown. First and foremost, these would be the inductance and resistance in the main current path, including the filter, and other matters that were simplified as explained above. But even if we now assume all these passive effects to be small enough to be neglected, the question remains how dramatic an influence the phase leg timing distortion has on the ADUDT performance. The timing errors can make the control difficult, since even though the desired pulse pattern is calculated, the actual implementation to a real-world drive would not result in the same pulse pattern at the phase leg output.

A major shortcoming of the simplified, ideal phase leg model is the fact that the real-world power electronic switching components such as the IGBT and diode do not follow the logic-level status command precisely. A phase leg constructed using these components will have some slope at the output voltage edges, and the switches turn on and off with a delay. Some part of this delay can be addressed to the gate driver circuit, and thus, the detailed switching operation of an IGBT is inherently with a delay. This gate drive signal chain is shown in Figure 3.6

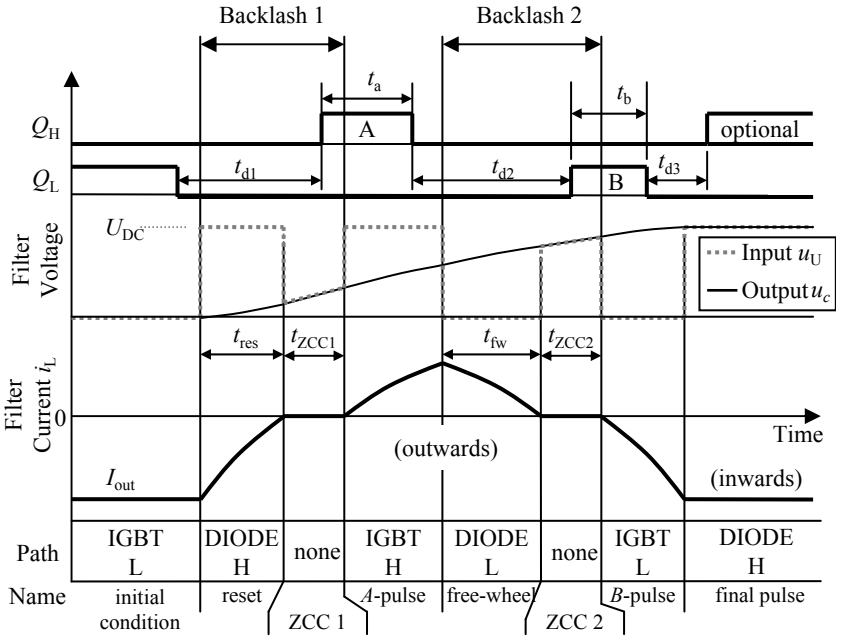


Figure 3.4. In general, any combination of active voltage pulses from the phase leg and the periods of only load current affecting the filter can be used to successfully change the filter output voltage level. Ultimately, the optimal filter output waveform is achieved with control pattern which has to take the timing distortions into account. Excessive dead times cause backlash in the leg control, which can lead to ZCC to appear.

When the logic-level gate drive control passes through the gate driver circuit, and eventually starts to change the status of the IGBT, the internal operation of the IGBT must be considered. This operation, together with the gate driver delay and the characteristic of the IGBT dependency on temperature, results in phase leg output voltage edges that are no longer exactly following the logic-level gate control signals. Figure 3.7 shows the IGBT waveforms during the switching transient in a phase leg driving an inductive load. The phase leg was shown above in Figure 3.5.

This figure is for a case when the phase leg current is commutated from the opposite-side freewheeling diode to the opposite-side IGBT in the turn-on process, that is, either from D_2 to S_1 or from D_1 to S_2 in Figure 4.1 but with actual devices. In the turn-off case, the current is commutated to the opposite-side diodes (S_1 to D_2 or from S_2 to D_1). Using the high-side switch as an example, the following steps in the turn-on process take place (this will produce a rising edge in the phase leg output voltage):

- The logic-level gate drive signal Q_H is changed by the control electronics. Some delay takes place before the gate driver circuit reacts and sets its output voltage to U_{G+}, and starts to change the IGBT gate-source voltage u_G. The initial reaction delay is not shown above, but at $t = 0$, the gate-source u_G starts to increase from U_{G-}. Before u_G

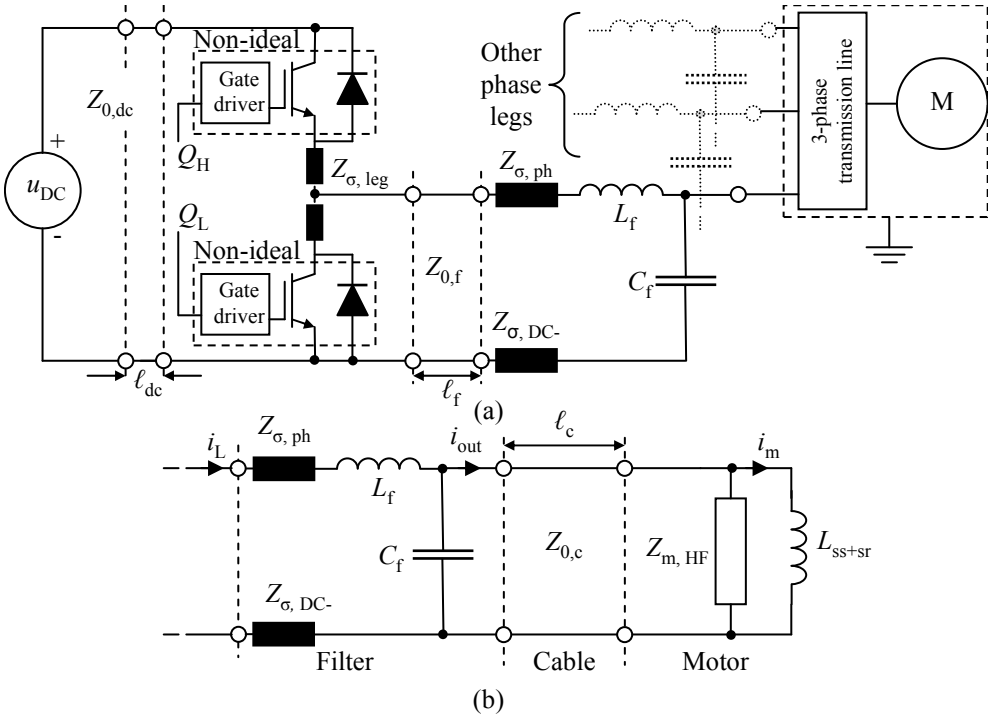


Figure 3.5. In the actual VFD IGBT phase leg, with an ADUDT filter, motor cable, and a load, there are several nonideal components and effects that were dismissed in the simplified model, and which can affect the ADUDT operation. Impedances Z_σ are any parasitic components in the circuit, and Z_0 are wiring transmission line characteristic impedances. These impedances also affect the phase leg voltage timing.

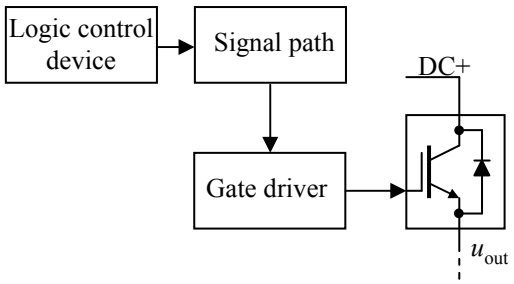


Figure 3.6. Signal chain from the control electronics to the phase leg output.

reaches the gate threshold voltage, there is no change in the IGBT collector current or the collector-emitter voltage.

- After $t_{d,on}$, u_G has reached the threshold voltage U_T. The gate voltage continues to increase, but now the IGBT reacts to the gate voltage and can start conducting current,

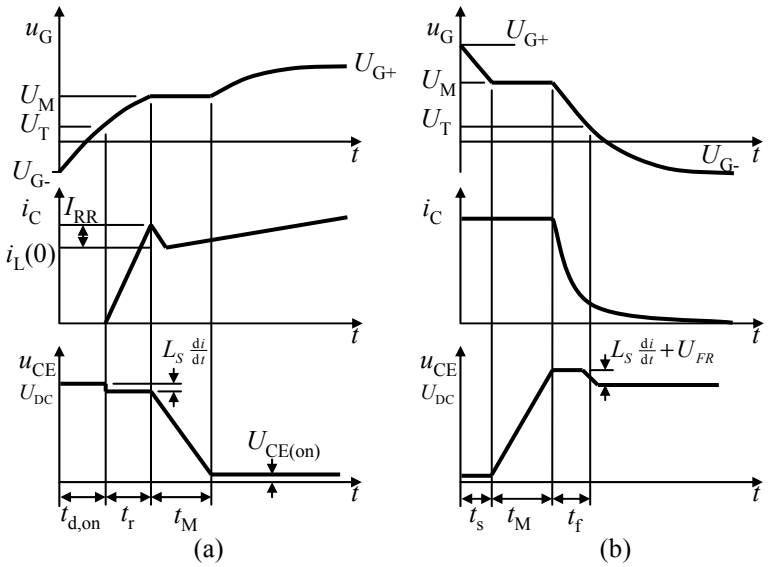


Figure 3.7. IGBT switching waveforms under inductive load. When this depicts the high-side IGBT, the phase leg output voltage is $u_{out} = U_{DC} - u_{CE}$. (a) is the turn-on, (b) is the turn-off.

where the current depends on the IGBT forward transconductance graph (Mohan et al., 2003). The current is commutated from the opposite-side diode, during the current rise time period t_r. If there is inductance L_s in the phase leg, it produces a voltage drop, which is visible during this current rising edge.

- The diode exhibits a reverse recovery phase (Lutz et al., 2011), causing a visible current overshoot I_{RR} in the IGBT collector current if there was current flowing in the diode prior to the IGBT state change. Now, the diode changes to reverse-biased state, and the IGBT u_{CE} can start to change. During this period, the gate-collector Miller capacitance is charged, clamping u_G to the Miller plateau voltage $U_M = U_T + i_C/g_{fs}$, where g_{fs} is the forward transconductance of the IGBT. During the Miller clamp period t_M, the phase leg output voltage edge is observed, with its exact shape dependent on the behavior of the Miller capacitance vs. the collector-emitter capacitance and the gate driver circuit performance (a simplified linear slope is shown here).

- After the Miller capacitance is charged, the u_{CE} voltage edge is completed and sets in the steady on-state saturation value of $U_{CE(on)}$ as the u_G continues to increase. The IGBT gate charge is increased until u_G slowly approaches the gate driver positive output voltage U_{G+}. The turn-on process is now completed.

The turn-off process is basically the same steps in reverse, where once again the gate voltage u_G defines the timing of the event turning points. Now, the phase leg is commutated from the high-side IGBT to the low-side diode, producing a falling edge in the leg output voltage:

- Again, the logic-level gate drive signal Q_H is changed by the control electronics. After a delay, the gate driver outputs U_{G-}, and u_G starts to decrease. Before u_G reaches the Miller plateau voltage U_M during the storage time t_s, there is no change in the IGBT collector current or the collector-emitter voltage.

- Reaching the Miller plateau, the gate voltage gets clamped to U_M voltage, and the Miller capacitance starts to discharge. Now, the voltage across the IGBT begins to rise as it gets pulled out from saturation. There is no change in the collector current during this period. The linear voltage ramp is a simplification; in reality the shape depends on the Miller capacitance and the gate driver current behavior.

- As the collector-emitter voltage continues to increase, the opposite-side diode exhibits a forward-recovery phase. This phenomenon is typical for power switching diodes, and depends on the semiconductor design. This causes a voltage overshoot U_{FR} in u_{CE} as the phase leg voltage must overcome the diode forward recovery before the diode conduction can take place. Now, the gate Miller clamp is released, and after the forward-recovery process in the diode, the current starts commutating to the diode. The current fall imposes an inductive voltage drop with the phase leg inductance, which is also summed with U_{FR}. This initial IGBT current fall time is t_f, which continues until the gate voltage reaches the threshold voltage level U_T.

- After the gate voltage has reached U_T, the IGBT u_{CE} settles to the DC link voltage level. The voltage edge is completed, but the IGBT current shows the slow 'tail' decay phase, slowly commutating the rest of the current to the opposite-side diode. The gate voltage continues to decrease towards U_{G-}.

The mechanism of the phase leg output voltage edge is rather straightforward to understand when the phase leg output current direction is either inwards or outwards, forced to flow already by the inductive load. The role of the high-side and low-side turn-on and turn-off, in terms of the output voltage edge polarity, is changed according to the current direction. This makes four possible switching scenarios to appear in the phase leg, all of which involve an active change in the IGBT gate command to cause an output voltage edge. Thus, for the current flowing into the phase leg, the low-side IGBT affects the output voltage edges, with a turn-on causing a falling voltage edge and a turn-off causing a rising voltage edge. For the current direction outwards, the high-side IGBT is important, with a turn-on causing a rising voltage edge and a turn-off causing a falling voltage edge.

With a zero output current, there are three possible cases. It is possible that both IGBTs are in the nonconducting state, and the load defines the voltage in the phase leg output. This is called the floating leg or the zero current clamped (ZCC) state. The leg output voltage can be anywhere between 0 and U_{DC}, set by the voltage appearing on the output side of the load inductor. In the ADUDT application, this voltage is defined by the filter capacitor, with no current flowing in the filter inductor. Now, the turn-on of either IGBT will define the output voltage edge. A high-side IGBT turn-on produces a rising voltage edge, but the edge starting voltage is the initial voltage at the leg output. Likewise, a low-side IGBT turn-on results in a falling voltage edge at the output, with the initial voltage set by the external source. These

are zero current turn-on incidents, with the output voltage edge observable depending on the initial leg output voltage.

The high-side IGBT can be in a conducting state with the phase leg output voltage equalling U_{DC}, and a zero output current. Likewise, the low-side IGBT can be in a conducting state with the phase leg output voltage equalling zero, and a zero output current. A direct turn-on of the opposite-side switch would lead to phase-leg cross-conduction. This kind of operation is not deemed practical or beneficial for the ADUDT application, and is not included in the study. On the other hand, if the IGBT of the initial turned-on status were first turned off, it would not affect the phase leg output voltage. Then, the leg would go to the ZCC state, after which a subsequent IGBT gate command change would be required to cause any phase leg output voltage edge. Thus, in these cases, a turn-off of the initial-state IGBT has no effect on the output voltage, and these cases are seen as having no significance for the ADUDT control. This leaves us with only one practical zero output current state in the study, and this is the ZCC state occurring after diode conduction.

In some cases, the IGBT in the phase leg is controlled to turn on, even though it will not affect the phase output voltage. This case will be discussed later with the concept of phase leg shoot-through prevention.

The objective of the timing distortion study is to investigate the timing distortion phenomena and their possible implications on the active du/dt control principle. Producing output voltage edges in an actual IGBT phase leg is investigated using the test setup.

3.2 Output voltage timing distortions

As shown in Figure 1.5, at this point of studies the functional control principle for the ADUDT filtering was already developed. It was done assuming an ideal phase leg and no parasitic effects in the circuit. The filter output voltage control worked in simulations, but the implementation in the test setup resulted in an erroneous output voltage edge shape, with overshoot, largely resulting from the timing distortions in the actual IGBT phase leg. Now, since the implementation in the test setup was the main technical task in the study project, the question arose of how to compensate for these timing distortions in order to obtain a filter operation approach that could be achieved in simulations using an ideal phase leg. It seemed that all the effort put on the control algorithm were in vain because of the lack of knowledge on how an actual phase leg behaved compared with the ideal model. The timing distortions were to be studied in the hope of building a model of them, and possibly compensating their effect in the ADUDT control. This compensation would work in conjunction with the ADUDT algorithm, to yield filter output voltages approaching their best possible shape.

Parameter variations in the control algorithm were observed to affect the extent of timing distortion effects in the output voltage overshoot. It was thus postulated that some compromise could be made between the accuracy of the phase leg timing delay compensation model

and the proper parameters for instance for the pulse-width limitations in the ADUDT pulse sequence to get a filter output that would be satisfactory within some limits. It was not yet known whether the behavior of the timing distortions could be modeled accurately enough to give a practical compensation method. At this point, the scope of the study was limited to

- Study the behavior of the phase leg output voltage timing distortion, in a case study manner using the test setup as a platform. The results should describe how the timing distortions behave in this particular case, and whether there are some general rules on how it might apply to other hardware cases.
- Study the effect of the phase leg output voltage timing distortions in this particular hardware case. Again, it would be desirable to draw some conclusions on how the timing distortion affects the ADUDT in general, and what could be proposed as a compensation strategy against their effect. Furthermore, if the distortion model is inevitably incomplete, and some role could be achieved in the effect minimization through control algorithm parameter variations, what would be the 'good enough' solution for practical applications?

The research question concentrates on the case study, using this test setup hardware as a platform to investigate the typical effects seen in an industrial low-voltage VFD. Many different types of timing distortion effects were found, and in each type, the underlying reason based on the circuit and semiconductor operation theory was investigated.

In principle, studying the actual IGBT phase leg dynamic characteristics could be possible with analytical and simulation modeling tools, opposed to direct measurements and characterization from the test setup. This could be done with a dynamically accurate IGBT model such as the Hefner model (Hefner and Diebolt, 1994), available for instance in PSPICE and Saber software. An alternative is to use a simpler behavioral model based on equations describing the IGBT/diode dynamics, derived from the physical semiconductor equations as in (Lauritzen et al., 2001). The IGBT phase leg could be constructed in the simulation software, together with the most important parasitics in the circuit. The gate driver circuit can be simulated either directly or with a simplified step voltage source, with effective delays gained from gate driver input/output measurements or values provided by the manufacturer. This would give a model for the phase leg 'wish box', suitable for simulating the timing distortions.

However, it was seen that there could be a problem in identifying the parasitics in the circuit, and getting a model for the IGBT/diode module such that the results would reflect the test setup case. This simulation-based approach could prove a good method for investigating the general timing distortion effects in future studies, but the method used in this thesis is more straightforward. The approach uses direct measurement of the experimental setup inverter output voltage. The idea is to collect timing data so that a timing distortion model of the test setup VFD could be constructed. As a result, the distortion model can be considered valid only for this particular setup case, but if the underlying reasons for the timing distortion effects are investigated at the same time, then perhaps some conclusions could be drawn based on the results. The results are not compared with any specific analytical/simulation tool method, but rather, they present a possible way to characterize the inverter output timing

distortion. The arrangement of the measuring setup used to study the phase leg output voltage timing distortion, is shown in Figure 3.8.

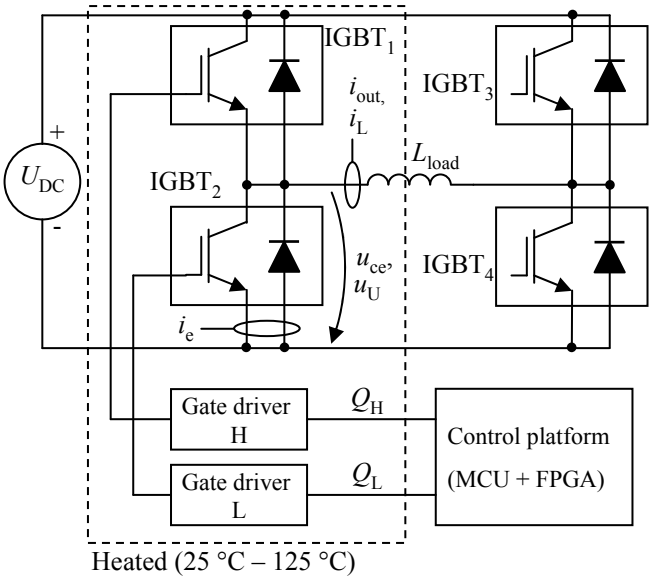


Figure 3.8. Setup for phase leg output timing measurements.

The timing distortion study involves two phase legs of the three-phase test setup VFD. It is based on the Vacon NXP-FR6 electronics, with IGBT modules of SEMIKRON SKM100GB123D. The gate driver electronics and the IGBT bridges were left as they are in the standard product. A heater was added to the heat sink element to study the temperature variation effects on the timing distortion. Two temperature settings were tested; the IGBT modules/gate drivers at 25 °C / 25 °C, and 125 °C / 80 °C (all temperatures within $\pm$5°C). The DC link voltage U_{DC} was 600 V nominal, with variations included in the study. At the phase leg output, a load inductance was connected to provide behavior resembling an inductive current source at the phase leg output. This is based on the fact that the ADUDT filter itself can be considered an inductive load. The load inductance L_{load} was approx. 45 µH nominal, constructed of double Ferroxcube E80-3F3 ferrite core with an air gap, and having very linear inductance up to peak current of 170 A, when configured as a 45 µH inductance. The inductance could be changed by adjusting the core air gap and the winding turns. The control platform, which is the motor control application equipped with an ADUDT modulator, is able to produce gate control pulses in a 10 ns resolution, with a 10 ns timing accuracy. For the timing distortion studies, the control software is configured such that it produces repetitive ADUDT pulse sequences, with a full control over the repetition rate and the pulse pattern shape. The generated logic-level ADUDT pulse sequence fed to gate drivers is shown in Figure 3.9.

The typical pattern repetition rate was 10 patterns/second. This means that the distortion tests were performed as pulse tests, with RMS current flowing in the phase leg or load. The

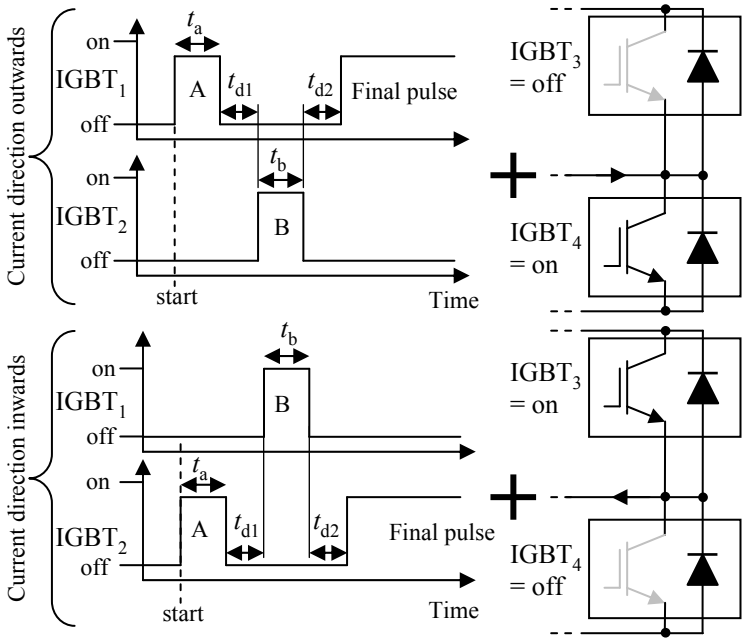


Figure 3.9. Output timing measurement gate driver waveforms.

instantaneous current during the test pattern could then exceed the thermal rating of the electronics, making it possible to use a light-weight construction of the load inductor and wiring, and requiring no signicant power from the supply. Test pulse current was supplied by the DC link capacitors, and an additional capacitance was added should the DC link voltage drop significantly during the test pulse.

The first test pulse in the sequence charges the load inductance to a test value, and then, after a desired dead time t_{d1}, the opposite side IGBT is commanded to turn on. After the second dead time t_{d2}, the original-pulse IGBT is commanded to turn on again. Since these represent the digital controller-level gate command pulses, it is generally unknown when the actual turn-on and turn-off instances take place in the phase leg, and what actually happens to the phase leg output voltage. This is exactly the idea of the test; to determine a figure for the output voltage delay as compared with the control signal status change. The lower IGBT emitter current i_e is monitored with a current probe, as is the phase leg output current. The DC link in the phase leg is constructed of copper bus bars, and an additional loop had to be opened in the emitter connetion to accomodate the current probe. This is suspected to increase the emitter inductance in such a way that it could affect the delay measurement results, as will be later discussed. The emitter current measurement could be used for phase leg shoot-through and diode reverse recovery observations, which is an important subject in the study since the typical ADUDT pulse sequence involves the use of both the high-side and low-side IGBTs, and the diodes will change between the forward-biased and reverse-biased states. The phase leg output voltage u_{out} gives the output current waveform, and it is measured with a differential voltage probe. The models of equipment used in the tests were

- Agilent N2781 current probe, combination of a Hall sensor and a current transformer, rated 150 A RMS, 10 MHz, 1% base accuracy at nominal current, at 50 Hz.
- Tektronix P5205A differential voltage probe, rated 1300 V max., 100 MHz.
- Agilent MSOX3054A oscilloscope with digital channels for monitoring the logic-level gate drive signals.
- Fluke 8840A benchtop multimeter for DC link voltage and heat sink temperature monitoring.

The method for defining the output voltage edge delay is shown in Figure 3.10. It was previously published in (Tyster et al., 2013), and uses the inspiration from previous studies by (Allard et al., 1998). The oscilloscope integration function is used to give the output voltage integral, which is basically the same signal as the load current flowing in the load inductor, assuming ideal inductance in the output. This signal represents the effective 'idealized' load inductor flux linkage generated by the output voltage change. Now, the steady-state asymptote of the slope in the voltage integral intersects the initial value horizontal level, and the effective output voltage edge delay is found at that intersection, when measured from the logic-level control signal change that caused that output change to be triggered. This gives the 'virtual output voltage delay', and conveniently combines all the internal delay and slope shape effects in the phase leg. It gives a result that could later be used for instance in an ideal phase leg simulation model, with a virtual delay in the switch command to simulate the behavior of the real phase leg.

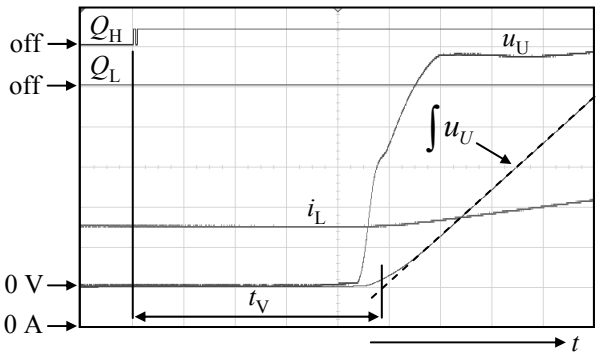


Figure 3.10. Method of determining the output voltage delay.

Not all output voltage changes are attributed to the changes in the IGBT gate drive command changes, however. If the output current crosses zero, and perhaps becomes clamped at the zero level, then the IGBTs play no role in the output voltage value, and the operation of the diodes under the output current change defines the output voltage. Still, the output voltage can be measured in the same manner as with IGBT command changes, but there is no reference logic-level command with which to compare the output voltage edge. This will be discussed later.

IGBT module datasheets also give timing data based on the collector current measurements. The definition of these delay times are shown in Figure 3.11. It shows an example for a high-side IGBT, but the same process applies also to the low-side IGBT.

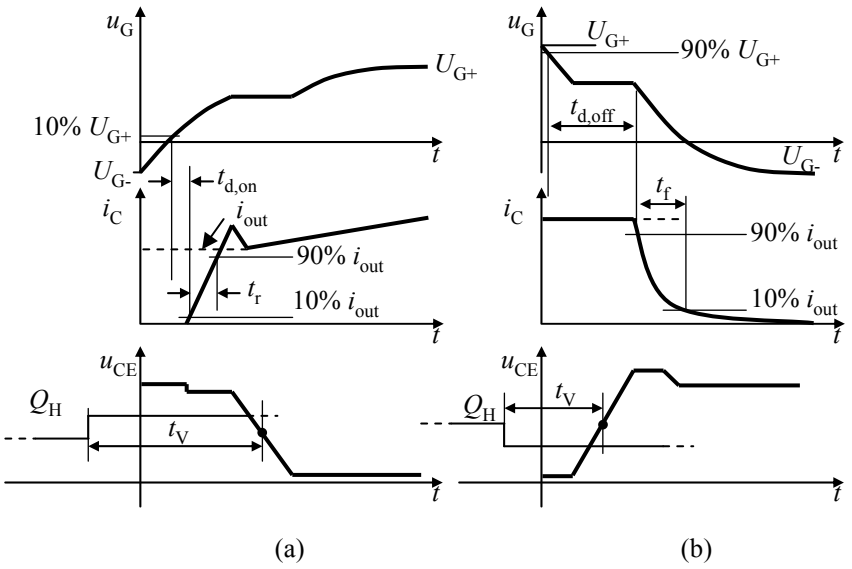


Figure 3.11. Standard (IEC, 2007) defines the measurement method for the datasheet values $t_{d,on}$, t_r, $t_{d,off}$, and t_f. The load connected to the phase leg output, however, experiences input voltage edges that are not directly related to the datasheet delay values. This logic-level gate drive signal to the output voltage virtual edge delay is t_V, and is in the focus of this thesis. 'Virtual' voltage edge means that the output voltage edge shape is idealized as described above.

It can be seen that the phase leg output voltage is what drives the load connected to the output, causing load current changes in the case of an actual load such as the ADUDT LC filter. The current flowing in the phase leg during the switching operations has a different waveform than the load current. The phase leg current is not directly observable in the load current. The load experiences the output voltage changes.

The pulse sequence contains both phase leg state changes (output voltage changes from U_{DC} to 0 and 0 to U_{DC}), and programmable dead times between the high-side and low-side IGBT gate commands. The initial load current direction can be selected to be either inwards or outwards from the phase leg, and this current magnitude is varied by changing the pulse width t_a.

The phase leg state / current direction combinations appear in Figure 3.12 and are termed as follows:

- Scenario I: Load current direction inwards to the phase leg, and the phase leg state change from 'down' to 'up'. Shoot-through prevention with the dead time t_{d1}.

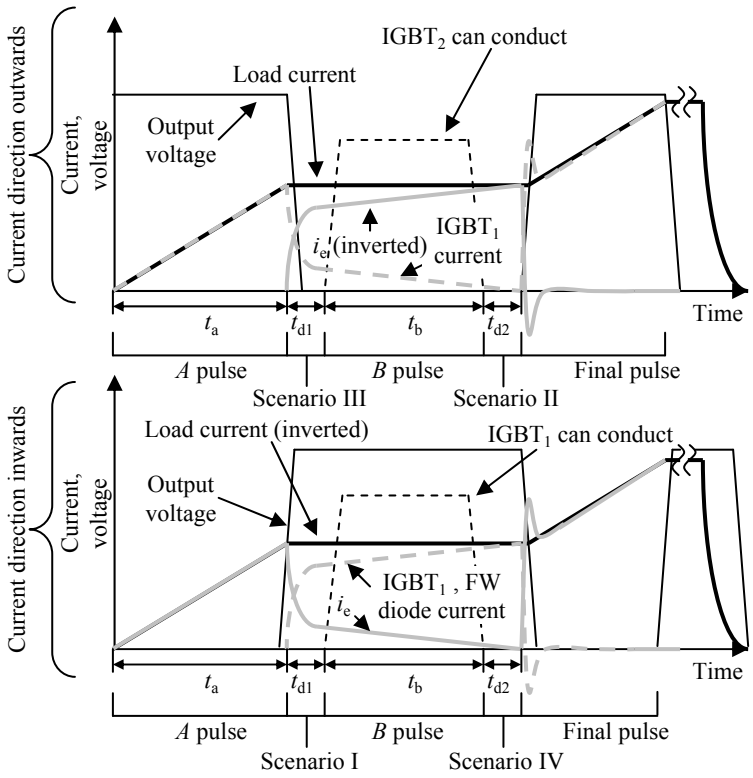


Figure 3.12. Terminology applied to sequential Q_H and Q_L state changes in the phase leg. These are also the situations where a dead time might be required if there is a risk of overlapping conduction periods of the IGBTs. The Roman numerals I to IV indicate four possible state change/current direction scenarios.

- Scenario II: Load current direction outwards from the phase leg, and the state change from 'down' to 'up'. Shoot-through prevention with the dead time t_{d2}. The reverse recovery current of the low-side diode is also observed during the state change.
- Scenario III: Load current direction outwards, the state change from 'up' to 'down'. Shoot-through prevention with the dead time t_{d1}.
- Scenario IV: Load current direction inwards, the state change from 'up' to 'down'. Shoot-through prevention with the dead time t_{d2}. The reverse recovery current of the high-side diode is also observed during the state change.

3.2.1 Effects of load current, module temperature, and DC link voltage

The first test was to investigate the dependency of the phase leg output voltage timing on the load current and the IGBT/diode module temperature. In normal ADUDT operation, the mo-

tor load current makes a full cycle, superimposed with the filter charging current waveform, which is then the current seen in the ADUDT filter inductor (current i_L). This means that the phase leg current varies during the filter operation, and there could be a dependency between the phase leg current and the output voltage edge timing. The IGBT module temperature can also be a source of timing distortion, if the delays are a function of temperature. Further, the DC link voltage U_{DC} varies during the VFD operation.

Applying the measurement method described above, the results for the load current and the IGBT module temperature are shown in Figure 3.13. The test pulse duration was set sufficiently long so that the gate voltage was able to reach the steady-state value in order to remove the possibility of storage-time deviations affecting the turn-off delay.

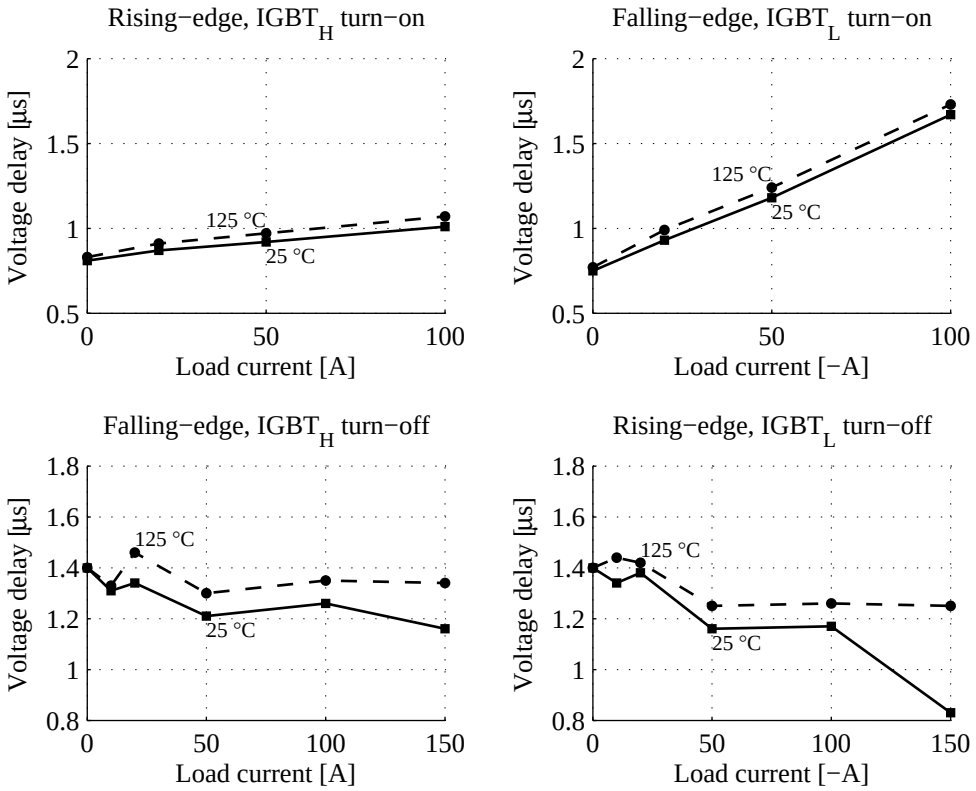


Figure 3.13. Output voltage delays (as t_V in Figure 3.10) as a function of initial load current and IGBT module temperature. Negative current direction is towards the phase leg center point. There is some challenge in defining the zero-current turn-off event.

The behavior of the voltage edge delay needs more analysis when the load current approaches zero and the turn-off is affecting the edge (lower row above). When the load current is zero, then neither of the IGBTs' turn-off defines the output voltage edge timing. The lowest current magnitude used in the turn-off timing tests was 10 A in/out. We may consider what happens to the voltage edge if the current amplitude goes even beyond zero, to the left side in Figure

3.13. Having the load current polarity changed, it means that the IGBTs in each pane no longer define the corresponding voltage edge:

- With the load current direction into the phase leg, the high-side IGBT no longer defines the edges of the phase leg output voltage. Only the low-side IGBT is capable of affecting the output voltage edges.
- With the load current direction out from the phase leg, the low-side IGBT no longer defines the edges of the phase leg output voltage. Only the high-side IGBT is capable of affecting the output voltage edges.

This means that when the output current direction is reversed, the roles of the IGBTs in the output voltage edge generation are also reversed. In this case, from the viewpoint of the voltage edge, the fact that the IGBT is not capable of altering the output voltage is not important in the analysis. Still, the question remains: what happens to the output voltage edge delay when the load current magnitude approaches zero at the turn-off. At this point, we assume the zero-current turn-off voltage delay to equal the 10 A current magnitude delay value, and return later to the zero-current turn-off subject.

It is interesting to observe the characteristics of the delay behavior, even with visual inspection. All delay graphs show a considerable amount of average baseline delay. This baseline delay seems to be quite similar between the high-side and low-side IGBT switching processes, per turn-on and turn-off, respectively (compare the left and right rows in the figure above). There seems to be approximately 0.8 µs baseline delay in turn-on-related events. The turn-off events show more complicated behavior, with a significant deviation in the -150 A $\mathrm{IGBT_L}$ turn-off compared with the 150 A $\mathrm{IGBT_H}$ turn-off. This deviation is not present in the 125 °C results, and thus, a bad measurement for 25 °C at -150 A is suspected. Overall, the voltage edge delays seem to increase as the IGBT module temperature is increased.

The $\mathrm{IGBT_L}$ turn-on is significantly more dependent on the load current value than the $\mathrm{IGBT_H}$ is. One possible explanation for this phenomenon is the location of the emitter current measurement probe at the low-side IGBT, possibly increasing the inductance in such a way that the current di/dt is reduced during turn-on (see Figure 3.7), delaying the beginning of the Miller plateau and thus creating a load current-dependent turn-on voltage edge delay. All in all, the voltage edge delay values seem to be mostly constant as a function of load current, with a relatively small dependency on the current value except for the $\mathrm{IGBT_L}$ turn-on process.

The effect of load current di/dt during the switching process was also investigated. The hypothesis is that the load current rate of change during the switching process may affect the voltage edge delay. This was seen important as the load inductance had to be varied during the previous tests, and if the load current di/dt had a significant effect on the voltage edge delay, this effect would have to be reduced from the delay values. Because the DC link voltage had to be varied during the test, and in theory the Miller clamp process is IGBT voltage dependent, it was also important to investigate the DC link voltage effect on the voltage edge delay. A linear regression model for the U_{DC} effect was made, and the U_{DC} variation effect reduced from the di/dt results. The U_{DC}-corrected results for the di/dt tests, together with the

U_{DC} dependency test results, are shown in Figure 3.14. The test was made by varying the load inductance and U_{DC} in such a way that different load di/dt were achieved. The test was repeated for two peak load current values.

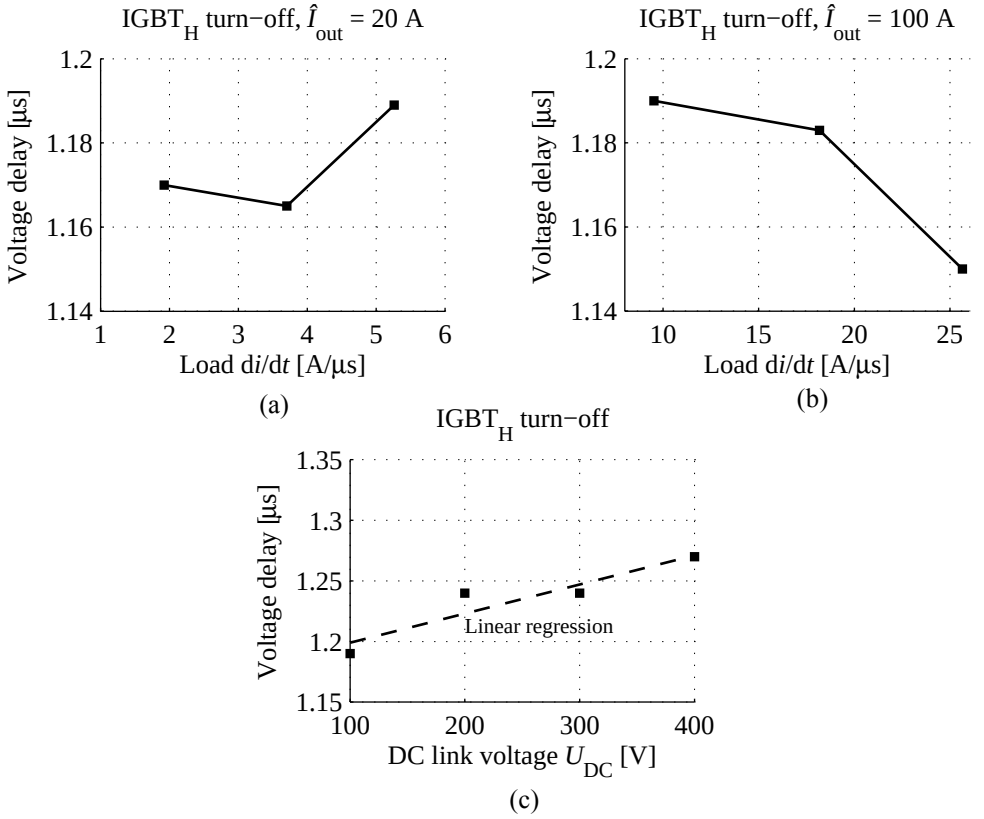


Figure 3.14. Effect of load di/dt and DC link voltage during the switching process.

The tests were made at 25 °C temperature. We first analyzed the effect of U_{DC} variation in the voltage delay results. Linear regression $t_{\mathrm{V,UDC}}$ for the U_{DC} results is

$$t_{\mathrm{V,UDC}} = \left(1.175 + 2.4 \times 10^{-4} \frac{U_{\mathrm{DC}}}{[\mathrm{V}]}\right) \mathrm{s} \tag{3.2}$$

The U_{DC} values used in the di/dt tests ranged from 30 V to 73 V for the 20 A peak load current, and 140 V to 356 V for the 100 A peak load current. The linear regression model for U_{DC} effect suggests the following:

- For the 20 A peak load current tests, a +0.9% increase in the delay results is expected when di/dt is changed from the lower test value to the upper one. This is due to U_{DC} increasing from 30 V to 73 V.

- Likewise, for the 100 A peak load current tests, a +4.2% increase in the delay results is expected, the U_{DC} increasing from 140 V to 356 V.

Using the U_{DC} model, the di/dt effect measurement results were corrected such that the U_{DC} variation would not be visible in the results. The following observations were made:

- For the 20 A peak load current, the average timing delay is 1.175 µs, with a (population) standard deviation of 10 ns, with the di/dt values 1.923 A/µs, 3.704 A/µs, and 5.263 A/µs.
- For the 100 A peak load current, the average timing delay is 1.174 µs, with a (population) standard deviation of 17 ns, with the di/dt values 9.524 A/µs, 18.182 A/µs, and 25.641 A/µs.

The standard deviation of the results is less than 2% of the average timing delay. The standard deviation is close to the hardware ADUDT controller pulse resolution of 10 ns. It is unlikely that the load current di/dt has a significant effect on the output voltage edge timing.

According to the U_{DC} effect test, the variation of the DC link voltage can affect the output voltage edge timing. If U_{DC} is varied between 486 V and 594 V, the voltage edge timing changes from 1.292 µs to 1.318 µs, that is, by +2%. The difference in timing is in the order of 10 ns, which is the pulse resolution of the ADUDT controller hardware in the test setup.

3.2.2 Effect of pulse width on the timing delay

A phenomenon was observed when the turn-off delay events were studied in the phase leg. When the load current effect on the turn-off voltage delay was measured, it was noticed that the width of the measurement pulse had an effect on the pulse turn-off (a falling voltage edge with $IGBT_H$, a rising voltage edge with $IGBT_L$). The results obtained by decreasing the pulse width while keeping the turn-off current constant are illustrated in Figure 3.15(a). A similar test was repeated by decreasing the logic-level gate drive command Q_H in (b), and observing the linearity of the load current change.

It is clearly seen from the graph in Figure 3.15(a) that a decrease in the pulse conduction time makes the falling edge voltage delay smaller. The initial current before the test pulse was always zero in these tests. The 50 A test current shows some average decrease in the delay, a result which can be expected based on the previous load current tests. Nevertheless, the dependency of the turn-off process on the pulse width needs to be explained. A similar result with a different measurement method is shown in Figure 3.15(b), where the decrease in the gate command pulse width produces a nonlinear decrease in the load inductor current graph. It seems that with the logic-level gate command pulse width decreasing below approx. 2 µs, the output pulse width does no longer decrease linearly. Since the rising edge delay

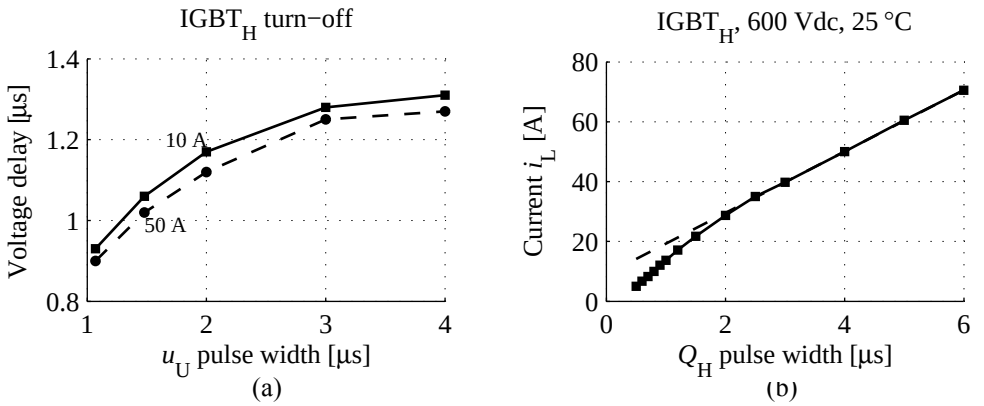


Figure 3.15. Narrow positive pulse behavior. In (a), the positive output voltage pulse is produced with $IGBT_H$ and a turn-off load current having constant values of 10 A or 50 A. This was achieved by using a variable load inductance. In (b), the load inductance is constant, and the gate command width is varied, producing similar results as in (a).

is constant, and the inductor was verified to be linear in the measurement current range, the reason must be the falling voltage edge delay.

Another example of the narrow pulse turn-off effect is shown in Figure 3.16(a). Here, an output voltage pulse width of approx. 0.5 µs was tested, with a zero initial load current. The load current at the falling edge is 10 A, and the falling edge delay is 0.7 µs, a value significantly lower than could be expected based on the load current value only.

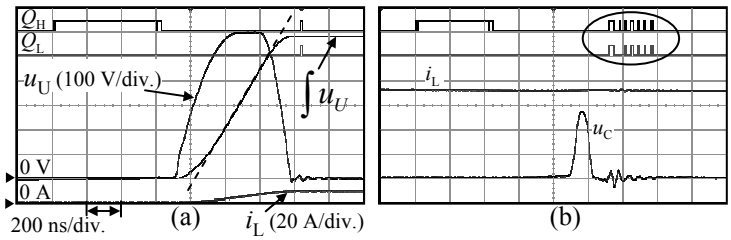


Figure 3.16. In (a), the falling edge delay is 700 ns, which is rather small compared with the long pulse falling-edge delay value at the 10 A load current. (b) is to demonstrate how the pulse behaved when the initial load current was increased, and the gate command pulse width reduced further. The phase leg still produces a runt voltage pulse, and there is electromagnetic interference visible in the gate drive command signal conductors (circled area).

This turn-off behavior introduces a challenge into the timing distortion modeling. It is probably not feasible to repeat all turn-off process voltage delay measurements with the pulse width as a parameter. Rather, the underlying physical reason in the IGBT operation was investigated so that the turn-off process could be modeled with a separate behavioral model. Let us consider the shape of the IGBT switching waveforms as shown in Figure 3.7. The progression of the gate voltage is then

- At turn-on, the voltage edge is produced while the gate voltage is in the Miller plateau. The gate voltage is constant during this period.
- After the turn-on voltage edge is completed, the Miller clamp is released and the gate voltage starts to increase again towards the U_{G+} voltage. The gate charge increases.
- At some point, the turn-off process is initiated. After the initial gate driver delay, the gate drive sets its output voltage to U_{G-}, and the gate voltage/charge starts to decrease. It decreases until it hits the turn-off Miller plateau. The time required before the plateau is reached is the storage time t_s.
- As the storage time has passed, and the turn-off Miller plateau has been reached, the output voltage edge is generated during the Miller clamp period.
- After the output voltage edge is completed, the IGBT current can start to decrease. The IGBT gradually turns off.

Now, the pulse width during IGBT conduction dictates whether the gate voltage u_G will reach the steady-state value of U_{G+} or, if the pulse is sufficiently narrow, the u_G will remain at some lower value. With long pulses, u_G is always charged to U_{G+}, maximizing the subsequent storage time t_s at turn-off, resulting in a maximum turn-off delay. This gives the largest possible value for the voltage edge delay at turn-off, the results that were gained in the load current voltage delay tests. But with short gate drive pulses such that u_G is not able to reach U_{G+}, the storage time t_s is decreased. The turn-off process becomes a function of gate drive pulse width. It is now possible to construct a mathematical model for the turn-off edge delay as a function of pulse width and switch process parameters. The steps in the gate charge analysis are shown in Figure 3.17.

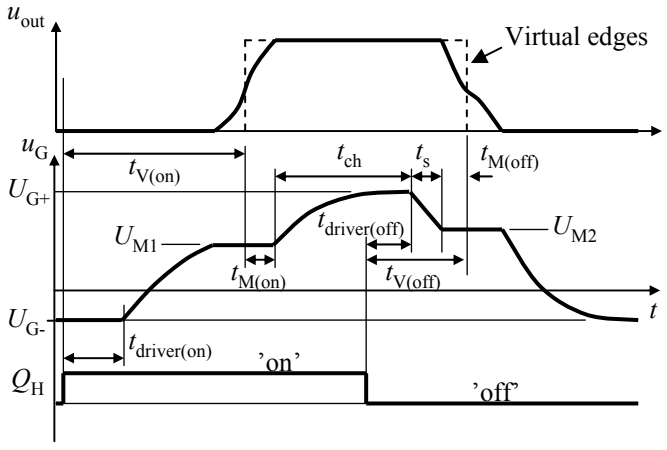


Figure 3.17. Progression of the gate voltage in the switching process. After the turn-on Miller plateau, the gate continues to be charged by the gate driver during t_{ch}. The gate discharging period is t_s, and since the starting charge is dependent on t_{ch}, the start of the turn-off Miller plateau becomes a function of pulse width. $t_{V(on)}$ and $t_{V(off)}$ are the t_d virtual delays as in Figure 3.10.

During t_{ch} and t_{s}, the gate capacitance is constant since the voltage across the IGBT is constant (Mohan et al., 2003). Assuming a constant gate resistance during these periods, the gate has a fixed RC time constant τ_{gate}. According to (Lutz et al., 2011), the Miller plateau voltages U_{M1} and U_{M2} are a function of collector current

$$\begin{aligned} U_{\mathrm{M1}} &= U_{\mathrm{T}} + \frac{i_{\mathrm{c(on)}}}{g_{\mathrm{fs}}} \\ U_{\mathrm{M2}} &= U_{\mathrm{T}} + \frac{i_{\mathrm{c(off)}}}{g_{\mathrm{fs}}} \end{aligned} \tag{3.3}$$

where U_{T} is the IGBT gate threshold voltage, g_{fs} is the IGBT forward transconductance, and $i_{\mathrm{c(on)}}$ and $i_{\mathrm{c(off)}}$ are the collector current at either the turn-on or turn-off Miller plateau, respectively. It is assumed that the load current value can be used as a collector current value in calculating the U_{M} values.

In this model, it is assumed that the starting point of the t_{ch} period can be defined using the virtual voltage edge as a landmark, and then adding some fraction of the Miller plateau duration $t_{\mathrm{M(on)}}$ before starting t_{ch}. The same principle is applied at the turn-off, with the virtual voltage edge assumed to appear at some point during the Miller plateau, with a delay $t_{\mathrm{M(off)}}$ after the t_{s} period. The value for $t_{\mathrm{M(on)}}$ and $t_{\mathrm{M(off)}}$ requires knowledge of the Miller plateau durations and shape, since they will affect the location of the virtual output voltage edges. Several turn-on and turn-off processes were measured in order to determine a viable, simple value for the Miller plateau delays:

- For the load current values of 0 A, 20 A, 50 A, 100 A, and 150 A, $t_{\mathrm{M(off)}}$ was measured for turn-off. Both $\mathrm{IGBT_H}$ and $\mathrm{IGBT_L}$ processes were used. The average of $t_{\mathrm{M(off)}}$ was 138 ns, with a standard deviation of 21 ns.
- For the load current values of 0 A, 20 A, 50 A, and 100 A, $t_{\mathrm{M(on)}}$ was measured for turn-on. Both $\mathrm{IGBT_H}$ and $\mathrm{IGBT_L}$ processes were used. The average of $t_{\mathrm{M(on)}}$ was 211 ns, with a standard deviation of 47 ns.

The values acquired for $t_{\mathrm{M(on)}}$ and $t_{\mathrm{M(off)}}$ were deemed accurate enough. The values cover the expected load current range. The purpose of the u_{G} turn-off model is to give timing values in the range of approx. 0.7 µs to 1.4 µs. Gate driver delays $t_{\mathrm{driver(on)}}$ and $t_{\mathrm{driver(off)}}$ are also needed, and they were measured in the test setup. A value of 0.5 µs is used for the gate driver delays. Also needed are the IGBT gate threshold voltage U_{T}, the forward transconductance g_{fs}, and the gate driver output voltage $U_{\mathrm{G+}}$ and $U_{\mathrm{G-}}$. The threshold voltage and the forward transconductance values were picked from the IGBT datasheet, and the gate driver output voltages were measured from the setup. The gate time constant was approximated by curve fitting the simulation results with the experimental results shown in Figure 3.15(a).

The equation for storage time t_{s} can be solved using the voltage after t_{ch} as the initial state for the t_{s} period. This gives

$$t_s = \tau_{gate}\left[\ln\left(U_{G+} - U_{G-} + (U_{M1} - U_{G+})\,e^{-\frac{t_{ch}}{\tau_{gate}}}\right) - \ln\left(U_{M2} - U_{G-}\right)\right] \tag{3.4}$$

The turn-off voltage edge delay is now defined by the u_G model above, but unfortunately, this u_G model cannot be directly combined with the experimental results of the load current, U_{DC}, and temperature variations. Future work could include studying the combination of the u_G model with other measurement-result-based turn-off voltage delay models. Using the u_G model gives more realistic results for narrow pulses, which are exactly what the ADUDT uses. Long-pulse turn-off voltage delay result values are not a good model to use when analyzing ADUDT operation. The typical pulse widths for the ADUDT in the test setup application range between 0.8 µs and 2.4 µs, a range which is in the nonlinear turn-off voltage edge portion in Figure 3.15. It can be seen that the minimum turn-off voltage delay value using the u_G model is $t_{driver(off)}+t_{M(off)}$. Compared with the experimental result in Figure 3.16(b), the minimum u_G model turn-off voltage delay value of approx. 640 ns is very close to the observed case.

Narrow gaps in the gate control signal cause a similar effect in the turn-on process as narrow on-times in turn-off process. Here the mechanism is somewhat different, as it involves the u_G voltage decreasing below U_T after turn-off, see Figure 3.7(b). If a subsequent turn-on command is issued, and the gate voltage has not yet reached U_{G-}, the following turn-on process will occur earlier. Figure 3.18 shows a typical case of the narrow gap effect in the turn-on voltage delay.

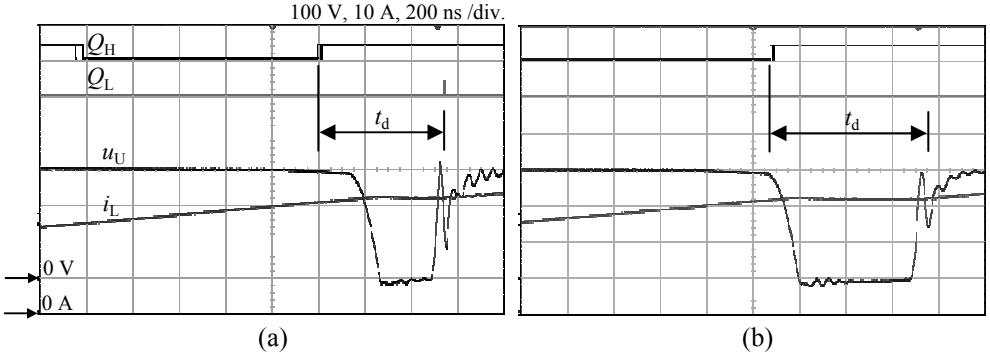


Figure 3.18. Behavior of narrow gaps in IGBT conduction. If the IGBT were previously turned off and then turned on again before the gate charge has reached the steady-state 'off' value, the turn-on process will occur earlier.

It was now important to investigate whether the narrow-gap turn-on phenomenon could occur with such gaps as are used in the ADUDT operation. For the prototype setup parameters, the smallest time to occur between turn-off and turn-on voltage edges in the same IGBT is 2.4 µs. If a significant timing nonlinearity is experienced with gaps having this width, it may have to be taken into account in the model. The measurement pulse pattern was arranged so that a narrow gap was produced in the gate drive command signal. The load current at the end of

the test pulse pattern was measured to reveal how the gap affects the output voltage. This is shown in Figure 3.19.

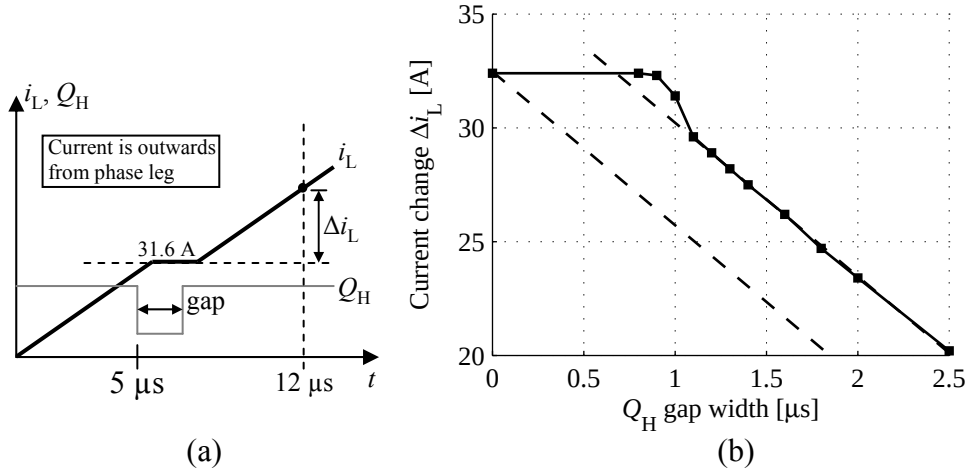


Figure 3.19. Waveforms (a) and results (b) of the narrow gap effect measurement method. The lower dashed line in (b) represents the current graph expected if the switches in the leg are ideal. The upper dashed line is the asymptote of the measured current graph with large gap values.

It was noticed that when the gap was large enough, the dependency of load current and gap length was linear. Since the turn-off delay is larger than the turn-on delay, the phase leg does not show any change in the output before the gap is wide enough; that is why the current values are generally higher than with an ideal phase leg. However, when the gap is decreased and approaching 1.1 µs, there is a visible deviation from the linear asymptote in the graph. It seems that the output voltage gap gets narrower faster than the gate drive signal gap is changed. Then, just below 0.9 µs gap in Q_H, the output voltage gap disappears completely, latching the current to a constant value.

The conclusion based on this result is that for Q_H gaps larger than 1.1 µs, the turn-on voltage delay is not dependent on the previous turn-off process. Below this value, the turn-on will occur earlier as the gate charge has not reached the steady-state value, and the timing shows a nonlinear behavior. The conclusion is shown in Figure 3.20.

Even though the coupling between the gap turn-on and turn-off was found, the boundary value for the gap width is considerably smaller than what would actually occur in the example ADUDT application setup. Nevertheless, if the ADUDT pulse patterns are made more dense in the future by adding more pulses or when trying to make fast and accurate ADUDT output voltage edges, the gap phenomenon may have to be considered.

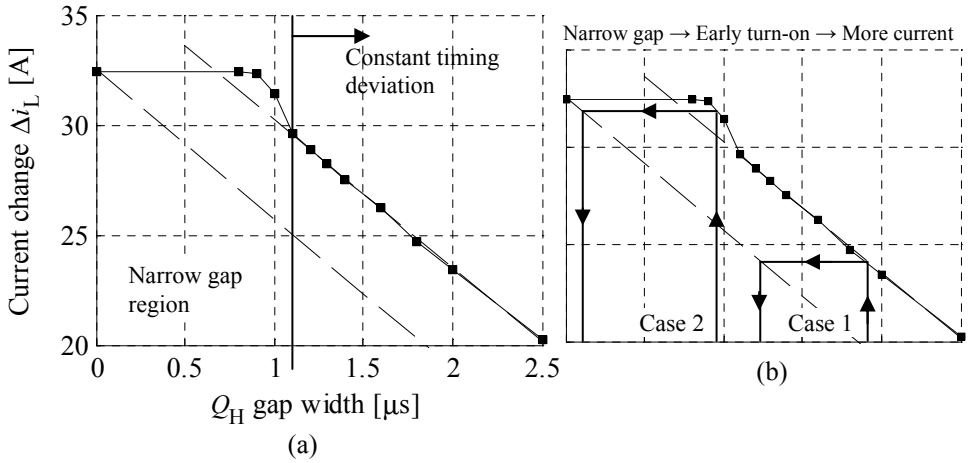


Figure 3.20. Understanding the behavior of narrow gaps. The turn-on can become coupled with the previous turn-off. In (b) Case 1, the difference between the observed output voltage gap and the calculated ideal case is constant. However, with smaller gaps in Case 2, the observed output current corresponds to an ideal gap of a significantly smaller value than the constant difference in the wide-gap case.

3.2.3 Controlling the IGBT state during its anti-parallel diode conduction period

It is possible to control the IGBT to turn on or turn off even though there is going to be no current flowing. One typical setting is when either of the anti-parallel freewheeling diodes in the phase leg are conducting the load current. The IGBT in parallel with the conducting diode can be controlled to turn on, but it will not affect the phase leg operation or the output voltage. Likewise, the IGBT can be turned off, with no effect on the output. Nevertheless, there are situations when the turn-on or turn-off during diode conduction is beneficial or even required by the ADUDT application. One option is to counteract the IGBT delays in the event of load current zero-crossing. Turn-on and turn-off during diode conduction are generally required when producing narrow output voltage pulses. The reason is the IGBT delays.

In theory, the IGBT gate voltage will go through the turn-on and turn-off processes just like the IGBT would if it was controlling the phase leg output. But the question is, how does the ability to conduct or stop conducting behave when there is no current in the device (yet). In other words, how would the phase leg react if the IGBT were controlled for turn-on, but the load current direction were such that the current would be transferred to the IGBT *some time after* it was turned on? Likewise, how does the IGBT turn-off show itself if the load current direction is changed after the IGBT is controlled to turn off?

The test procedure pulse pattern is shown in Figure 3.21. In (a), the narrow pulse turn-off behavior is tested again to see if the storage time effect on the turn-off voltage edge delay still exists. This test would suggest that the IGBT gate control pulse width affects the turn-off

delay regardless of whether the IGBT actually carries any current during the gate charging periods. It also shows how the turn-on command must be placed in relation to the load current zero crossing in order to prevent a ZCC during current direction reversal. In (b), the IGBT turn-off distance from the load current zero crossing point is varied. The target is to demonstrate the production of narrow output voltage pulses after load current zero crossing.

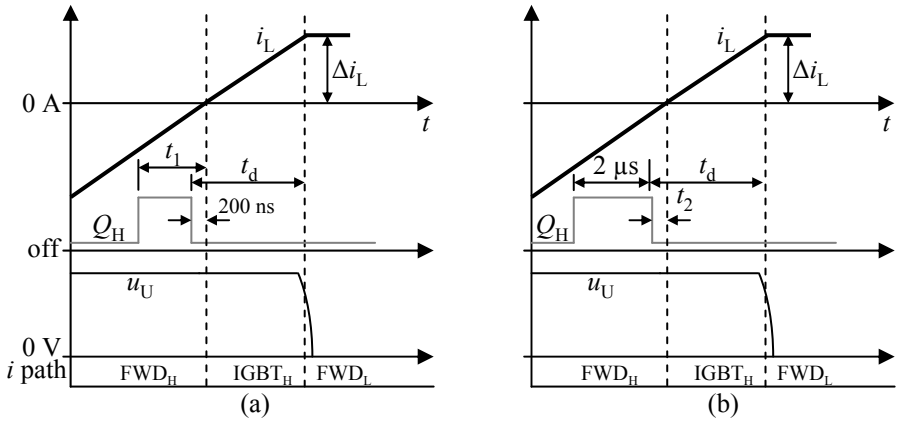


Figure 3.21. Measurement method of turn-on and turn-off of the IGBT that has its freewheeling diode (FWD) conducting.

The test results are shown in Figure 3.22. The narrow-pulse turn-off delay effect can be seen in (a), with the interesting observation that the zero current turn-off with a narrow pulse width is very similar in behavior to the case of current-conducting IGBTs. In (b), the logic-level gate control pulse has a constant width of 2 µs. One result here is the zero-current turn-off behavior, showing that the turn-off process of the IGBT does not require current to flow in the collector.

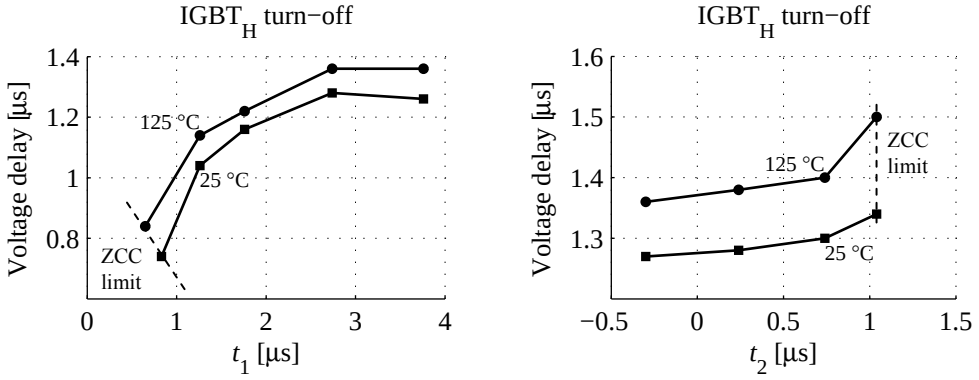


Figure 3.22. IGBT switching during FWD conduction results.

In order to produce narrow output voltage pulses after load current zero crossing as above, the logic-level gate drive commands are sometimes placed within diode conduction periods.

It seems that the gate voltage waveform is what matters in terms of IGBT conduction, even when the IGBT is not going to conduct the current.

3.3 Phase leg shoot-through and diode reverse recovery

It is generally desirable to prevent both IGBTs from conducting at the same time, as this case effectively causes a current to flow from the positive DC bus bar to the negative, a current that does not contribute to the load current. This case of simultaneous IGBT conduction is referred to as 'cross conduction', 'phase leg short circuit', or 'phase leg shoot-through'. The current is limited by the IGBT dynamic resistance and the current path impedance, but can still be high and cause additional losses in the phase leg. If the cross-conduction duration is long enough and the current magnitude large enough, the result can be IGBT destruction. In less severe cases, the resulting current spikes can cause EMI problems.

The sequential turn-off and turn-on waveforms of the high-side and low-side IGBTs are shown in Figure 3.23.

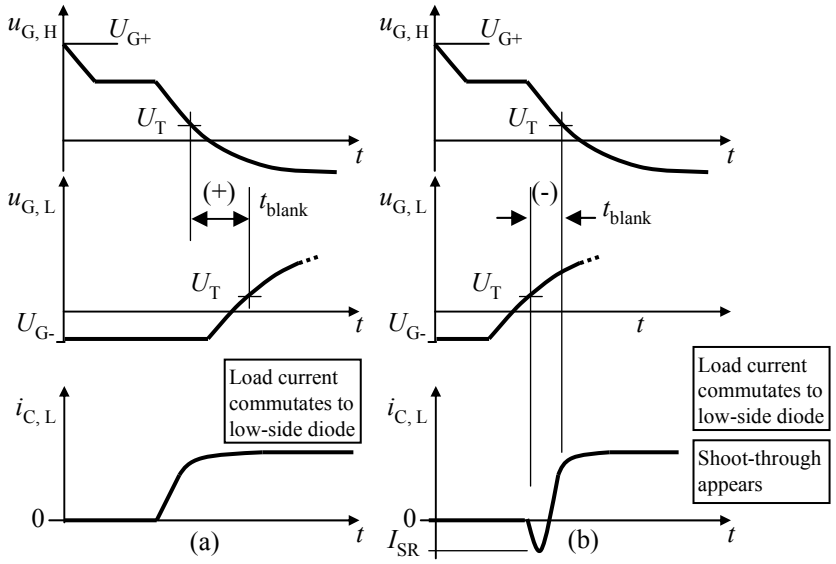


Figure 3.23. Shoot-through is generated when the turn-on of the IGBT takes place before the opposite-side IGBT has turned off. The figure shows a case for current direction outwards from the phase leg, initially through $IGBT_H$. The turn-on of the $IGBT_L$ is not necessary for the load current to flow.

Free-wheeling diodes exhibit the reverse recovery phenomenon when turning from the forward-biased mode to the reverse-biased mode. During the reverse recovery process, the diode permits some current to flow in the reverse direction, the amount of which depends on the diode characteristics. Figure 3.24 shows the waveform of the reverse recovery process.

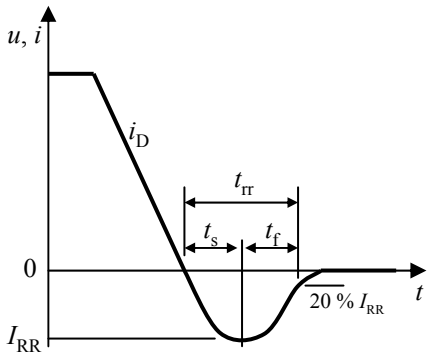


Figure 3.24. Diode reverse recovery.

Whenever the load current is commutated from the conducting diode to the opposite-side IGBT by turning that IGBT on, the reverse recovery produces a current pulse in the phase leg, which is similar to the shoot-through caused by the overlapping IGBT conduction. This behavior is shown in Figure 3.25.

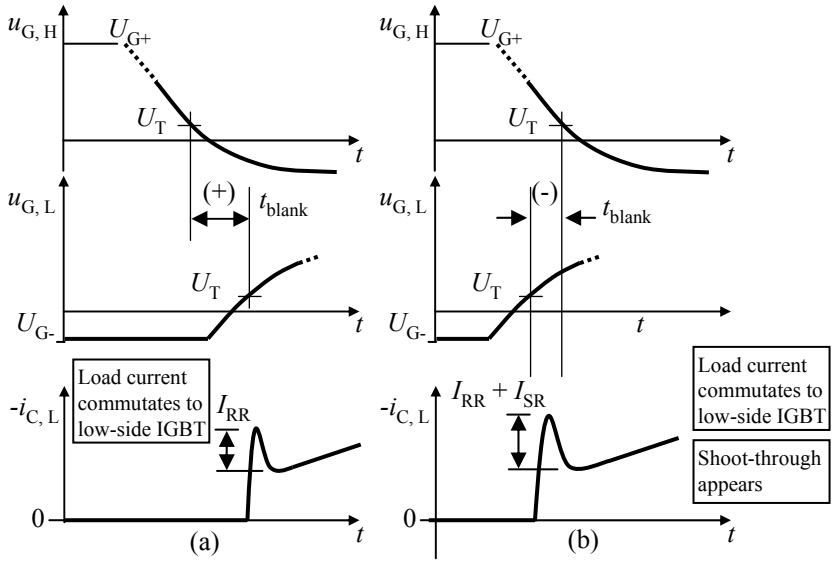


Figure 3.25. When load current is commutated from the high-side diode to the $IGBT_L$, the reverse recovery of the diode will cause a phase leg shoot-through. Any overlap in the IGBT conduction will increase this shoot-through current peak.

Next, measurements were made to investigate the minimum dead time of the logic-level gate drive signal required to prevent the overshoot caused by an overlap. The test was conducted using a load current up to 150 A, in both directions. The IGBT gate command sequences were both $IGBT_H \rightarrow IGBT_L$ and $IGBT_L \rightarrow IGBT_H$. This gives four sets of data as a function of

load current. The temperature was also varied. U_{DC} was constant 600 V during the test, and the pulse widths such that the turn-off was not affected by the differences in the gate charge storage times. The test procedure for observing the dead time requirement is shown in Figure 3.26, and for the reverse recovery case, the I_{RR} peak is observed to detect the I_{SR}.

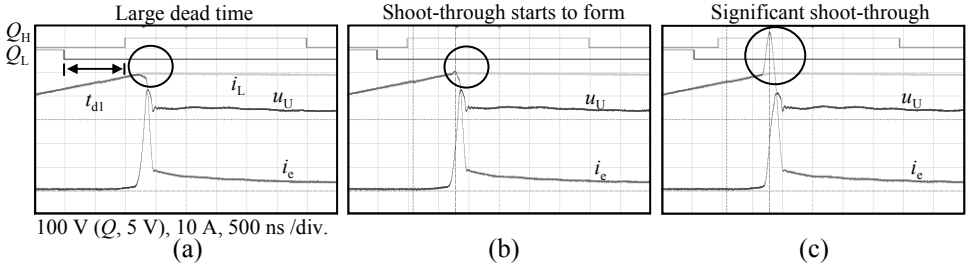


Figure 3.26. Occurrence of phase leg shoot-through and how the dead time is used to prevent it.

The minimum dead time test results are depicted in Figure 3.27.

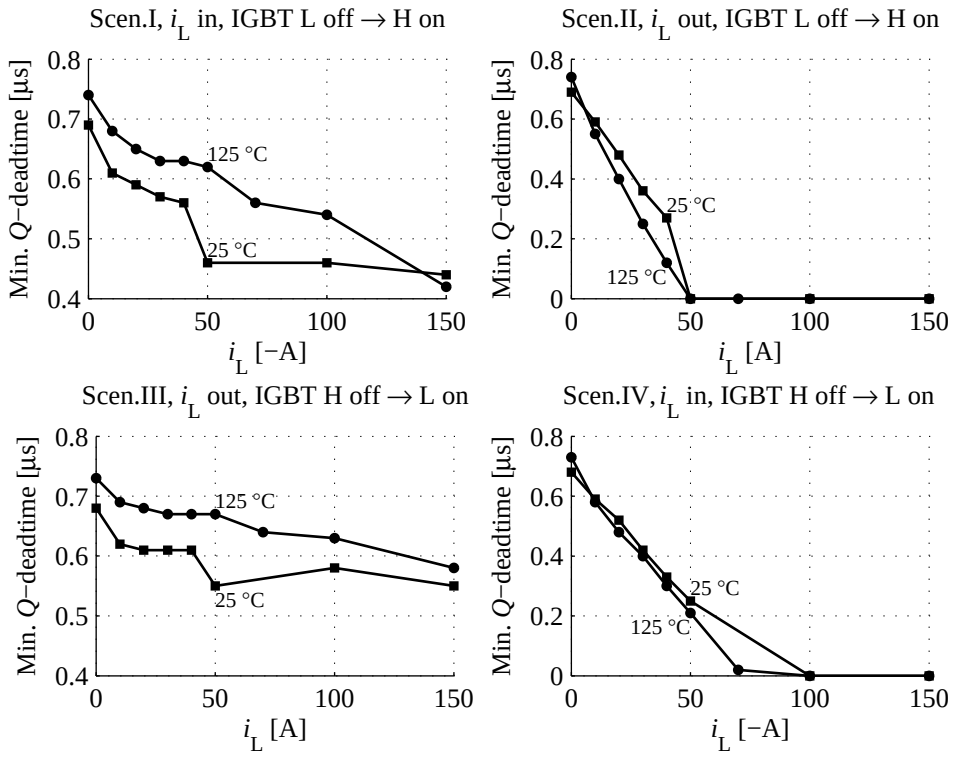


Figure 3.27. Minimum dead time results. In scenarios where reverse recovery takes place, the required minimum dead time decreases as the load current magnitude is increased.

In Figure 3.27 it appears as if the required dead time diminishes to zero as the load

current magnitude increases. Further, the gate command sequence transition from $\mathrm{IGBT_H}\rightarrow\mathrm{IGBT_L}$seems to require more dead time than $\mathrm{IGBT_L}\rightarrow\mathrm{IGBT_H}$. It is reasonable to assume that the diode reverse recovery peak masks the IGBT conduction overlap, if the I_{RR} peak duration is increasing as the load current increases. To verify this, the reverse recovery peak duration t_{rr} as a function of commutated load current was measured. The results are illustrated in Table 3.1.

Table 3.1. Reverse recovery time as a function of load current. U_{DC} 600 V, $T = 125\ ^{\circ}\mathrm{C}$

i_{c} [A]	t_{rr}[ns]
10	300
50	400
100	600
150	900

The reverse recovery process is indeed dependent on the current and temperature (Lutz et al., 2011), which is the reason why the need for dead time is reduced with diode-IGBT commutation. If one single value for dead time had to be chosen, such that under no circumstances the phase leg would go to even slight shoot-through, then approx. 0.8 µs would be a good value for this test setup. But as the conditions vary, a smaller value would suffice. What happens during this wasted dead time? The logical conclusion is that the leg blanking time t_{blank} in Figures 3.23 and 3.25 increases, and neither of the IGBTs is able to conduct for a short period of time. This condition leads to a variable t_{blank} to appear in the phase leg. If the leg output current is driven to zero by the external load circuit, a ZCC period can appear, having a variable length depending on the blanking time length and the external load circuit di/dt.

To understand what happens, we should look at one possible ADUDT sequence in Figure 3.28, which occurs frequently in the application.

Now it is possible that with a generously large value of dead time, the phase leg will go in the ZCC during the ADUDT sequence, as a result of the filter inductor current 'trying' to cross the zero and continue in the opposite direction, but it will fail as there is no IGBT able to conduct. However, with a proper timing of the pulse sequence, the sequence can still achieve the optimal response of the output voltage, even with two ZCCs to appear, or complete removal of the A-pulse. This is illustrated in Figures 3.29 and 3.30.

As the phase leg output current reaches the ZCC, the di/dt in the phase leg is directly the value of the load di/dt, unlike the forced-commutation associated with IGBT participation. This makes the reverse recovery process di/dt quite low compared with normal hard-switching operation. In our test setup, the filter di/dt is approx. 40 A/µs, compared with the observed 400 A/µs with hard-switching. The voltage edge produced at the ZCC is defined by the current cross-over point, with no additional delays.

Before entering the next chapter where the actual algorithm and the ZCC-aware filter control

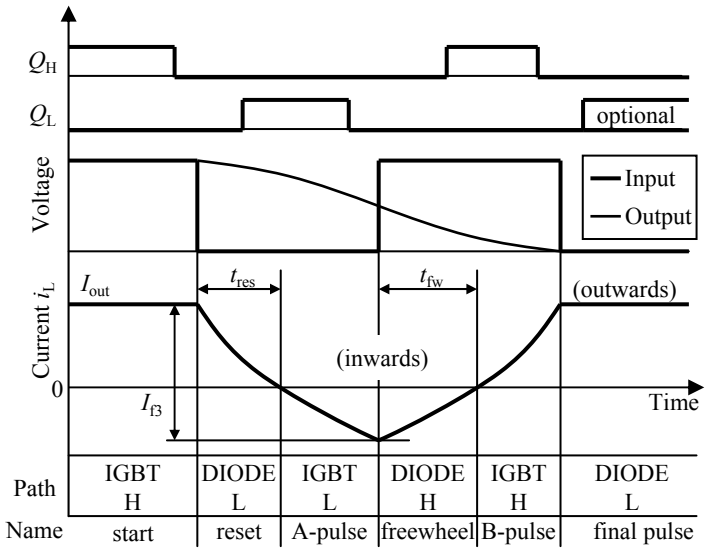


Figure 3.28. When ever the situation in ADUDT application is such that the filter inductor current has to cross zero for successful output voltage control, a zero-current clamp (ZCC) may appear if the phase leg blanking time is longer than t_{res} or t_{fw}. As there are delays in the phase leg, the change in output state does not follow the gate commands precisely.

method are discussed, we must point out that the origin of the ZCCs, and their duration, is a consequence of various possible reasons:

- Unknown phase leg timing characteristics, and choosing large enough value for a fixed dead time to be free from overlap in IGBT conduction. This results in ZCCs that are also unknown and varying.
- Knowing the timing characteristics, but using a fixed value for the dead time. Results in known ZCCs.
- Limited knowledge of timing, and using a generously large value for the dead time. It is possible to mask the timing variations under the dead time such that the ZCC durations are mostly constant.

One possible method would be to use a minimized, variable dead time, resulting in a minimum ZCC, and simplifying the ADUDT control itself while possibly making the pulse generation logic more demanding because of the variable dead time. Based on the IGBT switching waveforms, there is no need for a surplus blanking time, other than ‘being careful’ because of not knowing/trusting the timing data. In any case, the success of the ADUDT control is dependent on the timing data accuracy, be it with a ZCC or not. With the new control method, the dead time does not need to be minimized, as the ZCC can be compensated. What is more

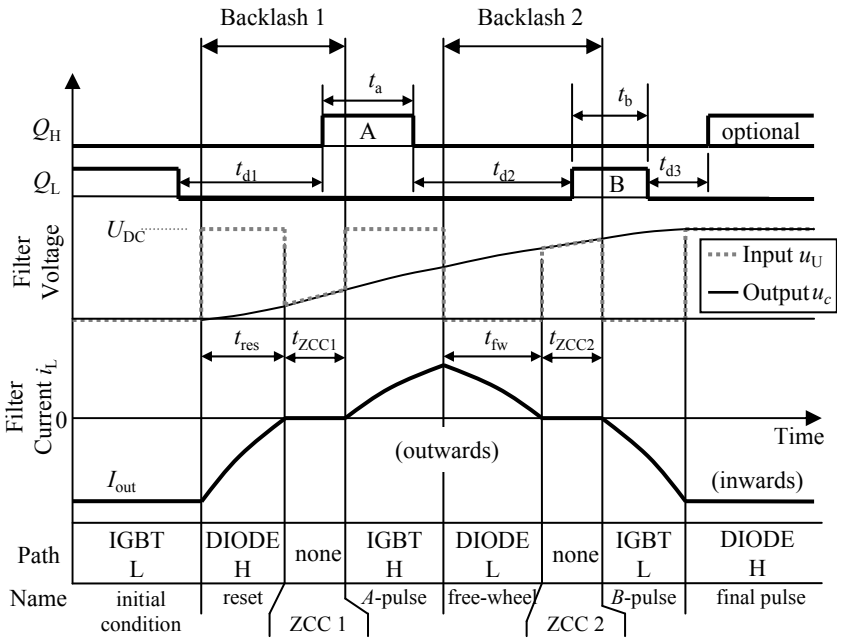


Figure 3.29. ZCCs are not a problem, and their effect can be taken into account in the new control algorithm. However, the phase leg delays are still present.

important is the accurate knowledge of the timing; The method cannot compensate for unknowns. But as the knowledge of timing increases, at the same time decreases the need for ZCC compensation, as the dead time could be minimized.

Future studies should investigate the significance of short-time phase leg cross-conduction, in the order of for instance 50 ns. Already the diode reverse-recovery process causes current conduction spikes in the phase leg. If the slight cross-conduction had not to be taken into consideration, then it could mean the dead time (if technically possible in the PWM electronics) could be made to track the time-variating nature of the phase leg, squeezing the ZCC out of the pulse pattern. Then, the emphasis would be on the accurate timing delay compensation, and the complications of the ZCC algorithm can be removed from the ADUDT control. It must be noted that the ADUDT control is not able to compensate for unknown ZCC either, so in any case, the ultimate accuracy of the ADUDT is only achieved through phase leg delay compensation. Inaccuracies in the ZCC compensation will generally not cause any harm, as major shoot-through could, but result in less than optimal ADUDT performance because of the output voltage overshoot.

The phase leg shoot-through could be estimated by using the virtual voltage edges as a metric for the IGBT turn-on and turn-off. Looking at the IGBT switching waveforms, a virtual rising voltage edge occurs after the IGBT has turned on, and a virtual falling edge before the turn-off takes place. This means that there must be a separation between the virtual voltage edges in the analysis, if shoot-through is to be prevented.

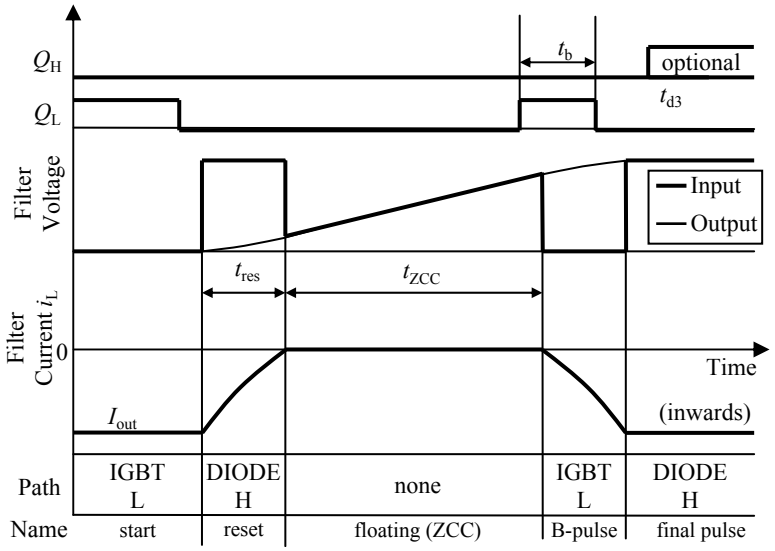


Figure 3.30. ZCC periods can be chained by a technique using the load current and the B-pulse, without the A-pulse, to control the filter output voltage.

Chapter 4

New active d*u*/d*t* pulse pattern solution algorithm

The active d*u*/d*t* output filtering method uses voltage pulses formed in the phase legs to control the filter output voltage. The structure of this pulse pattern is critical for the ADUDT operation. Ideally, the purpose is to change the filter output voltage between zero and the DC link value in such a way that the overshoot in the output voltage is zero. The step response of the filter output voltage to filter the input voltage is a typical second-order system response with a low damping factor. Thus, with a stepwise input voltage, the filter output voltage has a peak value of close to double the input voltage amplitude. This is where the control pulse pattern is needed. Its purpose is to eliminate this overshoot and provide active damping of the system (the filter network). The structure of this pulse pattern is, first and foremost, dependent on the filter inductance and capacitance values, which directly affect the control pulse widths. The motor load current also affects the requirements of the pattern shape, and if there are such long dead times in the phase leg that a zero current clamping of the filter inductor occurs.

Previous solutions for forming the ADUDT control pulse pattern have been presented in (Ström, 2009), (Ström et al., 2011), and (Korhonen et al., 2009). The fundamental idea behind the operation is to use narrow voltage pulses from the inverter to control the voltage of an LC low-pass filter circuit. With these voltage pulses, the LC circuit capacitor voltage is made to transit smoothly between zero and the DC link voltage, in a controlled manner without the typical overshoot of a low-damping factor resonance circuit. With suitably timed pulses with respect to the LC circuit resonant frequency, the LC filter output voltage has gradual transitions from zero to the DC link voltage and back, at the edges of the original PWM control pulse commands. The LC filter has ideally a very low damping factor, resulting in low losses in the filter. Since the damping factor is low, the filter capacitor voltage can have peak values reaching double the DC link voltage as a result of the resonance in the LC circuit if the pulse operation is not correct for the filter. The purpose of the active d*u*/d*t* submodulation

pulses is thus to keep this voltage below acceptable limits, reaching the DC link voltage in ideal cases. As the voltage source inverter is seen as a device that is supposed to output voltage pulses with amplitude of U_{DC}, then U_{DC} is the target steady-state filter output voltage value after the edge slope. At the same time, the inductance in the filter can be comparatively low to achieve voltage transition times required for 100 s of meters-long cables encountered in variable-speed AC drive applications.

4.1 Starting point for the solution

The algorithm solution assumes the power electronics and the circuit to be ideal. All non-idealities have to be added in a form of timing correction coefficients. However, this new solution can handle zero-current clamping times in the sequence, making it easier to include dead times of varying duration. The simplified case of an ideal LC circuit, controlled by an ideal phase leg (ideal switches, ideal diodes) and also interacted on by the motor load current, is shown in Figure 4.1.

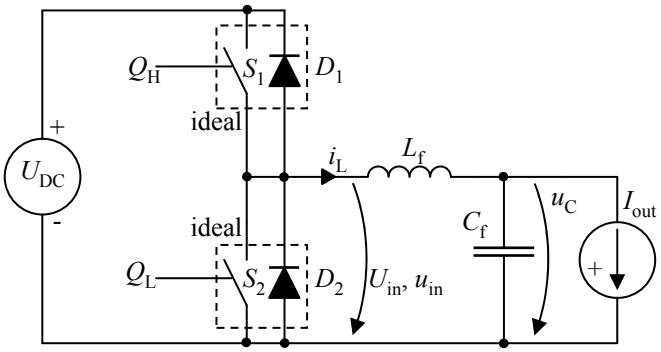


Figure 4.1. Simplified model of a phase leg with an ADUDT filter and a load current source. All components are assumed ideal.

In this simplified model, the following simplifications have been made compared with the real IGBT phase leg and ADUDT filter electronics:

- The DC link voltage U_{DC} is constant during the ADUDT pulse pattern, and known in advance.
- There are no additional impedances in the filter circuit, such as stray reactances or resistance.
- The high-side and low-side switch conduction states follow the gate drive commands precisely, with no delay.
- The switches in the phase leg are ideal, and there are no parasitic reactances in the

phase leg. The change in the phase leg output voltage resulting from the switch status change is immediate, and there are no slopes in the output voltage pulse edges.

- The diodes are ideal, having immediate blocking and conduction when changing between reverse-biased to forward-biased states.
- There is no resistance in the DC link or the switches.
- The filter inductance and capacitance are constant.
- The motor cable surge impedance (the characteristic impedance) does not interact with the filter circuit; for instance, the transmission line is omitted in the analysis.
- The load current is constant during the ADUDT pulse pattern.

For this idealized case, it is possible to express the equations for the filter capacitor voltage and the filter inductor current, with the phase leg output voltage constant over the observation period and the motor load current assumed constant during the whole ADUDT pulse sequence. The state-space equation of this initial-value problem is

$$\begin{aligned} \dot{u}_{\mathrm{C}} &= \frac{1}{C_{\mathrm{f}}} i_{\mathrm{L_f}} - \frac{1}{C_{\mathrm{f}}} I_{\mathrm{out}} \\ \dot{i}_{\mathrm{L}} &= -\frac{1}{L_{\mathrm{f}}} u_{\mathrm{C_f}} + \frac{1}{L_{\mathrm{f}}} U_{\mathrm{in}} \end{aligned} \tag{4.1}$$

which gives a Laplace-transformed form

$$\begin{aligned} sU_{\mathrm{C}}(s) - u_{\mathrm{C_f}}(0) &= \frac{1}{C_{\mathrm{f}}} I_{\mathrm{L_f}}(s) - \frac{1}{C_{\mathrm{f}}} \frac{I_{\mathrm{out}}}{s} \\ sI_{\mathrm{L}}(s) - i_{\mathrm{L_f}}(0) &= -\frac{1}{L_{\mathrm{f}}} U_{\mathrm{C_f}}(s) + \frac{1}{L_{\mathrm{f}}} \frac{U_{\mathrm{in}}}{s} \end{aligned} \tag{4.2}$$

The time-domain solution for the filter voltage and current equations when the filter inductor current is nonzero (meaning i_{L} is flowing through either S_1, S_2, D_1, or D_2) are

$$\begin{aligned} u_{\mathrm{C}}(t) &= U_{\mathrm{in}} \left[1 - \cos\left(\omega_{\mathrm{f}} t\right)\right] + Z_{\mathrm{f}} \sin\left(\omega_{\mathrm{f}} t\right) \left(i_{\mathrm{L}}(0) - I_{\mathrm{out}}\right) + u_{\mathrm{C}}(0) \cos\left(\omega_{\mathrm{f}} t\right) \\ i_{\mathrm{L}}(t) &= I_{\mathrm{out}} \left[1 - \cos\left(\omega_{\mathrm{f}} t\right)\right] + Y_{\mathrm{f}} \sin\left(\omega_{\mathrm{f}} t\right) \left(U_{\mathrm{DC}} - u_{\mathrm{C}}(0)\right) + u_{\mathrm{C}}(0) \cos\left(\omega_{\mathrm{f}} t\right) \end{aligned} \tag{4.3}$$

It is also possible that i_{L} is zero, the leg output is floating, and the load current is the only source affecting the capacitor voltage, in which case the filter time-domain state equations are

$$\begin{aligned} u_{\mathrm{C}}(t) &= u_{\mathrm{C}}(0) - \frac{1}{C} I_{\mathrm{out}} t \\ i_{\mathrm{L}}(t) &= 0 \\ u_{\mathrm{in}}(t) &= u_{\mathrm{C}}(t) \end{aligned} \tag{4.4}$$

Figure 4.2 shows an example of how in principle the A-pulse sequence can be used to bring the capacitor voltage from zero to U_{DC} with no overshoot.

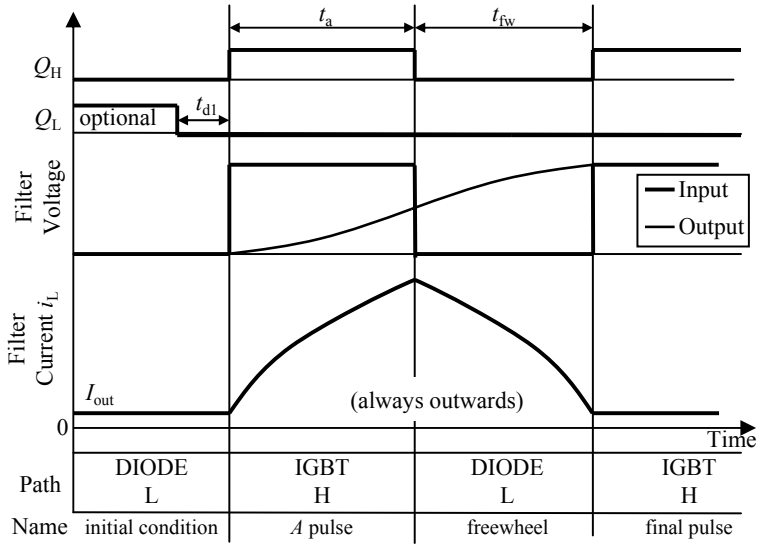


Figure 4.2. Simple active d*u*/d*t* pulse pattern where only the A-pulse is used.

In Figure 4.3 filter current zero crossing is involved, since the load current direction is opposite to filter charge current change. This requires B-pulse to be used, to restore inductor current back to the load current value at the end of the sequence. In this example, the zero-current crossing is made with no zero-current clamping (ZCC) time, such that the direction changes with no interruption.

If the dead time constraints require A-pulse and/or B-pulse to be delayed, then ZCC can occur in the sequence, complicating its structure. The ZCC can also appear as a result of uncompensated timing errors, although the calculation of correct sequence with ZCC requires the ZCC times to be known in advance. Thus, the ZCC is considered as an integral part of the sequence just like A-pulse and B-pulse. It is also possible to design-in the ZCC times, as this might give some advantages for delay effect immunity or pattern implementation. This will be discussed in more detail later. The sequence example using two ZCC time periods is shown in Figure 4.4.

The concept of ZCC can be further exploited to give a sequence where the A-pulse is completely discarded. This works for A+B-sequences, and is feasible for reasonable I_{out} values

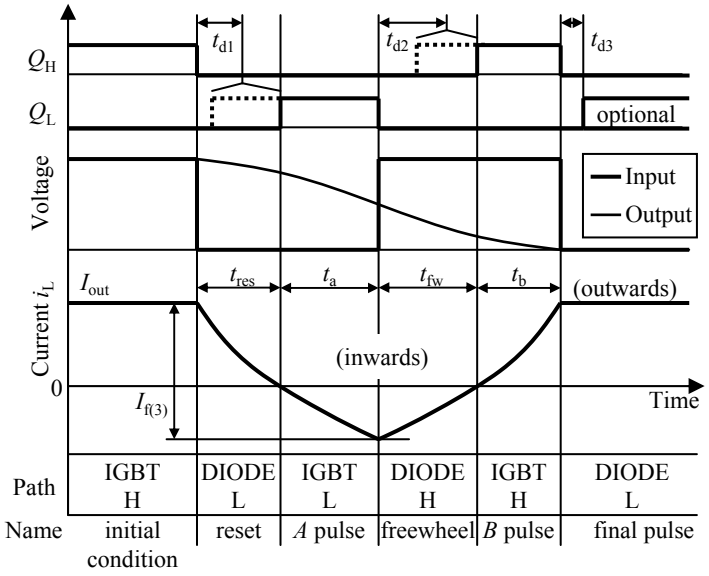


Figure 4.3. Motor load current can affect the sequence, requiring the B-pulse to be added.

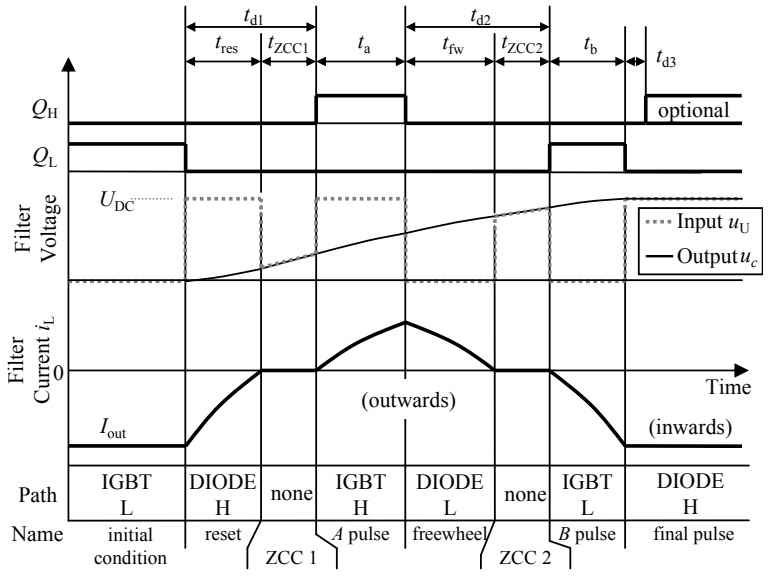


Figure 4.4. If the phase leg is unable to conduct the load current for some time periods within the pulse pattern, the filter inductor goes into ZCC, possibly before the A-pulse and/or after a freewheeling period. This also affects the A-pulse width and the freewheeling period, complicating the pattern timing solution.

such that the filter capacitor can be charged using only ZCC effect. B-pulse is still required, as it cannot be substituted with any other property in the phase leg.

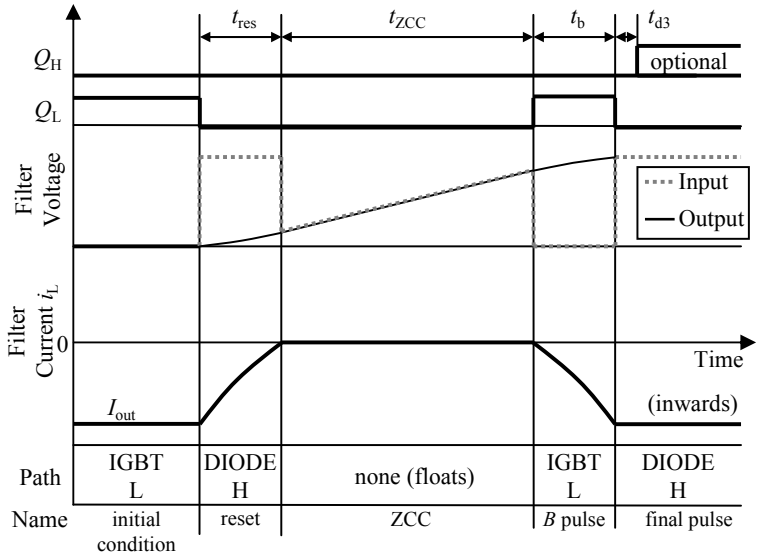


Figure 4.5. Motor load current can be used as a sole means to charge the filter, and thus, the A-pulse can be dropped out.

The algorithm proposed in this thesis is a mathematical tool allowing the structure of the pulse pattern to be solved, and as a new feature, it can now handle the ZCCs. The solution is in analytical form, except one unsolved constraint equation when t_{ZCC2} is also included. This equation is solved numerically for now, and analytical solution could be included in future work. It must be noted that the algorithm does not have any internal means of compensating for the phase leg delay effects. This compensation would have to be designed separately. The new algorithm merely makes it possible to have total freedom over ZCC in the sequence. Previous solutions did not include the ZCC, and only iterated/numerical solutions were demonstrated for limited example cases. Figure 4.6 lists all the possibilities of the new algorithm, together with all possible single A/B-pulse sequences for the ADUDT.

4.2 Development of the new pulse pattern solution algorithm

We first define some useful characteristic values for the filter, as they are frequently used in the filter equations:

$$Z_f = \sqrt{\frac{L_f}{C_f}} \tag{4.5}$$

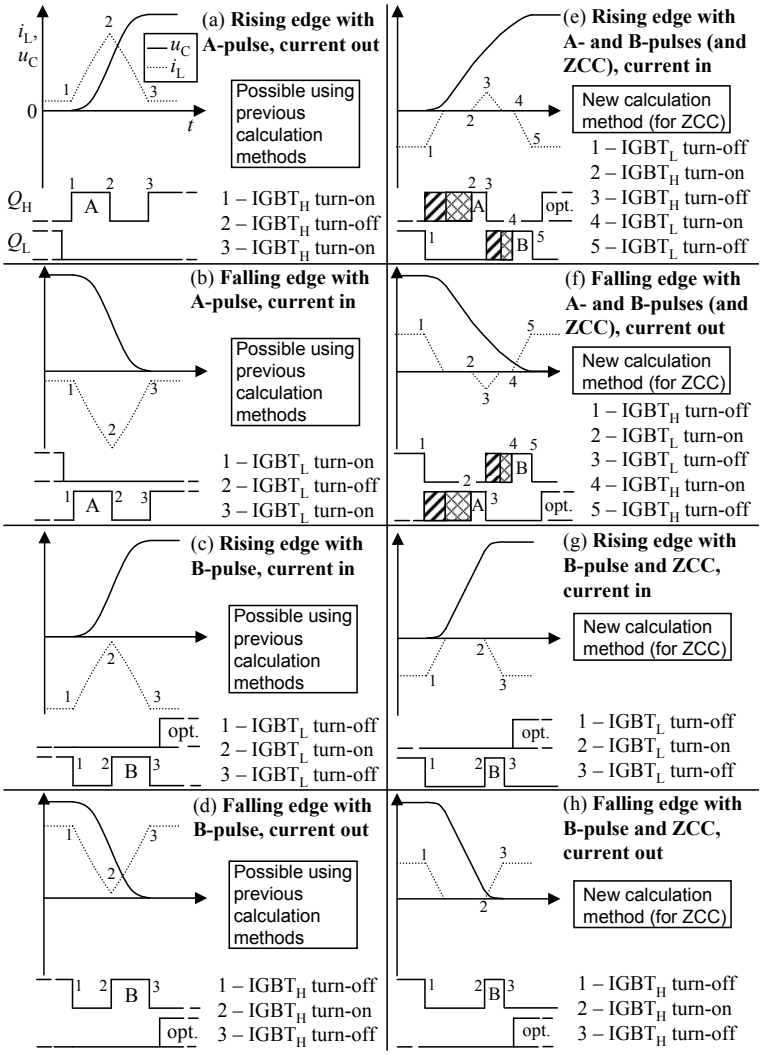


Figure 4.6. Some pulse pattern types could be solved using the previous calculation methods. In addition, the new algorithm can also solve the patterns that contain filter zero current clamping periods.

$$Y_{\mathrm{f}} = \frac{1}{Z_{\mathrm{f}}} \tag{4.6}$$

$$\tau_{\mathrm{f}} = \sqrt{L_{\mathrm{f}} C_{\mathrm{f}}} \tag{4.7}$$

$$\omega_{\mathrm{f}} = \frac{1}{\tau_{\mathrm{f}}} \tag{4.8}$$

$$I_{\mathrm{f}} = U_{\mathrm{DC}} Y_{\mathrm{f}} \tag{4.9}$$

$$I_{\mathrm{f3}} = \frac{\sqrt{3}}{2} I_{\mathrm{f}} \tag{4.10}$$

Z_{f} and Y_{f} are the impedance and admittance of the filter network, respectively. They describe what is the natural ratio of voltage and current in the filter resonance. τ_{f} and ω_{f} describe the resonant frequency of the filter in natural units, and τ_{f} can be considered as the angular period of the filter, often called the filter time constant in this thesis (as it appears in equations describing the timing of filter pulses). I_{f} is the resonant current amplitude of the filter with undamped step response, dependent on the filter admittance and U_{DC} step voltage. I_{f3} is the characteristic peak filter charge current with no ZCC, as shown e.g. in Figure 4.3.

The goal of the algorithm is quite simple: Bring the filter voltage from zero to U_{DC} or U_{DC} to zero with no overshoot, using any arrangement of periods t_{res}, t_{ZCC1}, t_{a}, t_{fw}, t_{ZCC2}, and t_{b}, to construct a piece-wise continuous u_{C} voltage to appear at the filter output. It can be seen from sequence examples above that for some I_{out} directions versus output voltage transient directions, this task can be relatively straightforward to solve and having a simple sequence structure, if no ZCC is involved. Such solutions have already been proposed in previous work. The solution for ZCC is more general and covers all possible cases with up to single A- pulse and B-pulse.

The solution starts with taking the negative load current / rising u_{C} voltage edge as a model case. This is the normalized solution. The inverse load current / edge direction is a symmetrical inversion of the normalized solution, and so is handled with the same algorithm but using input parameter inversions and gate signal swapping at the end, needing no separate solution method other than the inversion logic. If the sequence does not involve ZCC, then the solution becomes simple as described above and in previous work. These cases are included in the final algorithm here. At the beginning, the input parameters for the ADUDT case are known. The first part of the algorithm arbitrates between the possible sequence cases. Four possible combinations exist that lead into the simple solution, requiring no further action but applying the pattern calculation as already published in e.g. (Ström, 2009). Two remaining cases may or may not require the new algorithm equations, depending if the ZCC really appears, and this is dependent on the parameters. If ZCC is still not present in these cases, then the previously published method in (Ström, 2009) could be used to calculate the pattern timing. It is only when ZCC appears that new equations are needed, and they are presented in this thesis. The ADUDT case arbitration in the first part of the algorithm is shown in Figure 4.7.

If the algorithm detects the cases for possible ZCC, the algorithm then advances to the second part of the solution, shown in Figure 4.8.

Whether or not the ZCCs appear is dependent on the input parameters. The first ZCC period t_{ZCC1} can be calculated from the dead time constraint t_{d1} and filter t_{res}:

$$t_{\text{res}} = \tau_{\text{f}} \arcsin \left| \frac{I_{\text{out}}}{I_{\text{f}}} \right| \tag{4.11}$$

$$t_{\text{ZCC1}} = t_{\text{d1}} - t_{\text{res}} \tag{4.12}$$

If the resulting t_{ZCC1} is positive, then ZCC must appear before A-pulse, and new equations for t_{a} and t_{fw} are required in the process. This is where the new solution is used. It continues by calculating the ZCC properties of the sequence case, first the maximum ZCC time. The maximum total time we can spend on both the floating leg periods combined (the zero current clamped status) is $t_{\text{ZCC,max}} = t_{\text{ZCC1}} + t_{\text{ZCC2}}$:

$$t_{\text{ZCC,max}} = \sqrt{4 \left(\frac{U_{\text{DC}} C_{\text{f}}}{I_{\text{out}}} \right)^2 - 4 L_{\text{f}} C_{\text{f}}} - U_{\text{DC}} \left| \frac{C_{\text{f}}}{I_{\text{out}}} \right| \tag{4.13}$$

where the balance between ZCC1 and ZCC2 can be freely chosen. At this point t_{ZCC1} is already known based on the dead time constraint and the reset time t_{res}, and the algorithm knows the constraint for t_{ZCC2} using the maximum ZCC time as solved in Equation 4.13. Now comes the first section in the sequence where the capacitor voltage is changed. During the filter reset time t_{res}, the filter capacitor voltage will change according to

$$u_{\text{C,tres}} = U_{\text{DC}} - \sqrt{U_{\text{DC}}^2 - I_{\text{out}}^2 Z_{\text{f}}^2} \tag{4.14}$$

Whether or not the first ZCC appears, the algorithm calculates the voltage change during t_{ZCC1} (the voltage change which would become zero if t_{ZCC1} is zero). The voltage change during t_{ZCC1} appears after t_{res}. During the zero current clamp time periods, the filter capacitor voltage will change according to Equation 4.15.

$$u_{\text{ZCC1}} = \left| \frac{1}{C_{\text{f}}} I_{\text{out}} t_{\text{ZCC1}} \right| \tag{4.15}$$

At this point the algorithm jumps to a subroutine which calculates the t_{ZCC2} using the given parameters (dead time constraints, minimum times). The subroutine is described later. The subroutine returns the value for t_{ZCC2} after which the voltage at second ZCC is calculated. The voltage change during t_{ZCC2} appear after t_{a} and t_{fw} periods but its value is needed in t_{a} and t_{fw} equations.

$$u_{\text{ZCC2}} = \left| \frac{1}{C_{\text{f}}} I_{\text{out}} t_{\text{ZCC2}} \right| \tag{4.16}$$

Now, we prepare to solve the time periods of the A-pulse and the freewheeling (FW) periods, t_{a} and t_{fw}, respectively. These are the most important parts of the new algorithm and involved most of the additional work. The method for their solution is described in more detail in Appendix B. This part starts by first calculating the specific filter capacitor voltages during the pulse sequence:

$$u_1 = u_{\mathrm{C,tres}} + u_{\mathrm{ZCC1}} \tag{4.17}$$

which can be understood as voltage before the A-pulse, for solving the FW period length, and then

$$u_2 = U_{\mathrm{DC}} - u_{\mathrm{C,tres}} - u_{\mathrm{ZCC2}} \tag{4.18}$$

which is the capacitor voltage after the FW period. For the A-pulse width calculation, the time is reversed, the meaning of voltages inverted in relation to the DC link voltage, and the A-pulse is solved using the same equation as for the FW period:

$$u_{1,\mathrm{rev}} = U_{\mathrm{DC}} - u_{\mathrm{ZCC2}} \tag{4.19}$$

$$u_{2,\mathrm{rev}} = U_{\mathrm{DC}} - u_{\mathrm{ZCC1}} \tag{4.20}$$

Appendix B describes the simultaneous solution of the voltage equation pairs of capacitor voltage and voltage derivative at the boundary between t_{a} and t_{fw} periods, and the final solution is a pair of equations for t_{a} and t_{fw}. Their solution requires some intermediate values to be calculated as in Equation 4.21 and 4.22.

$$\begin{aligned} a_1 &= Z_{\mathrm{f}} I_{\mathrm{out}} \\ b_1 &= -u_2 \\ r_1 &= \sqrt{a_1^2 + b_1^2} \\ \phi_1 &= \arctan \frac{b_1}{a_1} \end{aligned} \tag{4.21}$$

$$\begin{aligned} a_2 &= Z_\mathrm{f} I_\mathrm{out} \\ b_2 &= -u_{2,\mathrm{rev}} \\ r_2 &= \sqrt{a_2^2 + b_2^2} \\ \phi_2 &= \arctan\frac{b_2}{a_2} \end{aligned} \tag{4.22}$$

Now, the A-pulse and the FW period can be solved using the new equations:

$$t_\mathrm{a} = \tau_\mathrm{f}\left(\arcsin\left[\frac{u_{1,\mathrm{rev}}^2 - u_{2,\mathrm{rev}}^2 - 2U_\mathrm{DC}u_{1,\mathrm{rev}}}{2U_\mathrm{DC}r_2}\right] + \phi_2\right) \tag{4.23}$$

$$t_\mathrm{fw} = \tau_\mathrm{f}\left(\arcsin\left[\frac{u_1^2 - u_2^2 - 2U_\mathrm{DC}u_1}{2U_\mathrm{DC}r_1}\right] + \phi_1\right) \tag{4.24}$$

The algorithm now exits with full description of the required timing components in the ADUDT pulse pattern. Apart from one numerically solved equation inside the t_{ZCC2} subroutine, the solution is analytical and includes free insertion of ZCC, with ability to remove the A-pulse if required. The use of the algorithm could make dead time constraints easier to handle in the ADUDT sequence.

4.2.1 Behavior of the A-pulse and the FW periods

It might be interesting to analyze the behavior of the t_a and t_fw solutions, as their use together with ZCC can reveal some symmetry within the sequence. Figure 4.9 shows the shape of the t_a and t_fw surfaces as a function of ZCC periods t_{ZCC1} and t_{ZCC2}. The examples are shown for a fixed normalized I_out value of $-0.35I_{\mathrm{f3}}$. Changes in load current value would be seen as z-axis magnitude change and shifting of z-plane interception, but the overall shape of the function surfaces would remain the same.

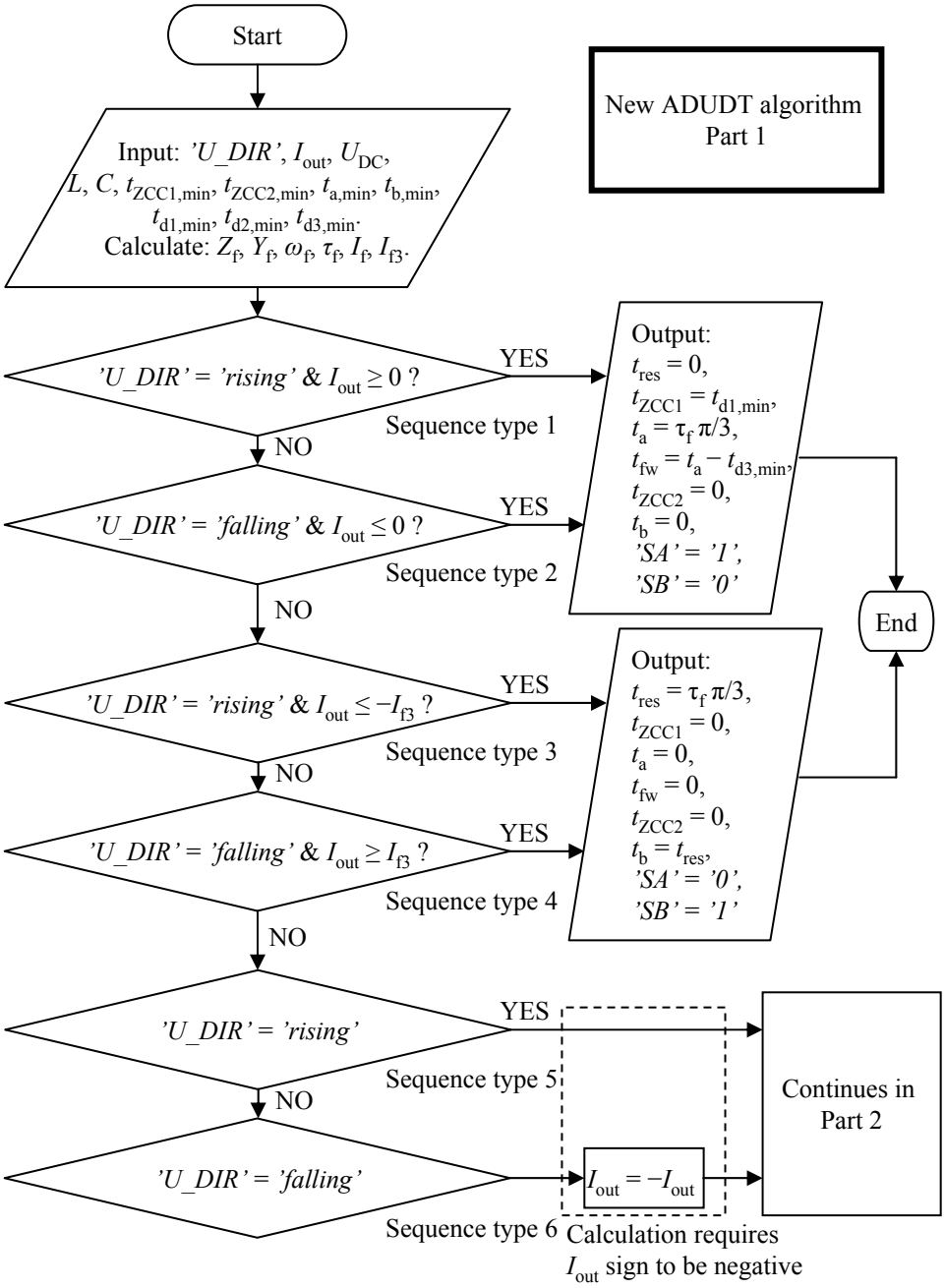


Figure 4.7. First part of the ADUDT pulse pattern solution algorithm. This part covers all the 'easy' sequence cases as shown in Figure 4.6, left column. This first part then redirects to the algorithm part 2 (Figure 4.8), which will handle the 'hard' sequence cases. If ZCC appears, the new proposed equations are used in the solution.

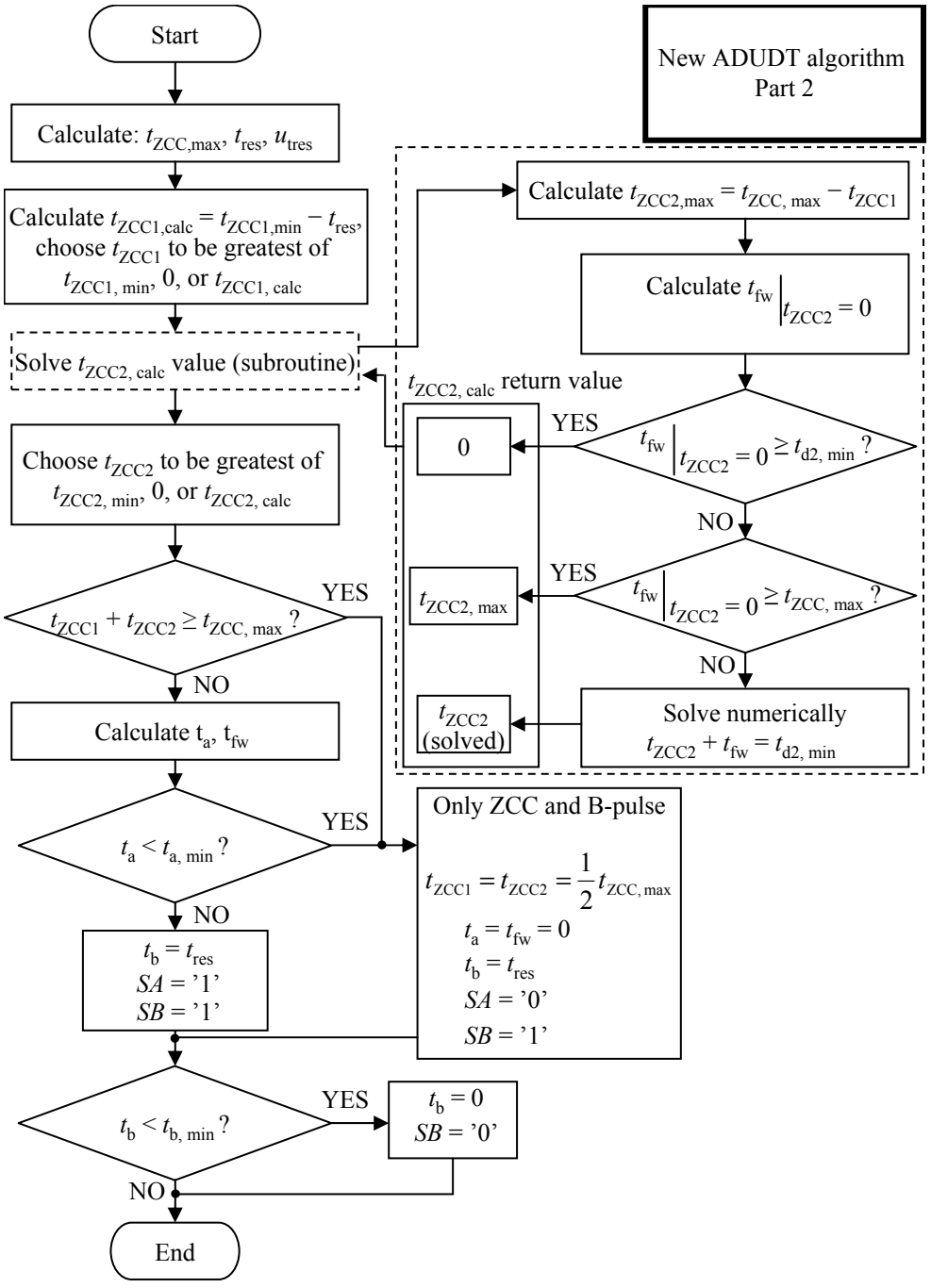


Figure 4.8. Second part of the ADUDT pulse pattern solution algorithm. Here the t_{ZCC1}, t_{ZCC2}, t_a, and t_{fw} periods are solved, and it is also decided whether the A- or B-pulse should be removed.

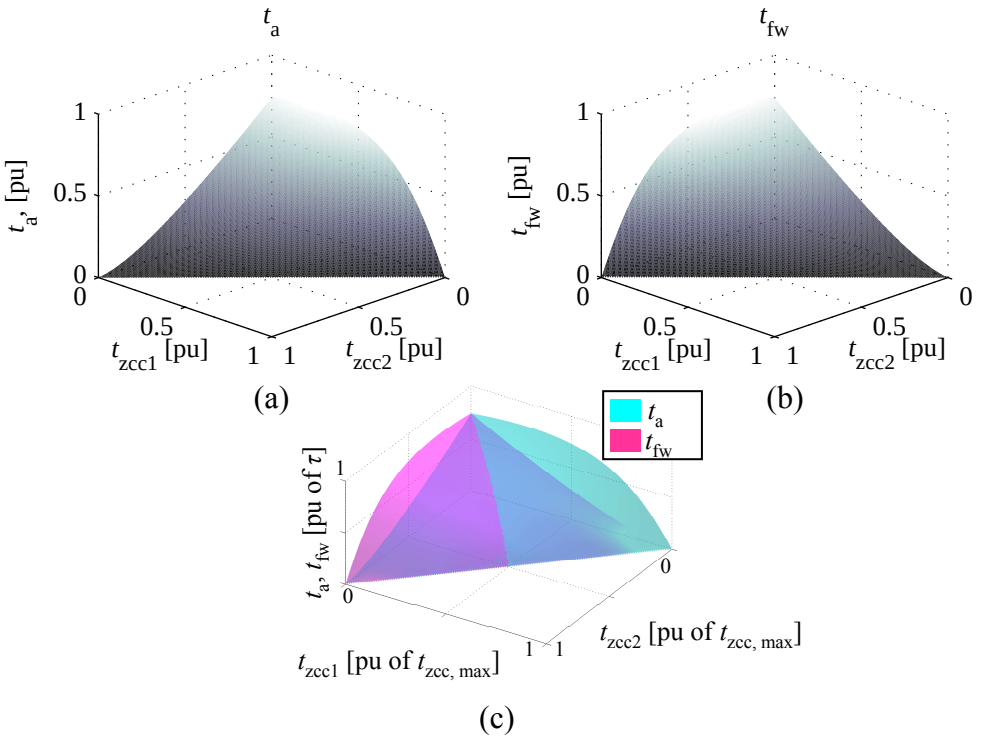


Figure 4.9. Behavior of t_a and t_{fw} width as a function of ZCC periods t_{ZCC1} and t_{ZCC2}. t_a and t_{fw} are mirrored about the $t_{ZCC1} = t_{ZCC2}$ plane.

As can be seen in Figure 4.9, there is a symmetry of t_a and t_{fw} about the t_{ZCC1}=t_{ZCC2}plane, which means the whole sequence would be symmetrical about t_a to t_{fw} boundary (example in Figure 4.4 is quite close to this case). Making t_{ZCC1} and/or t_{ZCC2} shorter requires a change in t_a and t_{fw} values, and the link between the values is shown in the surfaces; it is possible to 'trade' between the ZCC times, as the t_a and t_{fw} periods are adjusted accordingly by the algorithm. If total ZCC time is maximized, then A-pulse is dropped out, and freewheeling period t_{fw} also disappears. This is the $z = 0$ plane intersection line of the surfaces. A conclusion can be made that the t_{ZCC1} and t_a periods can be interchanged with t_{ZCC2} and t_{fw} periods in the sequence, and their dependence on each other is described by the algorithm equations, and constraints set by the operating point parameters. The next section of the algorithm analysis describes the t_{ZCC2} solution subroutine.

4.2.2 Introducing ZCC and dead time limitations

As can be seen in the above steps, the solution for the A-pulse width requires the knowledge of the ZCC time periods. The first ZCC period t_{ZCC1} can be known in advance, because it forms the first blanking time as $t_{d1} = t_{ZCC1} + t_{res}$. However, the second ZCC period t_{ZCC2}

cannot be defined by taking such an approach, because it is a part of the middle blanking time as $t_{d2} = t_{ZCC2} + t_{fw}$. This is because the A-pulse and the freewheeling period were solved as a function of ZCC periods. Before using the equations for the A-pulse and the FW, we first need to solve the value for the ZCC2 period, using the constraint given by t_{d2} and rearranging the FW equation as

$$t_{d2} = t_{fw} + t_{ZCC2} \tag{4.25}$$

This equation is solved for t_{ZCC2}. But first, a simple check for the constraints of the ZCC2 period is made. Because t_{ZCC1} is known, and $t_{ZCC,max}$ applies as described above, the maximum time for the ZCC2 period is

$$t_{ZCC2,max} = t_{ZCC,max} - t_{ZCC1} \tag{4.26}$$

Next, we calculate the limit for t_{fw} as $t_{ZCC2} \to 0$, using the FW equation directly as above, and we get the value for $t_{fw,\,ZCC2=0}$. Now a decision is made:

- If $t_{d2} < t_{fw,\,ZCC2=0}$, it means that the freewheel period can be longer than the required minimum value of t_{d2}, which means that there is really no need for t_{ZCC2} greater than zero. The B-pulse can start immediately after the FW period.
- If the requirement for t_{d2} is such a large value that the maximum ZCC period limit is hit, the sequence cannot contain the A-pulse anymore. In other words, if $t_{d2} > t_{ZCC2,max}$, the A-pulse is disabled, and the total ZCC time is to be $t_{ZCC,max}$.

In any other case, we must solve t_{ZCC2} by using the equation (4.25) above. So far, there is no analytical solution available for this equation, and a numerical solution is used. It should be possible to solve the equation analytically, and this could be a topic for future study.

After having the solution for the ZCC2 period, the algorithm can return to solving the A-pulse and the FW periods. The solution for ZCC2 as shown above is the minimum required for a succesful filter control, meeting the original t_{d1} and t_{d2} limits. However, it is possible to set a minimum allowed width for ZCC2 itself. The same applies to ZCC1, as a value based on $t_{d1} = t_{ZCC1} + t_{res}$ can result in very short durations for the ZCC1 period when the inductor current reset period end meets with the A-pulse beginning. The same applies to ZCC2, as the zero current clamp period between the FW and B-pulse approaches zero as the FW period end meets with the B-pulse start. It is possible that such low values for ZCC periods are to be avoided, for reasons not known yet. Thus, any value calculated for the ZCC periods can be overriden with larger values, and thus, the algorithm once again checks if the total ZCC time would violate the maximum of $t_{ZCC,max}$. If it happens, the A-pulse must be removed to obey the ZCC limit, as removing the A-pulse gives more time for the ZCC periods within the sequence. This happens as follows:

- If $t_{\mathrm{ZCC1,min}} + t_{\mathrm{ZCC2,min}} \geqslant t_{\mathrm{ZCC,max}}$, then $t_{\mathrm{ZCC,max}}$ is equally divided between the ZCC1 and ZCC2 periods, and the A-pulse is disabled, also removing the FW period.
- Else, the durations of ZCC1 and ZCC2 follow the minimum values defined by $t_{\mathrm{ZCC1,min}}$ and $t_{\mathrm{ZCC2,min}}$, respectively. The A-pulse is still used, and there will be the FW period also.

If the A-pulse had to be removed because of a ZCC limit violation, then $t_{\mathrm{a}} = 0$, $t_{\mathrm{fw}} = 0$, using $t_{\mathrm{ZCC,max}} = t_{\mathrm{ZCC1}} + t_{\mathrm{ZCC2}}$ the values for ZCC1 and ZCC2 are chosen (the sum matters, but the balance does not as there will be only one long ZCC period), the A-pulse is not used, but most importantly, the B-pulse is still applied, with the duration of $t_{\mathrm{b}} = t_{\mathrm{res}}$.

In the other case of still using the A-pulse after the ZCC period check, the algorithm proceeds to using the equations for t_{a} and t_{fw} above. Now, it is perfectly possible to hit the minimum limit for the A-pulse width. If the time period t_{a} becomes too short, and it is desirable to be avoided, it must once again be removed, and the algorithm reverts to the identical steps as for the ZCC violation case, as described above.

4.3 Using the algorithm

As can be seen, the pulse sequence is quite flexible in terms of using ZCC periods and the A-pulse. Setting limits for the blanking times and the A-pulse width can be handled, as both the ZCC periods and the A-pulse can be used to control the filter state during the sequence. However, this does not apply to the B-pulse, as it is the only period capable of restoring the filter current state back to the load current value at the end of the pulse sequence. The B-pulse cannot be replaced, for its function in the filter state control is unique. If there is a limit for the minimum width of the B-pulse, $t_{\mathrm{b,min}}$, the B-pulse must be simply discarded, resulting in a certain amount of residual filter oscillation after the ADUDT sequence. But, as can be seen in the sequence waveform figures e.g. 4.4, the low values of t_{b} occur with low values of I_{out}, usually resulting in rather low-amplitude residual oscillation as in Figure 2.16. In practical applications, this might not pose a serious problem as the filter always has some amount of damping. But in theory, with low-damping factor filters, there is a potential for filter instability.

Any correction for nonideal delay effects has to be included separately. It is not possible to directly see the timing distortion effects from the ADUDT algorithm equations. A hypothesis is that pulse timing distortion can negate much of the advantages brought by the algorithm, reducing the potential of the method. The parameters of the algorithm affect the structure of the sequence solution, and the inclusion of ZCC is hypothesized to give some advantage in case the timing distortions are present. This will be tested with simulations in the next chapter. The development version of the algorithm was also tested in the test setup, and results are discussed later. In the test setup implementation, the algorithm was calculated in real-time, for each PWM pulse edge.

Chapter 5

Results

In this chapter, the test results relating to the ADUDT filter output voltage and motor terminals are shown. A simulation model is used to study the timing distortion effects, and filter output voltage and motor terminal voltage measurements are conducted to verify the operation of the new control algorithm in actual motor drive applications. Finally, the ADUDT method losses and performance are compared with the traditional output filtering methods. The following issues were to be addressed by the simulation and measurement results:

- Using the timing distortion data from the test setup as a case study, how does the filter output voltage depend on the phase leg output timing distortions?
- What is the role of ADUDT algorithm parameter variations in the operation under timing distortions?
- When the filter L and C have deviations, and there is some error in the I_{out} and U_{dc} values, how sensitive is ADUDT under such conditions?
- Using synthetic delay values in the simulator, could the effect of individual IGBT timing deviation be located and recognized?
- Does the algorithm operate with similar performance as the simulation model in an actual IGBT inverter, with the motor cable and motor connected, running at various load current values?
- Can ADUDT work as an effective du/dt and motor terminal overvoltage limitation method, and how it compared with the methods used previously in industrial applications?
- How effective should a fixed delay compensation value be in order to decrease the overshoot envelope?

- ADUDT is already known to increase the losses in the inverter, and therefore, the losses should be investigated, including the ADUDT filter. How do the ADUDT method losses compare with the traditional output filtering methods?

The results involve a case study of one particular variable-speed AC drive. Measured timing data and the phase leg delay behavior were presented in Chapter 3, which is valid for this case study. Thus, any generalizations based on these results have to be carefully evaluated.

5.1 Simulations of timing distortion effects

The study of the phase leg output voltage timing distortion aims at providing knowledge on how the test setup would behave when using the ADUDT. Instead of measuring the filter output voltage directly with the test setup, the phase leg output timing data are used with a simulation model. The model simulates the delay effects and contains the voltage and current equations describing the state behavior of the ADUDT LC filter. Using the virtual delays based on the test setup measurements, the simulated filter output voltage would then show how the timing distortion affects the filter output, isolating all other possible error sources from the process. This was considered important as the actual filter and the VFD construction contain resistance and potentially depend on the filter inductor construction. The reason for using a phase leg and filter simulation model was thus to provide a case where only the timing distortion would matter. Effects such as the DC link voltage and load current deviations could be tried by model parametrization. The filter inductance and capacitance values could also be varied to see the possible effects of filter tolerances. Using the simulation method allows easier variation of all parameters in the study. It also enables direct alteration of the delay behavior, making it possible to set up a 'what if' scenario with the phase leg delays. This would be more difficult with actual phase leg electronics.

There are also drawbacks in the simulation method. These limitations are basically the same as in the control pulse pattern solution algorithm. The model does not contain any kind of resistance in the filter or the phase leg. The filter inductance is assumed linear over the whole current range. The load side of the filter is assumed an ideal current source, where the motor cable transmission line and then load impedance would appear in reality. The model does not contain any parasitic effects. Thus, it assumes that the measured and modeled virtual edge delay is sufficient to describe the phase leg output behavior. All the simplifications made in the model were also applied when solving the pulse pattern algorithm equations, and thus, the model has exactly the same limitations as the ADUDT algorithm.

The simplified structure of the simulation model is shown in Figure 5.1. More detail is provided in Appendix D. A phase leg simulator gives the ADUDT filter output voltage and current waveforms, and an external script stores the peak voltage values (overshoot values for rising and falling output voltage edges). The filter output voltage is the principal figure-of-merit for the timing errors. If the pulse pattern has no distortion effects, the output voltage has no overshoot. The key idea is now to simulate a load current sweep and analyze the

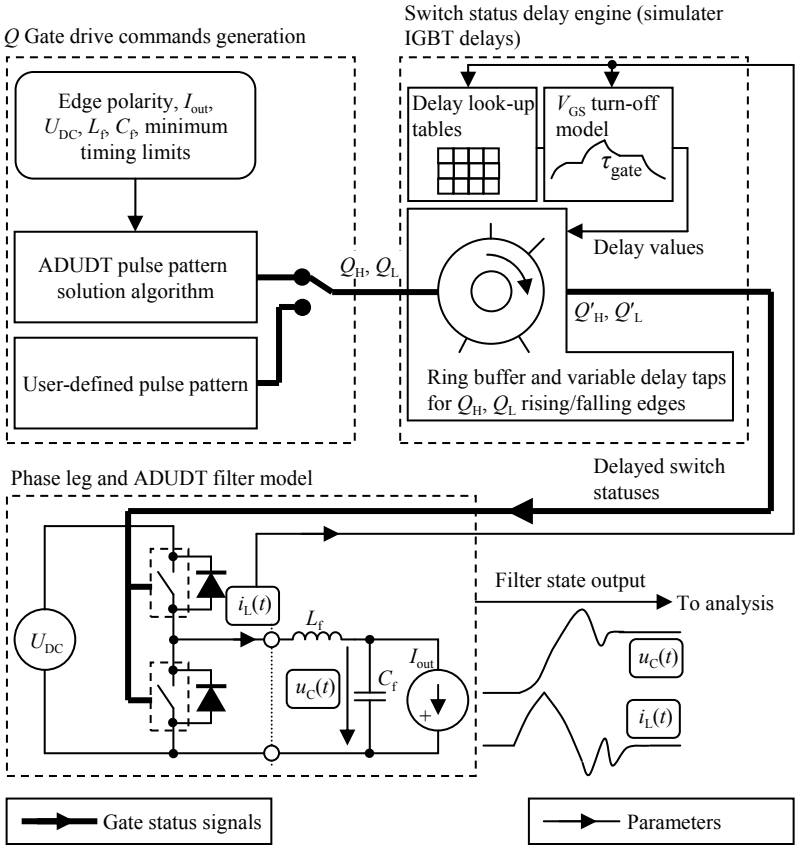


Figure 5.1. Script-based phase leg simulator produces the ADUDT control pulse pattern, distorts the pulse timing according to the measured/modeled delays, and drives a state model of the phase leg switches, diodes, and the ADUDT filter.

output voltage overshoot, when the timing distortion effects and/or parameter variations are introduced in the simulation model. The total overshoot envelope area is then the ultimate figure-of-merit, making possible the meaningful comparisons of output voltage results. This overshoot envelope can be examined by its total area and perhaps the largest positive and negative peak values. The envelope can be reproduced in direct measurements by producing a load current sweep. The method for the overshoot envelope analysis is shown in Figure 5.2.

Some parameters in the simulations are considered as default, and any deviation in the following simulations is indicated separately. The default parameters are given in Table 5.1. The gate voltage turn-off model parameters are given in Appendix A. The default settings always use the turn-on voltage delay based on the measured and interpolated timing look-up table method and the u_G model for the turn-off voltage edge. The algorithm is allowed to produce both A- and B-pulses as required.

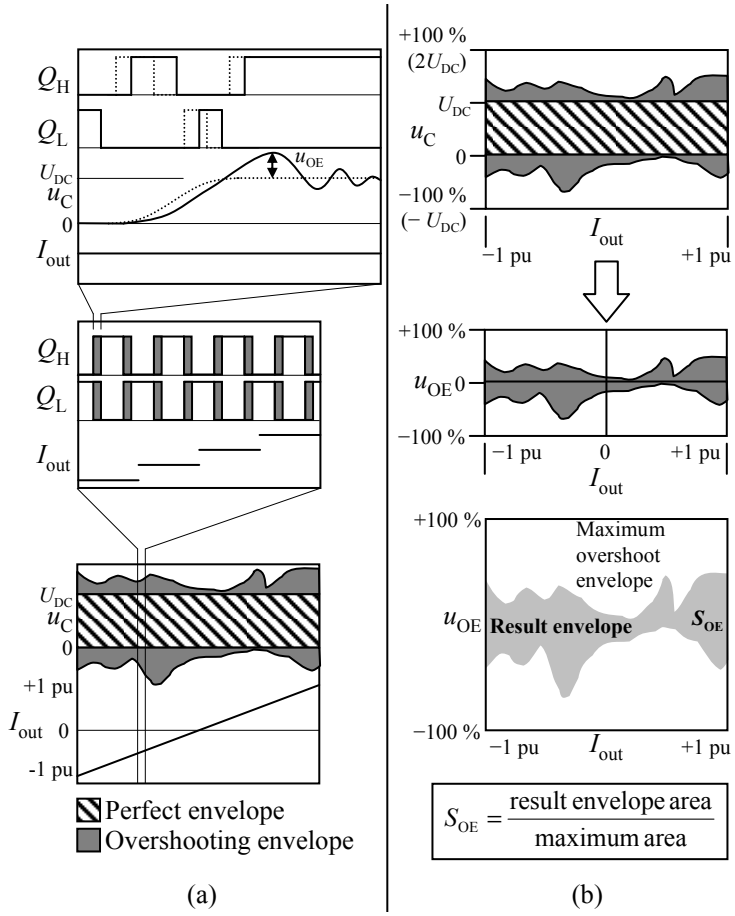


Figure 5.2. (a) Load current value I_{out} is swept between the maximum peak values, and both the rising and falling output voltage edges are produced with the ADUDT. The errors in the pulse pattern cause an overshoot in the filter output voltage. The sweep results are postprocessed as shown in (b). The perfect envelope is removed from the u_C peak value envelope, and the remaining overshoot envelope is normalized to the maximum, worst-case envelope. The result is an overshoot figure-of-merit S_{OE}.

In contrast to the algorithm-based and load-current-tracking ADUDT pulse sequence, a fixed pulse pattern was also investigated. Two pattern structures were used. The first pattern *FIXED1* had a rather naive setting based on minimum dead times and t_a at zero current. The second constant sequence *FIXED2* has the dead time subtracted from the A- and B-pulse widths, and this modification was found to produce the smallest possible S_{OE} value for the fixed pattern case. The pattern timing data are given in Table 5.2.

The first simulation run tests whether the algorithm can bring zero overshoot if no delays are involved and how the timing distortion affects the S_{OE} figure. A comparison with fixed pattern results was also tested. The results are shown in Figure 5.3.

Table 5.1. ADUDT algorithm default parameters.

Parameter	Value
DC link voltage U_{DC}	600 V
Load current I_{out} peak value	80 A
IGBT/Diode temperature	25 °C
Filter inductance L	15 µH
Filter capacitance C	330 nF
Minimum t_{ZCC1} value	0
Minimum t_{ZCC2} value	0
Minimum t_a value	0.8 µs
Minimum t_b value	0
Minimum t_{d1} value	1 µs
Minimum t_{d2} value	1 µs
Minimum t_{d3} value	1 µs

Table 5.2. Constant sequences used in the simulations.

Parameter	Value
FIXED1	
t_{d1}	1 µs
t_a	2.33 µs
t_{d2}	1 µs
t_b	2.33 µs
t_{d3}	1 µs
FIXED2	
t_{d1}	1 µs
t_a	1.33 µs
t_{d2}	1 µs
t_b	1.33 µs
t_{d3}	1 µs

In Figure 5.3(a), the S_{OE} would be expected to have $S_{OE} = 0$, if the algorithm worked correctly. It was found that the simulation time step of 5 ns presents enough timing deviation so that S_{OE} is not exactly zero. Thus, we may conclude that the algorithm is working properly. In Figure 5.3(b), the measured and modeled timing distortions are included, using the measured look-up tables and the u_G model as described above. Now, the S_{OE} value increases as the phase leg output voltage timing is distorted in contrast to the algorithm solution. It is worth noting that for some current values, the overshoot envelope has a low magnitude, which is due to the delays matching more closely (for matched delays in all edges, the result is zero overshoot,

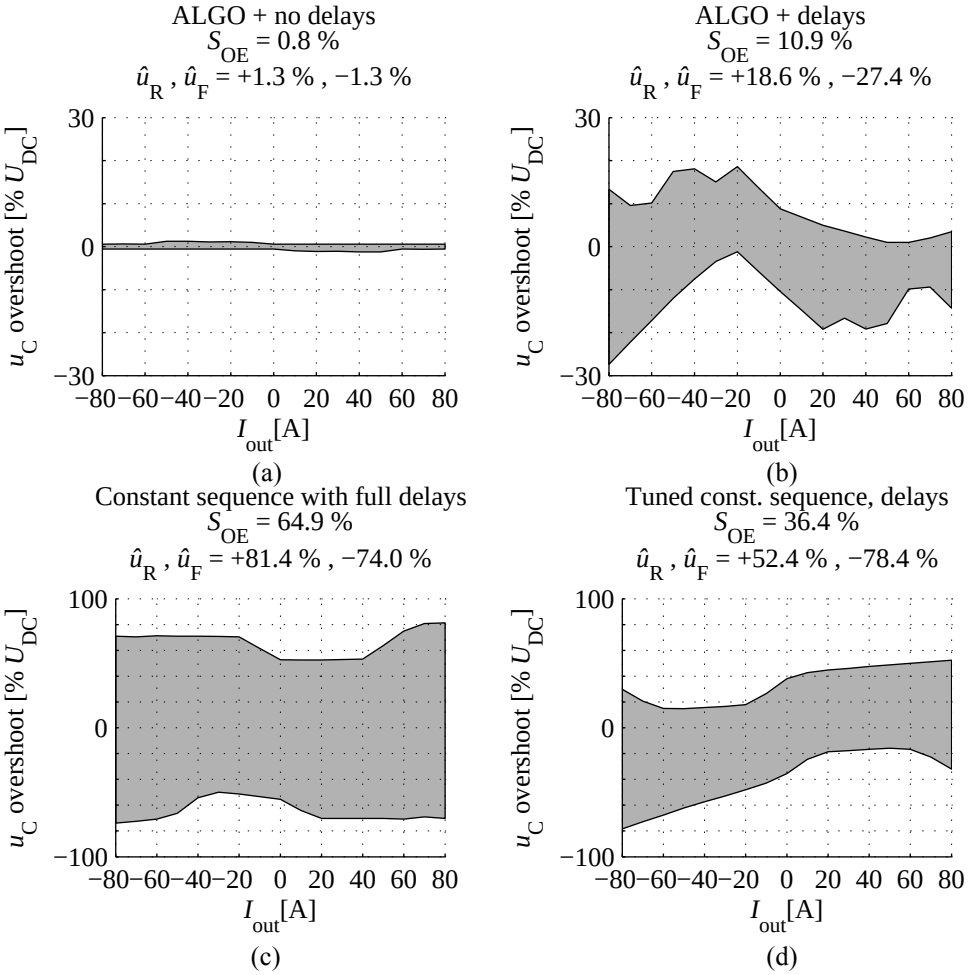


Figure 5.3. (a) Algorithm with no delays, (b) algorithm with delays, (c) constant sequence *FIXED1* (with delays), and (d) constant sequence *FIXED2* (with delays).

as described later). The constant sequence method does not seem to be competitive in terms of S_{OE} and peak overshoot values, as is shown in Figures 5.3(c) and (d).

The question of the turn-off delay being dependent on pulse width can be speculated, and the results without the u_G model are shown in Figure 5.4(a). It seems that the u_G-dependent turn-off delay introduces such a matching effect in the delays that it is actually beneficial for the S_{OE} figure, as simulating without the u_G model increases S_{OE}.

Another possible adjustment to sequence parameters is to increase the ZCC times and give less role for the A-pulse in the filter operation. The motivation is to use ZCC since it should be more accurate in timing than the A-pulse, as ZCC is formed naturally unlike the active turn-

on and turn-off of the A-pulse. The ZCC extension (A-pulse limitation) results are depicted in Figures 5.4(b)–(d). S_{OE} decreases slightly, but the peak overshoot values remain unchanged compared with the default algorithm case.

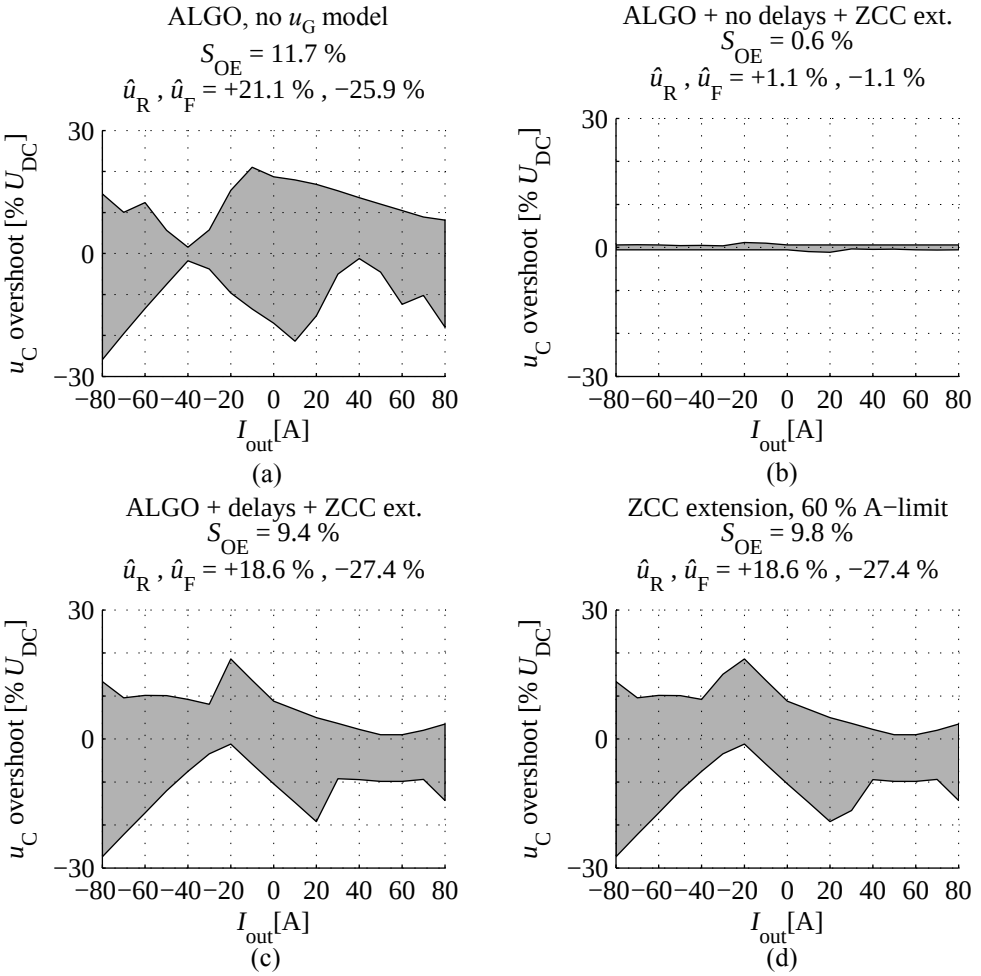


Figure 5.4. (a) Algorithm with delays but no u_G turn-off model, (b) algorithm with the minimum t_a limit of 80% of $\frac{\pi}{3}\tau_f$ without delays, (c) algorithm with the 80% $t_{a,min}$ repeated with delays, (d) algorithm with the 60% $t_{a,min}$ limit with delays.

Dead time can also be changed to see if it brings any improvement to the overshoot envelope. This also results in a ZCC period increase within the ADUDT sequence, and a similar improvement in S_{OE} can be expected as with the A-pulse limitation. The results are shown in Figure 5.5.

It is also possible to test if the removal of the A-pulse minimum limit improves the S_{OE}. This is shown in Figure 5.6(a). This actually results in a slight increase in S_{OE}. The results

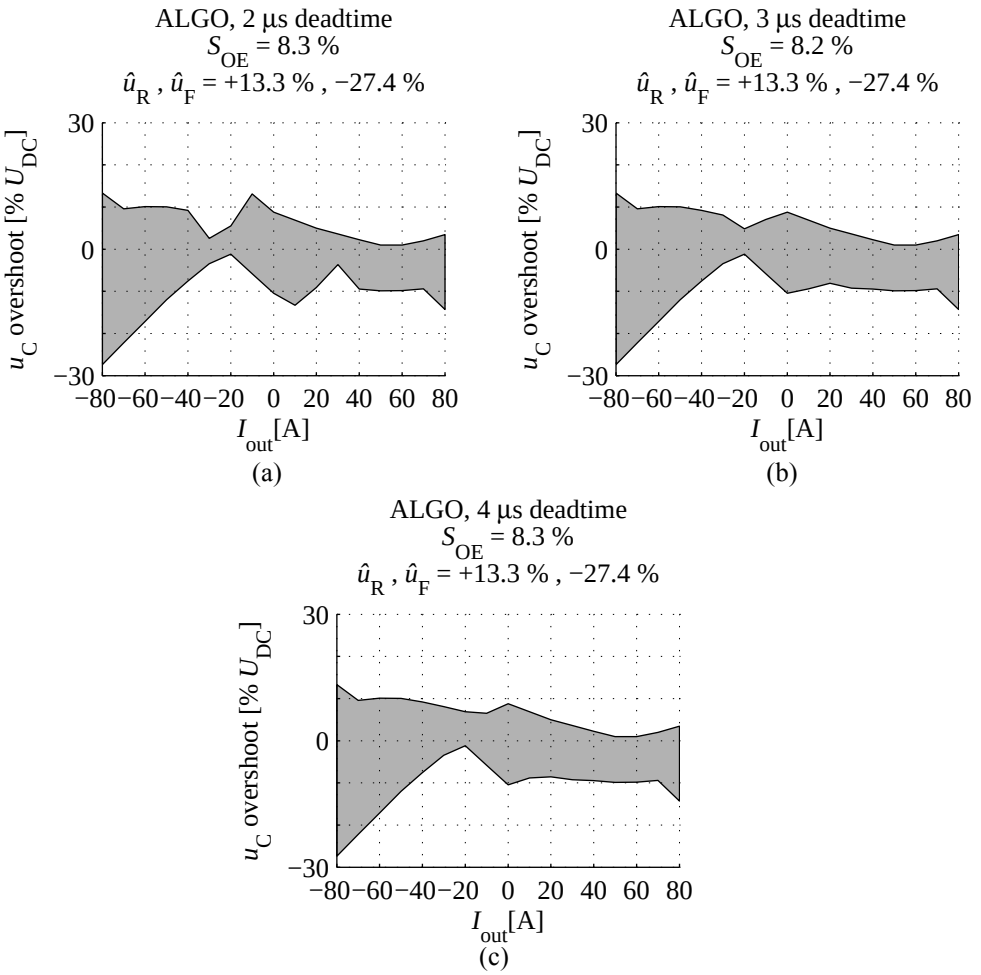


Figure 5.5. (a) Extending the dead time to 2 µs, (b) 3 µs, and (c) 4 µs. This results in a ZCC period increase within the sequence. Compared with the 1 µs dead time case above (the default parameters), the dead time increase helps initially, but a further increase gives no extra advantage.

suggest that using ZCC in the ADUDT sequence is beneficial when trying to overcome the timing distortion effects. However, the B-pulse limitation does not work in a similar manner, since the B-pulse is actively used to compensate the load current at the end of the ADUDT sequence, and is essentially required. The B-pulse is indispensable in this role. Thus, all limitations to the B-pulse implementation are expected to increase the S_{OE}. The results are illustrated in Figures 5.6(b)–(d).

The load current I_{out} and the DC link voltage U_{DC} are usually expected to have some uncertainty in their value. Some effect in the ADUDT operation can be expected if the actual I_{out} and/or U_{DC} values deviate from the value used in the ADUDT algorithm calculations.

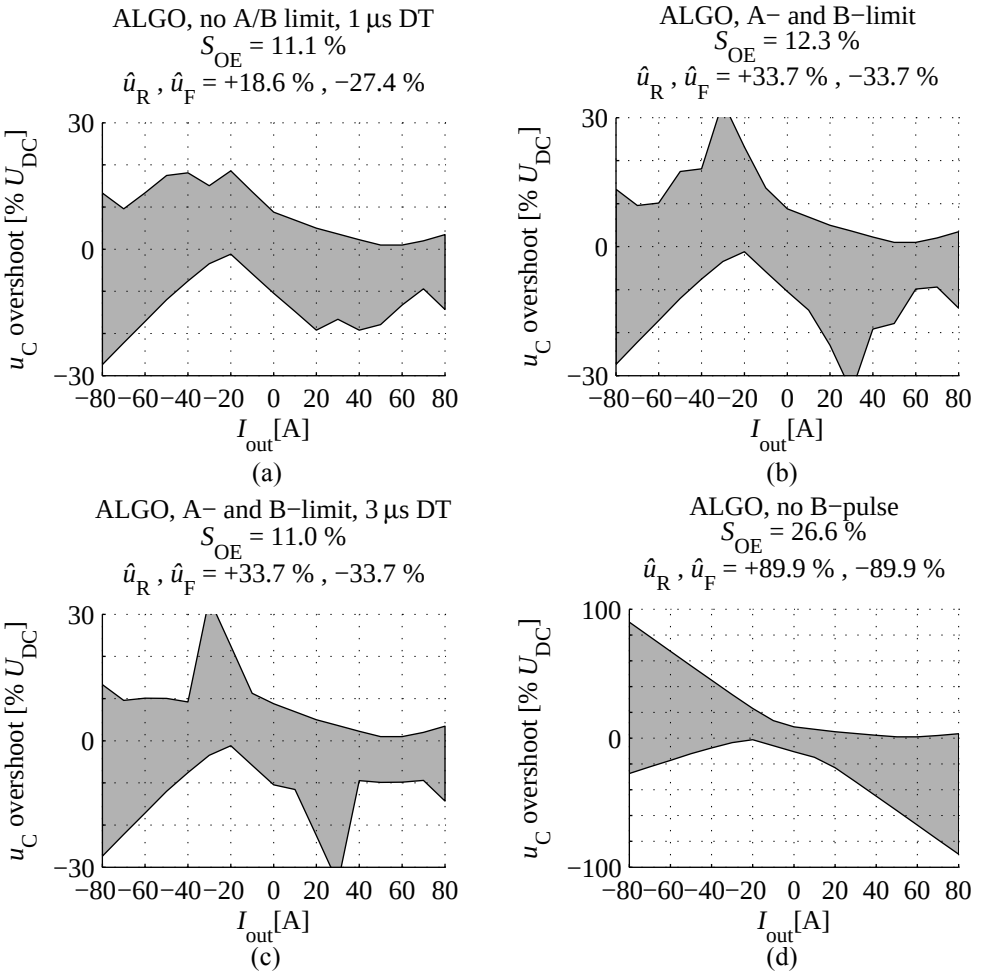


Figure 5.6. (a) A-pulse minimum limit is removed, and this does not give any improvement to the S_{OE} figure (but a slight increase compared with the 10.9% S_{OE} with the default parameters). In (b), both the A- and B-pulse have a 0.8 µs minimum limit, and the B-pulse drop-out results in an increased S_{OE}. (c) improves the figure by using a larger dead time value, but the peak overshoot values remain unchanged. Dropping out the B-pulse completely naturally results in an uncontrolled overshoot and a bad S_{OE} because of the lack of load current compensation within the sequence.

This deviation was simulated, and the results are shown in Figure 5.7. As a 10% deviation in either I_{out} or U_{DC} is rather large in terms of measurement electronics found in actual VFDs, the conclusion is that the effect can be neglected in normal applications.

Similarly, the filter inductance and capacitance are expected to deviate from their nominal value. The inductance could be nonlinear in nature, which could not be directly simulated in the model, but a static deviation could be simulated. Deviations up to 20% in L and/or C were used. It was found that any operation that leads to a τ_f deviation produces a rapid increase in

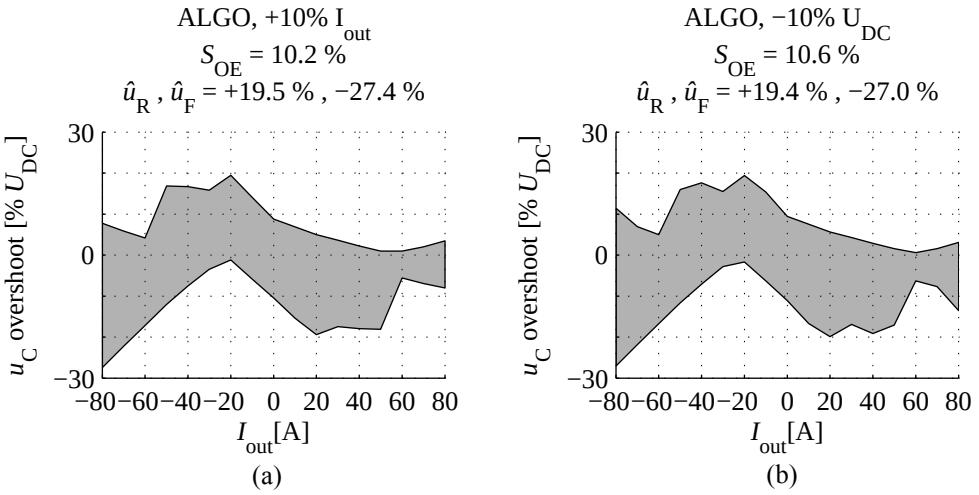


Figure 5.7. 10% deviation in load current or U_{DC} value does not result in a significant overshoot error.

S_{OE}, but if L and C change in such a manner that τ_f value is conserved, the effect is minimal. The results are given in Figures 5.8 and 5.9.

All the S_{OE} results are gathered in Table 5.3. The boldface row is the case with algorithm and full delays, using default parameters. This can be considered the reference case and would be the expected result in actual test setup measurements.

It is reasonable to ask how much S_{OE} and peak overshoot would be tolerable in the VFD application. Using default parameters, the timing distortion gives an S_{OE} value of 10.9% and peak overshoot magnitudes less than 30 %. The criteria for the overshoot envelope shape have to be defined first if the overshoot effects and their severity is to be evaluated. One comparison can be drawn from passive du/dt output filters and their inherent overshoot behavior. The reference passive du/dt filter used in the loss comparison tests discussed later has an overshoot of 58 %, appearing for every output voltage step. Since the overshoot is constant, it would compare as having S_{OE} of 58 %. This is a considerably larger value than what is caused by timing distortions in the simulated ADUDT case with the default parameters. If the criteria for S_{OE} were relaxed enough, no further measures would have to be taken to reduce the overshoot envelope. If, however, the application requires overshoot levels approaching zero, some kind of delay compensation has to take place, perhaps combined with an increased ZCC use in the ADUDT sequence. Overshoot results obtained from the actual VFD test setup measurements are presented later.

Looking at Table 5.3, the improvement in the S_{OE} value when trying different parameter changes is rather small. The peak overshoot values could not be decreased effectively. Using fixed ADUDT pulse patterns over the full load current range gives generally a poor S_{OE} figure. It is possible to use a set of fixed ADUDT patterns that change as the load current value hits a certain threshold, effectively working as the algorithm but with quantized I_{out} value steps. This comparison was not included and could be in the scope of future work. Based on the

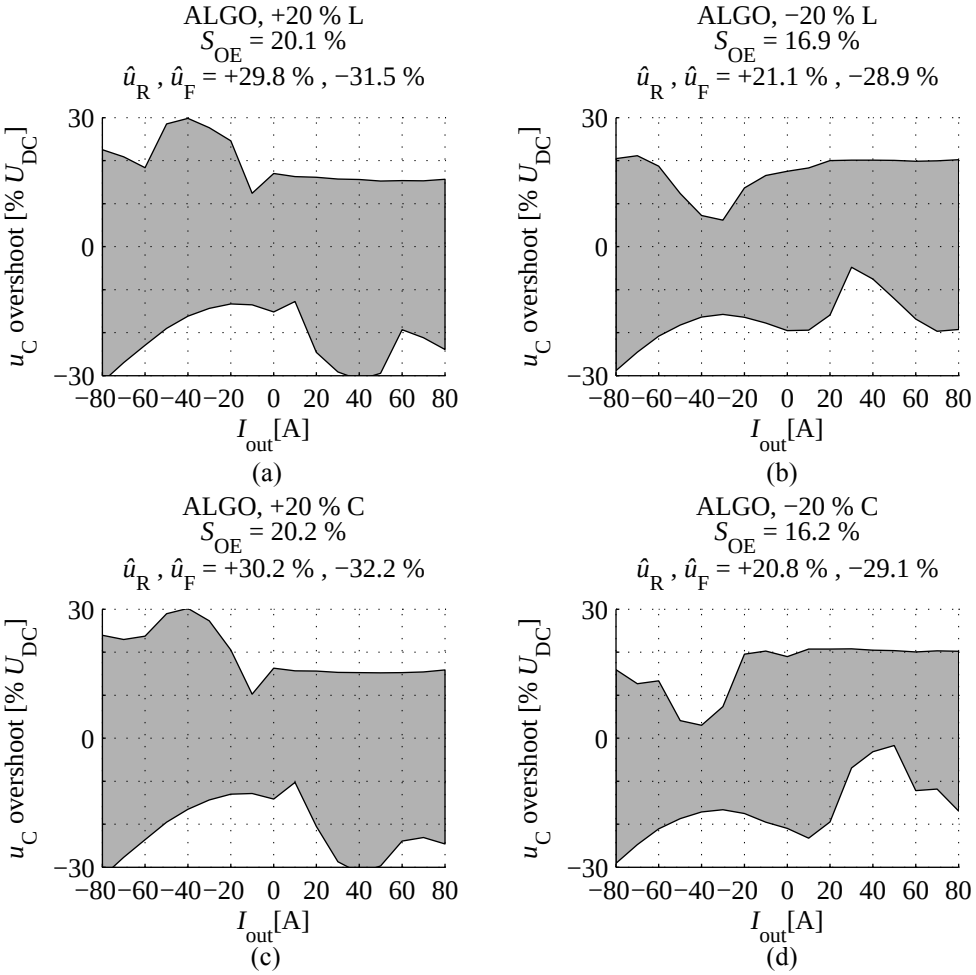


Figure 5.8. 20% deviation of either L or C results in a significant S_{OE} increase.

results shown here, it is concluded that the algorithm with the B-pulse is the best option to give the lowest overshoot envelope values, even with the timing distortion effects included.

Overshoot envelopes produced by the measured/modeled delays do not reveal the behavior of overshoot per individual output voltage edge delay. When using full delay modeling, it is not possible to directly assess why certain characteristics appear in the overshoot envelope. This was found to be one point of interest, that is, to investigate how each edge timing deviation can affect the S_{OE} figure. By using arbitrary delays for each voltage edge timing, a synthetic delay simulation could be produced. It was expected to reveal something about the nature of the overshoot caused by timing distortion, and in such a way that individual edges could be analyzed. The principle and results are shown in Figure 5.10.

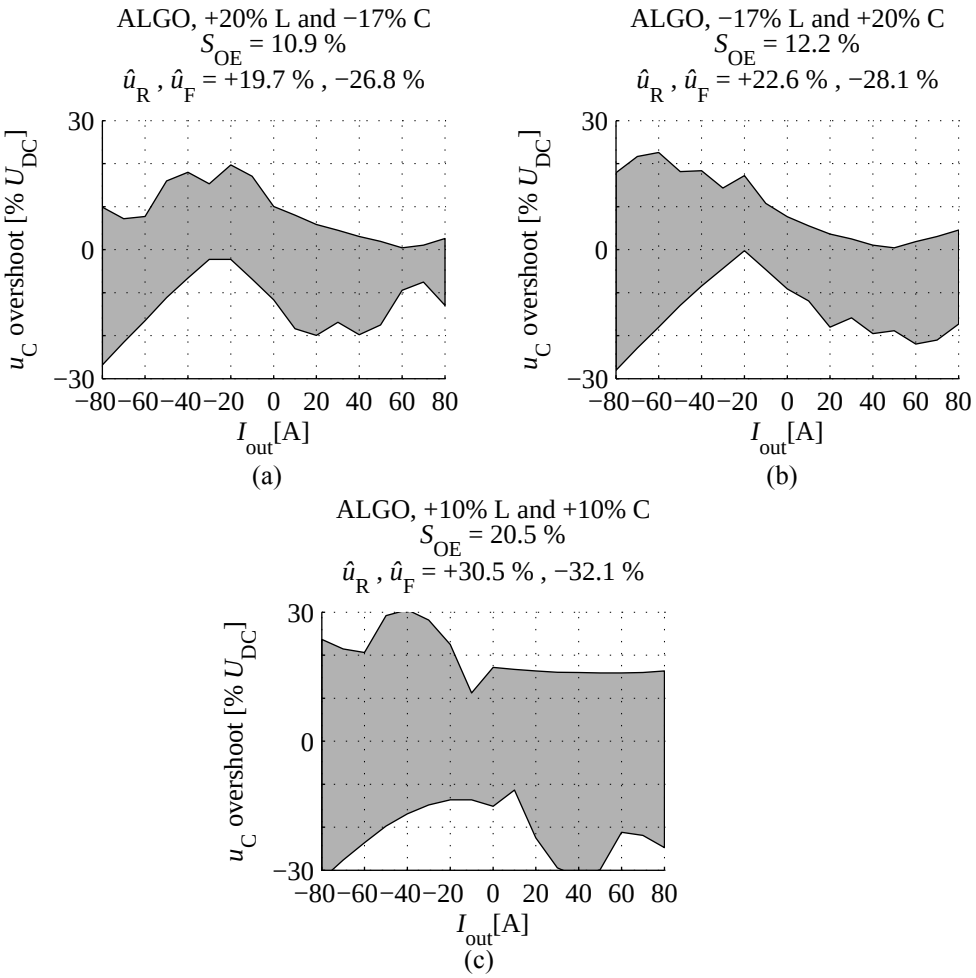


Figure 5.9. (a) and (b), compared with Figure 5.8, the deviation in filter component values does not cause a significant S_{OE} change if the L and C change in such a way that τ_f remains unchanged.

As expected, the timing delays do not cause any overshoot effect if all the edges have the same delay. This means that delay minimization is not necessarily the objective of the ADUDT performance tuning, but matching of the delays is desirable. Then, again, it can be questioned whether the dead times could be minimized, if the delays were known in advance. With minimized dead times the ZCC periods are removed, and assuming no pulse width limitation, the algorithm solution approaches the zero ZCC sequence. This would have the remarkable effect of actually removing the need for an algorithm (since the zero ZCC sequence has a constant shape if the A-pulse and the B-pulse can be made with zero dead times). At the same time, the accurate delay compensation would become more important. Investigating the delay compensation methods would be the scope of the future work.

Table 5.3. All the S_{OE} results gathered. Uncertainty analysis can be found in Appendix C.

Figure	ALGO	Delays	Custom parameters	S_{OE}[%]	$\hat{u}_R$[+%]	$\hat{u}_F$[−%]
5.3(a)	Yes	-	-	0.8	1.3	1.3
5.3(b)	**Yes**	**LUT + u_G**	**-**	**10.9**	**18.6**	**27.4**
5.3(c)	-	LUT + u_G	*FIXED1*	64.9	81.4	74.0
5.3(d)	-	LUT + u_G	*FIXED2*	36.4	52.4	78.4
5.4(a)	Yes	LUT	-	11.7	21.1	25.9
5.4(b)	Yes	-	$t_{a,min}$80%	0.6	1.1	1.1
5.4(c)	Yes	LUT + u_G	"	9.4	18.6	27.4
5.4(d)	Yes	LUT + u_G	$t_{a,min}$60%	9.8	18.6	27.4
5.5(a)	Yes	LUT + u_G	dead times 2 µs	8.3	13.3	27.4
5.5(b)	Yes	LUT + u_G	dead times 3 µs	8.2	13.3	27.4
5.5(c)	Yes	LUT + u_G	dead times 4 µs	8.3	13.3	27.4
5.6(a)	Yes	LUT + u_G	$t_{a,min}$0	11.1	18.6	27.4
5.6(b)	Yes	LUT + u_G	$t_{a,min}$, $t_{b,min}$ 0.8 µs	12.3	33.7	33.7
5.6(c)	Yes	LUT + u_G	", 3 µs dead times	11.0	33.7	33.7
5.6(d)	Yes	LUT + u_G	B-pulse disabled	26.6	89.9	89.9
5.7(a)	Yes	LUT + u_G	I_{out}+10% (deviation)	10.2	19.5	27.4
5.7(b)	Yes	LUT + u_G	U_{DC}−10%	10.6	19.4	27.0
5.8(a)	Yes	LUT + u_G	L +20%	20.1	29.8	31.5
5.8(b)	Yes	LUT + u_G	L −20%	16.9	21.1	28.9
5.8(c)	Yes	LUT + u_G	C +20%	20.2	30.2	32.2
5.8(d)	Yes	LUT + u_G	C −20%	16.2	20.8	29.1
5.9(a)	Yes	LUT + u_G	L +20% / C −17%	10.9	19.7	26.8
5.9(b)	Yes	LUT + u_G	L −17% / C +20%	12.2	22.6	28.1
5.9(c)	Yes	LUT + u_G	L +10% / C +10%	20.5	30.5	32.1

In Figure 5.10, another interesting effect can be seen in the left column with low S_{OE} values of 4.8 %. This is a result of matched turn-on and turn-off delays in the switches, but the high-side and the low-side having a different delay value in total. No overshoot appears in the sequences where only one side switch is used (i.e. only the A-pulse involved). This is demonstrated as zero overshoot in the upper right and lower left quadrant of the overshoot envelope figure. When the B-pulse is required in the sequence, the timing distortion starts to introduce some overshoot. Then, still observing the results in the left column, all the delay settings that produce pulse width distortion within the switches give a high overshoot, even for sequences using only the A-pulse (top right/lower left quadrant). In the right column, only one edge delay is different from the remaining three. Once again, the most severe effect is observed for the A-pulse-only sequences, but this time only one quadrant has this effect per time, as the remaining edge delays are matched. For combined A- and B-pulse sequences (top left/lower right quadrants), the overshoot envelope is a function of load current.

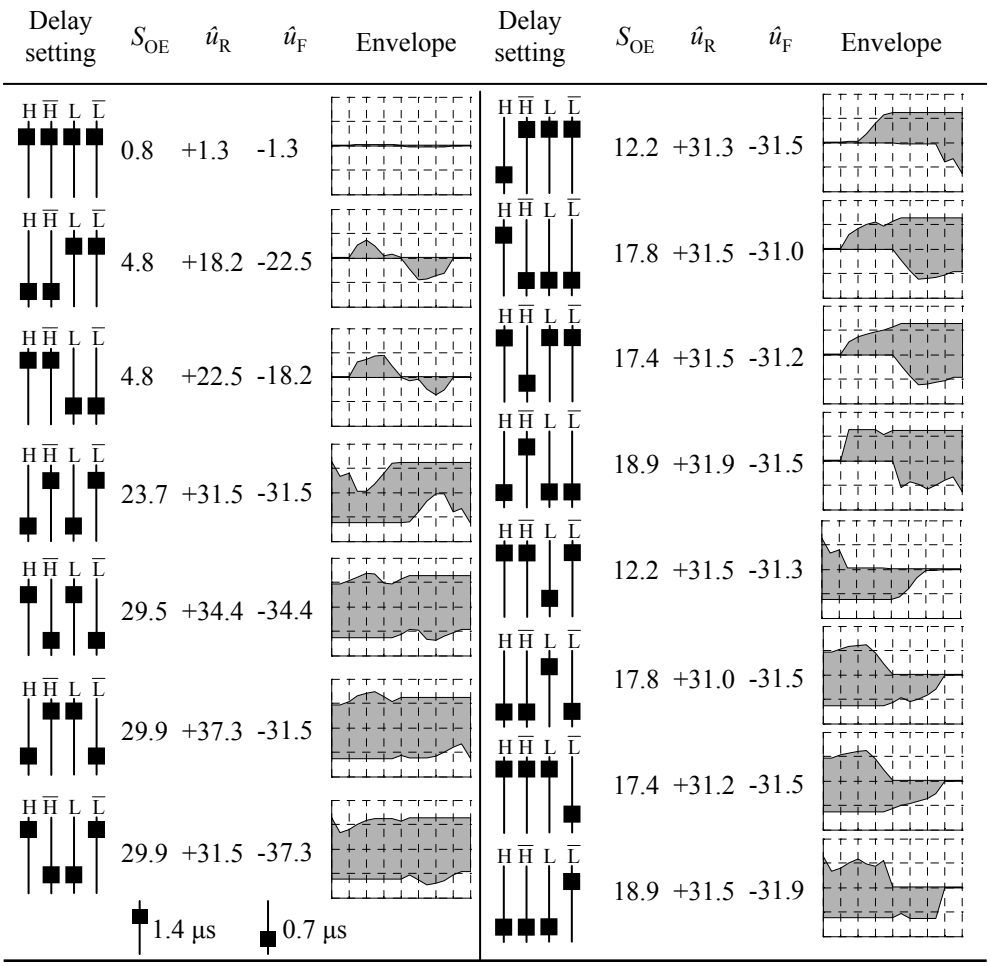


Figure 5.10. Synthetic delay values were used to investigate the general relation of the IGBT timing to the ADUDT output voltage. The simulation uses default algorithm parameters, but arbitrary voltage edge delays as shown. In the left column, two edges out of four are delayed, plus the reference case of identical delays. If all the voltage edge delays are identical, there is no overshoot error. Having either low-side or high-side switch delayed at both edge polarities in relation to the other side switch results in a relatively small S_{OE} error. All the other cases have a considerably larger S_{OE} value.

These observations give some explanation why the large overshoot value is observed in the simulated cases for the A-pulse sequences. The reason is that since the turn-on and turn-off delays are not matched for the switch in effect, the result is a pulse width error within the sequence, and thus, an overshoot increase. It is now clear that any form of delay matching would be beneficial for the ADUDT operation. This matching would have to operate in the delay path from the logic-level gate drive command to the phase leg output voltage edge.

5.2 ADUDT performance tests using a three-phase test setup

In Chapter 3, the setup was used to gather the timing data in order to construct a timing distortion model for simulation use. The ultimate goal was to implement the ADUDT method in the test setup such that filtering operation could be verified with the motor cable and the motor load attached. Actually, the implementation of the ADUDT control was first tested in a motor application, and the deeper analysis provided in Chapter 3 and overshoot envelope simulations were carried out after the motor and cable tests. In the course of this study, the ADUDT algorithm was developed into its present form. The initial version used in the test setup measurements presented here had one limitation and parameter change compared with the ADUDT simulations presented above, namely

- The early algorithm version could not solve sequences with two ZCC periods. The B-pulse always had to follow the freewheeling period with no ZCC. This did not limit the functionality of the algorithm as the parameters could be chosen such that t_{ZCC2} would always become zero. A B-pulse was still included, and the algorithm solution always existed over the full load current range.
- As the initial test naturally showed up with some overshoot envelope resulting from the timing distortion, the first reaction was to try to counteract the effect with simple fixed delay compensation. This attempt is completely absent in the simulation results presented above. Thus, the measurement result overshoot envelopes should not be directly compared with the simulation results, and actually, the measurements would produce lower values of S_{OE} owing to the simple but effective delay compensation. The further investigation of the delay compensation should be in the scope of future studies.

In all other aspects, the test setup ADUDT VFD implementation can be seen as a verification of the method in an actual motor drive. The reason behind the backward order of the study and the results is that the significance of the delays and the timing distortion was found only after the motor drive measurements were made. It does mean, however, that there will be no extensive S_{OE} comparisons with the simulation results, and the elaborate parameter variations are not repeated in the motor drive measurements. On the other hand, the motor drive test results show

- Filter output voltage and motor terminal voltage envelopes over the load current cycle, for the nominal load current of 43 Arms.
- Examples of individual output voltage edge waveforms.
- Effect of a B-pulse in the sequence; what happens in reality when the B-pulse is omitted.

- Voltage comparisons with the passive d*u*/d*t* and sine filter, with two different ADUDT filter structures (ferrite core and air core).

- Extensive testing of VFD and filter losses and comparisons using the different filtering methods and filters, cable length, and IGBT module type. A silicon carbide freewheeling diode included in the comparisons. Loss measurements provided with two different load current values (5.5 kW/11 A and 22 kW/43 A, or 45 kW motor with no load and 43 A current). 43 A measurements made with a calorimeter chamber to show the total losses in the VFD/filter.

The enhanced active d*u*/d*t* control algorithm was programmed into a control platform of a Vacon NXP-based prototype. The power electronics section is identical to the unit used in the measurements for the work presented in (Ström, 2009). The differences in the upgraded setup are (for the variable-speed drive unit)

- Availability of IGBT modules SKM100GB123D, SKM75GB176D, and SKM75GB176D with silicon carbide freewheeling diodes.

- New control electronics: a field-programmable gate array (FPGA) and a 150 MHz 32-bit microcontroller (MCU) connected together. The FPGA handles the ADUDT sequence state machine and produces the ADUDT pulses, while the MCU is the master PWM controller. The MCU runs the motor control, user interface communications, real-time ADUDT algorithm and state machine parametrization, and protection features (current and temperature limits).

The software implementation in the MCU allowed real-time calculation of the ADUDT algorithm up to the 8 kHz motor PWM switching frequency. The motor controls available were a field-oriented control and an open-loop scalar control. All the essential parameters could be varied during the test run. The block diagram of the control electronics platform is shown in Figure 5.11.

The prototype input power could be fed through the built-in grid filter, or as an externally rectified DC. This allowed the losses of the input filter and the rectifier to be excluded from the test. Three different AC induction motors were used in the tests; 5.5 kW, 22 kW, and 45 kW 400 V motors. The motor data are gathered in Table E.1, Appendix E.

5.2.1 Motor loads

The connection of the motors, output filters, and an optional braking machine/drive unit is shown in Figures 5.12–5.14.

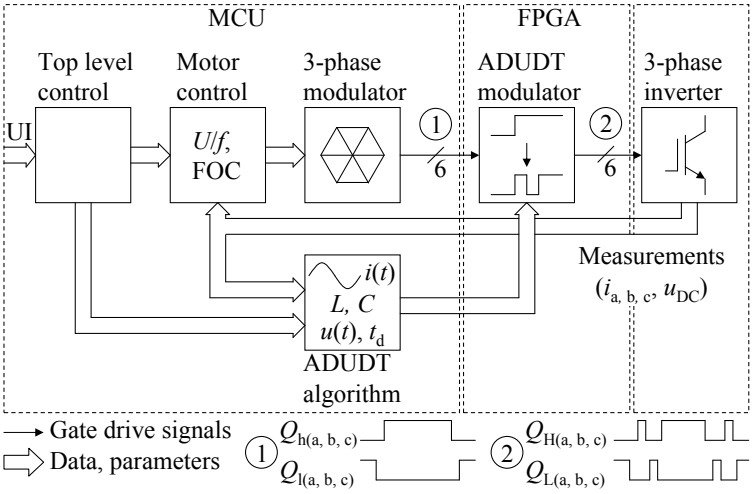


Figure 5.11. Block diagram of the control platform of the active d*u*/d*t* variable-speed frequency drive unit. (Tyster et al., 2011), ©2011 IEEE.

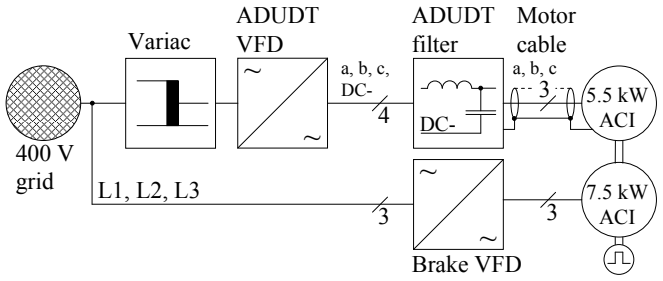


Figure 5.12. Block diagram of the VFD setup using a 5.5 kW induction motor as a load. Two AC induction (ACI) machines are mechanically coupled. The other (7.5 kW) machine is a brake generator. The power circulation is carried out through an AC grid with a braking VFD/grid inverter unit. The ADUDT VFD DC link voltage can be adjusted using an autotransformer. (Tyster et al., 2011), ©2011 IEEE.

5.2.2 IGBT modules

The two remaining blocks in the setups that could be varied were the IGBT modules and the output filter. The differences and theoretical background of the IGBT modules, chip technologies, and freewheeling diodes were discussed in Section 2.2. Table 5.4 lists the modules used in the measurements.

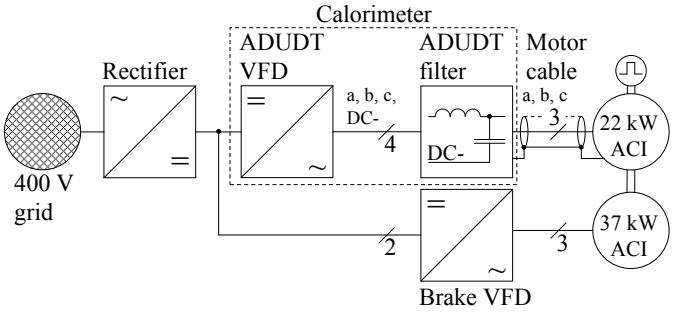


Figure 5.13. Block diagram of the VFD setup using a 22 kW induction motor as a load. Again, two ACIs are mechanically coupled and used as a motor/generator pair. Now, the power circulation is carried out through a DC link connection with a braking VFD (no grid inverter). The DC link voltage is not adjustable. (Tyster et al., 2011), ©2011 IEEE.

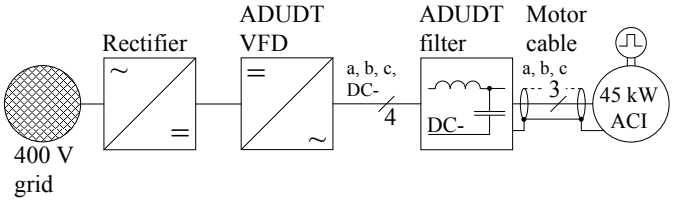


Figure 5.14. VFD setup using an unloaded 45 kW induction motor as a load. Since there is no mechanical load, the load current is almost completely reactive (ind.), with some active power to compensate for the losses. By using a lowered fundamental frequency with the maximum output voltage, the motor flux could be increased to provide the 43 A load current for the ADUDT measurements. The VFD power factor also changes, and thus, loss comparisons between the 22 kW and 45 kW motor setups were to be avoided. This test setup is more straightforward to use than the active power 22 kW setup.

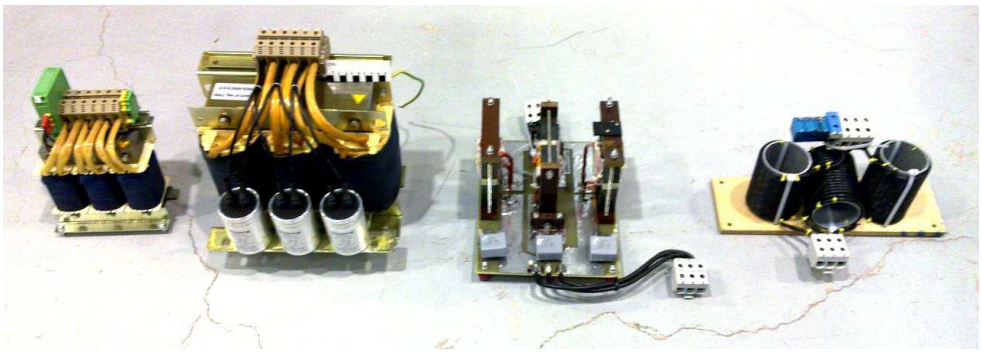
5.2.3 Filters

Four different output filters were included in the 43 A tests. The 15 µH/330 nF ADUDT filter was constructed with both ferrite E-cores and as an air-core version. Traditional passive output filters were available, one of du/dt type and one sine filter type. The manufacturer has stated approx. 52 A nominal current for the passive filters, but no rating for the maximum design cable length. A photo of all the filters included in the test setup is shown in Figure 5.15. The detailed filter electrical specifications are listed in Table E.2, Appendix E. The mechanical and winding construction details can be found in Table E.4, Appendix E. The voltage step response overshoot is an approximate value measured with a voltage step input from a VFD. The excitation is not ideal, and has some slope resulting from the nonideal voltage step of the phase leg output. The quality factor Q was measured with a Venable FRA 3120 frequency response analyzer. The resonant peak height is assumed to be the merit for the quality factor. For the sine filter (since capacitors are in delta connection), the measurement was made with the reference potential in the phase v output, while the input and output were at the phase u. This arrangement results in a resonant capacitance of 24 µF instead of 16 µF, the actual capacitor value. The AC inductance tests were made with an HP 4284A LCR

Table 5.4. IGBT modules used for investigations. (Tyster et al., 2011), ©2011 IEEE.

Component	Value/Description	Unit
Module A		
Model	SKM75GB176D (Si)	
Collector-emitter breakdown voltage	1700	V
Rated collector current	55	A
Allowed collector peak current	100	A
Module B		
Model	SKM75GB176D (SiC)	
Collector-emitter breakdown voltage	1700	V
Rated collector current	55 (IGBT)	A
Allowed collector peak current	100 (IGBT)	A
Module C		
Model	SKM100GB123D	
Collector-emitter breakdown voltage	1200	V
Rated collector current	90	A
Allowed collector peak current	150	A

meter, which only gives small-signal results. In reality, the inductance is expected to be non-linear towards the upper current range. There is also a phenomenon in the core materials that makes the inductance itself slightly dependent on the flux frequency, as presented in (Abeywickrama et al., 2008) for laminated steel cores. The material permeability can decrease as the frequency increases, and this was observed when measuring the filter inductances.



(a) (b) (c) (d)

Figure 5.15. Filters used in the loss measurements. (a) Passive du/dt, (b) sinusoidal, (c) ferrite/air gap active du/dt, and (d) air-core active du/dt filter.

The filters have some special characteristics that have to be taken into account when comparing the loss results. The passive filters have a laminated steel core with a plate thickness of about 0.35 mm, and at least a passive du/dt filter possibly having an air gap to linearize the inductance. The inductance was found to be linear up to at least 100 A peak current, using a voltage pulse test with a current measurement. The winding is made of nonisolated multifilar copper wiring, having a rectangular bundle cross section in the core post area. All the filters use plastic-insulated capacitors, and the passive du/dt filter has 220 kΩ resistors connected in parallel with its capacitors. The air-core active du/dt filter winding is made of 1.3 mm diameter copper wire strands, with seven strands in a conductor bundle. The individual strands are not insulated from each other. This is the simplest winding conductor construction of all the filters. The ferrite/air gap core active du/dt filter has a winding with individual strands insulated in the bundle, thus effectively forming a Litz wire structure. Passive filters also have a relatively large number of strands in the conductor, but individual strands are not insulated.

5.2.4 Motor cables

Finally, the cables used in the tests were polyvinyl chloride (PVC) insulated copper cables with a symmetrical phase conductor arrangement and a protective screen connected to protective earth at the grounded inverter chassis (and filter, where applicable) and the motor terminal box grounding lug. The data for the cable are given in Table 5.5. Very short connection wires between the VFD, filter, and connection terminals were made with ordinary installation wire, but still trying to minimize the interphase and return inductance by bundling the wires closely together and minimizing their length.

Table 5.5. Motor cables used in the test setups.

Cable type	Length [m]	[mm^2] (phase + screen)	L [µH/km]	C [nF/km]
5.5 kW				
Draka MCMK	100	2.5 + 2.5	320	300
22 kW				
Draka MCMK	200	35 + 16	260	550
45 kW				
Draka MCMK	11	16 + 16	260	400

This array of motor size, filter type, and control parameter variability allows comparative measurements to be made. The primary target of the measurements is to verify the enhanced active du/dt algorithm in a motor drive and compare it with the control method without a correction pulse or any of the new properties of the developed method. At the very minimum, a properly operating active du/dt filtering was expected, with motor terminal voltages below those achievable with the classic active du/dt control method. Loss measurements were the second major task. Different output filters were to be compared, and the loss results themselves compared with each filter's capability to reduce the motor terminal overvoltage.

The Vacon NXP variable-speed drive unit is a commercially available off-the-shelf product. Small modifications were made by J. Tyster such as the increased plastic-insulated capacitor at the DC link and refitting of different IGBT modules for each test. All the active du/dt filters were designed and constructed at Lappeenranta University of Technology by J. Tyster. The passive output filters were commercial products provided by Vacon Plc. The control electronics platform in the prototype consisted of a XILINX Spartan-3 FPGA board previously designed at LUT, a Texas Instruments TMS320F28335 microcontroller board, and an analog interface card. The analog interface card was designed by J. Tyster, while the other parts were either commercial products or designed in previous research projects at LUT. The motor control software in the MCU uses parts from the Texas Instruments Digital Motor Control library. Parts of the software framework are from Texas Instruments example projects. The MCU and FPGA software design and implementation was made by J. Tyster.

The active du/dt prototype was operated with a wide array of speed, loading, and IGBT module configurations, with different motor sizes. The 22 kW and 45 kW motor setups were used in the calorimeter loss measurements, with 22 kW running with a mechanical brake load and a 45 kW motor running idle. 43 A rms was chosen as the full load value for the tests. The choice for the 43 A rating is not a coincident. This is the nameplate value for the 22 kW motor, and summing the peak value of the 43 A sinusoidal current plus some ripple caused by the PWM operation and the characteristic charge current for the active du/dt filters used (approx. 80 A), the result is close to the 150 A short-time rated limit of the SKM100GB123D IGBT modules. For the 75GB176D modules, the current generally exceeds the adviced maximum ratings given in the datasheet by SEMIKRON. Thus, it can be stated that the IGBT modules were actually undersized for the application. It was the intention to push the power electronics to the limit and beyond, so as not to get overly optimistic results with oversized IGBT modules. It is advisable to choose slightly larger IGBT modules for active du/dt applications than would normally be with ordinary motor drives.

5.2.5 Filter du/dt reduction performance and voltage measurements

The du/dt reduction and the motor terminal voltage reflection overshoot are the main tasks of the VFD output filter. It is thus logical to verify the ADUDT operation in this task, and compare its performance with traditional passive filters. For the selected ADUDT filter L and C, and assuming a wave propagation velocity of 0.5c, Equation 3.1 gives a maximum cable length of 106 m for zero reflection overshoot operation. Any cable longer than this will introduce an increasing reflection overvoltage. The mid-slope du/dt (highest rate of change) for the ADUDT filter output is 230 V/µs (assuming 600 V U_{DC}). The passive du/dt filter has a lower measured du/dt rate of 160 V/µs, but it has an inherently larger value of overshoot owing to the filter resonance, 58 %. Knowing that timing distortions also cause the ADUDT overshoot envelope to increase, there is a certain cable length that produces a similar overvoltage envelope for both the ADUDT and the passive du/dt when observing the motor terminal voltages. If passive du/dt filter performance is accepted as a reference norm, then, from the application viewpoint, it suffices to remain below or approach the passive du/dt filter motor voltages when using the ADUDT. In other words, a longer cable for ADUDT can be used if some overvoltage is allowed anyway. The sine filter is expected to produce nearly sinusoidal

voltage, and it has so low d*u*/d*t* values that reflection overvoltages were not observed. Therefore, it is not included in the voltage performance comparisons, but is included in the loss measurements and physical characteristics comparisons. The voltage quality of the sine filter is, however, reduced by its rather large inductance, which can decrease the motor terminal voltage at motor control frequencies, reducing the nominal flux operating point and perhaps making the motor control more challenging.

The first test for the ADUDT is to see if the algorithm is able to keep the output voltage under control and within a reasonable overshoot envelope. It must be noted that the parameters for the algorithm differ from the simulation parameters as follows:

- All dead time values were set to 1.5 µs.
- The minimum A-pulse width is 1.3 µs, and the minimum B-pulse is 0.8 µs (the algorithm is forced to do the B-pulse drop-out at some point).
- The algorithm uses an L value of 18 µH; this was observed to produce a smaller overshoot envelope. The effect is suspected to counteract the timing distortion, or the interconnection leads to some added inductance.
- The average turn-on voltage edge delays are estimated to be 0.8 µs. The average turn-off voltage delays are 1.3 µs. The ADUDT pulse pattern timing is compensated accordingly by effectively delaying all the turn-on commands by 0.5 µs. This naive approach does not take into account the narrow-pulse turn-off behavior of the phase leg, but was observed to give a smaller overshoot envelope than with no compensation.
- The algorithm uses an U_{DC} value of 600 V, when in fact the average value is close to 540 V. However, this should cause an insignificant error as discussed in the simulation results.

A typical voltage rising edge for the active d*u*/d*t* prototype with the ferrite-core filter is shown in Figure 5.16. The filter output voltage can be observed to rise to the U_{DC} value in approx. 5 µs, which is in agreement with the nominal ADUDT sequence duration of 4.7 µs.

To see how the filter output voltage overshoot behaves over the full load current swing, a longer timescale waveform is shown in Figure 5.17. It can be seen that the filter output voltage is kept under control by the algorithm, and is quite good even though the B-pulse limitation is in effect. In a comparison, the simulation results showed an approx. 34% overshoot resulting from the B-pulse limit, with timing distortions. The test results depict a case of 60 A current swing and some level of delay compensation, and show a maximum overshoot of 35 %.

As the operation of the ADUDT algorithm was verified, the tests moved on to the motor terminal voltage measurements with a 200 m cable and different filters and filtering methods. The sine filter was excluded from the result figures as it produced a nearly perfect sine wave voltage with no overvoltage phenomena observable. A compilation of motor terminal voltages is shown in Figure 5.18. The active d*u*/d*t* filtering is operating with the algorithm.

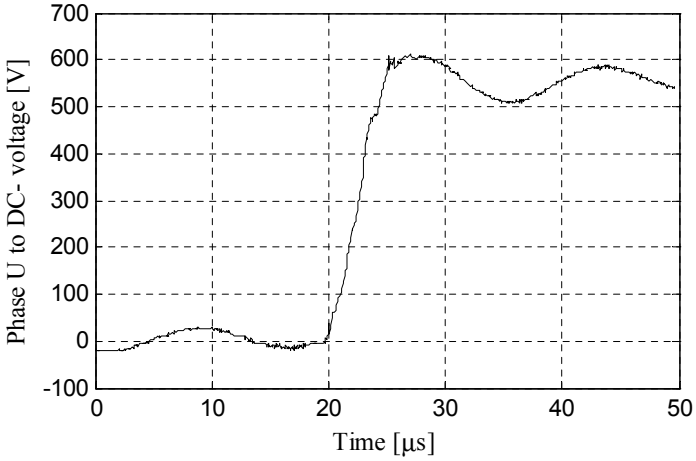


Figure 5.16. Rising voltage edge after the ferrite-core filter in the FR6 prototype operating under a 43 Arms load current. The instantaneous load current value is 50 A. (Tyster et al., 2011), ©2011 IEEE.

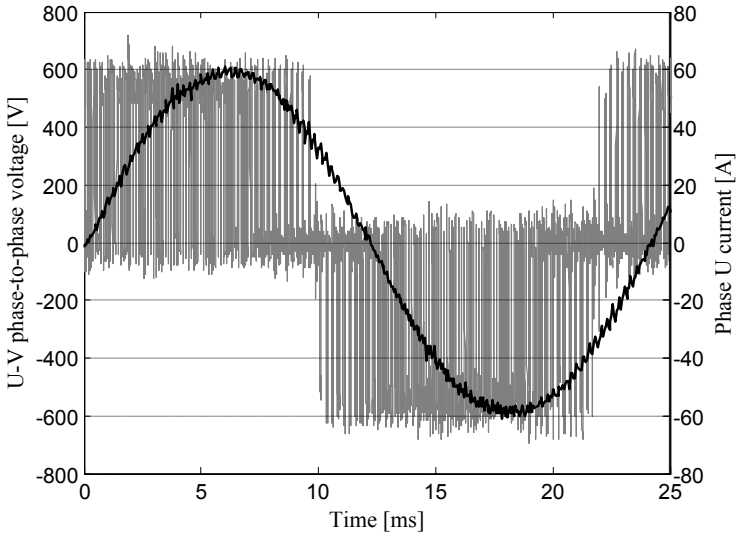


Figure 5.17. 43 A rms load current, typical line-to-line voltage seen at the output of the ferrite ADUDT filter. The algorithm in operation. This test is conducted using the idling 45 kW motor setup.

As can be seen in Figure 5.18, the active d*u*/d*t* method is more than able to compete with the passive d*u*/d*t* output filtering when it comes to the motor overvoltage reduction. Generally, the overvoltage is visibly reduced both in magnitude and envelope area. It is suspected that it is the inherent overshoot characteristics of the passive d*u*/d*t* filter that produce such a high overvoltage envelope at the motor terminals, rather than the overvoltage caused by reflection.

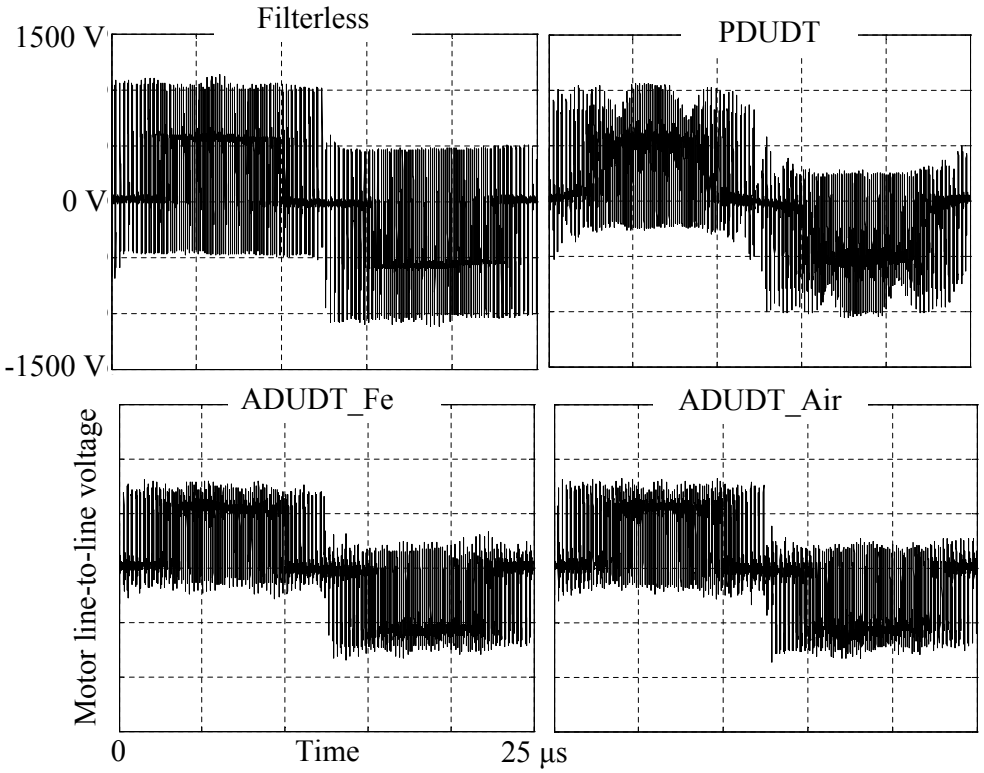


Figure 5.18. While the 45 kW motor was operated at no load and a 43 Arms 40 Hz phase current, the motor terminal voltages for different filters were measured. ADUDT_Fe is the ferrite-core ADUDT filter.

This should be the case as the passive filter has a lower du/dt value than the ADUDT filter. The air-core and ferrite-core ADUDT filters seem to perform equally well in the voltage tests. It shows that air-core inductors are definitely a viable option if other factors such as stray field effects are not a problem. Referring to the filter mechanical data in Appendix E, this could result in quite a low filter mass (2.4 kg air-core ADUDT, 5.5 kg ferrite-core ADUDT, 14.0 kg steel-core passive du/dt filter).

It was decided that the observation of the ADUDT functionality with these default parameters suffices to give confidence to move to loss measurements. The ADUDT method using the algorithm works and is able to beat the passive du/dt in voltage performance. Before going into the loss measurements section, a final test on the role of the B-pulse in the sequence was performed. A comparison of the B-pulse disabled vs. enabled is shown in Figures 5.21 and 5.22, respectively. It is once again reminded that the B-pulse cannot be replaced by ZCC as the A-pulse can be, and thus, a B-pulse drop-out or complete disabling is always expected to result in an increased overshoot. This is most evident as the load current to filter characteristic peak current ratio is increased. These tests were carried out with the no-load 22 kW motor

setup, using increased flux for a 50 A peak load current range.

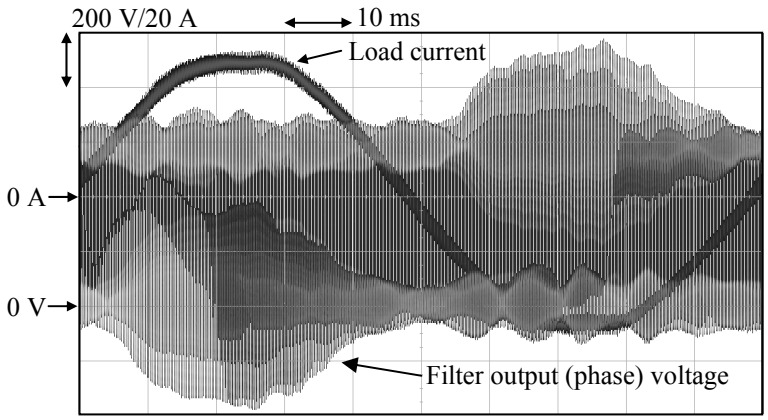


Figure 5.19. 10 Hz constant rotating voltage vector is fed to the 22 kW motor running idle to examine the effect of a varying load current value on the active du/dt filtering if the B-pulse is not in use. A ferrite ADUDT filter is used. The filter output voltage overshoots at the falling edges/current out and the rising edges/current in, since the ADUDT algorithm has no ability to compensate for the load current.

If the B-pulse is omitted completely, there is clearly an increase in the output voltage envelope as seen in Figure 5.21. Once again, a comparison with the simulation results is made, which gives an S_{OE} figure of 26.6% and 89.9% peak magnitudes for uncompensated delays and a 80 A load current swing (the parameters are not exactly the same, but judging by the parameter effects, this would not make much difference in the figure). The overshoot magnitude in Figure 5.21 is 65%, a value close to the simulation results if the lower load current value and perhaps the presence of delay compensation is taken into account. Omitting the B-pulse is not possible for the ADUDT implementation in motor drive applications, when the load current level is high enough compared with the filter peak current.

In contrast, Figure 5.22 shows how enabling the B-pulse brings the overshoot envelope back to low residual values, mainly caused by timing distortion effects. It is also possible that as the S_{OE} becomes small, the relative effect of parameter errors and measurement uncertainty becomes significant in the overshoot envelope magnitude. It would be interesting to study the effect of parameter variations and delay compensations using the actual output voltage measurements, in the same way as the S_{OE} simulations were conducted, and this should be in the scope of future studies.

A closer look into one of the rising voltage edges with the algorithm disabled versus enabled is shown in Figures 5.21 and 5.22, respectively. Here, the algorithm is first completely disabled, which introduces the combined overshoot effect caused by the initial dead time ZCC and the A-pulse of excessive length, and then omission of the B-pulse, although the B-pulse could no longer help as the overshoot is more caused by the wrong charge period in the sequence.

The algorithm is able to take into account the dead time ZCC effects and reduce the A-

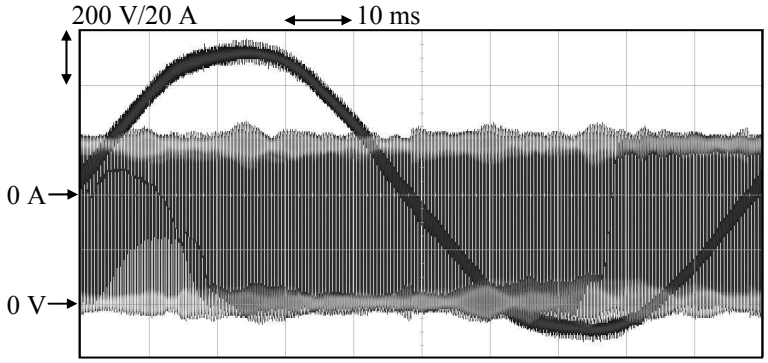


Figure 5.20. Same situation with the B-pulse in the ADUDT algorithm in operation. The overshoot tendency is almost completely removed.

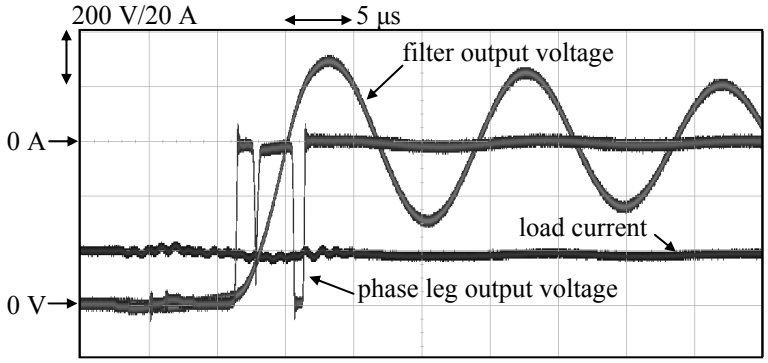


Figure 5.21. Zoom into one of the rising voltage edges, with the ADUDT pulse operation visible in the phase leg output voltage. No current correction B-pulse/algorithm is used, and the sequence timing error is enough to cause approx a + 50% voltage overshoot at the filter output.

pulse duration accordingly. Then, the B-pulse is used to compensate the load current effect, resulting in a considerably improved waveform compared with Figure 5.21.

Based on the voltage performance measurements, the implemented ADUDT method is able to operate with motor loads, and gives a very satisfactory du/dt reduction. The next step is to compare the filtering methods in terms of losses and filter physical qualities.

As a side note, the suggested algorithm is not strictly required for B-pulse implementation, as any sequence bearing the ability to compensate for the load current can be considered to have the B-pulse. Rather, the algorithm is an automatic solver for the pulse sequence, operating with the given constraints and implementing the dead times, A-pulse, ZCC, and B-pulse. An effective ADUDT sequence or a set of sequence look-up tables could be solved in advance, including the B-pulse. As a matter of ADUDT implementation in value line MCUs of lower calculation capacities, the algorithm could be used in the programming phase to solve a preset

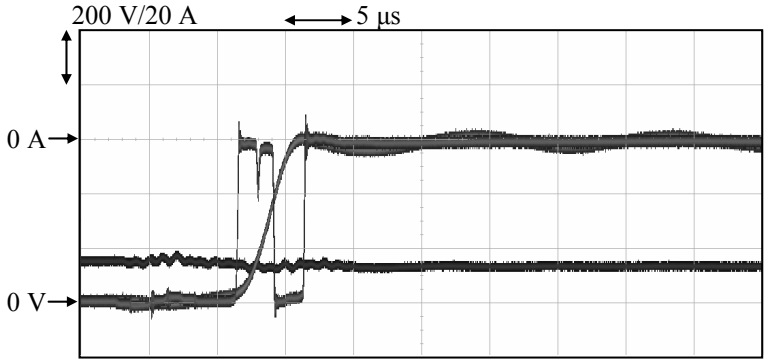


Figure 5.22. Active d*u*/d*t* algorithm remedies the overshoot. The narrow notch in the middle of the charge period is an indication of ZCC being present, during which the output voltage clamps to the filter capacitor voltage value (but as the power electronics is not ideal, the very brief ZCC ends before the voltage have time to transit).

look-up table. Strictly speaking, this kind of an approach is perfectly possible with trial-and-error solving of the sequence, as already presented in (Korhonen, 2012). Using the algorithm just makes it easier to solve and analyze.

5.3 Loss measurements and comparisons with other filtering methods

The measurement of the losses was made by two methods, which are both based on direct measurement of the thermal power loss. The first one is a temperature difference method using the predetermined heat sink thermal resistance and heat sink temperature rise as an indication of the IGBT and diode losses. It is assumed that if the thermal resistance can be determined with a sufficient accuracy (and later verified by calorimetric results), the inlet air temperature is kept reasonably constant, and the measurements are controlled in such a way that the temperature measurement locations are always fixed, the method should give the inverter loss with some accuracy. The heat flux through the heat sink to the ambient under a forced-convection cooling can be calculated by

$$P_{\text{th}} = \frac{\Delta T}{R_{\text{th}}} \tag{5.1}$$

where P_{th} is the thermal flux (heat loss), ΔT is the temperature difference between the heat sink and the ambient, and R_{th} is the thermal resistance of the heat sink. There could be variability of the thermal resistance owing to a change in fluid characteristics caused by temperature, moisture, and pressure (Incropera et al., 2006), and therefore, the variation in the

air flow characteristics in each setup should be minimized. The possible error sources and method uncertainty is discussed in more detail in Appendix C. The temperature measurement accuracy directly affects the resulting accuracy. The heat sink thermal conductivity is anisotropic as a result of its construction, as it is made by pressing together individual fin elements and later milled into a thermal interface surface. The thermal resistance characterization should be conducted using identically shaped resistors as the IGBT modules, in an identical location, and keeping the temperature measurement location in the heat sink fixed. The principle of this temperature rise measurement method is shown in Figure 5.23.

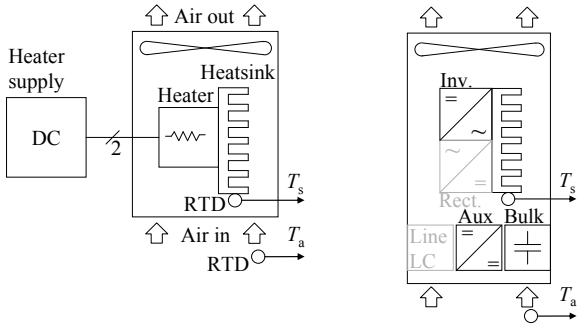


Figure 5.23. Power dissipation of an electronics device can be measured based on the temperature difference and the thermal resistance. (Tyster et al., 2011), ©2011 IEEE.

For R_{th} characterization, the cooling fan was operated with a constant voltage, and several temperature rise measurements were made using IGBT-module-shaped heating resistors in place of the IGBT modules, in a thermal mock-up model of the actual VFD. Multiple measurements were averaged to get an estimate for the heat sink thermal resistance. The tests were made in ambient temperature remaining within approx. $\pm$ 0.5 °C limits to keep the air flow conditions as repeatable as possible (no extra objects located near the inlet or exhaust ports). The thermal resistance was determined as 0.033 K/W. The temperature was always measured as a difference between the inlet air temperature and the heat sink temperature. For actual loss measurements, the temperature measurement locations were repeated exactly as in the thermal mock-up model, and the fan was operated with the preset voltage. The VFD control electronics card could introduce a few watts of heat flux in the test, and this effect should be separately compensated for in the results. The ΔT method has quite a few error sources, and an attempt to address the uncertainty analysis is included. Details are provided in Appendix C.

The ΔT loss measurement method is unable to reveal the passive losses of the output filter. The second loss measurement method used is the calorimetry, consisting of a calorimeter chamber with an option to locate the active du/dt VFD, the output filter, or both inside. The losses in the components inside the chamber are measured based on the air flow required to keep the chamber temperature constant. The method and the calorimetric measurement setup, with preconfigured chambers and equipment were run at Lappeenranta University of Technology by Associate Professor, Dr. Antti Kosonen, and Dr. Lassi Aarniovuori. The verification of the measurement accuracy has been published in (Kosonen et al., 2013) and (Aarniovuori et al., 2013). The reported combined uncertainty for the loss measurements is

$\pm$0.4%, depending on the measurement parameters. For the ADUDT loss measurements, an uncertainty of less than $\pm$1.0% is guaranteed. This was considered the most accurate method to evaluate the losses in the system, and further, it was the only direct method to measure the filter losses. However, it is suggested that whenever possible, the comparison of loss measurement results should be relative only, and for instance the results obtained by the ΔT method should not be directly compared with the chamber method loss results.

A list of various measurement equipment used in the loss measurements is given below. The calorimeter setup has its proprietary measurement equipment, which is directly related to the loss measurements, and not relevant here. The calorimeter postprocessing gives the loss results with the indicated uncertainty limits.

- Agilent DSO6104A and MSO-X 3054A oscilloscopes, for voltage and current waveform observations.
- Tektronix P5205 high-voltage dfferential probe, voltage measurements.
- Yokogawa WT1600, for load RMS current monitoring and VFD output power measurement in the calorimeter chamber tests.
- Agilent 34970A data acquisition unit, for temperature measurements in the ΔT loss measurement method.
- ISK PT100 resistance temperature detectors, model P0K1.232.6W.A.010, DIN class A, in the ΔT method.

The calorimeter loss measurements were conducted with the assistance and under the supervision of Dr. Antti Kosonen and Dr. Lassi Aarniovuori. The results were analyzed and corrected for calorimeter equipment-specific factors by Dr. Antti Kosonen. The measurement plan was made by J. Tyster, as were the operations directly related to the VFD setup and installations.

5.3.1 Loss measurement results

The aim of the loss measurements is to compare the ADUDT with the traditional output filtering solutions in terms of power loss. Both VFD losses and filter losses should be addressed. It is interesting to know how the ADUDT compares with passive du/dt in losses, after convincing voltage performance results. After all, the motivation to use variable-speed drives is to improve the process energy efficiency. It has to be shown how the ADUDT agrees with this target.

Besides filtering method comparisons, the effect of the drive setup on the losses has to be investigated. If the cable length has some effect on the losses, it should be indicated. Varying the ADUDT filter construction can produce some difference to the filter loss figures.

There might be a potential for loss reductions when using SiC freewheeling diodes with the ADUDT.

The first measurements used the 5.5 kW motor setup with the ΔT loss measurement method. This is quite a low-power load when comparing the load current with the filter peak current, and thus, the algorithm/B-pulse plays a very small role in the ADUDT operation. In fact, the 5.5 kW tests did not use a B-pulse at all. The peak load current is 16 A, which would result in less than 20% overshoot magnitude based on the simulation results in Figure 5.6. The loss measurement results are shown in Table 5.6.

Table 5.6. Loss measurement results with the 5.5 kW motor setup. The losses indicated are the inverter losses obtained with the ΔT method. (Tyster et al., 2011), ©2011 IEEE.

Effect of cable length on losses with ADUDT_Fe filter, 5.5 kW setup. Losses in [W]. Motor current (11 ± 0.5) A.

	Cable length [m]		
Module	1	100	300
C	389	405	420

5.5 kW full load (11 ± 0.5) A, 100 m & 300 m cables, f_{sw} = 4 kHz. Losses in [W]. ADUDT_Fe.

	Filter, module type, cable length [m]			
	ADUDT, C, 100	ADUDT, A, 100	ADUDT, B, 100	PDUDT, A, 300
Loss	405	514	315	155

Inverter losses in [W] as a function of switching frequency. No load. ADUDT_Fe.

	f_{sw} [kHz]			
Module	1	2	4	6
C	77	148	296	472
A	-	157	328	545
B	-	109	217	344

Looking at the results in Table 5.6, the topmost pane, an 8% increase in losses is observed as the motor cable is varied between 1 m and 300 m. With a ±5% uncertainty for the ΔT method, this difference is considered barely significant. The lower left pane shows the effect of IGBT module variation. Module C is the 1200 V/100 A model, which gives lower losses than the 1700 V/75 A module A. However, module B, 1700 V/75 A with SiC diodes, produces even lower losses than module C. These differences are significant and suggest that the SiC diode can have a dramatic effect on the inverter losses when applying the ADUDT method. Nevertheless, the ADUDT losses are higher than what is experienced with the passive du/dt filter, module A, and 300 m cable length. This suggests that even using the SiC diode cannot bring the losses back to the level of passive du/dt filtering. The lower right pane shows the ADUDT loss dependency on the fundamental switching frequency. Within the measurement

uncertainty, the losses can be observed to follow the switching frequency linearly. If linear regression is made for these results, the regression y-intercept has a low value, suggesting that the losses are dominated by switching losses.

Next, the results obtained with the 22 kW motor setup are presented and discussed. The measurements are partially repeated with both loss measurement methods, showing the correlation of the loss measurement results obtained by the approximate ΔT method versus the calorimeter-method-based loss measurement results. The results are given in Table 5.7. The results indicate at least two interesting things; (a) the ΔT method has quite a large deviation compared with the calorimeter result, and (b) SiC does not give as much loss savings with the now-increased load current compared with the 5.5 kW setup results. These results should be taken with caution, as the ΔT method uncertainty is rather large compared with the loss difference. Unfortunately, the SiC modules did not survive the tests for long, perhaps because of operating so close to their current rating and exceeding their safe operating area. The SiC tests could not be repeated with the calorimeter.

Table 5.7. Loss measurement results with the 22 kW motor setup. (Tyster et al., 2011), ©2011 IEEE.

IGBT module	Output filtering	ΔT [°C] ($T_s - T_a$)	R_{th} [°C/W]	Calorimeter-based loss (method 1)	$\Delta T/R_{th}$ - based loss (method 2)	Difference $\frac{\text{method 2}}{\text{method 1}}$ [%]
C	ADUDT_Fe	24.4	0.0353	803	691	-14
C	None	14.8	0.0353	460	419	-9
A	ADUDT_Fe	33	0.0329	-	1003	-
B	ADUDT_Fe	26.9	0.0329	-	818	-

It is also interesting to note that the loss increase resulting from the ADUDT versus no filtering is 75% according to the calorimeter results. If the relative loss difference between the SiC and Si diode results is considered significant (18%), and then directly compared with the loss increase caused by the ADUDT, it can be roughly estimated that as the load current level is increased, the use of SiC diodes results in lower returns in loss savings. It would be advisable to continue the SiC measurements in future studies.

The value of the thermal resistance in Table 5.7, calorimeter setup was adjusted after an error in the air vane settings was observed. After measurements, it was found that two air guide vanes were missing in the heat sink cavity, thus the R_{th} had to be determined again. Even after adjusting the results with the uncertainty analysis, the deviation between the calorimeter result and ΔT method result cannot be explained. It is recommended not to compare the calorimeter results with the ΔT method results in Table 5.7, and perhaps the reason for the deviation can be found in the future.

The final loss measurements were conducted with SKM100GB123D IGBTs with a 45 kW idling motor in order to compare the filter losses and the impact of the active du/dt on the

inverter losses. The results are gathered in Table 5.8. The test setup inside the calorimeter chamber had difficulties in surviving through the measurements, probably because of the elevated temperature of 40 °C in the chamber and the test VFD being already at the limit because of the losses increased by the ADUDT operation. The set of IGBT modules had to be changed three times during the tests, together with the gate driver board. This is indicated in the table as the IGBT specimen number. Some tests were repeated just to see how large an influence the IGBT specimen change could have on the results, and to be able to take the possible effect into account in the result analysis. The variation caused by the IGBT module change is less than 2% based on one reference measurement pair. Thus, the actual results should not be made with less than a combined uncertainty of approx. ±2%.

Table 5.8. Loss measurement results with the 45 kW motor setup.

	PDUDT 11 m		PDUDT 200 m		Sine 200 m		PDUDT 200 m		ADUDT_Fe 200 m		ADUDT_Fe 200 m		ADUDT_Air 200 m	
	VFD	Filter	VFD	Filter	VFD	Filter	VFD	Filter	VFD	Filter	VFD	Filter	VFD	Filter
f_{out} [Hz]	40		40		35		40		40		40		40	
I_{out} [A]	43.01		43.01		43.01		43.01		43.01		43.00		43.02	
Losses P [W]	432	85	434	184	406	166	426	183	794	125	774	127	782	111
P,sum [W]	518		618		573		609		919		901		893	
IGBT specimen	I		I		II		II		II		III		III	

Table 5.8 shows a significant filter loss dependency for the passive du/dt filter; the filter losses with the 200 m cable are 2.19-fold compared with the 11 m motor cable. The cable length dependency of the losses was not repeated with the ADUDT, but both the ADUDT filters can be seen to have lower filter losses with the 200 m cable length. In theory, the ADUDT filter losses could be decreased further by design, as the filter passive damping is not needed as much as with the passive du/dt filter. The air-core filter has a marginally lower loss than the ferrite-core filter. Referring to Appendix E Table E.4, the air-core filter has almost an equal copper cross-sectional area as the ferrite-core filter, but the winding conductor length in the air-core filter is considerably larger. The effect is that the copper losses are greater in the air-core filter. If the air-core filter is given more copper area, and perhaps using a multifilar winding, the losses could probably be decreased.

The key findings based on the 45 kW motor results can be summarized as:

- The VFD losses do not vary with the cable length for any of the filtering methods. The sine filter produces slightly lower losses than the passive du/dt filter, assuming the sine

filter losses are not significantly dependent on the fundamental load frequency. An ADUDT loss increase is present. As the filter losses are also included, the ADUDT method total loss increase is approx. 51% compared with the passive du/dt filtering. If the load current is interpreted as active power of 22 kW (43 A for 22 kW motor setup), the VFD + filter losses would result in a drive efficiency value of 96.2% for the ADUDT versus 97.5% for the passive du/dt filtering.

- The ADUDT filters have a lower mass than the steel-core passive du/dt filter (2.4 kg air-core ADUDT, 5.5 kg ferrite-core ADUDT, 14.0 kg steel-core passive du/dt filter). The sine filter is even more massive; it weighs 44 kg. The volumes of the filters do not scale in the same way, and especially the air-core filter inductors are quite large compared with the total filter volume. Nevertheless, the ADUDT allows the filter construction to be more light-weight, and possibly produce lower losses with design, which could give it an advantage in some special applications.

Chapter 6

Conclusions and discussion

In this chapter, the key findings and results of the doctoral thesis are summarized. The outline and scope of the doctoral thesis are reviewed.

The use of a power electronic frequency converter is beneficial for the energy savings in present-day attempts to reduce energy consumption in industrial settings. The variable-speed AC motor drive has established a good reputation in applications such as pump and fan drives. There is a strong desire to equip lossy throttling valve type process controls with variable-speed equipment. The background for the energy savings potential was discussed in the thesis, and several publications have been made on the issue. In the near future, the need for power electronic converters in motor drive applications is certainly not expected to diminish, as big players such as India and China are bolstering up their industrial sector output.

The three-phase AC induction machine drive with an IGBT inverter is a mainstay component in any current and future installation. Hence, we may assume that there will be a market for power electronic converters for future applications. As was presented in this thesis, the variable-speed AC drives can also introduce side effects, affecting the lifetime of the electric machine doing the actual mechanical work in the process. The concept of cable-reflection-induced overvoltages was discussed, and the traditional methods to mitigate it were covered. The basic transmission line theory required for the understanding of the fundamental problem with present-day insulated-gate bipolar transistors (IGBT) with long motor cables was presented. The steep voltage transients associated with power electronic switching components in a three-phase inverter can have a detrimental effect on the life expectancy of the motor insulations and bearings. The problem is more pronounced with voltage-source inverters such as the basic example given in this thesis than with direct grid-connected motors. The speed and torque control of the AC induction motor is enabled through the use of variable-speed drive technology, and thus, the solutions for the harmful side-effects are most welcome. This is in conjunction with the energy savings objectives.

An emerging method for the overvoltage mitigation, that is, using an active combination of

the IGBT transistors and a suitable passive filter was discussed. This active d*u*/d*t* filtering method enables a very good overvoltage reduction at the motor terminals. The solution has been recently studied at Lappeenranta University of Technology, with similar propositions made previously. Compared with the traditional passive-only filtering solutions, more lightweight and physically small filter circuits can be constructed. The method would probably benefit from future improvements in power semiconductor technology. It is applicable today, at least in a limited sense, and experimental setups have been demonstrated. Judging by the loss measurement results, the active d*u*/d*t* output filtering is not beneficial if the total system loss is evaluated. The extra losses presented by the ADUDT sequence pulses increases the VFD losses.

The work presented in this doctoral thesis provides a new solution for the active d*u*/d*t* output filtering control. The solution is an algorithm, giving a pulse pattern structure as a function of drive parameters such as dead times and minimum pulse limitations. The solution enables active d*u*/d*t* to be used with present-day IGBT modules in general motor drive applications, with more flexibility towards dead times and control parameters than the previous control methods allowed. The development and operation principle of the algorithm were covered.

The concept of timing distortion effects in the half-bridges inside the variable-speed drive was given a look from the perspective of active d*u*/d*t* filtering. The active d*u*/d*t* filtering uses such a pulse timing in the IGBT half-bridge that any timing error source in the range of 1 µs for typical applications can have an effect, and although the proposed control algorithm in this thesis can cope with the dead times, the matching of the timing delays would improve the filter output voltage waveform. With matched delays, the dead times could also be minimized, and this would result in simplification of the active d*u*/d*t* operation.

Experiments were made to give an answer whether the active d*u*/d*t* method with the new algorithm is a viable motor overvoltage reduction solution in variable-speed drives; the results showed that the method is able to outperform the traditional passive d*u*/d*t* method. With two passive d*u*/d*t* filters available, comparisons in the overvoltage limitation capability and the impact on drive losses were discussed. With the help of the new active d*u*/d*t* control method, the solution was demonstrated to be a viable option for motor overvoltage limitation with long motor cables. Better yet, the method can benefit from future semiconductor material and component improvements, as demonstrated by the SiC diode tests.

6.1 Conclusions on the experimental results and suggestions for future work

The proposed active d*u*/d*t* control algorithm was capable of active d*u*/d*t* pulse sequences required for a 43 A rms motor load current, and good overvoltage limitation for a 200 m motor cable length, at the same time obeying the dead time and minimum pulse width constraints of the IGBTs and the gate drivers. It is suggested that the timing delay matching and compensation is studied in the future work. This could improve the output voltage performance.

The parameter selection for the ADUDT algorithm is still not optimized, and the results in this thesis could only give a hint how various parameter changes affect the ADUDT performance. Furthermore, the filter inductance characterization can be more involved than thought, as the wiring and resistive losses add to the impedance in the circuit. This was compensated in the test setup with an iterated value, and this effect should also be investigated. More parameter variations should be performed in the tests.

Once the algorithm was in such a working condition that it could be programmed in the experimental setup, certain questions related to the software and computation time requirements of the algorithm arose. The algorithm was demonstrated to be applicable to modern control electronics, even without any specific optimizations for computation time. A switching frequency of 8 kHz is possible with the experimental setup, calculating the algorithm for each switching device twice in the PWM period. Nevertheless, a look-up-table-based solution would be a low-requirement alternative to real-time algorithm solving, and an analysis of the minimum computation effort for the active du/dt could be made. One unsolved equation remains in the algorithm, and this could also be solved in the process.

The overvoltage mitigation performance was seen to be competitive with the passive filtering solutions with the 200 m cable length. The active du/dt method could be tested with considerably longer cable lengths to see if it can rival the sinusoidal output filter in performance. The comparison should also include other du/dt reduction methods not covered in this thesis, such as the active Miller clamp and the resonant DC link structure. The overshoot envelope should be analyzed directly, and used in a similar fashion as with the simulation results in this thesis.

The ΔT loss measurement method was not thoroughly verified, and the uncertainty could not be given reliably. The method should be investigated in the future studies.

Loss measurements revealed that a silicon carbide freewheeling diode decreases the losses with active du/dt operation. Different IGBT modules affected the losses, which was expected. The active du/dt filtering operating in the 45 kW motor setup showed that although the filter losses could be made smaller than with traditional passive du/dt filters, the inverter losses will increase. Thus, the active du/dt filtering is not directly competitive with traditional methods when it comes to drive efficiency. This is due to the increased losses in the IGBT modules mainly resulting from the switching loss increase. Future work should include an investigation on an opportunity to use a soft switching scheme of some sort to mitigate the rather steep loss increase with the active du/dt. Other than that, the selection of an IGBT module for the active du/dt use should aim to reduce the switching losses. The SiC diode studies should be continued further.

The active du/dt was not measured with minimized dead times. As suggested in the thesis, active du/dt could ultimately be operated with minimum dead times in the half-bridges, should the timing delay matching allow. This would simplify the control method, and perhaps eliminate the algorithm (but include an elaborate delay matching compensator). This alternative implementation should be investigated.

Active d*u*/d*t* filtering can be used today if an application requires the least filter losses with a minimum weight. Unfortunately, because of the increased losses in the inverter, it is not expected to be implemented in every general variable-speed drive application today. The future will show how the switching losses could be decreased. Perhaps then, the active d*u*/d*t* is taken into reconsideration. The optimization of the filter losses and structure could now make the method more competitive, and this is something to consider. There could be a comparison between passive d*u*/d*t* filter overshoot and ADUDT overshoot in case more damping losses are allowed in the passive filter. If losses are taken as a cost criterion, which filtering method would be the most economical one per given overshoot?

6.2 Final words

The previous studies on ADUDT concluded that the timing deviations and dead time insertion could be a problem for the ADUDT implementation in industrial motor drives. As demonstrated by the new algorithm and timing deviation study in this thesis, these problems can be solved. The use of a dead time is not a problem. Pulse limitations can be handled by the algorithm. The timing deviations do cause additional overvoltage, and their effect was seen in the simulations and measurements. However, in the test setup, a simple average-value compensation was tried, and the total overshoot envelope was considerably lower than with traditional passive d*u*/d*t* filtering methods.

Losses were found to increase as predicted by previous studies. Emerging component technology can help in the implementation, but still, the active d*u*/d*t* seems to be a method for special applications, requiring the lowest possible filter weight. Even after the slight disappointment with the loss results, the study of the control algorithm shows that the control of the ADUDT in actual applications is possible, and maybe the active d*u*/d*t* output filtering will find its place.

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Appendices

Appendix A

u_G turn-off model

Table A.1. u_G model parameters used in the S_{OE} simulations.

Parameter	Value
U_{G+}	17 V
U_{G-}	-10 V
U_T	6.9 V
g_{fs}	43 S
τ_{gate}	1.5 µs
$t_{M(on)}$	210 ns
$t_{M(off)}$	140 ns
$t_{driver(on)}$	0.5 µs
$t_{driver(off)}$	0.5 µs

Generally, all the u_G model parameters have some effect on the turn-off delay value. The following observations are made based on Figures A.1 and A.2:

- Increasing τ_{gate} (increasing the gate resistors, having a larger gate capacitance) increases the turn-off delay but also increases the time required to reach the u_G steady-state value, which means that longer pulses are required before a constant turn-off delay occurs.
- Having a lower threshold voltage U_T also increases the delay, since the Miller plateau voltages are directly influenced by the voltage. With a lower threshold, the surplus gate charge is increased.
- Gate driver voltages have the predicted effect. They directly influence the gate charging/discharging characteristics.

- The transconductance g_{fs} also affects the Miller plateau voltages, with a higher transconductance lowering the Miller voltage for nonzero load currents. Thus, a higher g_{fs} causes more surplus gate charge and a higher turn-off voltage edge delay.
- Not exactly a model parameter, but the turn-off current also affects the turn-off delay, since the Miller voltage depends on the load current. A higher current value results in a higher Miller plateau voltage, shortening the turn-off delay.

As can be seen in the example results in Figures A.1 and A.2, the relative delay value error is significant even with rather small variations in any of the parameters τ_{gate}, U_T, U_{G+}, or U_{G-}. Nevertheless, all of them have similar effects, either increasing or decreasing the model delay value (τ_{gate} having the major influence on the time constant behavior). Thus, the error in the parameters can be compensated by comparing the u_G model turn-off delay with the measured turn-off delays, and adjust one parameter in the model to achieve a satisfactory match; this was the approach taken in the simulations. The model parameters are thus not the actual physical values from the test setup, but rather the values that resulted in the best match between the simulated and measured turn-off edge delays for narrow pulses.

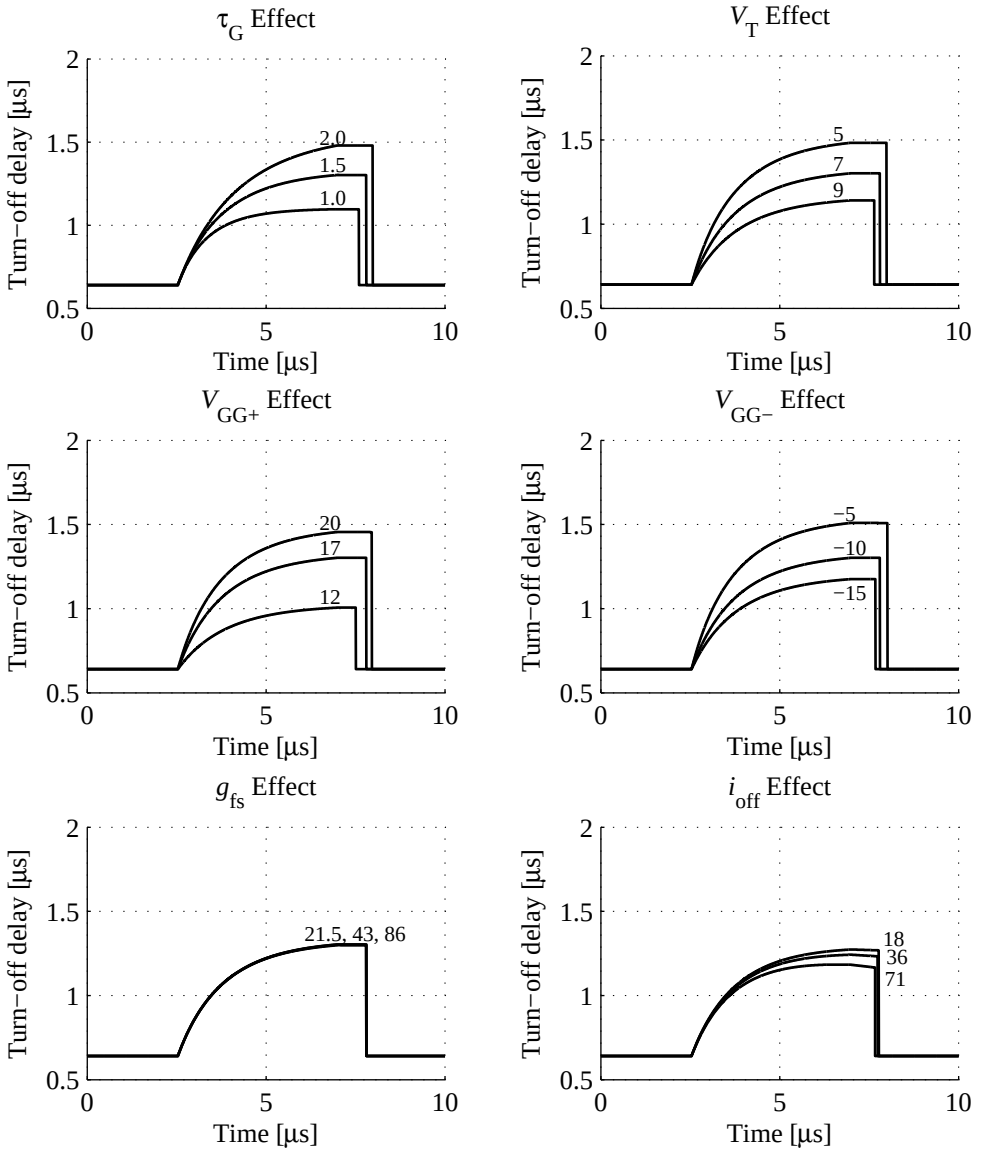

Figure A.1. Using a constant gate drive test pulse, the effects of u_G model parameter variation were tested. The waveforms are the responses of the u_G model at some point in time. A 4 µs gate drive command pulse is used, starting at 1.5 µs. The u_G model resets the delay counter after $t_s+t_{driver(off)}$ has passed, so the fall of the graph is not yet the turn-off voltage edge. The gate drive command goes to zero at 5.5 µs, after which the turn-off voltage edge occurs as indicated by the u_G delay counter value; this value is the y-axis value in the graphs. After the turn-on has occurred and the $t_{M(on)}$ Miller plateau delay has passed, the gate voltage model starts to increase the turn-off delay. This occurs at 2.5 µs. The load current is zero, and not allowed to rise, except in the i_{off} test. The zero load current results in the g_{fs} test showing no differences, and therefore, the test is repeated with some load current value different from zero.

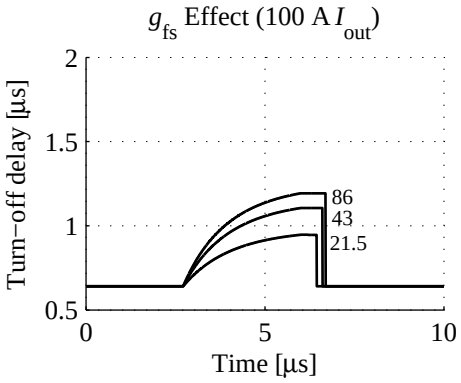

Figure A.2. With load current different from zero, the g_{fs} effect can be demonstrated.

Appendix B

Method of solving the t_a and t_{fw} equations

The solution starts with the time-domain equations of the filter voltage and current:

$$\begin{aligned} u_C(t) &= U_{in}\left[1-\cos(\omega t)\right] + Z_f \sin(\omega t)\left(i_L(0) - I_{out}\right) + u_C(0)\cos(\omega t) \\ i_L(t) &= I_{out}\left[1-\cos(\omega t)\right] + Y_f \sin(\omega t)\left(U_{DC} - u_C(0)\right) + u_C(0)\cos(\omega t) \end{aligned} \tag{B.1}$$

It is known that the capacitor voltage u_C must be continuous both in value and derivative at the boundary of the A-pulse and freewheeling periods, as shown in Figure B.1:

The initial values for the capacitor voltage are calculated as presented in the main chapter, repeated here:

$$u_1 = u_{C,tres} + u_{ZCC1} \tag{B.2}$$

$$u_2 = U_{DC} - u_{C,tres} - u_{ZCC2} \tag{B.3}$$

Using these initial values, a system of equations containing the capacitor voltages and its derivative is constructed. The voltage values for both sides must equal in order for the voltage to be continuous, and this will be the simultaneous solution for t_a and t_{fw}. The method involves initial-value u_C and u_C derivative equations, and their forward-time and backward-time representations. The forward-time equation sets an initial value and gives a final value

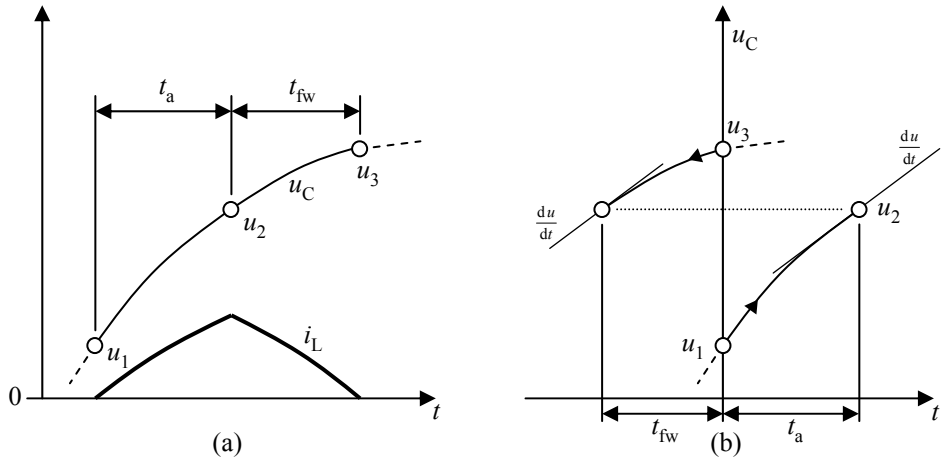

Figure B.1. (a) Charge pulse period t_a starts with some u_C voltage u_1 after the first ZCC period. The capacitor voltage u_C must be the ZCC voltage value u_3 after the t_{fw} period ends. Somewhere in the middle, the t_a period ends and t_{fw} starts, with the voltage u_2 in that point. The filter inductor current has its peak in this point. In (b), the graphs are visually arranged such that the solution method can be seen. The initial value u_1 and the positive-advancing time filter voltage function meets with the initial value u_3 and the negative-advancing time voltage function in some point with u_2, where also the function derivatives must be equal. u_2 does not need to be known. The equation pairs of voltage and derivative functions yield the two unknowns t_a and t_{fw}.

after time t_a. In forward-time sense, the backward-time equation sets a final value and gives the initial value after t_{fw}. The system of equations to be solved is shown if Equation B.4.

$$\begin{cases} U_{DC}\left[1-\cos\left(\omega_f t_a\right)\right] - Z_f I_{out}\sin\left(\omega_f t_a\right) + u_1\cos\left(\omega_f t_a\right) = \\ \qquad -Z_f I_{out}\sin\left(-\omega_f t_{fw}\right) + u_2\cos\left(-\omega_f t_{fw}\right) \\ U_{DC}\,\omega_f\sin\left(\omega_f t_a\right) - Z_f I_{out}\,\omega_f\cos\left(\omega_f t_a\right) - u_1\,\omega_f\sin\left(\omega_f t_a\right) = \\ \qquad -Z_f I_{out}\,\omega_f\cos\left(-\omega_f t_{fw}\right) - u_2\,\omega_f\sin\left(-\omega_f t_{fw}\right) \end{cases} \tag{B.4}$$

The equation system can be solved by first noticing that the angular argument inside the trigonometric functions has similarities such that a phasor addition can be made for both sides in each equation. The individual trigonometric functions are effectively grouped, and the equation only involves phasors with magnitude and angle arguments. Since the angular frequency of the phasors is the same, each equation has a solution similar to a vector sum. These intermediate steps then result in an equation with a phasor sum in one sine function, and the final solution for t_a and t_{fw} is obtained with inverse sine. By substituting the initial voltages by inverting about U_{DC}, the final solutions for t_a and t_{fw} and their phasor arguments have identical forms. The inverted voltage arguments are shown in Equations B.5 and B.6. The phasor arguments are given in Equations B.7 and B.8, and the final solutions for t_a and t_{fw} in Equations B.9 and B.10. The phasor sum method can be found in any suitable mathematics handbook. The solution method was found to be relatively straightforward but lengthy and

prone to errors in the intermediate step when solved manually.

$$u_{1,\mathrm{rev}} = U_{\mathrm{DC}} - u_{\mathrm{ZCC2}} \tag{B.5}$$

$$u_{2,\mathrm{rev}} = U_{\mathrm{DC}} - u_{\mathrm{ZCC1}} \tag{B.6}$$

$$\begin{aligned} a_1 &= Z_{\mathrm{f}} I_{\mathrm{out}} \\ b_1 &= -u_2 \\ r_1 &= \sqrt{a_1^2 + b_1^2} \\ \phi_1 &= \arctan \frac{b_1}{a_1} \end{aligned} \tag{B.7}$$

$$\begin{aligned} a_2 &= Z_{\mathrm{f}} I_{\mathrm{out}} \\ b_2 &= -u_{2,\mathrm{rev}} \\ r_2 &= \sqrt{a_2^2 + b_2^2} \\ \phi_2 &= \arctan \frac{b_2}{a_2} \end{aligned} \tag{B.8}$$

$$t_{\mathrm{a}} = \tau_{\mathrm{f}} \left(\arcsin \left[\frac{u_{1,\mathrm{rev}}^2 - u_{2,\mathrm{rev}}^2 - 2U_{\mathrm{DC}} u_{1,\mathrm{rev}}}{2U_{\mathrm{DC}} r_2} \right] + \phi_2 \right) \tag{B.9}$$

$$t_{\mathrm{fw}} = \tau_{\mathrm{f}} \left(\arcsin \left[\frac{u_1^2 - u_2^2 - 2U_{\mathrm{DC}} u_1}{2U_{\mathrm{DC}} r_1} \right] + \phi_1 \right) \tag{B.10}$$

Appendix C

Measurement error and uncertainty analysis

Uncertainty in edge delays and simulations

The values for the delays in the simulations are based on measurements from the physical VFD test setup. The turn-off process is based on the u_G model. The uncertainty of the delay look-up table values is the estimated reading error from the measurement device (oscilloscope), combined with the uncertainty of the test case parameters such as load current, U_{DC} voltage, and module temperature. The method for reading the virtual delay involves using the output voltage integral waveform, and reading its tangent intercept point on the scope x-axis, where the initial voltage level is found. The method was described in Figure 3.10. There is a possibility of error while reading the intercept point. The logic-level gate drive signal had some high-frequency ripple at its edges, and determining the exact location of the gate drive signal toggling could not be known with better than $\pm$10 ns uncertainty. The voltage integral tangent should have been drawn from the steady-state condition, as the voltage edge itself has a distorted integral tangent. Drawing the tangent too early causes the slope to deviate, and the x-intercept point does not give the virtual delay accurately. This process also has an uncertainty of $\pm$10 ns, which was determined by trying out different tangent lines from the worst-case edge waveforms. This would give a pessimistic estimate for the combined uncertainty of $\pm$20 ns for all the delay look-up table values.

The uncertainty estimate should also include the effect of measurement uncertainty of the test point load current, U_{DC} voltage, and module temperature. Their effect can be included by using the partial differential method. The uncertainty of the voltage and current values is $\pm$1% for both the voltage and current measurements, and $\pm$ 2% for the temperature measurement. In Equation 3.2, the slope of the regression function estimating the effect of the U_{DC} voltage in the delay values is 240 ps (picoseconds) per each volt in U_{DC}, and having a nominal U_{DC} voltage of 600 V, $\pm$1% U_{DC} causes a $\pm$1.44 ns uncertainty in the timing value. Compared

with the reading error caused by the visual intercept method ($\pm$20 ns, combined), the effect of the U_{DC} variation is small. Using a similar regression method for the current, the point of the highest slope in the delay look-up table graph occurs at the $\mathrm{IGBT_L}$ turn-on, where the delay slope is 0.9 µs per a 100 A current difference. The $\pm$1% at the peak current is $\pm$1 A, a deviation that would cause a $\pm$9 ns deviation in the delay value. This is quite significant, and thus, the total edge delay uncertainty should be combined again, giving $\pm$30 ns. The effect of temperature variations is so small that it causes no significant change in this figure. Thus, the final conclusion is that no delay value should be considered to be more accurate than having and uncertainty of $\pm$30 ns.

When the S_{OE} results are compared, the uncertainty of the figures should be taken into account. A relevant question is for instance whether the 10.9% and 11.3% S_{OE} results show a significant difference, or if the difference is due to some error sources in the process. Although the ADUDT algorithm in itself is an analytical solution (with t_{ZCC2} solved numerically, but the solution can be made arbitrarily precise), the S_{OE} calculation process involves measured and estimated inputs, the delay measurements, and the u_{G} model. These will have some error, and consequently, the S_{OE} is also assumed to have uncertainty, but in which limits?

The ADUDT phase leg simulation model produces a small error artifact owing to the limited calculation sample step. This was seen as a small nonzero S_{OE} value even with all the timing distortions turned off. Then, the virtual edge delays are determined by measurements, and as such, have error. The u_{G} model can produce turn-off voltage edge delays that deviate from the real-world device results. But what should be the reference point of the delay and u_{G} model accuracy? The study in this thesis took one VFD for a case study. Even if the delay models used in the simulations did not correspond with the test setup, assuming the error present, it could be that some other VFD equipment has exactly the kind of delay behavior as simulated by the delay model applied here. This means that the results should not be compared with any particular physical test setup results, but with each other. Then, the S_{OE} differences will give answers about the differences in the ADUDT settings.

ADUDT is such a complex and nonlinear system that the traditional compound uncertainty by partial differentials in an analytical form would be challenging, perhaps even impossible. Deviations in the pattern edge timings cause nonlinear effects, and this can already be seen by inspecting the ADUDT sequence graphs. Indeed, if the timing uncertainty effect on the output S_{OE} could be expressed analytically, the complex method of phase leg simulations would not be needed. Venturing into the analytical solution of the S_{OE} uncertainty could be in the scope of future work.

The approach for edge uncertainty and S_{OE} error taken here is completely based on the phase leg simulation model. Additional script was made in the simulator to test the deviation effect. The script forms all the possible combinations for the delay error, simulating the cases and giving the answer for the upper and lower bounds of S_{OE}. One such example result is shown in Figure C.1. There, the reference upper half S_{OE} envelope of the test case in 5.3(b) is shown in bold. The tolerance bands were simulated with an improved step size of 2 ns, giving less error owing to the simulation step. Assuming an uncertainty of $\pm$30 ns in the delay values,

the tolerance band mean value is 4.29% units (S_{OE}units), with relative deviation width of $\pm$21%. The reference simulated test case has an upper half S_{OE} value of 4.42 %-units. The reference envelope graph is inside the tolerance band, but could exceed the band as a result of a difference in the simulation step size, thereby increasing the error.

The relative tolerance band is quite large, with the absolute deviation about the mean value being approximately 0.9 S_{OE} units. This would imply that with S_{OE} result differences smaller than approximately $\pm$1.0 S_{OE} units, no significance should be assumed. This rules out several values in Table 5.3 from a viable comparison. However, if the shape of the envelope is completely different between the compared cases, even if the tolerance band is taken into account, the difference must be significant. Thus, encelope results cannot be compared by just looking at the S_{OE} values.

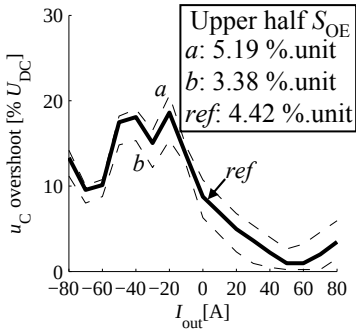

Figure C.1. If the virtual delays have an uncertainty of $\pm$30 ns, the S_{OE} figure shows tolerance bands of $\pm$0.9 %-units.

We may ask why the S_{OE} uncertainty is considered as a tolerance band, giving lower and upper bounds for the simulation results. How can the S_{OE} become smaller with delay value uncertainties spread in all edges? This is naturally due to the fact that with a suitable combination of edge timing variations, the effect is that the total error in the pulse sequence becomes smaller, that is, the deviations act as a delay compensation for the neutral values, thus producing a sequence that is close to the ideal ADUDT case, and giving a smaller overshoot error. Whether this actually happens in a real device has not been analyzed here. To be on the safe side, the lower and upper bounds of the S_{OE} tolerance band are considered the real uncertainty of the S_{OE} result.

Gate voltage model

The u_G model parameter variations can have an error of their own when the u_G model is used in the turn-off edges. The variation effects are discussed in the u_G model in Appendix A, but a thorough uncertainty analysis is not yet included. It is assumed that the $\pm$30 ns uncertainty also covers any effects caused by the u_G model. For the u_G model, an analytical uncertainty analysis could be made as the model is expressed in an analytical form.

Heat sink thermal resistance loss measurement method

Loss measurements and their uncertainty analysis are crucial for the conclusions in this work. Whereas the calorimeter method is relatively accurate compared with the results, and the method uncertainty analysis has been studied and published for instance in (Kosonen et al., 2013), the ΔT method using the estimated heat sink thermal resistance can potentially have a larger uncertainty as some comparisons between the loss measurement methods pointed out. Since the SiC measurements were carried out using the ΔT method exclusively, it is important to know how reliable the results are. The method is based on Newton's equation of heat transfer in convection in Equation C.1 (Incropera et al., 2006)

$$q = hA\Delta T \tag{C.1}$$

where q is the heat transfer per unit of time (thus, the loss power being cooled in the steady state), h is the convection heat transfer coefficient, A is the heat transfer surface area, and ΔT is the temperature difference between the heat sink and the ambient (inlet) air. q can be related to thermal resistance by $R_{\text{th}} = \frac{\Delta T}{q}$. A simplified assumption is now made that the flow mode is constant such that A can be assumed constant. Furthermore, the whole heat sink is viewed as having uniform heat transfer constant over its surface. The convection coefficient is now hypothesized to be subject to change if fluid properties change as a result of an ambient temperature change. Estimating the heat transfer coefficient and its dependence on air properties is a problem of its own, and the estimation shown here is based on free convection rather than forced convection simply because it was the only estimation available and relatively easy to analyze. It assumes turbulent flow along vertical plate. It is then assumed that the forced convection is less or equally dependent on the air properties as suggested by this simple analysis, at least giving a hint how much the heat transfer coefficient could change. Using free convection properties from (Incropera et al., 2006), the equation for h can be written:

$$h = C\left(\frac{\beta k^3}{\nu\alpha}\right)^{\frac{1}{3}} \tag{C.2}$$

In Equation C.2, C is a constant including all physical dimension-related constants and natural constants of the equation, so C can be considered constant. The rest are the fluid properties; k is the thermal conductivity, ν is the kinematic viscosity, α is the thermal diffusivity, and β is the thermal expansion coefficient. For air in temperatures 300 K and 350 K, this equation gives a decrease of 8% in the value of h when the ambient temperature increases. If the fluid properties are interpolated and calculation repeated for temperatures of 20 °C and 40 °C, the decrease in h is 3%. Thus, it can be concluded that up to a 3% increase in the thermal resistance R_{th} caused by an ambient temperature rise could be explained by this simple analysis. However, if the measurements are made in a relatively constant ambient temperature, the effect of changing fluid properties should be small compared with the uncertainty of the temperature measurements. If the thermal resistance is higher in reality than assumed, the actual power loss is lower than calculated by this method.

The thermal resistance uncertainty also depends on the air flow characteristics, and any disturbance in the setup that would shunt away some part of the heat such that it would effectively

change the thermal resistance. The mechanical assembly was not changed between the loss measurements or R_{th} characterization, and thus, no heat shunting effect should be possible with the loss measurements.

The result for the loss and its uncertainty is also due to the temperature difference between the inlet air and heat sink temperatures. If the temperature measurement locations in the heat sink surface and the inlet air duct are kept constant, and the shape and distribution of the heating elements in the thermal resistance characterization test are the same as in the actual loss measurements, the effects caused by these location differences are minimized and should be small, leaving the temperature measurement error as the source of uncertainty. It is not possible to know if the heat loss between the IGBT modules is unbalanced, and this will unarguably result in a measurement error that is difficult to estimate. Further, it is assumed that all modules have even dissipation. Thus, assuming that the thermal resistance has no significant uncertainty, the only error source would be from the temperature measurements. Nevertheless, this is not the case, as the thermal resistance also has some uncertainty.

For the temperature measurements, the DIN class A RTD sensors have a resistance of (100 $\pm$0.06) Ω at 0 °C, and their temperature reading uncertainty is given as $\pm(0.15 + 0.002[T])$, where $[T]$ is in °C (IEC, 2008). This would be an uncertainty of $\pm$0.19 °C at 20 °C measurement temperature, and $\pm$0.23 °C at 40 °C. Table C.1 shows how the measurement uncertainty affects the interpretation of temperature difference results, assuming a 20 °C ambient temperature and $R_{\text{th}} = 0.033$ K/W. the largest error is assumed for the temperature difference, in both directions.

Table C.1. Effects of RTD temperature measurement uncertainty.

Indicated ΔT [K]	True ΔT [K]	True P_{th} [W]	P_{th} uncertainty
5	4.61–5.39	140–163	$\pm$7.8%
10	9.60–10.40	291–315	$\pm$4.0%
15	14.59–15.41	442–467	$\pm$2.7%
20	19.58–20.42	593–619	$\pm$2.1%
25	24.57–25.43	745–771	$\pm$1.7%
30	29.56–30.44	896–922	$\pm$1.5%

Some amount of thermal resistance variation can be combined with the temperature measurement uncertainty. It is also possible that the inlet air temperature reading gives false results because of other heating effects, such as radiated heat from the surrounding equipment. Without further qualification of the method, it is actually not possible to say what the actual loss measurement uncertainty is. At this point, the uncertainty is taken as $\pm$5% for losses in the range of 300 W–1000 W, and $\pm$10% for losses less than 300 W, down to 100 W.

Appendix D

Phase leg simulator details

The phase leg simulator is implemented as a group of MATLAB scripts. In the core of the simulator there is a loop that calculates the filter u_C and i_L, using the filter voltage and current equations. The input voltage depends on the switch states in the leg, and thus, the conduction of virtual IGBTs and diodes is also tracked for each calculation step. A gate command input change and a phase leg current zero crossing can trigger a phase leg status change, which then sets the simulated leg output voltage and thereby the filter input voltage accordingly. The result is a piecewise continuous presentation of the filter voltage and current. The timing distortion effects are included by having a dedicated gate command delay subroutine between the virtual IGBT gates and the gate command data structure. The delay subroutine uses the measured timing delay look-up tables and the u_G turn-off model, but also allows the use of any arbitrary delay values. The block diagram of the simulation model is shown in Figure D.1.

SIMULATOR_TOPLEVEL

```
BEGIN SIMULATOR_TOPLEVEL:
initialize;
user_parameters;

FOR sweep = start TO stop WITH step
{
 FOR edge_polarity = 0 TO 1
 {
  CALL simulator_loop;
 }
 CALL store_results;
}
```

GATE_DRIVE_GENERATOR

```
BEGIN GATE_DRIVE_GENERATOR:
IF simulation just started
{
 ADUDT algorithm; //Calculated only once
}

state machine
{
 IF 0 <= t_sim < t1
 {
  update gate drive commands;
 }
 ELSEIF t1 <= t_sim < t2
 {
  update gate drive commands;
 }
 .
 .
 .
}
```

IGBT_DELAYS

```
BEGIN IGBT_DELAYS:
initialize;
create delay ring buffers;

push input gate drive commands to ring buffers;

READ delay value from LUT;
update u_G model and calculate turn-off delay value;

relocate ring buffer delay tap locations;
output gate drive commands from delay taps;
```

PHASE_LEG_MODEL

```
BEGIN simulator_loop:
BEGIN PHASE_LEG_MODEL:
READ timing LUTs;
initialize;
solve initial leg_status based on initial current and gate commands;
```

```
WHILE t_sim <= max
{
 WHILE BreakCondition = 0
 {
  IF Leg_floating = 0
  {
   filter voltage and current equations;
  }
  ELSE
  {
   filter voltage and current equations for floating leg;
   IF u > Udc OR u < 0
   {
    BreakCondition = 1;
   }
  }
  CALL GATE_DRIVE_GENERATOR;
  CALL IGBT_DELAYS;
  re-evaluate phase leg status;
  IF (new status is changed)
  {
   BreakCondition = 1;
  }
 }
 find the reason for BreakCondition;
 re-evaluate phase leg status;
 BreakCondition = 0;
 initialize voltage and current equations;
}
```

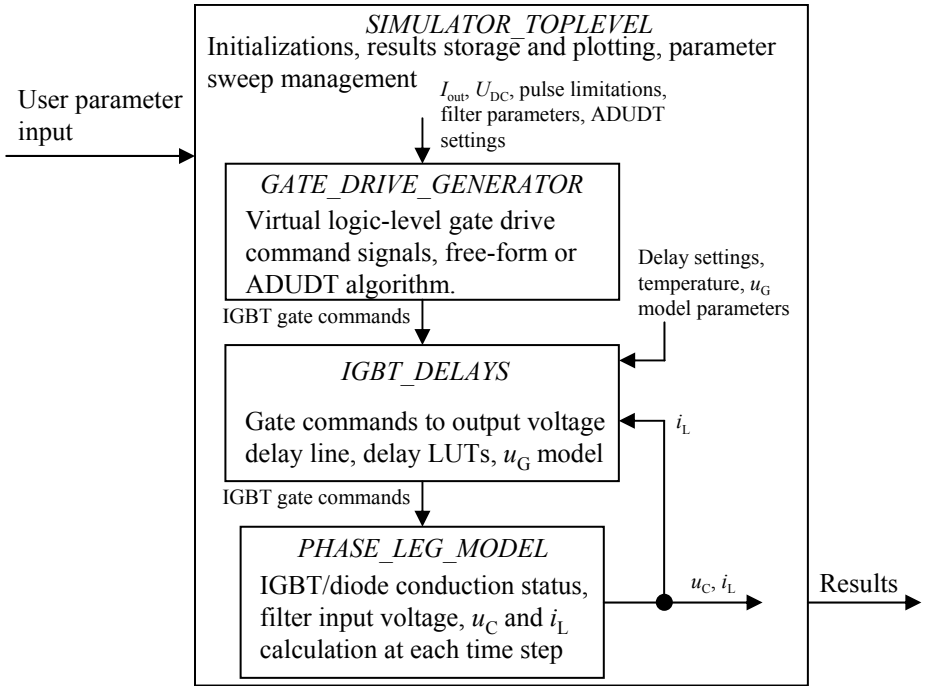

Figure D.1. *SIMULATOR_TOPLEVEL* contains the subroutines for gate drive command generation, phase leg, filter, and delay simulator blocks. The measured timing distortion look-up tables are inside the *IGBT_DELAYS* routine. The ADUDT algorithm is precalculated in *GATE_DRIVE_GENERATOR*, after which the routine outputs the gate drive commands in the calculation loop. *PHASE_LEG_MODEL* simulates the filter voltage and current, and feedbacks the filter current to the phase leg status routine for commutation status change purposes.

Appendix E

Experimental setup, detailed information

Table E.1. AC induction motors used in the test setups. (Tyster et al., 2011), ©2011 IEEE.

Component	Value/Description	Unit
5.5 kW motor		
Manufacturer	ABB	
Model	M2QA132S4A	
Voltage	380-420	V
Current	11.3	A
Frequency	50	Hz
Power factor (cos ϕ)	0.85	-
Nominal speed	1430	rpm
22 kW motor		
Manufacturer	Strömberg	
Model	HXUR 368G2 B3	
Voltage	380	V
Current	43	A
Frequency	50	Hz
Power factor (cos ϕ)	0.86	-
Nominal speed	1460	rpm
45 kW motor		
Manufacturer	ABB	
Model	M2AA 225 SMB 4	
Voltage	400	V
Current	83.9	A
Frequency	50	Hz
Power factor (cos ϕ)	0.83	-
Nominal speed	1479	rpm

Table E.2. Passive filter electrical specifications.

Component	Value/Description	Unit
Passive dudt filter PDUDT		
Model	Platthaus DUT-0055-6-0-P	
Phase inductance at 50 Hz	197	µH
Phase inductance at 10 kHz	169	µH
Capacitors	4.7	nF
Capacitor connection	Wye, star point left floating	
Additional resistors	3×220 kΩ, paral. with capacitors	
Manufacturer rated line-to-line voltage	690	V
Rated phase current at 40 °C ambient	55	A
Rated maximum switching frequency	3.6	kHz
Rated maximum fundamental frequency	70	Hz
Voltage step response overshoot	58	%
Undamped resonant frequency	230	kHz
Quality factor Q	2.4	
Sine filter		
Model	Platthaus 3REG-0052-6-0-P	
Phase inductance at 50 Hz	1.65	mH
Phase inductance at 10 kHz	1.49	mH
Capacitors	18	µF
Capacitor connection	Delta	
Additional resistors	-	
Manufacturer rated line-to-line voltage	690	V
Rated phase current at 40 ° C ambient	52	A
Rated minimum switching frequency	1.5/3.6	kHz
Rated maximum fundamental frequency	70	Hz
Voltage step response overshoot	Not tested	%
Undamped resonant frequency	810	Hz
Quality factor Q	32	

Table E.3. ADUDT filter electrical specifications.

Component	Value/Description	Unit
Active dudt filter (ferrite/air gap) ADUDT_Fe		
Phase inductance at 50 Hz	16.0	µH
Phase inductance at 10 kHz	15.2	µH
Capacitors	330	nF
Capacitor connection	Wye, star point in DC-	
Additional resistors	-	
Manufacturer rated line-to-line voltage	-	
Rated phase current at 40 °C ambient	Limits not tested	
Rated minimum/maximum switching frequency	Limits not tested	
Rated maximum fundamental frequency	Limits not tested	
Voltage step response overshoot	98	%
Resonant frequency	71	kHz
Quality factor Q	37	
Active dudt filter (air-core) ADUDT_Air		
Phase inductance at 50 Hz	14.9	µH
Phase inductance at 10 kHz	14.3	µH
Capacitors	330	nF
Capacitor connection	Wye, star point in DC-	
Additional resistors	-	
Manufacturer rated line-to-line voltage	-	
Rated phase current at 40 °C ambient	Limits not tested	
Rated minimum/maximum switching frequency	Limits not tested	
Rated maximum fundamental frequency	Limits not tested	
Voltage step response overshoot	96	%
Resonant frequency	74	kHz
Quality factor Q	55	

Table E.4. Filter mechanical specifications.

Component	Value/Description	Unit
Passive d*u*/d*t* filter		
Core material	Laminated steel + air gap	
Mass	14	kg
Dimensions (w×d×h)	190×130×250	mm
Number of strands in winding conductor	56	
Bundling scheme (bundles × strands)	7 × 8	
Strand conductor diameter (copper)	0.58	mm
Strand insulation	No	
Total copper cross-sectional area	14.8	mm^2
Sine filter		
Core material	Laminated steel	
Mass	44	kg
Dimensions (w×d×h)	300×250×310	mm
Number of strands in winding conductor	91	
Bundling scheme (bundles × strands)	7 × 13	
Strand conductor diameter (copper)	0.58	mm
Strand insulation	No	
Total copper cross-sectional area	24.0	mm^2
Active d*u*/d*t* (ferrite/air gap)		
Core material	Ferrite 3C90 Ferroxcube	
Mass	5.5	kg
Dimensions (w×d×h)	235×170×310	mm
Number of strands in winding conductor	51	
Bundling scheme (bundles × strands)	6 × 7 + 9 in center	
Strand conductor diameter (copper)	0.5	mm
Strand insulation	Yes	
Total copper cross-sectional area	10.0	mm^2
Active d*u*/d*t* (air core)		
Core material	Air	
Mass	2.4	kg
Dimensions (w×d×h)	280×150×130	mm
Number of strands in winding conductor	7	
Bundling scheme (bundles × strands)	1 × 7	
Strand conductor diameter (copper)	1.3	mm
Strand insulation	No	
Total copper cross-sectional area	9.3	mm^2

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