LUT University

NEUTRAL POINT CLAMPED CONVERTER PHASE-LEG LAYOUT OPTIMIZATION

Abstract

Henri Tulla

Neutral point clamped converter phase-leg layout optimization

The target of this thesis is to idealize a three-level Neutral Point Clamped (NPC) converter phase-leg layout for an Active Front End (AFE). This includes selecting a suitable power module type for the phase-leg and then optimizing the power module layout and laminated busbar structure for low commutation loop inductances. The performance of the converter layouts is assessed with loop inductance and Double Pulse Test (DPT) simulations.

In order to optimize the phase-leg layout a brief literature review of converter layout optimization methods and NPC topology is done. As a multilevel topology NPC has several commutation loops which complicates the layout optimization process. The topology's commutation behaviour is analysed and then the general laminated busbar design rules are applied for the phase-leg. A set of suitable power modules is selected for the converter to be used in simulations and in a future prototype.

In total five different phase-leg layouts are designed and their commutation loop inductances and DPT behaviours are simulated. Based on the simulation results there are some differences in the commutation loop inductances between the layouts but all the proposed layouts are feasible for further development and to be considered for the final three-phase converter layout. They are currently however in just a proof of concept state and will need a lot of optimization before they can be used as a part of the final product.

Tiivistelmä

Henri Tulla

NPC-vaihehaaran kiskostorakenteen optimointi

Tämän diplomityön tavoitteena on optimoida kolmitasoisen NPC-konvertterin vaihehaaran rakenne verkkotasasuuntaajasovellukseen. Tähän sisältyy vaihehaaralle sopivan tehomoduulityypin valinta ja tehomoduulien sijoittelun ja moduuleita yhdistävän laminoidun kiskostorakenteen optimointi kommutointi-induktanssien näkökulmasta. Suunniteltujen rakenteiden toimintaa analysoidaan kommutointi-induktanssi- ja tuplapulssitestisimulaatioilla.

Kirjallisuuskatsauksessa selvitetään laminoidun kiskostorakenteen optimoinnin periaatteet ja perehdytään NPC-topologian vaihehaaran rakenteeseen ja sen kommutointiin. NPC on monitasoinen topologia ja sillä on useita kommutointireittejä, mikä tekee vaihehaaran optimoinnista hankalaa. Vaihehaaraan valitaan tehomoduulit joiden parametreja voidaan käyttää simuloinneissa ja joita voidaan myöhemmin käyttää prototyyppilaitteessa.

Viiden erilaisen tehomoduuliasettelun ja kiskostorakenteen kommutointi-induktanssit selvitetään induktanssisimulaatioilla ja kytkentähetken ilmiöitä tarkastellaan tuplapulssitestisimulaatioilla. Simulaatiotulosten perusteella esitetyissä vaihehaararakenteissa on pieniä eroja kommutointi-induktansseissa, mutta niitä kaikkia voidaan harkita kolmivaiheisen konvertterin vaihehaararakenteeksi. Kaikki esitetyt kiskostorakenteet ovat kuitenkin vasta prototyyppiasteella ja niiden tuotteistettavuus ja kokoonpantavuus täytyy optimoida erikseen ennen kuin niitä voi käyttää valmiissa konvertterissa.

Acknowledgements

Symbols and abbreviations

Roman characters

C	capacitance	[F]
D	diode	
L	inductance	[H]
N	neutral point	
P	power	[W]
U	voltage	[V]
di/dt	current slew rate	[A/s]
f	frequency	[Hz]
sw	switch	
t	time	[s]
u	voltage	[V]

Constants

π	pi	3.14159...

Subscripts

σ	total value
-	negative
+	positive
f	fall
BB	busbar

C	capacitor, collector
cr	critical
CE	collector - emitter
D	diode
DC	DC link
peak	peak value
L	line
L-L	line to line
L-N	line to neutral
Long	long commutation loop
Loop	commutation loop
max	maximum value
N	neutral point
res	resonance
Short	short commutation loop
SF	safety margin
SW	switch

Abbreviations

2D	two dimensional
3D	Three Dimensional
AC	Alternating Current
AFE	Active Front End
ANPC	Active Neutral Point Clamped
CAD	Computer Aided Design
CharIN	Charging Interface Initiative e. V.
DC	Direct Current
DPT	Double Pulse Test

DUT	Device Under Test
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
EV	Electric Vehicle
EVSC	Electric Vehicles Smart Charging
EVSE	Electric Vehicle Supply Equipment
FEM	Finite Element Method
GaN	Gallium Nitride
IEA	International Energy Agency
IEC	International Electrotechnical Commission
IGBT	Insulated Gate Bipolar Transistor
L–N	Line to Neutral
MCS	Megawatt Charging System
MoM	Method of Moments
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NPC	Neutral Point Clamped
PCB	Printed Circuit Board
PEEC	Partial Element Equivalent Circuit
PFC	Power Factor Correction
RLCG	resistance, inductance, capacitance and conductance
SAE	Society of Automotive Engineering
SDO	Standards Development Organization
Si	Silicon
SiC	Silicon Carbide
THD	Total Harmonic Distortion
V2G	Vehicle to Grid

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1 Introduction

As the world is moving away from fossil fuels and towards net zero emissions the significance of Electric Vehicles (EVs) increases in both passenger and commercial vehicles (UN-FCCC, 2023; IEA, 2023). In order for the EVs to be a more appealing alternative for their counterparts fitted with internal combustion engines they need to have a long enough operating range. This can be achieved by fitting them with larger capacity battery packs but this also creates the need for higher power charging infrastructure to charge up the batteries faster.

Need for higher battery capacity and charging power have already led to higher voltages in commercial EV batteries and drivetrains in order to keep the currents smaller. The electrification of commercial transport vehicles in large scale introduces new challenges for the battery and charging technologies (Habib et al., 2020). As the commercial vehicles are larger in comparison to passenger vehicles they need larger battery capacities to begin with but the driving patterns of commercial transport also poses additional challenges for charging (CharIn, 2022).

In this thesis the goal is to design a three-level Neutral Point Clamped (NPC) phase-leg busbar layout for an Active Front End (AFE). Basic structure of a three-level NPC phase-leg consisting of four semiconducor switches, two clamping diodes and two capacitors (Baker, 1979) is shown in Figure 1. The main design goal is to optimize commutation loop inductances in a way to minimize voltage overshoot amplitudes during operation.
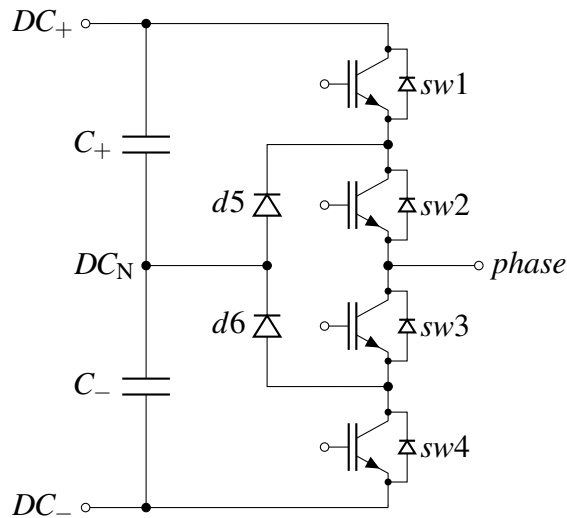
Figure 1: Basic structure of a three-level NPC phase-leg with DC link is on the left and phase connection on the right side.

Additional design constraints are to use standard off the shelf power modules and to find a module type which is available from several manufacturers to ensure component availability. This phase-leg will be part of a three-phase bi-directional grid interface in a high power EV charging station but for this thesis the scope was set to optimizing a single phase-leg to keep the work load reasonable.

Converter layout design has already been researched and the fundamentals to reduce parasitic inductances are well understood (Popova et al., 2012; Mattsson et al., 2022; Skibinski & Divan, 1993; Schanen et al., 1996; Zare & Ledwich, 2002; Popova et al., 2014) but in this thesis those are applied for the NPC topology. To better understand the topology's requirements for the busbar design the NPC phase-leg structure and fundamentals of the phase-leg's commutation are studied. Available power modules are surveyed to find what options are currently available and then a laminated busbar structure is applied for the NPC phase-leg and five phase-leg layout designs are created.

To evaluate the busbar designs Ansys Electronics Desktop simulation software is used to analyse commutation loop inductances and perform Double Pulse Test (DPT) simulations for the phase-leg designs. An option for a lab prototype of the phase-leg was also discussed but unfortunately there was no time left for this during the thesis.

2 High power EV charging

As the world is moving away from fossil fuels the demand for heavy duty EVs increases which creates the need for new higher power charging stations. As the existing EV battery reserve increases new ways to better utilize the capacity when the vehicles are not on the road are also researched. These include but are not limited to the ability to use the batteries as a part of the power grid by supplying energy for voltage and frequency regulation and peak load shaving. This imposes new requirements for the charging stations like ability to move power in both directions between the vehicle battery and the grid.

2.1 Road transport electrification

At the time of writing road transportation still relies heavily on fossil fuels despite the number of EVs increasing every year. According to International Energy Agency (IEA) in 2022 road transport produced over 15% of global energy-related emissions, nearly 6.2 Gt (IEA, 2022a; IEA, 2022b). EVs are seen as a key technology for greener road transportation with less emissions and better air quality especially in urban areas (Buekers et al., 2014; IEA, 2023). In December 2023 at the United Nations climate change conference it was agreed on to begin phasing out the use of fossil fuels globally (UNFCCC, 2023) which will most likely further emphasize the importance of EV development.

According to IEAs estimates (IEA, 2023) during 2023 18% of new passenger cars sold will be electric. Lacking battery technology and lack of charging infrastructure have been major slowing factors for spread of EVs resulting to a low available range and long charging time which made them unappealing for most of the consumers (Aghajan-Eshkevari et al., 2022) and now the heavy-duty EVs are facing the same problems. In 2022 number of sales of electric buses was 4.5% and electric trucks 1.2% of total bus and truck sales worldwide (IEA, 2022c).

As the society transitions towards net zero emissions with increased amount of renewable energy production like solar and wind the variability of energy production increases. At the same time the total and peak demand of electricity increases as the transport sector and domestic heating are electrified. In order to utilize the existing power grid capacity as well as possible and avoid the need for comprehensive infrastructure strengthening new solutions like Electric Vehicles Smart Charging (EVSC) are needed for load balancing. (Vahidinasab & Mohammadi-Ivatloo, 2022a)

With EVSC the battery charging can be scheduled for times when renewable electricity production exceeds the other demand on the grid therefore reducing the need for non-renewable

production methods and for times when other electricity demand is low to reduce the required peak power (Shi et al., 2020; Buekers et al., 2014). Vehicle to Grid (V2G) technology makes bidirectional energy flow between EVs and the power grid possible allowing EVs batteries to be used for example for voltage and frequency regulation, peak load shaving and load leveling (Tan et al., 2016). From the point of smart grids EVs could even act as temporary electricity storage alongside fixed energy storage systems if the battery capacity is large enough (Aghajan-Eshkevari et al., 2022).

2.2 High power EV charging

As the electric passenger cars have taken their place in society they have brought with them a handful of charging standards and technologies. Different Standards Development Organizations (SDOs) including International Electrotechnical Commission (IEC) and Society of Automotive Engineering (SAE) have issued numerous charging standards with both Alternating Current (AC) and Direct Current (DC) charging and varying voltage, current and power levels as well as different types of charging connectors and communication protocols (Habib et al., 2020; R. Singh et al., 2022; Vahidinasab & Mohammadi-Ivatloo, 2022b).

The system that converts grid power to DC and supplies it to the EVs battery pack is called Electric Vehicle Supply Equipment (EVSE) but is generally referred to as EV chargers. Based on the type of used charging current and location of the power electronics converter used to convert the grid's AC to DC for supplying the batteries EV chargers can be divided into AC (on-board) and DC (off-board) chargers (Habib et al., 2020; R. Singh et al., 2022).

The higher charging powers and speeds can be achieved with DC chargers since the converters integrated into EVs are small and relatively low power due to size, weight and cost limitations (R. Singh et al., 2022). Standardized on-board charger's maximum power is 120 kW while for off-board chargers it is 1–2 MW (Habib et al., 2020). Integrating high power chargers in vehicles might not be very cost effective since they are costly to manufacture and charger utilization rate would be low compared to public charging stations.

As the on board chargers are often used for charging at residential properties and with single-phase connection they are optimized for that. Typical on-board EV chargers have a nominal charging power of 6.6–11.5 (Khaligh & D'Antonio, 2019). Even if there were more power available for the charger the smaller charging current increases the lifetime of the battery pack atleast with the current battery technologies.

While EVs are slowly taking place in transportation industry with electric trucks and buses, need for new higher power charging technologies and infrastructure is also there to charge

the new higher capacity batteries in reasonable time. It has been understood that in order
to electrify the heavy-duty commercial vehicles in larger quantities the charge times need to
cohere with drivers mandatory break times (CharIn, 2022). Nominal charging power of 1.4
to 250 kW for majority of the current passenger car charging standards is not enough for this
(Habib et al., 2020).

One problem introduced by the numerous charging standards and technologies for passenger
vehicles is that a charger designed for one type of car cannot necessarily charge a car from
other manufacturers. This leads to a need for excessive amount of charging infrastructure
to be able to offer charging to all vehicles. In order to avoid this fragmentation with heavy-
duty vehicles Charging Interface Initiative e. V. (CharIN) has published a whitepaper about
Megawatt Charging System (MCS) (CharIn, 2022). The paper describes recommended MCS
specifications including charging connector, communication protocol during the charging
process and voltage and power levels to ensure compatibility between chargers and vehicles.

2.3 EV charging system

The interface between the EVs battery pack and power grid is the EVSE. The energy flow
between the grid and batteries can be one-directional from grid to batteries or bi-directional
if the charger supports V2G and can also supply power to the grid. For the scope of this thesis
we are mainly interested in the power electronic side of the EVSE and pay less attention to
the other factors like control and automation systems, mechanical design and user interfaces.

2.3.1 Typical EV charger structure

A typical off-board bidirectional EVSE block diagram for is shown in Figure 2. An unidi-
rectional system has the same basic components but in place of AFE there is a rectifier stage
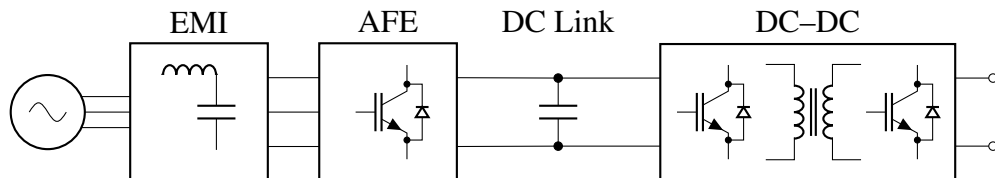with Power Factor Correction (PFC) capability.

Figure 2: Typical block diagram for a bidirectional off-board EV charger. The grid connec-
tion is on the left and connection to the vehicle charging port on the right side.

Starting from the left the first block from the grid is a Electromagnetic Interference (EMI)
filter to maintain grid's power quality. After the filter is an AFE or in case of an unidirectional

EVSE a some type of rectifier to convert the AC from the grid to DC. After the rectifier stage both topologies have an intermediate circuit commonly referred to as a DC link to temporarily store the energy and after that an isolated DC–DC converter. The converter stage allows to match the charger output voltage with the battery voltage in order to avoid a current rush when the charger is connected and to control the charging voltage and current independent from the grid and DC link voltages.

In bidirectional systems the DC–DC converter must be bidirectional to allow the power to also flow from battery to grid. Galvanically isolating the charger output from the grid provides additional safety for charging and is often required by safety standards (CharIn, 2022; Khaligh & D'Antonio, 2019). The DC–DC converters use relatively high switching frequency compared to the grid voltage to keep the size of the transformer and filter components small.

2.3.2 Charging system in question

The charging system in question is intended for heavy-duty vehicles with a higher nominal charging power compared to EVSEs discussed in Section 2.3.1. To raise the power level either the charging voltage or charging current or both must be increased. Usually since conducting losses are proportional to the square of the current it's better to increase the voltage if possible. Preliminary block diagram for this charging system is shown in Figure 3.
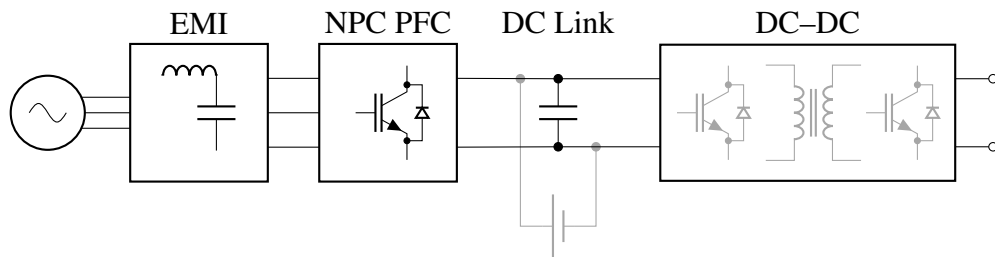
Figure 3: Preliminary block diagram for the charging system in question. DC link is simplified and drawn as a single capacitor even though with NPC AFE it will be atleast partially be divided into two series capacitors. The DC–DC converter implementation is still under research so it's internals are greyed out as well as the battery in parallel with the DC link.

To accommodate the higher charging voltages also increasing grid supply voltage from the standard $690\,V_{L-L}$ to $800\,V_{L-L}$ is considered to keep the grid size phase currents smaller. This requires an unconventional grid transformer with 800 V secondary which have previously been used mainly for some photovoiltaic and battery storage systems but it should not be a problem since larger charging fields would likely need their own transformers regard-

less. When increasing the supply and output voltages also the systems internal voltage levels increase. This needs to be taken into an account when selecting topologies and components for each part of the system since all of them must be able to tolerate the higher power rating and therefore overall more robust solutions are needed.

In the block diagram there is drawn a possibility for a battery in parallel with the DC link. The battery pack could be used to support the power grid as described in subsection 2.1 even with no vehicle connected. An other possible use case would be to charge the battery when the electricity is cheap and use the stored energy to charge up vehicle batteries later. Charging system's nominal parameters are shown in Table 1.

Table 1: Nominal parameters for charging system in question. Final charging current and nominal power are not yet decided so they are given as a range. In this thesis the target current for the phase-leg is 400 A.

Parameter	Value
U_{IN}	800 [V]
P_{OUT}	400 ... 1000 [kW]
I_{C}	400 ... 1000 [A]
V_{CE}	800 [V]

In MCS whitepaper a charging voltage range of 500–1250 VDC is proposed to allow charging of multiple vehicle types with different sizes of battery packs. It's recommended that for compatibility between EVs and charging infrastructure all MCS EVSEs should support the full voltage range. The nominal DC link voltage of the system is selected to be 1500 V to still keep it in low voltage range and then the charging voltage is adjusted with the DC–DC stage. The DC–DC converter is still under research and the topology is yet to be decided. To accommodate the recommended charging voltage range which is quite wide a possibility for modular DC–DC converter is considered. With multiple converter cells that can be connected either in series or parallel as needed the converter could operate at higher efficiency through out the output voltage range.

2.3.3 Active front end

Traditionally the conversion from AC to DC or so called rectification is done with a diode bridge rectifier accompanied with some passive filter components. The topology is simple and robust and has high power density as it does not need any sensors or control but it affects the supply grid power quality with a current Total Harmonic Distortion (THD) of around 30% when the requirement generally is < 5% which distorts also the grid voltage waveform (J. Kolar & Zach, 1997; J. W. Kolar & Friedli, 2013). The rectified voltage amplitude is also directly affected by the grid voltage and cannot be adjusted which might cause problems in

some systems.

The performance of diode bridge rectifier can be enhanced by adding an active PFC stage or replacing the full diode bridge with a hybrid topology rectifier with some PFC functionality where some of the diodes are replaced with switches which can improve the THD to meet the requirements. The active PFC also offers other features like sinusoidal phase currents, controllable power factor, and DC link voltage control. (J. W. Kolar & Friedli, 2013).

In many industrial applications like motor drives with frequency converters and energy storage systems a bidirectional power flow between the system and power grid is needed. In these applications AFEs have been widely adopted since they offer the same desired characteristics as active PFC and also enables the bi-directional power flow eliminating the need for a separate grid inverter (Mehreganfar et al., 2019; Quevedo et al., 2012; J. W. Kolar & Friedli, 2013). AFE can also help to improve the system efficiency especially as the system nominal power increases since it has fewer semiconductors in the current path compared to a diode bridge rectifier with a separate PFC stage (Z. Zhang & Griepentrog, 2023).

3 Active front end design considerations

Numerous AFE topologies have been researched and proposed for both single and three-phase systems (B. Singh et al., 2003; B. Singh et al., 2004). As with inverters first emerged topologies were two-level but as the popularity of AFEs has increased also multilevel alternatives are developed (Ide et al., 2005; Franquelo et al., 2008; Caseiro & Mendes, 2015; Schechter & Kuperman, 2017). Multilevel AFEs offer several benefits in comparison to the two-level counterparts like lower voltage THD, lower switch stress and higher voltage classes (Teichmann et al., 2005; Soeiro & J. W. Kolar, 2013).

These advantages offered by multilevel converter topologies come of course with the cost of a more complex phase-leg structure and complicated control system (Ide et al., 2005; Schechter & Kuperman, 2017; Scoltock et al., 2015). In many cases the more complex multilevel topologies are particularly suitable for medium voltage and high power systems since there the gained benefits of lower voltage steps and therefore less harmonic content and reduced switching stresses justify the extra implementation cost (Popova et al., 2012).

3.1 NPC topology

The diode clamped three-level NPC inverter topology initially proposed in the late 1970s (Baker, 1979) was most likely the first multilevel converter topology that was commercialized word wide (Leon et al., 2017). It is nowadays widely used in industry (pumps, fans, conveyors, etc.), marine and traction applications (Leon et al., 2017; Buekers et al., 2014; Schechter & Kuperman, 2017). It is also being adopted as an AFE topology for applications like EV charging stations, electrical drives and renewable energy conversion systems where bi-directional power flow is needed due to it's relatively simple construction and a good balance between performance and cost (Lin et al., 2022).

The main distinction of the topology is the two series DC link capacitors and that the phase output is clamped to DC link neutral point through diodes or in case of an Active Neutral Point Clamped (ANPC) additional semiconductor switches. Therefore with a three-level NPC topology there is three output stages DC_+, DC_- and N. Basic three-level NPC phase-leg structure is shown in Figure 4.
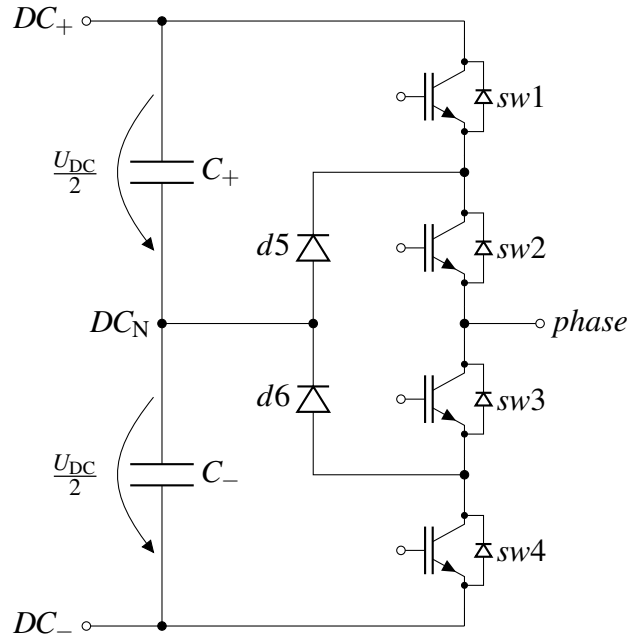
Figure 4: Three-level NPC phase-leg. On the left are the two series DC link capacitors then the two clamping diodes and four switches. Phase connection is on the right side at *sw2* and *sw3* midpoint.

NPC topology's biggest shortcomings are asymmetrical loading of switches and need for DC link voltage balancing to keep lower and upper capacitor voltages equal (Leon et al., 2017). The DC link voltage unbalance, which leads to neutral point creep, can be corrected with a suitable modulation method and a DC link voltage control loop (Lin et al., 2022; Leon et al., 2017). The unbalance problem gets worse and balancing harder when voltage levels and therefore series capacitors are added (Leon et al., 2017), which makes the three-level version the sweet spot for many applications.

Phase voltage and corresponding switch states are shown in Table 2. This loading unbalance needs to be taken into an account in thermal calculations and when dimensioning the cooling solutions since the switches with more strain also produce more heat. The loss distribution between the switches can be better balanced by using ANPC topology when necessary (Liu et al., 2015; Bruckner et al., 2005).

Table 2: NPC Line to Neutral (L–N) voltages and corresponding switch states. Outer switches (*sw*1 and *sw*4) are only modulated when output voltage is either DC_+ or DC_- respectively but inner switches (*sw*2 and *sw*3) are modulated also with zero output voltage.

$U_{\text{L}-\text{N}}$	*sw*1	*sw*2	*sw*3	*sw*4
$+U_{\text{DC}}/2$	1	1	0	0
0	0	1	1	0
$-U_{\text{DC}}/2$	0	0	1	1

In the target application of this thesis the NPC converter is used as a three-phase grid interface. The NPC topology is appealing option for a grid interface with 1500 V nominal DC link voltage since it allows the use of semiconductors with 1200 V nominal voltage rating. For three-phase system three NPC phase-legs are connected together with mutual DC link and each phase leg's midpoint is connected to a phase from the grid through an EMI filter. This three-phase structure is illustrated in Figure 5.
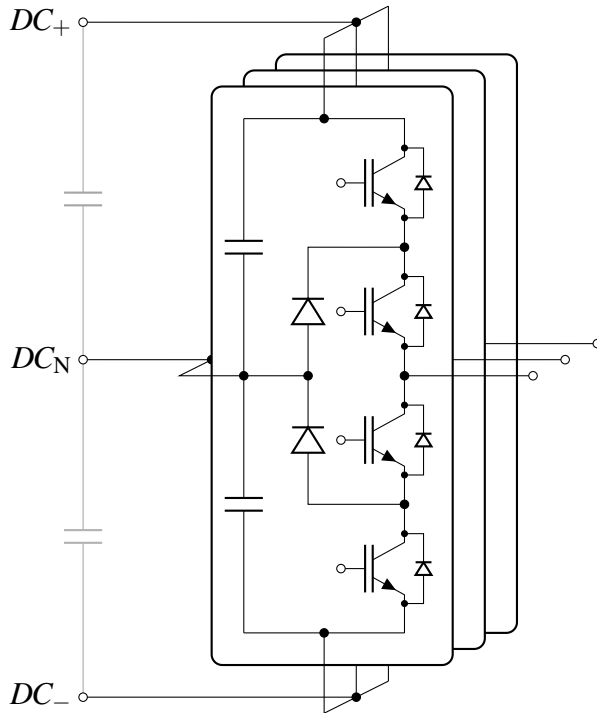

Figure 5: Three-phase three-level NPC AFE rectifier topology with three NPC phase-legs, one for each AC phase connected to a shared DC link. Phase connections on the right and DC link on the left.

In the final converter the DC link will consist of multiple capacitors to achieve small enough stray inductances for each phase-leg and large enough overall capacitance. In the picture

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above the DC link's bulk capacitance is illustrated with the light gray capacitors drawn further away. If needed in the future, multiple NPC phase-legs can also be connected in parallel for each phase to increase the overall current and further power rating above single power module's capabilities.

3.2   Switch commutation

In hard-switched inverters and converters commutation loop inductances can cause numerous problems during operation including over-voltage spikes, ringing, and possible DC link resonance. If these are not taken into account in design phase they might lead to improper operation and even to system failures. (Popova et al., 2012; Beukes et al., 1997)

Interrupting current flow in inductive path with semiconductor switch produces a voltage spike over the switching device. Turn-off peak voltage U_{peak} can be estimated by

$$u_{peak} = L_\sigma \cdot \frac{\mathrm{d}i}{\mathrm{d}t}, \tag{1}$$

where L_σ is commutation loop inductance [H] and $\mathrm{d}i/\mathrm{d}t$ is commutation current slew rate during turn-off [A/s] (Popova et al., 2012). It is crucial to take these spikes into account when designing power electronic converters and to ensure that the peak voltages do not exceed break down voltages of used semiconductors. This is also called voltage derating, switching component's nominal voltage rating cannot be matched to DC link voltage since they also need to withstand the voltage spikes that occur during the switching (Beukes et al., 1997).

Equation (1) shows two ways to limit the overvoltage peak amplitude which are to reduce current slew rate or the commutation loop inductances. Reducing the current slew rate is possible by slowing the switch turn-off but this is rarely a desirable solution since it increases the switching losses especially at high switching frequencies (Ioinovici, 2012). That leaves to the designer the optimization of commutation loop inductances. This is however in many cases easier said than done especially with multilevel converters which have complex phase-leg structures and therefore larger loop inductances in comparison with two-level topologies (Dechant et al., 2020). The commutation loop optimization is discussed in more detail in section 4.

Another option to mitigate the overvoltage spike problem would be to use snubbers to limit the voltage overshoot amplitude (Yatsugi et al., 2018; Gui et al., 2021). Passive snubbers however always introduce some additional energy losses and active snubber circuits make

the system more complex and less reliable (Gui et al., 2021). Utilizing new faster switching devices with faster voltage slew rates also imposes more strict requirements for the loop inductances to take full advantage from them.

3.2.1 NPC commutation paths

NPC topology's commutation paths are usually called short and long commutation paths based on their loop lengths. When considering both upper (DC_+) and lower (DC_-) half of the NPC phase-leg there are in total four commutation loops, which are illustrated in Figure 6. These are not the actual current paths between the phase connection and DC link but their inductances can be used for simulating the overvoltage spikes during commutation (Popova et al., 2012).
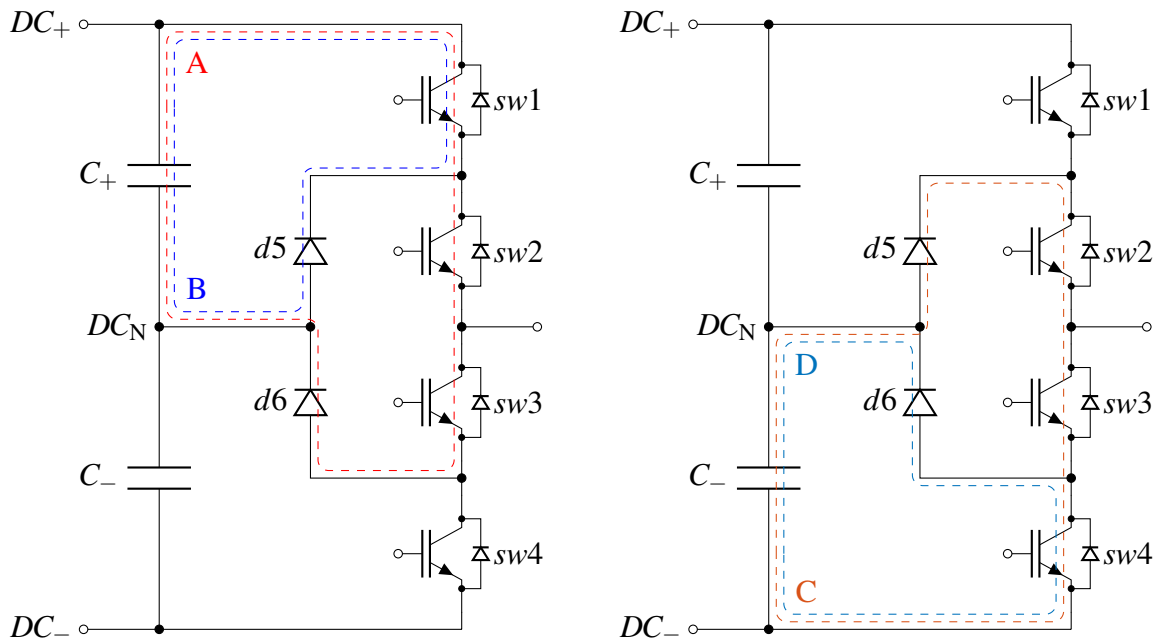
Figure 6: Three-level NPC phase-leg commutation loops DC_+ long (A), DC_+ short (B), DC_- long (C) and DC_- short (D).

In ideal conditions with symmetrical load both upper and lower halves of a phase-leg would commutate symmetrically over one fundamental period. In reality this is unfortunately not the case since the commutation loops of a phase-leg yet a three-phase converter are not possible to design and manufacture to completely identical. Therefore each commutation loop has to be addressed individually in layout design to ensure safe operation of the system.

Converter's commutation loop inductances are a combination of power modules' and DC link capacitors' internal inductances and busbar structure's loop inductances. In terms of power module and capacitor stray inductances there is a little that the converter designer can

do besides selecting modules with relatively small values. Busbar loop inductances however can be affected with component placement as well as busbar layout and stack-up optimization which are discussed in section 4.

Tthe NPC topology's long and short commutation loops have a significant inductance difference between them. Total inductances of the long commutation loops include two more semiconductor switches with their inductances and also more busbars to connect all of them together. The long and short loop inductances can be estimated with equations

$$L_{\text{Long}} = L_{\sigma_{\text{BBLong}}} + L_{\text{C}} + 3 \cdot L_{\text{SW}} + L_{\text{D}} \tag{2}$$

$$L_{\text{Short}} = L_{\sigma_{\text{BBShort}}} + L_{\text{C}} + L_{\text{SW}} + L_{\text{D}} \tag{3}$$

respectively, where $L_{\sigma_{\text{BB}}}$ is the busbar loop inductance of the loop in question [H], L_{C} is parasitic inductance of DC link capacitor [H], L_{SW} is parasitic inductance of used semiconductor switch [H] and L_{D} is the parasitic inductance of used diode [H].

In case of an NPC AFE the importance of the long loop inductances is highlighted since the main current direction is from grid to the DC link and most of the current flow and commutation occurs through the long loops. Therefore in layout optimization of NPC AFE phase-leg the goal is often to attempt to minimize the long loop inductances. In many cases this leads to slightly increased short loop inductances but since they are a lot smaller to begin with it's not really an issue. This way the commutation loop inductances are also a little better balanced between the long and short loops leading to more even voltage overshoot amplitudes.

3.3   Power module topologies for NPC phase-leg

NPC phase-leg can be constructed from standard semiconductor power modules in three ways. One option is to use single device modules, where each of the phase-leg's six semiconductors has its own module as for example in (Popova et al., 2012; Popova et al., 2014). This however, is not the most space effective solution and additional power modules add their own parasitic inductances further increasing the total commutation loop inductances.

Other options are to use two phase-leg switch modules, which have two switching devices in series, in combination with a a phase-leg diode module as clamping diodes. Or to use one phase-leg switch module as two middle switches and boost and buck chopper modules, which have a switch and a diode each, as outer switches and clamping diodes. These two structures are illustrated in Figure 7. Combinations of phase-leg modules and sigle device

modules are also possible but are not discussed here.
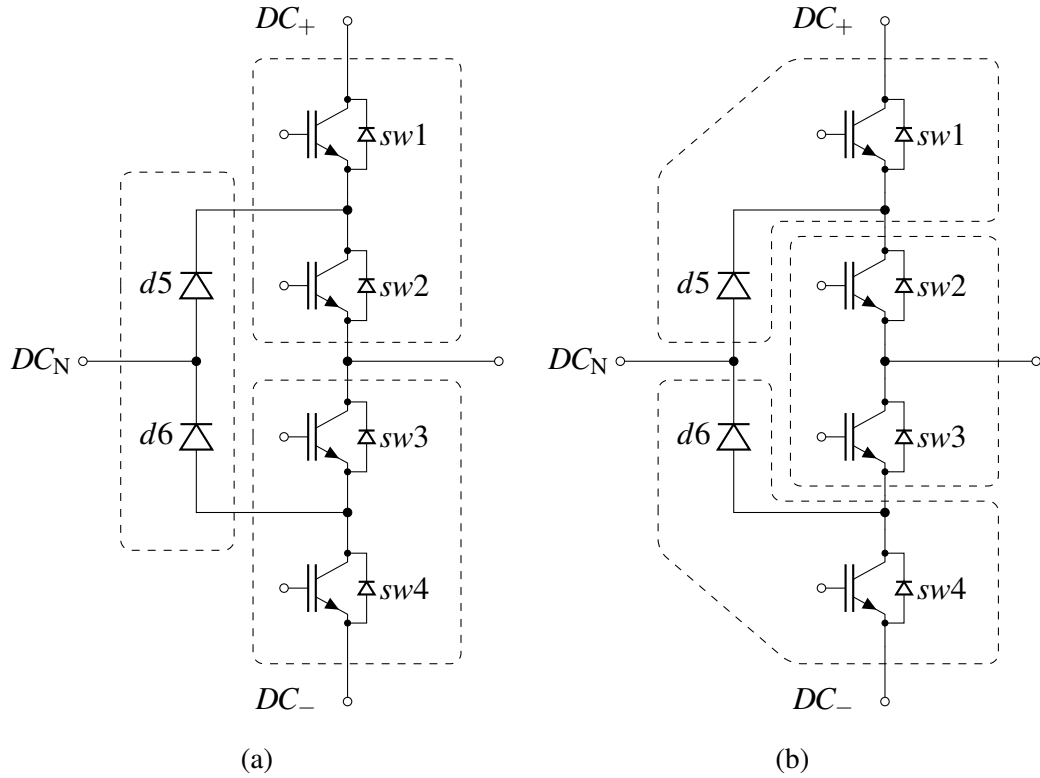
Figure 7: NPC phase-leg can be constructed from power modules in multiple ways. One option (a) is to use two phase-leg switch and one phase-leg diode modules. A second option is to use a phase-leg switch module in combination with boost and buck choppers (b).

The optimal phase-leg structure for a particular application depends on numerous factors starting with available power modules for targeted voltage, current and power levels with selected semiconductor technology. Selected converter topology adds it's own requirements in form of commutation loop optimization. This differs between topologies and with the NPC converter the phase-leg optimization is more complicated compared to two-level topologies due to a more complex phase-leg structure.

Typical semiconductor power modules in phase-leg configuration are designed mainly for H-bridge topology which has dictated module's terminal layout. This makes them non-optimal for the NPC-topology with fundamentally different structure since constructing the phase-leg requires more complex busbars easily leading to higher loop inductances. Especially the long commutation loops that travel through multiple power modules can be challenging.

Some component manufacturers have also designed power modules which contain the whole NPC phase-leg in one package like Semikron Danfoss' SKiM® 4 and Vincotech's I-Type (Semikron, 2023; Vincotech, 2023). These have the advantage of smaller commutation loop inductances since the module is specifically optimized for the NPC topology but have the disadvantage of limited voltage ratings. These are however not package compatible between manufacturers so they were left out from the module comparison here as one design goal was to find a manufacturer independent solution.

3.3.1 Switch technologies

Silicon (Si)-Insulated Gate Bipolar Transistors (IGBTs), later just IGBTs, have been the most used switch technology in power electronic converters for high power applications for the past decades. They are well studied and understood which has made the currently available devices reliable and cheap. Biggest shortcoming of the IGBT technology is the high switching losses which limit the usable switching frequency range (Yin et al., 2022).

The increase in renewable energy production and number of EVs has increased the demand for high power and high power density power converters with high efficiency (Prado et al., 2022). To reach higher switching frequencies so called wide bandgap technologies which include Silicon Carbide (SiC) and Gallium Nitride (GaN) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) have been developed. These technologies also have better voltage blocking abilities and can tolerate higher operating temperatures compared to IGBTs (Prado et al., 2022).

A converter with SiC MOSFETs can operate at a significantly higher switching frequencies compared to one with IGBTs due to their significantly lower switching energy (L. Zhang et al., 2019). SiC devices can reach a switching frequency of 100 kHz with hard switching where IGBTs based converters usually use at maximum 20 kHz switching frequencies (L. Zhang et al., 2019). This means a notable reduction in size of required filter components and possible transformers. High $\mathrm{d}i/\mathrm{d}t$ values of SiC devices which can be 5–10 times larger than IGBTs and the high switching frequencies however also imposes more strict requirements for the parasitic stray inductances of the busbars in order to limit the voltage overshoots (Wang et al., 2021).

As of now the cost of SiC MOSFET power devices is considerably higher than a IGBT module with similar power rating. Available higher switching frequency however makes it possible to use smaller and therefore less expensive filter components and smaller losses reduce the need for cooling solution. These factors lowers the total system cost of a converter and when also factoring in the achievable higher efficiency and life cycle cost use of SiC

devices might be feasible from also the financial point of view but that's a subject for an other thesis entirely.

At the time of writing GaN MOSFETs are best suited for applications with high switching frequency and relatively low power levels. In a comparative analysis presented in (Prado et al., 2022) the GaN switches were recommended for power levels less than 8 kW and at that power range it was the only one recommended with a switching frequency higher than 200 kHz. For the time being the GaN technology is still unsuitable for systems with power rating in hundreds of kilowatts even though the idea of connecting several GaN devices in parallel is researched for example in (Lu & Chen, 2017).

3.3.2 Available power modules

To establish an understanding of what power modules are currently available, a power module survey was conducted. As described in subsection 3.3 NPC phase-leg can be constructed in a couple of ways from phase-leg and chopper modules. Based on that surveyed module types were restricted to phase-leg switch, phase-leg diode and boost and buck chopper modules. Acknowledging the initial system parameters presented in Table 1 the survey was also limited to modules with voltage rating $U_{CE} = 1200$ V and current rating $I_C \geq 400$ A.

The survey was carried out by consulting product catalogs from several semiconductor manufacturers including Infineon, Microchip, Wolfspeed, Semikron Danfoss, Fuji Electric and Mitsubishi Electric. Biggest challenge was to find compatible module types across manufacturers which was one of the key goals for the design task. Many manufacturers have a lot of proprietary module designs which would limit the busbar design to only work with that specific manufacturers power modules which is undesirable for supply chain reliability especially considering the recent chip shortage.

Through systematical research a couple of suitable options were found for phase-leg switch as well as buck and boost chopper modules. Due to the required current $I_C \geq 400$ A most of the found candidates are based on IGBT technology but also some SiC MOSFETs options were found. Suitable phase-leg diode modules were not found at the time of writing with either switch technology. This is likely due to lack of demand of high-speed diode phase-legs since the most common use for those is as an input grid rectifier where frequency is much lower than the switching frequency of a converter. One option around this would be to special order modules with two diodes to fit the need but this would oppose the design goal to prefer modules available off the shelf and from multiple manufacturers.

Summary of found power modules is shown in Table 3. Only the module types with met the requirements for $U_{CE} = 1200$ V and $I_C \geq 400$ A are listed. The modules are divided

into three groups named options 1, 2 and 3 and modules in each group have identical physical dimensions (acknowledging tolerances) across the manufacturers. In the table is also shown the manufacturer specific name for the module type, used switch technology and each module type's current rating for both phase-leg and chopper variant if they are available.

Table 3: Overview of the power module survey results, modules inside groups 1, 2 and 3 are physically compatible with each other. All listed modules have nominal voltage rating of 1200 V and current rating is given for both phase-leg and chopper configurations if they are available.

	Manufacturer	Package name	Type	Current [A]	
				Phase-leg	Chopper
Option 1	Infineon	62 mm	IGBT	200 . . . 800	200 . . . 450
			SiC	250 . . . 500	
	Microchip	D3	SiC	281 . . . 584	475 . . . 700
	Mitsubishi electric	T series	IGBT	600	
	SemikronDanfoss	SEMITRANS 3	IGBT	400 . . . 600	400 . . . 600
			SiC	378 . . . 485	
	Wolfspeed	62 mm	SiC	175 . . . 530	
Option 2	Fuji electric	M254	IGBT	300 . . . 600	
		M282		225 . . . 600	
		M285, M286		600 . . . 1000	
	Infineon	EconoDUAL™ 3	IGBT	150 . . . 900	
	Mitsubishi electric	T1 series, S1 series	IGBT	150 . . . 800	
	ROHM	G	SiC	358 . . . 576	
	Semikron Danfoss	SEMiX 3p	IGBT	600	
	Vincotech	VINco E3s	IGBT	200 . . . 690	
Option 3	Fuji electric	M271	IGBT	600 . . . 1200	900
	Infineon	PrimePACK™ 2	IGBT	450 . . . 900	600 . . . 900

Since phase-leg diode modules were not found the phase-leg structure Figure 7b is selected for the design. Even if it's not technically required all the power modules are selected to have the same package type. This simplifies the busbar design since all the connections are same size and at the same height across the modules.

Looking at the modules in Table 3 module groups 1 and 3 have both phase-leg switch and chopper modules. Option 3 is only available from two manufacturers and it is intended for significantly larger current and power ratings than the other two and is therefore also considerably larger in size. At this time the option 1 is selected for the design since it

is readily available and it meets the project's requirements. Selected module housing is referred to with several different names across manufacturers but 62 mm module seems the most established and it will also be used in this thesis. The name also has a logical reason behind it since the modules short edge is 62 mm long. This package type is illustrated in Figure 8.
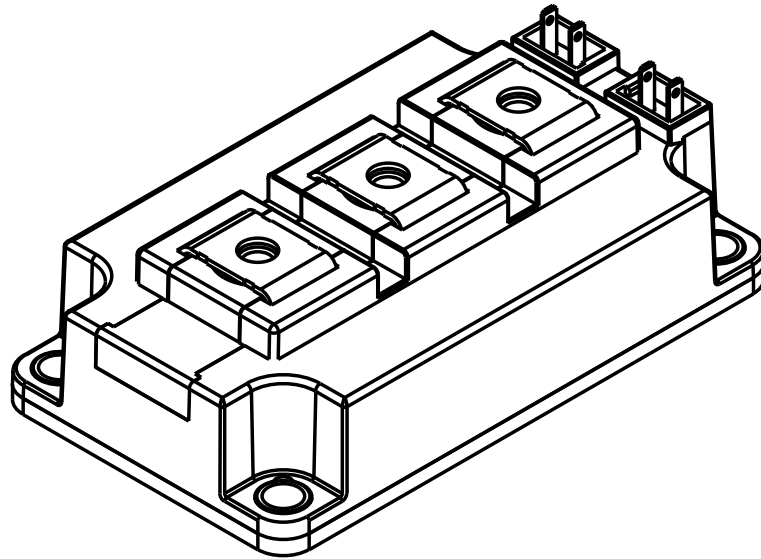
Figure 8: Drawing of a 62 mm power module with three power terminals. Power terminals are at the top of the package and the two smaller connector on the short edge are for gate signals. Drawing is created from .stp file provided by Infineon (Infineon, 2023)

For the design validation a set of Infineon power modules is selected. The selected phase-leg module is FF400R12KE3 and boost and buck chopper modules are FD400R12KE3 and DF400R12KE3 respectively. These are all IGBT3 type modules and were selected to match the phase-leg's nominal current rating of 400 A. Parameters from these modules are used later in busbar design validation for creating a IGBT simulation model in Simplorer for DPT simulations.

4 Layout design

Busbars are used to link power electronic converter's components such as semiconductor switch modules and DC link capacitors together. The significance of the busbar layout for power electronics converter performance has been widely acknowledged and analyzed in multiple publications (Popova et al., 2012; Mattsson et al., 2022; Skibinski & Divan, 1993; Schanen et al., 1996; Zare & Ledwich, 2002; Popova et al., 2014 etc.). Commutation loop stray inductances have been identified as a common cause for voltage overshoots during switching and even equipment failure if not properly taken into an account during the busbar design process.

4.1 Laminated busbar structure

As discussed in subsection 3.2 the NPC topology has multiple commutation loops with different lengths which makes the layout optimization for low inductance commutation paths harder than in traditional two-level converters. It is important to take into an account all of the loops to ensure safe and proper operation in all switching states. In case of NPC topology especially the long commutation loops need careful consideration to keep their total inductances as small as possible.

Laminated busbar structure consisting of two or more parallel conducting plates separated with insulation layers, is a proven good design for minimizing the stray inductances from DC link and busbars connecting the switching components together and to the DC link (Skibinski & Divan, 1993; Schanen et al., 1996; Beukes et al., 1997; Zare & Ledwich, 2002; Popova et al., 2014; Guichon et al., 2006). This structure is illustrated in Figure 9.
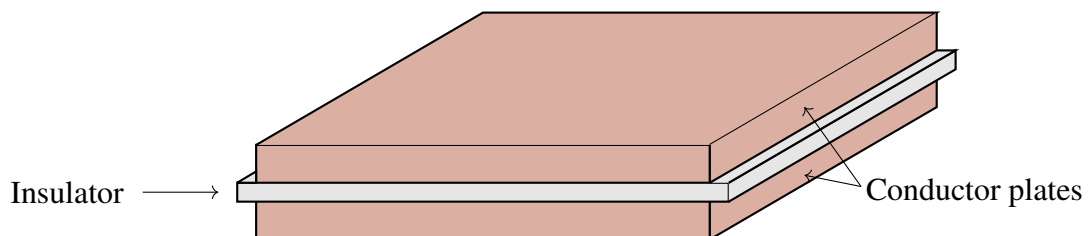

Figure 9: Basic concept of a laminated busbar structure with two conductor plates separated by an insulation layer. Dimensions are not to scale.

Different design factors and mathematical analysis of laminated busbars is studied in depth

in several publications (Gui et al., 2021; Beukes et al., 1997; Guichon et al., 2006; Zare & Ledwich, 2002). Based on the results general rules to reduce the stray inductances are to decrease distance between conducting plate mid-planes and increase the overlap between the busbar layers. Other key factors are to minimize the size of forming current loops with component placement and by placing busbars utilized in same current path on top of each other. For busbar ampacity the cross sectional area of the layers is also relevant but increasing the layer thickness drifts the layer midplanes further away which in return increases the loop inductances.

Following these guidelines should lead to a good initial design but since in electromagnetism everything affects everything and nothing is as easy as it might seem, this is not the whole truth especially in more complex cases. Each design should be verified using more refined methods such as Finite Element Method (FEM) or Partial Element Equivalent Circuit (PEEC) analysis early in the design process to avoid costly revisions later on.

The busbar stack-up can be put together in multiple ways, here a couple of the most typical ones are shown. One option for lamination scheme is to place DC_+ and DC_- one on each side of the neutral busbar, which maximizes the area between the DC and neutral busbars. Other options proposed in (Zare & Ledwich, 2002; Popova et al., 2012) are reduced layer and staircase lamination structures where DC_+ and DC_- share a plane on one side of the neutral busbar. Difference between these two is that in the staircase structure there is additional busbars on top of the DC_+ and DC_-. These typical lamination schemes are illustrated in Figure 10.

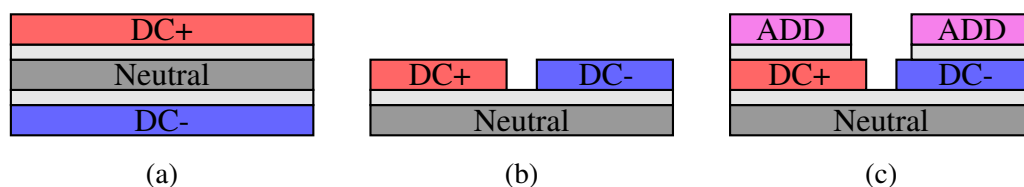

Figure 10: Parallel (a), reduced layer (b) and staircase (c) lamination structures illustrated. Light grey layers represents the insulation between the busbars.

Where the parallel and reduced layer lamination schemes are in many cases suitable for two level converters (Zare & Ledwich, 2002) in multilevel topologies like three level NPC more layers are often needed to fabricate the phase-leg.

To be able to minimize the inductance of the commutation loops it is important to first recognize the commutation paths of the selected topology. NPC phase-leg's commutation was discussed in subsection 3.2 and the commutation paths were identified. It was found that the commutation happens between either DC_+ or DC_- and the neutral busbar so both DC_+ and DC_- should be placed adjacent to the neutral. Since current won't flow directly between DC link positive and negative those busbars don't need to be on top of each other.

4.2 Experimental layouts

Constructing a NPC phase-leg from standard off the shelf power modules was discussed in subsection 3.3. Considering module availability a combination of a phase-leg switch module with boost and buck chopper modules in so called 62 mm package was found to be a feasible solution. The first step of a layout design is to optimize the power module layout in a way that the connections between module terminals are as short as possible and if possible with no overlapping connections. The power modules dictate a lot of physical layout limitations in addition to just the power terminals since also things like the control terminal clearances and possibly gate driver circuit placement need to be taken into an account.

After a suitable module arrangement is found the design is continued towards the whole laminated busbar structure. The module layout design is done in two dimensional (2D) since the modules are placed on a same plane meaning that they can all be mounted to one heatsink and all of the power terminals are at the same height. The busbar structure however consists of multiple parallel busbar layers on top of each other. This would be cumbersome to design with 2D drawings so a Three Dimensional (3D) Computer Aided Design (CAD) program is used. This also saves an extra step since the busbar 3D models will be needed for the simulation phase.

The design process is described here as relatively linear for clarity reasons with module layouts first and busbar design after that. In reality there were a lot of back and forth iteration rounds and minor changes along the process to optimize the designs which is left out.

4.2.1 Simplifications

With every design task there is the need to make some initial assumptions and simplifications to make the problem manageable. Many times these are made with inadequate information and the designer needs to redefine them later on in order to get to the final solution but nonetheless they are needed to get a hold of the problem.

As usually in high power application grid connections this NPC AFE will be three-phase. However in this thesis the scope is in optimizing layout of one phase-leg. This is to keep the

amount of work reasonable for the scope of a Master's thesis. For the same reason a lot of other components affecting the final converter layout like most of the DC link capacitors as well as voltage and current measurement and gate driver circuits are left out.

Cooling solution for this converter is also left to be dimensioned and designed in the future since it will require more knowledge about the whole three-phase converter and the whole EVSE that the AFE would be a part of. The module layouts are done with an assumption that all the three power modules of a phase-leg will be mounted to one heatsink below the modules. Manufacturability of the busbar designs is considered where possible. In reality this means mostly ruling out the layout options that are obviously impractical to manufacture and assemble. With no previous experience from busbar designing or assembling there will certainly be still a lot left to optimize before any of the proposed layout designs is ready for production.

4.2.2   Power module layout

The initial goal for module layout optimization was to find a layout where the NPC phase-leg could be fabricated with minimal distance between power module terminals. An other factor to consider is the symmetricality of the module layout to keep the commutation paths from upper and lower halves of the phase-leg symmetric. These does not guarantee the lowest possible stray inductances but is a one factor towards it. Multiple tools were used to help visualize the design problem including 2D drawing programs, printed paper cut-outs and 3D printed models of the 62 mm power module.

NPC phase-leg's long commutation loops travel through three semiconductor switches in comparison to short loop's one as described in section 3.2.1. Therefore they are the most likely to cause voltage overshoot problems since the long loop inductances easily accumulate as all of the power modules and busbars between them add their own inductances. To keep the long loop inductances below the critical value they are focused on first.

After a module arrangement was chosen the commutation paths were drawn between the power modules to assess the forming commutation loops. At this state some adjustments were often made since some quite obvious problems were spotted which were easy to fix now. Other things to consider are the placement of DC link capasitors as well as space required by heatsink, gate driver signals. The placement of the DC link capacitors has quite significant impact on the commutation loop inductances and atleast one DC_+ and one DC_- capacitor should be placed as close as possible to the power modules.

The final DC link of the final converter will consist of numerous capacitors and most likely of both film and electrolytic capacitors to achieve fast response and large enough total ca-

pacitance. At this design stage however only the one DC_+ and DC_- capacitors closest to the phase-leg modules are taken into an account since considering the whole DC link would be cumbersome and partially unnecessary since it's form factor will most likely change anyway later on the converter design.

Gate signals are taken into an account by leaving room for the module's auxiliary terminals where gate signals will be connected. With 62 mm modules the gate driver Printed Circuit Boards (PCBs) might be connected directly to the modules or they can be a little further away in which case the signals are connected through wires (Infineon, 2012). Since the scope of this thesis is at layout and busbar design of a NPC phase-leg, other additional components are left out as they belong more to a layout design of the whole three-phase converter.

First an arrangement A presented in Figure 11 (a) was considered with the DC link on one side of the modules and the phase connection on the other. This would allow placing the three phases compactly side by side so that DC link is on one side and phase connections on the other. This layout was however presumed to have uneven inductances between DC_+ and DC_- commutation loops due to asymmetrical layout. The DC link capacitors are closer to the buck-chopper module which will likely result in lower commutation path inductances in the DC_+ side. Also the connection between buck chopper and phase-leg modules is as long as it can be as the boost module is in between them increasing the inductance of both long loops.

To address the problems from asymmetric phase-leg structure a layout B (Figure 11 (b)) was created and this time the focus was on trying to keep the positive and negative halves symmetric. This was achieved by placing the phase-leg module in between the two chopper modules and distributing the DC link to both sides of the modules. This way the connections between the power modules are more symmetric since the phase-leg that connects to both of the chopper modules is in between them. Also the DC_+ and DC_- capacitors are right next to the corresponding chopper modules to minimize and even out the stray inductances from the connection to the DC link.

The layout B was proven to be more symmetric in simulations compared to the layout A and thus two more layouts were made utilizing the same split DC link idea. In layout C presented in Figure 11 (c) the buck chopper is rotated 180° to reduce long loop inductances by shortening the distance between phase-leg and buck chopper terminals. The drawback in this design is the buck module's control terminal location that is now separated from the two others which may introduce challenges later with gate driver placement.
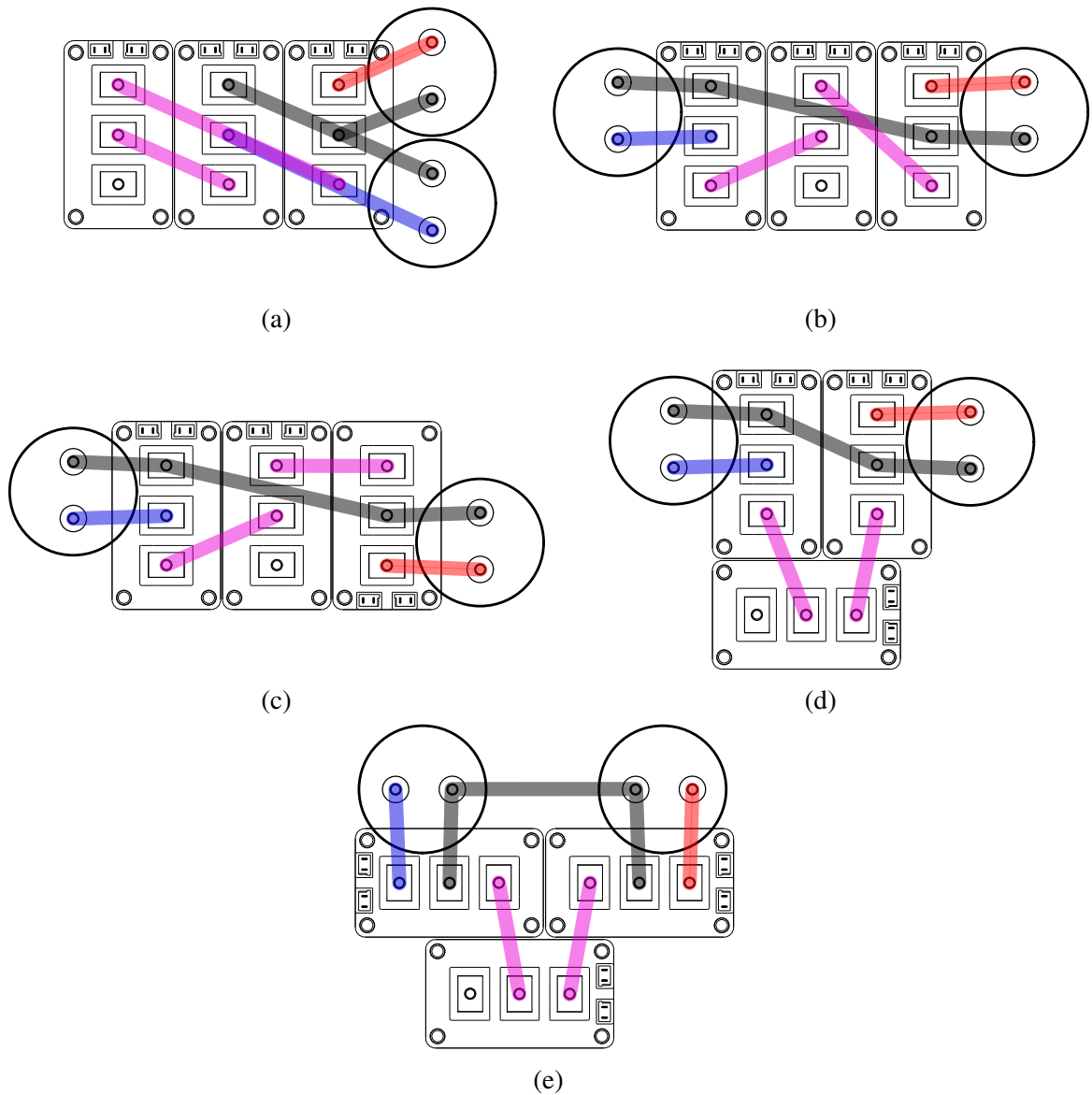
Figure 11: Placement of power modules and closest DC link capacitors in considered module layouts. Colored lines represent required connections between the modules and capacitors. Grey color represents DC_N busbar, red represents DC_+ busbar, blue represents DC_- busbar and pink represents additional busbars. Phase-connection is from the terminal which in these pictures is left unconnected.

In layout D shown in Figure 11 (d) the chopper modules were placed right next to each other and the phase-leg module below them. This way the DC link and phase connection are on different sides of the power module stack which may help the layout design of the three-phase converter. The same principle is applied for the design E but the choppers are sideways between the DC link capacitors and the phase-leg module. This could allow stacking the three-phases of the converter closer together since all of the capacitors can be placed on one side of the power modules.

Each layout has only one DC_+ and DC_- capacitor although in final converter there will almost certainly be several of each and possibly several different types of capacitors with an arrangement to ensure minimal stray inductances between the DC link and each of the power module. This simplification was done to in order to keep the DC link structure and therefore its stray inductances as constant as possible to analyse the affects of module layout and busbar stack-up to the stray inductances. The number of DC link capacitors and their layout is a considerable factor while optimizing converter layout but in this case it was deliberately left out at this stage.

4.2.3 Laminated busbar designs

After the power module layout was determined the design process continued with busbar layout first in 2D and then transitioning to 3D. With the laminated busbar structures the vertical busbar stackup is as if not more critical than the module layout for the performance. Generally the current path and return path busbars should be paced on top of each other to minimize stray inductances but in more complex phase-leg structures like the NPC topology that is not always so obvious.

Initial outlining of the busbar layers was done in 2D drawings and after that the design was taken into 3D CAD program in this case Autodesk Fusion 360. That made the handling of complex 3D structures easier since both the individual layers and the whole stack were easy to examine from any angle. Designing the busbars straight away to 3D-models also saved one additional step since the models are anyway needed for the simulation phase. To help with the busbar design first the phase-legs power modules were added into the 3D assembly. For this the Infineon's .stp file of the 62 mm power module was used (Infineon, 2023) since there was really no point of re-inventing the wheel. Originally the model was all one color and the colors seen in the 3D renders were added later on to the module model. After the power modules were in their places it was easy to take the necessary measurements for the busbars using measurement tool.

Each busbar layer was drawn as its own component and then imported into the main busbar assembly. Joints were then used to join the component together and place the imported components to appropriate places. All the busbar layers have thickness of 2 mm and there is 0.5 mm empty space in between for insulation. Drawn busbar 3D layouts are displayed in Figure 12 and their order corresponds to the 2D layout images presented in Figure 11.
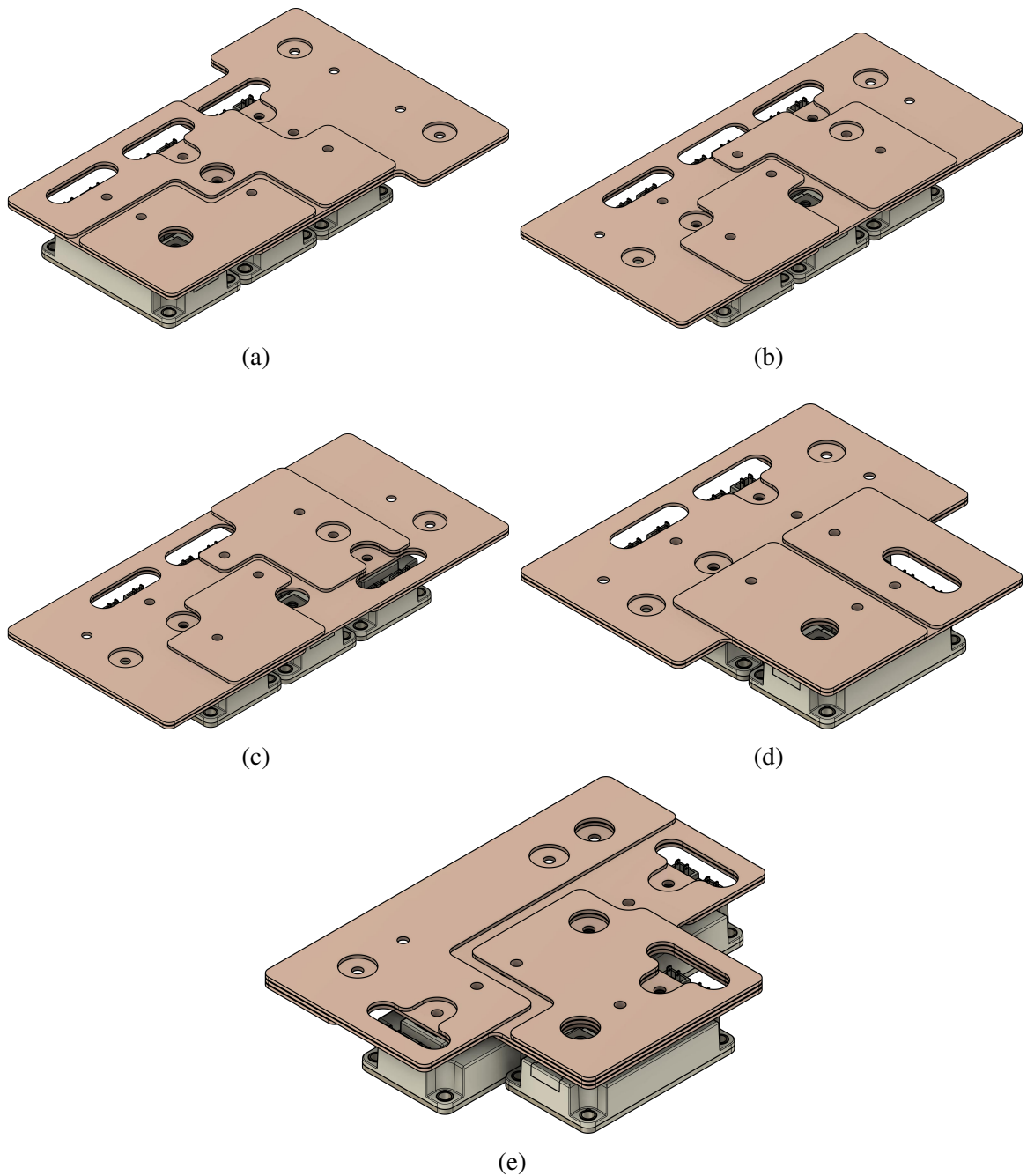
Figure 12: Designed busbar layouts as 2D projections. Power modules are below the laminated busbar structures. Round holes are for the electrical connections to the power modules and capacitors and oval cut-outs for the IGBT gate signal terminals. DC link capacitors are left out for better view as their place would be on top of the busbar stack.

The laminated busbar structures shown in Figure 12 utilize a combination of parallel and staircase lamination structures which were discussed in subsection 4.1. In layouts A, B, C and D the DC_+ and DC_- busbars share a plane next to the DC_N busbar like in the staircase lamination structure. As for layout E, the DC_+ and DC_- are on the different sides of the DC_N busbar. This will affect the options for the whole converter DC link layout design since if the

DC_+ and DC_- busbars are on the same plane there is less freedom for placing the DC_+ and DC_- capacitors which may result in sub-optimal performance due to increased parasitics. There shouldn't however be any major problems adapting the busbar designs to either of these lamination strategies if it's required for the DC link design. The additional busbars are also laminated next to the neutral busbar, either side by side on one side or in case of laout E on opposite sides which is assumed to result in smallest long loop inductances and which was also confirmed with some preliminary simulations.

The starting point for each busbar design was drawing the neutral busbar since it was pretty much the middle component of the laminated structure. It is also the largest busbar layer since it extends over both of the DC link halves and both chopper modules as a way to trying keep the area between the busbar layers as large as possible. It was originally drawn as a large square over the power modules overlapping them on each side and then it was extended for the capacitors and cut outs were made as necessary. In the busbar design the shape of some of the additional busbars at the top of the looks quite odd since they were shaped by eliminating parts that would have been connected only with very narrow pieces of copper which would have caused trouble in manufacturing. Also sharp edges are avoided where possible and all the busbar layer corners are rounded.

As the laminated busbar layers extend across the power modules for maximizing the overlap between them to reach minimum loop inductances some form of connection method is required to be able to connect the module terminals to the busbars. At this time bushings are used between the modules and the appropriate busbar layers which can be seen in the busbar side-view displayed in Figure 13. The bushings add one contact point per connection with some resistance at the seam of the bushing and the busbar but their advantage is a small footprint which is pretty much required since the clearance between the module terminals is quite short especially between the three terminals of one power module. In these busbar models however the bushings are a fixed to the busbar plates and affect of their contact point is therefore omitted.
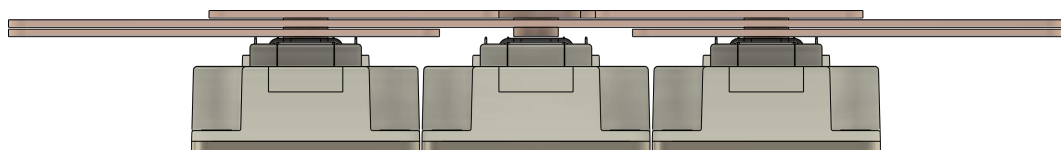

Figure 13: Side-view of the layout B busbar stackup. Three busbar layers are clearly visible as well as the bushings connecting the top layer busbars to the phase-leg module in the middle.

Used bushings have inside diameter of 6 mm matching the diameter of M6 bolts that will be used to fasten the busbars to the power modules and outside diameter of 12 mm. In the layer closest to power modules a bushing height of 0.5 mm is used to leave room for one insulation layer directly on top of the power modules. This was done to preserve as much busbar cross-sectional area as possible since the busbar layers can extend on top of the module terminals they are not connected to.

For the next layers the required bushing height is calculated from the busbar and insulation layer thickness's of 2 mm and 0.5 mm respectively. For these bushings an opening is required for all the layers between the connection layer and the power modules. The openings have a diameter of 20 mm leaving 4 mm of clearance between the bushing and the busbar it perforates. This is most likely not enough of an air gap for an air-cooled converters operating in sub-optimal environments where moisture and contaminants can and will enter the device.

The diameter of these openings was selected to be so small to keep the busbar layer's cross-sectional area as large and unified as possible. In further development the requirements for this clearance and options for reducing the required distance using solutions like insulating collets of coating the inside of the opening with insulating materials needs to be researched further. In similar busbar structures an epoxy coating has been used before for insulating a screw head from adjacent busbar (Gui et al., 2021). The size of these perforated terminals also have an effect to the parasitics of the busbars including inductances which is researched for example in (Mitsui & Wada, 2022) so they should be kept as small as possible.

5 Evaluation of the designs

Numerical analysis tools based on PEEC and FEM methods are widely used in power electronics design for calculating parasitic inductances as a part of converter design and validation (Popova et al., 2014; Clavel et al., 2009; Ardon et al., 2010; Schanan et al., 1994; Tran et al., 2010; Zare & Ledwich, 2002; Lai et al., 2006). They allow the designer to test different solutions relatively fast and help reduce product development time by making it easier to spot potential problems early in the design process and therefore reduce required prototype phases.

5.1 Simulation tools

Simulations are done in Ansys Electronics Desktop 2021 using Ansys Simplorer multiphysics circuit simulator in combination with Ansys Q3D Extractor. The Q3D Extractor is first used to characterize the busbar 3D models based on a combination of FEM analysis and Method of Moments (MoM) and extract the resistance, inductance, capacitance and conductance (RLCG) parameters. Then the Q3D design is imported to Simplorer for further analysis. Also MATLAB is used at the end for calculating inductance values based on simulation results and for data visualization.

5.2 Inductance Simulations

Commutation loop inductance simulation must take into account the highest frequency present in the system. According to (Skibinski & Divan, 1993) the highest critical frequency f_{cr} can be calculated as

$$f_{cr} = \frac{1}{2\pi t_f},$$

(4)

where t_f is the fall time [s] of used switching devices. Fall time of an IGBT device with nominal voltage rating of 1200 V is around 100–200 ns (Infineon, 2013a; Infineon, 2013b; Infineon, 2013c) depending on used module type and junction temperature. Assuming the shortest fall time $t_f = 100$ ns we get the critical frequency $f_{cr} \approx 1.6$ MHz. At this frequency in laminated busbar, both skin and proximity effect have a considerable impact on inductance values (Skibinski & Divan, 1993).

The busbar 3D model is first imported into Ansys Q3D Extractor and the busbars are defined to be made out of copper. In these simulations the empty space in between the busbar layers in the 3D models acts as the insulation. The busbar connections to power module terminals

and capacitors are then defined and given names so that components can be connected to the busbars later on as necessary. The busbar model is then characterized at frequency 1.6 MHz with allowed error of 0.1%.

After the characterization the Q3D Design component is imported into Ansys Simplorer circuit simulator as a state space model using RLCG parameters generated from the frequency analysis. In Simplorer one of the four NPC commutation loops is then constructed by connecting busbar connection points together with ideal conductors where the commutation loop's switches and diode would be. A series LC resonant circuit is then formed from the busbar model commutation loop as the inductor in combination with an ideal capacitor with capacitance $C = 33\,\mu\text{F}$ and AC voltage source with AC magnitude $U = 1\,\text{V}$. This is done for each of the four commutation loops in separate Simplorer designs. Layout B's DC_- long commutation loop simulation setup is shown in Figure 14.
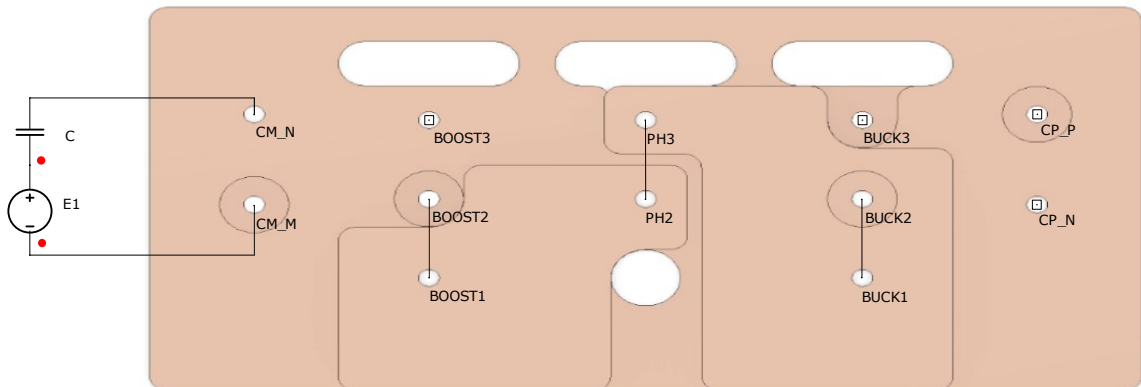

Figure 14: Picture from Simplorer design used to simulate the DC_- long commutation loop inductance showing the imported busbar model as well as used capacitor and AC voltage source. Terminal names and positioning of some elements is edited to make the image more clear.

To solve the commutation loop inductances an AC Analysis setup is used. A linear frequency sweep from 1 Hz to 500 kHz with a step size of 10 Hz is run and a bode plot of the AC voltage source current is produced. From the bode plot the LC circuit resonant peak can be found and the resonant frequency is obtained as *peakgrainfreq*. The commutation loop inductances are then solved using MATLAB according to

$$L_{\text{loop}} = \frac{1}{C(2\pi f_{\text{res}})^2},$$ (5)

40

where C is the capacitor capacitance used in simulation [F] and f_{res} is the resonant frequency of the series LC circuit [Hz].

In addition to the busbar stray inductances the commutation loop inductances consist of stray inductances of the power modules and DC link capacitors as discussed in section 3.2.1. Component manufacturers usually give some stray inductance values for their components which can be used for approximating what the total commutation loop inductance will be.

For the power modules selected for the simulations Infineon's datasheets give a stray inductance value of 20 nH per module (Infineon, 2013a; Infineon, 2013b; Infineon, 2013c). As no more details were provided it is assumed that this is distributed evenly among the two switches or a switch and a diode of the module and therefore each switch and diode on the commutation path is assumed to have a paracitic inductance of 10 nH. As a hindsight this is quite large inductance for a power module and while it might not be a problem with the selected IGBT modules with for example SiC devices the module stray inductance should be taken into an account when selecting the modules. Especially with multilevel topologies where there is multiple switches in a single commutation loop like NPC.

As the DC link capacitors closest to the power modules a capacitor type with low Equivalent Series Inductance (ESL) should be used. At this time a capacitor from TDK Electronics' MKP DC ULSI HF series is chosen with a given ESL of 13–15 nH depending on the exact capacitor model (TDK, 2022). A value of 15 nH is therefore used as it's the least optimal option.

5.2.1 Inductance simulation results

To have something to compare the simulated loop inductances to the maximum allowed commutation loop inductance considering the voltage overshoot was calculated by applying (1) as

$$L_{\text{max}} = \frac{U_{\text{CE,peak}} - \frac{U_{\text{DC}}}{2} - U_{\text{SF}}}{\frac{\mathrm{d}i}{\mathrm{d}t}}, \tag{6}$$

where L_{max} is the maximum allowed commutation loop inductance [H], $U_{\text{CE,peak}}$ is the nominal voltage rating of the power modules [V], U_{DC} is the DC link voltage [V] and U_{SF} is the safety margin for DC link voltage fluctuation [V]. Using values $U_{\text{CE,peak}} = 1200\,\text{V}$, $U_{\text{DC}}/2 = 800\,\text{V}$, $U_{\text{SF}} = 50\,\text{V}$, $\mathrm{d}i = 400\,\text{A}$ and $\mathrm{d}t = 100\,\text{ns}$ we get a maximum commutation path inductance of 87.5 nH. The value $U_{\text{DC}}/2 = 800\,\text{V}$ is used instead of the nominal 750 V as the DC link neutral point voltage fluctuates during operation and voltage over either upper

or lower half of the DC link can occasionally reach 800 V.

In addition to the busbar loop inductances this maximum value includes all the semiconductor and capacitor parasitic inductances on the commutation path. As explained in section 3.2.1 in the short loops there is one switch, one diode and one capacitor and in the long loops there are three switches, a diode and a capacitor. Using the values in previous section we can calculate the maximum values for just the busbars according to (2) and (3) which gives maximum busbar loop inductances of 32.5 nH and 52.5 nH for long and short loops respectively.

The calculated busbar stray inductances for busbar layouts A–D are shown in Figure 15. With all simulated layouts both long and short loop inductances are lower than the maximum values calculated above. In all of the short loops there is plenty of headroom since even the highest simulated short loop inductance is less than 17% of the calculated maximum. With long loop simulation results the corresponding value is less than 66% which is significantly closer to the limit but there's still a decent margin. Especially considering that the limit was calculated with DC link voltage of 1600 V instead of the nominal 1500 V and on top of that a 50 V safety margin.
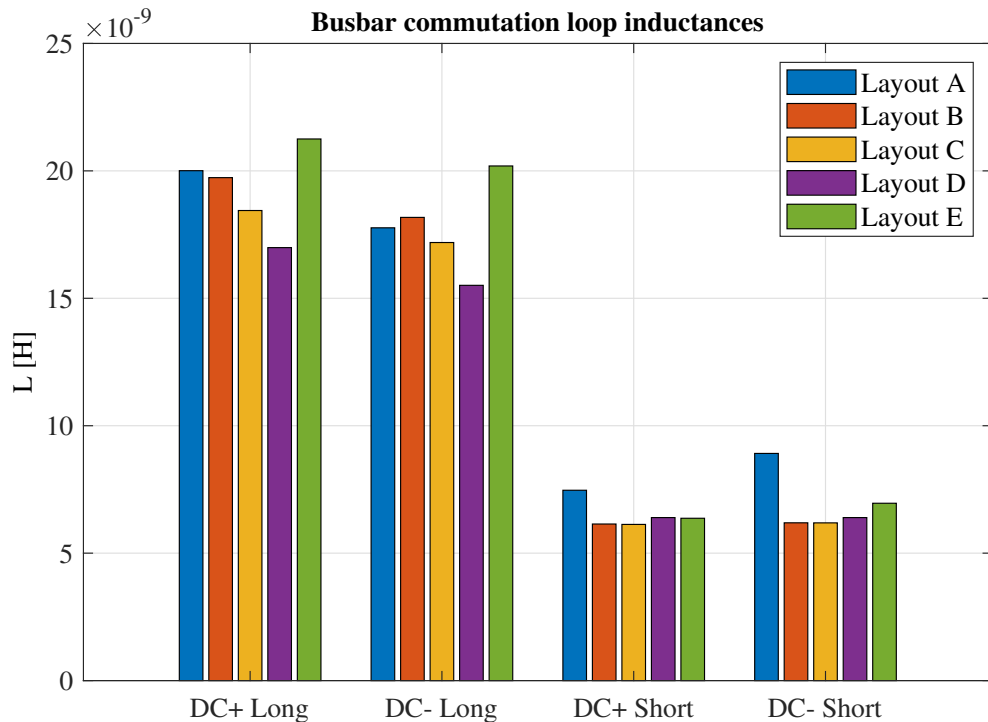

Figure 15: Busbar commutation loop inductances of the different layout designs grouped by the commutation loop so that comparisons between layouts is easier.

As can be seen from the Figure 15 the DC_+ long commutation loops have a little higher inductances compared to the DC_- long loop in the same layout. Some asymmetry is of course to be expected since there are a lot of design factors affecting them. The DC_+ long commutation stray inductances are 5 to 11% higher in comparison to DC_- long loops. This is likely due to the different terminal layout of buck and boost choppers since they have the switch and diode reversed. In DC_- long loop the commutation path travels through both choppers from terminal 1 to terminal 2 which are right next to each other but in DC_+ long loop the path travels from chopper terminals 1 to terminals 3 which are on the opposite ends of the modules. This makes the loops a little asymmetric even if the busbars are designed to be as symmetric as possible between the upper and lower halves of a phase-leg.

With short loops the difference between DC_+ and DC_- is notably smaller and to the other way around as the DC_+ loops have the lower inductances. In layout A the DC_+ short loop inductance is 7% lower compared to DC_- and for all the other layouts the difference is less than one percent. Most likely this amount of a difference won't cause any problems even with the long commutation loops but if needed the inductances could be balanced by adjusting the busbars or the DC link capacitor placement relative to the chopper modules.

The busbar layouts were done in order from A to E and with each new design the attempt was to solve the issues in the previous one. With layouts A to D the DC_+ and DC_- long loop inductances are getting closer together and also decreasing with every design but the layout E is a little different. As described in section 4.2.2 it was designed based on to the layout D and the idea was to move the capacitors on the opposite side from the phase connection. This might be caused by the module layout since DC_+ terminal on the buck chopper is far away from DC_N terminal of the boost chopper as those are connection points of the DC_+ long commutation path to the DC link. Similar situation is also with the DC_- terminal of boost chopper and DC_N terminal of buck chopper. This might add stray inductance at the connection from DC link capacitors to the power moduels therefore increasing the total commutation loop inductances. Still the loop inductance is well below the critical limit and especially with this design the stray inductances probably will decrease with proper DC link layout with several capacitors.

5.3 Double pulse test

DPT is widely used by both semiconductor manufacturers to evaluate dynamic performance of their semiconductors as well as system engineers to evaluate the switching behaviour of a converter. The first pulse is used to reach the current that the test is to be done and then second pulse for the actual switch characterization. In this thesis DPT simulations are used for estimating the over voltage spikes during switching with the proposed busbar layouts.

The DPT simulations are done in Ansys Simplorer similarly to the commutation loop inductance simulations and using the same busbar Q3D design component as in them. A method proposed in (Korhonen et al., 2022) is used where the DPTs can be done for the NPC phase-leg's four commutation loops with only half of the nominal DC link voltage. The DC_+ long and short loop can be tested with just the upper half of the DC link charged to half of the nominal DC link voltage and respectively the DC_- loops with the lower half of the DC link. With this method the unused half of the DC link must be disconnected from the system in order to ensure the correct commutation paths.

The DC link capacitor model is made from ideal capacitor, resistor and inductor connected in series. The parameter values of $C = 160\,\mu\text{F}$, $R = 1.4\,\text{m}\Omega$ and $L = 15\,\text{nH}$ are taken from a B25632E1167K000 capacitor datasheet (TDK, 2022). Initial voltage of the capacitor is set to 800 V as it is used as the voltage source for the DPT. These capacitor models are done for both DC_+ and DC_- side and the one not in use is then deactivated and treated as an open circuit.

Used IGBT semiconductor model is characterized as basic dynamic IGBT using the Ansys Twin Builder's Characterize device tool based on information in the FF400R12KE3 phase-leg power module datasheet (Infineon, 2013c). Since the characterized module and selected choppers DF400R12KE3 and FD400R12KE3 are from the same product family and their datasheets (Infineon, 2013a; Infineon, 2013b) didn't reveal any notable differences between the IGBT freewheeling diodes and the chopper module diode the same model is used as the chopper module diodes with constant '0' gate signal.

In short commutation loop DPTs the load inductor is connected between the phase-leg's phase connection and DC link's DC_N and then for long loop tests the DC link connection is moved to either DC_+ or DC_- depending on which loop is under testing. The used load inductor has an inductance of $20\,\mu\text{H}$ and it was dimensioned so that the nominal current of 400 A is reached with the first pulse.

The DPT simulation setup for layout B is shown in Figure 16. All three of the power modules are constructed out of the previously characterized IGBT model and connected to the busbars. This way all of the four DPT tests can be done by editing just the load inductor connection and DC link capacitor configuration and applying the suitable gate signals for the four switches. The IGBT switches which are not used in any particular DPT are given a '0' gate voltage. At the bottom left corner there are all the needed signals available including the DPT pulses and constant '0' and '1' which are then connected to the appropriate gate drivers.
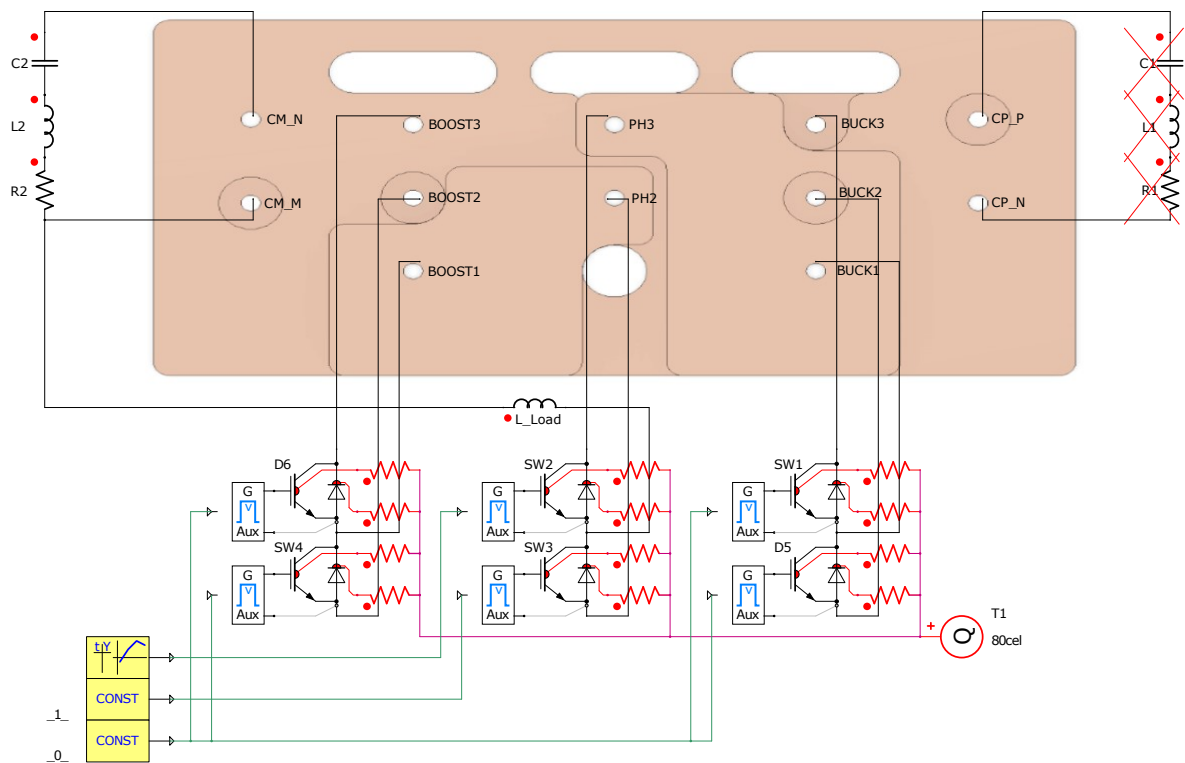
Figure 16: DPT simulation setup in Ansys Simplorer. At the top the Q3D busbar model and the DC link capacitors and at the bottom the IGBT models representing the power modules. Since the picture is from DC_- long loop simulation the DC_+ capacitor is commented out and replaced with an open circuit. Picture is edited by cleaning up and removing some text fields to make it easier to read.

The used gate commands for each DPT simulation are shown in Table 4. With each loop one switch is a Device Under Test (DUT) controlled with the double pulses and other switches have static states during any one of the four DPTs. The total length of the DPT simulations is $20\,\mu s$ with a pulse pattern where the first $10\,\mu s$ pulse starts at $1\,\mu s$ and then there is a $2\,\mu s$ delay before the second $2\,\mu s$ pulse. The simulations are done with transient analysis setup with minimum simulation step size of $1\,ns$ and maximum step size of $10\,ns$.

Table 4: DPT gate commands for each switch and corresponding commutation loops of the NPC phase-leg. *Pulsed* means the DPT's double pulses and for other switches their constant state during the test are given.

DUT	$sw1$	$sw2$	$sw3$	$sw4$	Commutation loop
$sw1$	Pulsed	1	0	0	DC_+ Short
$sw2$	0	Pulsed	1	0	DC_- Long
$sw3$	0	1	Pulsed	0	DC_+ Long
$sw4$	0	0	1	Pulsed	DC_- Short

The thermal side of the IGBT models is connected to a temperature source with constant temperature of 80 °C through thermal resistances. First a resistance value of 0.01 K/W was was tried corresponding to the case to heatsink thermal resistance given in power module datasheets (Infineon, 2013a; Infineon, 2013b; Infineon, 2013c). This however made the IGBT model oscillate when given a control pulse and at the same time simulation got extremely slow. As no obvious causes for this behaviour was found the characterization was done again but that model behaved in the same way. At some point of debugging the issue the thermal resistances were chaged to the Simplorer default value of 1e-12 K/W which fixed the problem. At this time the source of the problem is assumed to be in the thermal side of the IGBT model as the model seems to otherwise function fine. The model is used for the DPT simulations but for thermal simulations later on the root cause of the problem must be solved.

5.3.1 DPT Simulation results

From DPT simulations DUT IGBT collector current and collector–emitter voltage waveforms are acquired using Simplorer's probe tool. They are then exported as .csv files and data is then imported to MATLAB as it offers more flexibility compared to Ansys' plot tools for visualizing the data. The DPT waveforms for each commutation loop of the busbar layout A is shown in Figure 17.
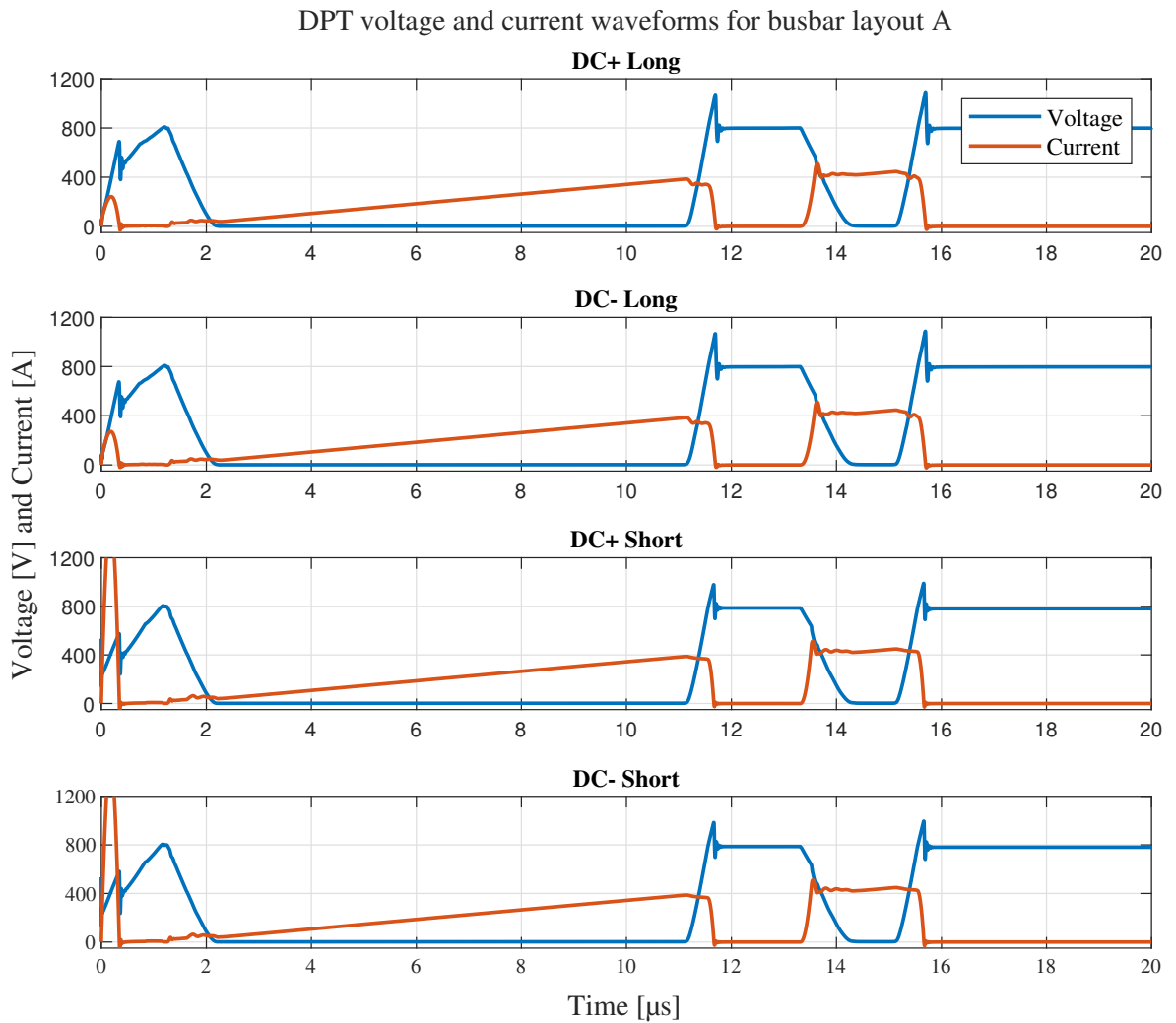
Figure 17: Simulated DPT voltage and current waveforms for busbar layout A. At the start there are some voltage and current transients caused by the initial DC link capacitor voltage which is set at $t = 0$.

As can be seen from the figure above the voltage spike amplitudes in both pulses is below the 1200 V maximum with a margin of roughly 100 V. The voltage and current waveforms from all of the busbar layouts are nearly identical at this voltage/current and time scale and when drawn into a same figure the individual lines were almost perfectly on top of each other. To better illustrate the differences a zoomed views of the DPT's second voltage peak between 15 and 16 μs with each busbar layout is shown in Figure 18.
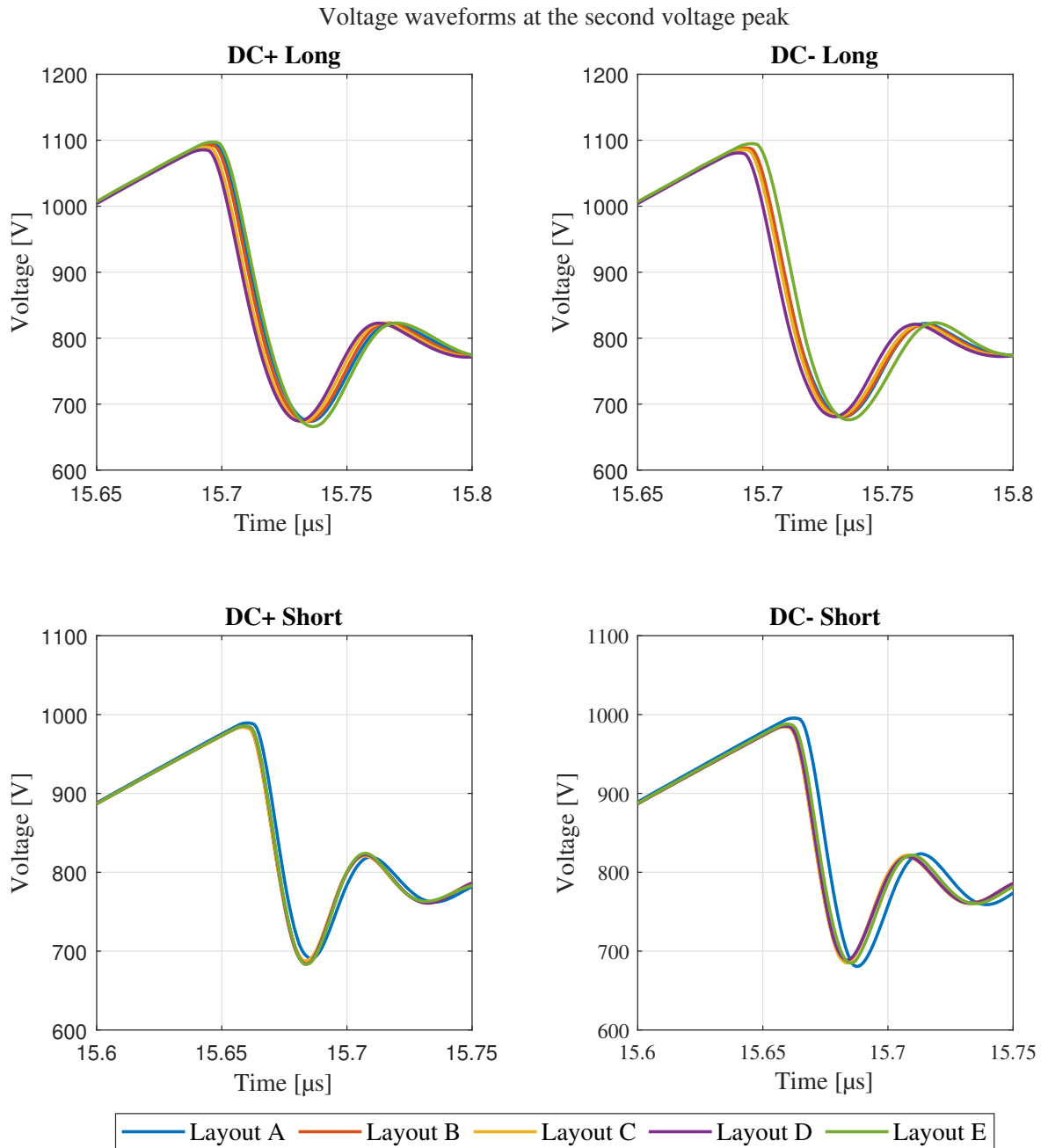
Figure 18: Voltage waveforms at the second voltage peak of the DPT from each commutation loop and for each busbar layout. Long and short loop figures have different time and voltage axes to better show the peak voltages in each case.

In Figure 18 small variations in the voltage peak amplitudes between the layouts are noticeable. The differences are more noticeable in the long loop voltage waveforms which is in line with the larger stray inductance variations in the long commutation loops loops. When comparing the order of the peak values to the simulated commutation loop inductances shown in Figure 15 it can be seen that the highest voltage peak amplitudes are in the layout E with highest stray inductances. The other peak values below that seem to also be in the order

of decreasing commutation loop inductance. However the difference between highest and lowest peak voltages is only around 15 volts.

Similar to the peak voltage amplitudes, the time instant the peak voltage is reached differs between the layouts. Layout D with lowest loop inductance reaches the peak voltage first and after that the other layouts in order of the loop inductances the layout E being last. This makes sense since in all of the simulations the same semiconductors were used so the systems should have nearly identical slew rates and therefore reaching the higher peak voltage takes a longer time.

The short loop inductance values are even closer to each other and correspondingly also the voltage waveforms are nearly identical. In both DC_+ and DC_- short loops the layout A's blue line is a little separated from the others which are for the most parts combined to one. The difference between long and short loop peak voltages is about $100\,\mathrm{V}$ which was expected since the inductance difference between the two of them is significant.

5.4   Future research

Based on the DPT simulations the designed busbar layouts have potential to be feasible as a phase-leg structures. Especially structures C, D and E were proven to be quite symmetric in terms of commutation loop inductances and simulated DPT waveforms. The busbar stackup should still be considered from the point of view of the whole converter DC link design to ensure that all of the DC_+, DC_- and DC_N busbars from the three-phases can be connected together and to the mutual DC link.

The inductance and DPT simulations were done with plate thickness of $2\,\mathrm{mm}$ which was guesstimated to be appropriate early at the design process. The dimensioning should be done to ensure that the cross sectional are of the busbars is enough and that as part of thermal simulations the busbar temperatures are okay. One related factor is the thermal properties of the insulation material used between the busbar layers. Insulator should be able to endure high temperatures and preferably have low thermal resistance to help remove the heat from the middle of the busbar stack (Popova et al., 2012).

The clearances for the bushings connecting the busbar layers to the power module terminals are currently too small to have just the air gap as an insulator as described in the section 4.2.3. Since in the selected $62\,\mathrm{mm}$ power module package the terminals are quite close together increasing the clearances might result in a loss of significant amount of the busbar cross sectional area. Also as researched in (Mitsui & Wada, 2022) the perforation clearance has an effect for the stray inductances of the busbar structures. For this module type it might

be necessary to consider some form of insulation material to be used in these perforations to reduce the needed perforation size like for example in (Gui et al., 2021).

In a (Gui et al., 2021) a quite systematical approach was shown for the busbar optimization of a three-level converter. Especially the process of identifying the commutation loops and the busbars in them could be tried also for this optimization case to see if the results are any different. Otherwise the described process were mostly in line with the ones used here. To ensure the accuracy of the simulations at some point a phase-leg prototype should be built and the loop inductances should be measured and DPTs done in a laboratory. Before the prototype phase however the busbar layout's suitability for the thee-phase system should be verified as explained above.

One step tied to both the phase-leg optimization and combining the three phase-legs into a three-phase converter is the design of the intermediate circuit. Each phase should have a low inductance path to the DC link and atleast one capacitor close to its DC_+ and DC_- connections. Intermediate circuit layout is researched for example in (Mattsson et al., 2022) from the point of view of the placement and orientation of the capacitors and in (Mitsui & Wada, 2022) from the point of view of the number of capacitors. Furthermore the used capacitor types need to be chosen, whether to use all film capacitor for lower parasitics or also cheaper electrolytic capacitors to provide the bulk capacitance.

6 Conclusions

A compact literary survey was done about NPC topology's commutation behaviour and bus-bar layout design fundamentals to first get an understanding of how stray inductances in a laminated busbar structure can be minimized and how to apply that to a NPC phase-leg. The key findings were to optimize the power module layout to get the corresponding terminals and DC link capacitor terminals as close together as possible and trying to keep the structure as symmetric as possible. With the NPC topology it's best to try minimize the long loop inductances since they are inevitably higher and therefore the ones which first cause any voltage overshoot problems.

To minimize the stray inductances from the laminated busbar structure the busbar layers should be as close together and have as much overlap as possible. The busbar layers should also be kept as continuous as possible and all unnecessary holes and sharp corners should be avoided. When considering the busbar stackup the current path and their return path busbars should be placed adjacent to each other. This sound obvious but is not always so straight forward with a multilevel converter topologies. The phase-leg structure of a multilevel converter is often complex with numerous commutation loops and with several connections to the DC link.

Based on a power module survey where one of the criteria was that the module is available from several manufacturers the 62 mm power module package was selected. Modules three power terminals are relatively close to each other which caused some challenges with clearances in connections through other busbar layers. Therefore with these bushing connections some additional insulator should be considered in addition to just air. If the perforations are made large enough for air insulation the busbar cross sectional area is considerably reduced. The chosen module package also has a rather high paracitic inductance which in this case was not an issue with the used IGBT technology but might be a problem with faster switches like SiC MOSFETs due to higher di/dt during switch turn-off.

In total five busbar designs were created and their performance was evaluated through stray inductance and DPT simulations done in Ansys Electronics desktop software. The busbar designs had some variation in the loop inductances between the different designs but also between the upper and lower commutation loops of a phase-leg. Based on the DPT simulations the inductance differences of couple of nanohenries led to peak voltage differences of around 10 volts in all of the long loops. Based on the DPT simulations all the proposed phase-leg layouts are feasible options for NPC topology with 1600 V DC link voltage and a phase-current of 400 A.

However more research is still needed before any of the proposed layouts can be used in an actual product. Their applicability for a three-phase converter structure needs to be assessed as well as the structure of the intermediate circuit. Current state of the shown busbar designs is more a proof of concept and they are nowhere near ready for production. At some point in the product development process the structure should be optimized to be assembled on a production line. This includes reducing the assembly steps to a minimum to make the manufacturing of the converter financially viable.

This thesis subject had an option to also make a laboratory prototype of a converter phase-leg and to compare the simulated results to the measured ones. Unfortunately that didn't happen as learning even the basics of busbar design and how to use the ANSYS software took a lot longer than anticipated and there were no time left for this. In the end taking the time with the busbar optimization and simulations rather than trying to rush to the prototype stage with half-finished busbar design was most likely the right decision.

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